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3D Atomic Scale Analysis of CMOS type structures for 14 nm UTBB-SOI technology

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As the dimensions of microelectronic devices are progressively reduced new architectures and materials are being introduced to try and meet ever stricter performance criteria. The use of high-k dielectrics (hafnium based oxides) can reduce leakage current leading to better electrical properties. The coupling of these dielectrics with metallic gate materials (TiN) has led to structures of greater complexity in CMOS (complementary metal oxide semiconductor) devices. Due to current dimensions (a few nanometres) atom probe tomography (APT) is one of the very few techniques which can give 3D chemical information at this scale [1-2]. But due to the insulating and high evaporation field nature of these materials analysis is often difficult, with very low analysis yields, or even impossible [3].

We here show that using simplified test structures it is possible to overcome these limitations and perform complete analysis of a finished gate stack, including source/drain regions. Although simplified, these structures are representative of current nanometre scale transistors, and give the opportunity to study the chemical composition of the final device. Analysis of both n and p-type 14/20nm structures have been performed by APT on both SOI and bulk silicon substrates, before and after a spike anneal.

The samples have followed a conventional gate first UTBB-SOI (ultra-thin body buried silicon-on-oxide) 14nm deposition flow up to silicide deposition. At this point manufacture has been halted and a 150 nm nickel layer deposited to facilitate specimen preparation by focused ion beam. By preparing the tips in different parts of the test zones, it is possible to obtain information about the gate stack or source/drain areas. The samples have then been analysed under pulsed UV laser until the SOI interface or Si substrate in the case of bulk samples.

The APT reconstructions have been calibrated using transmission electron microscopy (TEM) images. To improve the reconstructions, correlation between the APT element mapping and TEM tomography volumes has been made, thus reducing artefacts [4]. Once the structures were correctly reconstructed, localised chemical data could be extracted. Of particular interest is the dopant localisation after deposition and anneal. All dopants in the structures (arsenic, phosphorous and boron) have been mapped. Of these, the most interesting is boron, due to the impossibility to obtain this information via other characterisation methods. We show that the boron distribution follows an irregular profile, with a concentration maxima situated between the channel and epitaxial source/drain. Due to the fact that this distribution is already present before anneal, we attribute it to inhomogeneous boron incorporation during epitaxy of the source/drain regions. This has been compared with time-of-flight secondary ion mass spectroscopy measurements made on the same test structures and larger planar zones. There is a good agreement between the profiles, although a smaller amount of boron is detected by APT. This can be explained by a saturation of the APT detector and can be accounted for in post-treatment of the data.[5]

In conclusion, using simplified test structures and careful sample preparation it is possible to analyse a complete high-k metal gate device. Using complementary techniques on the same sample it is possible to obtain a better reconstruction and a more complete and quantitative picture of dopant distribution. An irregular boron distribution can thus be clearly observed.

References

[1] Thomas F. et al.,, Rev Sci Instrum **78**, (2007), 031101.
[2] F. Panciera, et al., Appl Phys Lett **100**, (2012), 201909.
[3] S. Jin et al.,. J Vac Sci Technol B **29**, (2011) 061203.
[4] A. Grenier et al., Ultramicroscopy **136**, (2014), 185.
[5] This study has been performed at the nanocharacterisation platform (PFNC) of the Minatec Campus and ST Microelectonics, Crolles. The author would like to acknowledge a CIFRE (ANRT) scholarship.

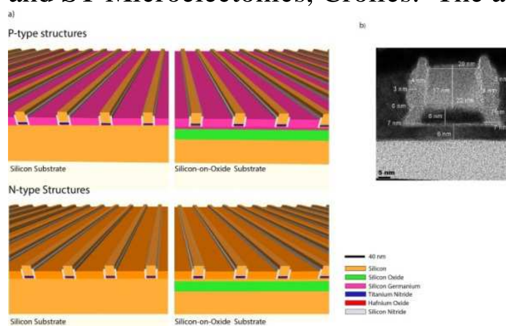

Figure 1. (a) Schematic representation of test structures, showing the extended nature of the gate-stacks. (b) TEM micrograph of p-type stack on SOI substrate

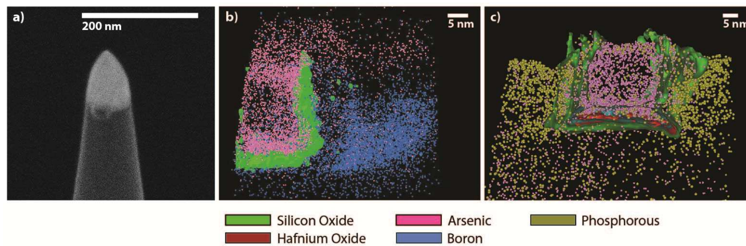

Figure 2. (a) Atom probe tip prepared by FIB and reconstructions of both p-type (b) and n-type (c) on bulk silicon substrate.

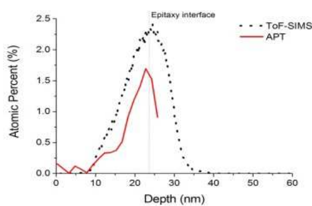

Figure 3. Comparison of Boron concentration profiles extracted from source/drain area by APT and ToF-SIMS after spike anneal.