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Time-Resolved Imaging of Electrochemical Switching in Nanoscale Resistive Memory Elements

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FLASH memory is reaching its scaling limit, but resistive random access memory (ReRAM) is considered a promising successor [1]. In ReRAM, metal electrodes sandwiching an insulating electrolyte form a digital memory element, where the presence or absence of a conducting path through the insulator represents one bit of information. The conducting filament is thought to form, atom-by-atom, when subject to a SET voltage applied across the electrodes, and to disintegrate when subject to a RESET voltage. We use scanning transmission electron microscopy (STEM) to image nanoscale ReRAM devices switching *in situ*. Operating the devices with small current limits slows the rate of filament formation and reduces confounding thermal effects, allowing us to obtain time-resolved images of filament formation and regeneration.

We fabricated Pt/Al_2O_3/Cu ReRAM devices with a slant-vertical geometry. The "slant" gives good imaging access, while keeping the electrodes completely encased to ensure that conducting filaments form though the Al_2O_3 layer (as in the standard vertical geometry) and not across exposed surfaces or layer interfaces [2]. Figure 1a shows a STEM image of a pristine device, and Fig. 1b shows the same device after a 4.4 V SET bias has been applied. Applying the SET caused the current to jump to the 50 nA compliance limit as the device switched from its ~10 GΩ OFF state to a ~20 MΩ ON state. The STEM images show that, coincident with the SET, the device developed a 5 nm wide Cu filament connecting the electrodes. After a -4V RESET, the device was cycled repeatedly between the ON and OFF states. The low current compliance regulated the rate of the switching processes so that the SET and RESET processes could be time-resolved: each was imaged over several frames. The electronic and imaging data acquired under these conditions corroborate the electrochemical model for switching [3].

Devices tested with higher current limits showed evidence of heating during SET. Figures 1c-e show STEM images of devices that were switched with SET bias voltage values comparable to those of the device in 1a-b, but with current limits ranging from 100 nA to 700 nA (i.e. 2 to 14 to times larger). The resulting filaments are much wider than the filaments formed during low current SETs, and the ON resistances are < 1 kΩ. The electrodes exhibit reconfiguration and recrystallization consistent with heating to temperatures near their respective melting points. However, the programmed current limit values used are still small enough that such high temperatures are unexpected. RESETs following such large-current SETs could require more than 1 mA, which often resulted in device failure (Fig. 1f).

Using the larger compliance currents decreases the ON-state resistance R_{ON}, which allows transient currents larger than the compliance current limit to flow. These currents are sourced by stray capacitance C in the circuit, and can Joule-heat the device by hundreds of kelvins. A simplified circuit model of the ReRAM biasing setup is shown in Fig. 2. The time constant for the system is $\tau \sim C R_{ON}$,

and the maximum current $I \simeq Q/\tau \simeq CV/\tau \simeq V/R_{ON}$. Therefore, the maximum power through a device during an ON switch is $IV = V^2/R_{ON}$. For a device with a R_{ON} = 1 kΩ, the ≳1 mW SET heats the device above a thermal threshold. In comparison a R_{ON} = 10 MΩ device switches with 100 nW and remains near room temperature. Small compliance currents thus enable time-resolved imaging of ReRAM cycling *in situ*.

References:
[1] I. Valov *et al*, Nanotechnology **22** (2011), p. 289502
[2] W. Hubbard *et al*, Microscopy and Microanalysis **20** (2014), p. 1550-1551
[3] S. Menzel *et al*, Physical Chemistry Chemical Physics **20** (2013), p. 6945
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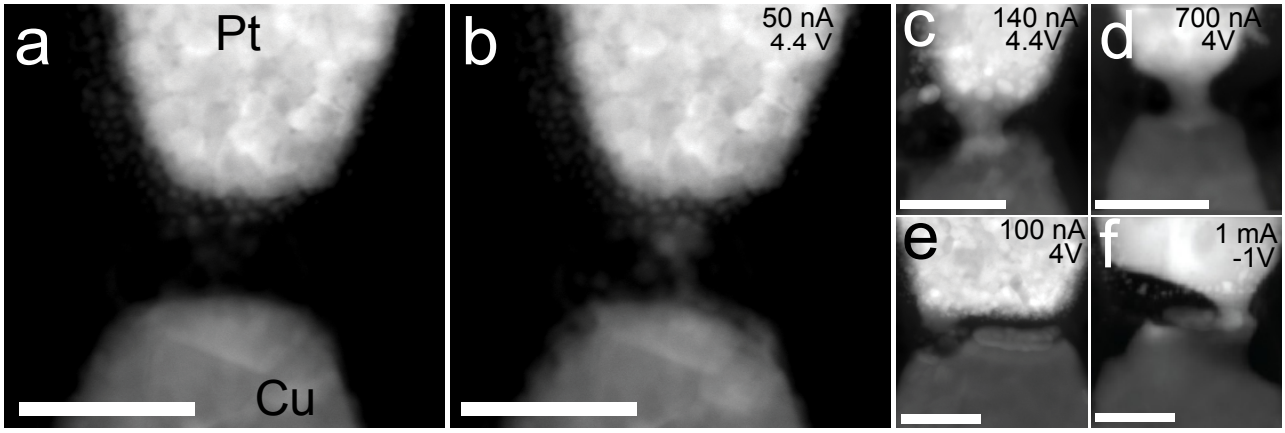

Figure 1. STEM images of a slant-vertical ReRAM device before (**a**) and after (**b**) its first SET (voltage and current limit shown). Similar devices (**c-e**) that were switched with larger current limits produced burlier connections with poorer cycling endurance. For instance, **f** shows the **e** device after a RESET attempt failed to change the device state to OFF. The scale bar in all images is 50 nm.

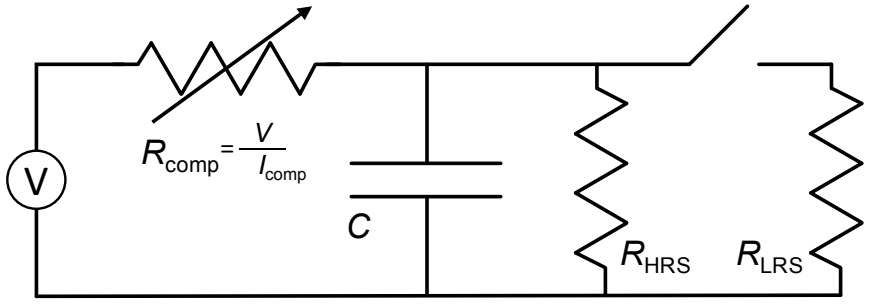

Figure 2. Circuit model of ReRAM device biasing. The resistance R_{comp} is determined by the programmed current compliance I_{comp}. The ON state device resistance R_{ON}, a function of I_{comp}, decreases rapidly once I_{comp} exceeds a thermal threshold value that in our devices is ≲ 100 nA.