Summary of Selected EMCR650/731 Projects for 2004-2005

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3-2-2005 650Projects04.ppt

INTRODUCTION

Each of the students in EMCR650 and EMCR732 are asked to do a process improvement project to make the student factory better. In place of a final exam they present their project results.

Students in EMCR731 did a observational study of particulate contamination in some of the tools in the laboratory.

This document is a summary of some of their presentations.

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OUTLINE

Introduction
Thin Gate Oxide Growth by Rapid Thermal Processing (RTP)
Ion Implant Masking Calculator
Maximum Ion Implant Beam Current without Photoresist Damage
Wet Etch of Small Contact Cuts
Observations of Problems with Aluminum Plasma Etch
Simulation of Well Implant Before STI Trench Fill Compared to
    Well Implant After STI Trench Fill
Verification of Oxide Side Wall Spacer Formation

THIN GATE OXIDE GROWTH BY RAPID THERMAL PROCESSING (RTP)

From Textbook by S. Wolf

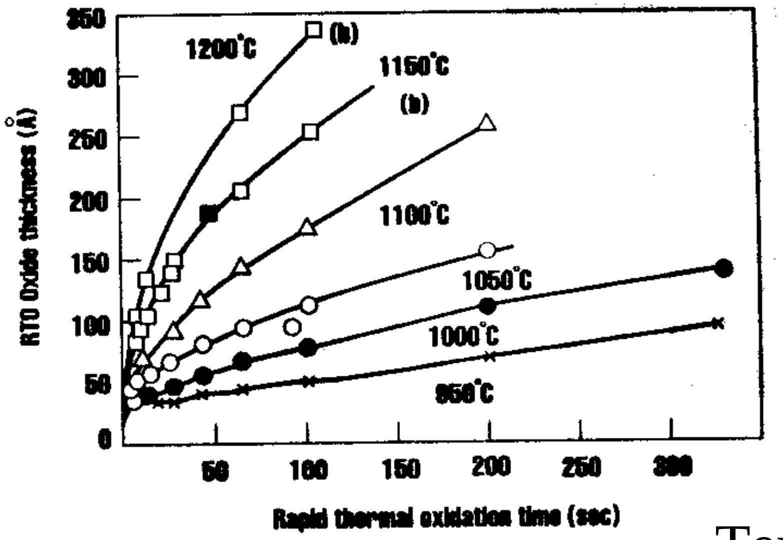
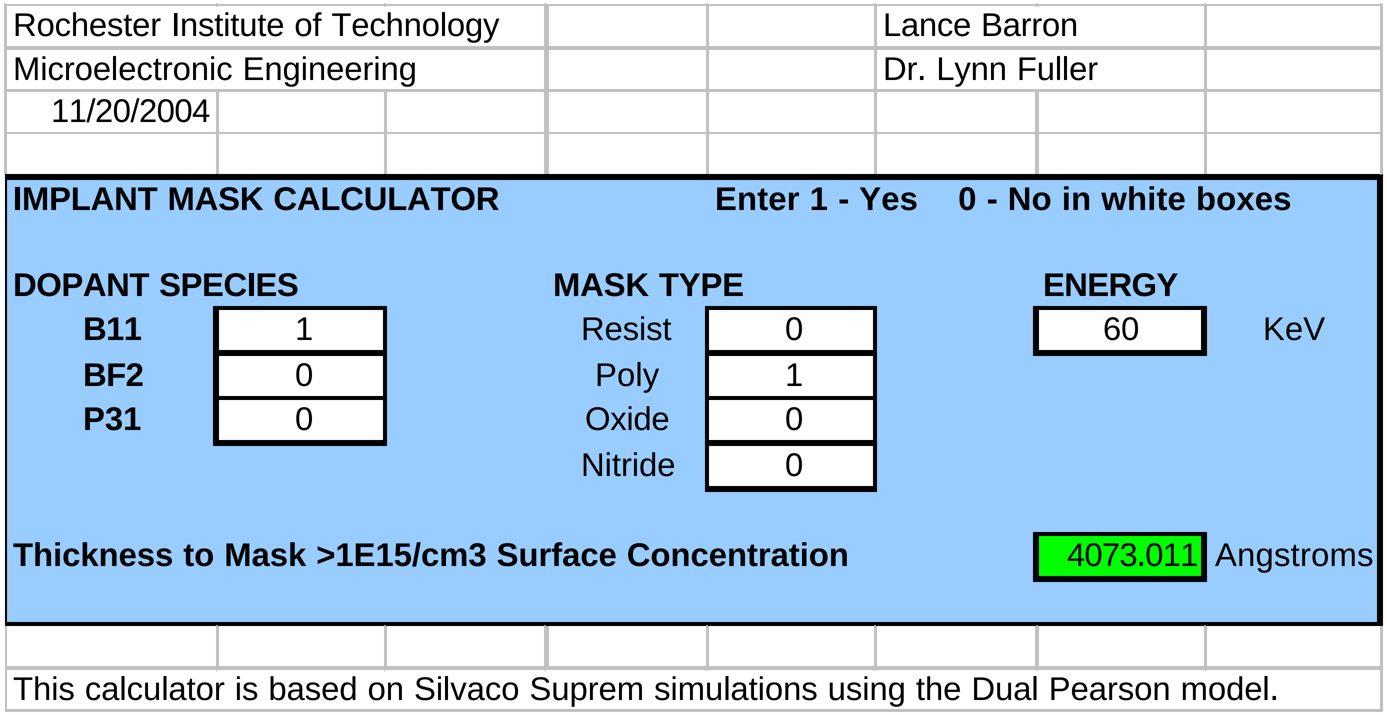


Figure 6-13 Typical data for oxide thickness as a function of time for a rapid thermal oxidation process (*after Moslehi et al., 1985*).

Textbooks say that 150Å of oxide can be grown by RTP at 1100°C in 60 sec. We tried to duplicate this at RIT but we have not been successful yet.

Sébastien Michel, February 2005

ION IMPLANT MASKING CALCULATOR



Rochester Institute of Technology	Lance Barron
Microelectronic Engineering	Dr. Lynn Fuller
11/20/2004	

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		**MASK TYPE**		**ENERGY**	
B11	1	Resist	0	60	KeV
BF2	0	Poly	1		
P31	0	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 4073.011 Angstroms

This calculator is based on Silvaco Suprem simulations using the Dual Pearson model.

In powerpoint click on spread sheet to change settings for a new calculation

Lance Baron, Fall 2004

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VARIAN 350D MAX IMPLANT CURRENT WITHOUT PHOTORESIST DAMAGE

The objective of this project is to experimentally determine the maximum ion implanter (Varian 350D) beam current for large 4E15 dose implants that does not cause photoresist (OIR620 & COAT.RCP) damage.

Steve Parshall
Winter 2004-05

Tool donated by Agere
Installation donated by Varian

VARIAN 350D MAX IMPLANT CURRENT WITHOUT PHOTORESIST DAMAGE

Species	Dose (ions/cm2)	Energy (KeV)	Current (uA)	Implant Time (min)	Photoresist Integrity
P31	4E15	120	200	10.47	Good
P31	4E15	120	300	6.98	Damaged
P31	4E15	120	450	4.65	Damaged
P31	4E15	100	200	11.35	Good
P31	4E15	100	250	9.1	Good
P31	4E15	100	285	7.48	Good

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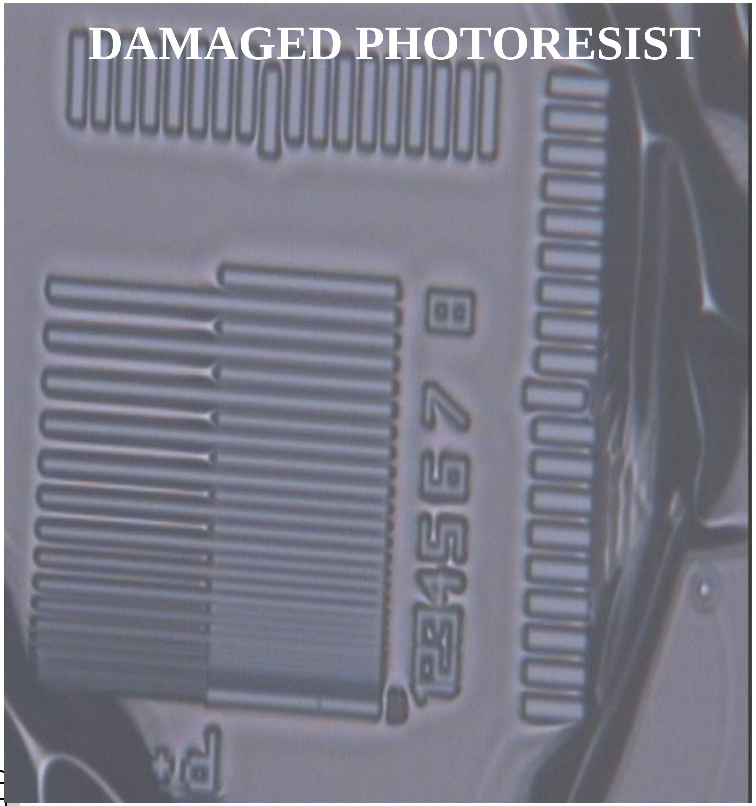
VARIAN 350D MAX IMPLANT CURRENT WITHOUT PHOTORESIST DAMAGE

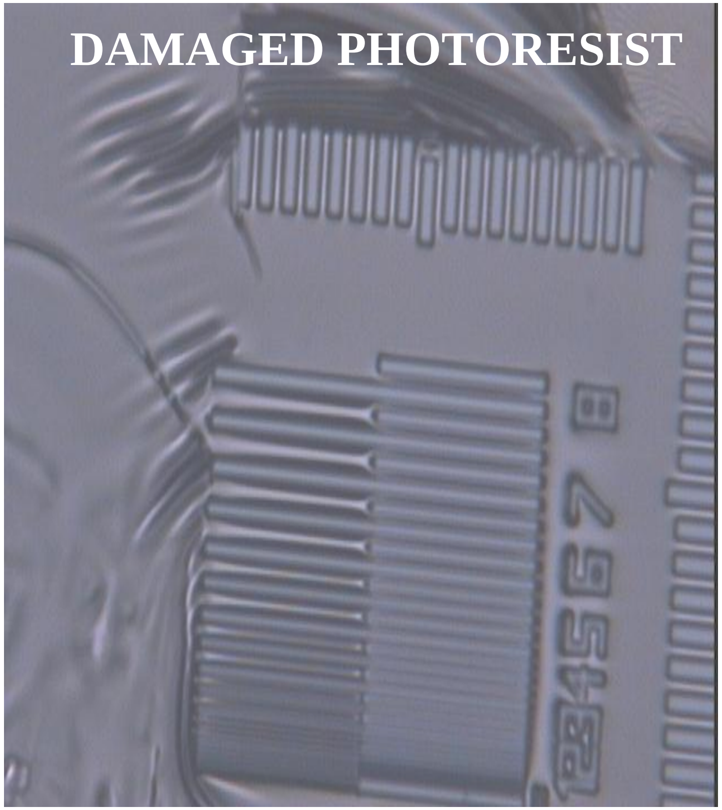
Species	Dose (ions/cm2)	Energy (KeV)	Current (uA)	Implant Time (min)	Photoresist Integrity
B11	1E15	50	100	5.23	Good
B11	1E15	50	200	2.62	Good
B11	1E15	50	380	1.5	Good

Species	Dose (ions/cm2)	Energy (KeV)	Current (uA)	Implant Time (min)	Photoresist Integrity
B11	4E15	120	100	5.23	Good
B11	4E15	120	200	2.62	Good
B11	4E15	120	275	1.97	Good

VARIAN 350D MAX IMPLANT CURRENT WITHOUT PHOTORESIST DAMAGE

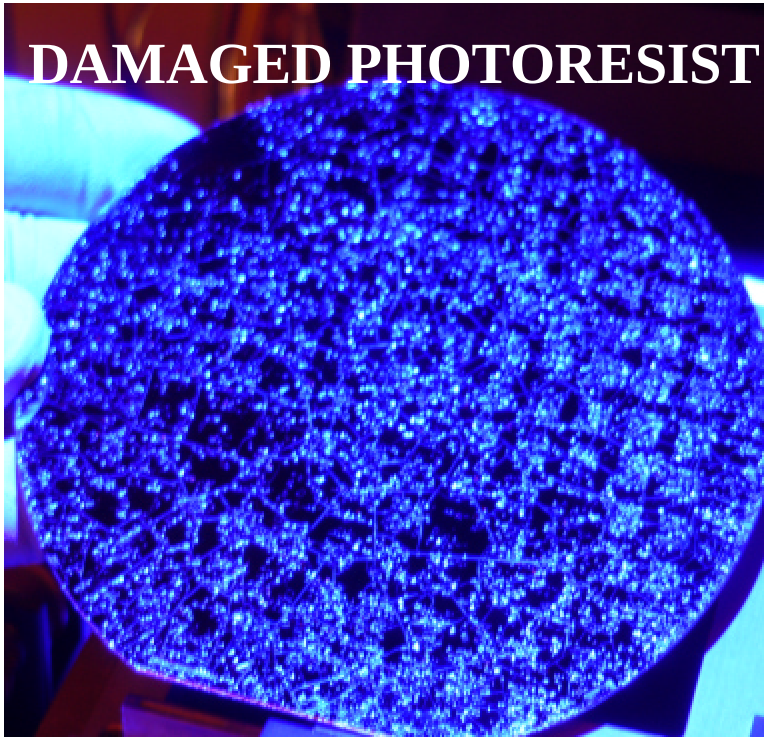


300 uA P31 Implant
Dose = 4E15 cm-2



450 uA P31 Implant
Dose = 4E15 cm-2

VARIAN 350D MAX IMPLANT CURRENT WITHOUT PHOTORESIST DAMAGE



P31 450uA Implant, Dose = 4E15 cm-2
Energy = 120KeV

VARIAN 350D MAX IMPLANT CURRENT WITHOUT PHOTORESIST DAMAGE

Conclusion

For lower implanted doses of 1E15 ions/cm2 and below, maximum beam current for the Varian ion implanter of 350uA may be used for both B11 and P31 species.

For higher doses (4E15 ions/cm2) of P31 and B11 dopants used in the S/D CMOS implants, the maximum beam currents are approximately 285uA and 275uA.

We recommend setting beam currents less than 250uA to avoid damaged photoresist

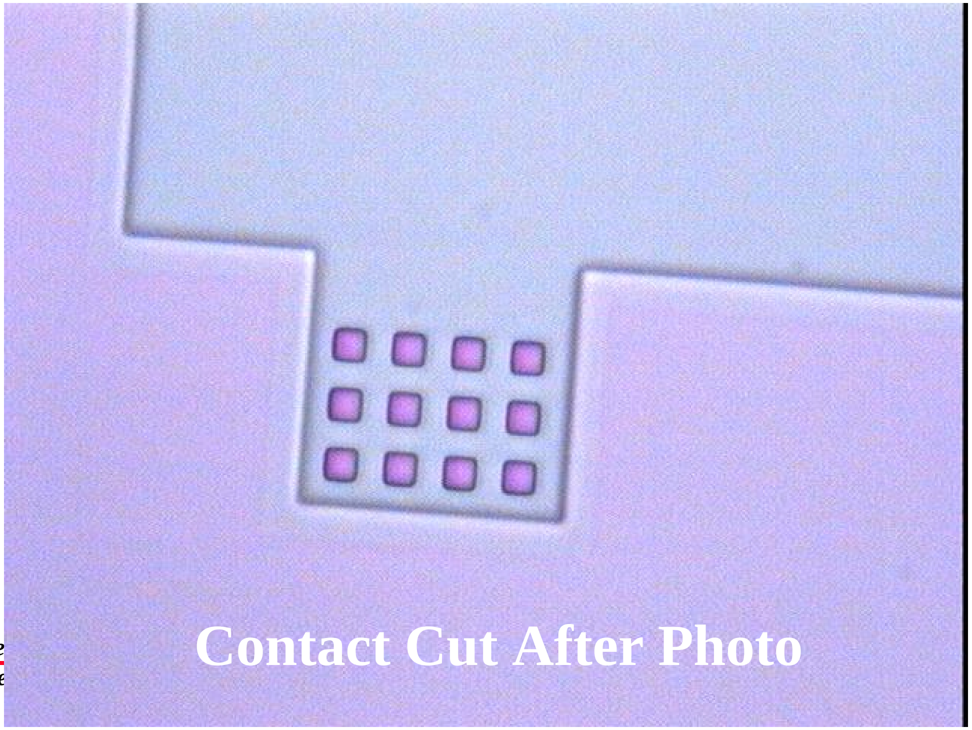
MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH

Contact Cut Lithography is difficult because of the complicated film stack. The contacts are through 4000Å TEOS oxide on thermal oxide on poly on gate oxide. The poly has a silicide layer in the Advanced CMOS process. The poly thickness might be 4000Å or 6000Å. The TEOS may be annealed. Other contacts are to drain and source through 4000Å TEOS on thermally grown oxide of ~500Å (from poly reox step) plus gate oxide. The gate oxides are 330Å, 150Å, or 100Å depending on the exact process.

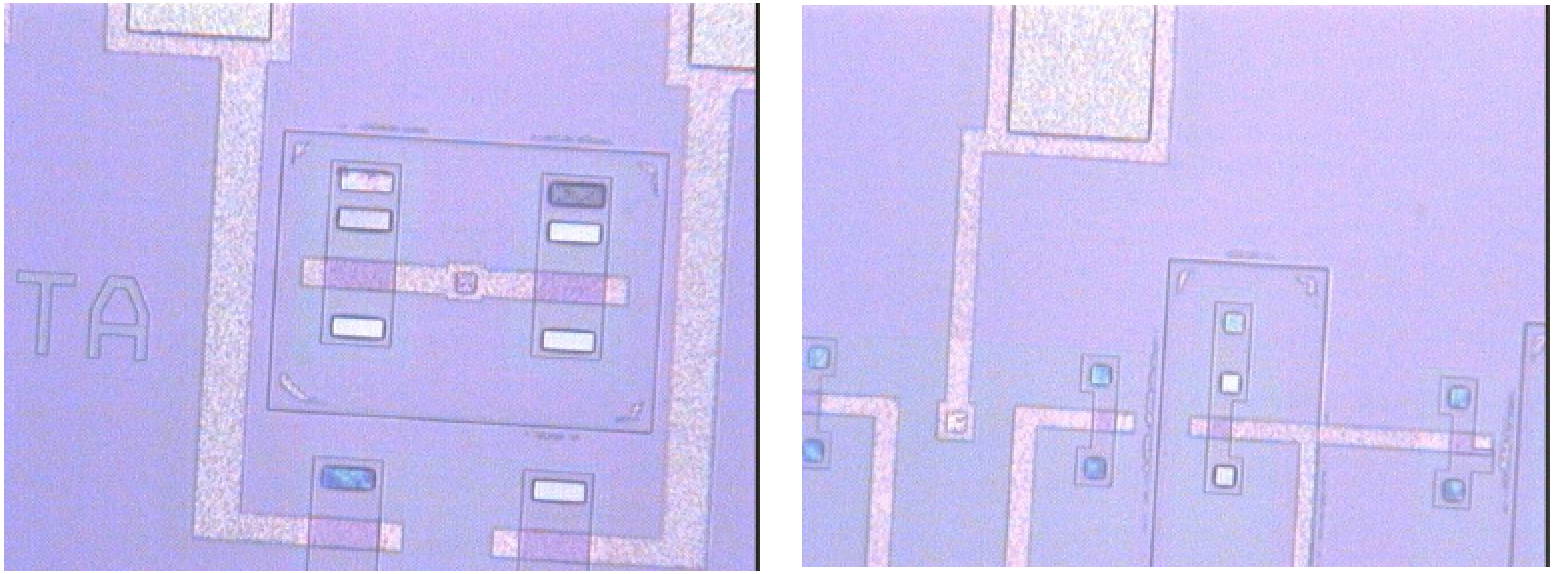
Contact cut etch is also difficult. Plasma etch is difficult because of the different oxide layers and thickness and the poor selectivity between etching oxide and the underlying poly or drain/source silicon. Wet etch has problems with blocking. That is where the BOE can not get into the small contact cut openings. Blocking depends on surface tension as measured by the wetting angle which depends on the type of photoresist used.

MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH

To ensure that the photoresist is cleared in the bottom of all the contact cuts the exposure dose is increased to 285 mj/cm2 and track develop time is increased to 3 min. This makes the 2µm x 2µm contacts a little larger ~2.2µm by ~2.2µm but they are clear regardless of the underlying film stack.

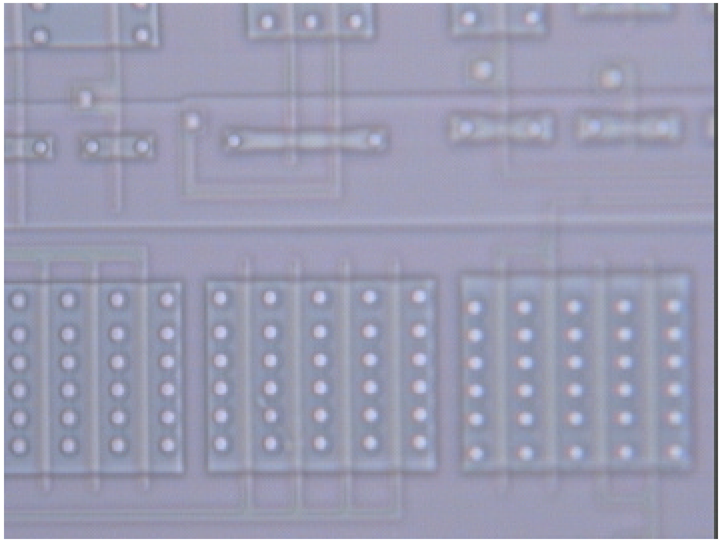


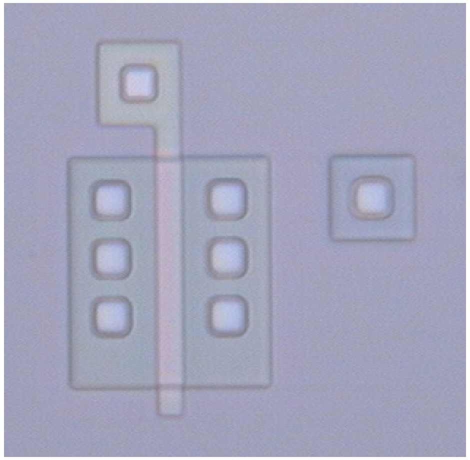
MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH



Wet etch has problems with blocking. That is where the BOE can not get into the small contact cut openings. Blocking depends on surface wetting angle. If blocking occurs some contact cuts will etch and clear while others will not etch as illustrated in the pictures above.

MAKING SMALL (2µm x 2µm) CONTACT CUT BY WET ETCH

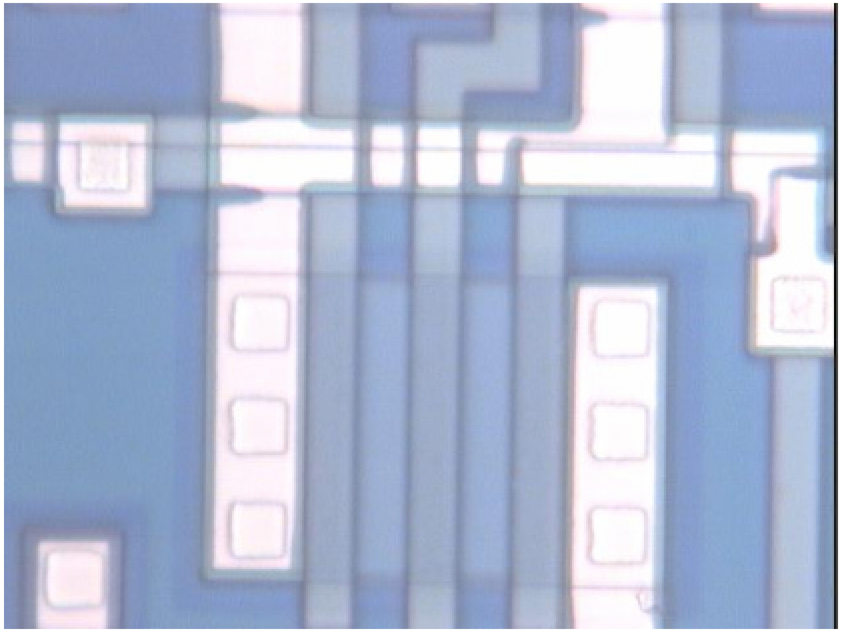




To overcome the blocking problem we raised the boat completely out of the BOE every 15 seconds throughout the entire etch. To be sure to clear all the contacts the etch time was extended to 5 minutes (approximately twice the expected etch time based on etch rates and approximate film thicknesses) This approach gave excellent results for all the various film stacks as shown in the pictures above.

1st LAYER ALUMINUM PHOTO

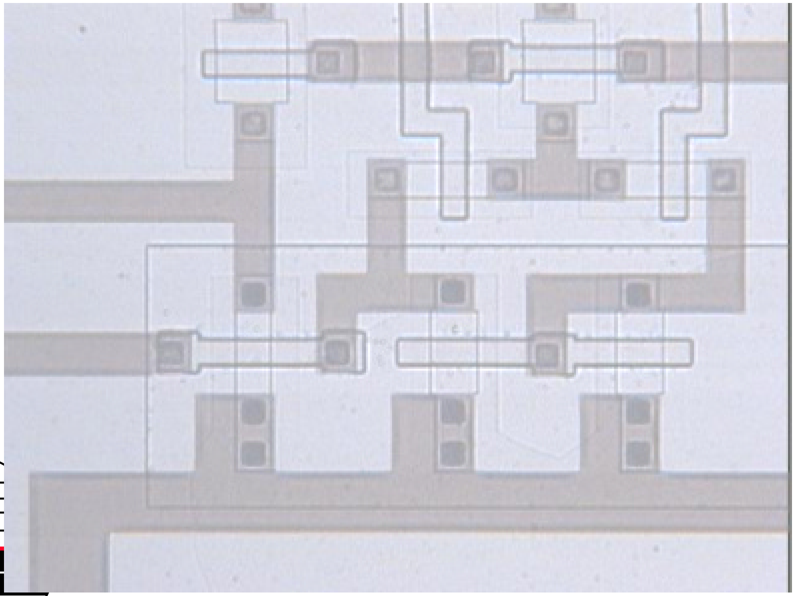
The 1st layer aluminum photo is difficult because there is topology on the wafer. The standard photoresist coat recipe COAT.RCP gives a resist coating of about 1.0 µm thickness. This is not thick enough to give good coverage at the edges of topography resulting in aluminum notching and broken lines as shown in this picture.



1st LAYER ALUMINUM PHOTO

Dan Jaeger
Fall 2004

To overcome this problem a new coat recipe to give thicker resist coating was created. A new develop recipe was also needed since the resist is thicker. The results are excellent as shown in the picture below.



Coat (Recipe: CoatMtl.rcp)
400RPM for 2 seconds
2000RPM for 30 seconds
Thickness of 13127A

Exposure
Energy: 140mJ/cm2
Focus: 0.24um

Develop (Recipe: DevMtl.rcp)
Dispense 7 seconds
Wait 120 seconds

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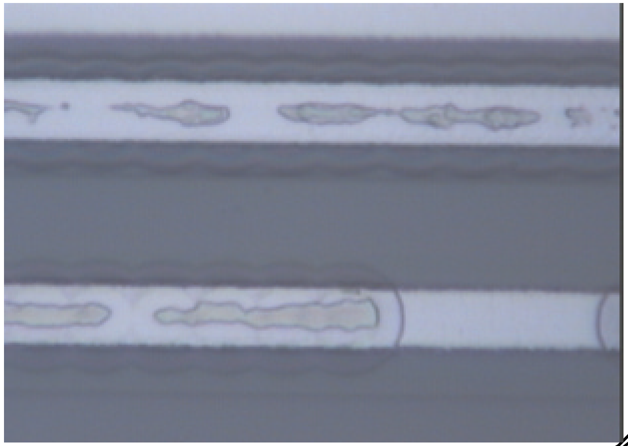
LAM4600 ALUMINUM ETCH OBSERVATIONS

Plasma aluminum etch is the preferred approach for CMOS manufacturing today. The Lam4600 is a chlorine Reactive Ion Etcher with endpoint detection capability. The student factory is starting to use this tool for its CMOS manufacturing. There were several observations made.

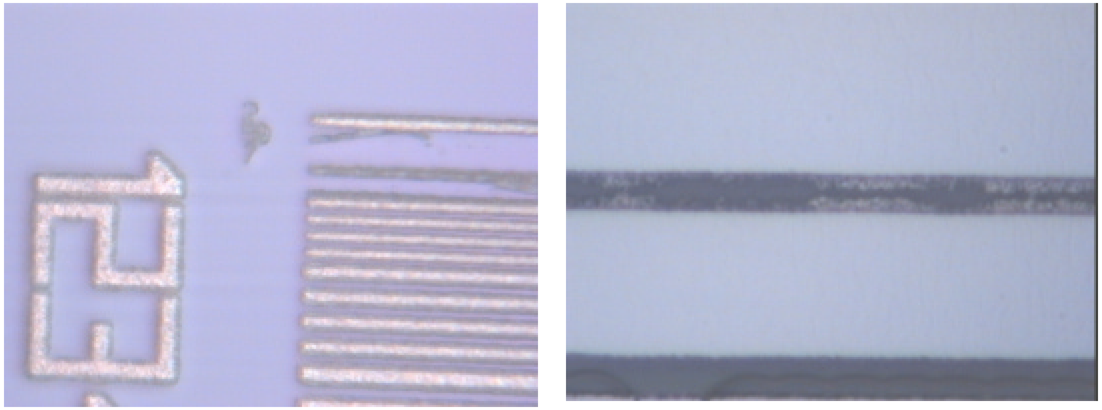
1. Resist is Harder to Remove in the Branson Asher
2. The Current Recipe Causes Significant Photoresist Damage
3. The Photoresist Damage Results in Aluminum "Crud" Around the Features

Resist Scum left after 6" Hard Ash Recipe
(New 6" Factory Recipe Removes This)

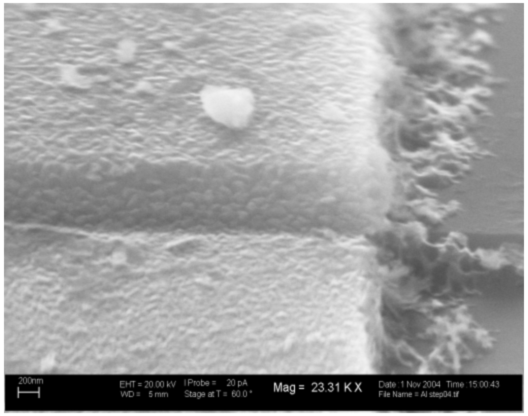


LAM4600 ALUMINUM ETCH OBSERVATIONS

Optical pictures showing aluminum “crud” after etch and resist strip



SEM pictures showing aluminum “crud” after etch and resist strip



LAM4600 ALUMINUM ETCH OBSERVATIONS

Old Aluminum Etch Recipe for Lam4600 (Recipe 1)

Step	1	2	3	4	5
Pressure (mtorr)	300	300	300	300	0
RF Top (W)	0	0	0	0	0
RF Bottom (W)	0	350	275	275	0
Gap (cm)	3	3	3	3	5.3
N2	25	25	40	50	50
BCl3	100	100	50	50	0
Cl2	10	10	60	45	0
Ar	0	0	0	0	0
CFORM	15	15	15	15	15
Complete	Stabl	Time	endpoint	Oetch	time
time (s)	15	8	120	25%	15

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LAM4600 ALUMINUM ETCH OBSERVATIONS

To address the photoresist damage problems and aluminum “crud” we made the following changes.

1. The photoresist was hard baked longer (increased bake from 1 to 2 min at 120 °C). (DEVMTL.RCP)
2. The etch recipe was modified to be less aggressive by decreasing the power in step 2 from 350w to 250w, and in step 3&4 from 275w to 125w. The new recipe is shown below

Step	1	2	3	4	5
Pressure (mtorr)	300	300	300	300	0
RF Top (W)	0	0	0	0	0
RF Bottom (W)	0	250	125	125	0
Gap (cm)	3	3	3	3	5.3
N2	25	25	40	50	50
BCl3	100	100	50	50	0
Cl2	10	10	60	45	0
Ar	0	0	0	0	0
CFORM	15	15	15	15	15
Complete	Stabl	Time	endpoint	Oetch	time
time (s)	15	8	120	25%	15

LAM4600 ALUMINUM ETCH OBSERVATIONS

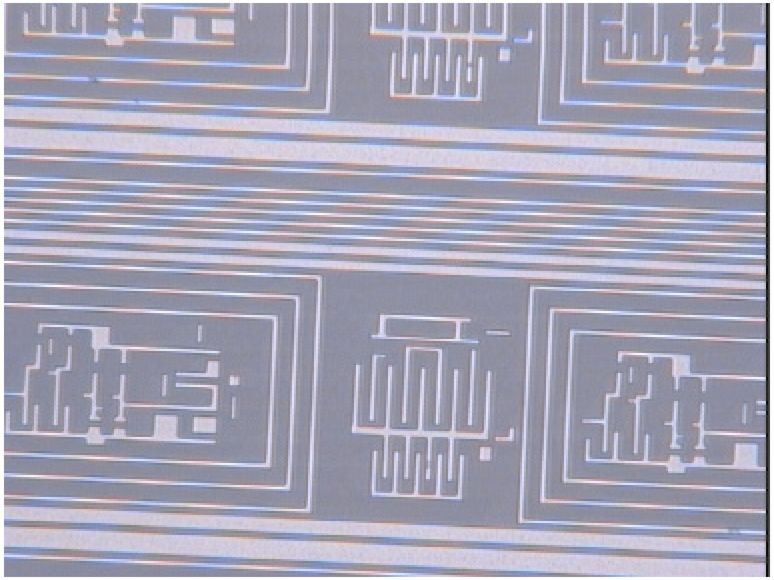
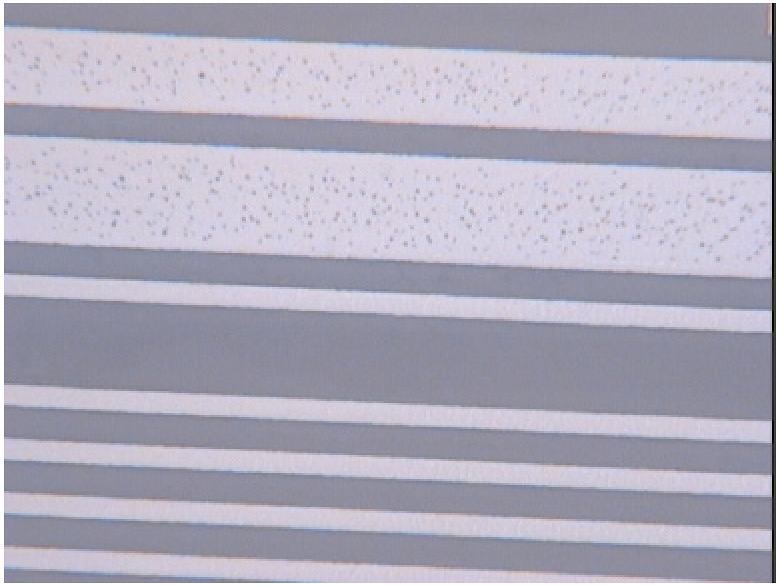


Image showing good line definition



No Aluminum "crud" noticed with the reduced power recipe

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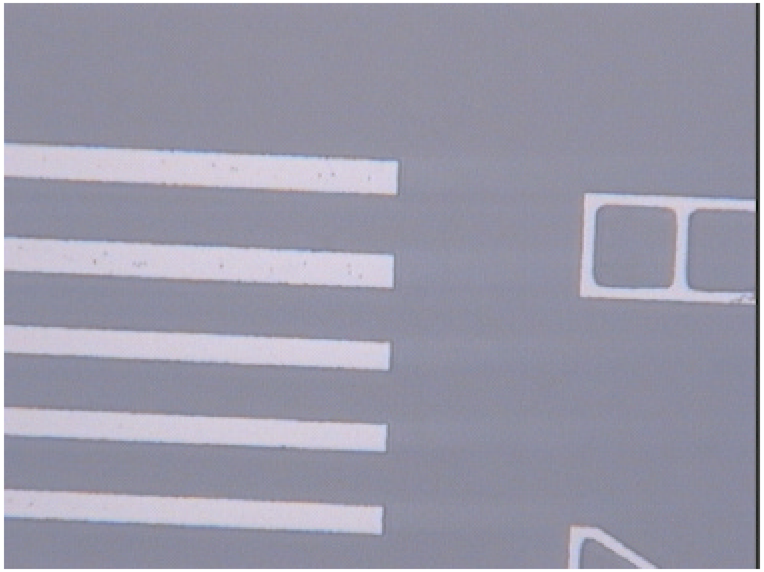
LAM4600 ALUMINUM ETCH OBSERVATIONS

- The Old Recipe 1 does NOT endpoint correctly, and runs the entire 120s.
- The resist is significantly damaged and reflows, causing significant "crud" between the lines.
- The New reduced power recipe also does not endpoint correctly and runs the entire 120s. There is significant over etch as shown in the picture.
- The resist is not as damaged, does NOT reflow.
- To optimize this process, the endpoint needs to be set up correctly. If endpoint fails the maximum time should be set less than 120s.

8µm mask defined feature measuring 5.6µm (over etched)



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ALTERNATIVE APPROACH FOR WELL FORMATION IN ADVANCED CMOS PROCESS

The current Adv-CMOS process calls for ion implanting the well through the filled trenches. This requires exact trench depths, exact CMP stop, and high energy implants. The normal photoresist is not thick enough to block these high energy implans, 180KeV for P31 and 150KeV for B11. This project investigated implanting the wells prior to trench fill and CMP. Using SILVACO ATHENA simulations a set of implant conditions was determined to give a well with the correct surface concentration, well junction depth and sheet resistance. The wells also need to be continuous under the trench isolation so that several devices can be placed in a single well with a single well potential. In addition our ion implanter has difficulty at high energy so lower energy implants would be useful.

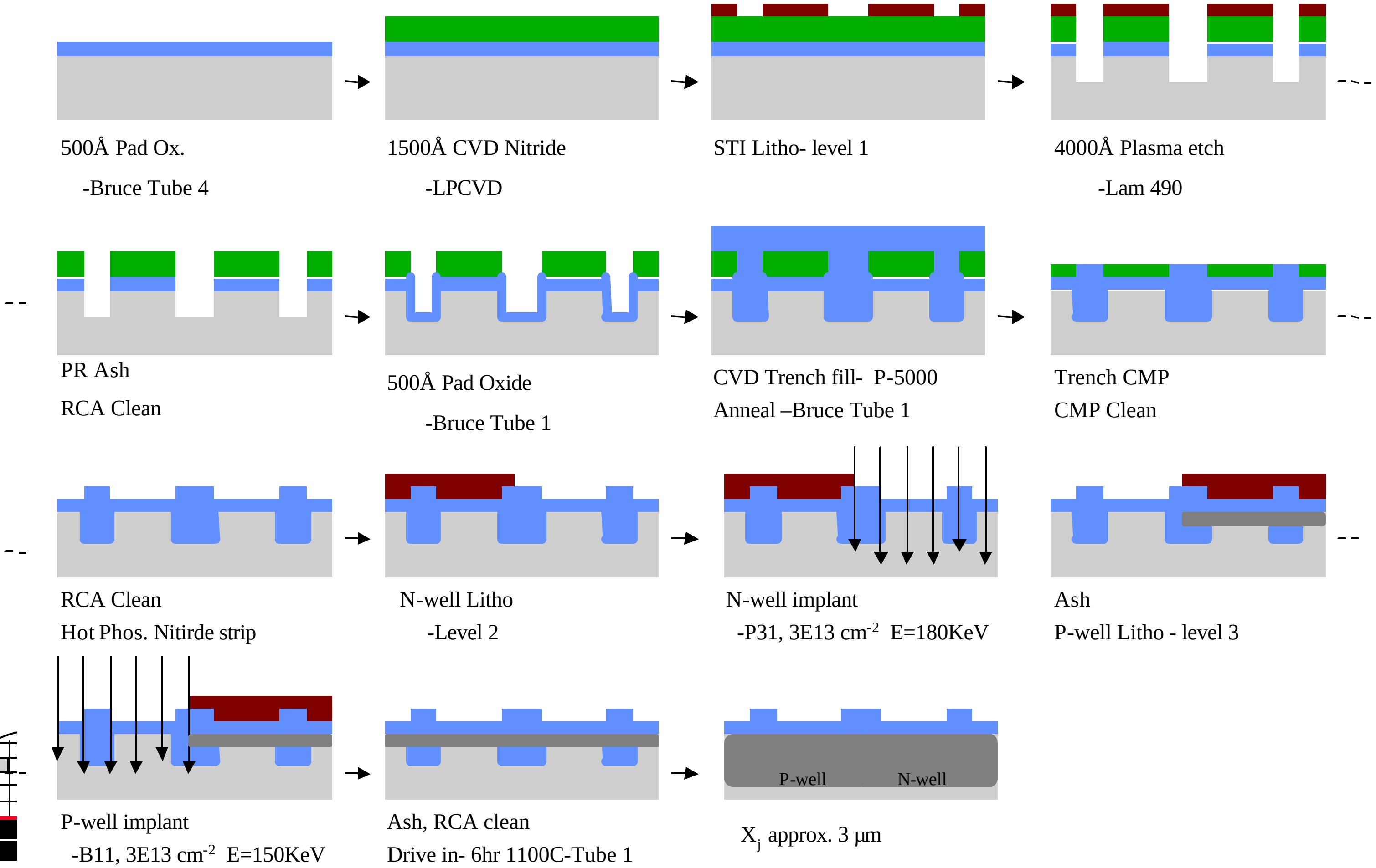
Jonathan Reese
February 22, 2005

WELL PARAMETERS

	Design Parameters	Old Process Simulation	New Process Simulation	
N well				
Dose	**3E13**	**3E13**	**3E13**	
Energy		**180**	**170**	**Lower**
Surface Conc.	**~1E17**	**2.4E17**	**1.08E17**	**Better**
N well Xj	**~3.0**	**4.0#**	**3.5**	**Better**
P well				
Dose	**3E13**	**3E13**	**8E13**	
Energy		**150**	**80**	**Lower**
Surface Conc.	**~1E17**	**3.6E16**	**1.0E17**	**Better**
P well Xj	**~3.0**	**3.3**	**3.1**	**Better**

* From integration of final well dopant profile
# If Boron penetration into N-well can be eliminated

ORIGINAL ADV-CMOS PROCESS FLOW



500Å Pad Ox.
-Bruce Tube 4

1500Å CVD Nitride
-LPCVD

STI Litho- level 1

4000Å Plasma etch
-Lam 490

PR Ash
RCA Clean

500Å Pad Oxide
-Bruce Tube 1

CVD Trench fill- P-5000
Anneal –Bruce Tube 1

Trench CMP
CMP Clean

RCA Clean
Hot Phos. Nitirde strip

N-well Litho
-Level 2

N-well implant
-P31, 3E13 cm^{-2} E=180KeV

Ash
P-well Litho - level 3

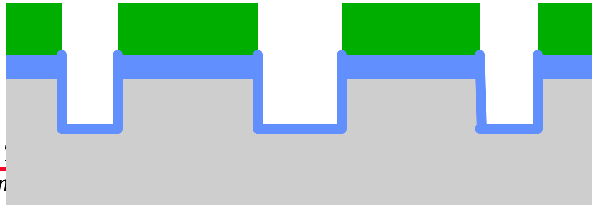
P-well implant
-B11, 3E13 cm^{-2} E=150KeV

Ash, RCA clean
Drive in- 6hr 1100C-Tube 1

X_j approx. 3 µm

SAMPLE WELL IMPLANT SIMULATIONS

		N-well						P-well		
Energy (KeV)	**Dose /cm2**	**Nsur (P) /cm2**	**Nsur (B) /cm2**	**Rs ohm-cm**		**Energy (KeV)**	**Dose /cm2**	**Nsur (B) /cm2**	**Nsur (P) /cm2**	**Rs ohm-cm**
60	3.00E+13	4.45E+14	2.70E+07	29998.8		40	3.00E+13	8.26E+12	4.45E+14	30398
70	3.00E+13	4.46E+14	4.22E+10	29820		50	3.00E+13	1.34E+15	4.45E+14	31305
80	3.00E+13	5.30E+14	6.29E+11	29238		60	3.00E+13	1.86E+16	4.45E+14	2104
90	3.00E+13	7.56E+14	1.45E+12	27175		70	3.00E+13	3.84E+16	4.45E+14	1145
110	3.00E+13	3.93E+15	1.66E+12	11936		80	3.00E+13	4.25E+16	4.45E+14	917
130	3.00E+13	1.89E+16	1.65E+12	2999		90	3.00E+13	4.04E+16	4.46E+14	838
150	3.00E+13	5.55E+16	1.82E+12	1116.54		100	3.00E+13	3.98E+16	4.52E+14	814
170	3.00E+13	1.08E+17	1.83E+12	641		110	3.00E+13	4.16E+16	4.63E+14	804
170	3.00E+13	1.08E+17	3.19E+12	641		110	5.00E+13	7.10E+16	4.62E+14	569
180	3.00E+13	1.34E+17	5.51E+12	539		110	8.00E+13	1.17E+17	4.69E+14	426
180	5.00E+13	2.22E+17	1.33E+14	390		120	8.00E+13	1.19E+17	4.83E+14	419
180	8.00E+13	3.52E+17	6.24E+12	300		110	1.00E+14	1.49E+17	5.00E+14	373
180	1.00E+14	4.38E+17	2.29E+14	275		110	5.00E+13	7.40E+16	5.85E+13	557
170	1.00E+14	3.50E+17	1.81E+12	314		110	4.00E+14	5.87E+16	4.52E+13	643
170	1.00E+14	3.52E+17	1.81E+12	305		80	3.00E+13	4.25E+16	4.45E+14	917
							Final Xj	2.92 um		



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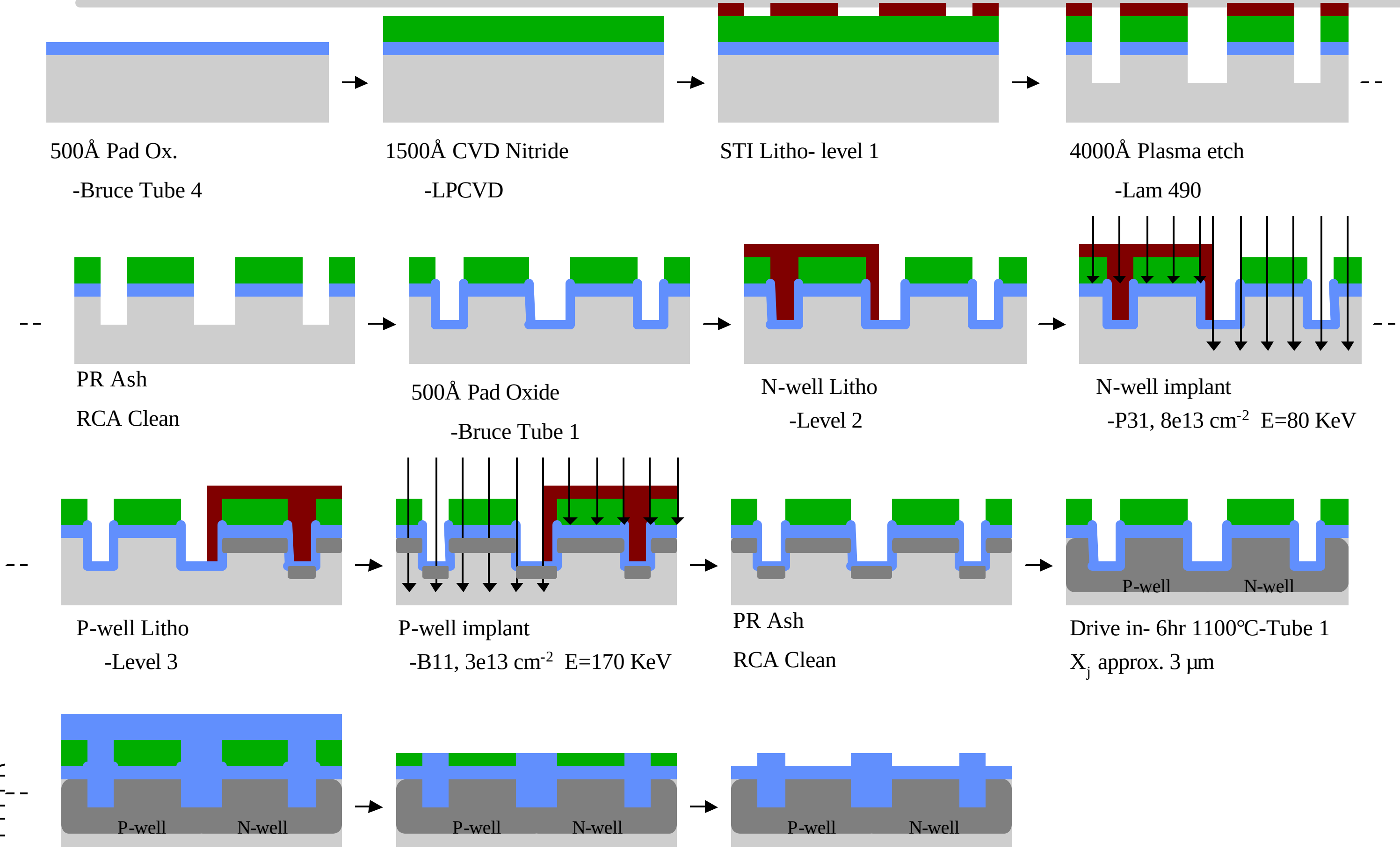
Microelectronic Engin

PROPOSED ADV-CMOS PROCESS FLOW



500Å Pad Ox.
-Bruce Tube 4

1500Å CVD Nitride
-LPCVD

STI Litho- level 1

4000Å Plasma etch
-Lam 490

PR Ash
RCA Clean

500Å Pad Oxide
-Bruce Tube 1

N-well Litho
-Level 2

N-well implant
-P31, 8e13 cm^{-2} E=80 KeV

P-well Litho
-Level 3

P-well implant
-B11, 3e13 cm^{-2} E=170 KeV

PR Ash
RCA Clean

Drive in- 6hr 1100°C-Tube 1
X_j approx. 3 µm

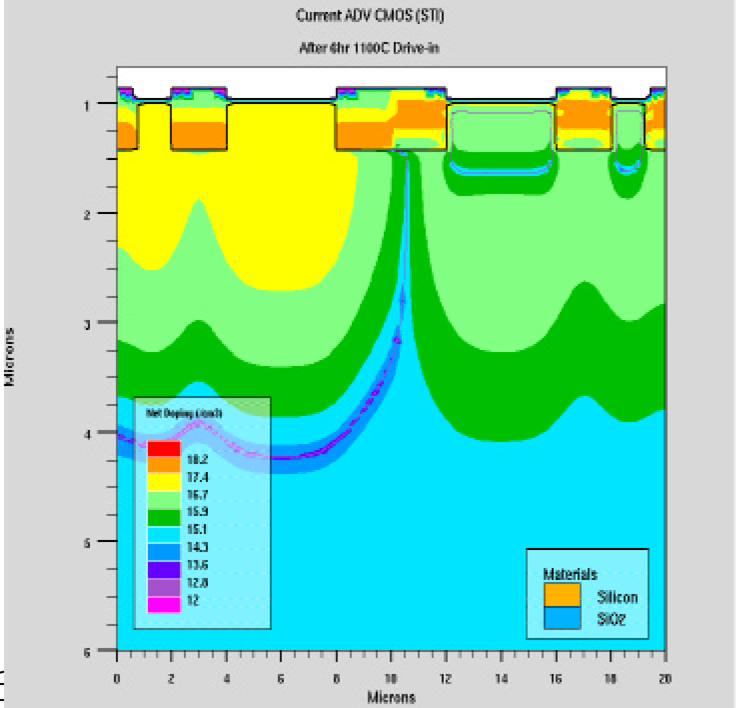
CVD Trench fill- P-5000
Anneal –Bruce Tube 1

Trench CMP
CMP Clean

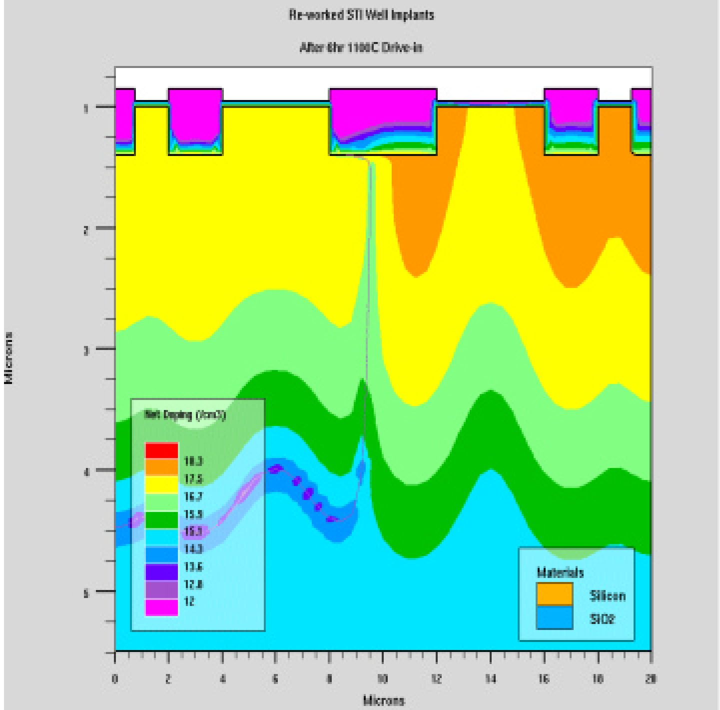
RCA Clean
Hot Phos. Nitirde strip

SIMULATION: PROCESS CROSS-SECTION

Current Process



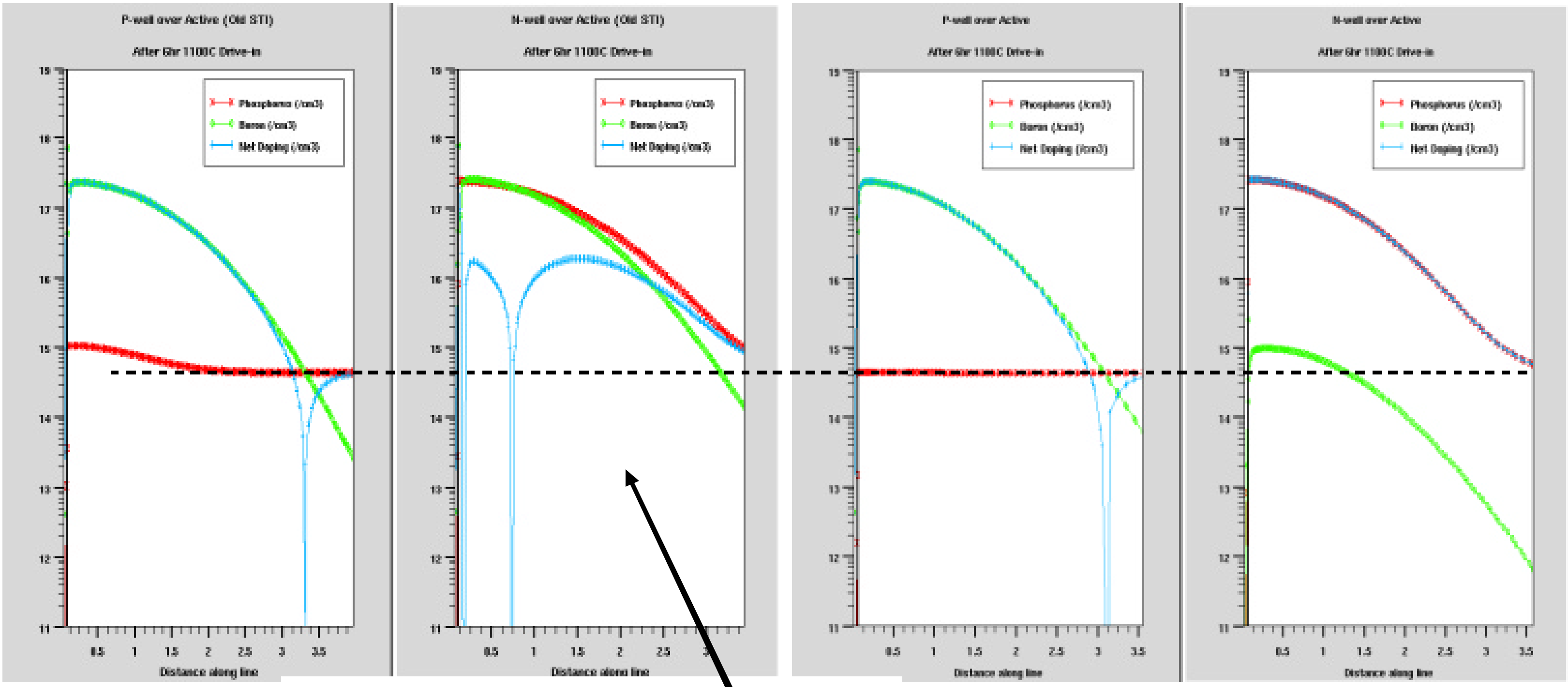
Proposed Process



SIMULATION: ORIGINAL PROCESS WELL PROFILES

Current Process

Proposed Process



Problems with Boron Penetration of Masking Resist

VERIFICATION OF OXIDE SIDE WALL SPACERS

Use factory process as given in MESA and see if sidewall spacers are created.

David Pawlik

February 22, 2005

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REFERENCES

1. "Silicon Processing", Stanley Wolf
2. EMCR650 lecture notes on line at http://www.rit.edu/~lffeee