*ROCHESTER INSTITUTE OF TECHNOLOGY*
*MICROELECTRONIC ENGINEERING*

# Summary of Selected EMCR650 Projects for Fall 2005

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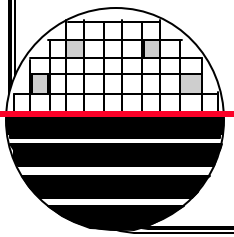
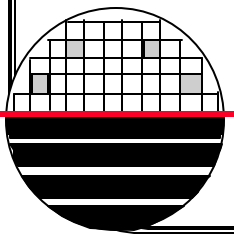


# *INTRODUCTION*

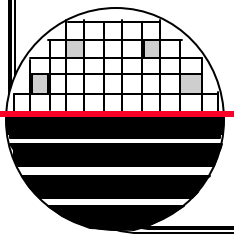
Each of the students in EMCR650 are asked to do a process improvement project to make the student factory better. In place of a final exam they present their project results.

This document is a summary of some of their presentations.



# *OUTLINE*

Introduction
Improved (Shorter Time) Branson Asher Recipe – Dan Pearce
Measured Etch Rates of PECVD TEOS & Oxide – Hang Lin
SEM Pictures of Factory STI – Nkiruka Okeke
Design, Fabrication and Testing of a PMOS 4-Input MUX–Dr. Fuller



# NEW IMPROVES SHORTER TIME BRANSON ASH

| | 6" POST_AL | | |
|---|---|---|---|
| **Step** | **1** | **2** | **3** |
| **Pump** | Fast | Fast | None |
| **Purge** | Slow | None | Fast |
| **Endpoint** | EOP | Time | Time |
| **Time** | 150 | 5 | 5 |
| **RF** | 500 | 0 | 0 |
| **Lamp** | 1800 | 0 | 0 |
| **Lamp Time** | 20 | 0 | 0 |
| **Platen Temp** | 40 | 40 | 40 |
| **Pressure** | 4500 | 50 | 8000 |
| **Gas1** | 5000 | 0 | 0 |
| **Gas2** | 0 | 0 | 3000 |
| **EOP Timeout** | 200 | 20 | 120 |

Dan Pearce


Increased lamp time from 15 to 20 sec.
Increased pressure from 4000 to 4500 mTorr
Changed from none to slow purge in step 1

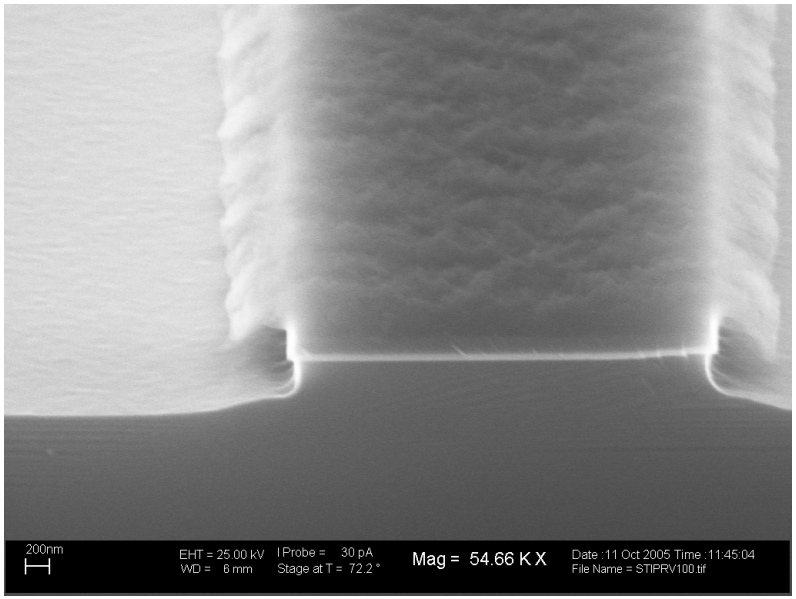
# MEASURED ETCH RATES OF PECVD TEOS & OXIDE

| | | | | |
|---|---|---|---|---|
| Rochester Institute of Technology | | Dr. Lynn Fuller | | |
| Microelectronic Engineering | | | | |
| | | | | |
| | **Summary of Etch Rates and Deposition Rates for RIT Processes** | | | |
| | | | | |
| **Wet Etch Process Description** | | **Date** | **Rate** | **Units** |
| | 7:1 Buffered Oxide Etch of Thermal Oxide, 300°K | 12/1/2004 | 1122 | Å/min |
| | 10:1 Buffered Oxide Etch of Thermal Oxide, 300°K | 10/15/2005 | 586 | Å/min |
| | 10:1 BOE Etch of PECVD TEOS Oxide, no anneal, 300°K | 10/15/2005 | 2062 | Å/min |
| | 10:1 BOE Etch of PECVD TEOS Oxide, anneal 1000C - 60 min, 300°K | 10/15/2005 | 814 | Å/min |
| | 10:1 BOE Etch of PECVD TEOS Oxide, anneal 1100C - 6 hr, 300°K | 10/15/2005 | 562 | Å/min |
| | Pad Etch on Thermal Oxide, 300 °K | 12/1/2004 | 629 | Å/min |
| | Pad Etch of PECVD TEOS Oxide, 300°k | | | Å/min |
| | Hot Phosphoric Acid Etch of Thermal Oxide at 175 °C | 10/15/2005 | <1 | Å/min |
| | Hot Phosphoric Acid Etch of TEOS Oxide, no anneal, at 175 °C | 10/15/2005 | 17 | Å/min |
| | Hot Phosphoric Acid Etch of TEOS Oxide, 1000 C 60 min Anneal, at 175 °C | 10/15/2005 | 3.3 | Å/min |
| | Hot Phosphoric Acid Etch of TEOS Oxide, 1100 C 6 Hr Anneal, at 175 °C | 10/15/2005 | 3.8 | Å/min |
| | Hot Phosphoric Acid Etch of Si3N4 at 175 °C | 11/15/2004 | 82 | Å/min |
| | 50:1 Water:HF(49%) on Thermal Oxide at room T | 10/15/2005 | 187 | Å/min |
| | 50:1 Water:HF(49%) on PECVD TEOS Oxide, no anneal, at room T | 10/15/2005 | 611 | Å/min |
| | 50:1 Water:HF(49%) on PECVD TEOS Oxide, anneal 1000 C -30 min, at room T | 10/15/2005 | 115 | Å/min |
| | 50:1 Water:HF(49%) of PECVD TEOS Oxide, anneal 1100C - 6 hr, 300°K | 10/15/2005 | 107 | Å/min |
| | KOH 20 wt%, 85 °C, Etch of Si (crystaline) | 2/4/2005 | 30 | µm/min |
| | KOH etch rate of PECVD Nitride (Low σ) | 2/4/2005 | 10 | Å/min |

Hang Lin

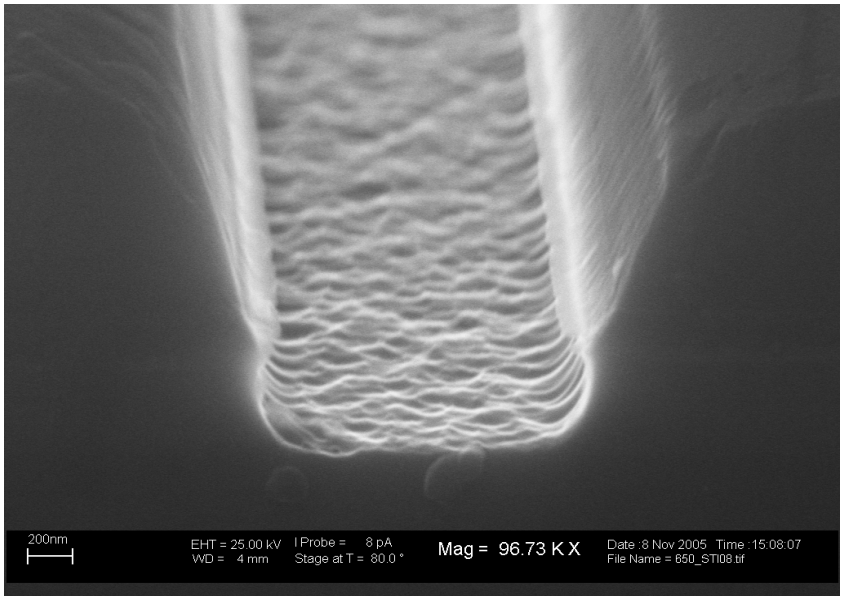
# SEM PICTURES OF FACTORY STI

## COMPARISON OF TRENCH ETCH IN DRYTEC QUAD AND LAM490




Hard bake not good enough
-Resist Flow (etch to hot)

Tool: Drytec Quad
RF Power: 250 W
Etch Chemistry: SF**6** & CHF**3** 30sccm
Pressure: 60 mTorr




Hard Bake not good enough
-Resist Erosion (etch to long)

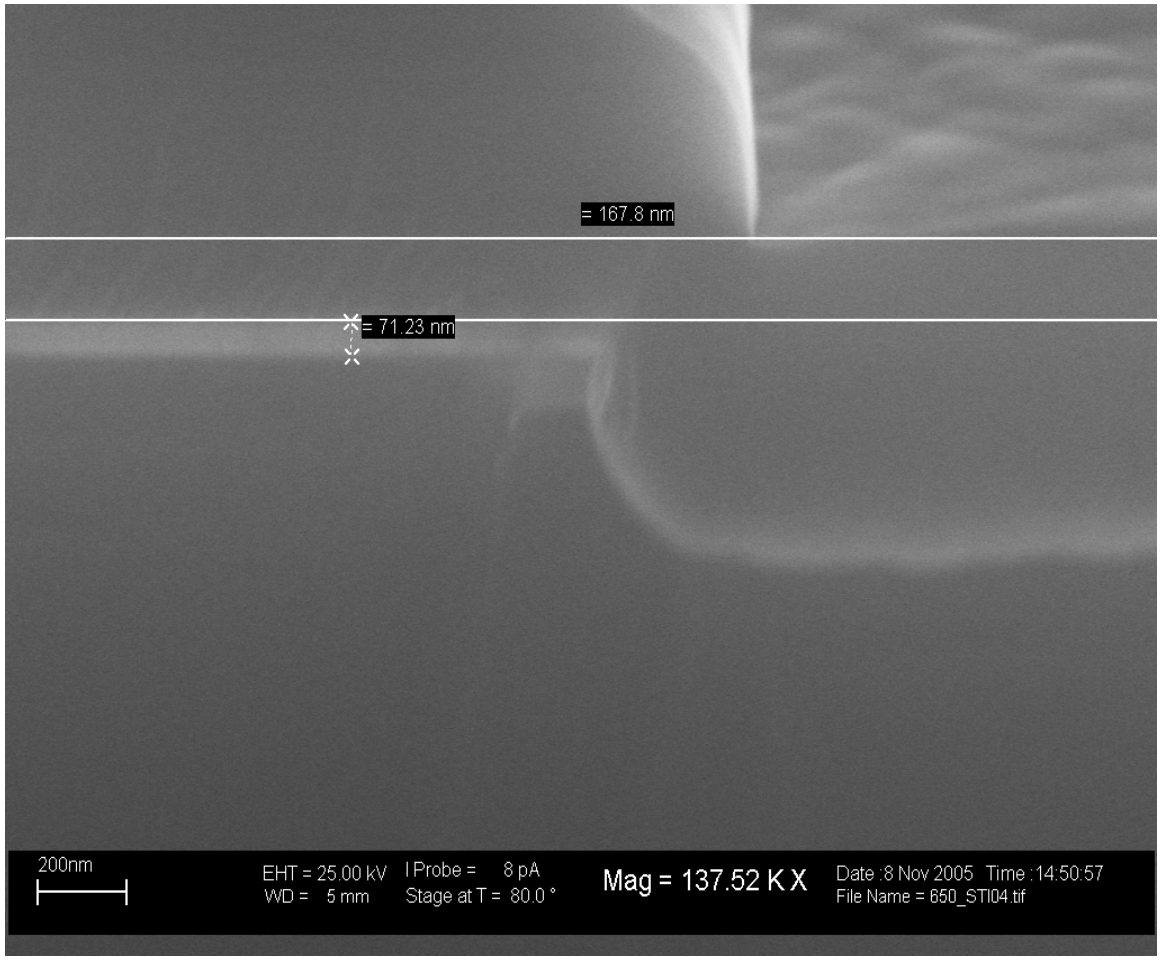
Tool: LAM 490
RF Power: 125 W
Etch Chemistry: SF6 200sccm
Pressure: 259 torr

Nkiruka Okeke

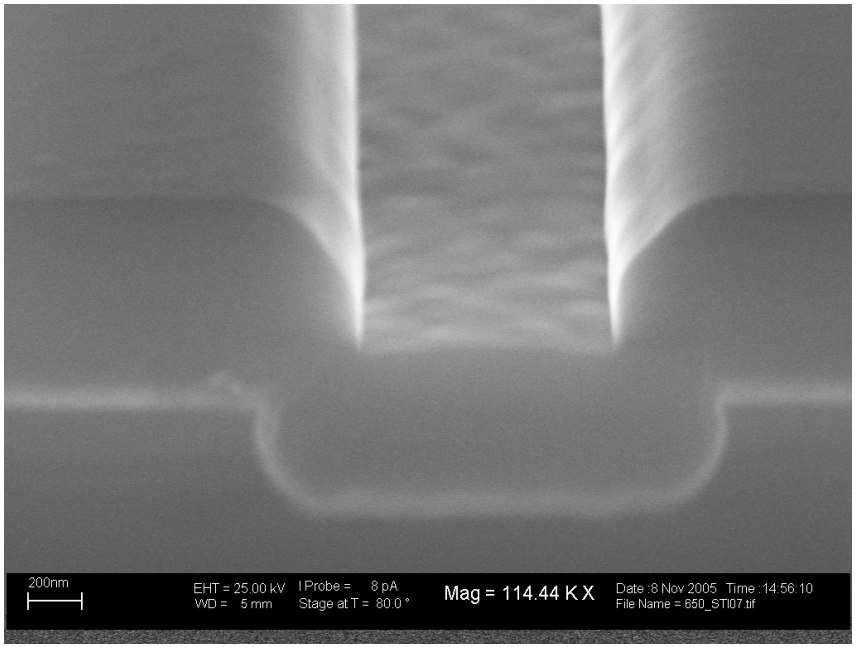
# *SEM PICTURES OF FACTORY STI*

Nkiruka Okeke

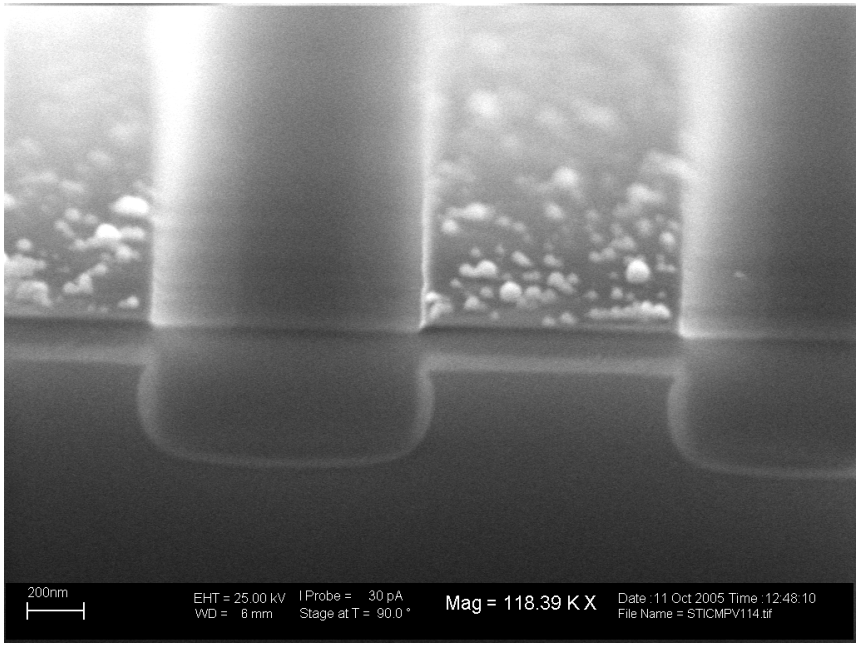
SEM Picture after Lam490 STI Etch, Resist Strip and trench fill. Shows correct trench depth of ~4000Å and fill of ~6000Å



# *SEM PICTURES OF FACTORY STI*




STI Formation using LAM 490
After PECVD TEOS trench fill but before CMP




STI Formation using Drytek Quad after CMP

*Rochester Institute of Technology*
*Microelectronic Engineering*

Nkiruka Okeke

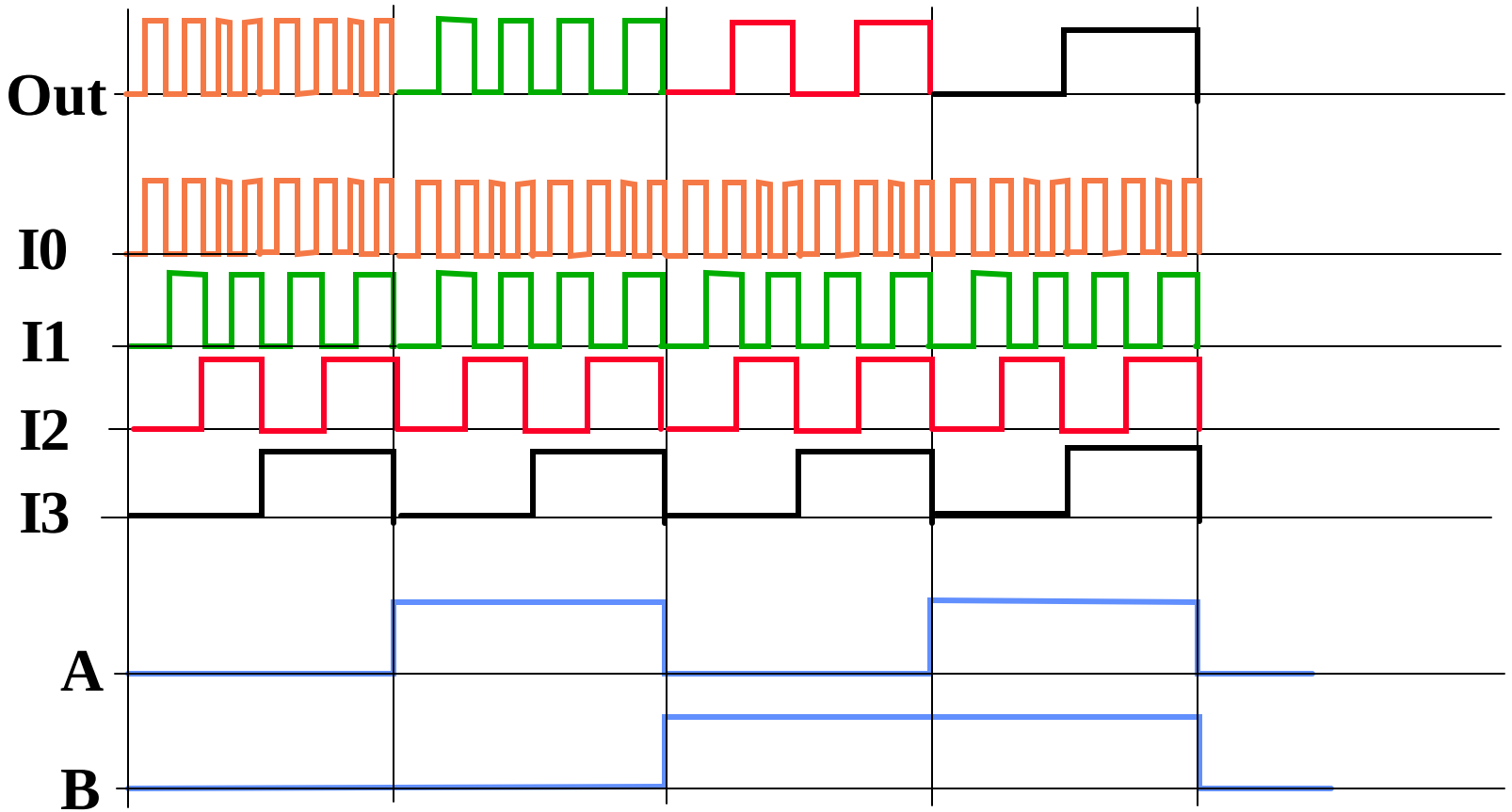
# SEM PICTURES OF FACTORY STI

Conclusion:

1. Lam 490 is a plasma etcher and gives isotropic etch (undercut)
2. DryTech Quad is an RIE and can give anisotropic etch (less undercut)
3. Both etch processes are tough on the photoresist so the resist needs to see a good hard bake. The standard SSI recipes don't really hard bake (1min at 120°C)
4. PECVD TEOS trench Fill Looks good before and after CMP.
5. Hang Lin showed that the PECVD TEOS needs to be densified.

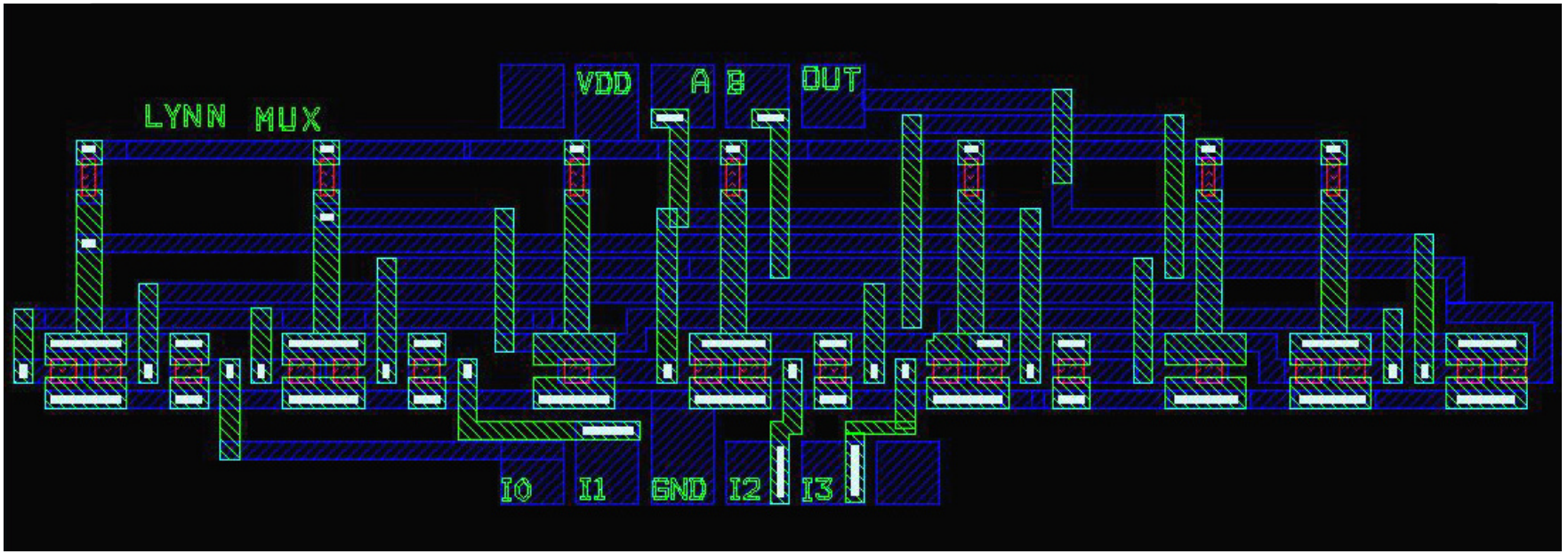
Nkiruka Okeke

# MULTIPLEXER TEST SIGNALS

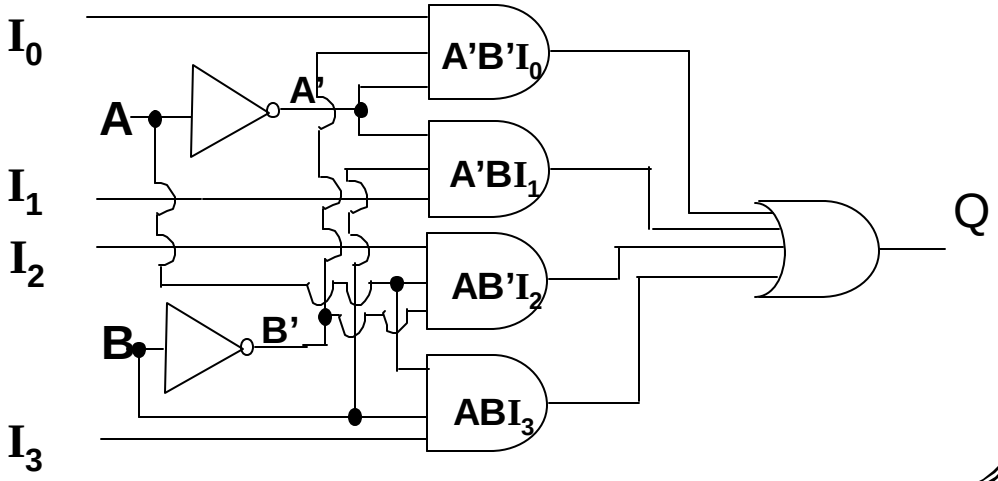



Input Signal I0, I1, I2 or I3 is directed to the output depending on the A and B select line values

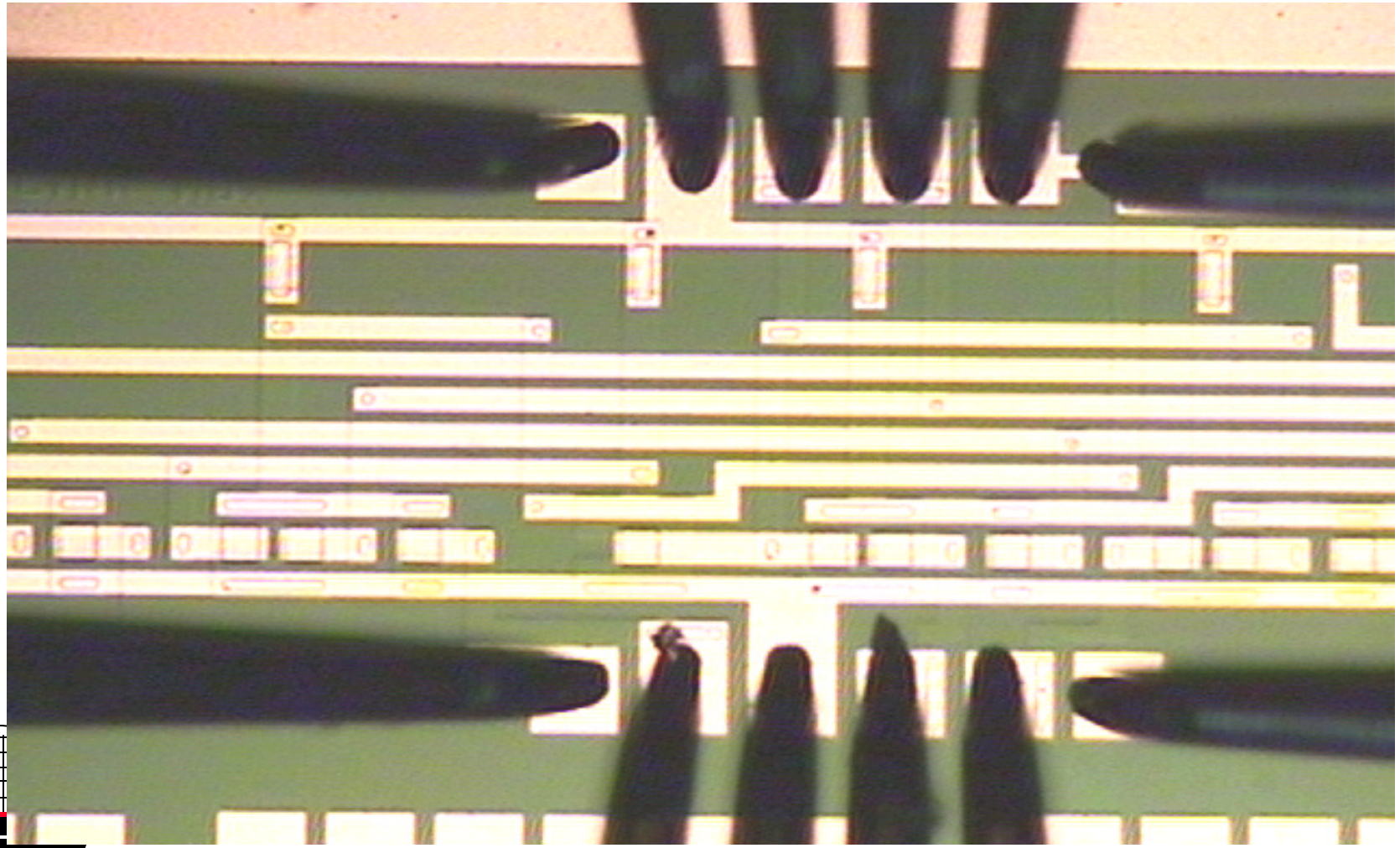
# MUX LAYOUT AND GATE LEVEL SCHEMATIC



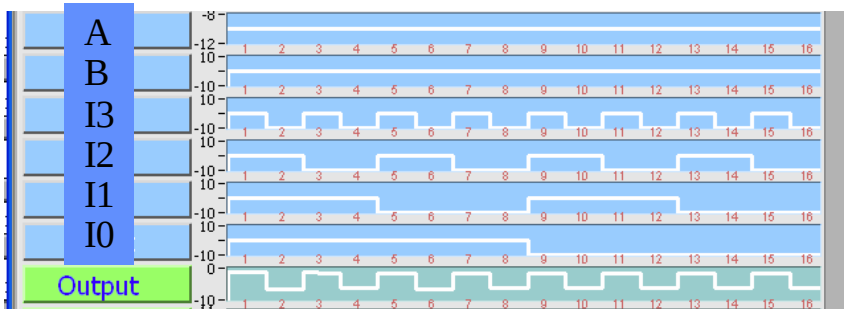

25 Transistors

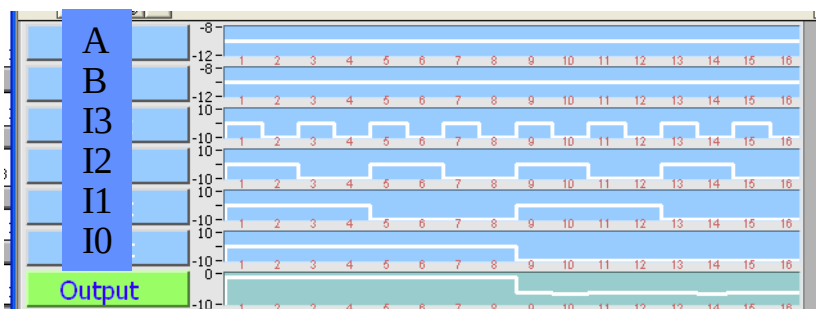


# PMOS 4-INPUT MULTIPLEXER

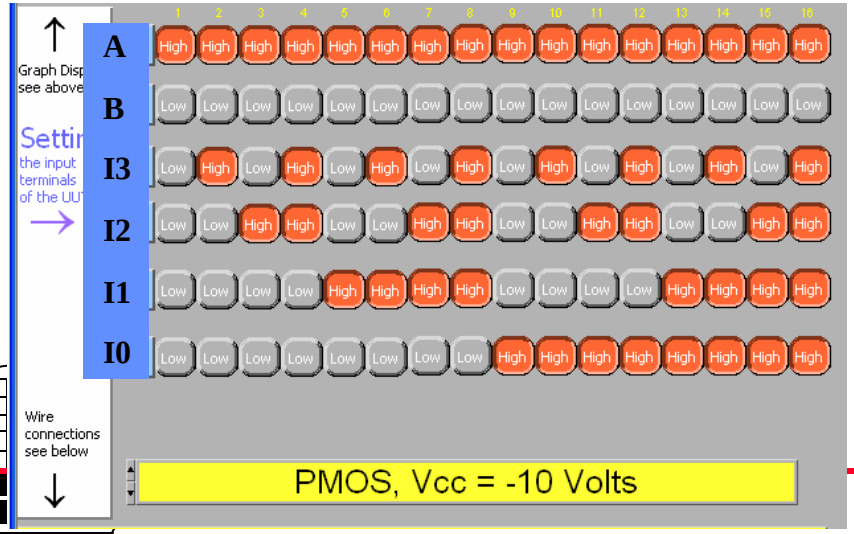


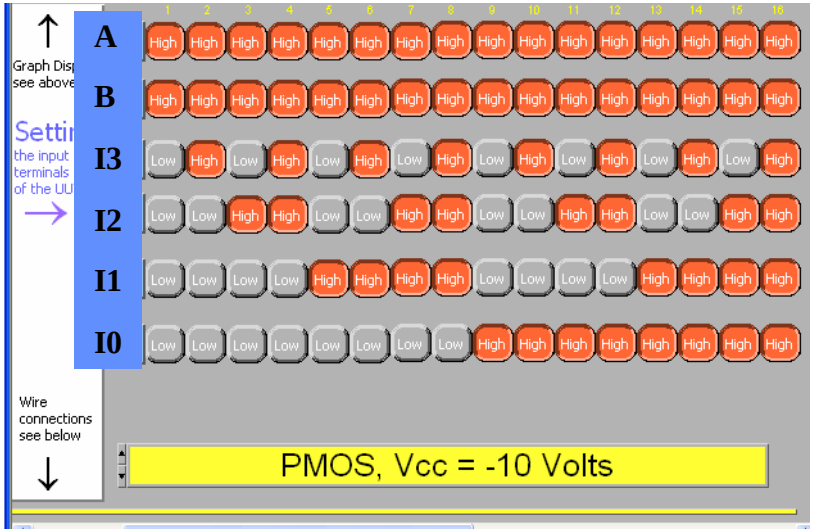
# MUX TEST RESULTS




In PMOS logic low is 0 volts, logic high is -Vcc



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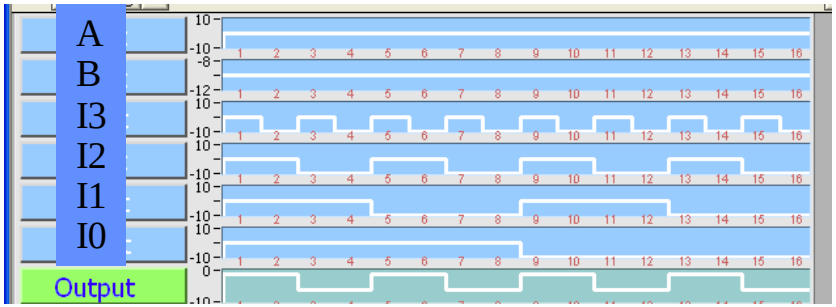


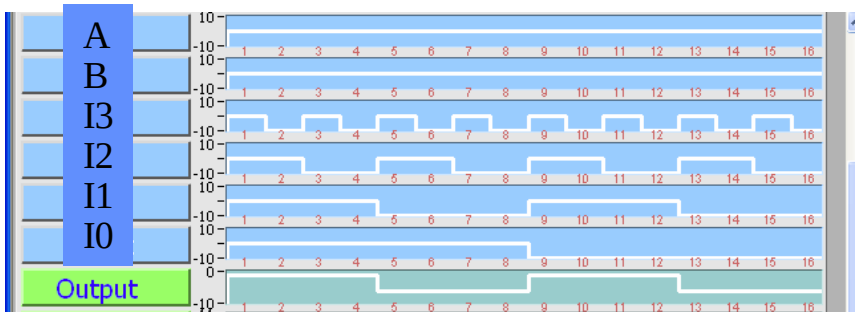


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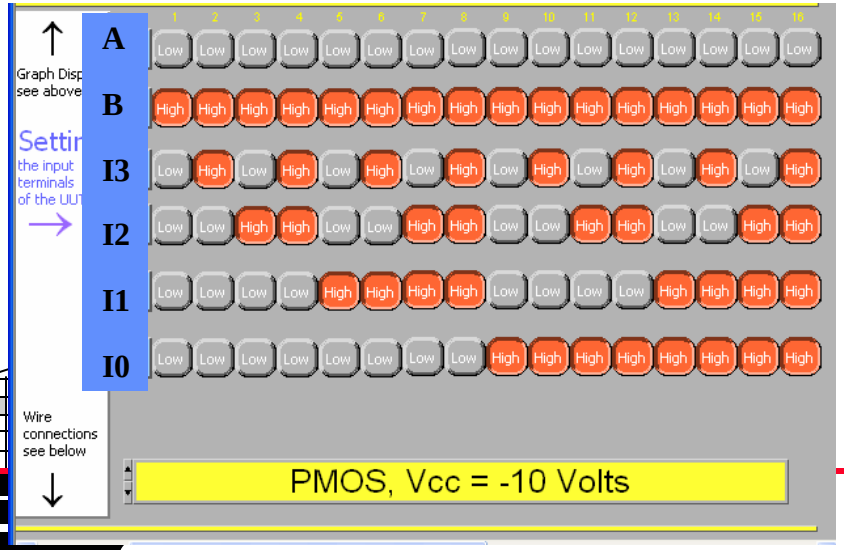


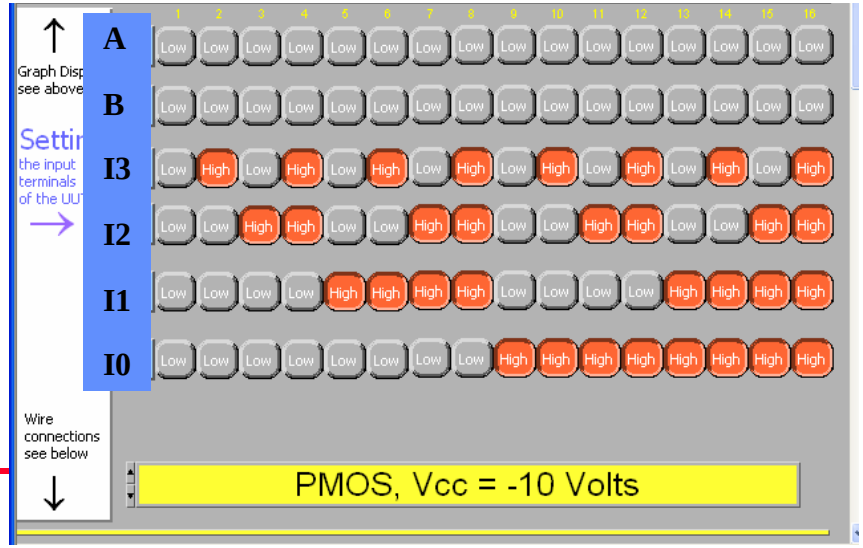

# *REFERENCES*

1. “Silicon Processing”, Stanley Wolf
2. EMCR650 lecture notes on line at http://www.rit.edu/~lffeee