ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Summary of Selected EMCR732 Projects for Spring 2005

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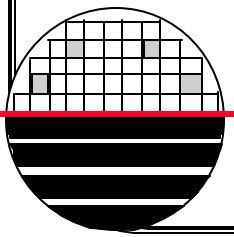
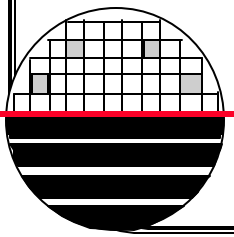


INTRODUCTION

Each of the students in EMCR650 and EMCR732 are asked to do a process improvement project to make the student factory better. In place of a final exam they present their project results.

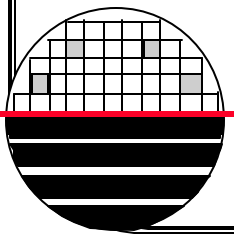
Students in EMCR731 did a observational study of particulate contamination in some of the tools in the laboratory.

This document is a summary of some of their presentations.



OUTLINE

Introduction
Thin Gate Oxide Growth by Rapid Thermal Processing (RTP)
Measurement of 50Å Oxides at RIT
Surface Charge Analyzer (SCA) Measurements of Oxide Quality
New Aluminum Etch Recipe for Lam4600 with Endpoint Detection
Rework Strategy for Aluminum Etch in Lam4600
Testing of First CMOS DAC Lot
Four Levels per Mask Plate Stepper Job for Canon Stepper
Drytek Quad Nitride Sidewall Spacer Etch Uniformity
Simulation of Threshold Adjust Implant for Adv-CMOS Process



THIN GATE OXIDE GROWTH BY RAPID THERMAL PROCESSING (RTP)

From Textbook by S. Wolf

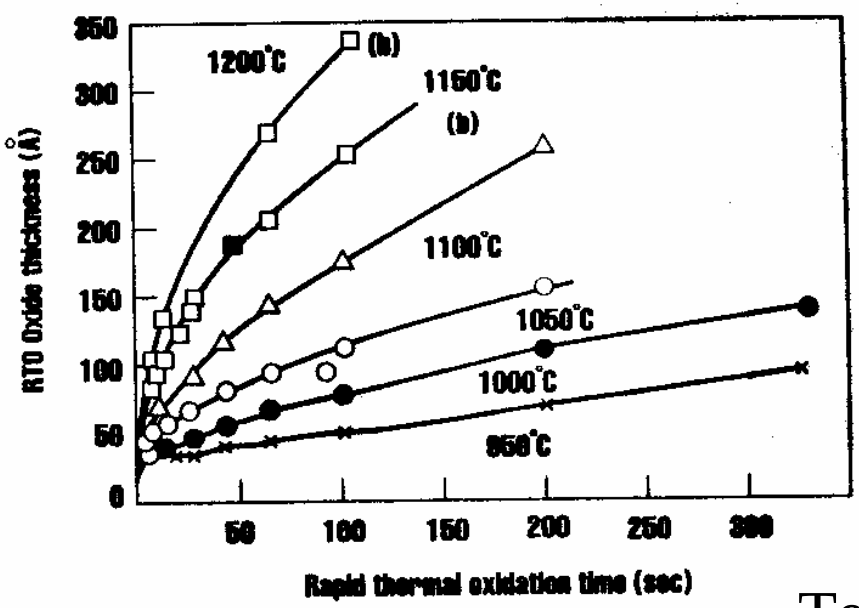
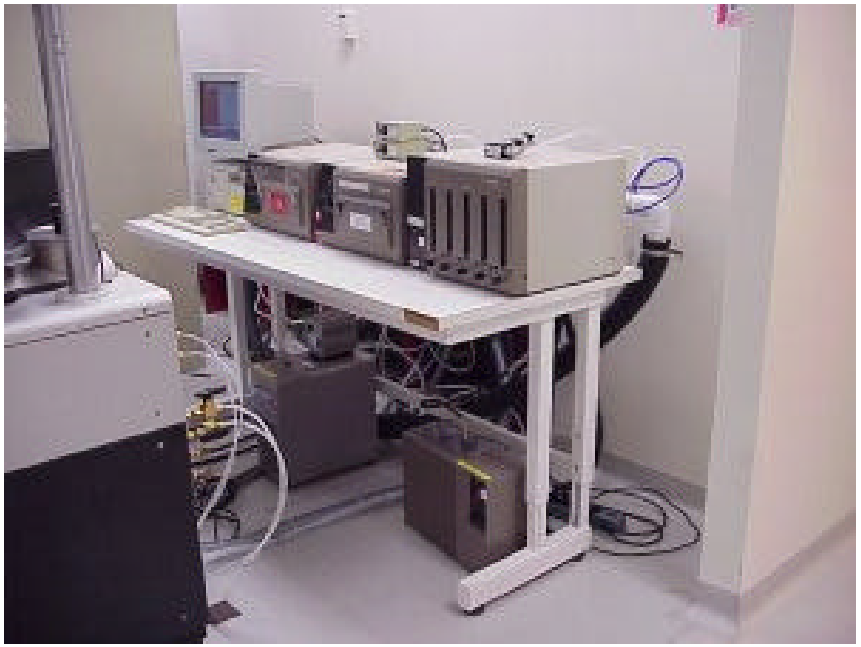


Figure 6-13 Typical data for oxide thickness as a function of time for a rapid thermal oxidation process *(after Moslehi et al., 1985).*



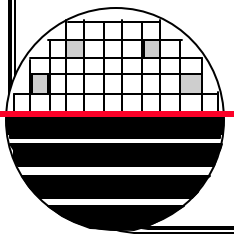
Textbooks say that 150Å of oxide can be grown by RTP at 1100°C in 60 sec.

RTP RECIPE

Recipe for RTP Oxide, time during SS (Steady State) was changed to obtain different oxide thicknesses, 60s, 120s, 240s, and 480s

Step	Time (sec)	Temp (C)	T sw	Gain	Dgain	Iwarm	Icold
Delay	10						
Ramp	120	1000					
SS	10	1000	20	-250	-60	5500	5500
SS	480	1000	20	-250	-60	5500	5500
Delay	300						

Sébastien Michel, February 2005
Steve Parshall, Kazuya Tokunaga, May 2005



OXIDE THICKNESS MEASUREMENTS

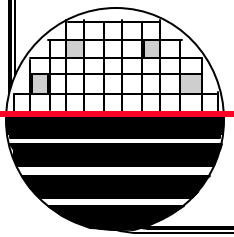
The data shown was obtained using the 5 point 6”wafer Spectromap

RTP Oxide at 1000 C, Dry O2

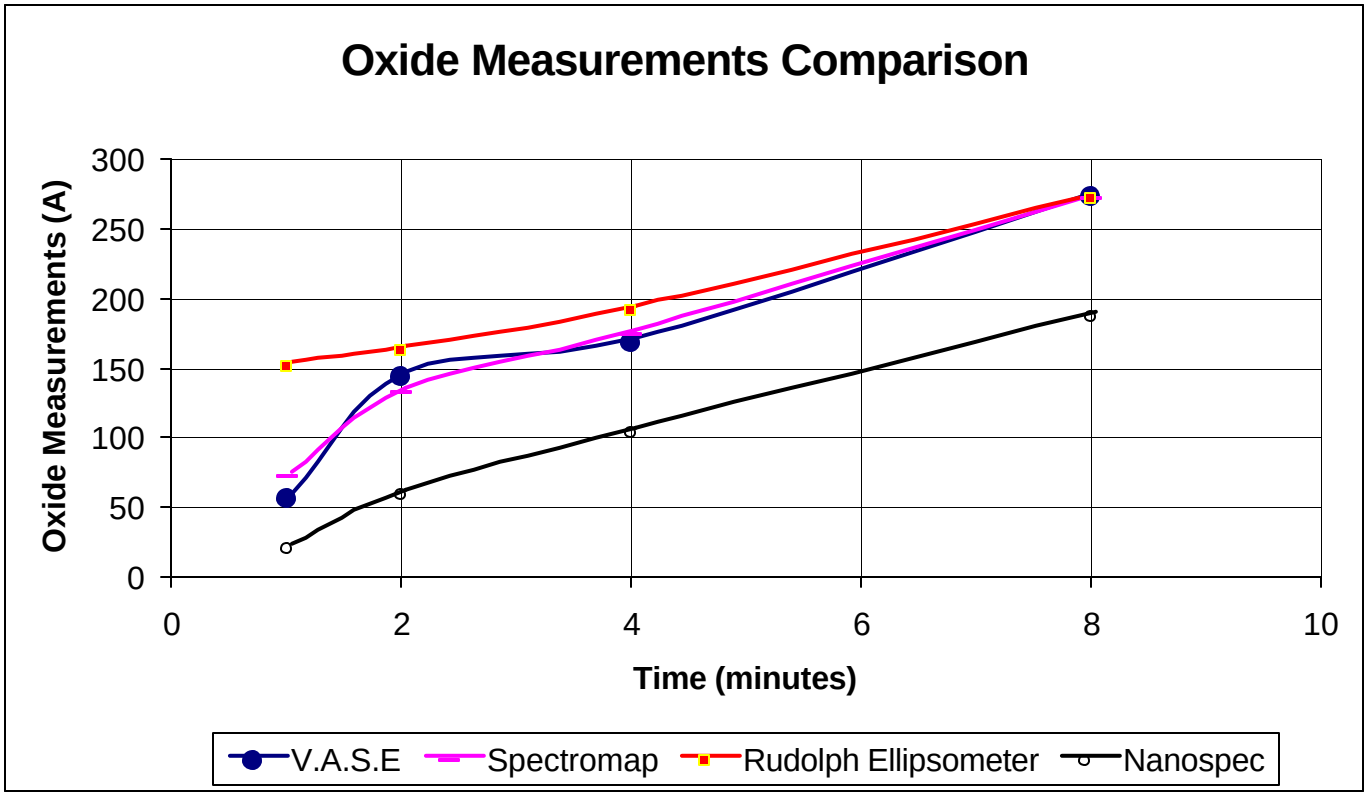
Time	8	4	2	1	Minutes
Mean	211.53	150.13	104.29	67.04	A
Max	271.26	174.22	132.36	71.245	A
Min	167.06	130.35	57.249	53.866	A
STDDEV	37.112	20.187	28.929	14.234	%
Center Pts	271.26	174.22	132.36	71.245	A

The data shown was obtained using the VASE (Variable Angle Spectroscopic Ellipsometer)

Time	8	4	2	1	Min
Xox	272.54	167.59	143.03	55.77	A
n	1.45	1.45	1.45	1.42	



OXIDE MEASUREMENTS COMPARISON



We believe the VASE and the Sprctromap are the best measurement tool for under 100 A

RTP OXIDE QUALITY MEASUREMENTS

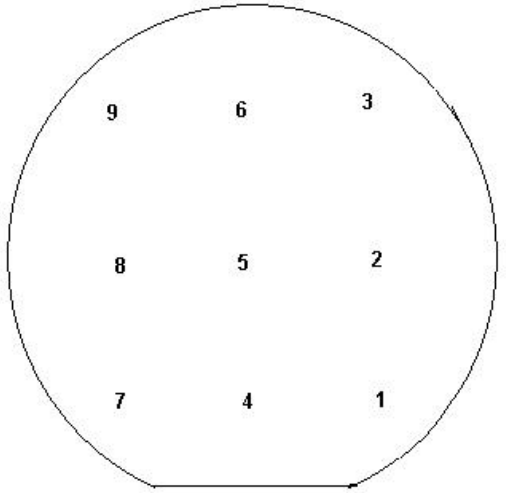
Measurements made using the SCA (Surface Charge Analyzer)

Time	8 minutes	4 minutes	2 minutes	1 minute
NSC	1.13E+14	1.64E+14	1.46E+14	7.56E+14
Qox	3.55E+11	4.26E+11	4.28E+11	4.73E+11
Dit	2.76E+11	3.05E+11	4.32E+11	4.13E+11
Qfb	4.66E+11	5.53E+11	5.94E+11	7.05E+11
Ts	83	78	126	151

Dit is close to Bruce Furnace thermal gate oxide values
Typically ~1E11

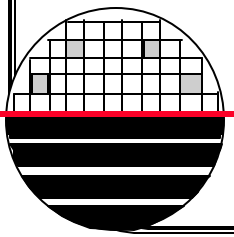
UNIFORMITY OF SURFACE STATE DENSITY

Experiments: 2 P-type bare wafers
→RCA clean
→TCA clean of the oxidation furnace, Bruce Tube 4.
→Gate oxide growth, 150A thin oxide growth, dry O2 Bruce recipe 215.
→Thickness measurement: 5 points, average value: 140A, standard deviation < 10A.
→Wafers inserted in the furnace show hundreds of added particles so did RCA clean without HF step.
→SCA 2500: Use Recipe FAC-P with a test wafer (known oxide thickness) in order to calibrate the probe by measuring 1 point.
→Program 9PTSQSIX, 9 points.



9 points square	Wafer 1	Wafer 2
Si doping (/cm3) N_{sc}	1,07e14 Std dev: 0,02e14	0,90e14 Std dev: 0,01e14
D_{it}(traps/cm2/ev)	1,41e11 Std dev: 0,07e11	0,84e11 Std dev: 0,02e11
T_s (usec)	233 Std dev: 5	235 Std dev: 7

Sébastien Michel
Spring Quarter 2005



ALUMINUM ETCH RECIPE END POINT DETECTION

Rochester Institute of Technology
Microelectronic Engineering

By Gianni Franceschinis

LAM 4600 Al Etcher

Plasma Chemistry

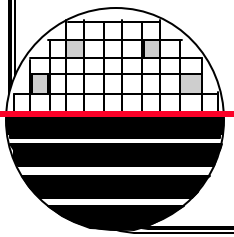
Cl2 – Reduces Pure Aluminum

BCl3 – Etches native Aluminum Oxide

-Increases Physical Sputtering

N2 – Diluent and carrier for the chemistry

Chloroform – Helps Anisotropy and reduces Photoresist damage



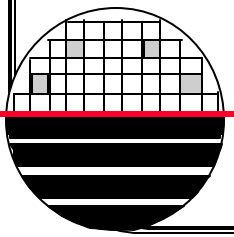
LAM 4600 Al Etch

Film Stack Used:

Sputtered Aluminum, CVC 601
5mTorr, 16 sccm Ar flow rate,
2000 watts
1500 Seconds (5 min pre sputter)
Average Al Thickness 8400Å

5000Å Wet Oxide

Bruce Furnace Tube 1, Recipe 50



LAM 4600 Al Etch

Recipe 12: Jeremiah Hebding

Step	1	2	3	4	5
Pressure (mtorr)	300	300	300	300	0
RF Top (W)	0	0	0	0	0
RF Bottom (W)	0	250	125	125	0
Gap (cm)	3	3	3	3	5.3
N2	25	25	40	50	50
BCl3	100	100	50	50	0
Cl2	10	10	60	45	0
Ar	0	0	0	0	0
CFORM	15	15	15	15	15
Complete	Stabl	Time	endpoint	Oetch	time
time (s)	15	8	120	25%	15

Never endpoints, always goes 120 seconds

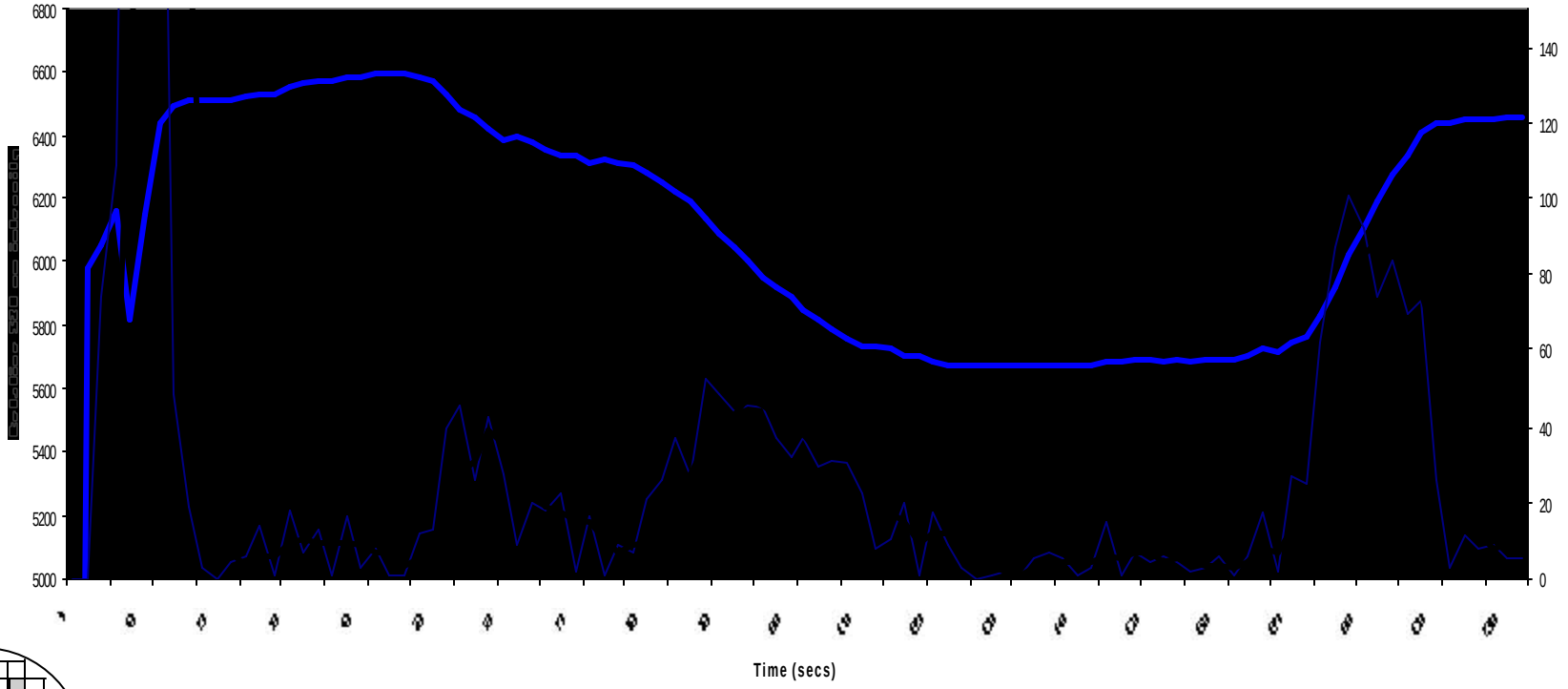
LAM 4600 Al Etch

Plot Configuration (Trend Menu)

	A	B
Name	1	2
Mode	Manual	Manual
Start	111	111
End	119	119
Target	34	35
Input	Hard	Hard
Sample Rate	0.5	0.5
Start	53	53
V.Slope	>	>
Value	1	1
Stop	53	53
V.slope	<	<
Value	0	0

LAM 4600 Al Etch

Typical Endpoint signal



LAM 4600 Al Etch

Final Proposed Recipe: Number 122122

Step	1	2	3	4	5
Pressure (mtorr)	300	300	300	300	0
RF Top (W)	0	0	0	0	0
RF Bottom (W)	0	250	125	125	0
Gap (cm)	3	3	3	3	5.3
N2	25	25	40	50	50
BCl3	100	100	50	50	0
Cl2	10	10	60	45	0
Ar	0	0	0	0	0
CFORM	15	15	15	15	15
Complete	Stabl	Time	endpoint	Oetch	time
time (s)	15	8	130	10%	15

Rate ~50Å/s

Channel	B
Delay	130
Normalize	10 s
Norm Val	5670
Trigger	105%
Slope	+

Gianni Franceschinis, May 2005

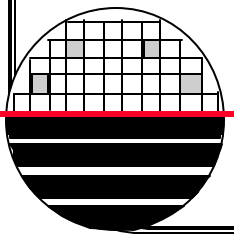
Rochester Institute of Technology
Microelectronic Engineering

LAM 4600 Al Etch Rework Strategy

Aluminum Etch Rework Strategy:

If the etch was not complete use the following procedure to do an additional etch

10 seconds Aluminum wet etch
Spin Rinse Dry (SRD)
LAM 4600 Recipe 12 or 122122 with manual endpoint calculated from 50Å/s etch rate

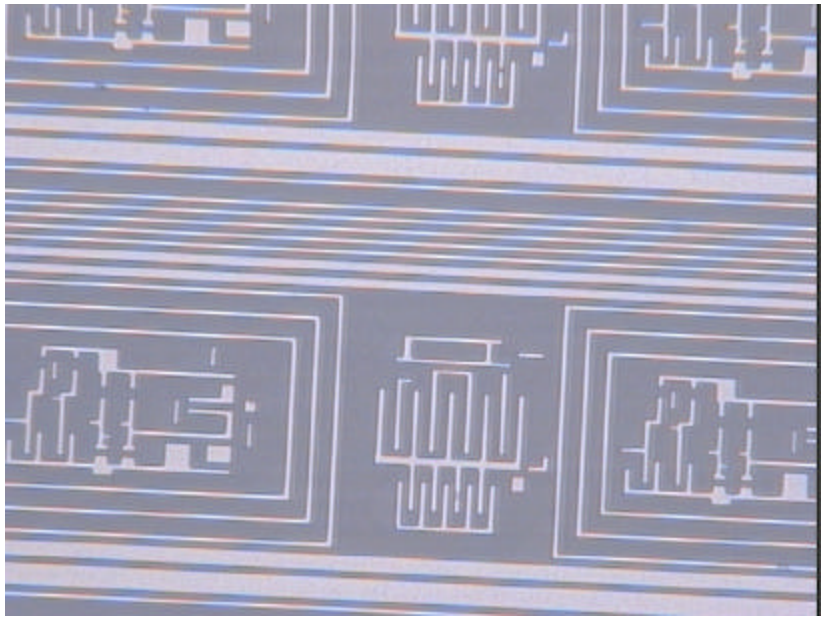


LAM 4600 Al Etch

Conclusion:

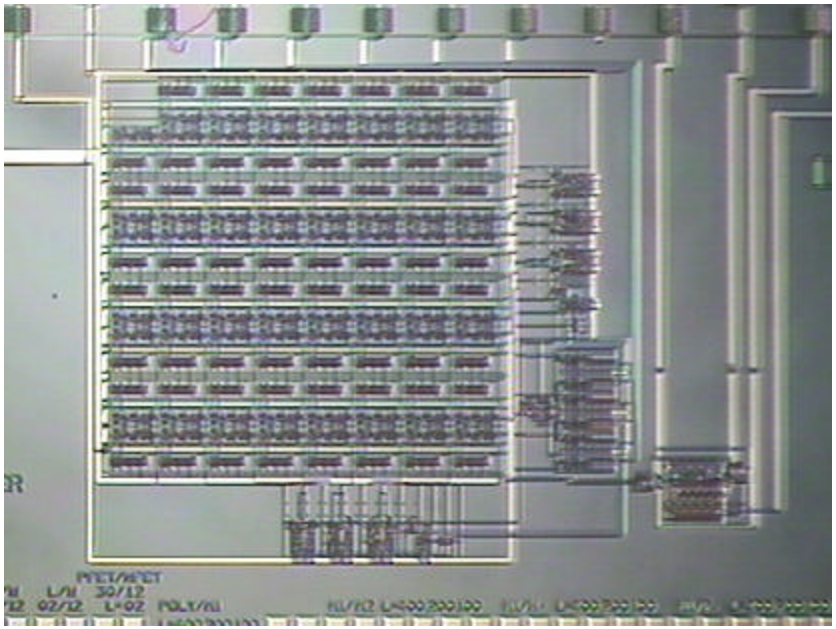
Endpoint detection is possible if the endpoint signal parameters are set appropriately

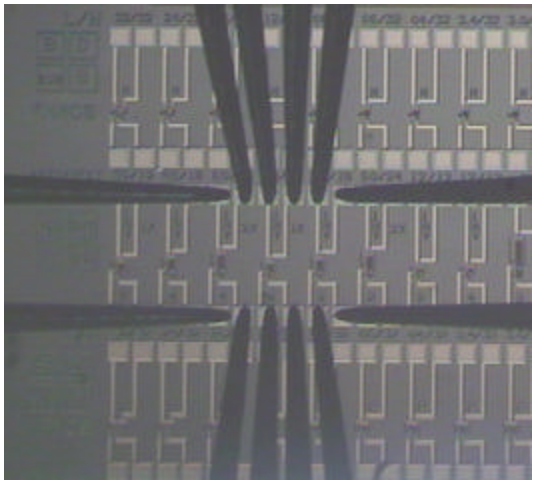
A rework strategy was developed for incompletely etched wafers.



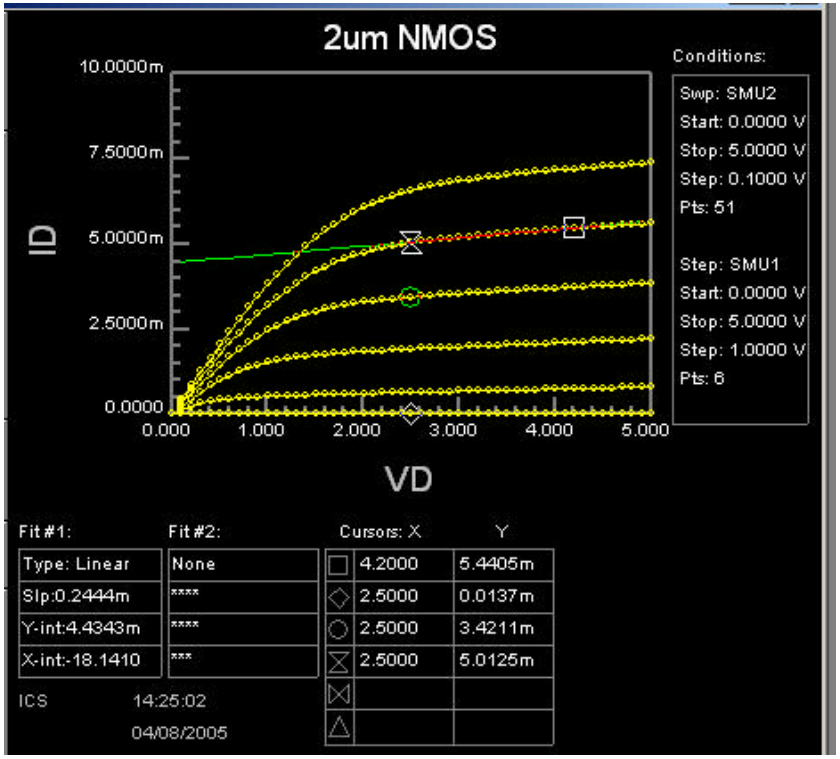
Gianni Franceschinis, May 2005

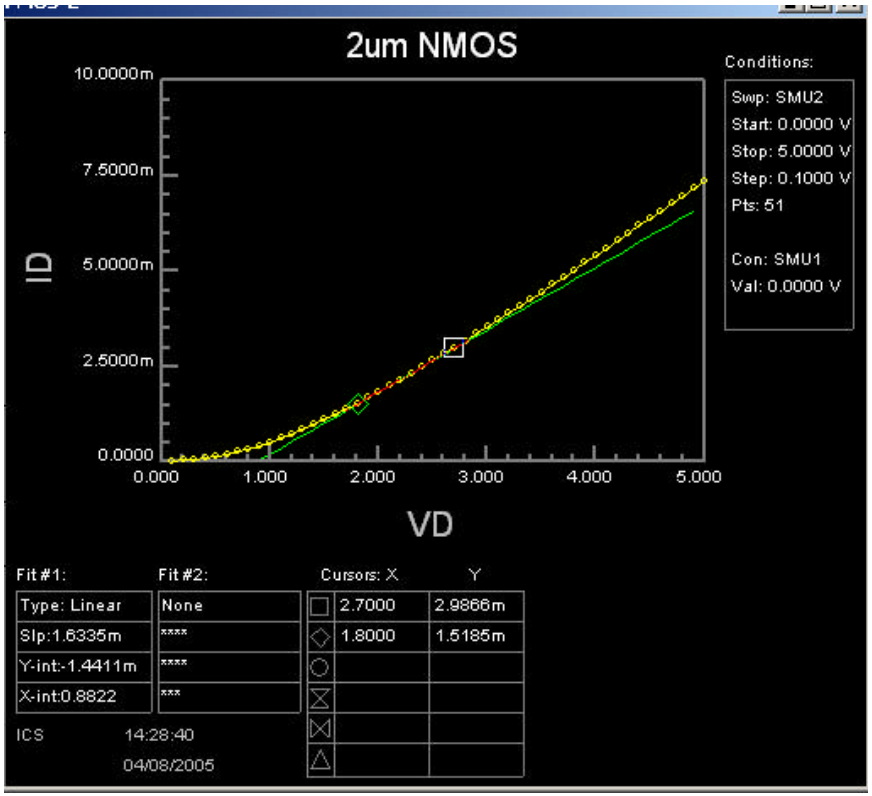
TESTING OF FIRST DAC LOT



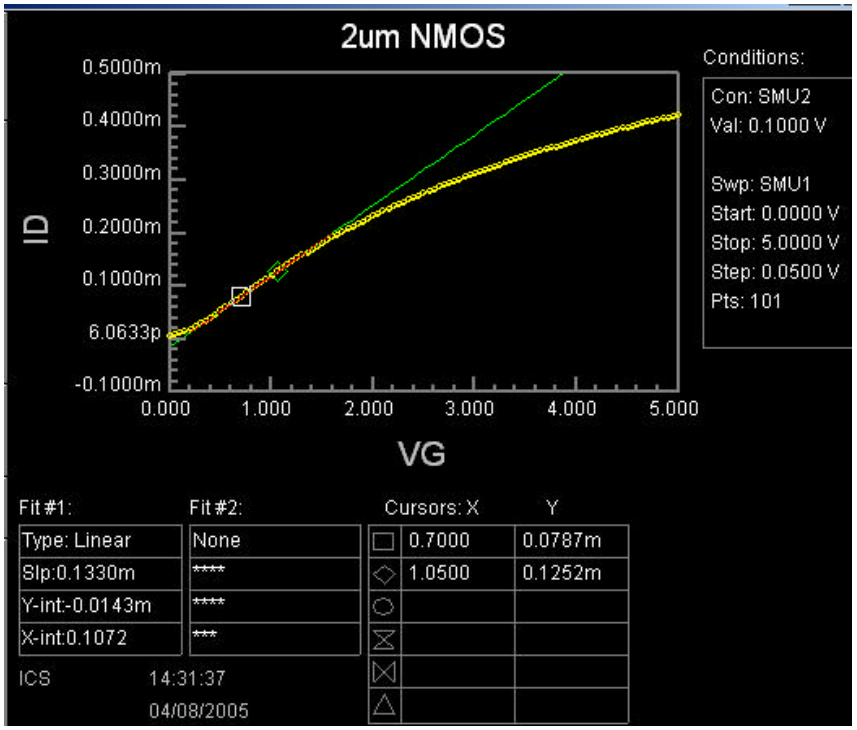


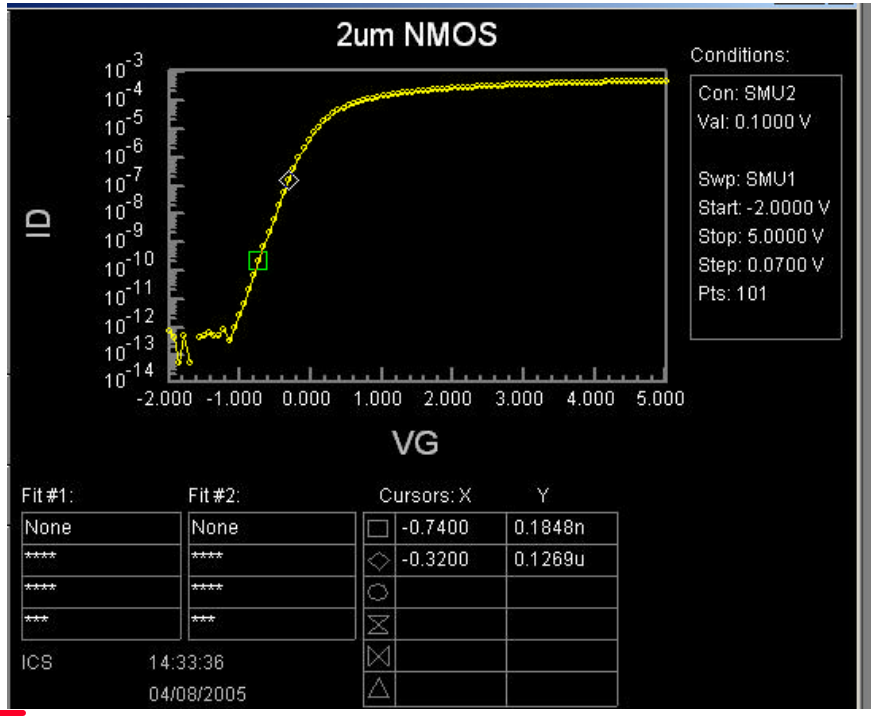
2 µm NMOS TRANSISTOR



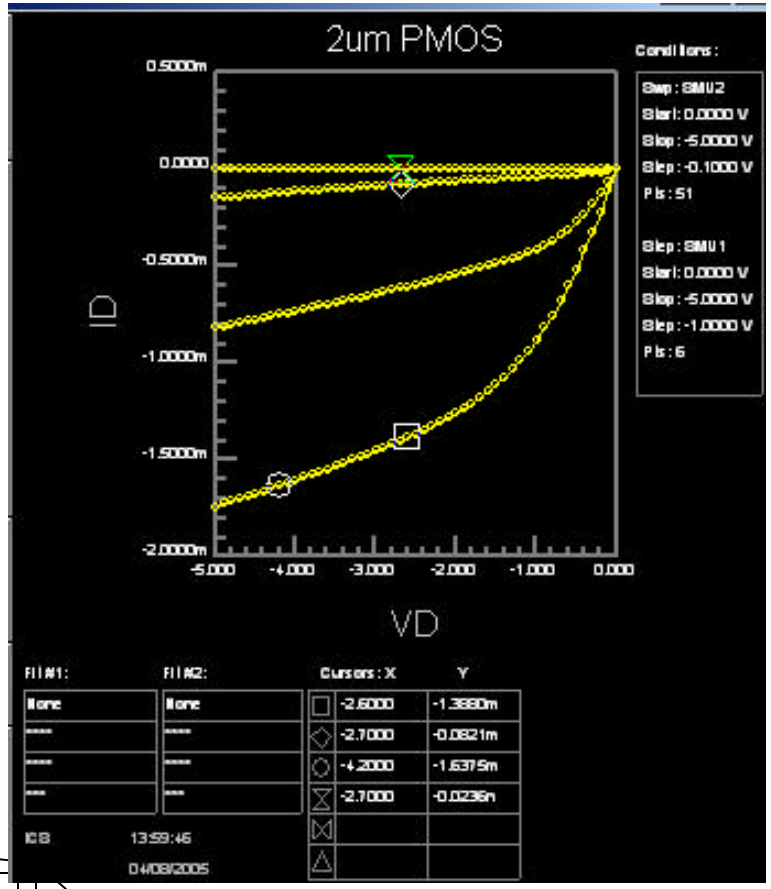


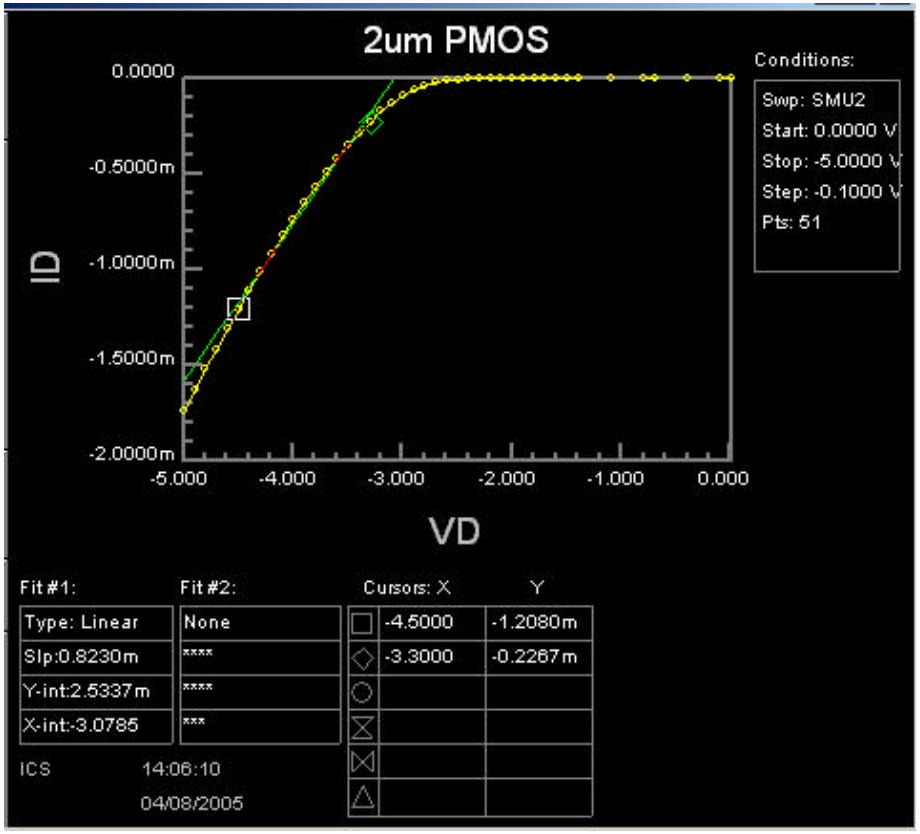
2 µm NMOS ID vs VGS



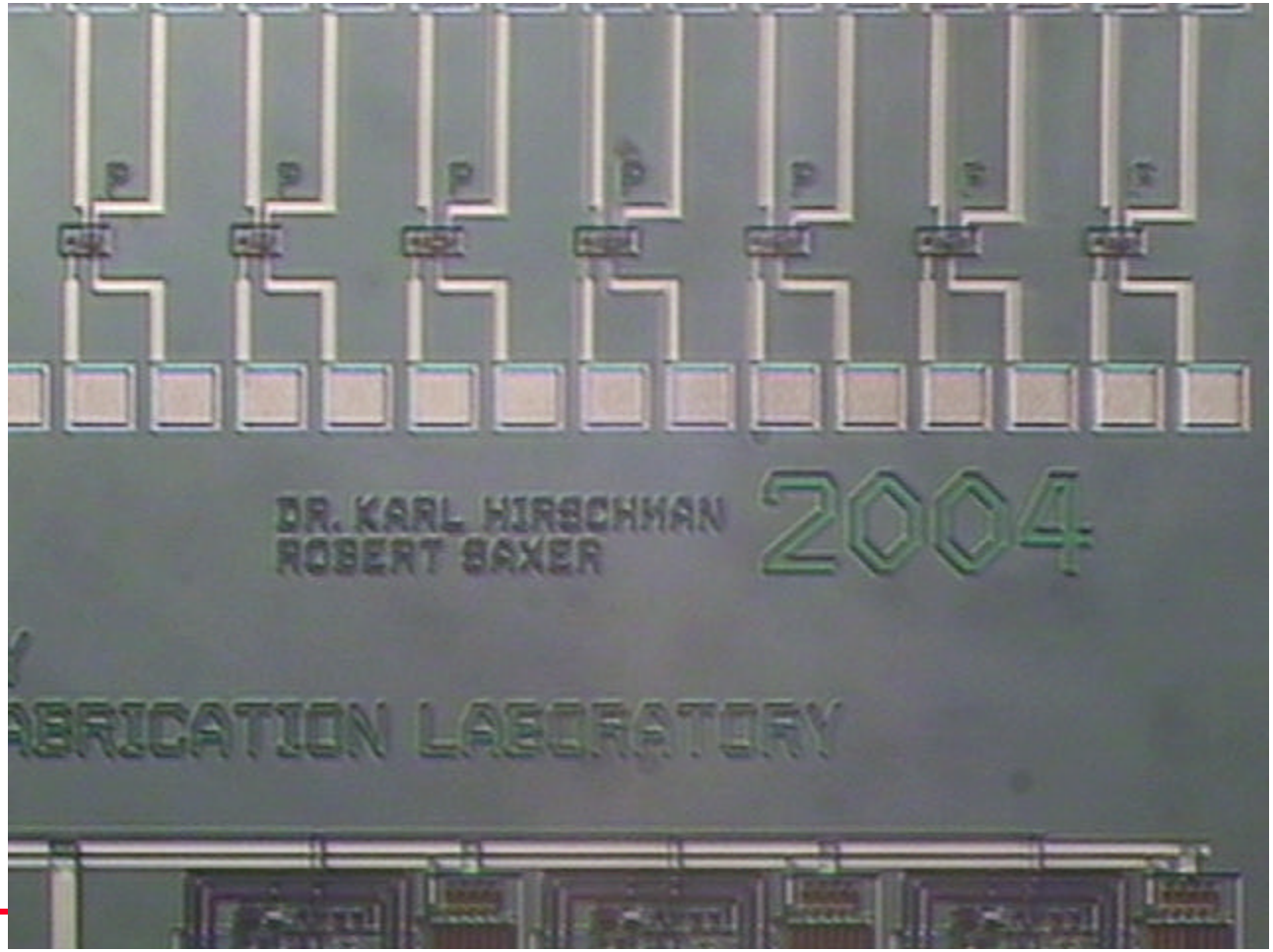


2 µm PMOS TRANSISTOR

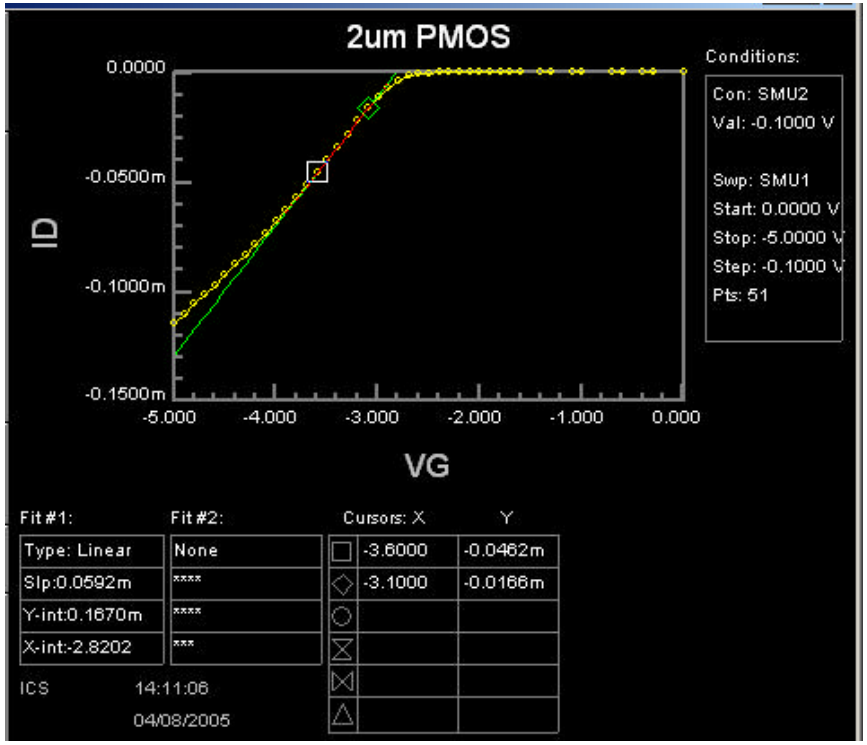


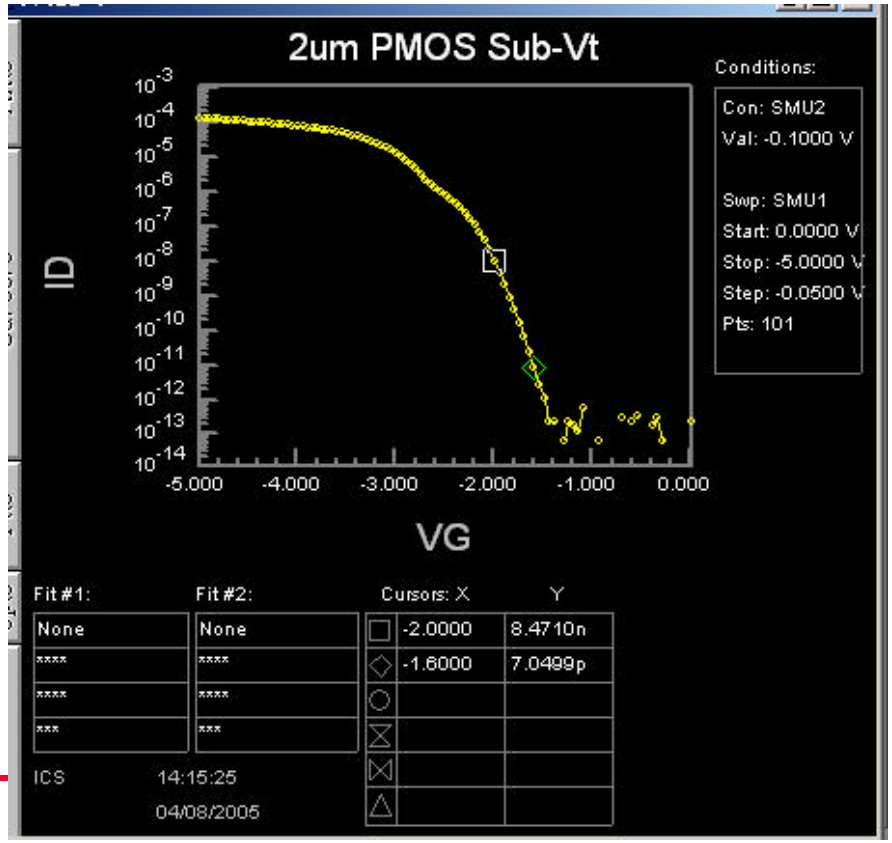


PMOS TRANSISTOR ARRAY

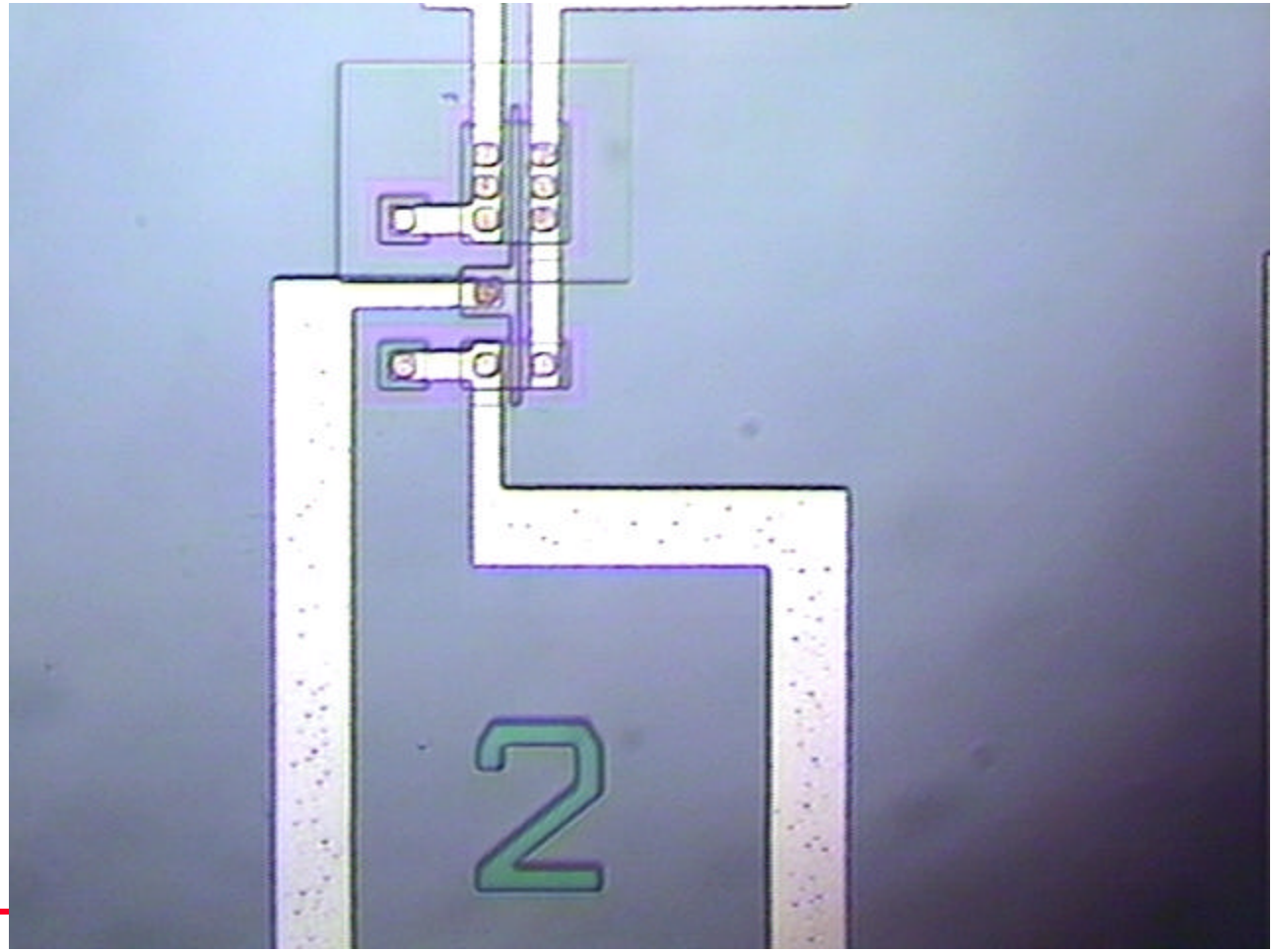


2 µm PMOS ID vs VGS

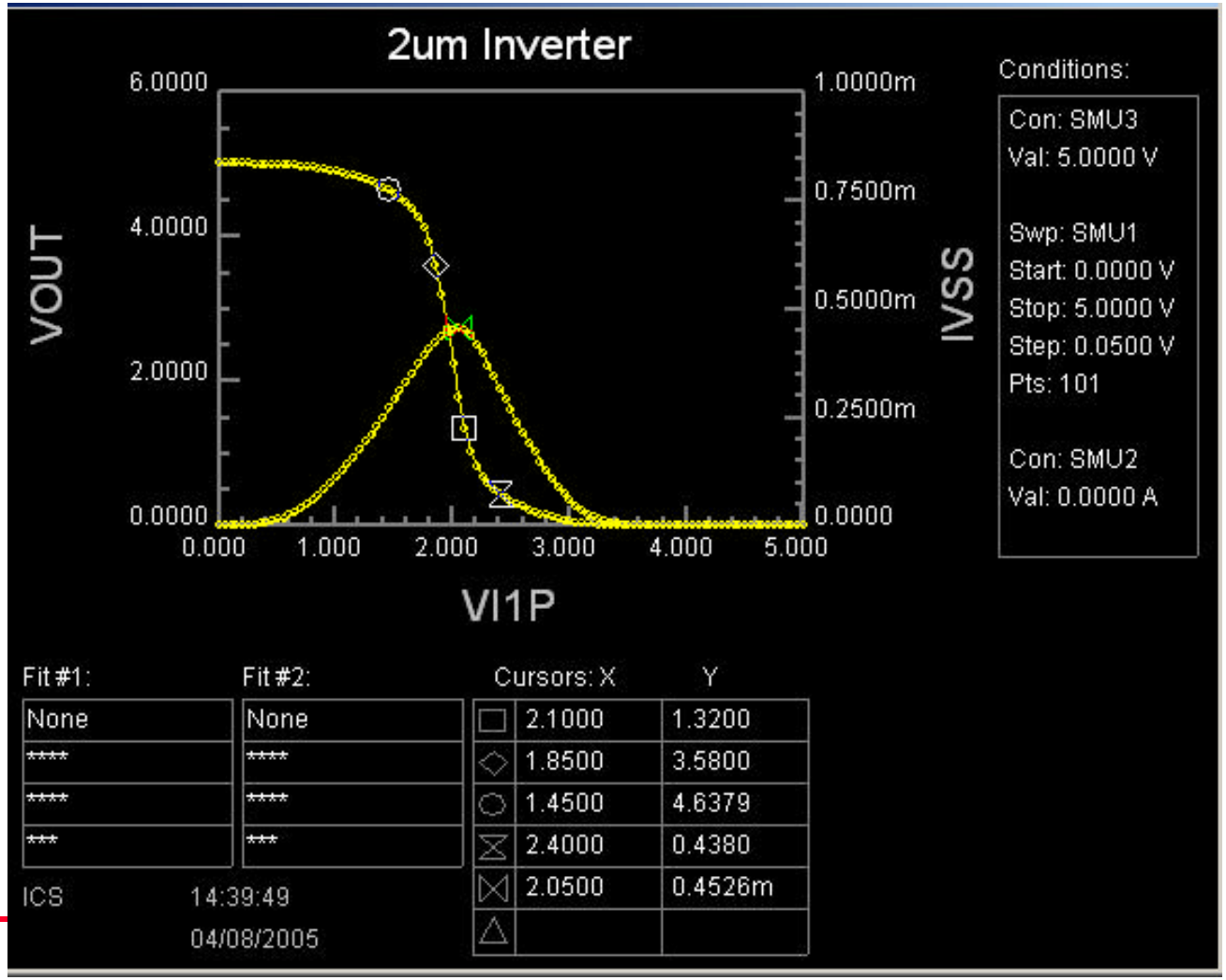




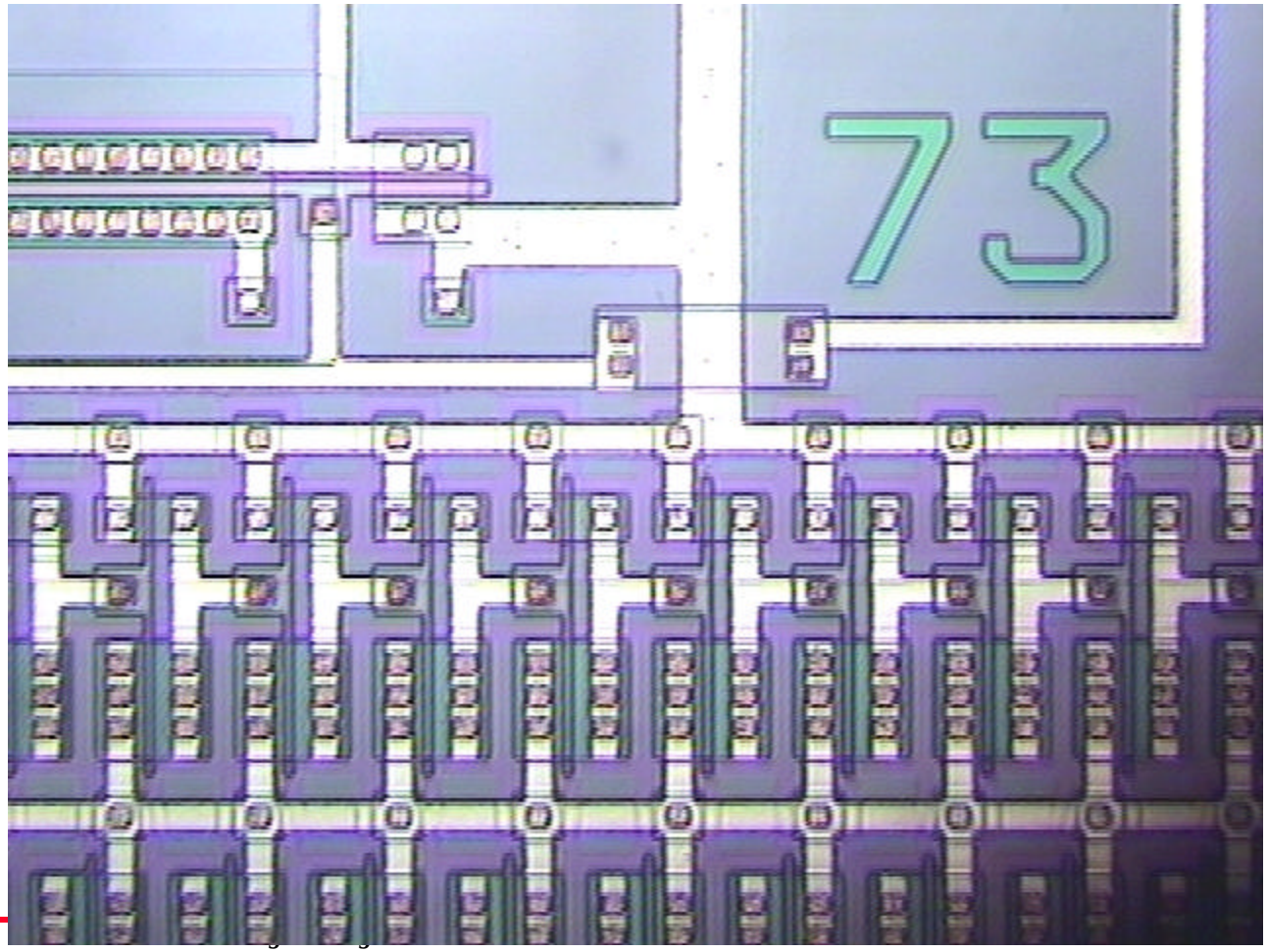
2µm INVERTER



2 µm INVERTER



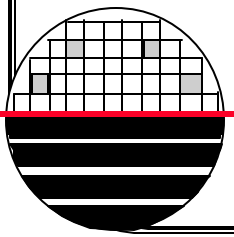
73 STAGE RING OSCILLATOR



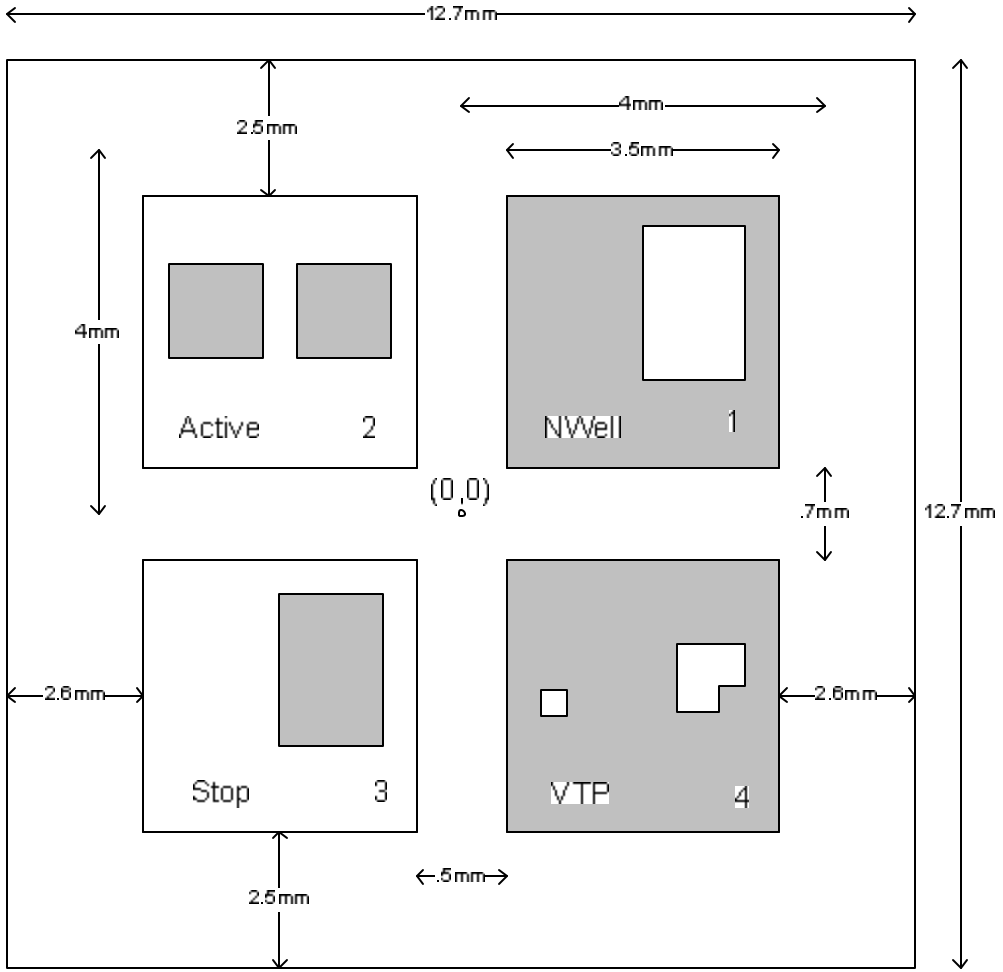
CANON STEPPER JOBS FOR 4-LEVELS/RETICLE

The objective of this project is to write stepper jobs for the Canon stepper that will allow the use of masks with four levels per quartz plate.

The key things that need to be changed are the masking blade positions in the shot file and shifts in the layout file. Four mask layers are placed on a single mask by placing the center of each layer 20 mm x 20 mm from the center of the quartz plate. This corresponds to a 4 mm x 4 mm shift on the wafer. The shifts are +4,+4 and +4,-4 and –4,+4 and –4,-4 depending on which quadrant is being printed. The blade positions are also different depending on which quadrant is being printed.

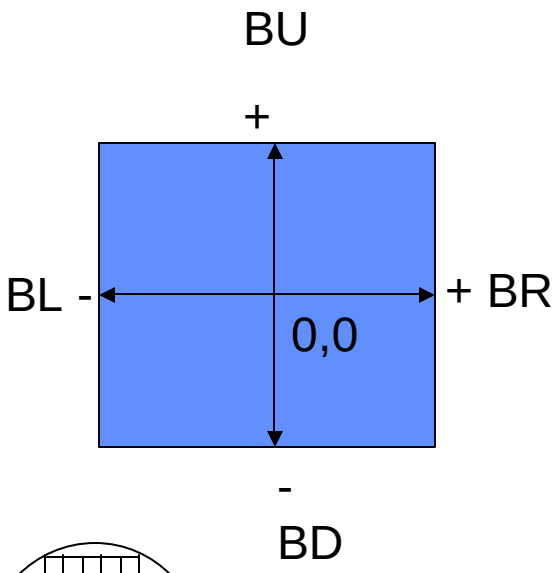


CANON STEPPER JOBS FOR 4-LEVELS/RETICLE



CANON STEPPER JOBS FOR 4-LEVELS/RETICLE

We named the Stepper Jobs:
Level 1: MIXED4X1_NWEL
Level 2: MIXED4X1_ACT
Level 3: MIXED4X1_STOP
Level 4: MIXED4X1_VT

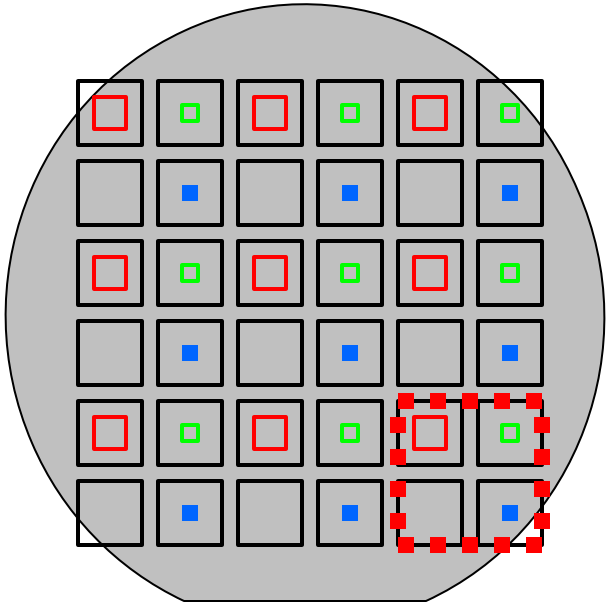


We named the Reticle File: RMIXED4X with the following reticle ID's and blade positions.

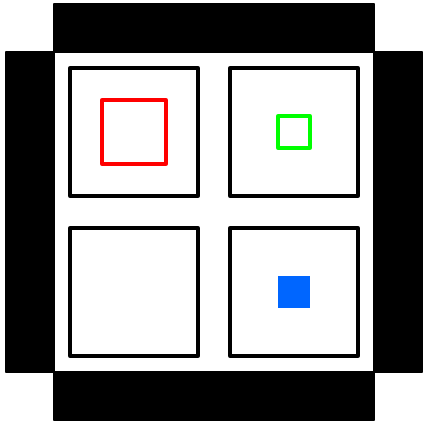
Level	BL	BR	BU	BD
RMIXED4X1	**-8**	**8**	**0**	**0**
RMIXED4X2	**0**	**8**	**8**	**0**
RMIXED4X3	**0**	**8**	**0**	**-8**
RMIXED4X4	**-8**	**0**	**0**	**-8**

UNDERSTANDING THE PROBLEM

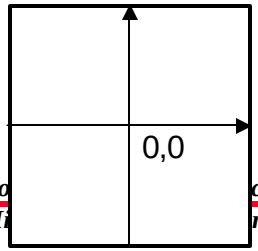
If Shot with Blades Open



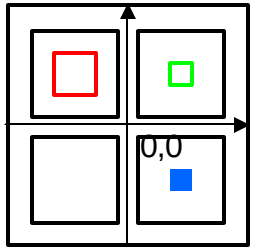
Blade Position

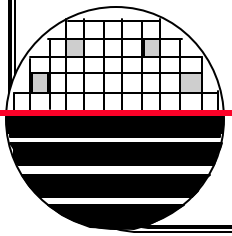


Normal Die Reference



4 Level Mask Die Reference





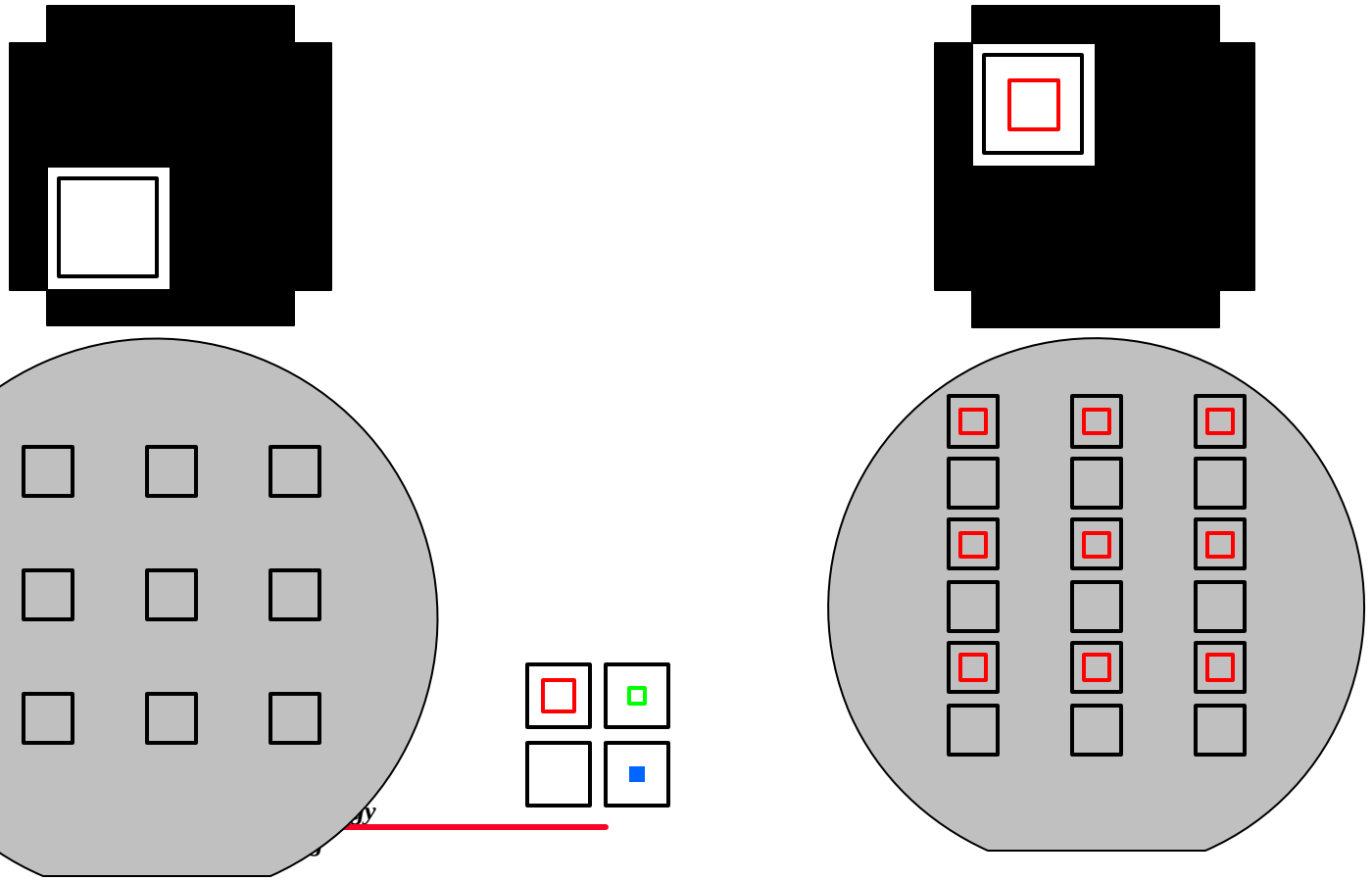
Ro chnology
Mi ring

UNDERSTANDING THE PROBLEM

If same layout file is used

Level 1

Level 2

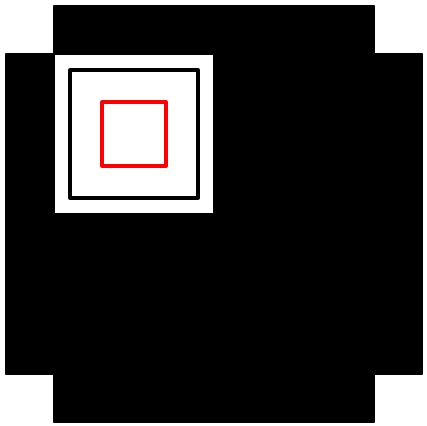


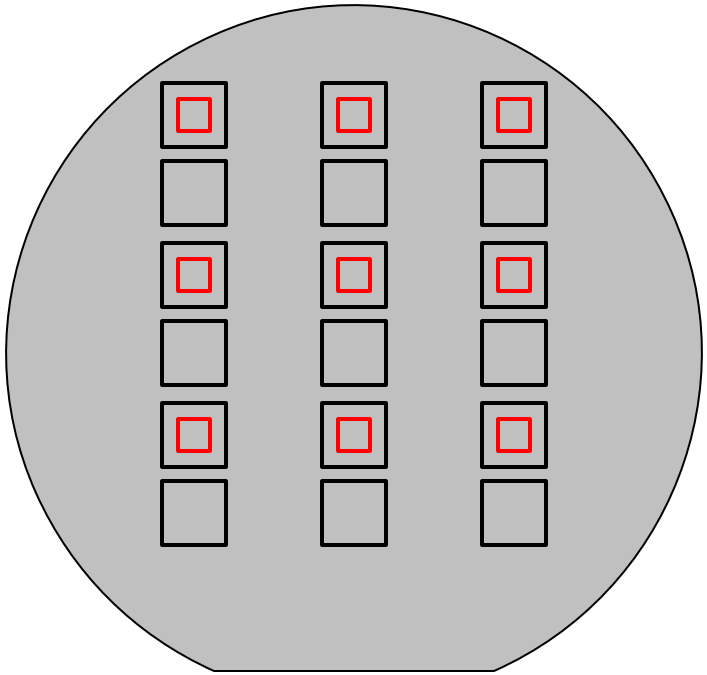
UNDERSTANDING THE PROBLEM

Need to include a layout (block) shift of successive levels (not shot shifting)

Duplicated the level 1 layout but include a layout shift

Shift Level 2 Down

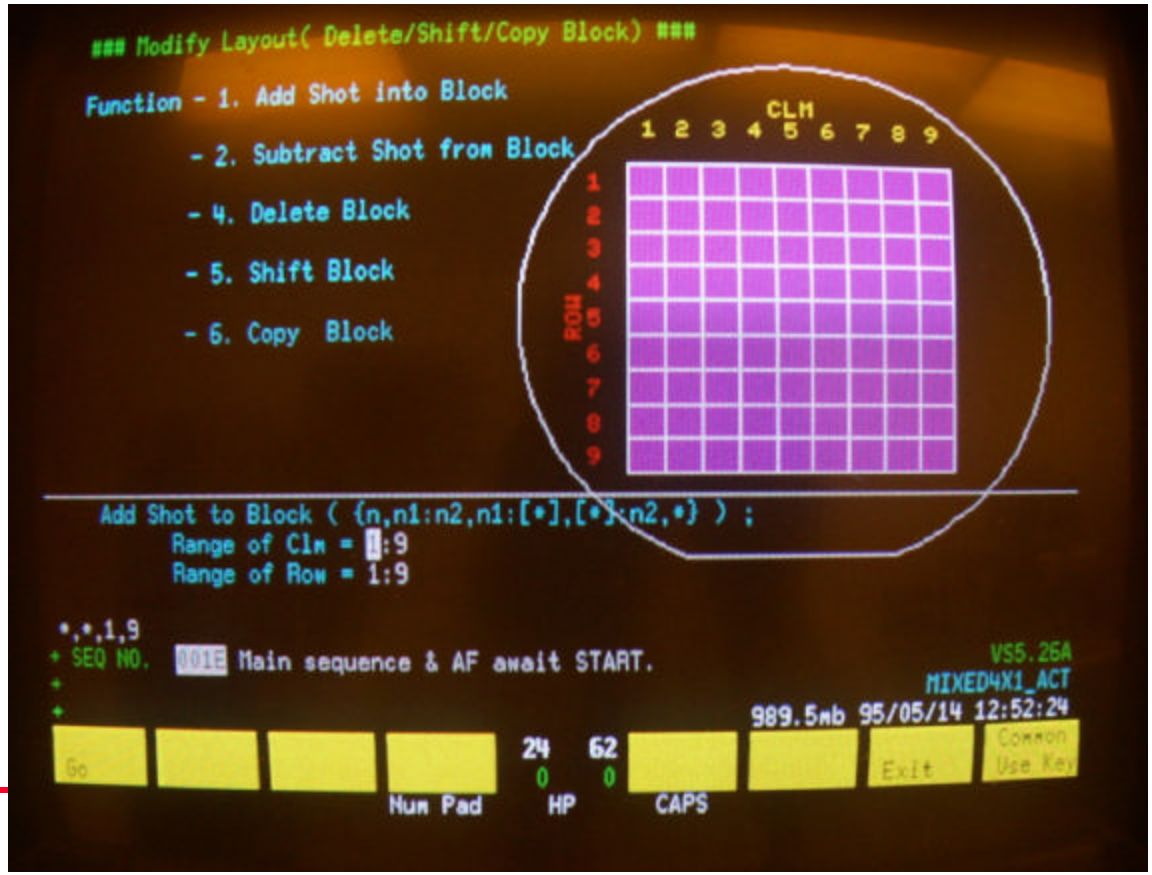




BLOCK SHIFTING

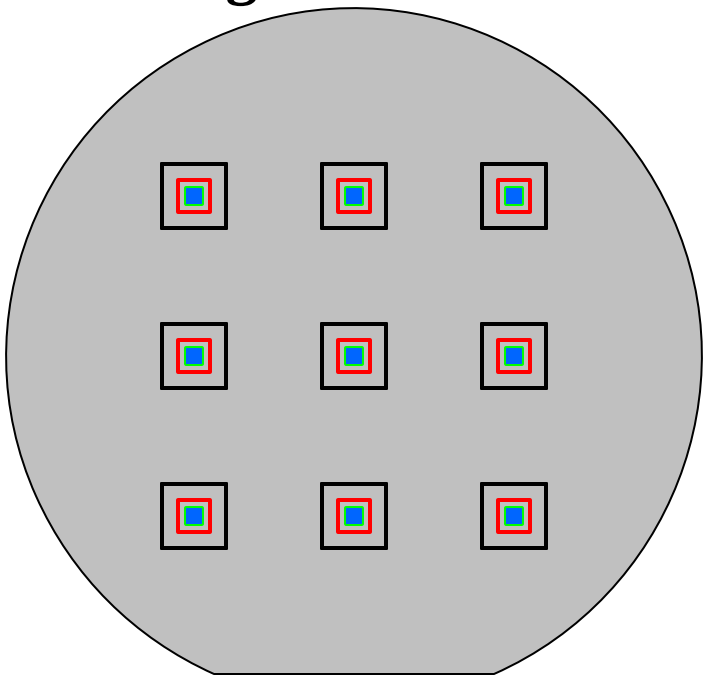
Copy level 1 layout file
Create Block and Shift

Edit layout>Create Block>Shift Block



LAYOUT SHIFTING

Similar shifting is done for higher levels

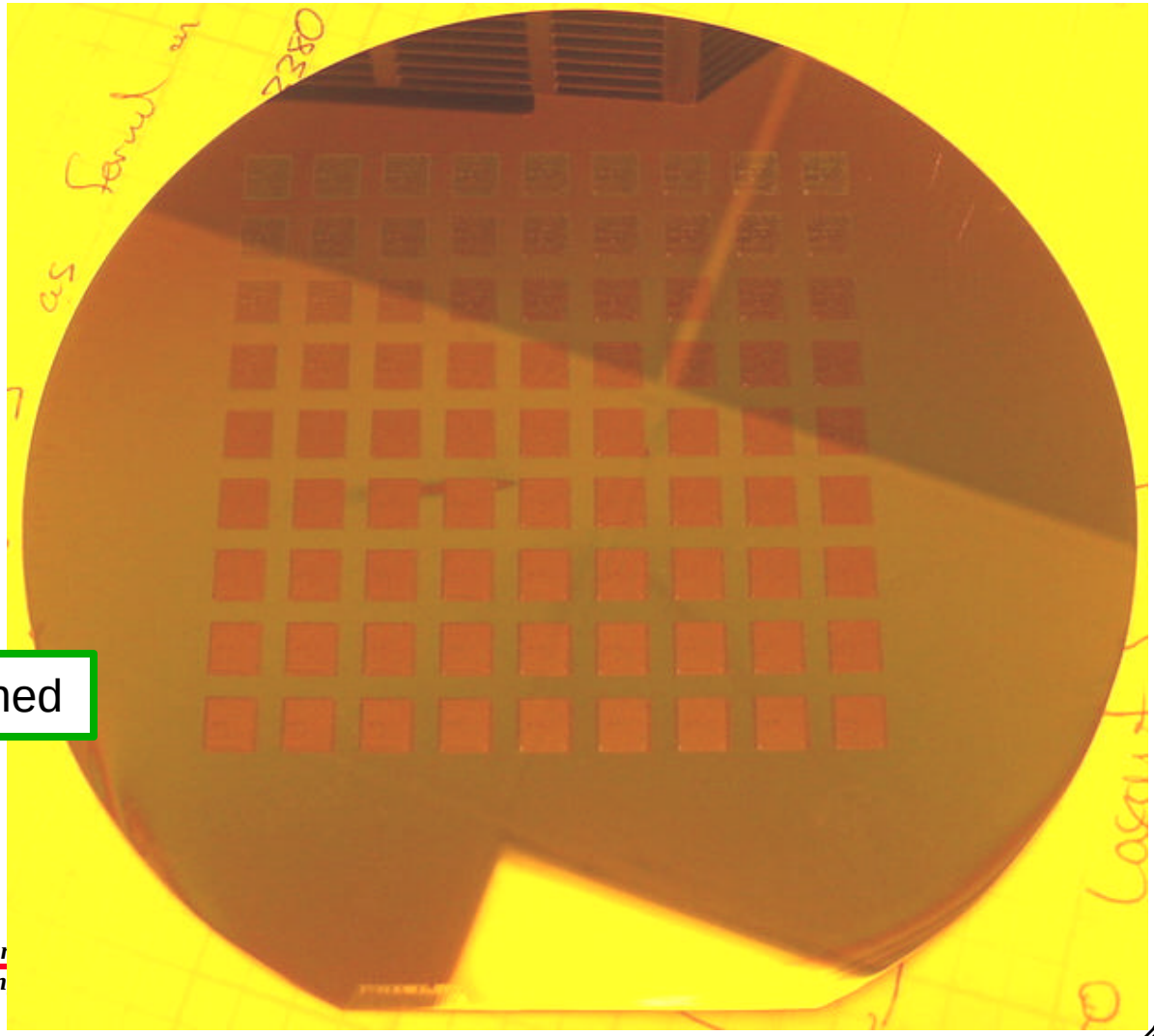


Because higher levels are shifted, need to add shift for TVPA mark locations in each level process file

RESULTS

Currently alignment with TVPA marks is successful

Work still needs to be completed with fine alignment marks



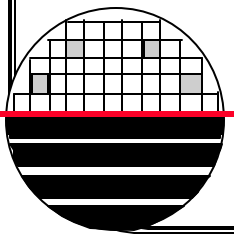
Both Levels Aligned

CONCLUSION

Successful alignment using TVPA marks has been accomplished using the 4x1 mask on the Canon Stepper

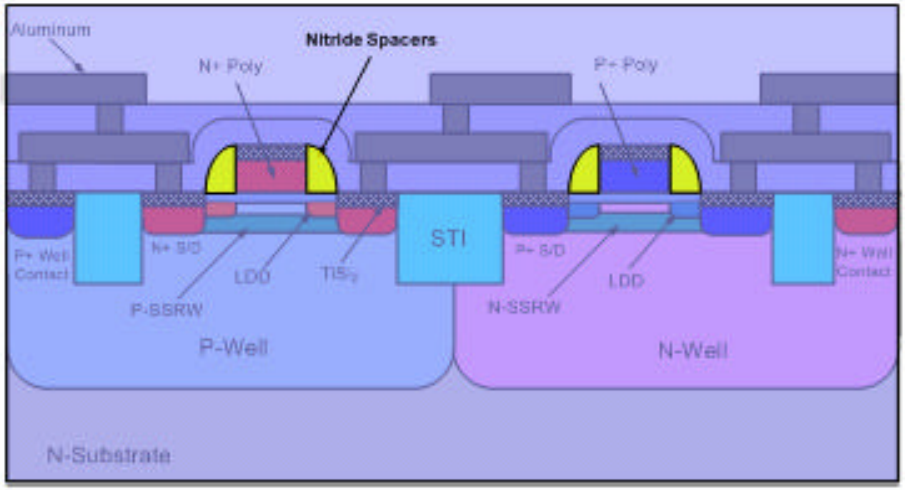
Work is still in progress on how to incorporated the use of the fine alignment marks

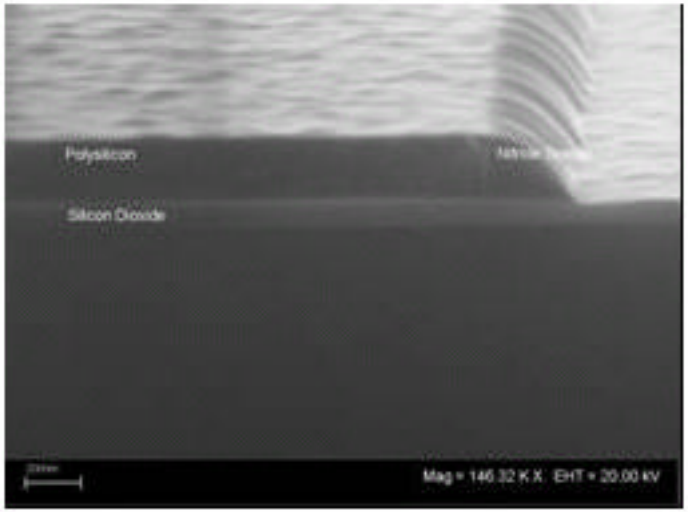
Robert Manley, May 16, 2005



INVESTIGATION OF ETCH UNIFORMITY

This project involved an investigation of the etch uniformity for the nitride sidewall spacer etch used in our advanced CMOS process.

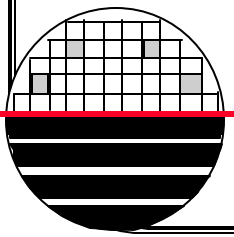




Swapnyl Shah, May 2005

PROCEDURE

1. Standard factory recipe to grow 500A gate oxide using Bruce 04.
2. Oxide measurement using Standard 5 point measurement on the wafer showed uniform 500A oxide growth.
3. Followed by 3500A Nitride deposition using ASM LPCVD tool.
4. The thickness measurement and deposition rate distribution profile was analysed on Tencor Spectramap. Mean thickness of 3044A with std deviation of 204.7A was measured on 24 pre-selected points.
5. Nitride was etched using the Drytech Quad, Reactive Ion etching system with wafer on **metal plate** and later using a **quartz plate** beneath the wafer . Pressure was set to 50 mTorr. Recipe ????
6. Half of the nitride was etched using a pre-determined etch rate of 1100A/min for 1.5 min and later analyzed for uniformity on the Tencor Spectramap.



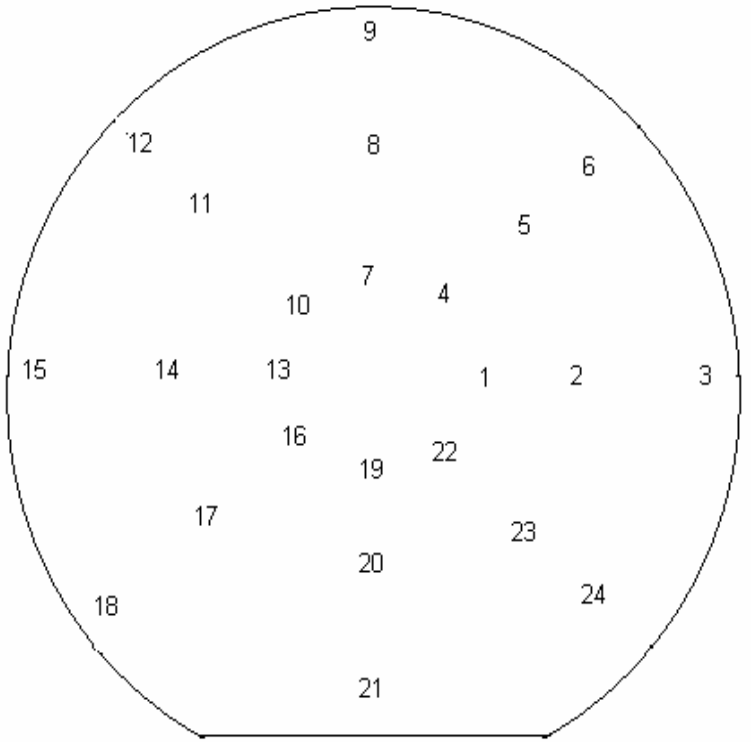
MEASUREMENTS

§The wafer placed with flats up during the Nitride deposition.

§Wafer placed with flats facing the user during etching nitride using the Drytech Quad.

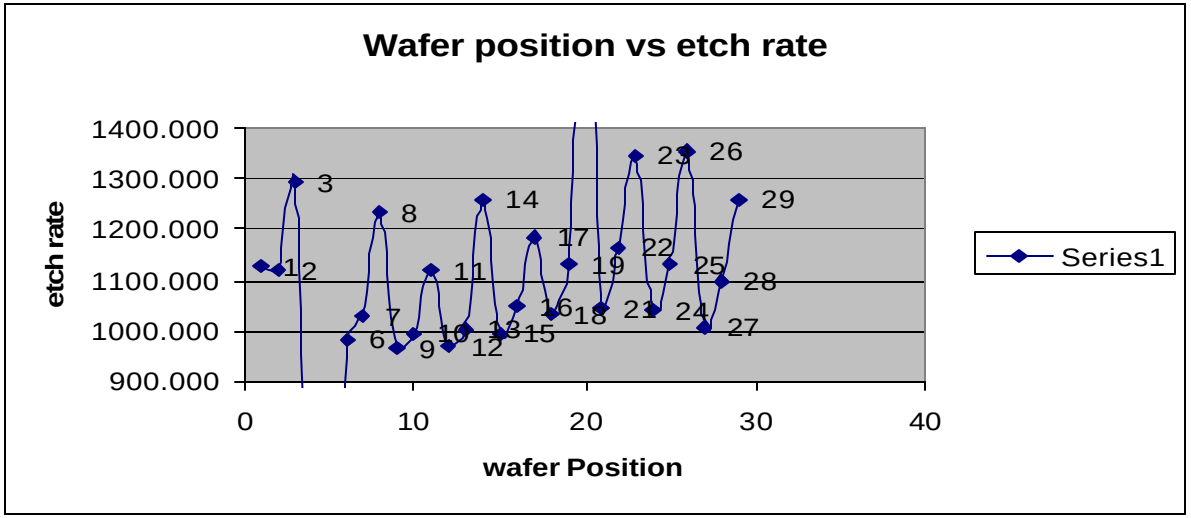
§Wafer placed with flats aligned to the plate on Spectramap and measurement taken on the following points.

§Wafer positioning very important during each step of wafer processing.

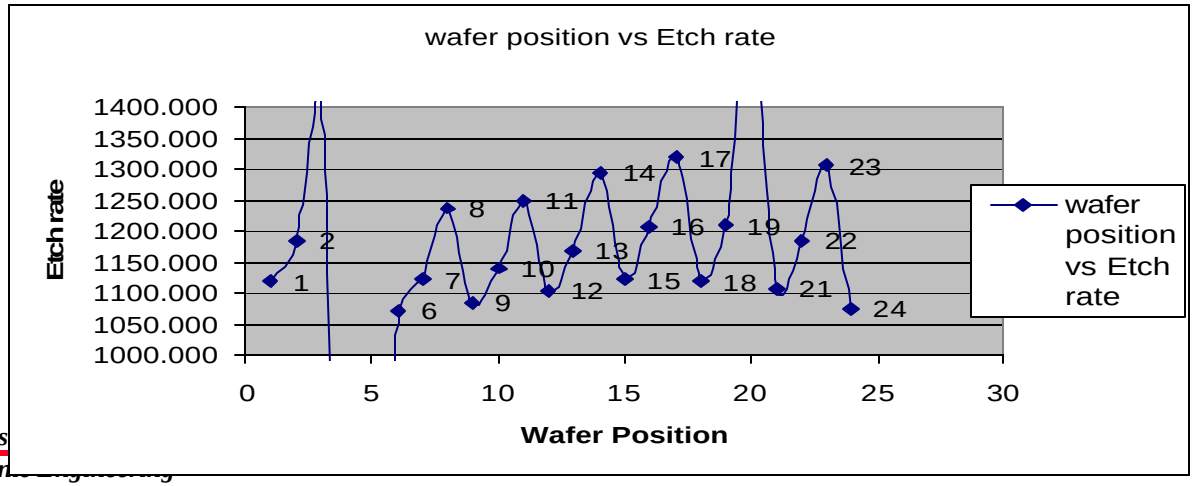


DATA

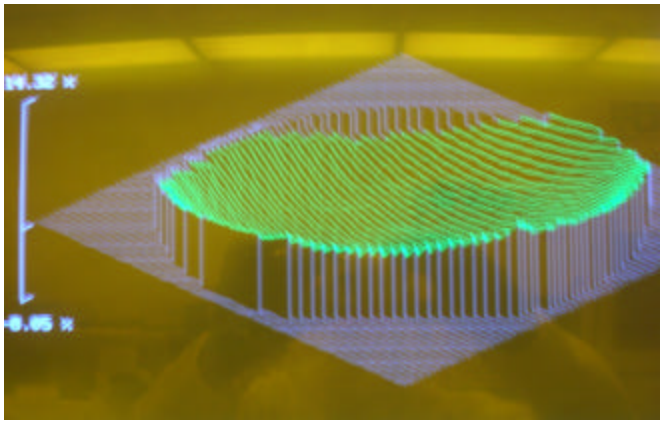
Wafer position Vs Etch rate for wafer #1 on **metal plate**



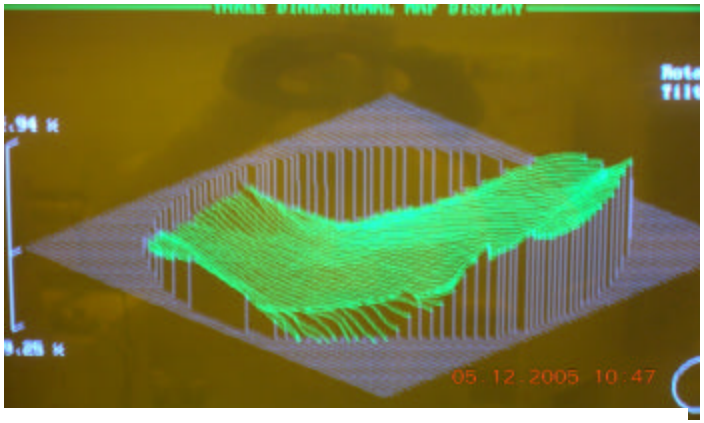
Wafer position Vs Etch rate for wafer #2 on **quartz plate**



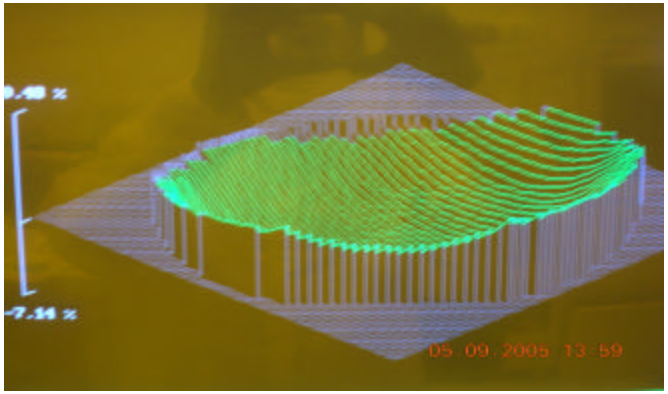
SPECTROMAP RESULTS



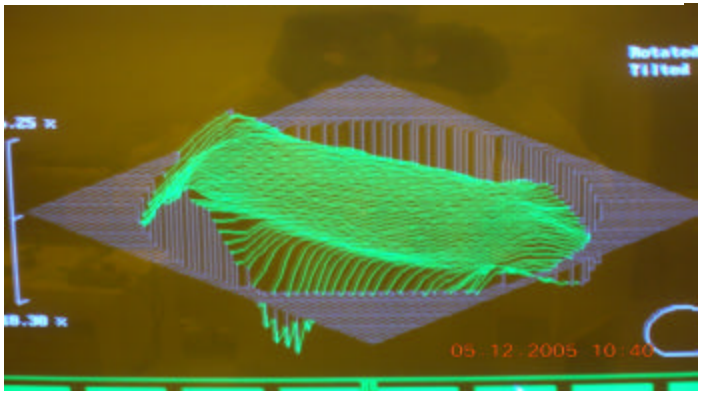
Wafer 1 after nitride dep



Wafer 1 after nitride etch



Wafer 2 after nitride dep



Wafer 2 after nitride etch

DATA

Wafer # 1 **(on Metal Plate)**

Data on all points:
Average Etch rate: 1141.55 A
Max Etch rate: 1897.1 A
Min : 964.53 A
Non uniformity percentage: 32.58 A

Data on standard factory 5 points:
Average Etch rate: 1201.88 A
Max Etch rate: 1346.8 A
Min : 1117.13 A
Non uniformity percentage: 9.32 %

Wafer # 2 **(on Quartz Plate)**

Data on all points:
Average Etch rate: 1190.89 A
Max Etch rate: 1541.06 A
Min : 1069.53 A
Non uniformity percentage: 18.06 A

Data on standard factory 5 points:
Average Etch rate: 1246.54 A
Max Etch rate: 1319.93 A
Min : 1117.26 A
Non uniformity percentage: 8.316 %

Swapnyl Shah, May 2005

CONCLUSION

§ The uniformity of nitride etching at the Drytech Quad increases by 1% using the quartz plate.

§ Overall, the etching mechanism using Drytech Quad is not very uniform and needs some changes in recipe of the Quad.

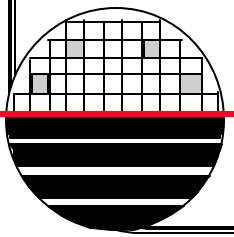
Rochester Institute of Technology
Microelectronic Engineering

Mike Aquilino

Simulation of Threshold Adjustment Implant for the Advanced CMOS Process at RIT

The objective is to do SUPREM simulations to determine the correct threshold adjust implants for the RIT Advanced CMOS Process.

Michael Latham, May 2005



HAND CALCULATIONS

CONSTANTS		VARIABLES			CHOICES	1=yes, 0=No	
T=	300 K	Na =	1.00E+17	cm-3	Aluminum gate	0	Select one type of gate
KT/q =	0.026 volts	Nd =	1.00E+17	cm-3	n+ Poly gate	1	
ni =	1.45E+10 cm-3	Nss =	1.00E+11	cm-2	p+ Poly gate	0	
Eo =	8.85E-14 F/cm	Xox =	100	Ang	N substrate	0	Select one type of substra
Er si =	11.7				P substrate	1	
Er SiO2 =	3.9						
E affinity =	4.15 volts				Desired VT	0.75	
q =	1.60E-19 coul				or		
Eg =	1.124 volts				Delta VT	20	
					Given Dose (Boron)	1.30E+12	

CALCULATIONS:		RESULTS			
METAL WORK FUNCTION	=	4.122988528	volts		
SEMICONDUCTOR POTENTIAL	= +/-	0.409409834	volts		
OXIDE CAPACITANCE / CM2	=	3.4515E-07	F/cm2	Wdmax =	0.103 µm
METAL SEMI WORK FUNCTION DIFF	=	-0.998421306	volts		
FLAT BAND VOLTAGE	=	-1.044777963	volts		
THRESHOLD VOLTAGE	=	0.25126959	volts		
DELTA VT = VTdesired - VT	=	0.49873041	volts		
IMPLANT DOSE	=	1.07586E+12	ions/cm2	x 2 =	2.15171E+12
where + is Boron, - is Phosphorous					
IMPLANT DOSE FOR GIVEN Delta VT	=	4.31438E+13	ions/cm2	x 2 =	8.62875E+13
Vt WITH GIVEN DOSE	=	0.552587857	volts	assume 1/2 dose in Si	

UNADJUSTED THRESHOLD VOLTAGES

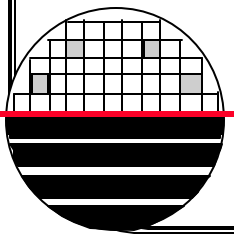
N-MOSFET VT, Nss=1E11, Xox=100 A, Na=1E17,
VT=0.25

Dose=1.07E12 x 2 = 2.15E12 Boron

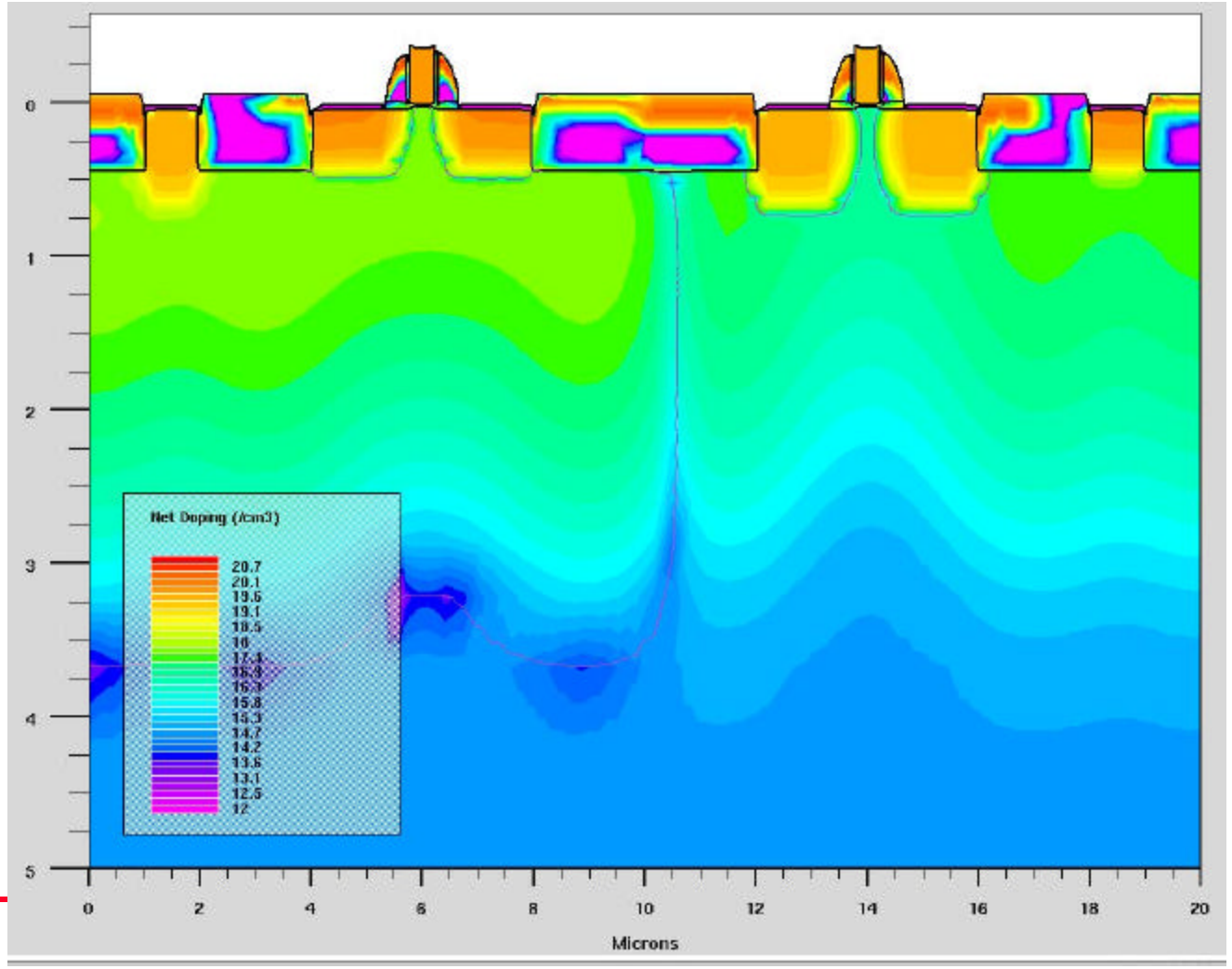
P-MOSFET VT, Nss=1E11, Xox=100 A, Nd=1E17,
VT=-0.34

Dose=8.76E11 x 2 = 1.75E12 Phosphorous

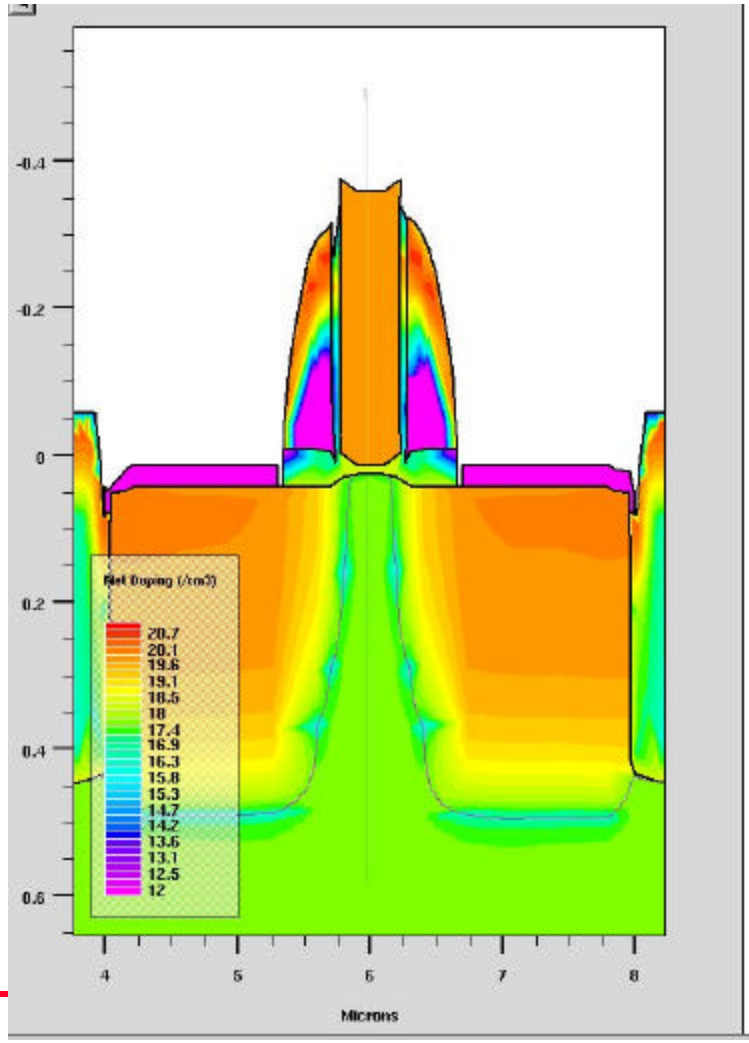
Note: we want +0.75 and –0.75 volts

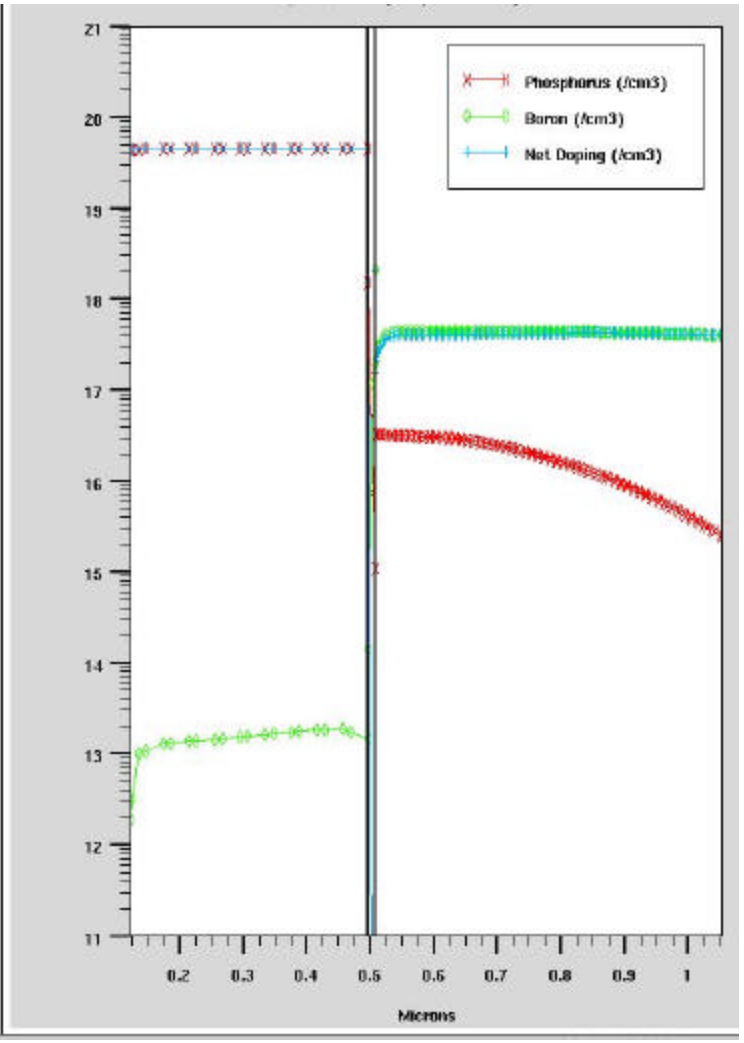


SIMULATIONS

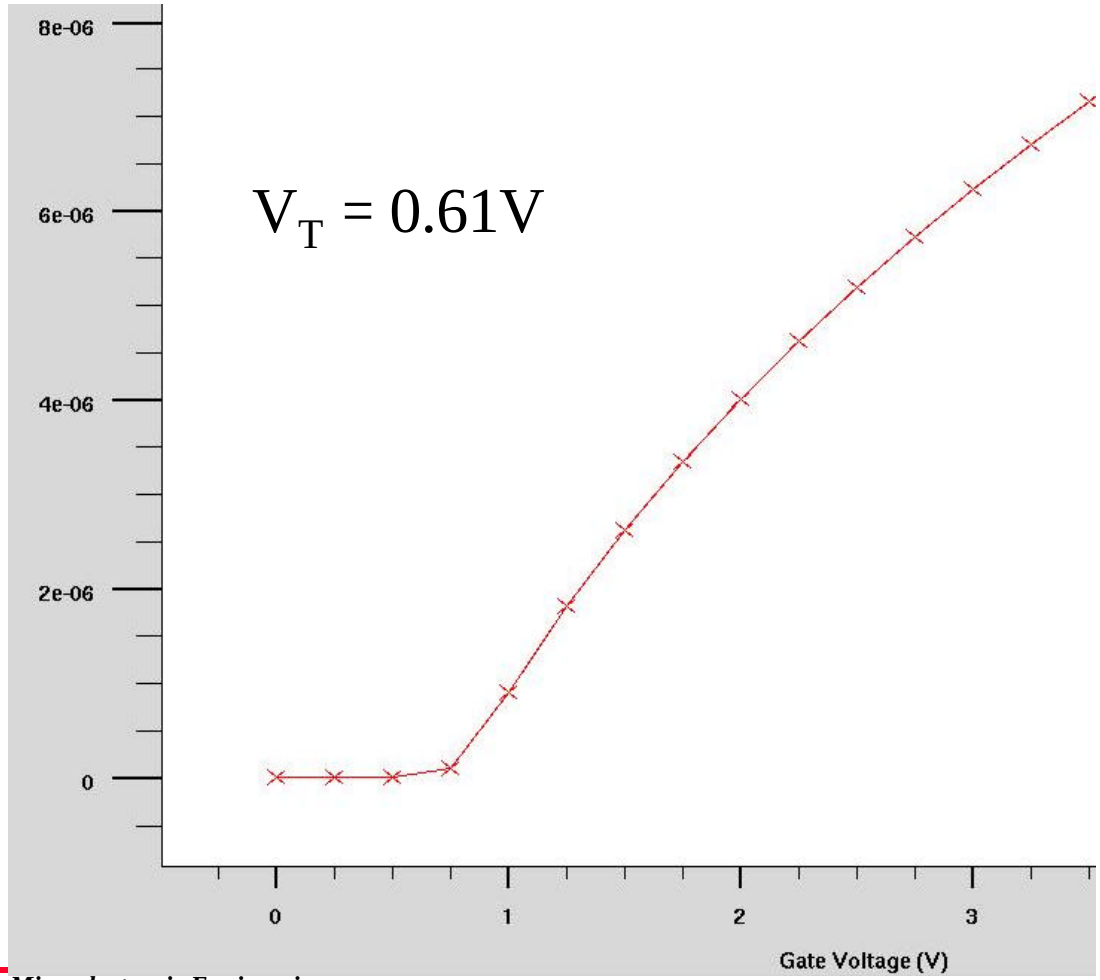


NMOS





NMOS-$I_D V_G$



V_T = 0.61V

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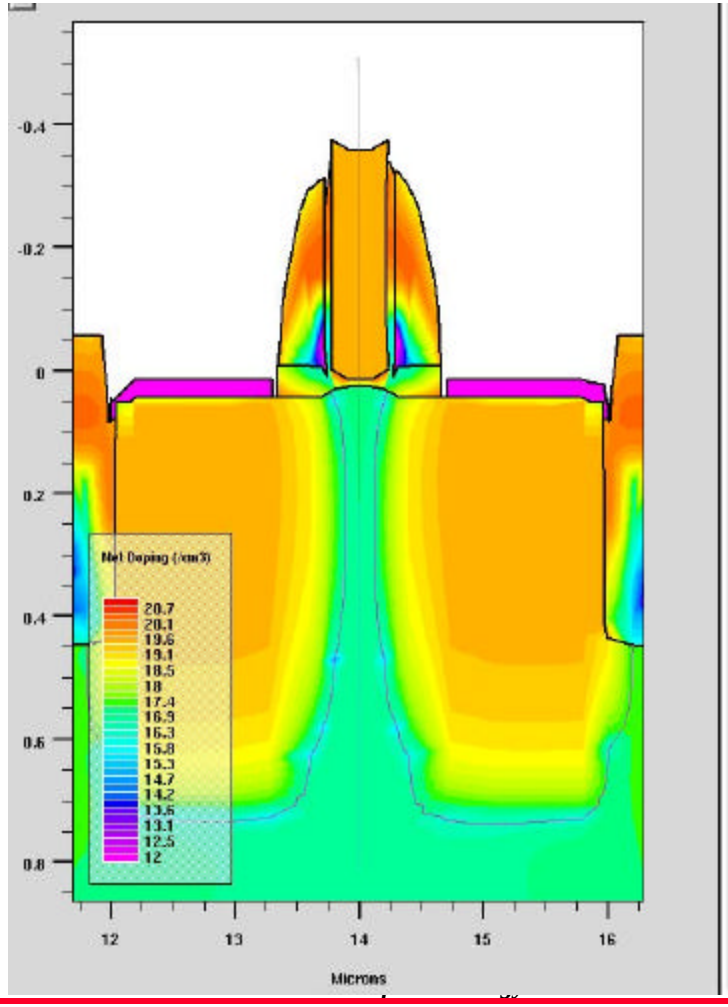
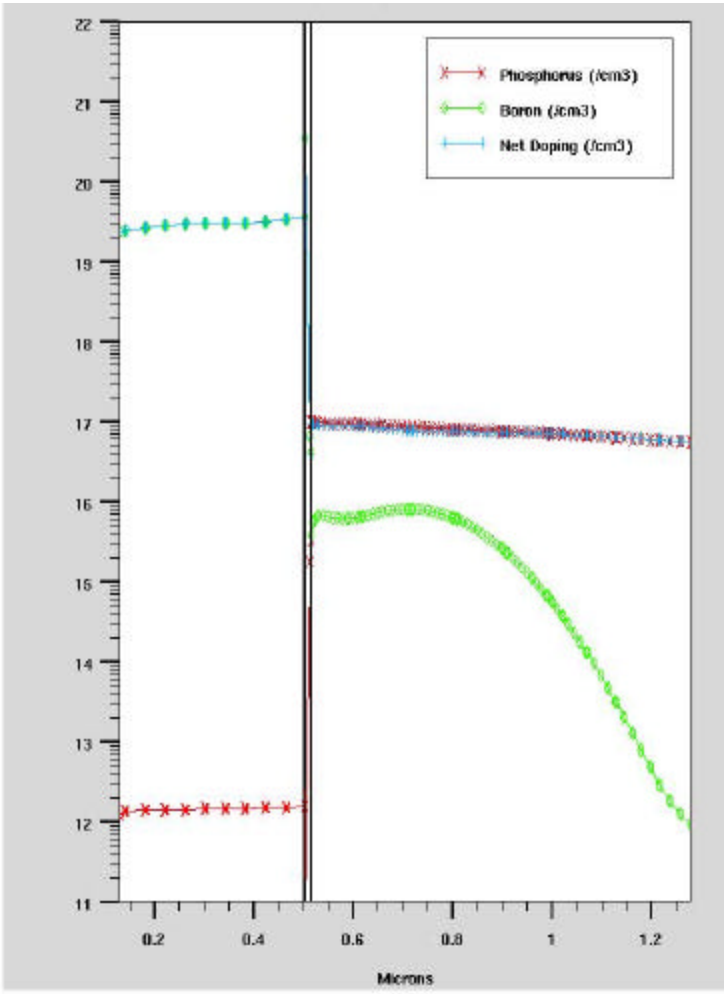
PMOS





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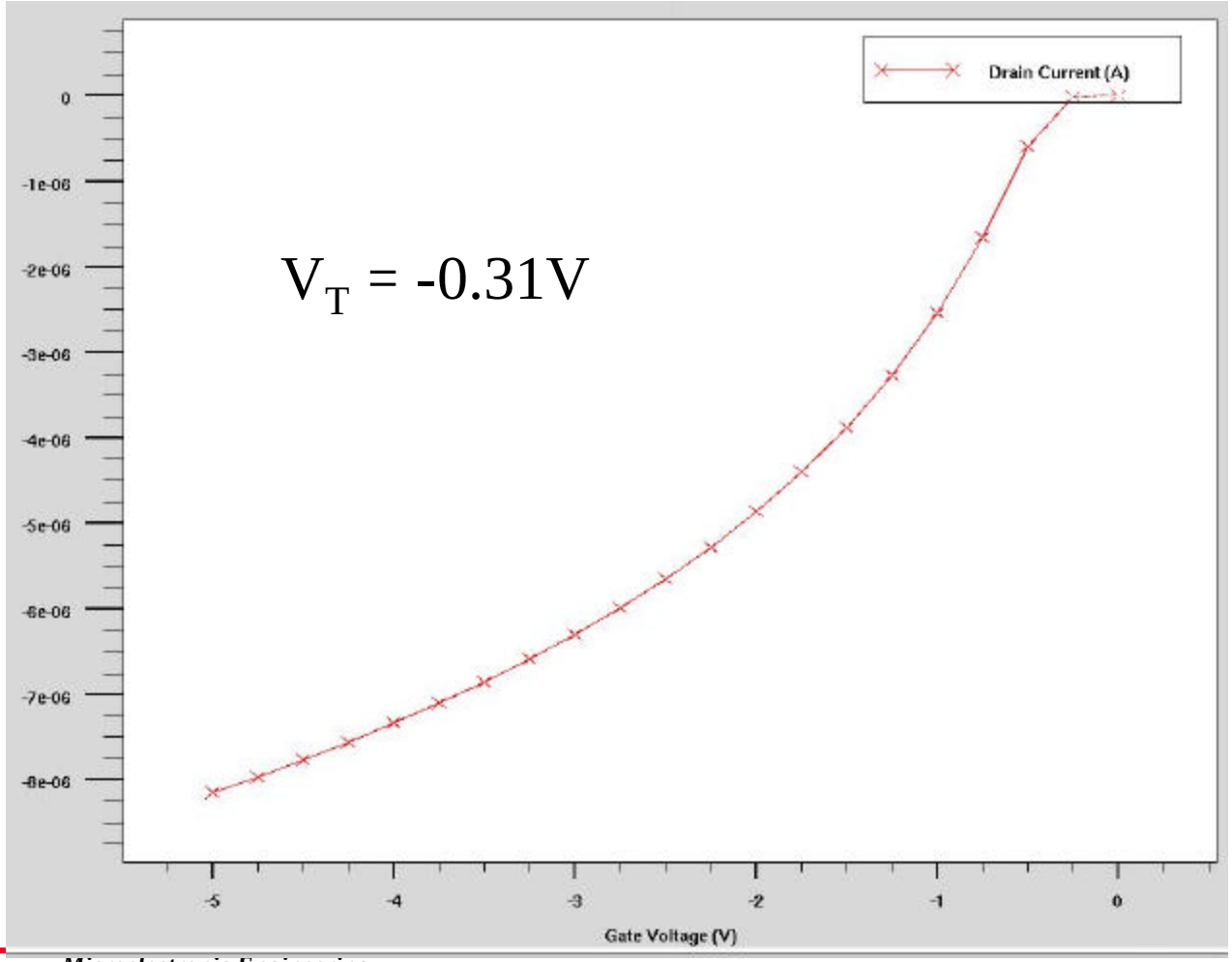
PMOS $I_D V_G$



V_T = -0.31V

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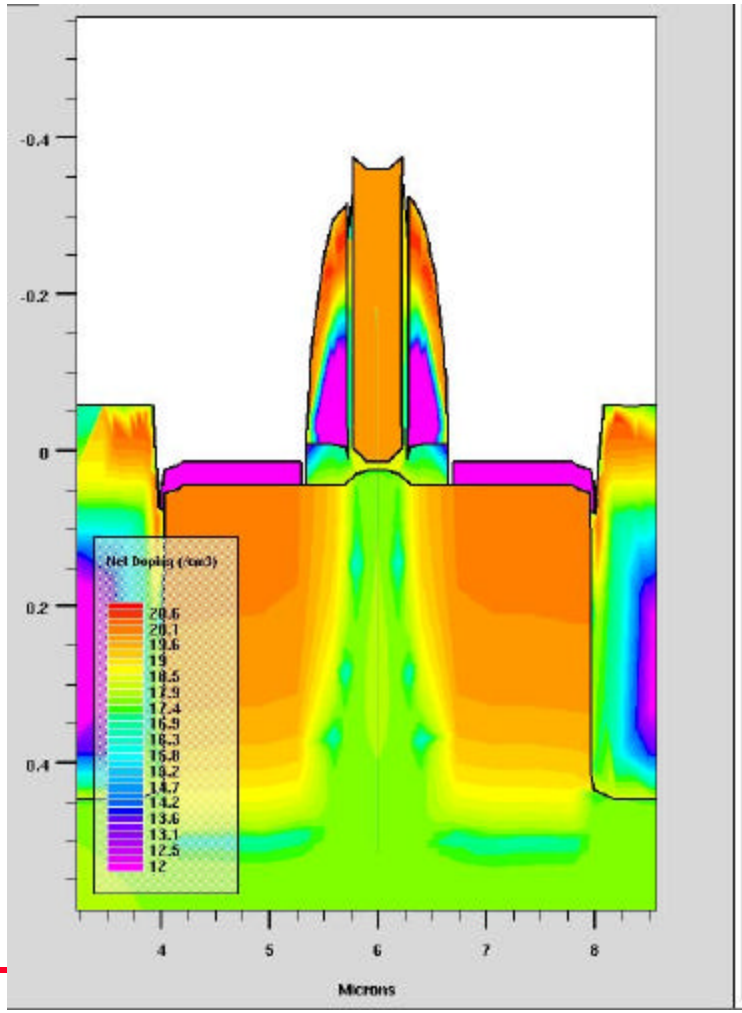
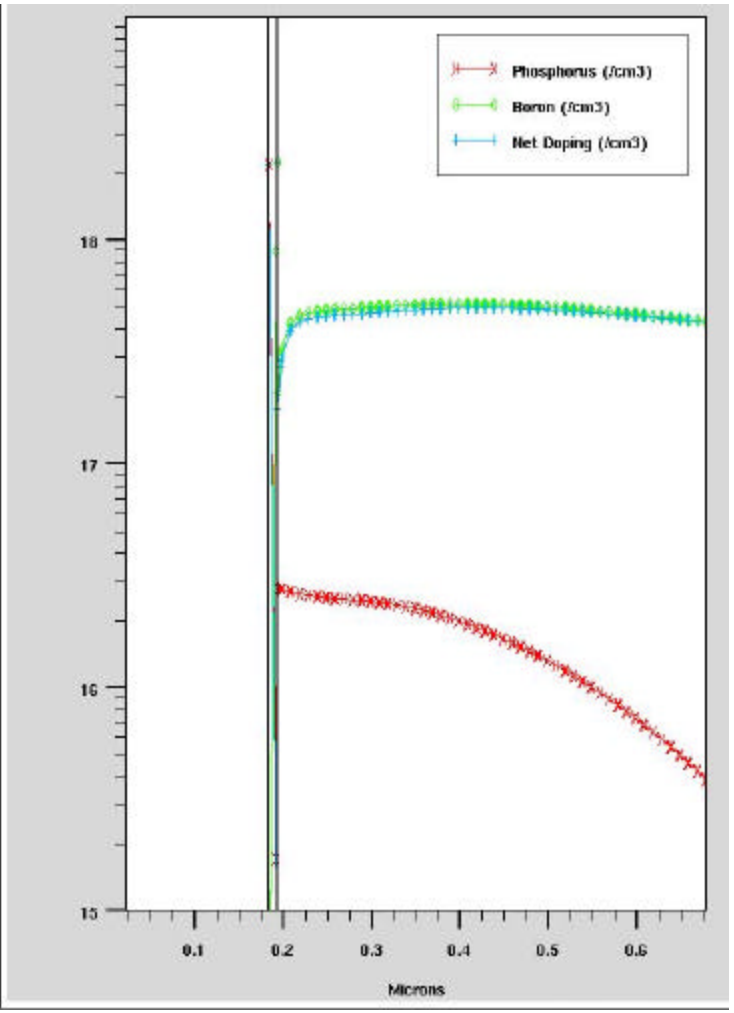
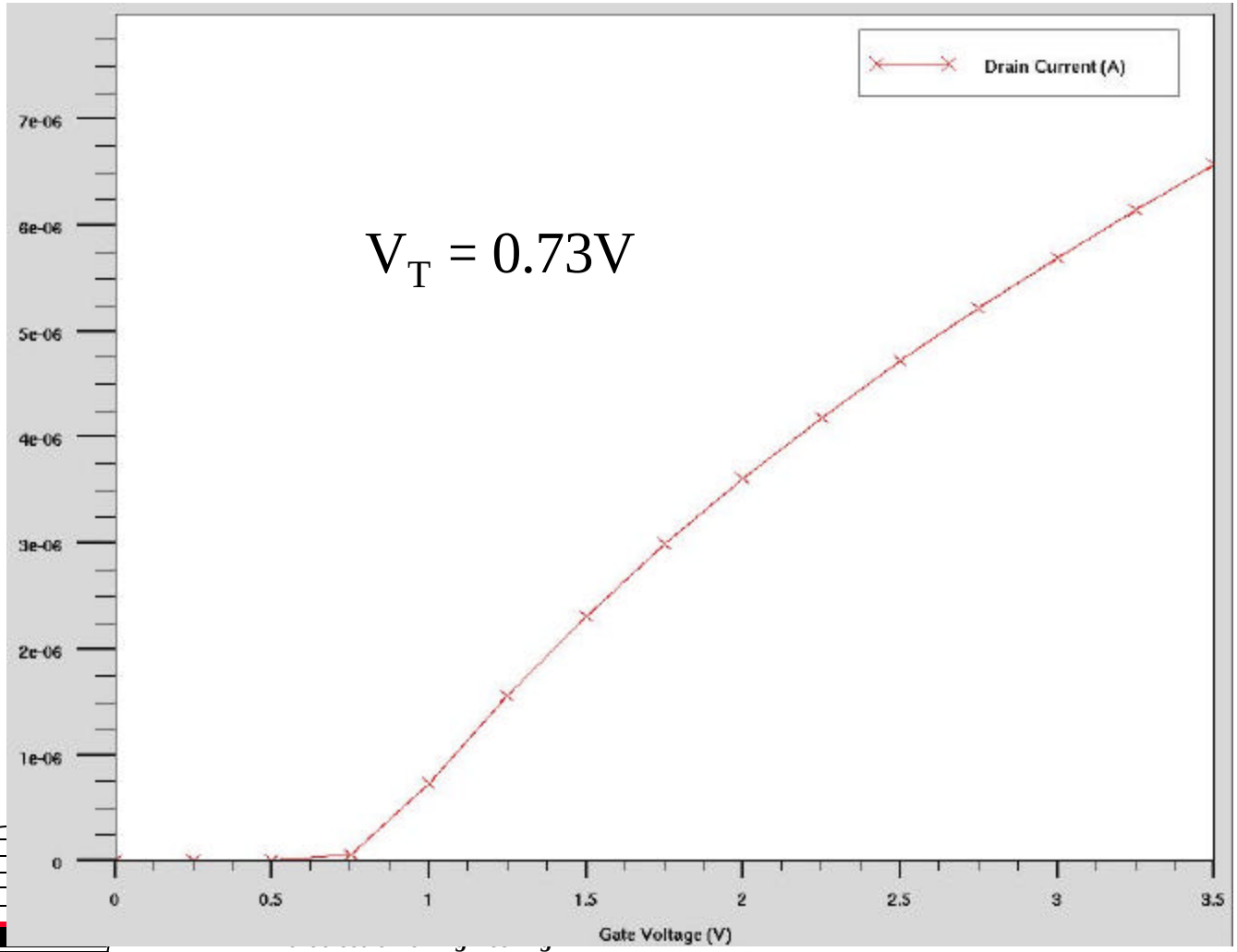
NMOS





NMOS – $I_D V_G$

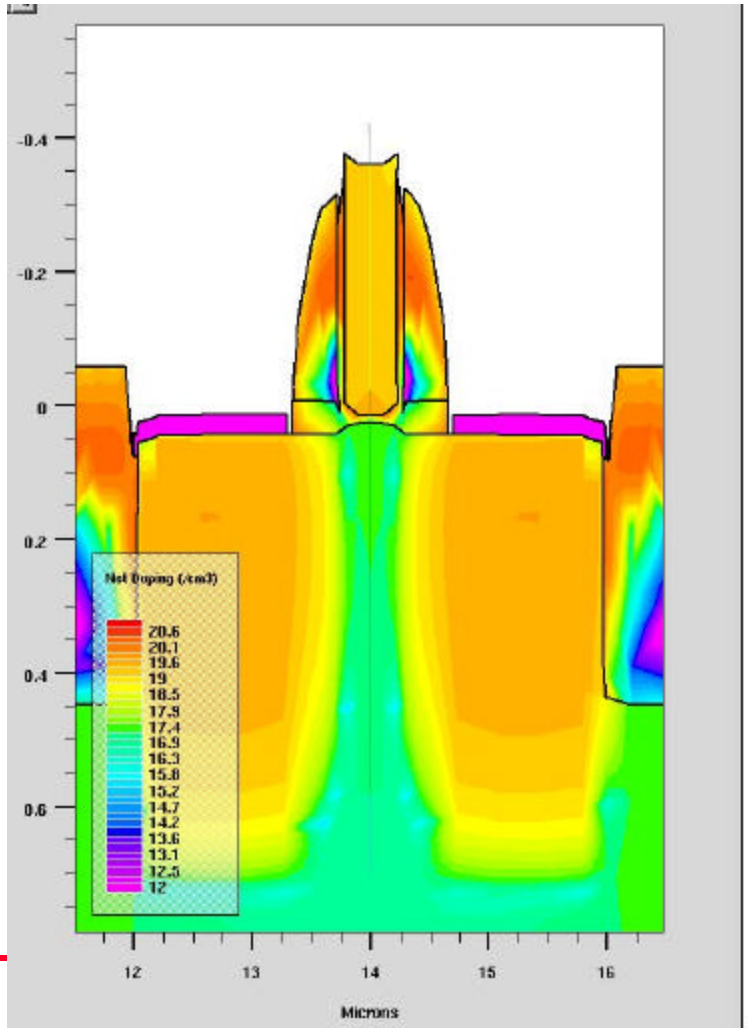


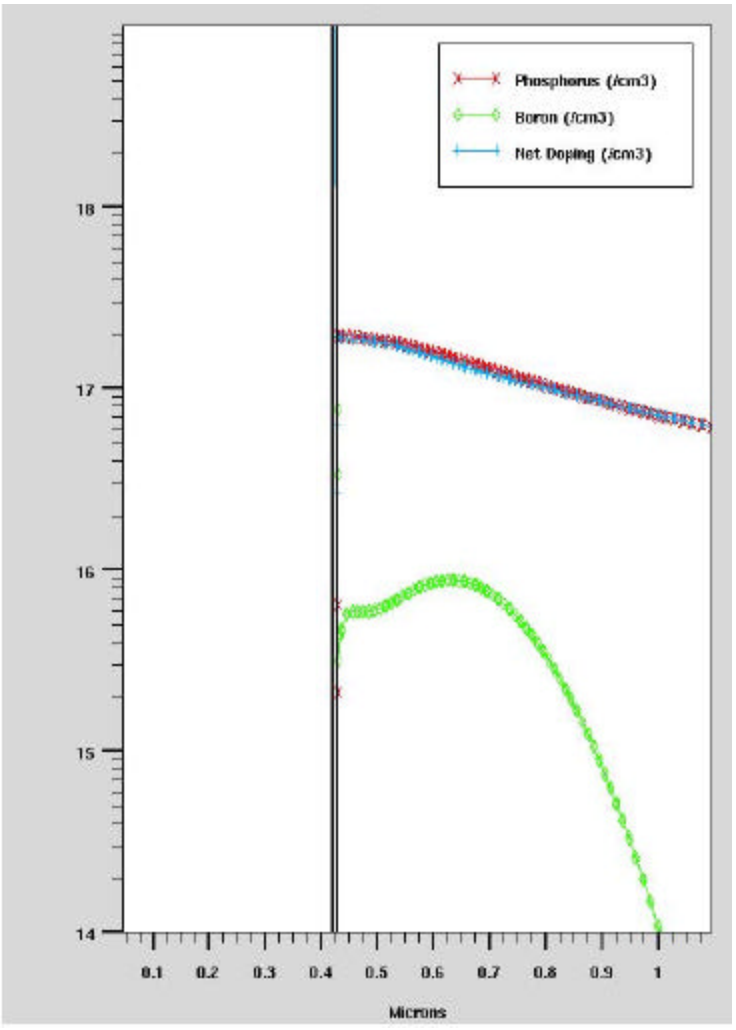
$V_T = 0.73V$

V_T Adjust Implant:

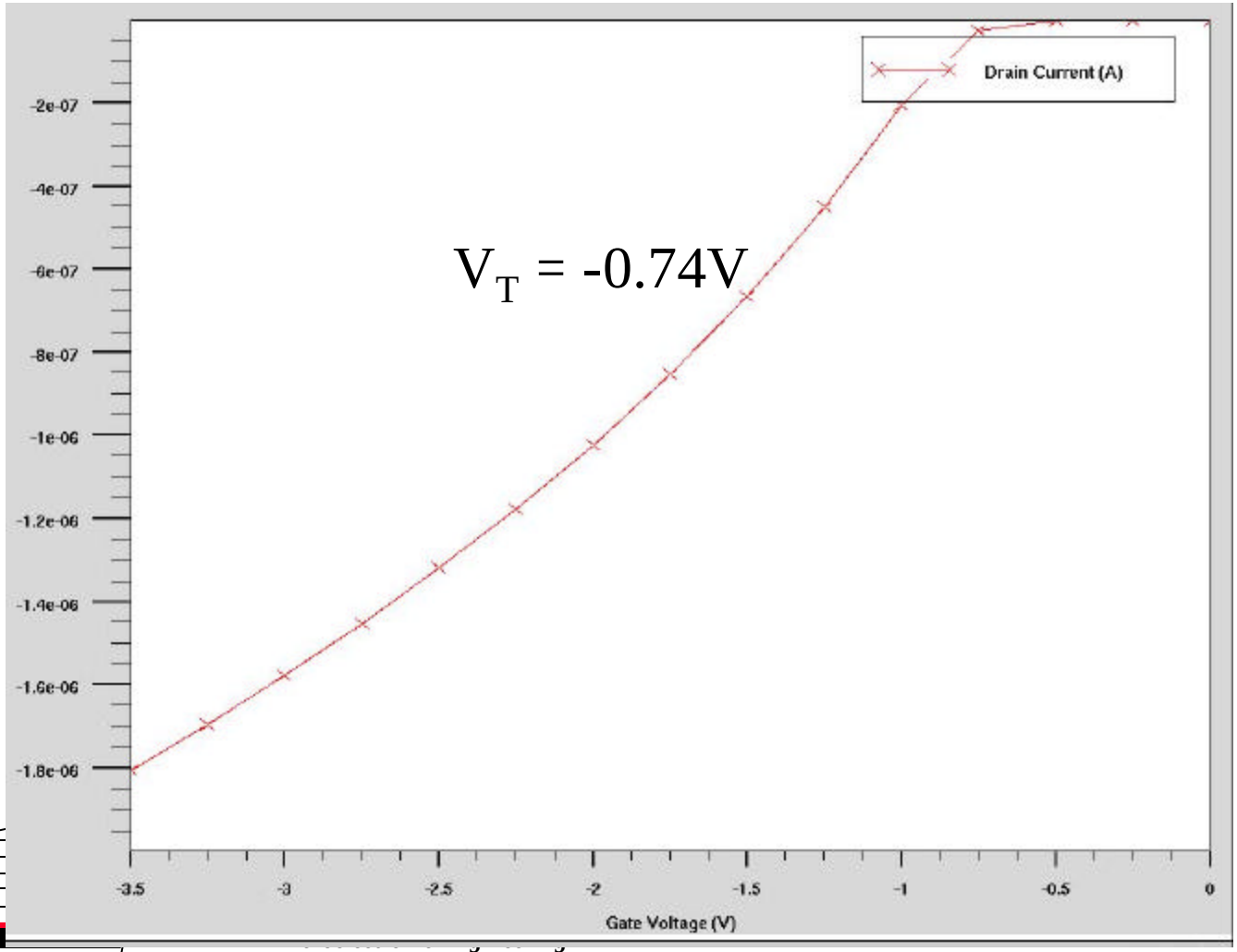
- oBoron
- o30KeV
- o3.0E12 cm^{-2}

PMOS





PMOS – $I_D V_G$



V_T = -0.74V

V_T Adjust Implant:

- Phosphorus
- 60KeV
- 3.5E12 cm^{-2}

CONCLUSION

NMOS

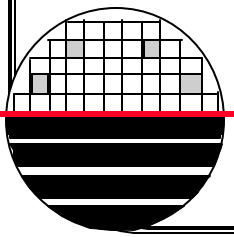
V_T: 0.73V

V_T Adjust Implant: 30KeV B_{11}, 3E12cm^{-2} Dose

PMOS

V_T:-0.74V

V_T Adjust Implant: 60KeV P_{31}, 3.5E12cm^{-2} Dose



REFERENCES

1. “Silicon Processing”, Stanley Wolf
2. EMCR650 lecture notes on line at http://www.rit.edu/~lffeee