

**MICROELECTRONIC ENGINEERING
ROCHESTER INSTITUTE OF TECHNOLOGY**

**Advanced CMOS Process Technology
Part 1 and 2**

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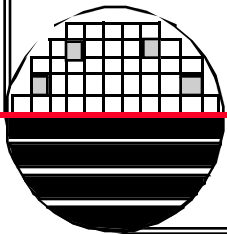
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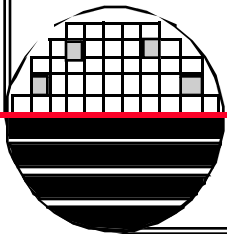
Devices for 0.15 μm CMOS

High Performance Sub 0.1 μm Channel nMOSFET's

Sub - 1/4 μm Dual-Gate CMOS Technology

High-Performance 0.07 - μm CMOS

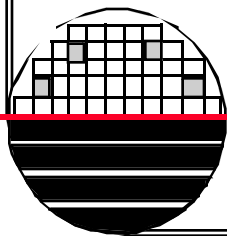
Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFET



High-Performance Devices for a 0.15- μm CMOS Technology

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Abstract—Devices have been designed and fabricated for a CMOS technology with the nominal channel length of 0.15 μm and minimum channel length below 0.1 μm . In order to minimize short-channel effects (SCE's) down to channel lengths below 0.1 μm , highly nonuniform channel dopings (obtained by indium and antimony channel implants) and shallow source-drain extensions/halo (by In and Sb preamorphization and low-energy As and BF_2 implant) were used. Maximum high V_{DS} threshold rolloff was 250 mV at effective channel length of 0.06 μm . For the minimum channel length of 0.1 μm , the loaded ($F_I = F_O = 3$, $C_L = 240$ fF) and unloaded delays were 150 and 25 ps, respectively.



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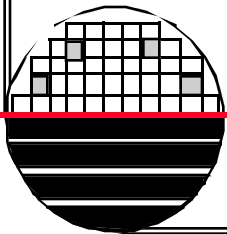
I. INTRODUCTION

DEEP-submicrometer CMOS is the main technology for ULSI systems. Presently the state-of-the-art CMOS is a 0.25- μm CMOS operating at 2.5 V [1]. As the CMOS technology is extended into the deep-submicrometer range, it is estimated that the next generation will have a nominal channel length of 0.15 μm . In such a technology, devices with L_{eff} less than 0.1 μm should have acceptable threshold voltage rolloff and off current. Control of the short-channel effects (SCE's) is one of the most critical issues faced when scaling into submicrometer range [2], [3]. In this paper devices with excellent SCE down to below 0.1 μm , demonstrating their potential for use in a 0.15- μm CMOS technology, are presented. In order to contain the SCE, a highly nonuniform channel doping [4], and very shallow extensions/halo were used. At the same threshold, the nonuniform channel doping results in a superior SCE when compared to a uniform channel doping [4]. The use of source-drain extensions/halo obtained by low-energy implants and In (for nMOS) and Sb (for pMOS) preamorphization result in an improved SCE, a reduced source-drain resistance, and a lower overlap capacitance.

II. PROCESS TECHNOLOGY

Both nMOS and pMOS were surface channel devices, fabricated in a twin-well CMOS process on p^-/p^+ epi. Indium and antimony were used in the wells to obtain a highly nonuniform channel dopant profile in order to minimize SCE's. Energies of about 190 keV resulted in the best SCE. Fig. 1(a) is a SIMS of channel implant used for nMOS and pMOS: the In and Sb channel implant peaks were placed at about 100 nm under the channel. Background dopings in the range from 1×10^{17} to 4×10^{17} were examined, and it was found that SCE was not affected significantly by the background doping over that range. The gate oxide thickness was 4.5 nm. The gate stack was dual doped polysilicon patterned by e-beam lithography to obtain channel lengths below $0.1 \mu\text{m}$. Ultrashallow source-drain extensions/halo were obtained with preamorphization by indium and a low-energy As implant for nMOS [7], and Sb preamorphization and a BF_2 implant for pMOS devices [5], [6] as shown in SIMS in Fig. 1(b) and (c). Counter-doping with the preamorphizing species results in more abrupt junction, lower source-drain resistance, and improved SCE. The nFET extension is about 50 nm deep and the pFET extension is

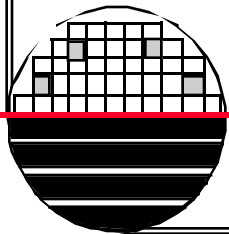
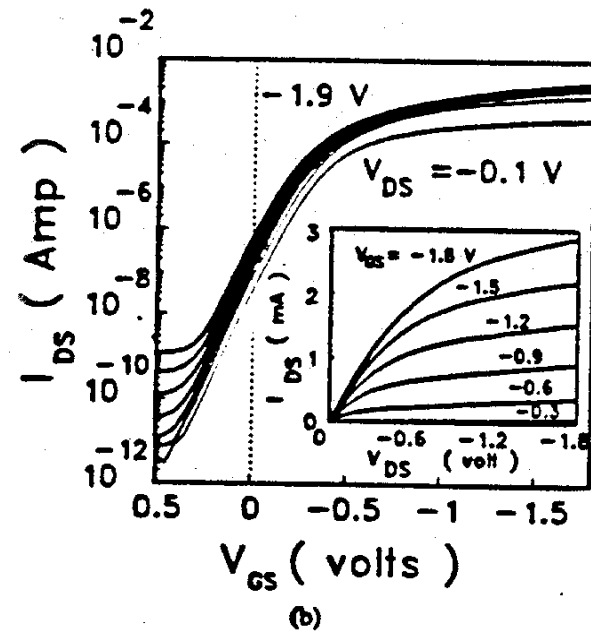
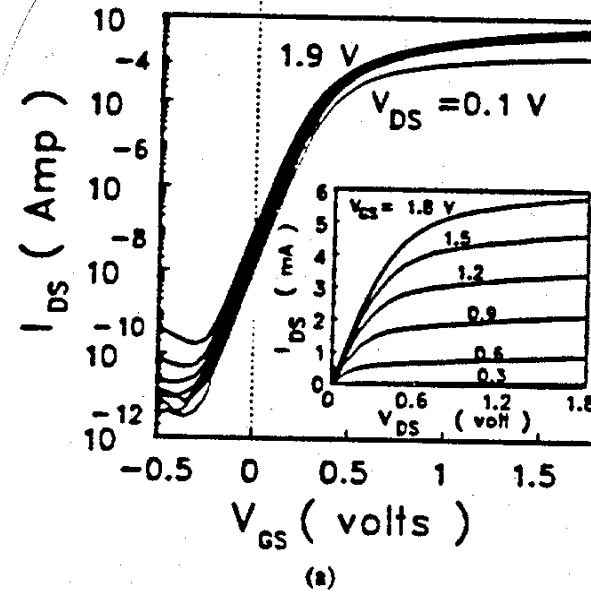
60 nm deep. Devices were also built using Ge preamorphization, and it was found that the V_T rolloff was shifted by about $0.07 \mu\text{m}$ to longer channel lengths for these devices. A thick spacer was formed in order to place the deep part of the source-drain junction far from the channel. The deep junctions are used to provide robust contact process. These deep source-drain junctions were designed to overwhelm the highly doped surface region of the well, intersecting the well dopant profile at close to the background level in order to minimize the junction capacitance. The heat cycle was minimized to avoid boron penetration through the gate oxide [6]. A Ti salicide process was employed to minimize the gate and the source and drain sheet resistance.



III. ELECTRICAL RESULTS

Fig. 2 shows the characteristics of 0.1- μm L_{EFF} nMOS and pMOS devices (ΔL is about 0.06 μm). The sub-threshold slope is about 85 mV/decade for the nMOS and 90 mV/decade for the pMOS. Fig. 3 shows the threshold rolloff for these CMOS devices at high V_{DS} (V_{GS} at which $(I_{\text{DS}}L)/W = 50 \mu\text{A}$ at $V_{\text{DS}} = 1.8 \text{ V}$). Devices with small SCE are demonstrated down to below 0.1- μm channel length. Fig. 4 shows a TEM cross section of a 0.06- μm L_{EFF} nMOS device (0.12- μm L_{DRAWN}) and its electrical characteristics (t_{OX} of this device is 4 nm). No punchthrough is observed. The drain-induced barrier lowering is 150 mV. The maximum V_{T} rolloff (from long-channel V_{T} at low V_{DS} to high V_{DS} threshold of this device) is 250 mV. Saturated transconductances of the 0.1- μm nMOS and pMOS were, respectively, 450 and 225 mS/mm at $|V_{\text{DS}}| = |V_{\text{GS}}| = 1.8 \text{ V}$. Device lifetime was measured as a function of peak substrate current. For a

Fig. 2. 0.1- μm nMOS (a) and pMOS (b) device characteristics. Device width is 10 μm , gate oxide is 4.5 nm, and device contact size is 10 \times 10 μm^2 . NFET and pFET I_{off} at $|V_{\text{DS}}| = 1.8 \text{ V}$ are 90 nA and 0.65 μA , respectively, and their output conductances at $|V_{\text{DS}}| = |V_{\text{GS}}| = 1.8 \text{ V}$ are 0.04 and 0.06 mho/mm, respectively.



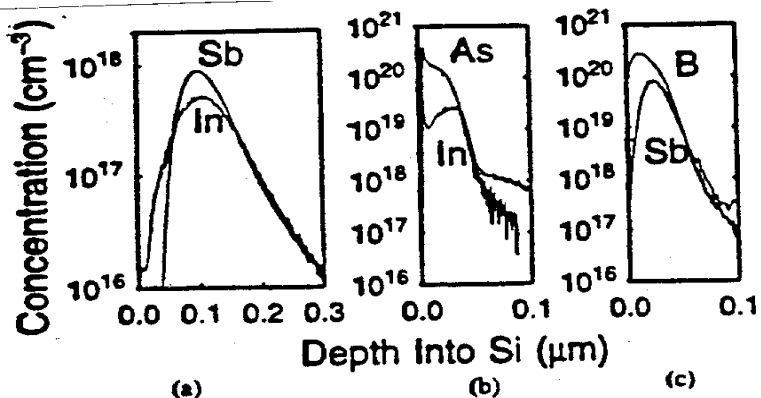


Fig. 1. SIMS measurement of the channel implant for nMOS and pMOS (a), and the source-drain extension/halo profiles for nMOS (b) and pMOS (c).

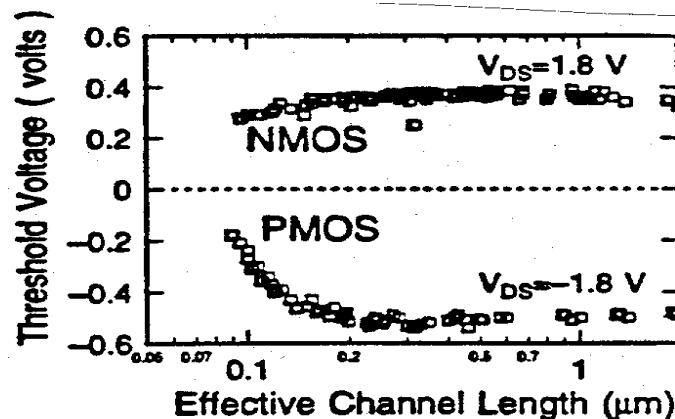
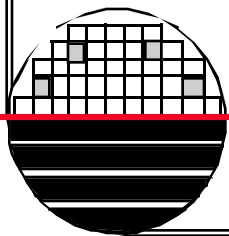
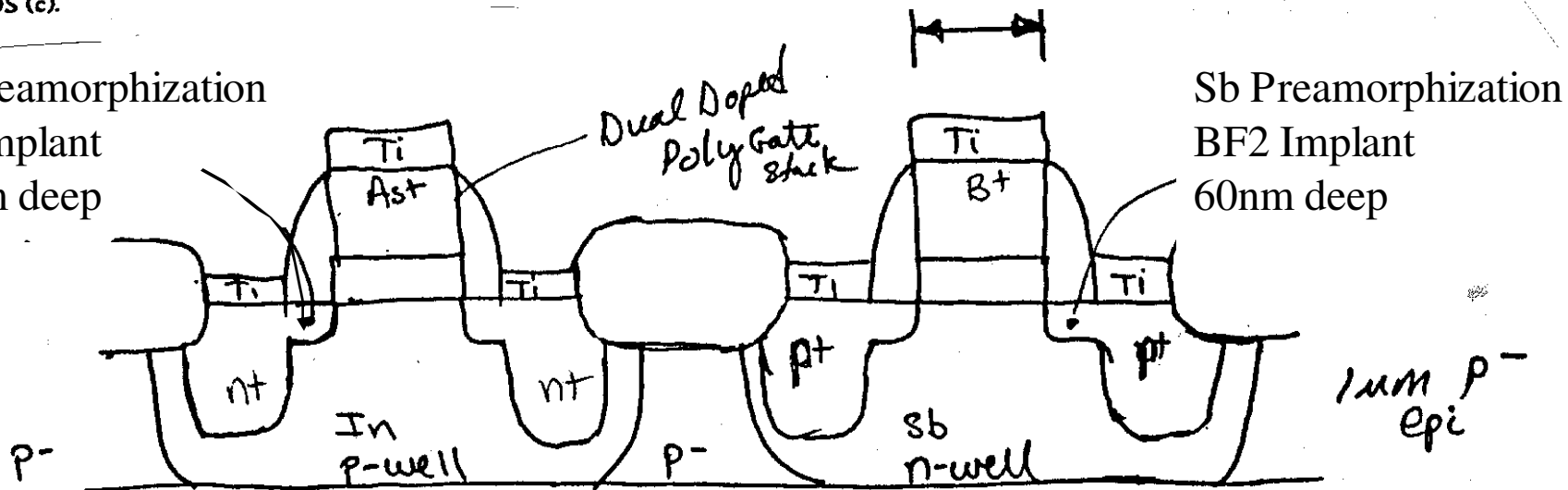


Fig. 3. Threshold rolloff for 0.15-μm CMOS at V_{DS} = 1.8 V

In Preamorphization
As Implant
50nm deep



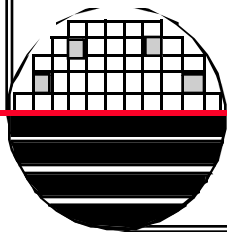
Experimental High Performance Sub- $0.1\mu\text{m}$ Channel nMOSFET's

Y. Mii, S. Rishton, Y. Taur, D. Kern, T. Lii, K. Lee, K. A. Jenkins,
D. Quinlan, T. Brown Jr., D. Danner, F. Sewell, and M. Polcari

Abstract— Very high performance sub- $0.1\mu\text{m}$ channel nMOSFET's are fabricated with 35 \AA gate oxide and shallow source-drain extensions. An 8.8-ps/stage delay at $V_{dd} = 1.5\text{ V}$ is recorded from a $0.08\mu\text{m}$ channel nMOS ring oscillator at 85 K . The room temperature delay is 11.3 ps/stage . These are the fastest switching speeds reported to date for any silicon devices at these temperatures. Cutoff frequencies (f_T) of a $0.08\text{-}\mu\text{m}$ channel device are 93 GHz at 300 K , and 119 GHz at 85 K , respectively. Record saturation transconductances, 740 mS/mm at 300 K and 1040 mS/mm at 85 K , are obtained from a $0.05\text{-}\mu\text{m}$ channel device. Good subthreshold characteristics are achieved for $0.09\text{ }\mu\text{m}$ channel devices with a source-drain halo process.

I. INTRODUCTION

ONE of the key questions concerning future ULSI technology is whether MOSFET devices can be scaled down to $0.1\text{ }\mu\text{m}$ and beyond for continuing performance and density improvement. To provide both high performance and good short-channel behavior in this region, MOSFET's need to be implemented with ultrathin gate oxides, shallow source-drain junctions, and low series resistances. The fabrication of very high performance sub- $0.1\mu\text{m}$ channel nMOSFET's with 35 \AA -thick gate oxide, retrograde channel doping profile [1], [2], and shallow source-drain (halo) [3] extension is presented. DC characteristics, cutoff frequency, and ring oscillator speed at both 300 and 85 K are described.



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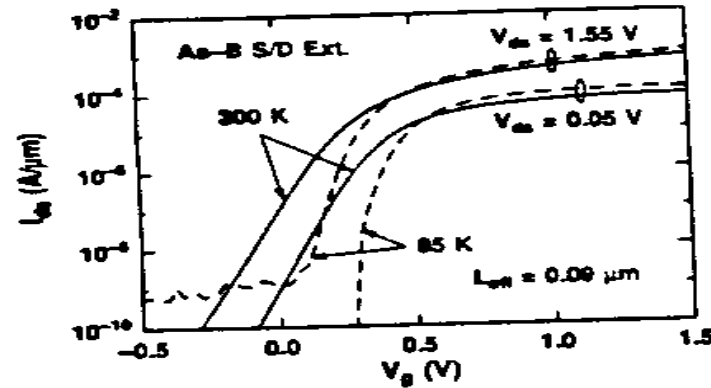


Fig. 3. Subthreshold turn-off characteristics of 0.09- μm channel device at 300 K and 85 K.

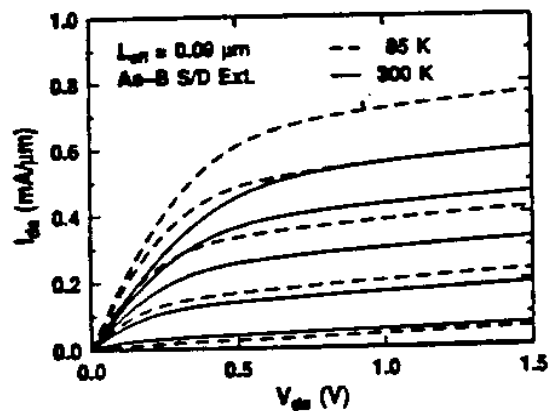


Fig. 1. I - V characteristics of 0.09 μm channel device at 300 and 85 K. Applied gate voltage is from -0.5 V to $+1.5$ V in 0.25-V steps.

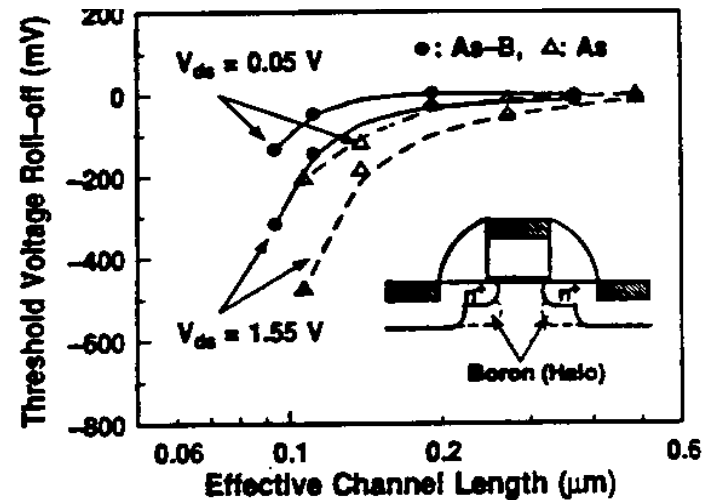
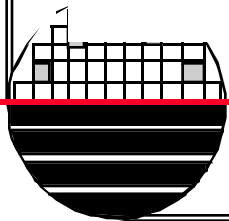


Fig. 4. Threshold voltage roll-off versus channel length for devices with arsenic and with arsenic/boron (halo) source-drain extensions. Inset shows schematic diagram of source-drain extension and halo.

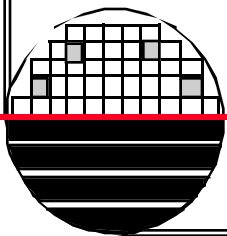


Sub-1/4- μm Dual-Gate CMOS Technology Using *In-Situ* Doped Polysilicon for nMOS and pMOS Gates

Yukio Okazaki, Toshio Kobayashi, *Member, IEEE*, Hiroshi Inokawa, *Member, IEEE*,
Satoshi Nakayama, Masayasu Miyake, Takashi Morimoto,
and Yousuke Yamamoto, *Member, IEEE*

Abstract—A new dual poly-Si gate CMOS fabrication process is proposed. The incorporated technology features a boron-penetration-resistant MBN gate structure for pMOSFET's, and a dual poly-Si gate CMOS process involving separate depositions of *in-situ* doped n^+ and p^- poly-Si for the nMOS and pMOS gates. 0.2- μm CMOS devices with 3.5-nm gate oxide have been successfully fabricated. The advantages of the new process are demonstrated on these test devices. A CMOS 1/16 dynamic frequency divider fabricated by the new process functions properly up to 5.78 GHz at a 2-V supply voltage.

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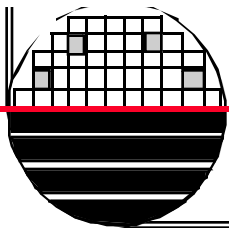
I. INTRODUCTION

A DUAL poly-Si gate structure is required for sub-1/4- μm CMOS in order to adopt surface-channel operation for both nMOS and pMOS. This is because surface-channel operation offers better short-channel and subthreshold I-V characteristics, and better threshold-voltage controllability than buried-channel operation does [1], [2]. The main issues related to the dual poly-Si gate process are the suppression of boron penetration from the p⁺ poly-Si gate through the thin gate oxide, and the doping process for the poly-Si gates. Boron penetration makes it difficult to control the threshold voltage and degrades gate-oxide reliability [3]–[5]. Thus, if the thickness of the gate oxide is reduced, it becomes difficult to use low-energy ion implantation and subsequent high-temperature diffusion to dope the gate poly-Si close to the gate/oxide interface. If the concentration of dopants in the vicinity of the interface is insufficient for degeneracy, a thick depletion layer forms in the gate poly-Si and reduces the device's current drivability [6]. Reduction of the gate resistance is also a key issue in the conventional dual-gate process.

In this work, we devised a new dual-gate CMOS fabrication process featuring two new technologies. The first is a multilayer p⁺-gate structure of boron-doped poly-Si on thin nitrogen-doped poly-Si (MBN-gate structure) for pMOS.

This is done by LPCVD. The MBN gate effectively suppresses boron penetration [7], [8]. The second is a dual-gate CMOS process in which *in-situ* doped n⁺ and p⁺ poly-Si are deposited separately for the nMOS and pMOS gates. This allows for uniform doping at a high concentration close to the gate/oxide interface without high-temperature diffusion [9]. The poly-Si sheet resistance is reduced by depositing as amorphous silicon with a high concentration of dopants. The combination of these technologies offers low-sheet-resistance dual poly-Si gates without the fear of boron penetration or gate depletion.

A sub-1/4- μm dual-gate CMOS with extremely thin gate oxide was fabricated to verify the advantages of the new process. First, the new dual-gate fabrication process and its key technologies are described. Then, the characteristics of the *in-situ* doped poly-Si gates and the results of transistor measurements are discussed. Finally, the high performance of the sub-1/4- μm CMOS fabricated by the new process is demonstrated using frequency divider circuits.



II. FABRICATION PROCESS AND KEY TECHNOLOGIES

A. Process Sequence

A schematic of the processing steps is shown in Fig. 1. In this process, the isolated p -well structure with high latchup immunity was adopted (Fig. 1(a)). This involves thin epitaxy over the n^+ buried layer and deep trench for inter-well isolation [10]. The active regions for each device were delineated by shallow trench isolation [11]. This makes the active-field boundary flat.

Channel implantation of boron and phosphorous is done through temporary oxide for the nMOS and pMOS regions, respectively. After the first gate oxidation at 800°C in dry O_2 , a phosphorous *in-situ* doped amorphous-Si layer is deposited by LPCVD using a $\text{Si}_2\text{H}_6\text{-PH}_3$ gas system at 510°C , to form the n^+ gate for the nMOSFET's (Fig. 1(b)). The phosphorous concentration is $3 \times 10^{20} \text{ cm}^{-3}$, and the film thickness is 380 nm.

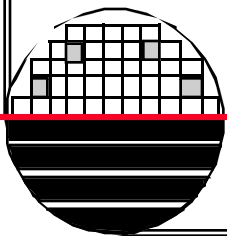
The phosphorous-doped amorphous Si over the pMOS region is selectively eliminated by ECR ion-stream etching, which has a high Si-to- SiO_2 etching-rate ratio. Then, the remaining gate oxide is eliminated by wet etching, followed by second gate oxidation in the pMOS region. The phosphorous-doped amorphous Si is crystallized during second gate oxidation.

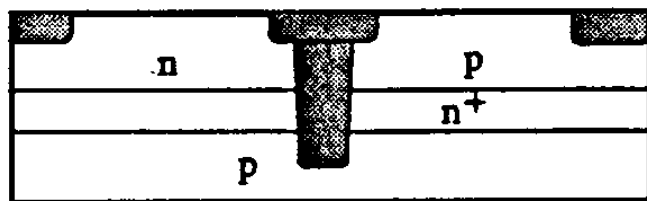
An amorphous-Si layer doped *in-situ* with nitrogen and boron ($\text{Si}_2\text{H}_6\text{-NH}_3\text{-B}_2\text{H}_6$), and then one doped with only boron ($\text{Si}_2\text{H}_6\text{-B}_2\text{H}_6$) are deposited in one continuous step by LPCVD at 510°C , to form the p^+ gate for the pMOSFET's (MBN gate) (Fig. 1(c)). The boron and nitrogen concentrations are $2 \times 10^{20} \text{ cm}^{-3}$ and $1.1 \times 10^{21} \text{ cm}^{-3}$, respectively. The total thickness is 380 nm.

To selectively remove the boron-doped amorphous Si covering the n^+ poly-Si and planarize the surface, the resist etchback technique is adopted. First a resist is coated on the poly-Si and etched back until the surface of the boron-doped amorphous Si on the n^+ poly-Si is exposed (Fig. 1(d)). The boron-and-nitrogen-doped amorphous Si on the n^+ poly-Si are eliminated and the remaining resist is removed. Another resist is coated on the poly-Si, then the resist and the projection on poly-Si are etched back simultaneously.

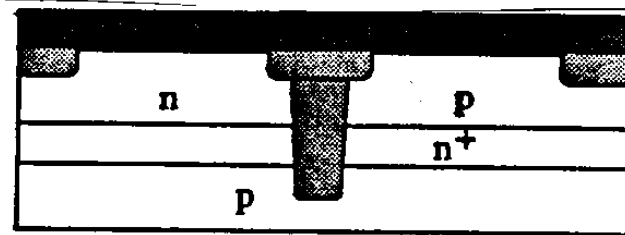
After this, resist patterns for the gate electrode are formed (Fig. 1(e)) and both the phosphorous-doped poly-Si over the nMOS region and the boron/nitrogen-doped amorphous Si over the pMOS region are patterned simultaneously by ECR etching.

The sidewalls of the poly-Si gates are oxidized in steam ambient at 750°C for 30 minutes, prior to source/drain implantation. The boron-doped amorphous Si is crystallized during sidewall oxidation. Then, shallow n^+ and p^+ S/D junctions are formed by low-energy BF_2 implantation with Si-preamorphization and low-energy As implantation, followed by rapid thermal annealing at 950°C for 15 s. Both junctions have abrupt profiles and a depth of 80 nm (Fig. 1(f)) [12].

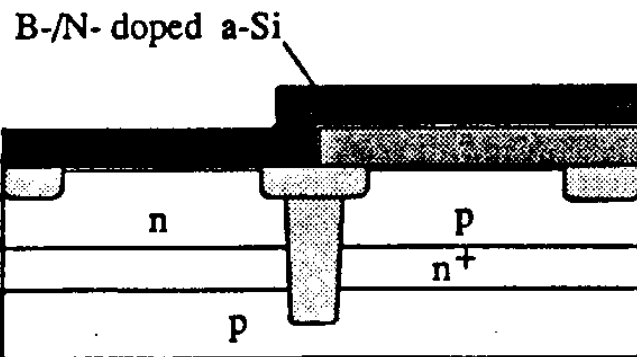




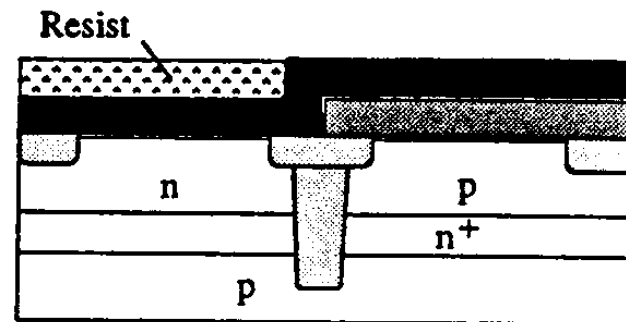
(a)



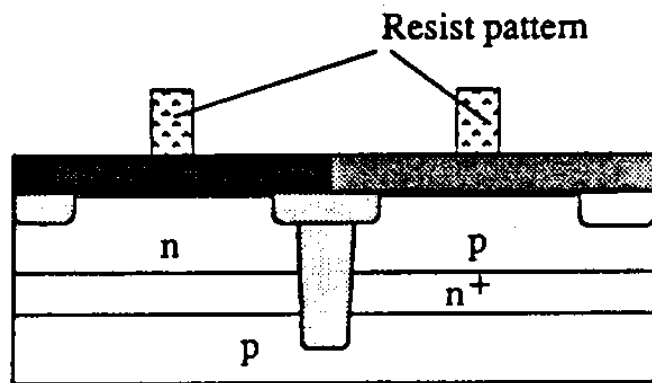
(b)



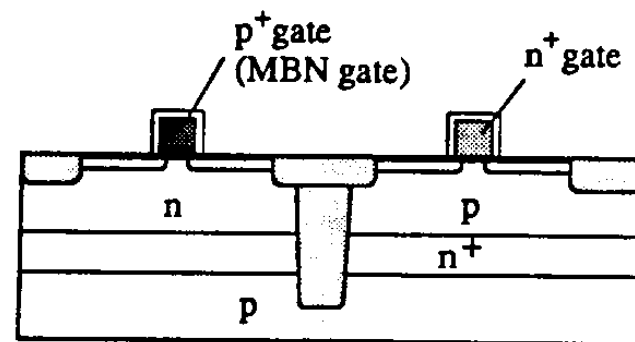
(c)



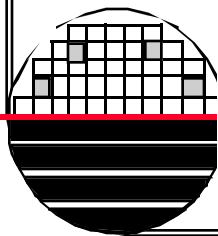
(d)



(e)



(f)



As described above, this process does not require any additional high-temperature diffusion or annealing processes to dope the gate poly-Si, which is advantageous in that it prevents boron penetration and facilitates the formation of a steep channel-impurity profile and an extremely shallow S/D junction.

Fully planarized two-level metalization is employed, featuring tungsten contact plugs formed by blanket CVD, and aluminum via plugs formed by selective CVD [13]. Synchrotron X-ray lithography with a single-layer resist process is used to define the six critical layers [14].

The gate-oxide thickness of the measured devices is 3.5 nm. Only the MOS capacitors used for quasi-static C-V

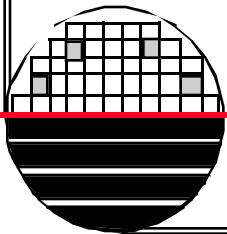
B. MBN Gate Structure

The MBN gate consists of a boron *in-situ* doped and a boron-and-nitrogen *in-situ* doped poly-Si double layer. Both layers are deposited by LPCVD without any break in the processing. The thickness of the boron-and-nitrogen-doped poly-Si is about 5 nm and the nitrogen concentration is $1.1 \times 10^{21} \text{ cm}^{-3}$. This thin layer successfully suppresses boron penetration through the 3.5-nm-thick gate oxide during subsequent thermal treatment [8]. The double-layer poly-Si is continuously etched by ECR ion-stream etching.

C. In-Situ Doped Poly-Si Deposited as Amorphous Si

Annealing the *in-situ* doped amorphous-Si film is useful in forming doped poly-Si with low resistivity, because it is compatible with low-temperature processing [15], [16]. Fig. 2 shows the sheet resistance of Si films *in-situ* doped with phosphorous and boron as a function of annealing temperature for several impurity concentrations. The Si films were deposited by LPCVD using $\text{Si}_2\text{H}_6\text{-PH}_3$ and $\text{Si}_2\text{H}_6\text{-B}_2\text{H}_6$ gas systems at 510°C . The as-deposited Si films are both amorphous, and are crystallized by annealing above 600°C .

The sheet resistance decreases as the impurity concentration increases at the same annealing temperature. The annealing-temperature dependence of the sheet resistance drastically decreases at concentrations above $1 \times 10^{19} \text{ cm}^{-3}$. At a concentration of 1.9×10^{20} for boron-doped Si the resistivity is as small as $2 \times 10^{-3} \Omega\text{cm}$, while at a concentration of 3.4×10^{20} for phosphorous-doped Si it is $7 \times 10^{-4} \Omega\text{cm}$. The generation of nucleation centers in amorphous Si leads to a larger grain size than that of the as-deposited polycrystalline Si [17]. The observed grain size is 1–4 μm .



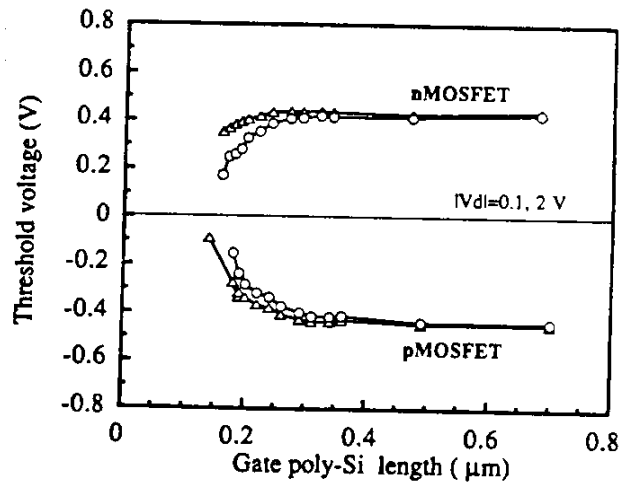


Fig. 9. Threshold-voltage rolloff as a function of gate poly-Si length for drain voltages of 0.1 and 2.0 V.

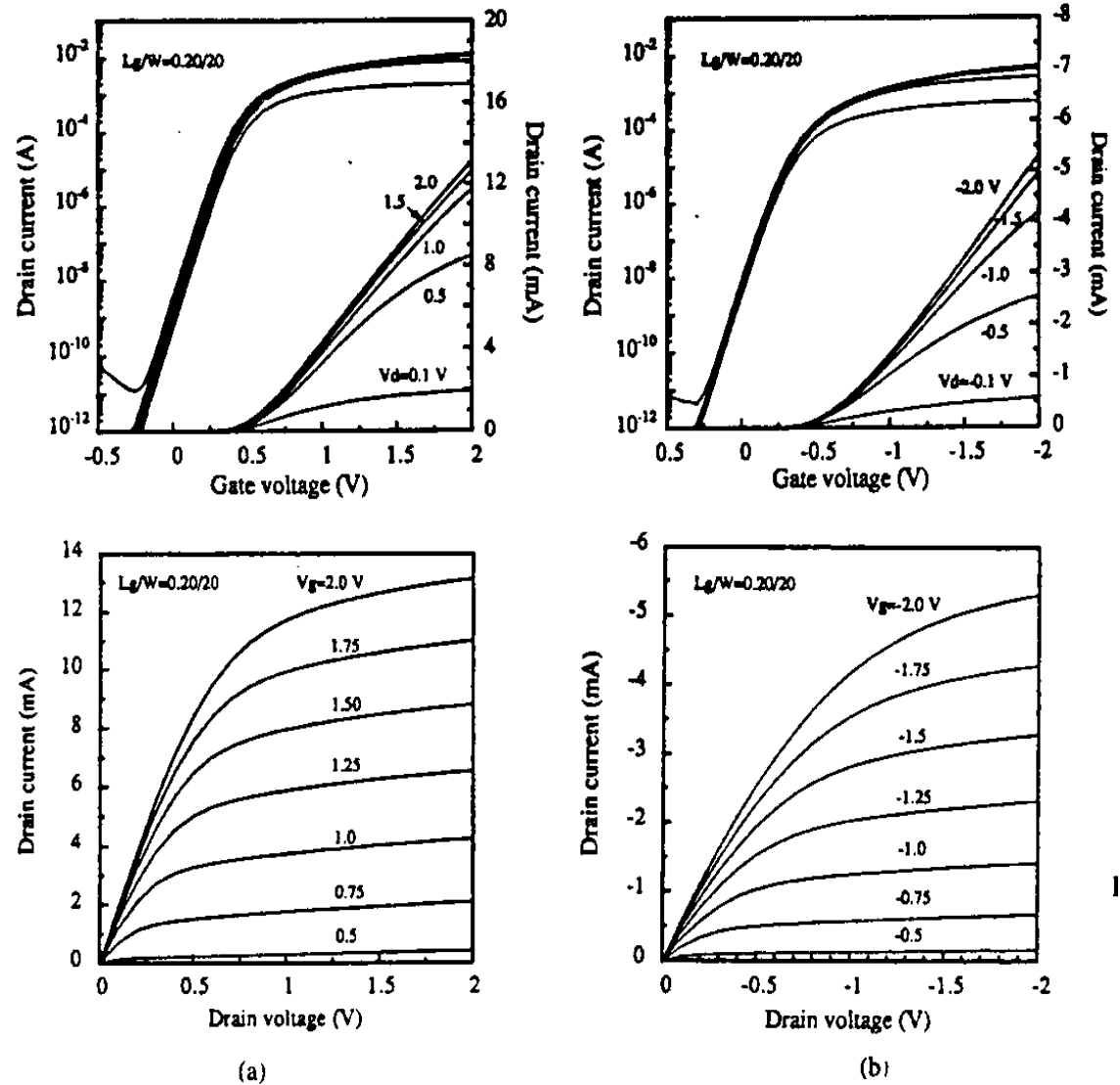
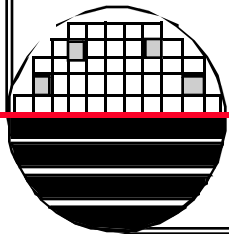


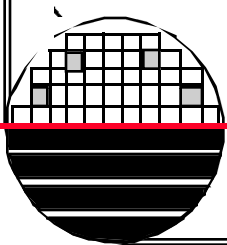
Fig. 8. I-V curves of 0.20- μ m-gate (a) nMOSFET's and (b) pMOSFET's. ($W_{eff} = 20 \mu\text{m}$).



High-Performance 0.07- μm CMOS with 9.5-ps Gate Delay and 150 GHz f_T

Clement Wann, Fariborz Assaderaghi, Leathen Shi, Kevin Chan, Steve Cohen, Harry Hovel, Keith Jenkins, Young Lee, Devendra Sadana, Raman Viswanathan, Shalom Wind, and Yuan Taur

Abstract— We report room-temperature 0.07- μm CMOS inverter delays of 13.6 ps at 1.5 V and 9.5 ps at 2.5 V for SOI substrate; 16 ps at 1.5 V and 12 ps at 2.5 V for bulk substrate. This is the first room-temperature sub-10 ps inverter ring oscillator delay ever reported. PFET with very high drive current and reduction in parasitic resistances and capacitances for both NFET and PFET, realized by careful thermal budget optimization, contribute to the fast device speed. Moreover, the fast inverter delay was achieved without compromising the device short-channel characteristics. At $V_{\text{dd}} = 1.5$ V and $I_{\text{off}} \sim 2.5$ nA/ μm , minimum L_{eff} is about 0.085 μm for NFET and 0.068 μm for PFET. PFET I_{on} is 360 $\mu\text{A}/\mu\text{m}$, which is the highest PFET I_{on} ever reported at comparable V_{dd} and I_{off} . The SOI MOSFET has about one order of magnitude higher I_{off} than bulk MOSFET due to the floating-body effect. At around 0.07 μm L_{eff} , the NFET cut-off frequencies are 150 GHz for SOI and 135 GHz for bulk. These performance figures suggest that sub-tenth-micron CMOS is ready for multi-gigahertz digital circuits, and has a good potential for RF and microwave applications.



I. DEVICE FABRICATION AND PERFORMANCE

SUB-TENTH-MICRON CMOS continues to deliver higher performance and less power consumption at lower V_{dd} . In this work sub-tenth-micron CMOS devices and circuits were fabricated on bulk and SOI substrates. The device fabrication processes were similar to that in [1]. The gate level was patterned using X-ray lithography, enabling high resolution and high throughput. Functional DC-to-DC converters, 10-GHz voltage-controlled oscillators, 5.8-GHz low-noise amplifiers, and 6-GHz frequency dividers were also successfully fabricated. The oxide thickness was 27 Å as measured by an ellipsometer.

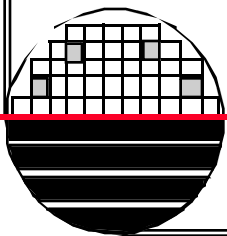
CMOS inverter ring oscillators had delays of 16 ps at 1.5 V, 13.5 ps at 1.8 V, and 12 ps at 2.5 V for bulk substrate; 13.6 ps at 1.5 V, 11 ps at 1.8 V, and 9.5 ps at 2.5 V for SOI substrate, as seen in Fig. 1. This is the first room-temperature sub-10 ps CMOS ring oscillator delay reported. The partially-depleted (PD) SOI CMOS devices (140 nm starting silicon thickness) in general have improved the inverter delay by about 25%, although I_{off} is one order of magnitude higher due to the floating-body effect. This fast ring oscillator speed mainly resulted from the high performance PFET and the reduction of the parasitic resistances and capacitances of the short-channel devices, both were realized by reducing the

thermal budget. Shallow source and drain extensions with abrupt profiles in both the vertical and the lateral directions are the keys to simultaneously reduce overlap capacitances and series resistances of bulk and PDSOI MOSFET's to about $200 \Omega \cdot \mu\text{m}$ for NFET's and about $400 \Omega \cdot \mu\text{m}$ for PFET's (both sides).

Fig. 2(a) and (b) show the characteristics of NFET and PFET devices of the same L_{mask} (0.125 μm) as those in the ring oscillators. For bulk CMOS, I_{off} for 0.085 μm L_{eff} NFET and 0.068 μm L_{eff} PFET (both of L_{mask} 0.125 μm) is 2.5 nA/ μm at 1.5 V. I_{on} of the 0.068 μm PFET is 360 $\mu\text{A}/\mu\text{m}$, which is also the highest ever reported at 1.5 V V_{dd} and comparable I_{off} . V_t roll-off characteristics of bulk CMOS are shown in Fig. 3.

III. CONCLUSION

High speed bulk and SOI CMOS technologies were fabricated. Our SOI CMOS delivers a 9.5-ps inverter ring oscillator delay at 2.5 V under room temperature, the first sub-10 ps room temperature ring oscillator ever reported. At $V_{dd} = 1.5$ V, our bulk CMOS delivers a 16-ps delay at 2.5 nA/ μm I_{off} . I_{on} is 360 $\mu\text{A}/\mu\text{m}$ for the 0.068- μm PFET, even higher than a previously reported 1.8 V technology [7]. By careful reduction of the thermal budget, we were able to realize high-current-drive PFET and low parasitics short-channel NFET and PFET. A scheme to compare τ_d with adjusted V_t is proposed. The f_T of the 0.07 μm L_{eff} NFET is 150 GHz for SOI and 135 GHz for bulk. Sub-tenth-micron CMOS is ready for multi-GHz digital applications and is also a possible candidate in high speed data communications.



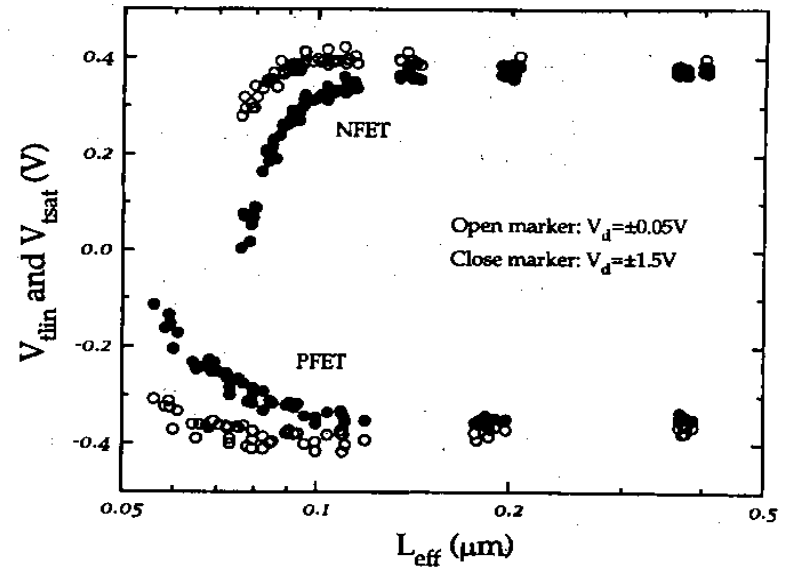
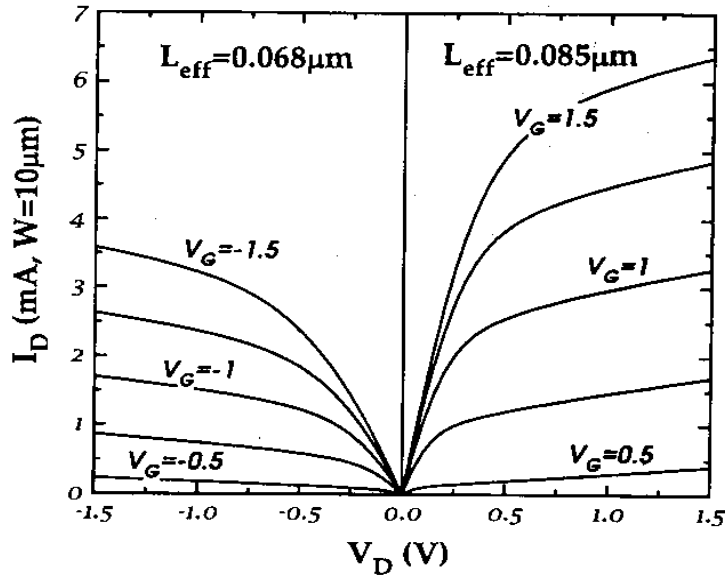
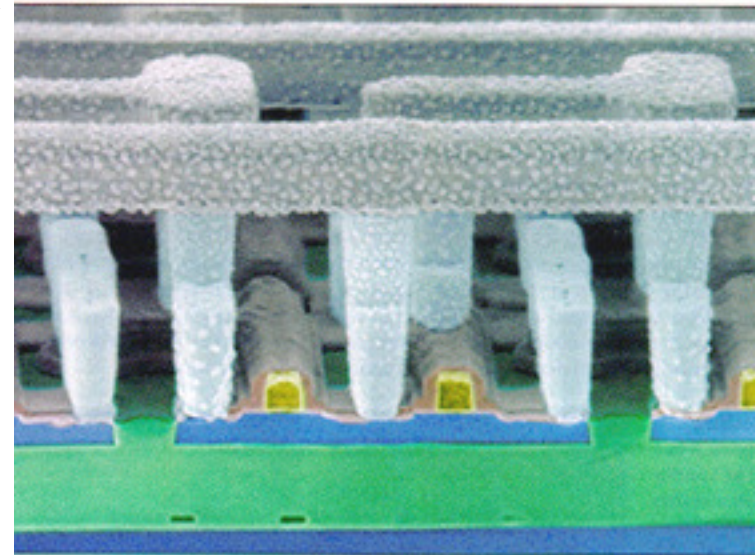
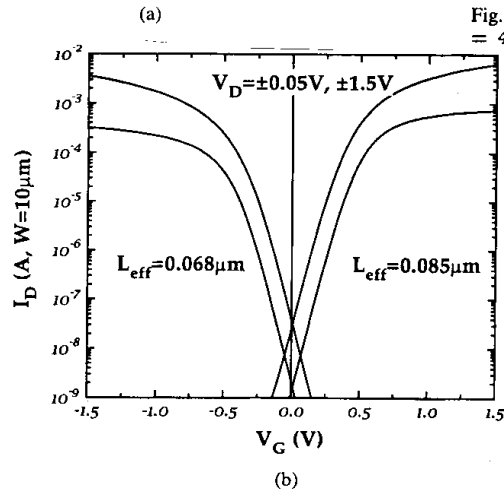


Fig. 3. NFET and PFET short-channel characteristics. V_t is defined at $I_{ds} = 40 \text{ nA}/(W/L_{eff})$.



Silicon on Insulator

An 0.18- μm CMOS for Mixed Digital and Analog Applications with Zero-Volt- V_{th} Epitaxial-Channel MOSFET's

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Abstract—An 0.18- μm CMOS technology with multi- V_{th} 's for mixed high-speed digital and RF-analog applications has been developed. The V_{th} 's of MOSFET's for digital circuits are 0.4 V for NMOS and -0.4 V for PMOS, respectively. In addition, there are n-MOSFET's with zero-volt- V_{th} for RF analog circuits. The zero-volt- V_{th} MOSFET's were made by using undoped epitaxial layer for the channel regions. Though the epitaxial film was grown by reduced pressure chemical vapor deposition (RP-CVD) at 750 °C, the film quality is as good as the bulk silicon because high pre-heating temperature (940 °C for 30 s) is used in H_2 atmosphere before the epitaxial growth. The epitaxial channel MOSFET shows higher peak g_m and f_T values than those of bulk cases. Furthermore, the g_m and f_T values of the epitaxial channel MOSFET show significantly improved performances under the lower supply voltage compared with those of bulk. This is very important for RF analog application for low supply voltage. The undoped-epitaxial-channel MOSFET's with zero- V_{th} will become a key to realize high-performance and low-power CMOS devices for mixed digital and RF-analog applications.

I. INTRODUCTION

LOW power consumption has been one of the biggest issues for developing next-generation high-performance CMOS. The most effective way of reducing power consumption is to lower the supply voltage. At the same time, gate oxide thickness should be reduced to maintain the current drive of MOSFET's. Table I shows the general trend of CMOS parameters for 0.25-, 0.18-, and 0.13- μm generations [1]. For the 0.18- μm generation, t_{ox} of 4.5 nm and V_d of 1.8 V are assumed. In the low-voltage/low-power design of 0.18- μm CMOS, we chose in advance the values of t_{ox} and V_d assumed for 0.13- μm generation—3.5 nm and 1.5 V, respectively. In addition, we chose n^+ gate for p-MOSFET's in order to simplify the process, and thus reduce the production cost. By optimizing the channel impurity profiles, the short-channel effects of n^+ gate buried-channel p-MOSFET's was sufficiently suppressed [2]. In the n^+ poly Si gate case, dopant penetration of the gate electrode is not a problem, differing from the p^+ poly gate case. Thus, nitrided oxide gate insulator is not necessary.

For low-voltage RF analog application, high g_m value at low V_g is critically important as shown in Table II. Generally, subthreshold leakage current at $V_g = 0$ V is not a problem in the analog circuits because the leakage current is controlled by current source. On the other hand, in the digital circuits, the leakage current is a serious obstacle for the realization of low power consumption because this current is not controlled. Thus, V_{th} required for analog MOSFET's is different from that for digital MOSFET's. In the design, we made a special analog n-MOS transistors with $V_{th} = 0$ V in addition with conventional digital CMOS transistors with $V_{th} = 0.4$ V for NMOS and -0.4 V for PMOS as shown in Table II. Short-channel effect suppression of zero-volt- V_{th} MOSFET is expected to be not very good when using ion-implantation for channel doping because the channel impurity profile cannot be very steep. This was solved by introducing an undoped-epitaxial-channel technique [3]–[12] with a small cost of processstep increase. In this paper, 0.18- μm CMOS technology with multi- V_{th} 's for mixed high-speed digital and RF-analog applications is reported.

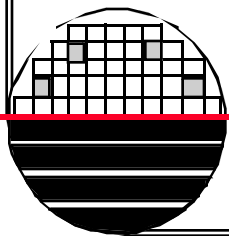
II. SAMPLE FABRICATION

Fig. 1(a) shows the process flow for the 0.18- μm CMOS involving digital n- and p-MOSFET's and analog n-MOSFET's. Key process steps are explained using the cross-sectional views shown in Fig. 1(b). After the formation of the isolation, thin sacrifice oxide was grown on Si substrate. Then, channel doping of n- and p-MOSFET's was carried out ion-implantation [Fig. 1(b)(i)]. The conditions are BF_2 at 30 KeV with dosage of $1 \times 10^{13} \text{ cm}^{-2}$ for digital and analog n-MOSFET's and P^{++} at 120 KeV with $5.0 \times 10^{13} \text{ cm}^{-2}$, As at 70 KeV with $4.0 \times 10^{13} \text{ cm}^{-2}$ and BF_2 at 15 KeV with $5 \times 10^{13} \text{ cm}^{-2}$ for digital p-MOSFET's, respectively.

The sacrifice oxide was removed selectively in the analog n-MOSFET area by using a mask step [Fig. 1(b), (ii)]. Then, undoped epitaxial Si layer of 30 nm was grown selectively on this area by RP-CVD [Fig. 1(b), (iii)]. The process conditions of RP-CVD are listed in Table III. Just prior to the deposition, the native oxide layer was evaporated by using *in situ* high-temperature pre-heating at 940 °C for 30 s in H_2 atmosphere. A 30 nm intrinsic or undoped silicon epitaxial layer was grown at 750 °C by using SiH_2Cl_2 gas. The growth rate is 2 nm/min.

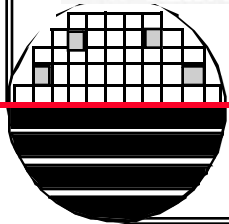
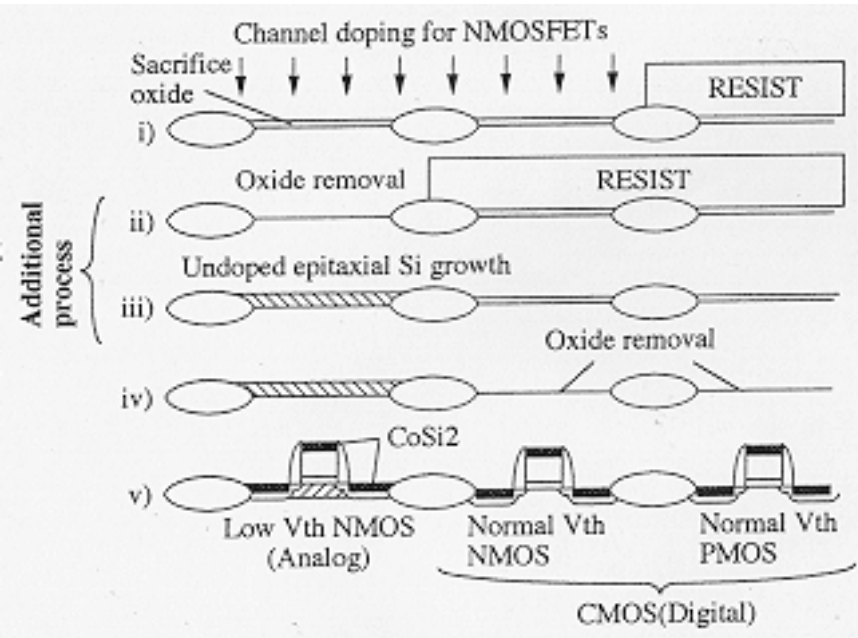
After growing the selective epitaxial layers, the sacrifice oxide on the digital n- and p-MOSFET areas was removed by the etching of the entire region without masking as shown in Fig. 1(b), (iv). Then, the gate oxide is grown [Fig. 1(a)] by dry O_2 oxidation at 800 °C for 30 min. The thickness of gate oxide was 3.5 nm. This is the standard oxide thickness used for 1.5 V supply voltage.

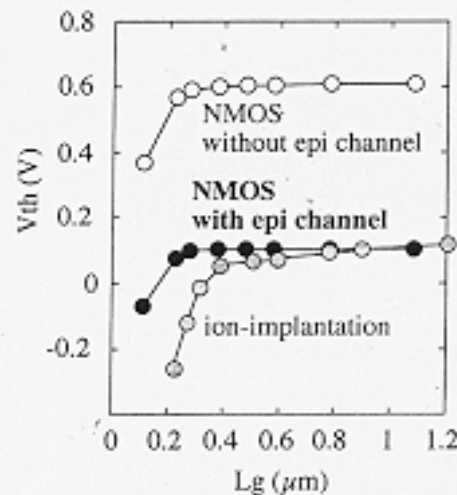
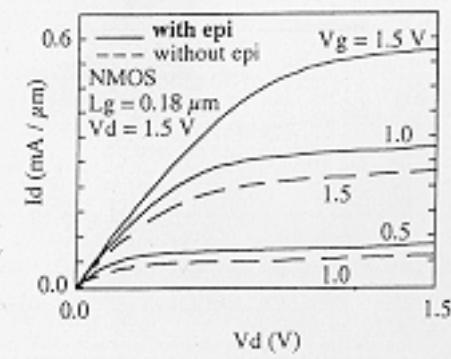
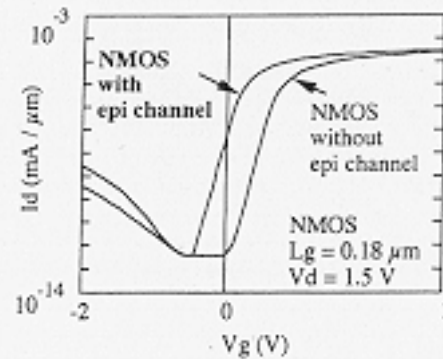
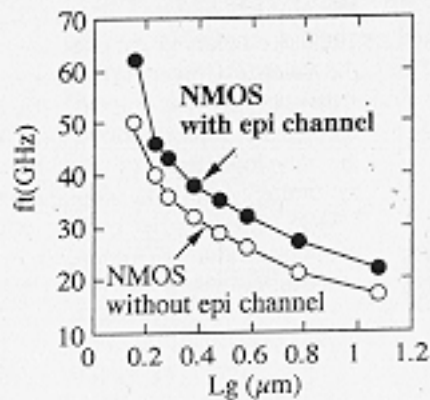
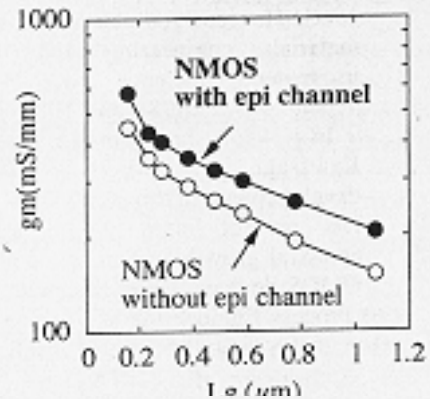
The *in situ* phosphorus doped poly-silicon was deposited



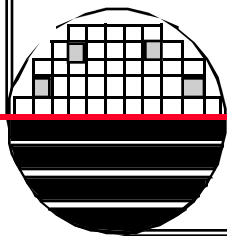
The *in situ* phosphorus doped polysilicon was deposited for the gate electrodes of all the three types of transistors. An $0.3\text{-}\mu\text{m}$ resist pattern for gate electrode was made on the polysilicon film by using excimer stepper. Then, the resist pattern was narrowed to $0.1\ \mu\text{m}$ by using ashing technique [13], [14]. A minimum gate length is $0.1\ \mu\text{m}$ in our experiments. After the formation of the phosphorus polysilicon gate electrode, extension regions of source and drain (As: $15\ \text{keV}\ 2.0 \times 10^{14}\ \text{cm}^{-2}$ for n-MOSFET's and $15\ \text{keV}\ 5.0 \times 10^{13}\ \text{cm}^{-2}$ for p-MOSFET's) were formed by using ion implantation. After the formation of $100\ \text{nm}\ \text{Si}_3\text{N}_4$ sidewall, arsenic ($50\ \text{keV}, 5.0 \times 10^{15}\ \text{cm}^{-2}$) for n-MOSFET's and BF_2 ($30\ \text{keV}, 3.0 \times 10^{15}\ \text{cm}^{-2}$) for p-MOSFET's was carried out with the Si_3N_4 sidewall as a mask to form a deeper source and drain region of CMOS.

Co-salicide technique [2], [15] was used in this process to reduce source, drain and gate resistances significantly as shown in Fig. 1(b), (v). After MOSFET formation, Co and TiN film were deposited by sputter. CoSi films were formed on source, drain and gate electrode selectively by annealing at $500\ ^\circ\text{C}$ for $60\ \text{s}$. After removing nonreactive Co and TiN films, Co silicide was changed from CoSi to CoSi_2 by annealing at $750\ ^\circ\text{C}$ for $30\ \text{s}$ to reduce its resistivity. By using this process, sheet resistance of the gate electrode below $5\ \text{ohm/sq.}$ was realized even at the gate length of $0.1\ \mu\text{m}$. The sheet resistance of the source and drain were also $5\ \text{ohm/sq.}$ Finally, metallization was carried out.





An $0.18\text{-}\mu\text{m}$ CMOS with multi- V_{th} 's for mixed high-speed digital and RF-analog applications has been developed. In the low-voltage/low-power design of $0.18\text{-}\mu\text{m}$ CMOS, we chose the values of t_{ox} and V_d assumed for $0.13\text{-}\mu\text{m}$ generation— 3.5 nm and 1.5 V , respectively. In addition, we chose n^+ gate for p-MOSFET's in order to simplify the process, and thus to reduce the production cost. The V_{th} 's of MOSFET's for digital circuits are 0.4 V for NMOS and -0.4 V for PMOS, respectively. In order to prevent the RF analog n-MOSFET performance degradation due to lower supply voltage of 1.5 V , zero-volt- V_{th} was applied to the analog n-MOSFET. The zero-volt- V_{th} MOSFET's were made by using undoped epitaxial layer for the channel regions. Though the epitaxial film was grown by reduced pressure chemical vapor deposition (RP-CVD) at $750 \text{ }^\circ\text{C}$, the film quality is as good as the bulk silicon because high pre-heating temperature ($940 \text{ }^\circ\text{C}$ for 30 s) is used in H_2 atmosphere before the epitaxial growth. Increase of process cost is small. High-performance under low-voltage in both analog and digital MOSFET's has been demonstrated.



A 130-nm Channel Length Partially Depleted SOI CMOS-Technology

Stephan Pindl, Jörg Berthold, Thomas Huttner, Stefan Reif, Dirk Schumann, and Henning von Philipsborn

Abstract— A partially depleted silicon-on-insulator (PDSOI) CMOS technology employing pocket implantation and a self-aligned titanium silicidation with an effective gate length of $0.13\ \mu\text{m}$ has been developed. An advanced mesa isolation process is used to suppress corner devices. A clear improvement of the device performance due to the novel isolation process is shown. Good transfer characteristics with a steep subthreshold slope and an excellent roll-off of threshold voltage is obtained for both nMOS and pMOS devices down to effective gate lengths of $0.13\ \mu\text{m}$. A 10k transistor circuit which is mostly combinatoric (carry select adder circuit) has been realized and characterized as a performance test circuit with an effective gate length of $0.18\ \mu\text{m}$ and shows high performance and low power consumption compared to an optimized $0.18\ \mu\text{m}$ effective gate length bulk technology with similar processing.

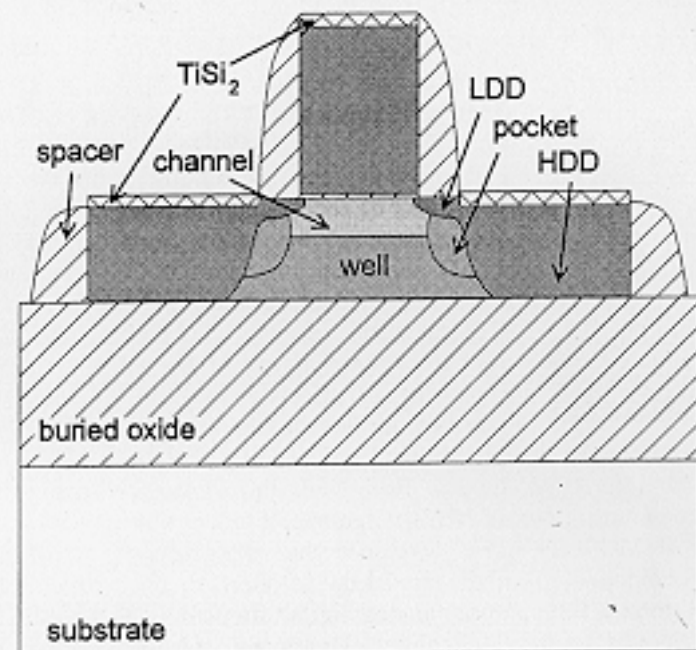
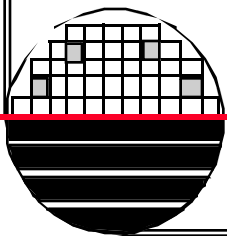


Fig. 1. Schematic cross section of the processed PDSOI devices.



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I. INTRODUCTION

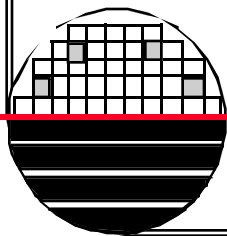
THE CMOS technology on thin-film silicon-on-insulator (SOI) substrates is very promising for low-power and high-performance applications at supply voltages of 1.2 V and below [1], as the parasitic capacitances are significantly reduced by the buried oxide [2], [3]. Other benefits are for example the simple isolation process and the high integration density, as no wells are needed as in bulk technology. Additionally, ultrathin film SOI devices with electrical fully depleted channel (FDSOI) have an excellent subthreshold swing caused by the perfect coupling between gate electrode and channel. However, FDSOI devices show more pronounced short channel effects than SOI devices with a partially depleted channel (PDSOI) in the 0.1- μm regime and beyond caused by top silicon thickness variations [4]. In this work, we present an advanced PDSOI CMOS technology for devices with channel lengths of 0.13 μm . Both device and test circuit characterization have been performed [5].

II. FABRICATION

Starting material for the SOI devices is 150 mm, 8 cm, (100) oriented bonded and etched back SOI (BESOI) wafers (Hughes Danbury, now Ipec Precision). The top silicon and buried oxide layer thickness is 190 and 390 nm, respectively (Fig. 1). First, an advanced mesa isolation process is performed, which is described in more detail in the Section III. After channel and well implantation for threshold adjustment a 4.7-nm thick furnace gate oxide was grown and a 300-nm thick polysilicon was deposited. Next to patterning of the gate with a tetraethylorthosilicate (TEOS) hardmask and performing a rounding oxide to perform a gate's bird's beak, lightly doped drain (LDD) implantations with arsenic for nMOSFET's and

TABLE I
PROCESS AND DEVICE PARAMETERS OF THE PDSOI TECHNOLOGY

process	NMOS	PMOS
material	BESOI ($t_{\text{Si}}=190 \text{ nm}$)	
channel	boron	phosphorus
gate oxide	4.7 nm	
LDD/HDD	arsenic	boron
pocket	boron	phosphorus
RTA anneal	1060°C/10s	1040°C/9s
salicidation	50 nm titanium	
contact hole	tungsten	
L_{eff}	130 nm	
V_{DD}	1.2 V	
V_{T}	310 mV	360 mV



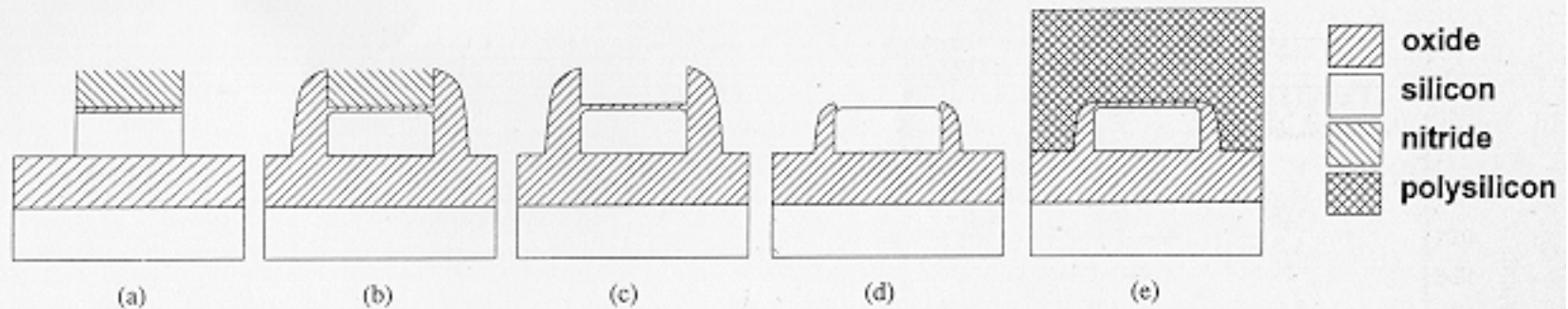


Fig. 2. Schematic process flow of the novel SOI mesa isolation concept with an additional nitride layer.

In this work, a novel concept is proposed to form a spacer higher than the silicon film with minimum additional processing. The investigations on different mesa isolation concepts are performed on SOI wafers with an initial silicon thickness of 45 nm. Both the conventional and the new isolation concept are realized within the same batch. To form the new mesa isolation first a pad oxide (3 nm) is grown. Subsequently, a 50-nm nitride layer is deposited. Then the wafers are patterned by dry etching of nitride and silicon [Fig. 2(a)]. After a corner rounding oxidation, a TEOS layer is deposited and dry etched to form a TEOS spacer [Fig. 2(b)]. Then the nitride layer is wet etched selectively to oxide and silicon [Fig. 2(c)]. After channel and well implantation the pad oxide acting also as screening oxide is removed by a wet etch [Fig. 2(d)] and a 4.7 nm gate oxide is grown followed by a deposition and patterning of the gate polysilicon [Fig. 2(e)].

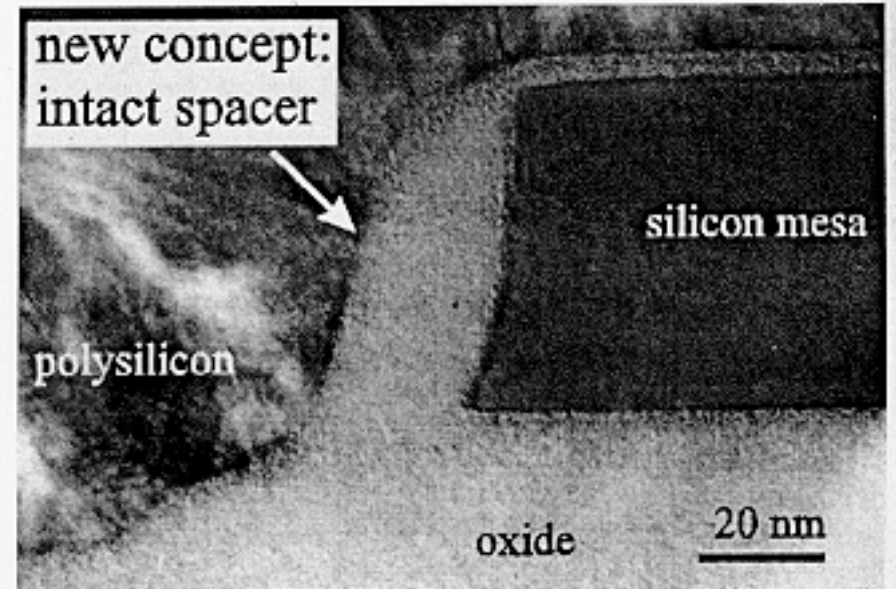
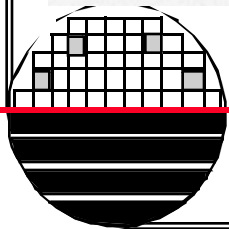


Fig. 4. TEM micrograph of SOI mesa isolation using the novel concept. Compared to the conventional concept there is obviously more spacer left at the mesa corner.



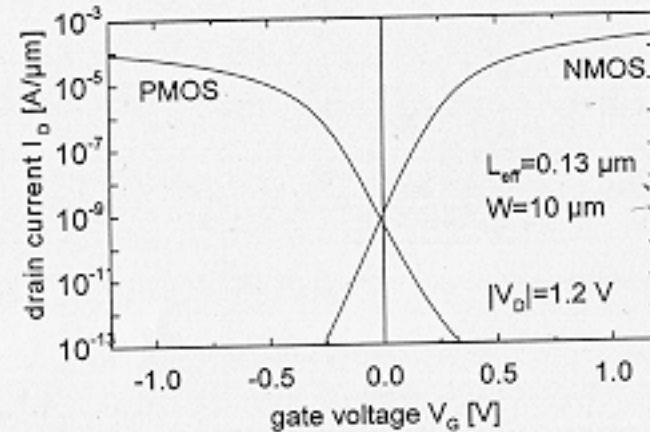
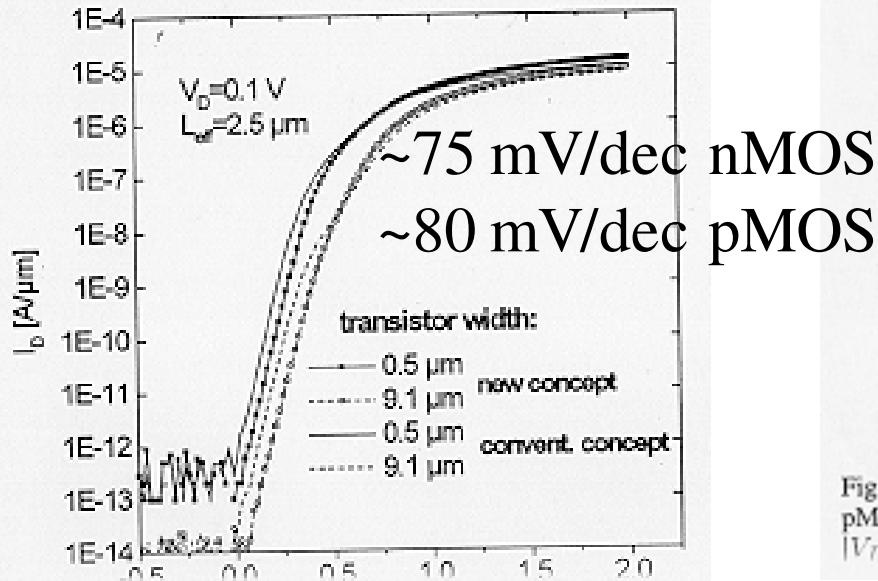


Fig. 8. Subthreshold characteristics of an 0.13- μm channel nMOS and pMOS. The inverse slope is about 75 and 80 mV/dec (nMOS/pMOS) for $|V_D| = 1.2 \text{ V}$ and 80 and 82 mV/dec (nMOS/pMOS) for $|V_D| = 0.1 \text{ V}$.

V. CONCLUSION

A high performance and low power 0.13- μm channel length partially depleted SOI technology has been realized and characterized. By using an optimized pocket implantation the roll-off of threshold voltage is effectively suppressed. Corner devices are omitted using an advanced mesa isolation process with an elevated mesa spacer process. A 10k transistor carry select adder test circuit with a 0.18 μm channel length shows a 45% smaller delay time and a 35% reduced power dissipation compared to a carry select adder processed with a similar bulk silicon technology with the same leakage current.

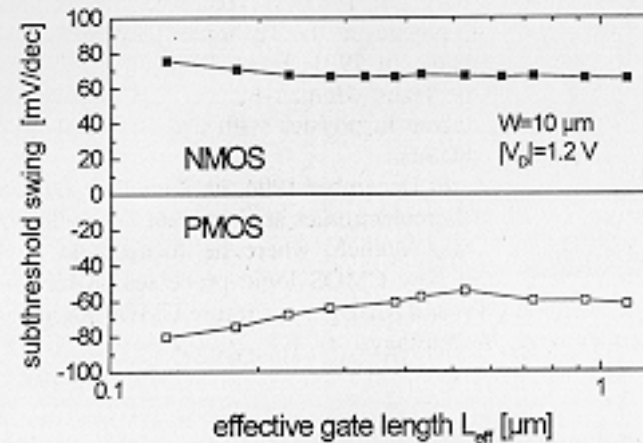
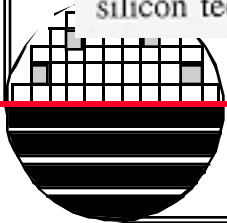


Fig. 11. Subthreshold swing versus effective gate length for nMOS and pMOS.



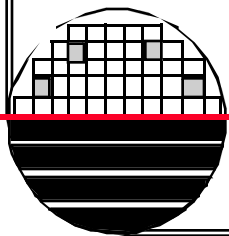
Fabrication and Characterization of Sub-Quarter-Micron MOSFET's with a Copper Gate Electrode

Y. Ma, D. R. Evans, T. Nguyen, Y. Ono, and S. T. Hsu

Abstract—Sub-0.25- μm P and NMOSFET's with a chemical vapor deposited copper gate electrode were fabricated using a novel nitride cast method wherein a silicon nitride gate is used as a stand-in gate which is then replaced by Cu with a PVD TiN barrier metal after source/drain formation. The maximum processing temperature after copper deposition is 400 °C. Excellent device performance was obtained on both P- and N-MOSFET. No signs of copper diffusion were observed after device fabrication and after bias-temperature stress tests at 200 °C.

Index Terms—CVD copper deposition, metal gate, replacement gate process, submicron MOSFET.

There have been a number of reports of MOSFET's fabricated with metals such as TiN, Ta, and W as the gate [2]–[5]. With increasing use of copper in the back end of the line, it is natural then to investigate the feasibility of using copper as the gate electrode as well. In addition to the greatly reduced gate sheet resistance with copper, its implementation may simplify the fabrication process and reduce cost since development effort and production equipment may possibly be shared with copper interconnect technology currently coming into the mainstream. Near term, copper gate electrode devices may be used as a test vehicle to study copper diffusion barriers and the effect of copper diffusion into the device active area. This information is important even if copper is used only in the backend of the process flow. In this letter we report the successful fabrication of copper gate electrode sub-0.25- μm MOSFET's using a replacement or “cast” process, wherein the metal gate is deposited after the S/D formation which is performed with a temporary silicon nitride “microcast”. Using this approach, the maximum temperature after copper deposition is 400 °C, well within the capability of current barrier metal technology.



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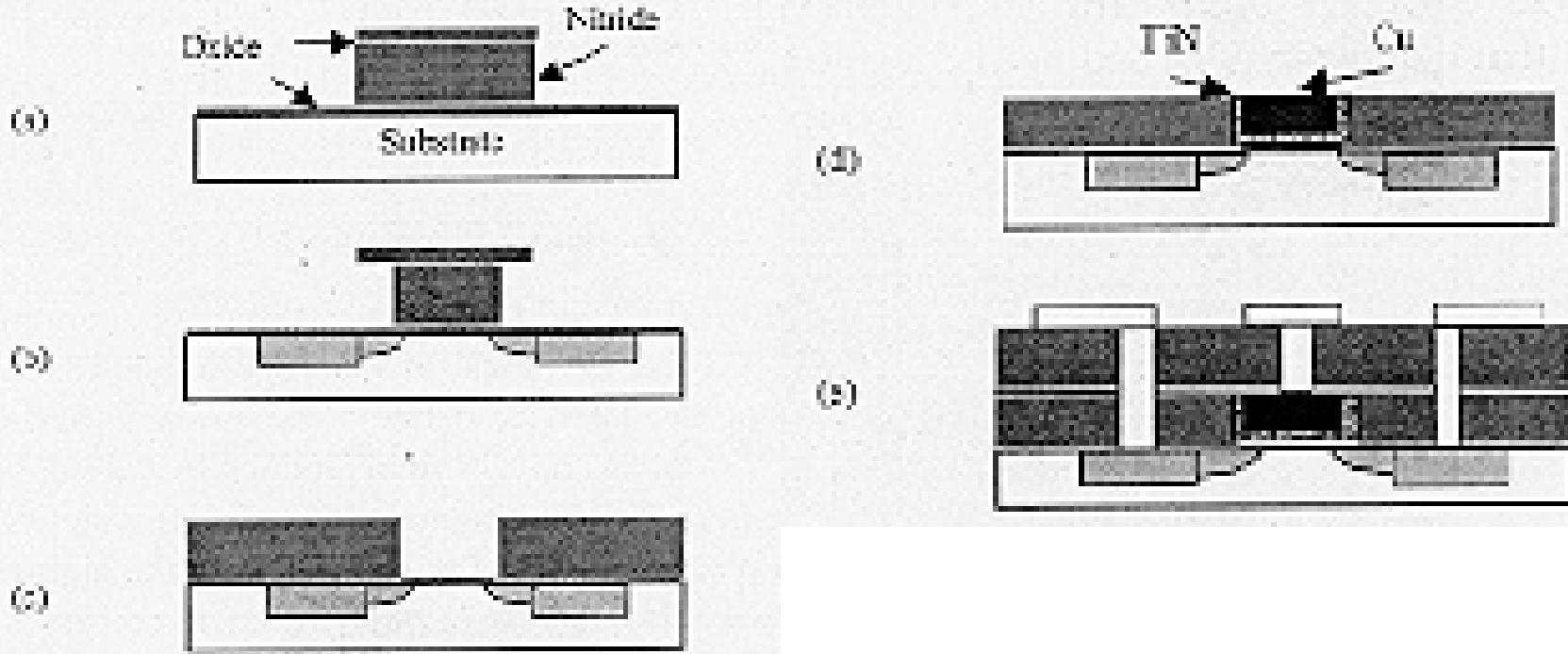
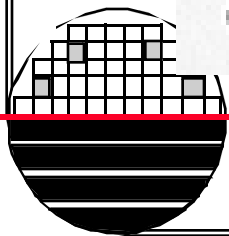
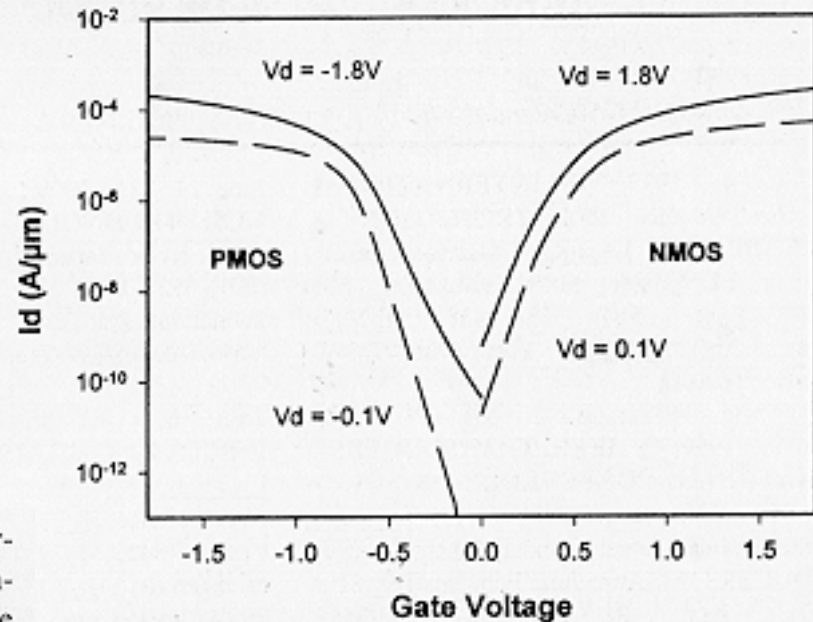
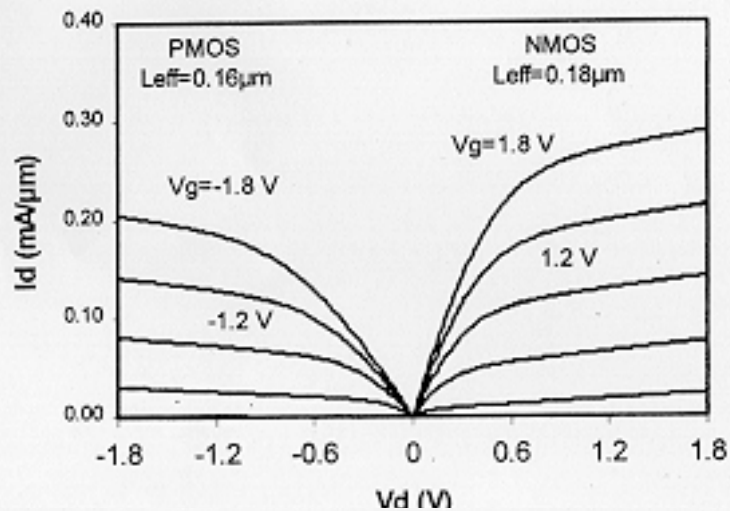
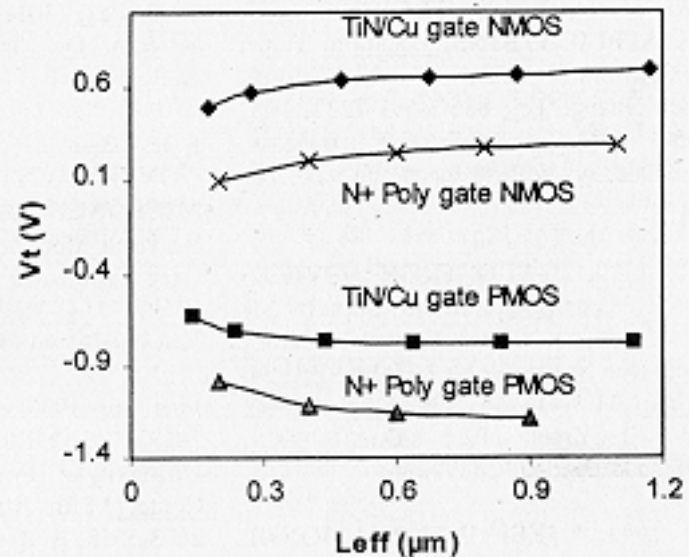


Fig. 1. Processing steps: (a) formation of the nitride cast; (b) after undercut etch using hot phosphoric acid and then a single implantation through the T-structure to form both S/D and the LDD extension regions; (c) after oxide fill and CMP to top of the nitride cast, the nitride is removed selectively using hot phosphoric acid; (d) after PVD TiN and MOCVD copper deposition and CMP to copper; (e) final structure after Al contact formation.





Figs. 2 and 3 show the drain and subthreshold characteristics, respectively, for N- and P-channel MOSFET's. Considering that a 5 nm N₂O gate oxide is used, the drive current is very good, especially for the PMOS devices. The subthreshold leakage is only a few pA/μm, suggesting that no copper contamination is found in the channel region. Fig. 4 shows the threshold voltage of copper gate P⁻ and NMOS transistors as well as N⁺ poly-silicon gate transistors made by the same process. The Fermi level of the TiN/Cu gate is close to the mid-gap [3]. This is confirmed by the VT shift of about 0.45 V between the n⁺ poly gate and the metal gate devices. A similar flatband voltage shift is shown by the high-frequency capacitance (*C-V*) measurements. Capacitance measurements also indicate that the copper gate devices have a $T_{ox} = 4.6$ nm which is smaller, while the poly gate devices have T_{ox} (= 5.1 nm) which is larger, than the as-grown T_{ox} of 4.8 nm



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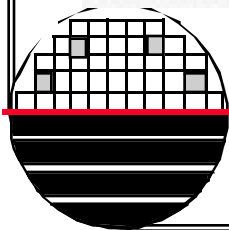
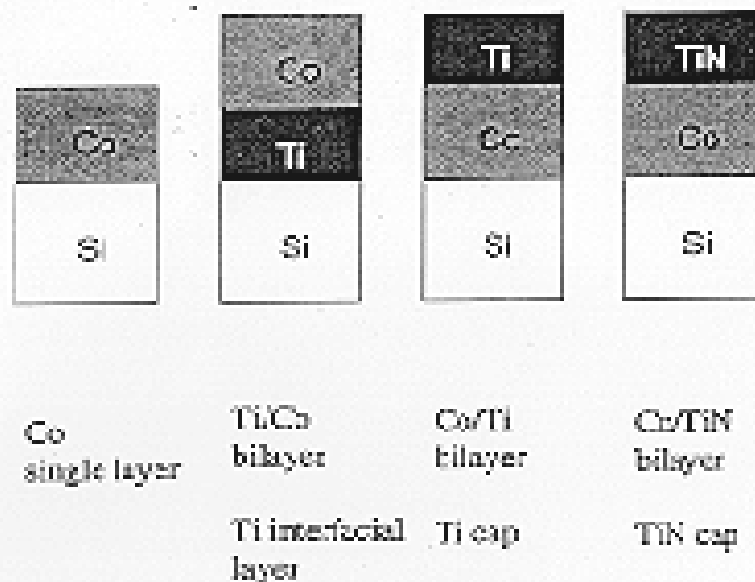
Self-Aligned CoSi_2 for 0.18 μm and Below

Karen Maex, Anne Lauwers, Paul Besser, Eichi Kondoh, Muriel de Potter, and An Steegen

Abstract— CoSi_2 is being used commonly for the advanced IC technologies. There are several process choices to be made for the formation of a high yielding and reproducible silicide. In this paper the various CoSi_2 technologies will be discussed. The scalability of the process of record, the Co/Ti(cap) process will be presented for 0.18 μm and below.

I. INTRODUCTION

RECENTLY, CoSi_2 has been introduced in MOS manufacturing as a replacement of TiSi_2 . Several CoSi_2 formation processes have been proposed. The single layer process using Co on Si has been replaced by others because of its difficult manufacturability [1]. Major problems are its sensitivity to cleaning and its irreproducible yield on narrow lines, partly attributed to a silicide thinning effect at the edges of the silicide lines. The Ti/Co (Ti at interface) has been introduced to alleviate the requirements for cleaning and has been proposed for its epitaxial CoSi_2 growth [2]. The Co/TiN process has been reported to have a large process window with respect to the control of lateral growth [3], [4]. The Co/Ti (Ti cap) process has been shown to be a very promising process and its scalability toward 0.1 μm and below has been demonstrated [5]–[7].



II. CoSi₂ FORMATION PROCESSES

Fig 1 gives a schematic overview of the various CoSi₂ technologies. All four technologies lead to the formation of CoSi₂, which is low resistive and is thermodynamically stable with Si. For all CoSi₂ processes under discussion the process consists of a first RTP (rapid thermal processing) cycle to start the self-aligned reaction, followed by a chemical selective removal of the unreacted metal. After that a second RTP step is performed to improve the resistivity of the final silicide. Its formation is independent of linewidth, i.e. the CoSi₂ formation from CoSi does not yield nucleation problems like TiSi₂ formation does with its cumbersome nucleation of the C54 phase from the previously formed C49 phase [8].

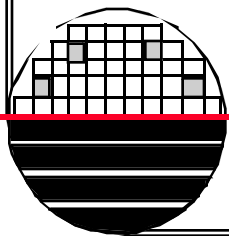
V. CONCLUSIONS

The Co only process suffers from bad reproducibility and is being replaced by other CoSi₂ formation processes. Based on arguments of stress induced in the Si adjacent to the silicide, epitaxially aligned silicides are less attractive than polycrystalline ones. The use of a capping layer during the Co-silicide formation is beneficial

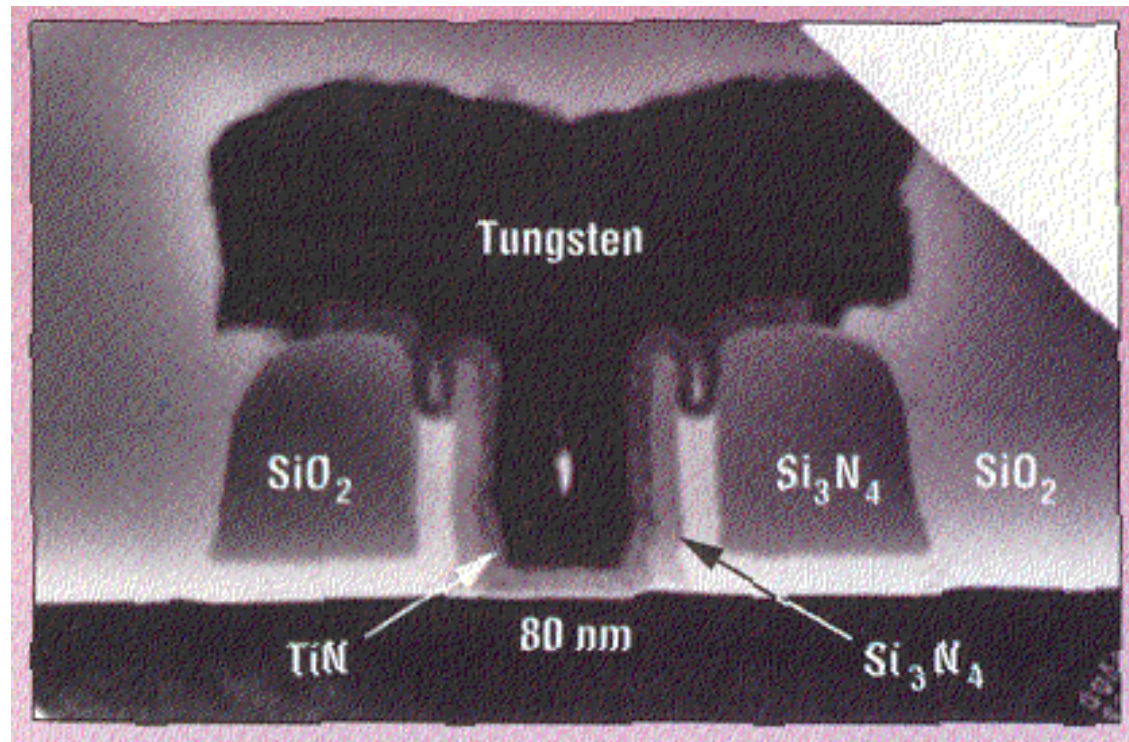
- to reduce the surface diffusion of Si leading to a better process window for self alignment
- to prevent ambient contamination from the RTP tool itself to impact the silicidation process.

The Ti cap outperforms the TiN cap because of its ability

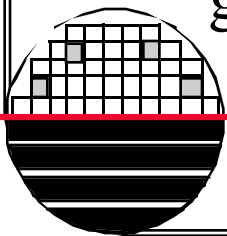
- to reduce an existing interfacial oxide on top of the growing Co₂Si front, thereby indirectly alleviating the requirements for the cleaning process prior to silicidation;
- to capture desorbing elements during the temperature ramp up of the silicidation RTP cycle. The electrical performance of the Co/Ti(cap) process was highlighted for sub 0.18 μm dimensions and the robustness of the process was demonstrated.



0.08 μm MOSFETS



The “T” shaped gate structure helps reduce resistance of the gate connection

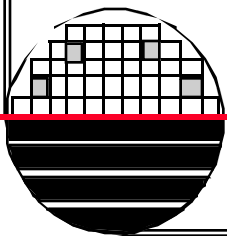


Bell Labs Claims Smallest 'Complete' MOS Transistor

MURRAY HILL, N.J.—Researchers at Bell Laboratories, the research and development arm of Lucent Technologies, have fabricated what the company claims to be the world's smallest "complete" metal oxide semiconductor (MOS) transistors, paving the way for new ICs to pack several billion components on a single silicon chip.

The experimental "nanotransistors" are only 60 nanometers (182 atoms) wide—four times thinner than the smallest transistors in today's IC, it was said. Despite the shrink in size, Bell Labs maintains that these transistors have excelled in speed, power consumption, and other key measures of performance to record levels.

"While Bell Labs and others have built transistors with feature sizes smaller than 100 nanometers before, no one has built a transistor this small with all of the components—source, drain, gate and gate oxide—scaled to deliver the kind of performance needed for a practical device," said Mark Pinto, CTO of Lucent Technologies' Microelectronics Group.



He tied this recent development in with the 50th anniversary of the transistor's invention at Bell Labs, saying the technology has ushered in the age of "nanoelectronics." According to Lucent, the experimental nanotransistor has delivered a current flow of 1.8 milliamps per micron in the "on" state at 1.5 volts—said to be the highest current flow ever reported for a MOS device. It also delivered transconductance—a measure related to the transistor's gain—at 1.12 siemens/mm, according to Bell Labs. It is five times faster and draws 60-160 times less power than today's transistors to perform equivalent operations. Specifically, operating at 1-volt, the device draws 60 times less power than current transistors; operating at 0.6-volt, it draws 160 times less.

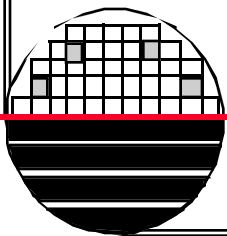
"This new technology could go a long way toward satisfying consumers' demands for longer battery life, less weight and additional capabilities in wireless telephones and portable computers," said Mr. Pinto.

The technology could prove especially attractive in digital signal processors, a class of chips used in cellular phones and other communications devices, something Lucent as a producer of digital signal processors hopes to cash in on.

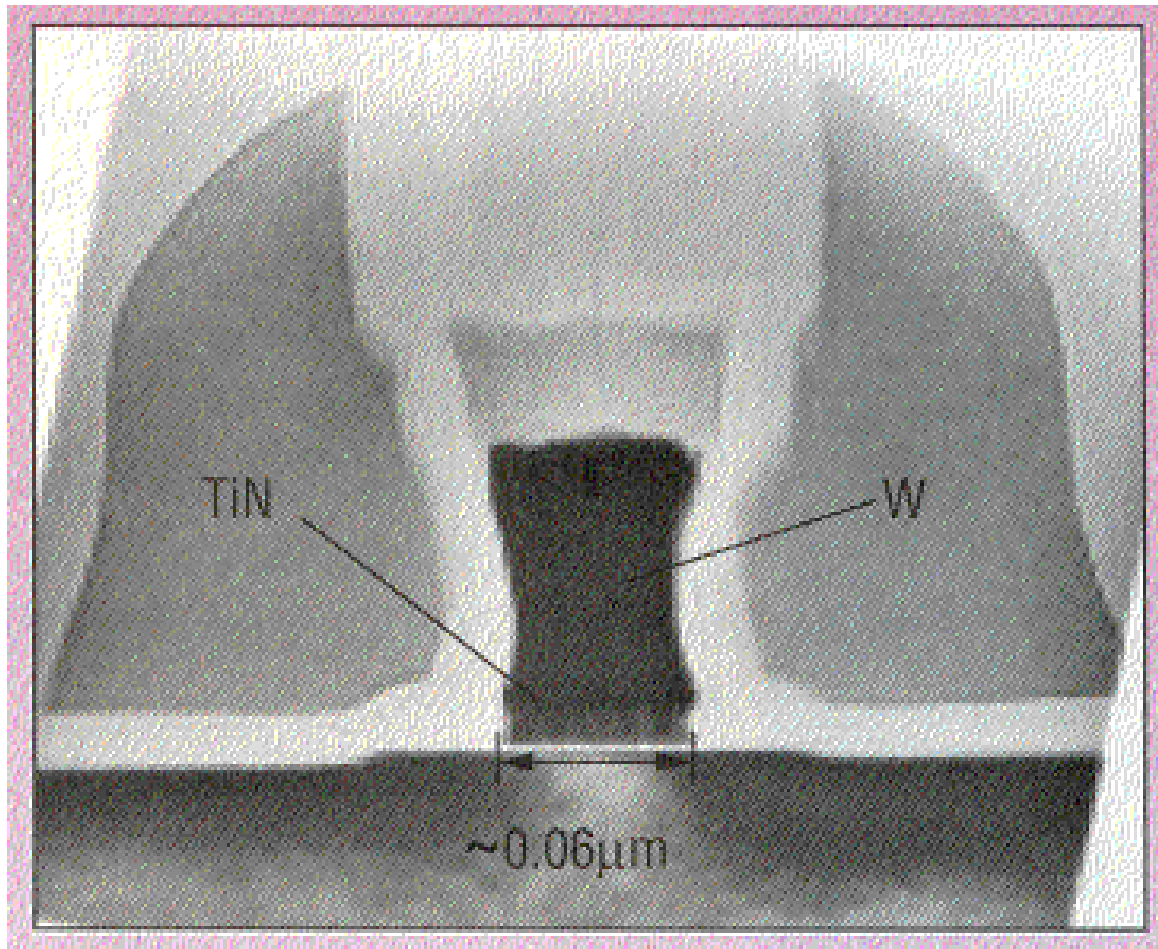
The key advance toward making the experimental transistor possible is said to be an ultra-thin layer of insulation between the gate, the component on which input signals are applied to the transistor, and the source and drain, the components through which the output signals travel. This layer, called the gate oxide, is only 1.2 nanometers, roughly three layers of atoms in thickness. According to Steven Hillenius, head of the Device Research Department in the Bell Labs Silicon Electronics Research laboratory, fabricating a layer this thin required advances in chip fabrication technologies also being pioneered at Bell Labs, including material deposition techniques for growing a three-atom-thick insulating layer of silicon dioxide on the silicon wafer, and an etching technique that eliminates excess material around the transistor gates, but stops short of damaging the delicate insulation layer. Another advance said to be "essential" to fabricating these exceptionally small transistors is the use of electron-beam lithography. Optical lithography processes were said to be "too large to print" the features required by this new transistor.

Bell Labs scientist and project team leader Greg Timp will describe the nanotransistor on Dec. 8 at the International Electron Devices Meeting (IEDM). ♦

(Continued)

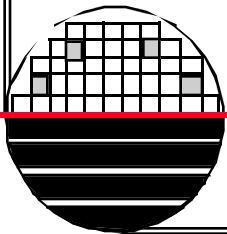


0.06 μm MOSFETS



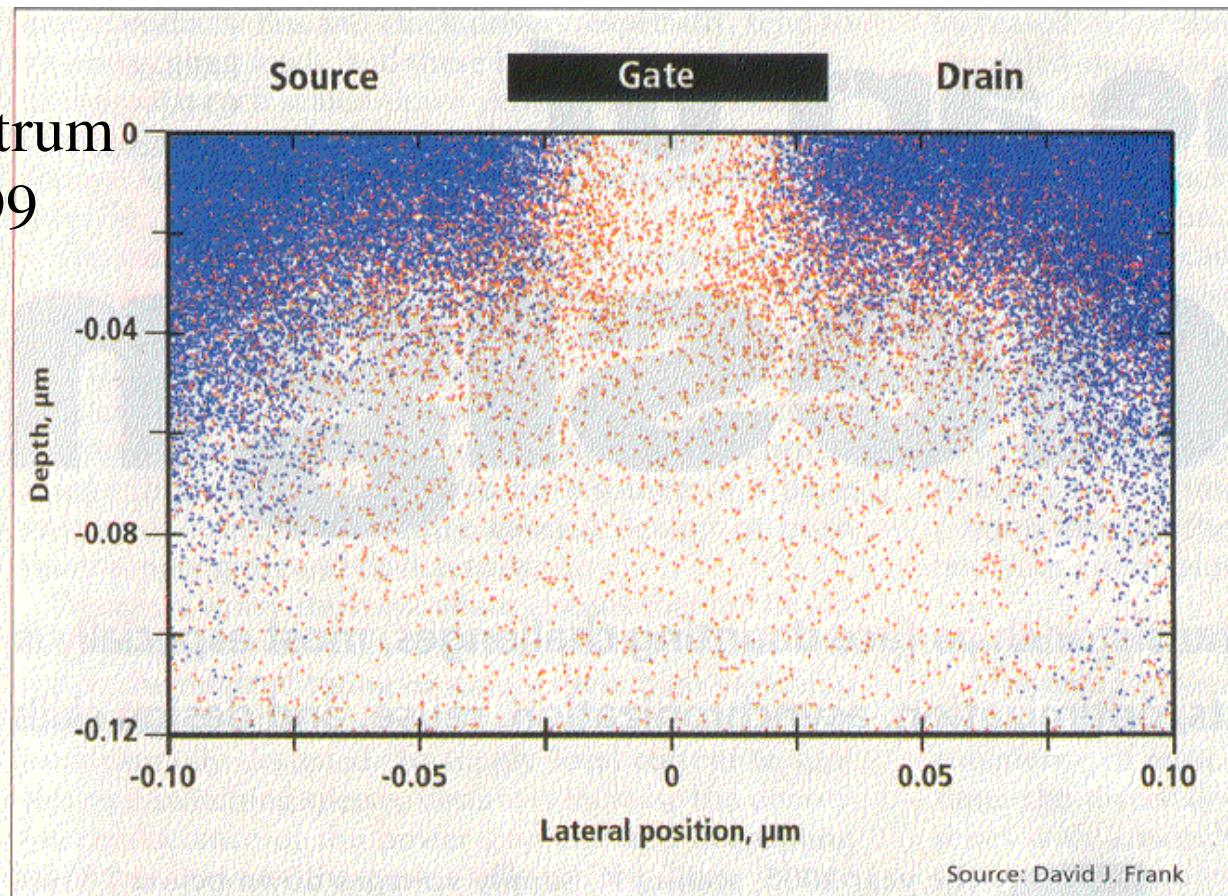
Rochester Institute of Technology
Microelectronic Engineering

IEDM 1999



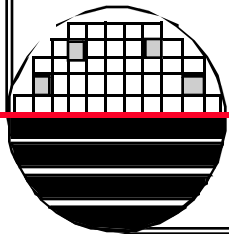
0.05 μm MOSFET Dopant Profile

IEEE Spectrum
July 1999



Source: David J. Frank

[8] A random distribution of discrete dopants in an nMOSFET is simulated above. The device has a channel length of $0.05 \mu\text{m}$ and a channel width of $0.1 \mu\text{m}$. Each red dot represents an acceptor (p-type) dopant atom; each blue dot, a donor (n-type) atom.



ATOMIC SCALE TRANSISTORS

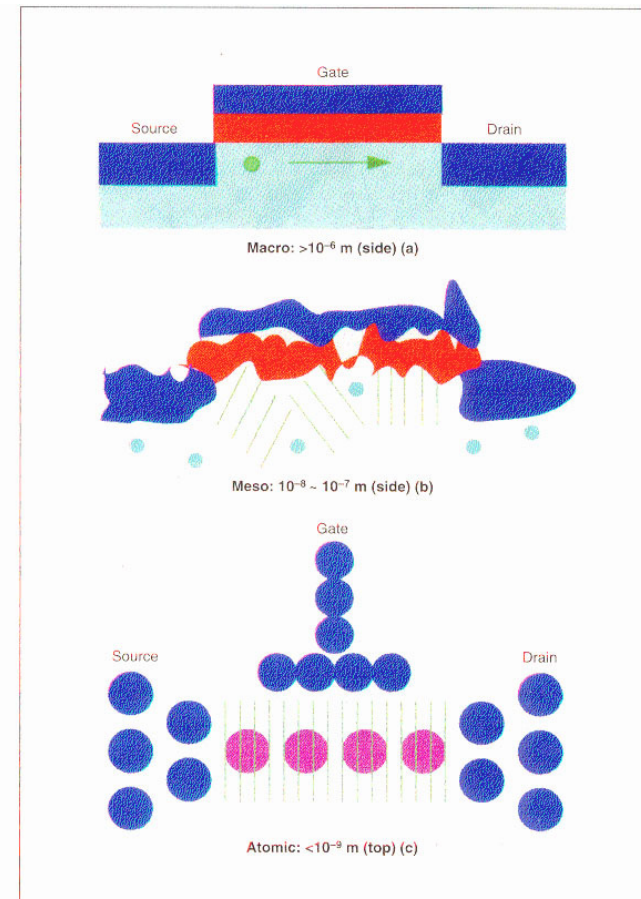
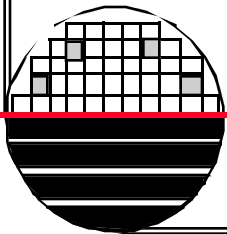
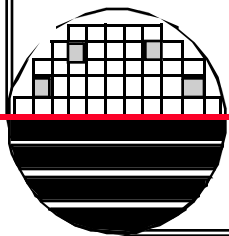
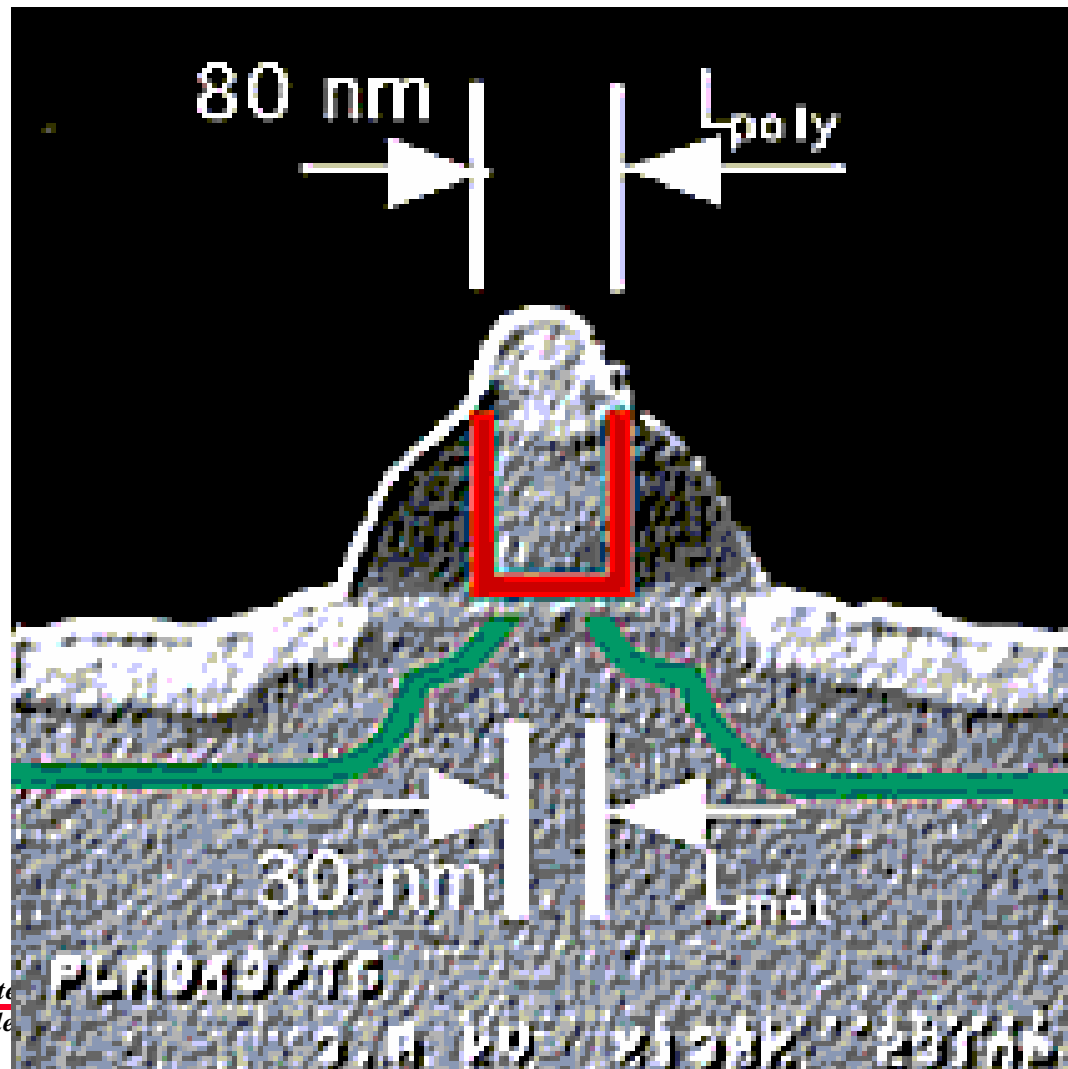


Figure 1. Transistors Have Been Miniaturized, starting from the macroscopic scale, where thousands of dopant atoms can be regarded as being in a smooth distribution that determines the switch-on voltage. At the mesoscopic scale, transistors have different switch-on voltages, depending on precisely where the dopant atoms are located. To prevent such unit-to-unit variations, the next step in miniaturization will not be accomplished by making conventional transistors smaller: instead, transistors with dimensions <1 nm will be made from chains of precisely positioned atoms.



0.03 μm L_{eff} MOSFETS

IMEC Meeting
December 1999



Rochester
Microelectronics

0.03 μm MOSFETS

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 47, NO. 4, APRIL 2000

Gate Length Scalability of n-MOSFET's Down to 30 nm: Comparison Between LDD and Non-LDD Structures

Eiichi Murakami, Member, IEEE, Toshiyuki Yoshimura, Yasushi Goto, and Shin'ichiro Kimura, Member, IEEE

Abstract—Gate length scalability of LDD and non-LDD n-MOSFET's are investigated in terms of resistance to short-channel effects. Extremely small gate electrodes are delineated using electron beam direct writing and highly selective dry-etching techniques. An LDD MOSFET with As-implanted 15-nm-deep junctions shows a superior scalability down to 30 nm. In contrast, in the case of a non-LDD MOSFET having Sb- δ -doped 18-nm-deep junctions, the drain induced barrier lowering (DIBL) mechanism limits the minimum gate length to around 80 nm, at which favorable device operation is achieved. The difference between built-in potential of source/drain junctions (around 0.1 eV) of LDD and non-LDD devices is found to remarkably affect short-channel characteristics in the sub-0.1- μm region.

Index Terms—LDD, MOSFET, short-channel effects, sub-0.1 μm .

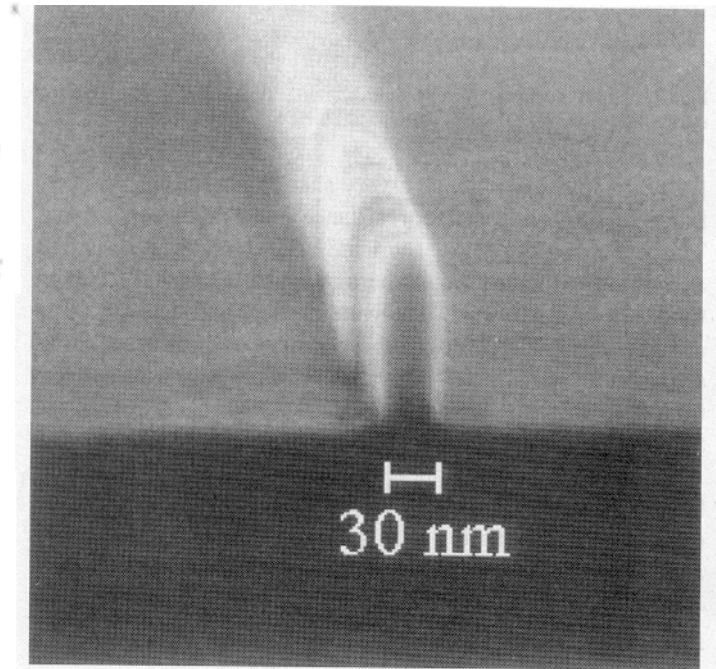
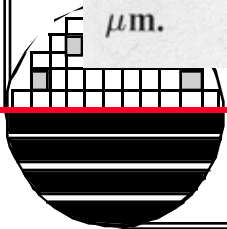
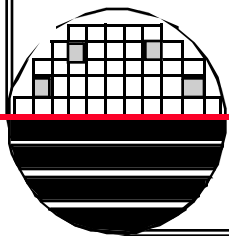
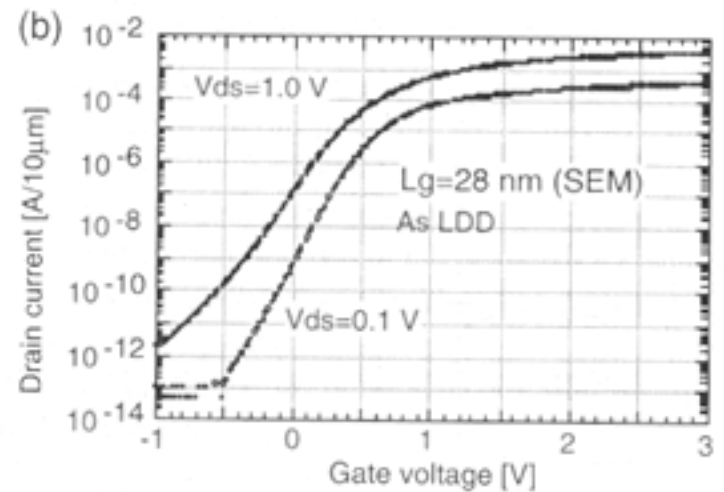
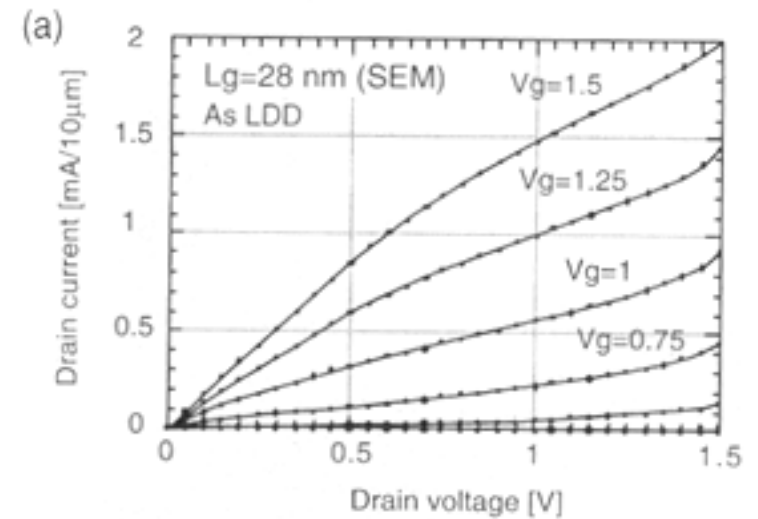
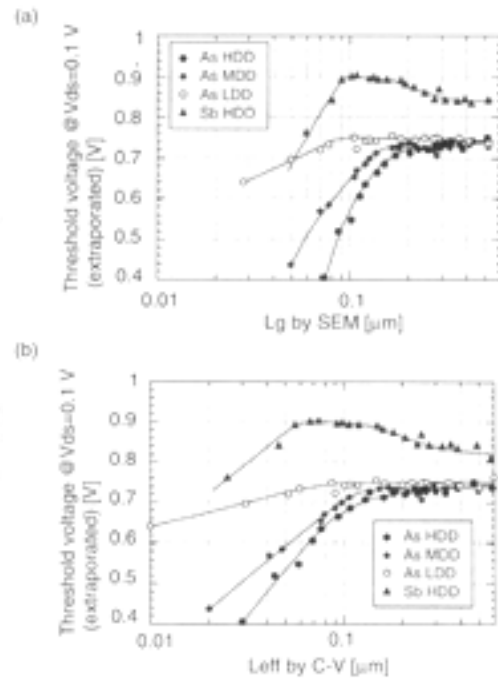
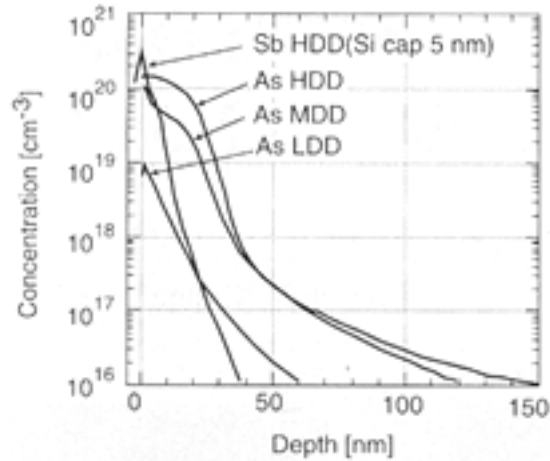


Fig. 1. SEM cross-sectional view of 30-nm poly-Si gate on 4-nm-thick gate oxide.

Xox 4.0 nm gate oxide



0.03 μm MOSFETS



0.025 μm

Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon–Carbon Source/Drain and Tensile-Stress Liner

Kah-Wee Ang, King-Jien Chui, Chih-Hang Tung, N. Balasubramanian,
Ming-Fu Li, Ganesh S. Samudra, and Yee-Chia Yeo

Abstract—We report the demonstration of 25-nm gate-length L_G strained nMOSFETs featuring the silicon–carbon source and drain ($\text{Si}_{1-y}\text{C}_y\text{S/D}$) regions and a thin-body thickness T_{body} of ~ 18 nm. This is also the smallest reported planar nMOSFET with the $\text{Si}_{1-y}\text{C}_y\text{S/D}$ stressors. Strain-induced mobility enhancement due to the $\text{Si}_{1-y}\text{C}_y\text{S/D}$ leads to a significant drive-current I_{Dsat} enhancement of 52% over the control transistor. Furthermore, the integration of tensile-stress SiN etch stop layer and $\text{Si}_{1-y}\text{C}_y\text{S/D}$ extends the I_{Dsat} enhancement to 67%. The performance enhancement was achieved for the devices with similar subthreshold swing and drain-induced barrier lowering. The $\text{Si}_{1-y}\text{C}_y\text{S/D}$ technology and its combination with the existing strained-silicon techniques are promising for the future high-performance CMOS applications.

Index Terms—Electron mobility, nMOSFET, silicon–carbon ($\text{Si}_{1-y}\text{C}_y$), silicon nitride liner, strain, stress.

I. INTRODUCTION

RECENTLY, channel-strain engineering is being actively pursued to enhance carrier mobility and drive current

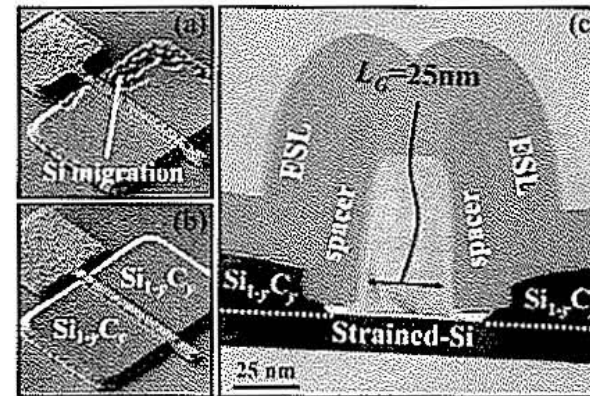


Fig. 1. (a) SEM image showing problems of silicon migration during the high temperature (800°C) prebake step in the $\text{Si}_{1-y}\text{C}_y$ selective epitaxy process. (b) Excellent morphology of $\text{Si}_{1-y}\text{C}_y$ on the S/D regions is demonstrated when a reduced prebake temperature (700°C) and a tightly controlled SOI body thickness are used. (c) TEM micrograph of a strained n-channel transistor with the $\text{Si}_{1-y}\text{C}_y\text{S/D}$ stressors and the high stress ESL. This transistor features the physical gate length L_G of 25 nm and the body thickness T_{body} of ~ 15 nm. A 25-nm-thick SiN ESL with the tensile stress of 1.1 GPa was used.

0.025 μm

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IEEE ELECTRON DEVICE LETTERS, VOL. 28, NO. 4, APRIL 2007

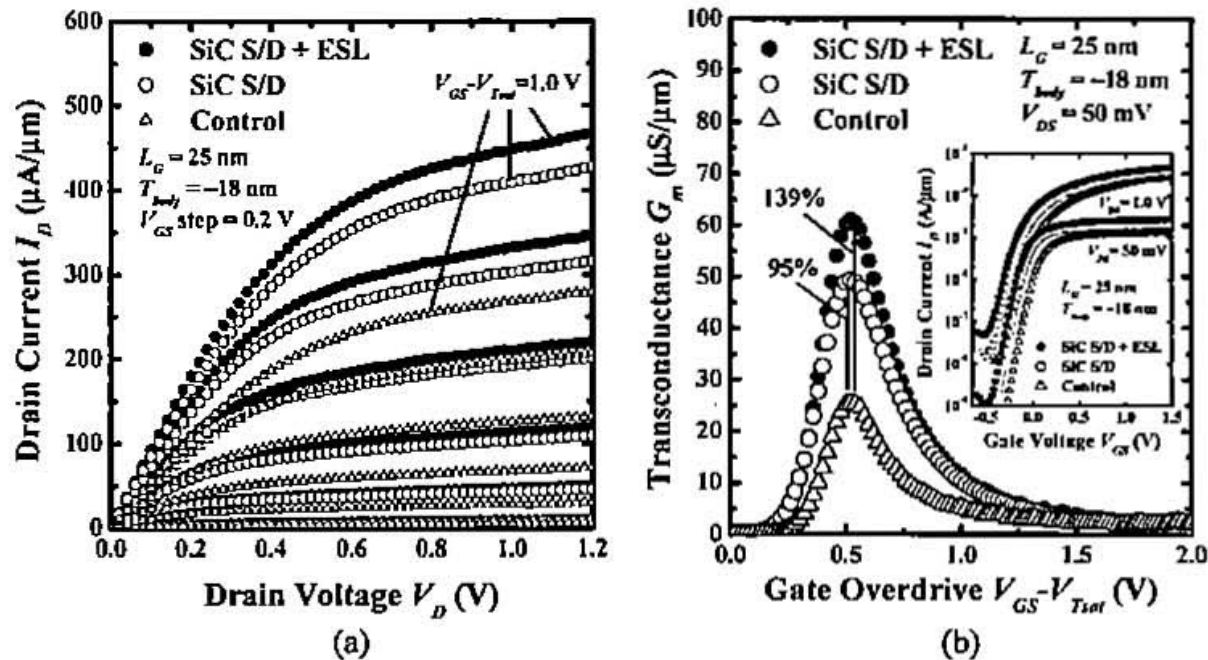
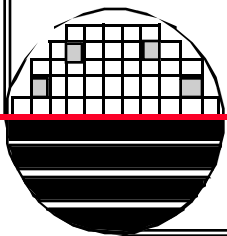


Fig. 2. (a) $I_{DS}-V_{DS}$ characteristics of the control and strained nMOSFETs with single stressor ($\text{Si}_{1-y}\text{C}_y\text{S/D}$) and dual stressors ($\text{Si}_{1-y}\text{C}_y\text{S/D}$ and tensile-stress SiN ESL). Significant $I_{D\text{sat}}$ enhancement of 52% is observed in the single stressor device over the control transistor. Even higher $I_{D\text{sat}}$ improvement of 67% is achieved with the integration of high stress ESL and $\text{Si}_{1-y}\text{C}_y\text{S/D}$. (b) Single and dual stressor strained devices are observed to enhance the transconductance by 95% and 139% over the control transistor, respectively.

0.025 μ m

IV. CONCLUSION

We demonstrated the successful integration of the $\text{Si}_{1-y}\text{C}_y$ S/D regions in the strained SOI nMOSFETs with the 25-nm gate lengths, enhancing the I_{Dsat} by 52%. Excellent subthreshold characteristics are achieved by the aggressive scaling of the SOI body thickness. Strain effects and I_{Dsat} are enhanced further by combining the high stress ESL and the $\text{Si}_{1-y}\text{C}_y$ S/D stressors. Further performance boost can be achieved with an increased $\text{Si}_{1-y}\text{C}_y$ S/D elevation.



0.02 μm MOSFET

IEEE ELECTRON DEVICE LETTERS, VOL. 21, NO. 4, APRIL 2000

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A 20-nm Physical Gate Length NMOSFET Featuring 1.2 nm Gate Oxide, Shallow Implanted Source and Drain and BF_2 Pockets

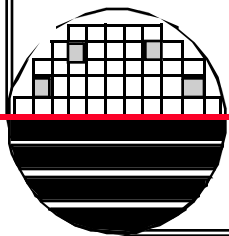
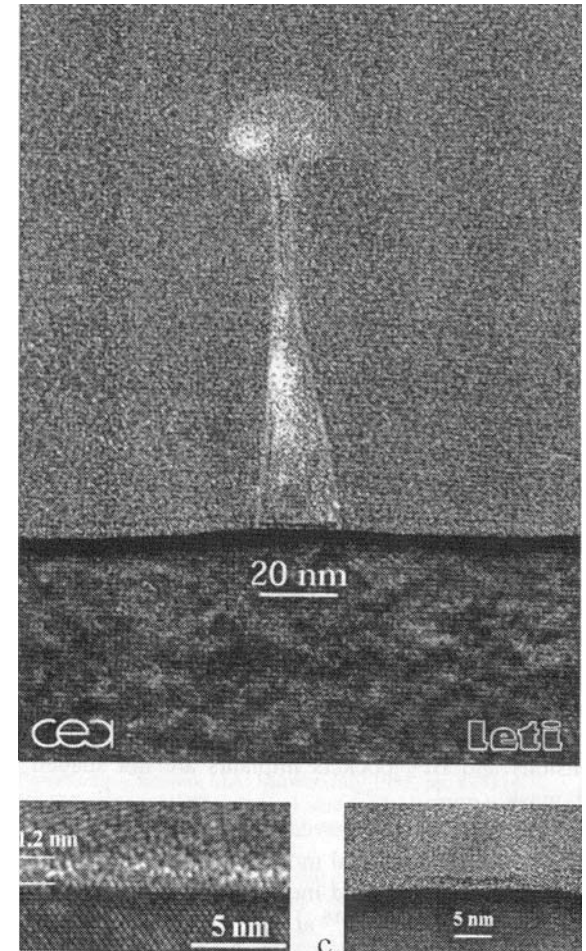
S. Deleonibus, Member, IEEE, C. Caillat, G. Guegan, M. Heitzmann, M. E. Nier, S. Tedesco, B. Dal'zotto, F. Martin, P. Mur, A. M. Papon, G. Lecarval, S. Biswas, and D. Souil

Abstract—We have demonstrated the feasibility of 20-nm gate length NMOSFET's using a two-step hard-mask etching technique. The gate oxide is 1.2-nm thick. We have achieved devices with real N^- arsenic implanted extensions and BF_2 pockets. The devices operate reasonably well down to 20-nm physical gate length. These devices are the shortest devices ever reported using a conventional architecture.

Index Terms—Hard mask, metallurgical length, NMOSFET, pockets, tunneling dielectric, 20-nm gate length.

I. INTRODUCTION

FOR THE first time, NMOSFET devices with a physical gate length down to 20 nm and a 1.2-nm thick gate oxide made in a conventional architecture are reported. Unlike the previous work on 14 nm EJ-MOSFET's [1], we have achieved devices with real N^- Arsenic implanted extensions and BF_2 pockets. Hence, our 20-nm gate length devices have a far much higher current drivality.



0.02 μm MOSFET

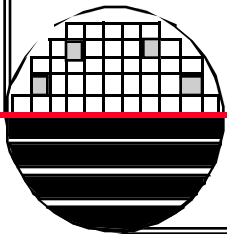
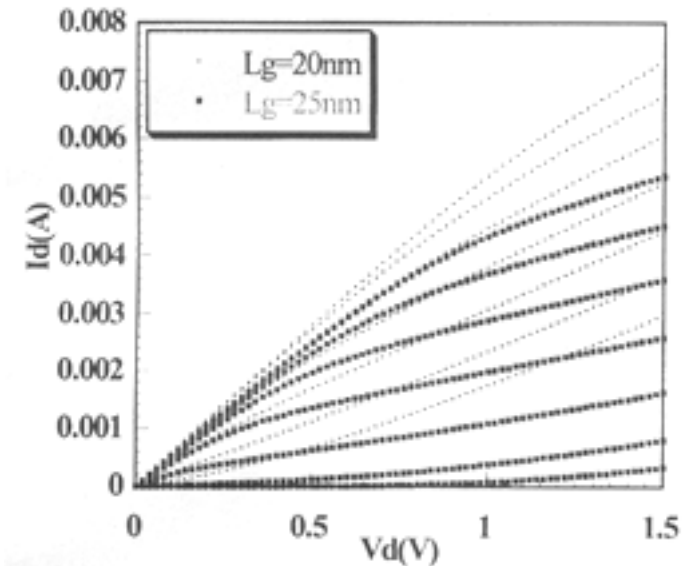
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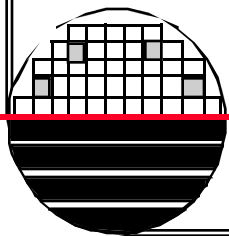
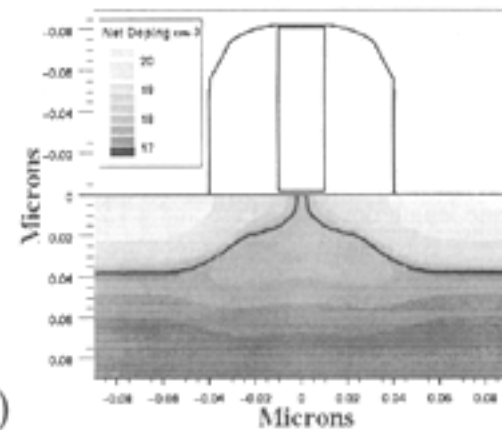
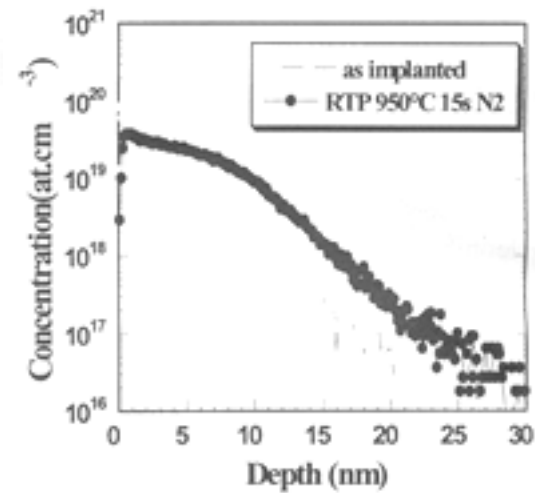
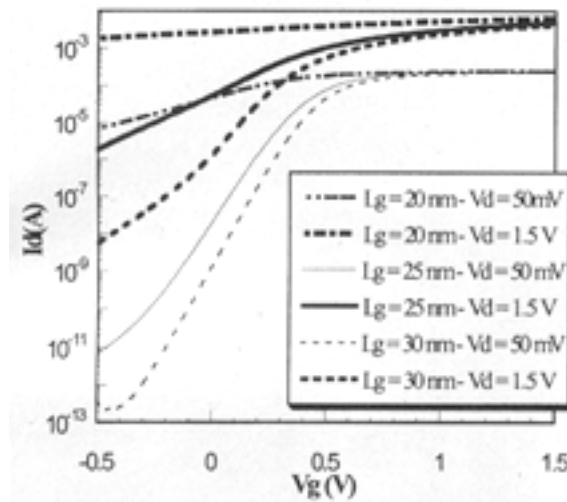
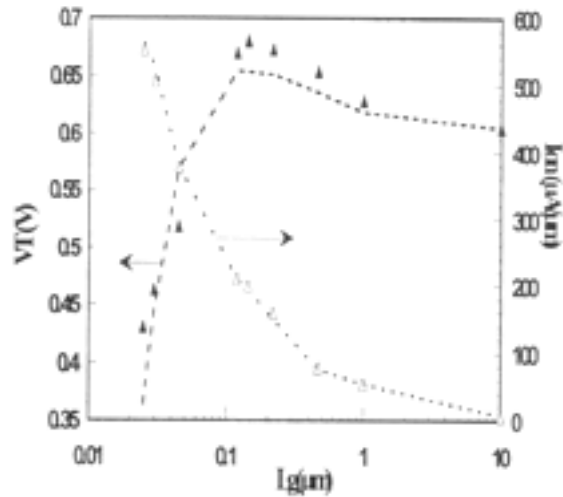
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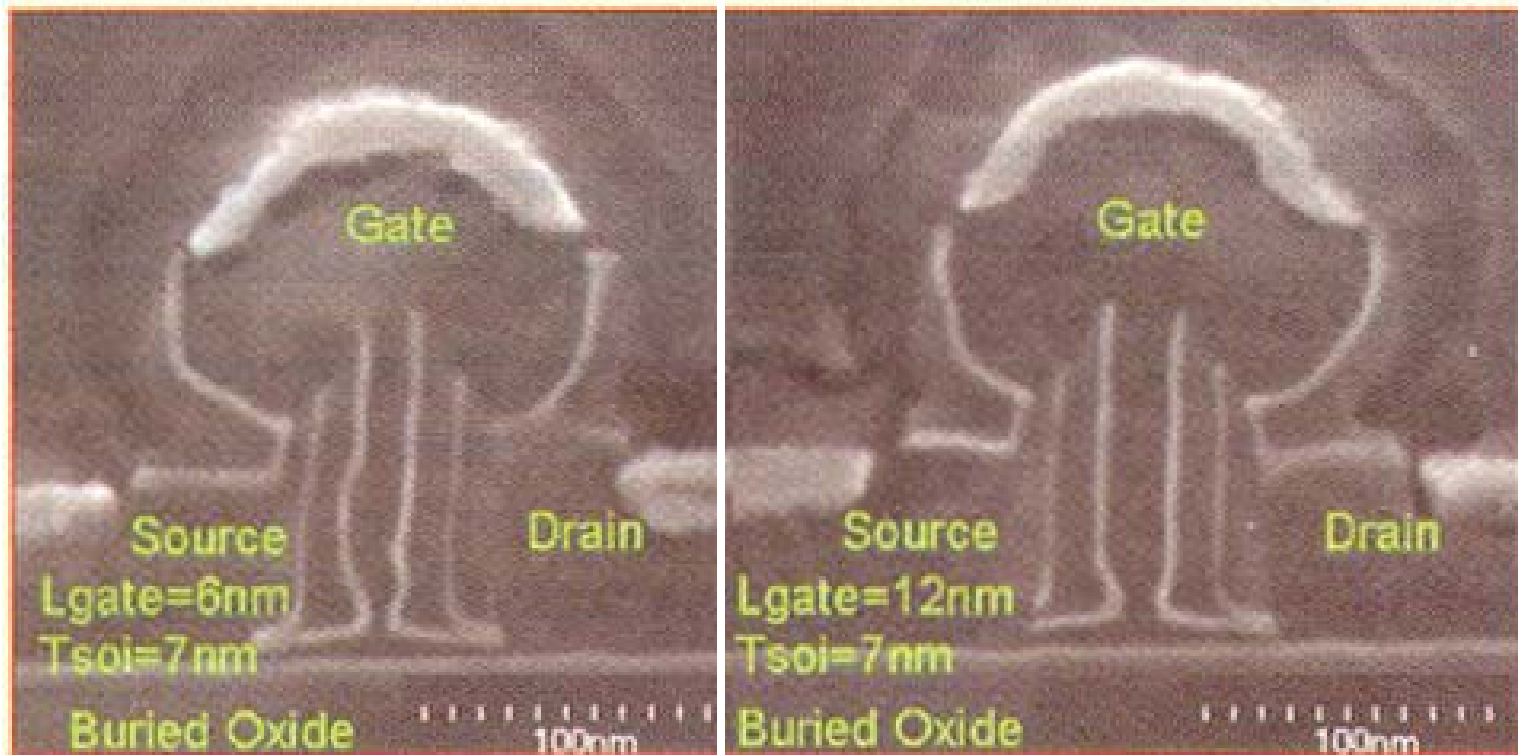
The gate oxide is found to be 1.2 nm thick by high resolution transmission electron microscopy (HR TEM) observation under a transistor gate of $100 \mu\text{m} \times 300 \mu\text{m}$ [Fig. 1(b)] or the 20-nm gate length devices [Fig. 1(c)]. Source and drain extensions are implanted with 3 keV accelerated arsenic. A dose of 10^{14} cm^{-2} leads to a junction depth (as implanted) of 11 nm at $10^{18} \text{ at.cm}^{-3}$ —measured by quadrupolar SIMS [4] [Fig. 2(a)]. One keV Cs^+ beam is used with a tilt angle of 60° to avoid ion mixing. BF_2 pockets are implanted with a moderate dose in order to reduce the short channel effect. A 30-nm wide spacer



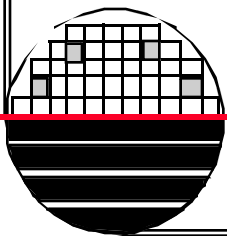
0.02 μm MOSFET



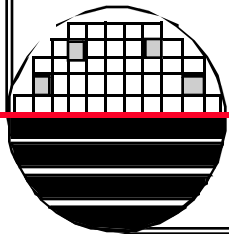
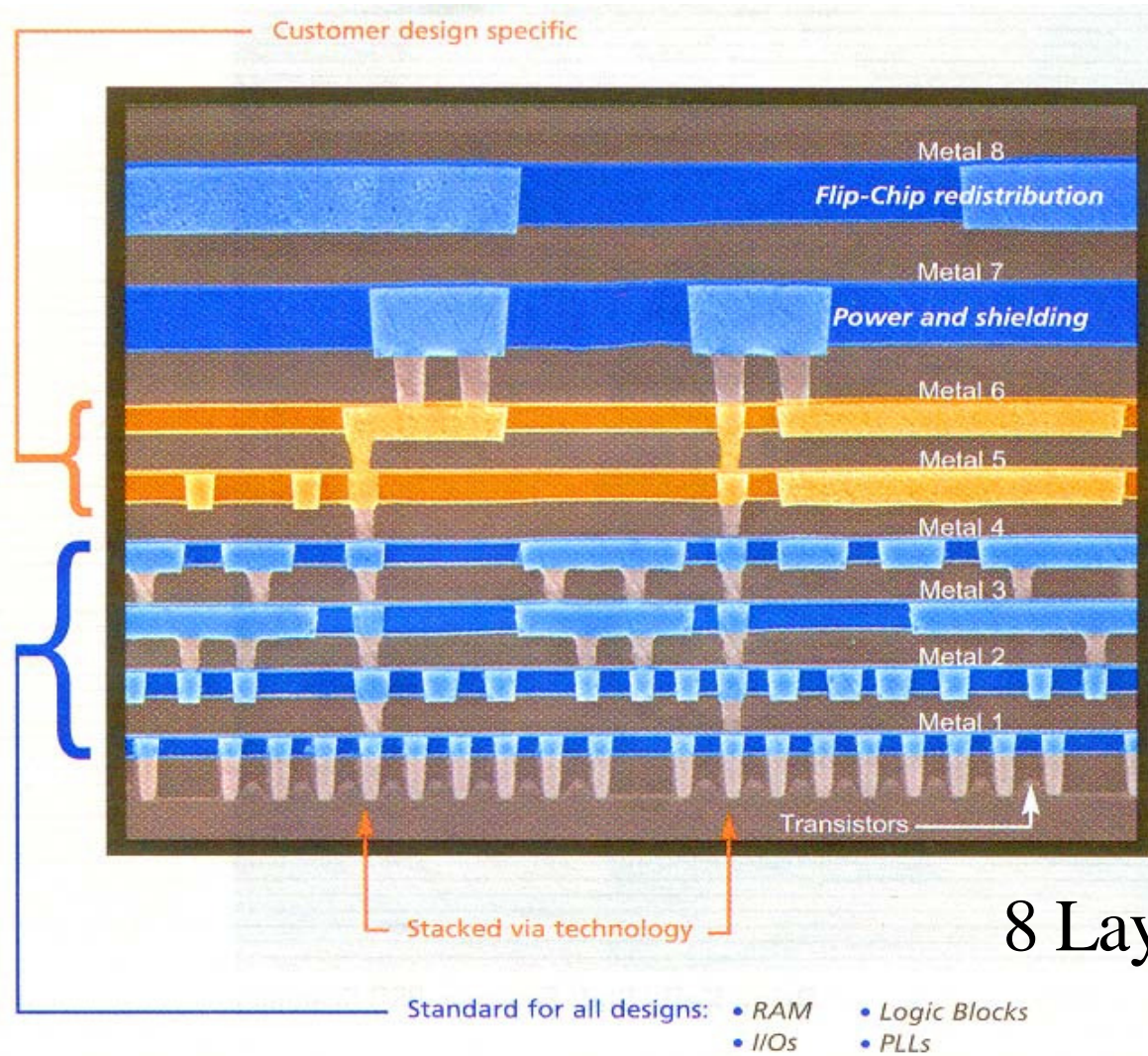
0.006 μm MOSFET



Channel is 4 nm thick on Buried Oxide. 8-19-2002

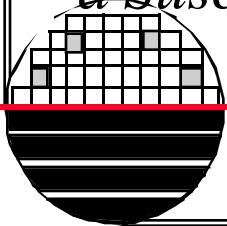


MULTILAYER METAL, W PLUGS, CMP



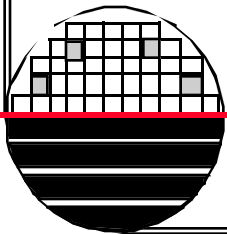
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<http://www.itrs.net>



HOMWORK- ADVANCED CMOS PART 1&2

1. Briefly describe the following CMOS process enhancements, a) silicide, b) salicide, c) dual doped gate CMOS, d) side wall spacers, e) gate stack formation, f) multi layer metal.
2. What types of lithography technology was used to make the $< 0.2 \mu\text{m}$ transistors described in this set of notes?
3. What types of isolation technology was used to make the CMOS devices described in this set of notes?
4. What technology is used to reduce Boron penetration through the gate oxide for the devices described in this set of notes?
5. Sketch the crosssection of the $0.07 \mu\text{m}$ CMOS described in this set of notes. Make the sketch to scale in both the lateral direction and the direction into the wafer.

