MICROELECTRONIC ENGINEERING
ROCHESTER INSTITUTE OF TECHNOLOGY

Advanced CMOS Process Technology
Part 3

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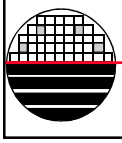

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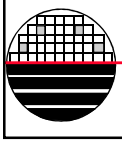
OUTLINE

Introduction
Strained Silicon
FinFET's
High-K, Metal Gate, Cu, Low-K
Advanced Lithography
Advanced Packaging



INTRODUCTION

At ~0.1 µm gate length and smaller MOSFET performance is degraded so much that further scaling does not give improved performance of the integrated circuit as a whole.

Electrostatics (constant field scaling)
- D/S space charge layer is bigger part of device length L
  - Vt rolloff, DIBL, channel length modulation (Lambda)
- Lower supply voltage means Lower threshold voltages
  - implies larger off-current for given sub-Vt slope

Parasitics
- Gate Oxide Leakage implies larger on-currents
- Higher Source Drain series resistance implies lower Idrive
- Gate Depletion reduces Idrive and gm

Channel Transport – High channel doping reduces Idrive and gm
- Current Drive proportional to mobility
- Transconductance proportional to mobility

STRAINED SILICON

deeper, strains appear

Intel's move to strained silicon at 90 nm has industry scrambling to react

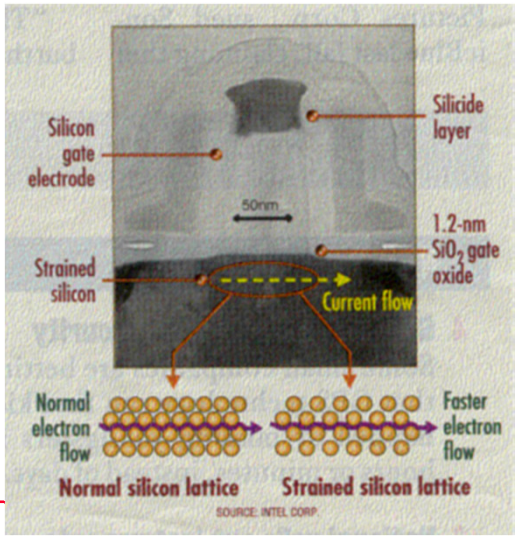
By David Lammers

AUSTIN, TEXAS – Intel Corp.'s announcement last week that it is adding strained silicon to its 90-nm technology mix stunned analysts and sent competitors into catch-up mode. One analyst, Dan Hutcheson of VLSI Research Corp., predicted that Intel's surprise move to implement a form of strained silicon at the 90-nm node–slated to move into manufacturing next year exclusively on 300-mm wafers at three Intel fabs–will reverberate as widely as IBM's 1997 decision to implement copper interconnects at 180-nm design rules.

Senior technology managers at half a dozen companies said last week that they either have decided to add strained silicon to their technology mix or already have dedicated research teams working on the problem.

STRAINED SILICON

Strained silicon can increase carrier mobility



STRAINED SILICON

A simple way to think about strained silicon follows: Tensile strain causes the silicon atoms to be pulled further apart making it easier for electrons to move through the silicon. On the other hand moving the atoms further apart makes it harder for holes to move because holes require bound electrons to move from a silicon atom to a neighboring silicon atom in the opposite direction, which is more difficult if they are further apart. Thus tensile strain increases mobility in n-type silicon and compressive strain increases mobility in p-type silicon (devices).

Strain can be created globally or locally. Growing an epitaxial layer of silicon on a silicon/germanium substrate creates (global) biaxial tensile strain in the silicon. N-MOSFETS built on these wafers will have higher mobility. P-MOSFETS will have lower mobility. Local strain can be created for each transistor such that N-MOSFETS see tensile strain and P-MOSFETS see compressive strain improving both transistors mobility. Local strain techniques include capping layers and introducing Ge or C in the source/drain regions.

INTRODUCTION TO STRAINED SILICON

The piezoresistive effect was first reported in 1954 [1] and has been used in making sensors for years. The effect of strain on the mobility of electrons and holes in semiconductors is important in today's sensors and transistors.

1. Charles S. Smith, “Piezoresistance Effect in Germanium and Silicon,” Physical Review, Vol 94, No.1, April 1, 1954.
2. Y. Kanda, “A graphical representation of the piezoresistance coefficients in silicon,” *Electron Devices, IEEE Transactions on,* vol. 29, no. 1, pp. 64-70, 1982.
3. C. Mazure, and I. Cayrefourcq, "Status of device mobility enhancement through strained silicon engineering." pp. 1-6.

CHARLES SMITH 1954

PHYSICAL REVIEW VOLUME 94, NUMBER 1 APRIL 1, 1954

Piezoresistance Effect in Germanium and Silicon

CHARLES S. SMITH
Bell Telephone Laboratories, Murray Hill, New Jersey
(Received December 30, 1953)

Uniaxial tension causes a change of resistivity in silicon and germanium of both *n* and *p* types. The complete tensor piezoresistance has been determined experimentally for these materials and expressed in terms of the pressure coefficient of resistivity and two simple shear coefficients. One of the shear coefficients for each of the materials is exceptionally large and cannot be explained in terms of previously known mechanisms. A possible microscopic mechanism proposed by C. Herring which could account for one large shear constant is discussed. This so called electron transfer effect arises in the structure of the energy bands of these semiconductors, and piezoresistance may therefore give important direct experimental information about this structure.

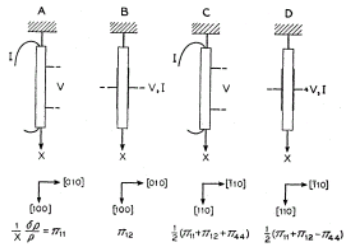
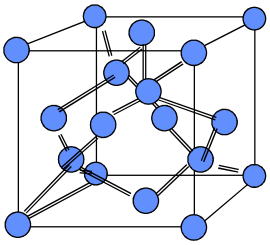


FIG. 1. Schematic diagram showing the stress system, the crystallographic orientations and the electrode structures which have been used. Arrangements A and C are designated as longitudinal in the text; B and D are called transverse.

CRYSTAL STRUCTURE

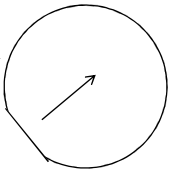
Diamond Lattice (Silicon)



Si

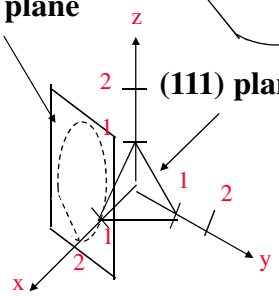
Equivalent Planes (100), (010), etc.
Directions <110>, <011>, etc.

(100) wafer
<110> direction



(100) plane

(111) plane



Miller Indices
(1/x,1,y,1/z)
smallest integer set

PIEZORESISTANCE

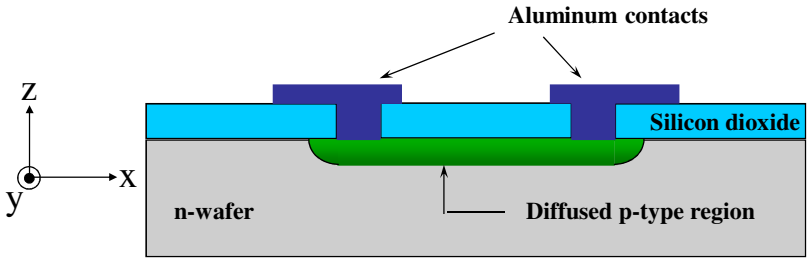
Piezoresistance is defined as the change in electrical resistance of a solid when subjected to stress. The piezorestivity coefficient is Π and a typical value may be $1E^{-10}$ cm^2/dyne.

The fractional change in resistance $\Delta R/R$ is given by:

$$\Delta R/R = \Pi \sigma$$

where σ is the stress in dyne/cm^2.

SINGLE CRYSTAL DIFFUSED RESISTORS



The n-type wafer is always biased positive with respect to the p-type diffused region. This ensures that the pn junction that is formed is in reverse bias, and there is no current leaking to the substrate. Current will flow through the diffused resistor from one contact to the other. The I-V characteristic follows Ohm's Law: I = V/R

Sheet Resistance $= \rho_s \sim 1/(q\mu \text{ Dose})$ ohms/square

EXPRESSION FOR RESISTANCE

$$R = Ro\,[\,1 + \pi_L\sigma_{xx} + \pi_T(\sigma_{yy} + \sigma_{zz})]$$

$$Ro = (L/W)(1/(q\mu(N,T)\text{ Dose}))$$

π_L is longitudinal piezoresistive coefficient
π_T is transverse piezoresistive coefficient
σ_{xx} is the x directed stress
σ_{yy} is the y directed stress

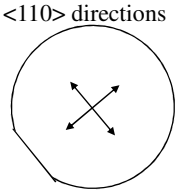
Charles S. Smith

PIEZORESISTANCE COEFFICIENTS

In the <110> direction

	π_L (E^{-11}/Pa)	π_T (E^{-11}/Pa)
Electrons	**-31.6**	**-17.6**
holes	**71.8**	**-66.3**

(100) wafer
<110> directions

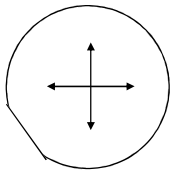


In the <100> direction

	π_L (E^{-11}/Pa)	π_T (E^{-11}/Pa)
Electrons	**-102**	**53.4**
holes	**6.6**	**-1.1**

Direction of
Carrier Flow

(100) wafer
<100> directions

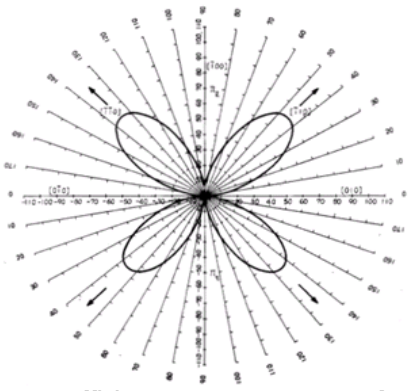


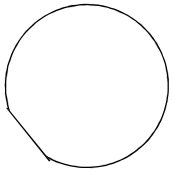
Tensile strain in (100) silicon increases mobility for electrons for flow in <110> direction
Compressive strain in (100) silicon increases mobility for holes for flow in <110> direction

Charles S. Smith

PIEZORESISTANCE COEFFICIENTS VS DIRECTION

For holes





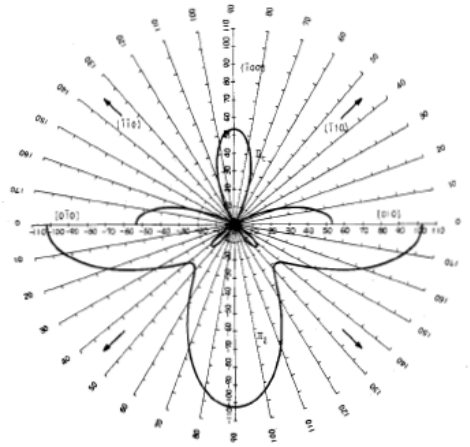
- Piezoresistance coefficients at room temperature for the (001) plane of p-Si

[2]

Y. Kanda

PIEZORESISTANCE COEFFICIENTS VS DIRECTION

For electrons



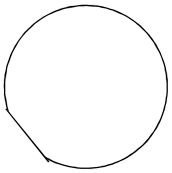


Fig. 2. Room temperature piezoresistance coefficients in the (001) plane of n-Si (10^{-12} cm^2/dyne).

Y. Kanda

SUMMARY FOR MOBILITY / STRAIN

1. Mobility is affected by strain in semiconductors. Mobility can be increased or decreased depending on the type of strain (tensile, compressive) and the direction of strain relative to crystal orientation and current flow.

For (100) wafers and current flow in <110> direction:

2. Tensile strain n-type silicon enhances mobility of electrons. Tensile strain transverse to current flow enhances mobility of electrons.

3. Compressive strain in the direction of current flow in p-type silicon enhances mobility of holes. Tensile strain transverse to current flow enhances mobility of holes.

0.025μm STRAINED SILICON MOSFET

Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon–Carbon Source/Drain and Tensile-Stress Liner

2007

Kah-Wee Ang, King-Jien Chui, Chih-Hang Tung, N. Balasubramanian, Ming-Fu Li, Ganesh S. Samudra, and Yee-Chia Yeo

Abstract—We report the demonstration of 25-nm gate-length L_G strained nMOSFETs featuring the silicon–carbon source and drain ($Si_{1-y}C_y$S/D) regions and a thin-body thickness T_{body} of ~18 nm. This is also the smallest reported planar nMOSFET with the $Si_{1-y}C_y$S/D stressors. Strain-induced mobility enhancement due to the $Si_{1-y}C_y$S/D leads to a significant drive-current I_{Dsat} enhancement of 52% over the control transistor. Furthermore, the integration of tensile-stress SiN etch stop layer and $Si_{1-y}C_y$S/D extends the I_{Dsat} enhancement to 67%. The performance enhancement was achieved for the devices with similar subthreshold swing and drain-induced barrier lowering. The $Si_{1-y}C_y$S/D technology and its combination with the existing strained-silicon techniques are promising for the future high-performance CMOS applications.

Index Terms—Electron mobility, nMOSFET, silicon–carbon ($Si_{1-y}C_y$), silicon nitride liner, strain, stress.

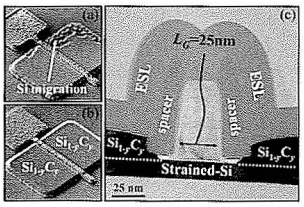


Fig. 1. (a) SEM image showing problems of silicon migration during the high temperature (800 °C) prebake step in the $Si_{1-y}C_y$ selective epitaxy process. (b) Excellent morphology of $Si_{1-y}C_y$ on the S/D regions is demonstrated when a reduced prebake temperature (700 °C) and a tightly controlled SOI body thickness are used. (c) TEM micrograph of a strained n-channel transistor with the $Si_{1-y}C_y$S/D stressors and the high stress ESL. This transistor features the physical gate length L_G of 25 nm and the body thickness T_{body} of ~15 nm. A 25-nm-thick SiN ESL with the tensile stress of 1.1 GPa was used.

I. Introduction

RECENTLY, channel-strain engineering is being actively pursued to enhance carrier mobility and drive current

0.025μm STRAINED SILICON MOSFET

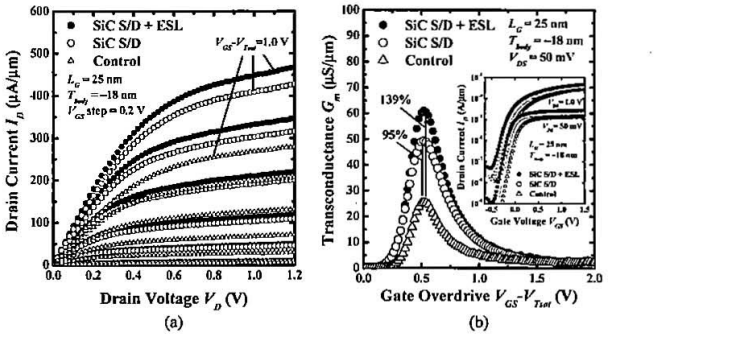


Fig. 2. (a) I_{DS}–V_{DS} characteristics of the control and strained nMOSFETs with single stressor ($Si_{1-y}C_y$S/D) and dual stressors ($Si_{1-y}C_y$S/D and tensile-stress SiN ESL). Significant I_{Dsat} enhancement of 52% is observed in the single stressor device over the control transistor. Even higher I_{Dsat} improvement of 67% is achieved with the integration of high stress ESL and $Si_{1-y}C_y$S/D. (b) Single and dual stressor strained devices are observed to enhance the transconductance by 95% and 139% over the control transistor, respectively.

0.025μm STRAINED SILICON MOSFET

IV. Conclusion

We demonstrated the successful integration of the $Si_{1-y}C_y$ S/D regions in the strained SOI nMOSFETs with the 25-nm gate lengths, enhancing the I_{Dsat} by 52%. Excellent subthreshold characteristics are achieved by the aggressive scaling of the SOI body thickness. Strain effects and I_{Dsat} are enhanced further by combining the high stress ESL and the $Si_{1-y}C_y$ S/D stressors. Further performance boost can be achieved with an increased $Si_{1-y}C_y$ S/D elevation.

STRAINED SILICON

AmberWave strained-silicon process removes troublesome SiGe layer

By David Lammers

AUSTIN, TEXAS – AmberWave Systems Corp. (Salem, N.H.) claims to have worked out a form of strained silicon that removes the silicon germanium layer, providing the ultrathin silicon top layer required for high-performance devices.

The process isn't cheap: Eventually, it could be about 50 percent more costly than a bonded-type SOI wafer, according to AmberWave CEO Mark Wolf. In strained-silicon on silicon-on-insulator (SS-SOI), the relaxed SiGe layer normally is left intact to provide a strain on the thin top layer of silicon.

Achieving strained silicon on an SOI wafer normally involves forming a thin (20- to 50-nanometer) combined layer of SiGe and strained silicon, a difficult thickness to achieve for the combined SiGe-Si films.

In the AmberWave process, presented at the recent IEEE SOI conference in Williamsburg, Va., strained silicon is flipped onto an oxide layer. A SiGe layer is created and planarized by chemical mechanical polishing to remove the cross-hatch surface roughness. The CMP step is key to controlling the thickness of the top films, said AmberWave co-founder Mayank Bulsara, who worked on the process development.

A 200-nm SiGe layer is deposited on the planarized SiGe, and then a thin layer of strained silicon is created on top. Hydrogen is implanted through the strained-silicon layer to induce a cleave plane, allowing the wafer to be split later in the process.

Next, the implanted structure is bonded to an oxidized silicon handle wafer. The transferred silicon germanium layer is oxidized and etched away selectively, with the oxidation stopping at the layer of strained silicon. The result is a thin layer of strained silicon bonded to an oxide layer.

"Creating a silicon layer that is tens of nanometers thick normally is very difficult. By bonding an integrated strained-silicon layer on top of the oxide, there are no fundamental issues to keeping the silicon layer as thin as possible," said Bulsara.

Twin challenges

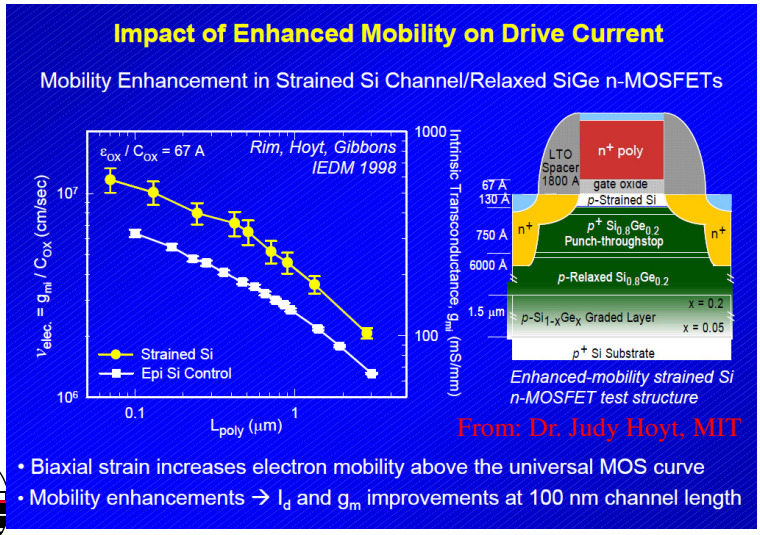
The process removes the twin challenges of SiGe thermal instability and contamination from the germanium atoms. And without the SiGe layer, the top active layer can be thinner, which is important to achieving a fully depleted state, Bulsara said.

CEO Wolf said the process could improve the device drive current significantly. But the process is in the developmental stage and will take several years to work out, Wolf added.

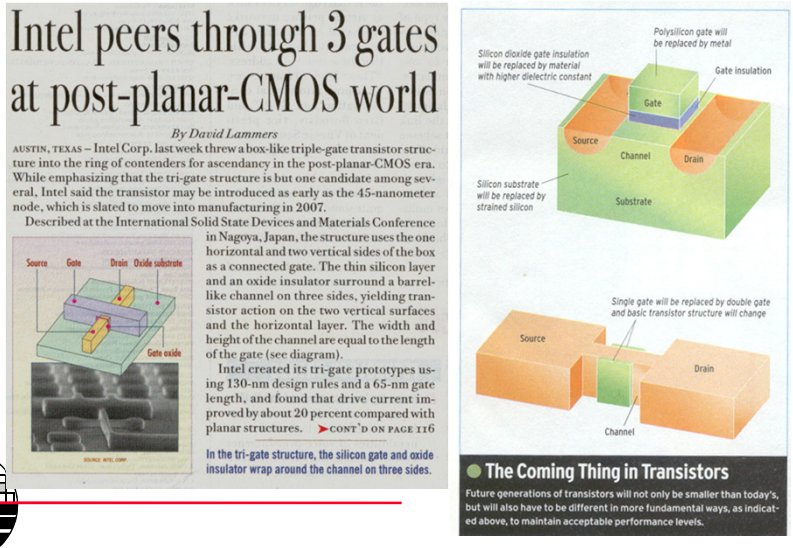
AmberWave is a spinout from the Massachusetts Institute of Technology, which offers a licensable form of strained-silicon technology. Advanced Micro Devices Inc. has confirmed that it is working with AmberWave on an SS-SOI process, and several other customers are using AmberWave's intellectual property for 130-nm strained-silicon devices fabricated at an unidentified foundry in Taiwan.

Silicon SOI wafers with bi-axial tensile strain

BI-AXIAL STRAIN



THREE GATE TRANSISTORS



Intel peers through 3 gates at post-planar-CMOS world

By David Lammers

AUSTIN, TEXAS – Intel Corp. last week threw a box-like triple-gate transistor structure into the ring of contenders for ascendancy in the post-planar-CMOS era. While emphasizing that the tri-gate structure is but one candidate among several, Intel said the transistor may be introduced as early as the 45-nanometer node, which is slated to move into manufacturing in 2007.

Described at the International Solid State Devices and Materials Conference in Nagoya, Japan, the structure uses the one horizontal and two vertical sides of the box as a connected gate. The thin silicon layer and an oxide insulator surround a barrel-like channel on three sides, yielding transistor action on the two vertical surfaces and the horizontal layer. The width and height of the channel are equal to the length of the gate (see diagram).

Intel created its tri-gate prototypes using 130-nm design rules and a 65-nm gate length, and found that drive current improved by about 20 percent compared with planar structures. ➤CONT'D ON PAGE 116

In the tri-gate structure, the silicon gate and oxide insulator wrap around the channel on three sides.

TRIPLE-GATE TRANSISTOR

Intel details its triple-gate transistor structure

➤CONTINUED FROM PAGE 1

The company claims the structure also facilitates the depletion effect in fully depleted transistors. "Just as it is easier to squeeze something from three sides instead of from just one side, the triple-gate device allows us to fully deplete the silicon layer, surrounded on three sides by gate oxide and gate electrode materials," said Gerald Marcyk, director of components research at Intel's logic development center in Hillsboro, Ore.

"We at Intel, and others in the industry, believe that we're getting closer to a fundamental shift in how we make transistors, largely because of leakage and power considerations," Marcyk added. "We need a different kind of structure, and we believe this tri-gate structure is a good step. But I can't say it is the final step."

The leakage current compared with bulk planar devices improved by about 10 to 100 times, Intel reported. That's similar to the power improvement seen with planar fully depleted silicon-on-insulator (SOI) transistors.

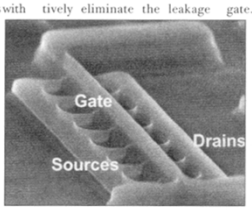
Power concerns are what's motivating Intel to consider fully depleted structures, and Marcyk said the tri-gate scheme may prove more manufacturable on SOI wafers than planar structures would be. To create a fully depleted box structure with a 30-nm gate length, the thickness of the silicon can be kept at 30 nm–a more manageable challenge than the 10-nm silicon thickness that may be required with a planar fully depleted SOI-type device, he said.

'We're getting closer to a fundamental shift in how we make transistors.'

Intel has demonstrated conventional planar transistors with gate lengths of 20 nm, and brute-force scaling is expected to enable performance and density gains. But the I_{off} is too high for microprocessors with 100 million to 200 million transistors. Such small planar transistors suffer high sub-threshold leakage as the gate electrodes are brought closer together, and leakage through the gate oxide also increases exponentially.

"As we shrink the gate below 30 nm, the I_{off} becomes unacceptable for actual devices with hundreds of millions of transistors," Marcyk said.

At last December's International Electron Devices Meeting (IEDM) in Washington, Intel proposed a fully depleted structure called the Depleted Substrate Transistor (DST). While such a structure would effectively eliminate the leakage from the source to the drain, the DST presents a manufacturing challenge: "It requires us to put the transistor on an ultrathin layer of silicon which is much smaller than the gate length," Marcyk said. "If you have a 30-nm gate length, you have to accelerate your lithography road map. With a FinFET, the smallest feature becomes the fin, rather than the gate. You have to extend your lithography to figure out how to pattern the fin. If you talk to anybody in the research community, that's the problem," Marcyk said.



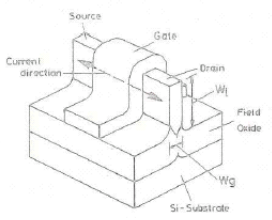
Intel's tri-gate structure uses a 65-nm gate length and 130-nm design rules to improve drive current.

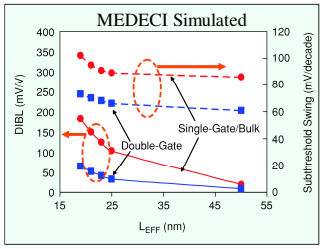
Further, FinFET performance has proved disappointing, he said.

"If we try to make a double gate structure in a really tall fin, it is hard to make something with that aspect ratio. In our case, if the width is equal to the height, it is a little better geometry–easier to etch–and you don't have to worry about the lines [for the fin] leaning over," he said.

"The triple-gate devices are very scalable to smaller sizes. But this [structure] is just a pos-

TRIPLE GATE TRANSISTOR





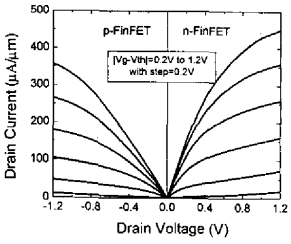


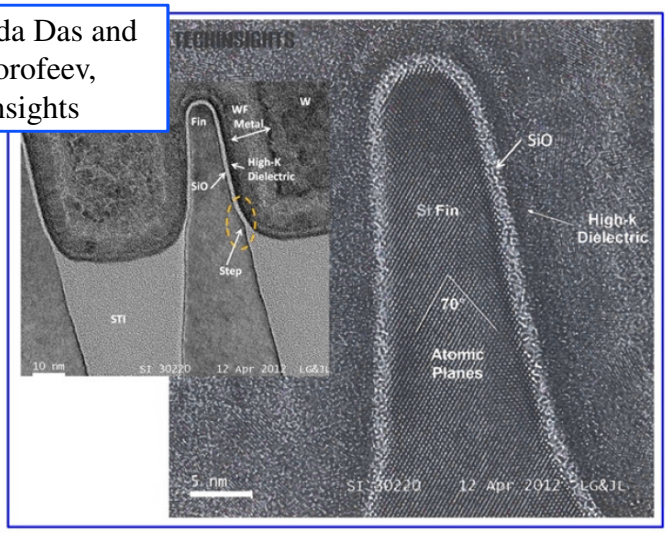
Fig.5 Id-Vd characteristics of 10nm gate length CMOS FinFET transistors.

- The drive currents are 446 uA/um for n-FinFET and 356 uA/um for p-FinFET respectively
- The peak transconductance of the p-FinFET is very high (633uS/um at 105 nm L_g), because the hole mobility in the (110) channel is enhanced
- Gate Delay is 0.34 ps for n-FET and 0.43 ps for p-FET respectively at 10 nm Lg
- The subthreshold slope is ~60 mV/dec for n-FET and 101 mV/dec for p-FET respectively
- The DIBL is 71 mV/V n-FET and 120 mV/V for p-FET respectively

Qin Zhang, 04/19/2005

FIN FET

from: Arabinda Das and Alexandre Dorofeev, UBM Tech Insights



FIN FETS IN FLASH MEMORY

FinFETs Used in Smallest Non-Volatile Flash Memory
Peter Singer, Editor-In-Chief – 2/1/2005
Semiconductor International

Acrobat Document

Scientists at Infineon Technologies AG (Munich, Germany) have built the world's smallest non-volatile flash memory cell using finFETs. With gate dimensions measuring only 20 nm, the new memory cell would make non-volatile memory chips with a capacity of 32 Gb possible within a few years. That is 8× the capacity of what is currently available on the market.

Non-volatile flash memories are becoming increasingly popular as mass storage media for devices such as digital cameras, camcorders and USB sticks. The most advanced non-volatile flash memory devices available today can permanently store one or two bits of information per memory cell without a supply voltage.

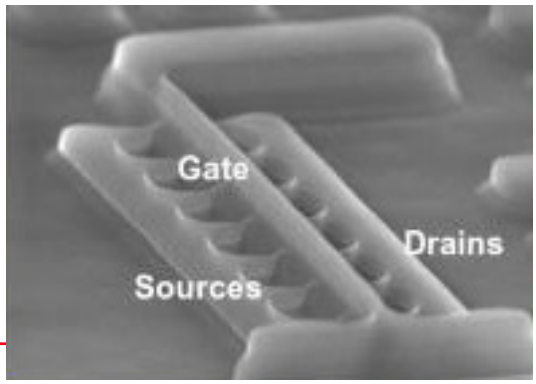
The International Technology Roadmap for Semiconductors (ITRS) notes that future high-density flash memories for standalone data storage applications require devices with minimum feature size F smaller than 50 nm. To achieve that, Infineon researchers used a three-dimensional transistor device called the finFET, so named because part of the structure sticks up like a shark's fine (Figure). By wrapping the gate electrode around the gate dielectric, this type of device provides greater control over carrier flow and leakage current. When used in memory

20 nm gate length fin FETS used in worlds smallest flash memory cell.

Possible future chips with capacity of 32 Gbit.

SUMMARY FOR FINFETS AND TRIPLE GATE FETS

1. Fin FETS have higher gm and Idrive because mobility is increased with lower doped channels.
2. Fin FETs have higher sub-threshold slope.
3. Fin FETS have lower DIBL



HIGH-K, METAL GATES, Cu, LOW-K, STRAINED Si

(HK+MG) from top chipmakers including Intel and IBM, as well as NEC, Toshiba, and Samsung.

CMP EETIMES ONLINE

EE Times: Latest News

Intel to get more bang for 45-nm buck

Mark LaPedus
(06/26/2007 8:20 PM EDT)
URL: http://www.eetimes.com/showArticle.jhtml?articleID=200000872

SANTA CLARA, Calif. — With its new fab and capital efficiency programs in place, Intel Corp. is readying a massive shift towards 45-nm chip production.

In total, Intel (Santa Clara, Calif.) has four 300-mm fabs in place that are geared for 45-nm chip production. Two fabs are expected to begin 45-nm manufacturing in the second half of this year, with two more plants slated for production in 2008.

The chip giant is also looking to get more bang for its buck in the fab, by advancing its intelligent fab automation, tool re-use and equipment efficiency efforts at the 45-nm node. In doing so, the company can keep its capital spending relatively flat — and maintain its leadership position in process technology over AMD, IBM and other rivals, according to Intel

In other words, the days of throwing money at new fab projects in a willy-nilly fashion are over at the chip giant. Seeking to get a jump on its rivals, Intel last year originally disclosed the initial details of its 45-nm process. The technology, dubbed P1266, incorporates the company's first adoption of high-k dielectrics and metal gates. It also consists of copper interconnects, low-k dielectrics, strained silicon and other features.

The planned 45-nm ramp, which remains "on track," will give the company a lead of about five quarters over the competition, said Tom Franz, vice president and general manager of fab/sort manufacturing for the Technology and Manufacturing Group at Intel.

"We can also say that we're at least one year ahead of the competition," Franz said in an interview at the company's headquarters here on Tuesday (June 26). In the interview, Franz outlined the company's 45-nm fab ramp -- and the challenges -- associated with the technology.

Intel has disclosed many of its 45-nm fab plans over the last year or two. The fabs are all 300-mm plants. As expected, Intel will initially move into 45-nm production within its D1D fab in Hillsboro, Ore. Intel has been sampling its 45-nm devices, but production is slated for the second of this year.

Also in the second half of 2007, Intel is expected to move into 45-nm production within its Fab 32 plant in Chandler, Ariz. In the second half of 2008, Intel is projected to ramp up two more 45-nm fabs, including Fab 28 in Israel and Fab 11x in New Mexico.

Despite the fab ramp, Intel is also moving to drive down capital costs and improve operational efficiencies. In the past, Intel attempted to outspend its rivals in terms of capital expenditures. The company remains one of the world's largest buyers of fab equipment, but its capital expenditures have remained flat in recent times — much to the chagrin of its fab-tool and materials suppliers. Applied, ASMI, ASML, Hitachi, Nikon, Novellus, TEL and Varian are among Intel's tool suppliers.

Intel's capital spending is projected to hit $5.5 billion in 2007, down from $5.766 billion in 2006, according to Pacific Crest Securities Inc. (Portland, Ore.). In 2008, Intel is projected to spend $5.3 billion, down 4 percent over 2007, according to the firm.

Overall, South Korea's Samsung Electronics Co. Ltd. is the largest buyer of equipment, surpassing Intel some time ago, according to the firm.

HIGH-K FOR GATES

In its approach, "TI will leverage a chemical vapor deposition (CVD) process to deposit hafnium silicon oxide (HfSiO), followed by a reaction with a downstream nitrogen plasma process to form HfSiON or hafnium silicon oxynitride. By implementing the nitrided CVD technique, TI is able to solve the leakage issue without degradation of the other key parameters that customers have come to expect from SiO2-based gate dielectrics," according to the company. "Through a modular addition to the typical CMOS gate stack process, HfSiON integration has been demonstrated offering mobility that is 90 percent of the silicon dioxide universal mobility curve, with effective oxide thicknesses (EOTs) below 1-nm," according to TI.

EE Times, June 2007

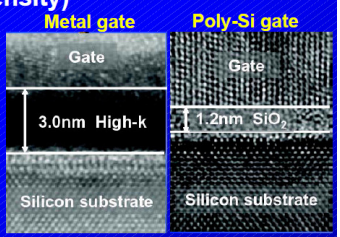
HIGH K, METAL GATE

Parasitics: Gate Electrode Depletion

- Gate Electrode Depletion:
  - Lower inversion charge density effectively limits EOT scaling
- Solution:
  - metal gates (high carrier density)
  - may also assist with high k mobility issues

From: Dr. Judy Hoyt MIT

R. Chau, et al., Intel, Nov. 2003



- Gate stack considered as a complete package:
  - Channel, dielectric, electrode

SUMMARY

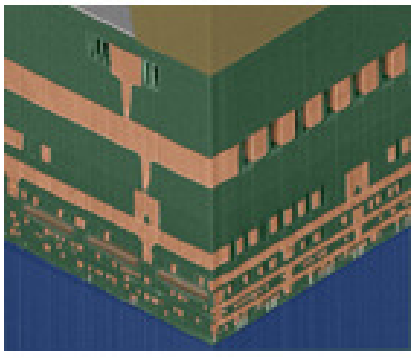
Electrostatics (constant field scaling)
- D/S space charge layer is bigger part of device length L
  - Vt rolloff, DIBL, channel length modulation (Lambda)
  - (Fin FETs reduce effect of D/S space charge regions)
- Lower supply voltage means Lower threshold voltages
  - implies larger off-current for given sub-Vt slope
  - (Increase sub-Vt slope with FINFETs)

Parasitic
- Gate Oxide Leakage implies larger on-currents (High K gate)
- Higher Source Drain series resistance implies lower Idrive (Schottky Metal Drain and Source)
- Gate Depletion reduces Idrive and gm (Metal gate)

Channel Transport – High channel doping reduces Idrive and gm
- Current Drive proportional to mobility
- Transconductance proportional to mobility

(Increase mobility with strained silicon, higher mobility materials)

LOW-K FOR INTERCONNECT



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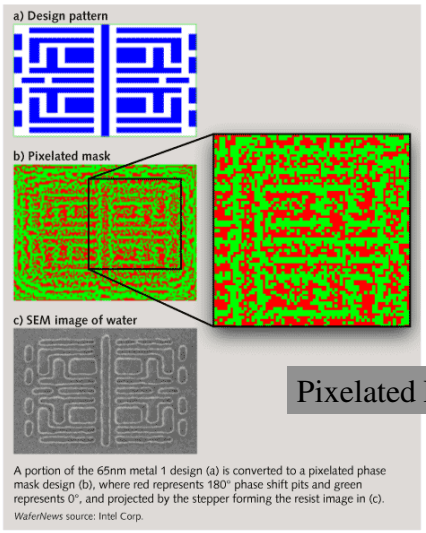
070608: IITC2007 airgaps & chip-stacks

Ed's Threads 070608
Musings by Ed Korczynski on June 08, 2007

IITC 2007: Airgaps & chip-stacks
Airgaps and 3D-stacks were the big news from the 10th International Interconnect Technology Conference (IITC) recently held near the San Francisco airport. Two major new materials was presented—IBM showed rhodium (Rh) electro-chemical deposition (ECD) for ≤32nm contact plugs, and Fujitsu showed nano-clustered silicon (NCS) with low k=2.25 for a dielectric—but most new work involves the same materials combined in clever new ways. Airgap technology was covered in four oral presentations, three posters, and countless informal hallway discussions.

Dan Edelstein, IBM Fellow and manager of BEOL technology strategy at Yorktown Heights, NY, gave an invited talk on the many integration challenges for 32nm node interconnects, including resist poisoning from low-k outgassing, low-k damage removal, and the need for improved thin-film interfaces. "We need to keep adding innovation just to stay on the trend-line," he commented. For example, the industry has historically seen chronically low SiCOH low-k adhesion on SiCHN barrier layers—regardless of equipment, CVD precursor, or plasma preclean—due to a carbon-rich initial deposition. Adding a diverter-valve to the tool allows for stabilized precursor flow before RF power is turned on, which eliminates the carbon-rich deposition and thus solves the adhesion issue. With subtle integration challenges such as these, IBM has chosen to add airgaps as a side-loop with no new materials, tools, or baseline processes. Airgaps drop k by ~35% for any given dielectric material, Edelstein noted, adding that IBM has "shown this on gapped SiOF and low-k SiCOH, and will do it next on ULK porous SiCOH."

ADVANCED LITHOGRAPHY

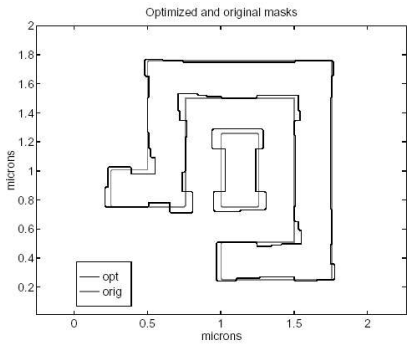


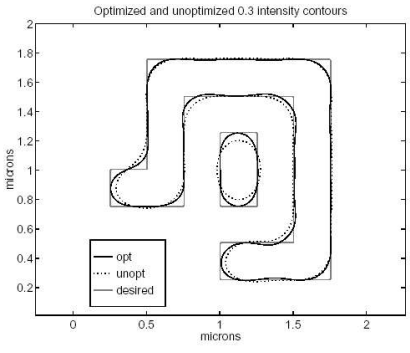
A portion of the 65nm metal 1 design (a) is converted to a pixelated phase mask design (b), where red represents 180° phase shift pits and green represents 0°, and projected by the stepper forming the resist image in (c).
WaferNews source: Intel Corp.

- Immersion Lithography
- Optical Proximity Correction
- Phase Shift Masks
- Off Axis Illumination
- Resist Trimming
- Double Exposure

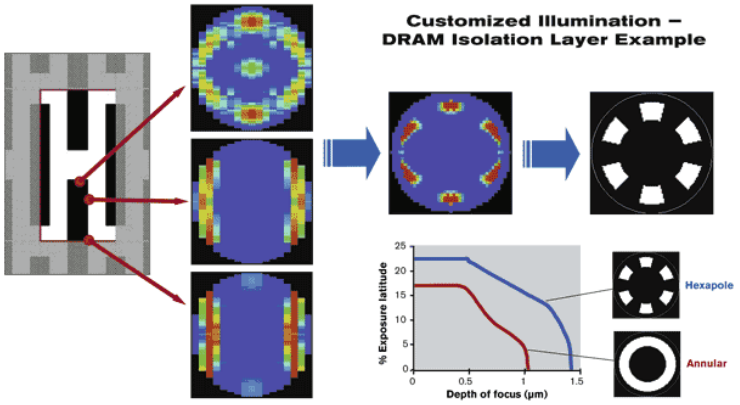
Pixelated Phase Shift Mask

OPTICAL PROXIMITY CORRECTION (OPC)



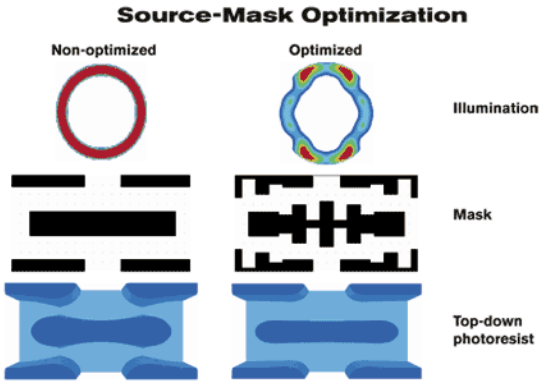


CUSTOM OFF AXIS ILLUMINATION AND MASK



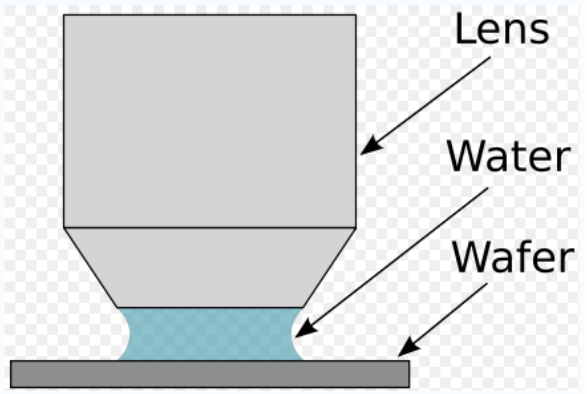
1. The lithography process window for a typical pattern, a DRAM isolation layer, can be improved by using an optimized Illuminator customized for that layer. In this example, NA=0.8, λ=248 nm and CD=120 nm.

CUSTOM OFF AXIS ILLUMINATION AND MASK



2. It is possible to optimize both mask layout and illumination simultaneously — called source- mask optimization (SMO) — to maximize image contrast.

IMMERSION LITHOGRAPHY

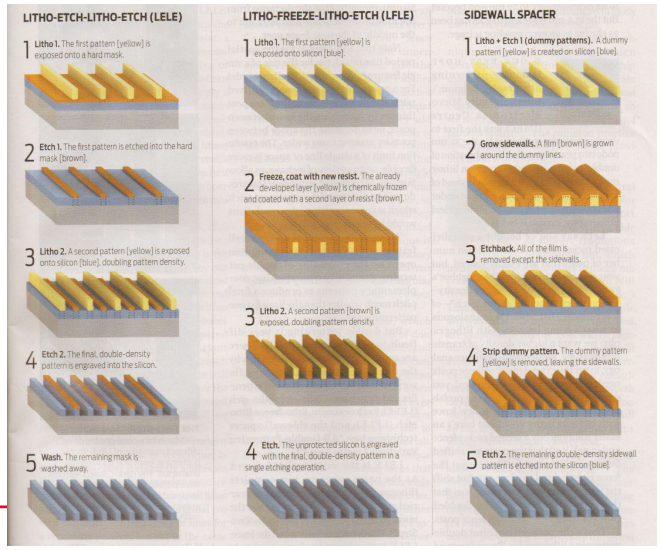


Immersion_lithography_illustration.svg (SVG file, nominally 433 × 290 pixels

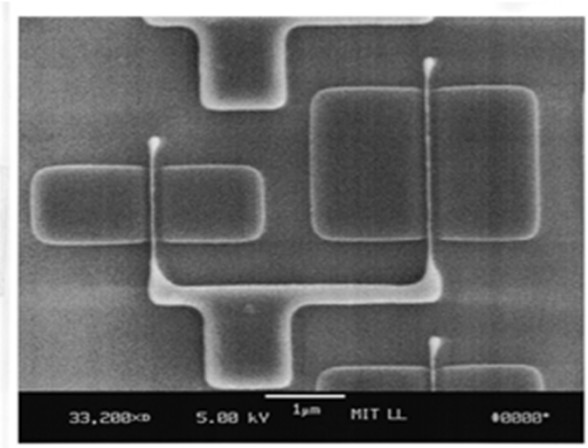
Increases NA
Increased Resolution

DOUBLE PATTERNING

IEEE Spectrum, Nov 2008
Page 49



DOUBLE EXPOSURE



Double Exposure: 25nm gate features – arguably the physical limit of CMOS! – printed by MIT Lincoln Lab with a 0.60NA KrF stepper (Canon FPA-3000EX4). Source: MIT Lincoln Lab.

RESIST TRIMMING

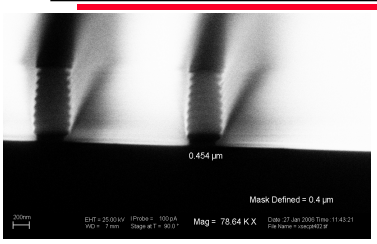


Figure 17: 0.45 μm PR Line Before Trim

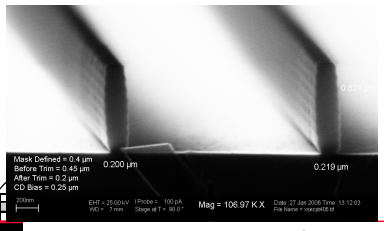


Figure 18: 0.2 μm PR Line After Trim

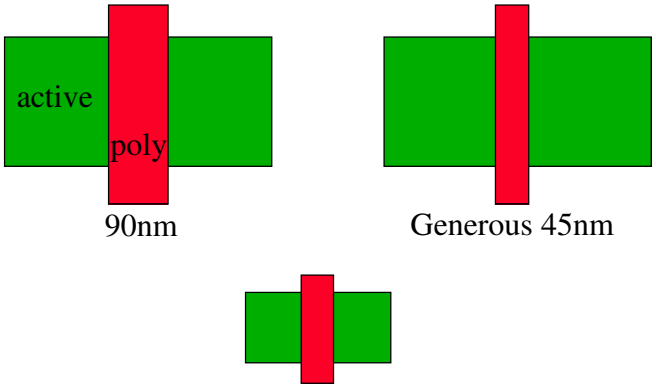
o Resolution limit of Canon i-line stepper ~ 0.5 μm

o 1250 Å of PR is etched off each side of 0.5 μm PR lines in O_2 plasma to make 0.25 μm lines

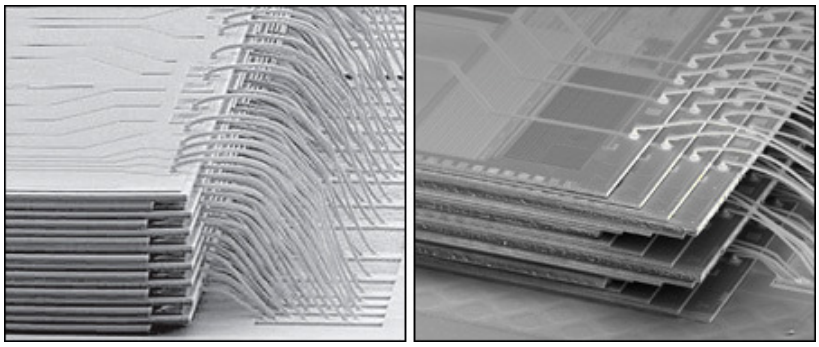
Recipe Parameters:
Power = 100 W
Pressure = 400 mTorr
O_2 = 20 sccm
Gap = 1.65 cm
Tool = LAM490

o PR Horizontal Etch Rate = 555 Å/min
o PR Vertical Etch Rate = 720 Å/min
o Anisotropy = (1-ER_H/ER_V) = 0.23

GENEROUS DESIGN RULES



ADVANCED PACKAGING



THROUGH WAFER VIAS

High Density Through Wafer Via Technology

Mr. Tomas Bauer

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Ph: +46 8 580 249 00, tomas.bauer@silexmicrosystems.com

ABSTRACT

The Through Silicon Via (TSV) process developed by Silex offers sub 50 µm pitch for through wafer connections in up to 600 µm thick substrates. Silex via process enables MEMS designs with significantly reduced die size and true "Wafer Level Packaging" - features that are particularly important in consumer market applications. The TSV technology also enables integration of advanced interconnect functions in optical MEMS, sensors and microfluidic devices. With several foundry customers using the process today and an extraordinary line-up of potential users, Silex aims at making the process a standard in the MEMS industry. The swift propagation of the technology will be facilitated by reasonable licensing agreements and technology transfer programs with customers and partners who may favor implementation in their existing manufacturing lines. This paper gives a brief introduction to the via formation process and focuses in more detail on the novel solutions made available by this enabling technology.

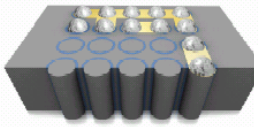


Figure 1: Schematic cross section of through wafer interconnect.

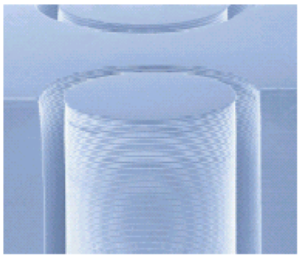
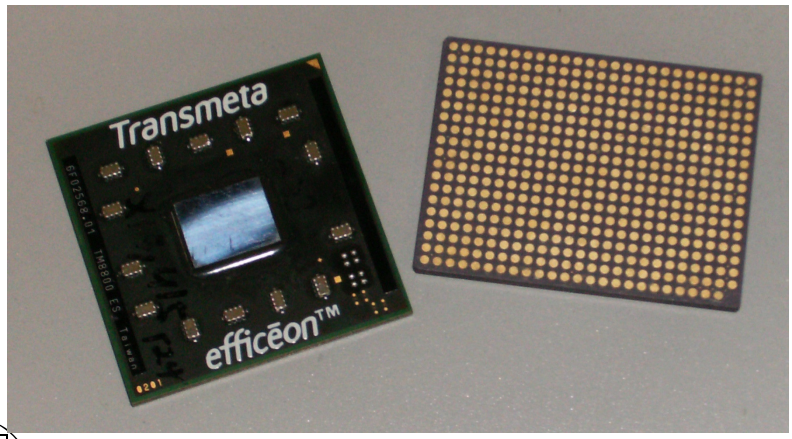


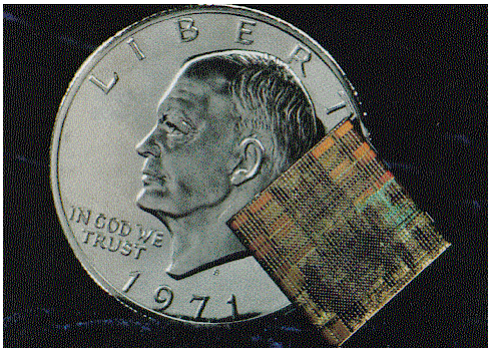
Figure 2: SEM picture of through wafer via "plug", formed using DRIE.

CHIP SCALE PACKAGE



C4 FLIP CHIP

Flip chip has the highest density of interconnects. Example: P2SC single-chip RISC 6000 processor has 2050 C4 bumps on 18x18 mm.



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8. UBM Tech Insights

REVIEW QUESTIONS

1. Explain why steep sub-threshold slope is good for transistors in IC's with millions of extremely small transistors?

2. Explain why mobility is lower in extremely small transistors?

3. What are the implications of lower mobility in extremely small transistors on overall integrated circuit performance?

4. What determines drive current? Why is it adversely affected in extremely small transistors? What can be done to improve drive current?