ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Advanced MOSFET Basics

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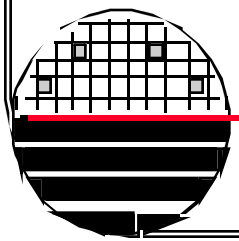
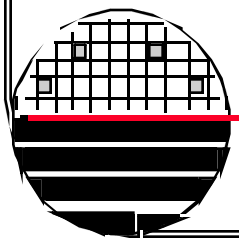


OUTLINE

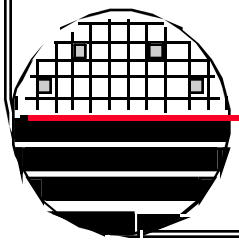
Introduction
Short Channel vs Long Channel
Effective Channel Length
Sub Threshold Effects
Low Doped Drain
NMOS with N+ Poly Gate
PMOS with N+ Poly Gate
PMOS with P+ Poly Gate
References



INTRODUCTION

The idea is to design a MOSFET that is as small as possible without short channel effects compromising the device performance much.

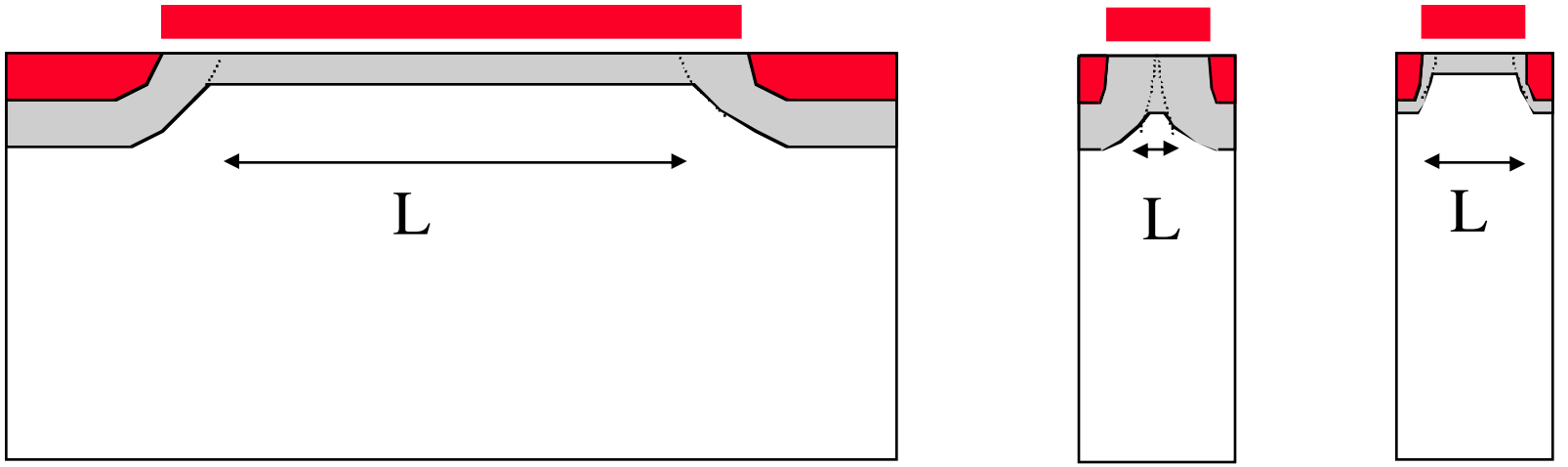
That is we want the smallest transistor possible that exhibits long channel characteristics.



SHORT CHANNEL MOSFET

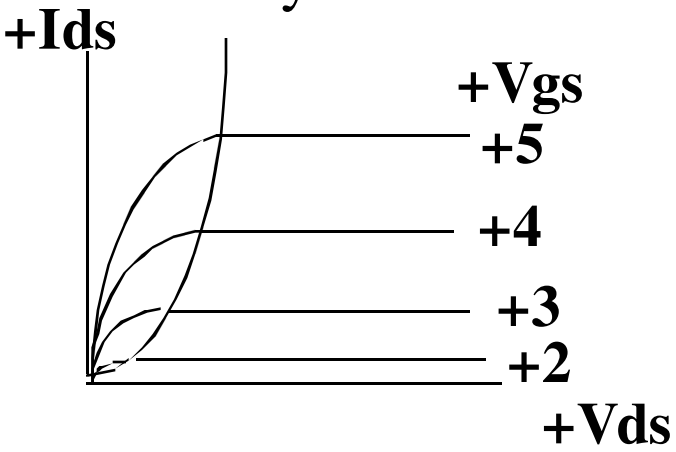
Long-channel MOSFET is defined as devices with width and length long enough so that edge effects from the four sides can be neglected

Channel length L must be much greater than the sum of the drain and source depletion widths

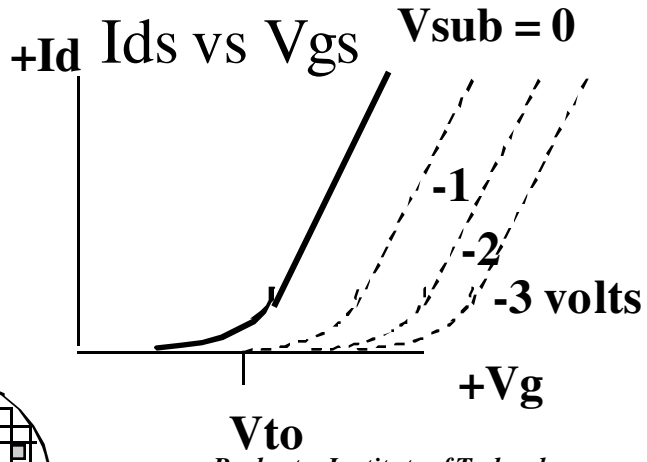


LONG CHANNEL MOSFET I-V CHARACTERISTICS

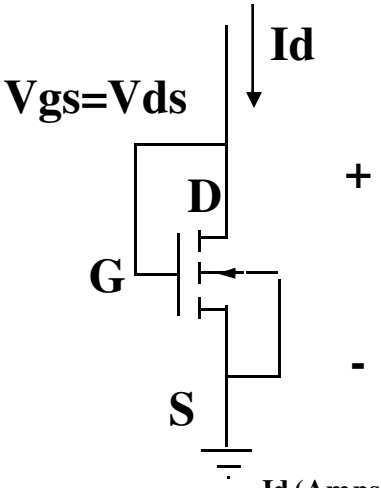
Family of Curves



Ids vs Vgs

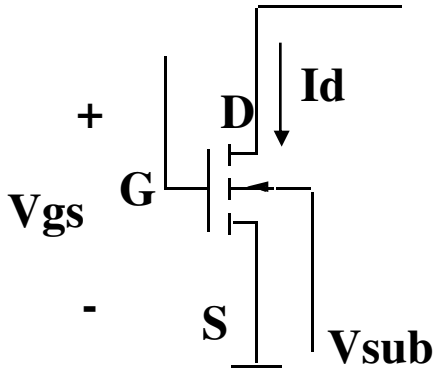


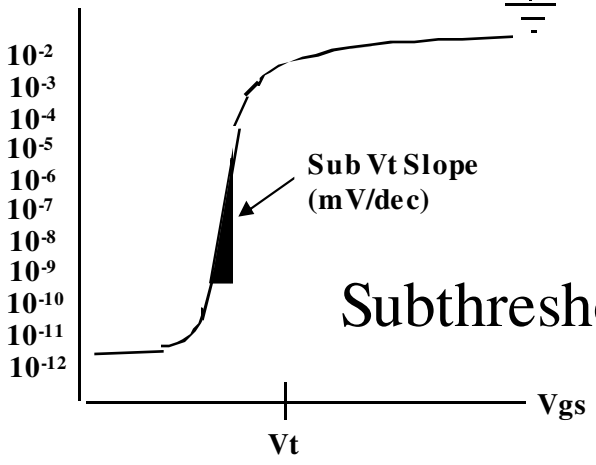
Saturation Region



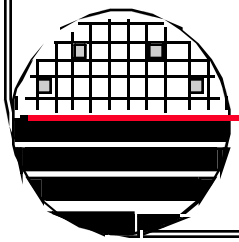
Non Saturation Region

Vd = 0.1 Volt





Subthreshold



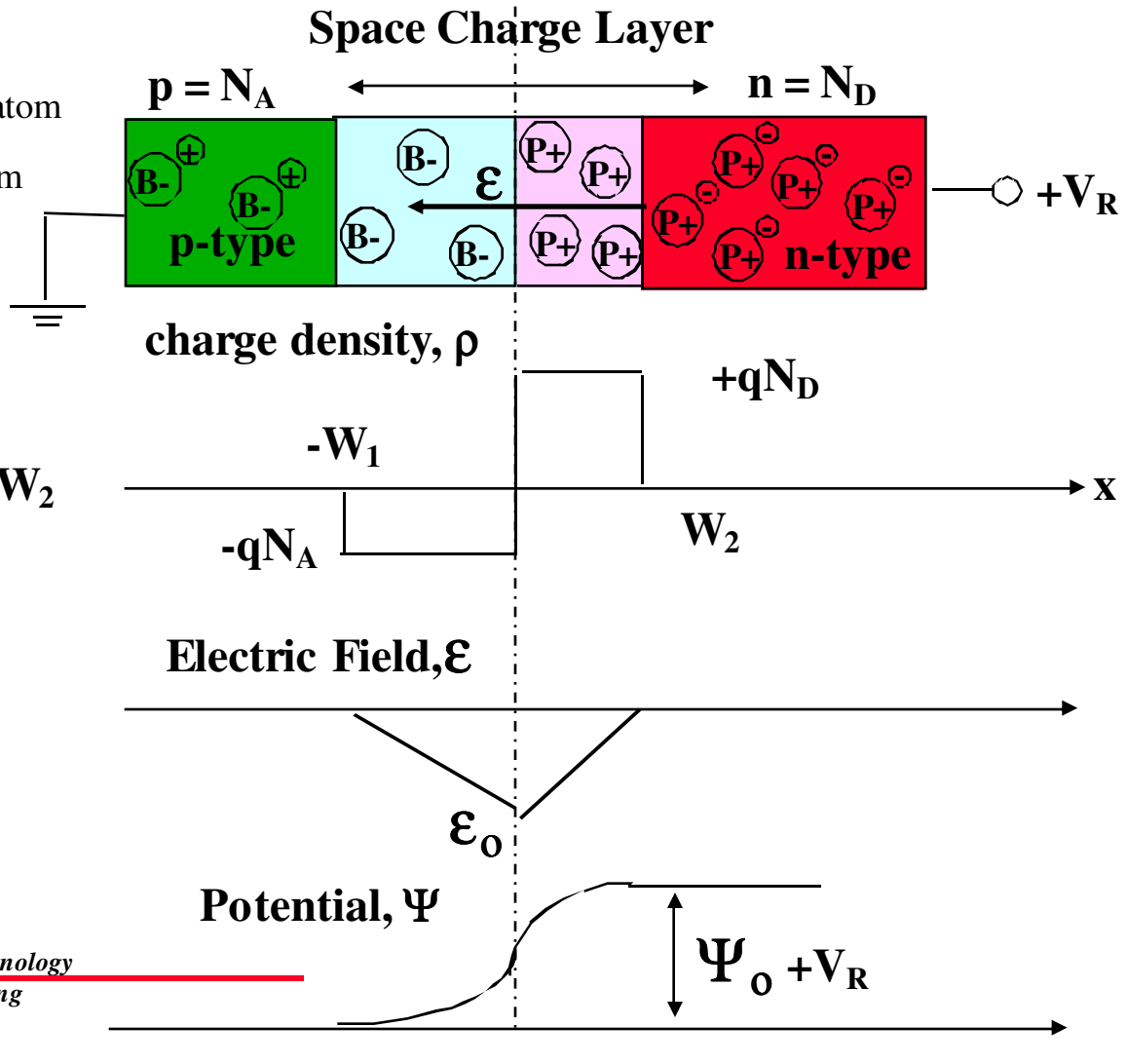
UNIFORMLY DOPED PN JUNCTION

P+ Phosphrous donor atom and electron

P+ Ionized Immobile Phosphrous donor atom

B- Ionized Immobile Boron acceptor atom

B- Boron acceptor atom and hole



UNIFORMLY DOPED PN JUNCTION

Built in Voltage: $\Psi_o = KT/q \ \ln (N_A N_D/ni^2)$

$ni = 1.45E10\ cm^{-3}$

Width of Space Charge Layer, W: with reverse bias of V_R volts

$$W = (W_1 + W_2) = [(2\varepsilon/q)(\Psi_o + V_R)(1/N_A + 1/N_D)]^{1/2}$$

W_1 width on p-side $\qquad$ W_2 width on n-side

$W_1 = W\,[N_D/(N_A + N_D)] \qquad W_2 = W\,[N_A/(N_A + N_D)]$

Maximum Electric Field:

$$E_o = -\,[(2q/\varepsilon)(\Psi_o + V_R)(N_A N_D/(N_A + N_D))]^{1/2}$$

Junction Capacitance per unit area:

$$C_j' = \varepsilon_o \varepsilon_r / W = \varepsilon_o \varepsilon_r / [(2\varepsilon/q)(\Psi_o + V_R)(1/N_A + 1/N_D)]^{1/2}$$

$\varepsilon = \varepsilon_o \varepsilon_r = 8.85E^{-12}\ (11.7)\ F/m$

$= 8.85E^{-14}\ (11.7)\ F/cm$

EXAMPLE CALCULATIONS

ROCHESTER INSTITUTE OF TECHNOLOGY — PN.XLS
MICROELECTRONIC ENGINEERING — 4/21/2011

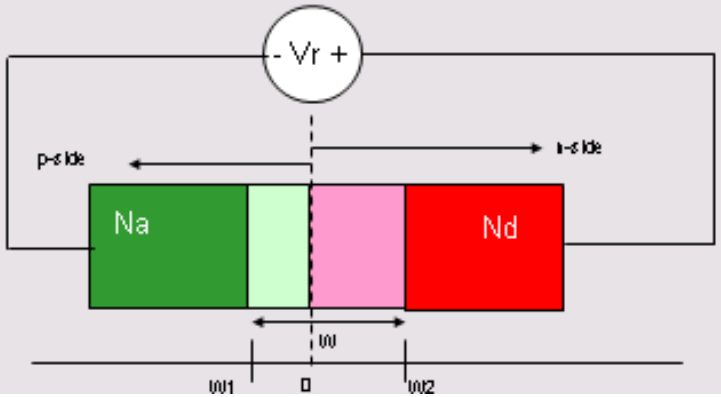
CALCULATIONS FOR PN JUNCTION (ELECTROSTATICS) — DR. LYNN FULLER

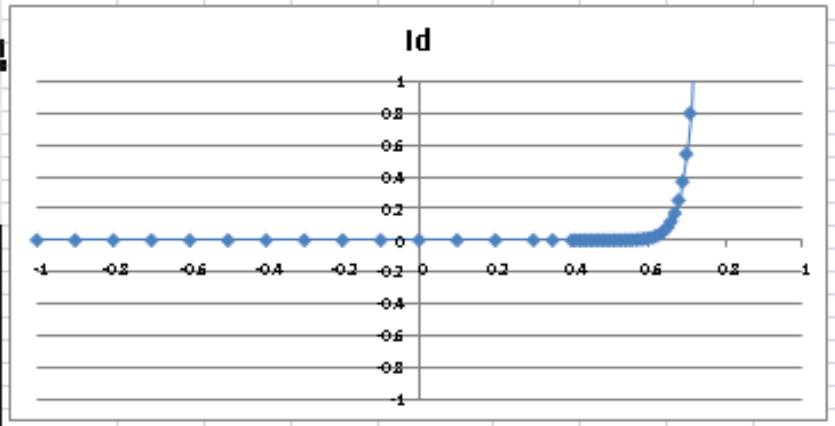
To use this spreadsheet change the values in the white boxes. The rest of the sheet is protected and should not be changed unless you are sure of the consequences. The calculated results are shown in the purple boxes.

CONSTANTS			VARIABLES			
K	1.38E-23	J/K				
q	1.60E-19	Coul	Temp=	300	°K	
Ego	1.12	eV				
zo	8.85E-14	F/cm	Nd =	1.00E+16	cm-3	
zr	11.7		Na =	5.00E+17	cm-3	
ni	1.45E+10	cm-3				
Breakdown E:	3.00E+05	V/cm	Vr =	30	Volts	Reverse Bias Voltage
Exceeds Emax !!!						

CALCULATIONS:

Eg = Ego - (aT^2/(T+B)	1.075	eV
ni^2 = A T^3 e^(-Eg/KT/q)	9.84E+20	cm-6
KT/q =	0.0259	Volts
Vbi = (KT/q) ln (NaNd/ni2)	0.76	Volts
W = [(2zr/q)(Vbi+Vr)(1/Na +1/Nd)]^0.5	2.02	µm
W1 =W[Nd/(Na+Nd)]	0.04	µm
W2 =W[Na/(Na+Nd)]	1.98	µm
Eo = -[(2q/eoer)(Vbi+Va)(NaNd/(Na+Nd)]^0.5	-3.05E+05	V/cm
Cj' = eoer/W	5.14E-09	F/cm2





$Id = Is\ (e^{qV/KT} - 1)$

$Is = CT^{\gamma} \exp^{[-qEg/KT]}$

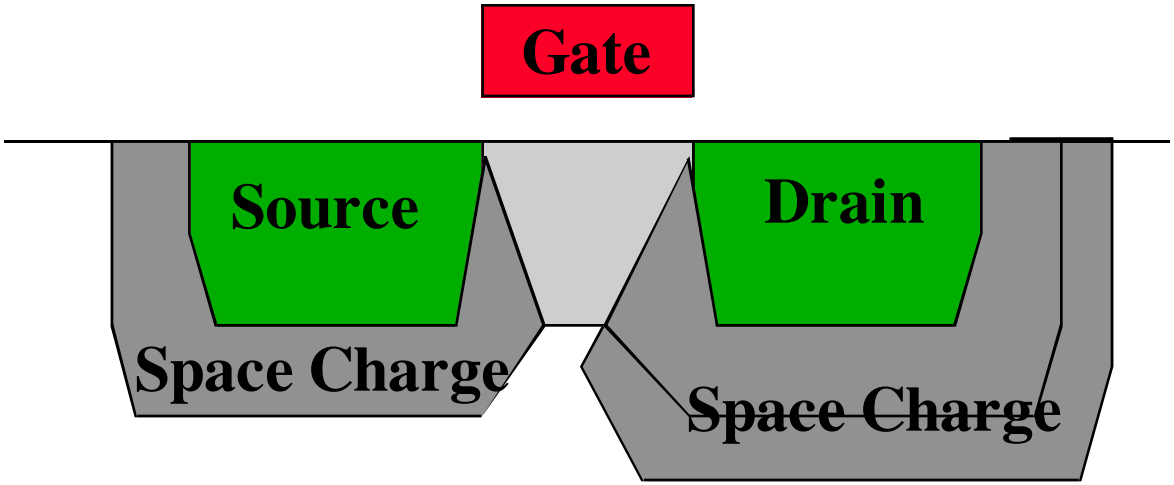
Is = 9.73E-13

V	Id
-1	-9.73E-13
-0.9	-9.73E-13
-0.8	-9.73E-13
-0.7	-9.73E-13
-0.6	-9.73E-13
-0.5	-9.73E-13
-0.4	-9.73E-13
-0.3	-9.73E-13
-0.2	-9.72E-13
-0.1	-9.52E-13
0	0
0.1	4.533E-11
0.2	2.203E-09
0.3	1.049E-07
0.35	7.24E-07
0.4	4.995E-06
0.41	7.35E-06
0.42	1.082E-05
0.43	1.592E-05
0.44	2.342E-05
0.45	3.446E-05
0.46	5.071E-05
0.47	7.462E-05
0.48	0.0001098
0.49	0.0001616
0.5	0.0002378

THE SHORT CHANNEL MOSFET

Sort channel MOSFET is defined as devices with width and length short enough such that the edge effects can not be neglected.

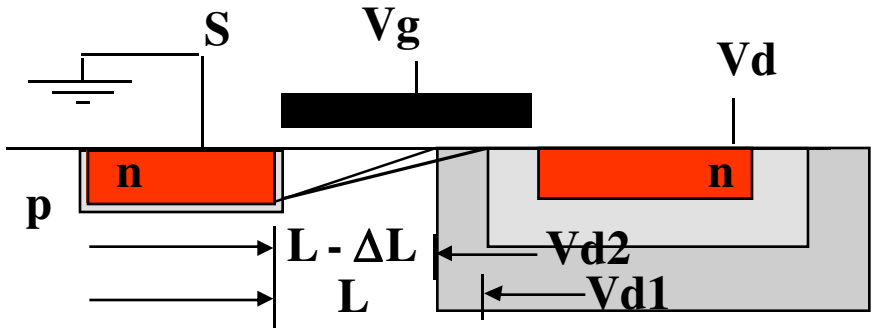
Channel length L is comparable to the depletion widths associated with the drain and source.

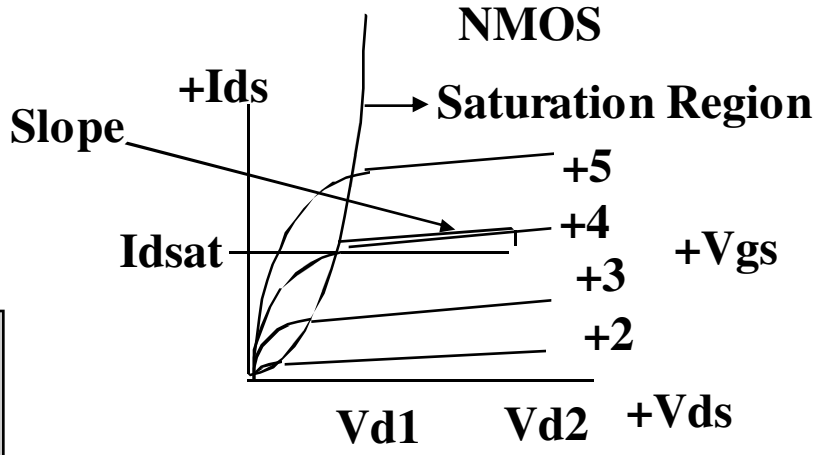


CHANNEL LENGTH MODULATION

Channel Length Modulation Parameter λ

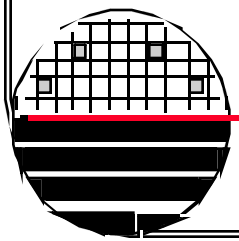
λ = Slope/ Idsat





$$I_{Dsat} = \frac{\mu W\, Cox'}{2L}(Vg-Vt)^2 (1+ \lambda Vds)$$

NMOS Transistor in Saturation Region DC Model, λ is the channel length modulation parameter and is different for each channel length, L. Typical value might be 0.02



TERADA-MUTA METHOD FOR EXTRACTING Leff and Rds

Terada-Muta Method for Leff and Rds

In the linear region (V_D is small):

$$I_D = \frac{\mu W\ Cox'\ (Vgs - Vt - V_d/2)}{Leff}\ V_D$$

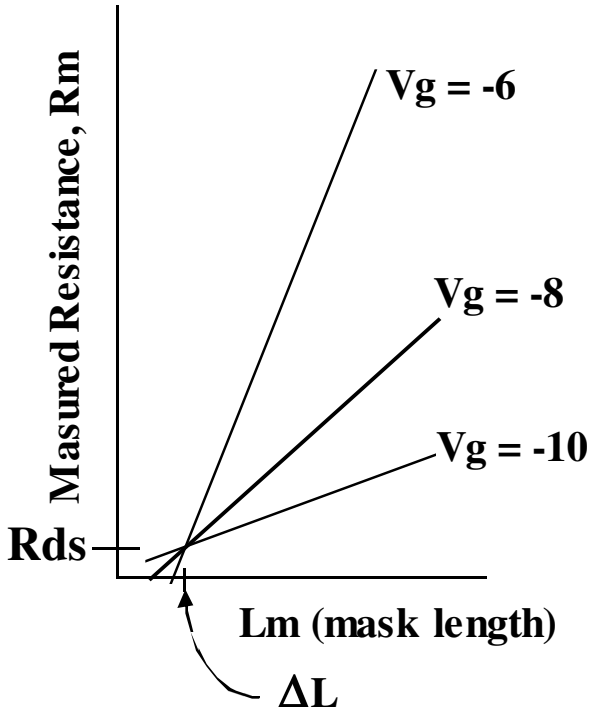
($V_d/2 \to 0$)

$1/Rm$

$$I_D = 1/R_m\ V_D$$

Leff = Lm - ΔL

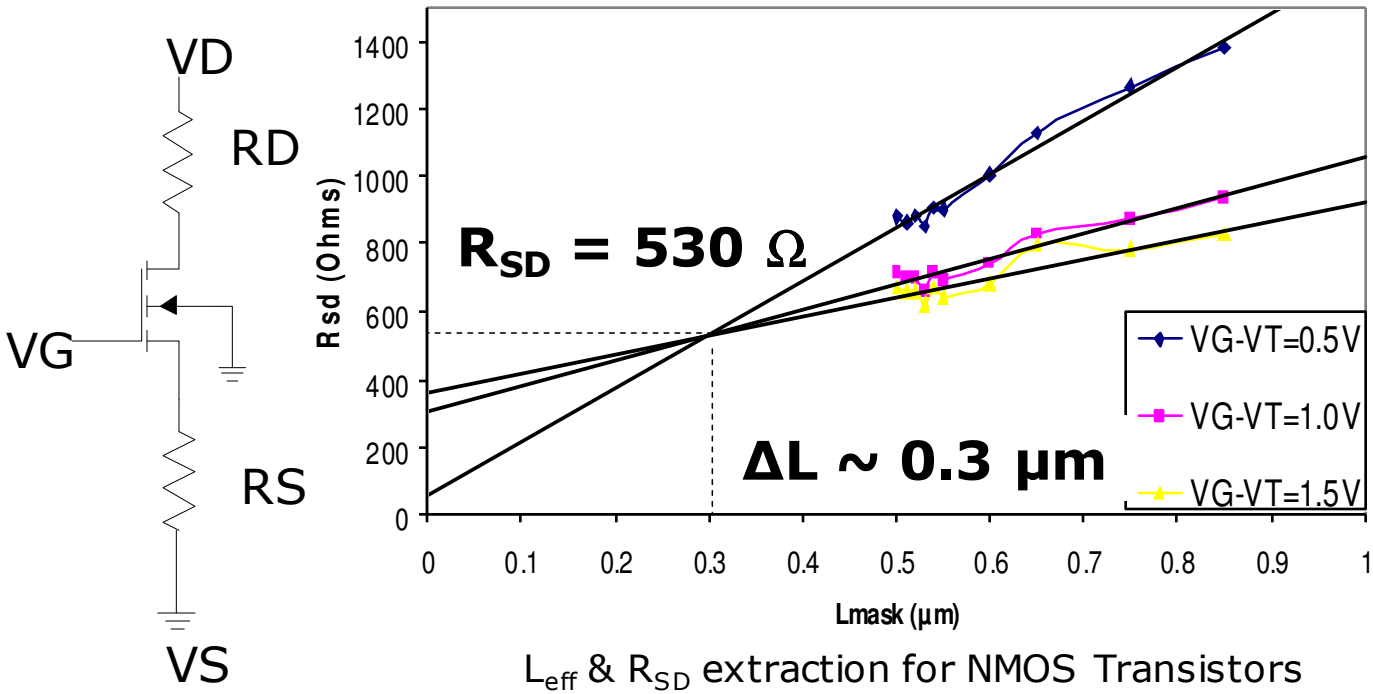
where ΔL is correction due to processing
Lm is the mask length



Rm = V_D/I_D = measured resistance
= Rds + (Lm - ΔL)/ μW Cox' (Vgs-Vt)

so measure Rm for different channel length transistors and plot Rm vs Lm
where Rm = intersect find value for ΔL and Rds
Then Leff can be calculated for each different length transistor
from Leff = Lm - ΔL

TERADA-MUTA METHOD FOR EXTRACTING Leff and Rds



$L_{eff} = L_{mask} - \Delta L$
$L_{eff} = 0.5\ \mu m - 0.3\ \mu m$
$L_{eff} = 0.2\ \mu m$

L_{eff} & R_{SD} extraction for NMOS Transistors

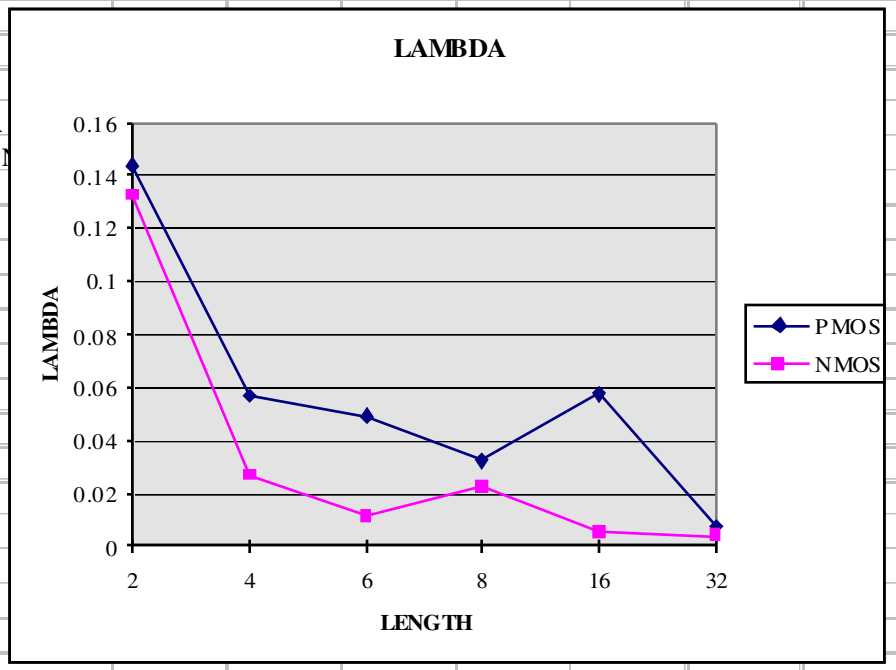
Linear Region:
$V_D = 0.1V$
$V_G - V_T >> I_D R_{SD}$
At low I_D, V_{RSD} small

$$Rm = \frac{Vd}{Id} = R_{SD} + \frac{(L_{mask} - \Delta L)}{\mu Cox'W(V_{GS} - V_t)}$$

Plot R_m vs. L_{mask} for different $(V_{GS} - V_t)$

LAMBDA VERSUS CHANNEL LENGTH

µA UNIT	SLOPE	IDSAT	W	L	LAMBDA PMOS
205	4.9	6.8	32	2	0.144118
71	2	7.1	32	4	0.056338
56	1.8	7.3	32	6	0.049315
34	1.2	7.5	32	8	0.032
21	2	7	32	16	0.057143
8.8	0.3	7.6	32	32	0.007895
415	4.3	6.5	32	2	0.132308
137	0.95	7.1	32	4	0.026761
91	0.4	7	32	6	0.011429
137	0.8	7.2	32	8	0.022222
27	0.2	7.2	32	16	0.005556
15	0.15	7.15	32	32	0.004196

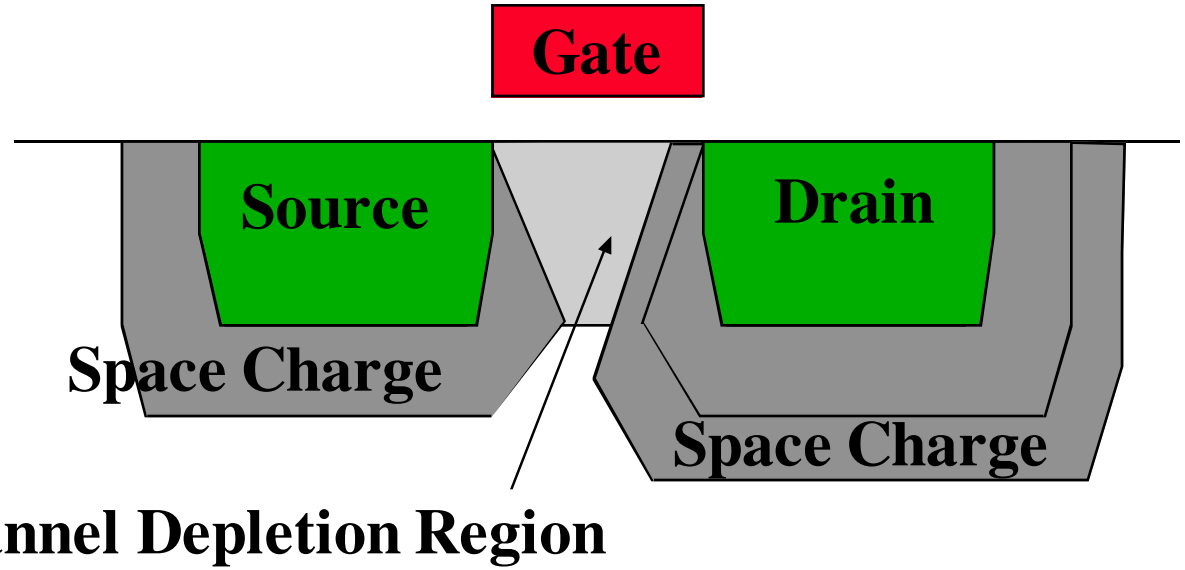


Some MOSFET models use lambda but you would need a different lambda for each different length transistor. More advanced models use and equation to find a lambda as a function of the length Leff

SHORT CHANNEL VT ROLL OFF

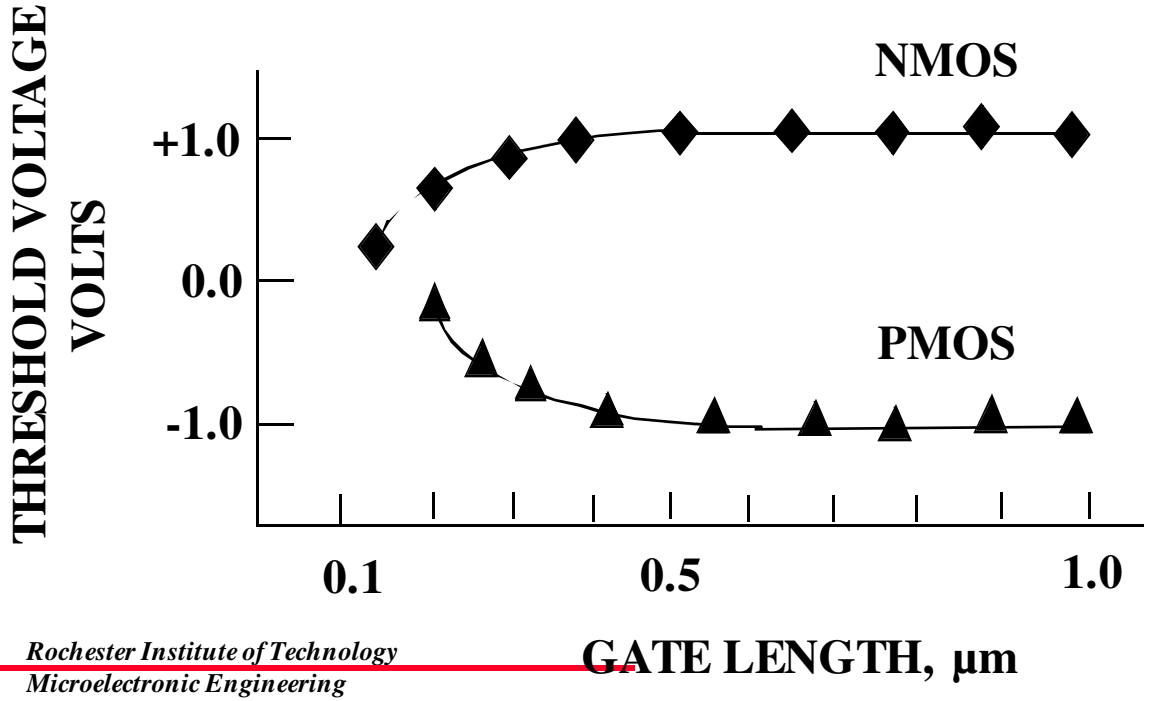
As the channel length decreases the channel depletion region becomes smaller and the Vt needed to turn on the channel appears to decrease.

A similar effect occurs for increasing V_{DS} which causes an increase in the drain space charge layer. Called drain induced barrier lowering or DIBL



THRESHOLD VOLTAGE ROLL OFF

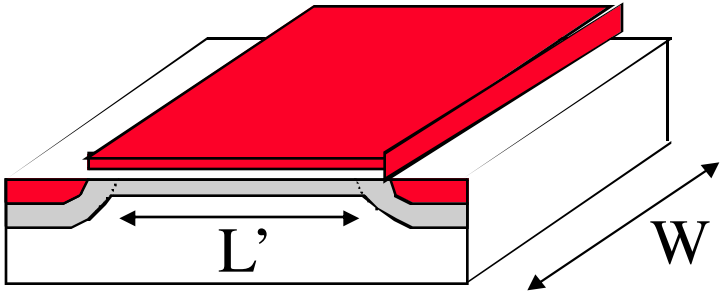
A Test Chip is used that includes nMOS and pMOS transistors of various lengths from 0.1 µm to 5.0 µm and the threshold voltage is plotted versus channel length. The threshold voltage needs to be high enough so that when the input is zero or +Vsupply the transistor current is many decades lower than when it is on. Vt and sub-Vt slope interact.

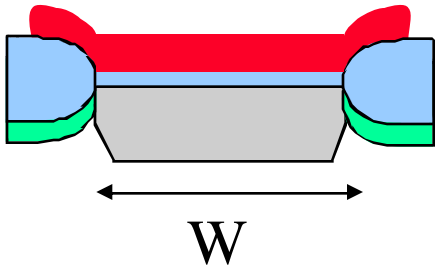


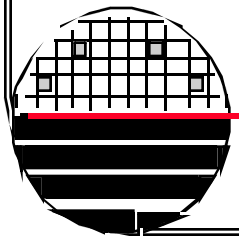
NARROW GATE WIDTH EFFECTS

Fringing field causes channel depletion region to extend beyond the gate in the width direction Thus additional gate charge is required causing an apparent increase in threshold voltage. In wide channel devices this can be neglected but as the channel becomes smaller it is more important

In NMOS devices encroachment of the channel stop impurity atoms under the gate edges causing the edges to be heavier doped requiring more charge on the gate to turn on the entire channel width. In PMOSFETs the phosphorous pile up at the surface under the field region causes a similar apparent increase in doping at the edges of the channel width



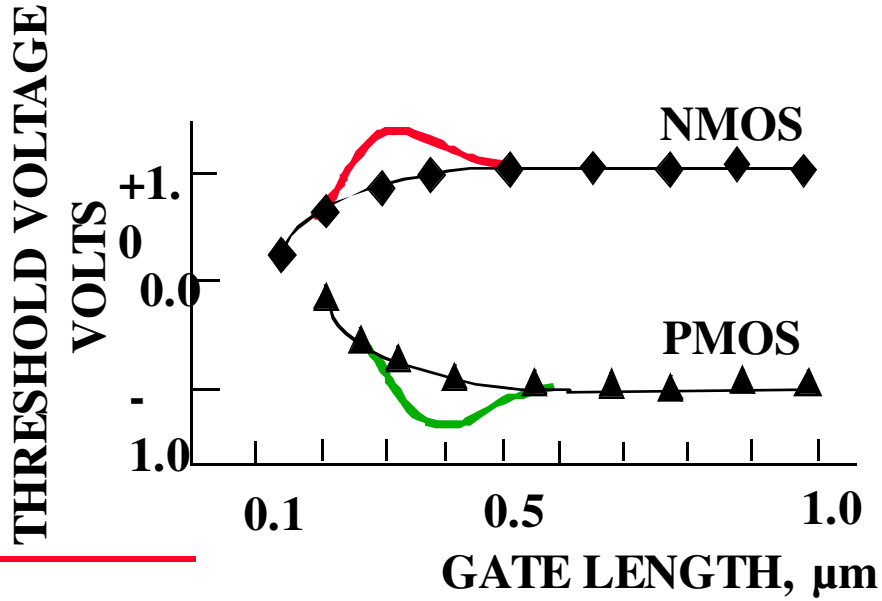


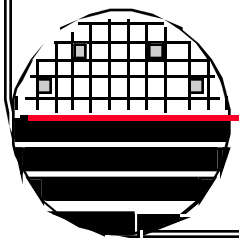


REVERSE THRESHOLD VOLTAGE ROLLOFF

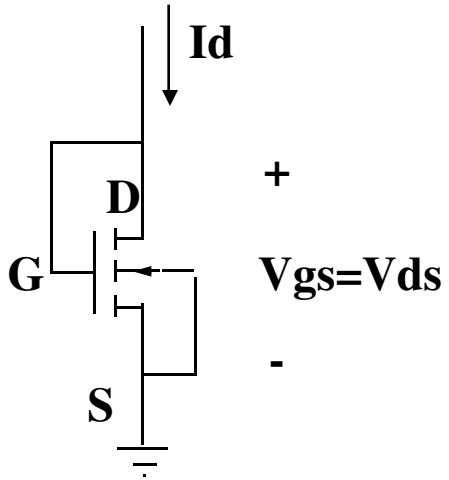
Vt initially increases with decrease in channel length then decreases. This is caused by various effects that result in lateral dopant nonuniformity in the channel.

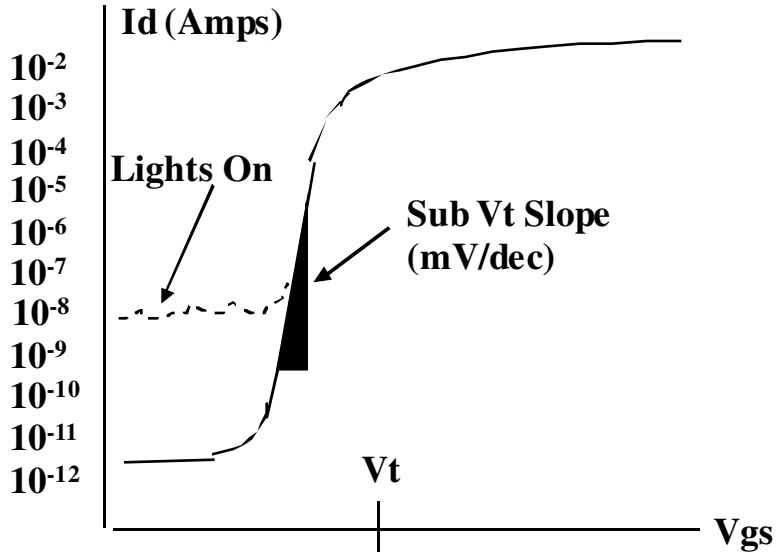
Example: Oxidation Enhanced Diffusion or enhanced diffusion due to implant damage causing the dopant concentration to be higher in the channel near the drain and source edges of the poly gate.



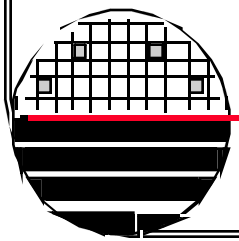


SUBTHRESHOLD CHARACTERISTIC

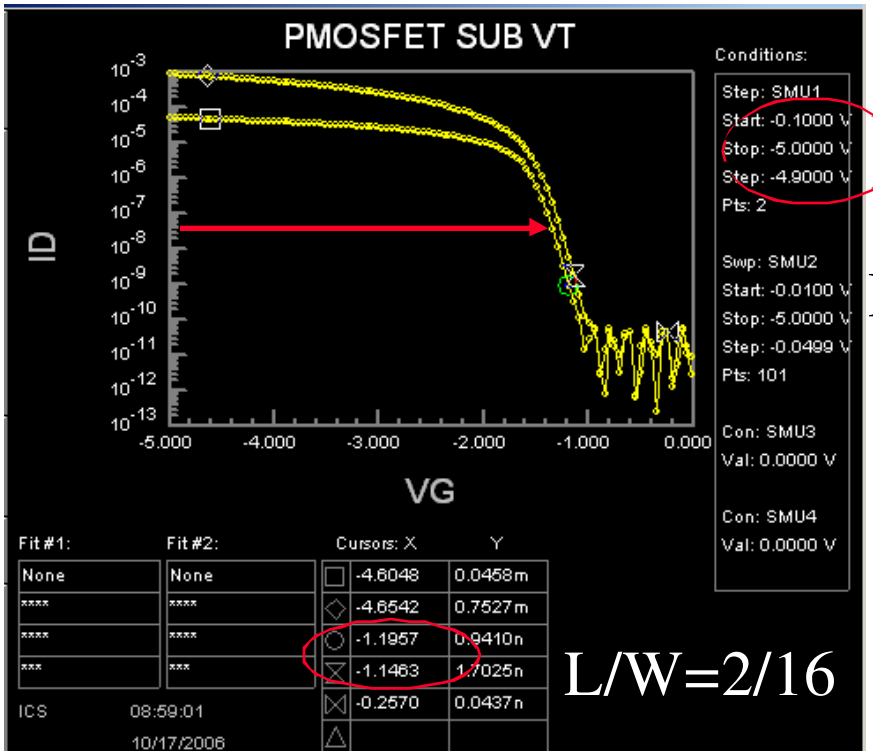




The subthreshold characteristics are important in VLSI circuits because when the transistors are off they should not carry much current since there are so many transistors. (typical value about 100 mV/decade). Thinner gate oxide makes subthreshold slope larger. Surface channel has larger slope than buried channel.



DRAIN INDUCED BARRIER LOWERING

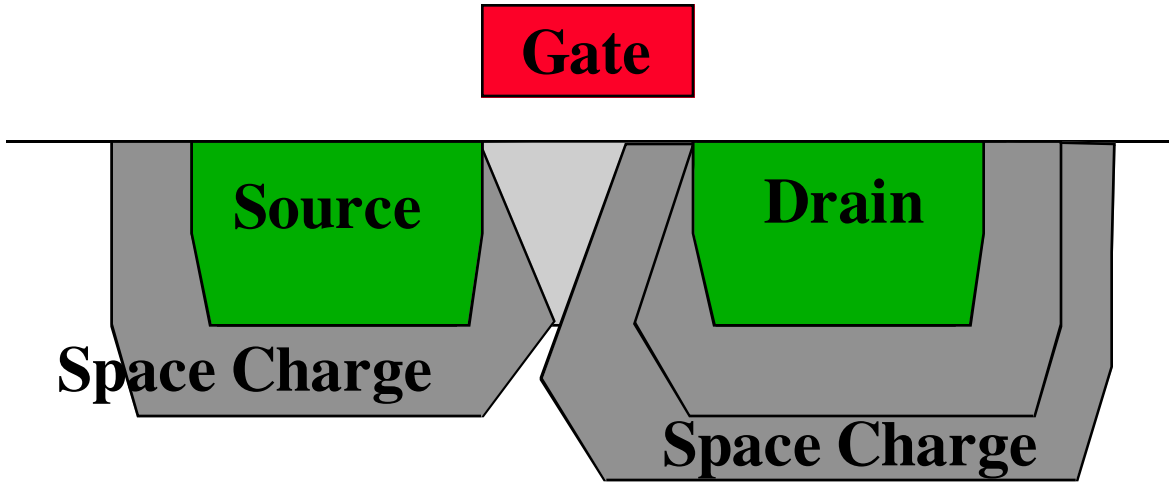


L/W=2/16

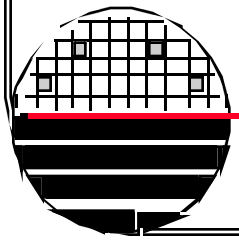
DIBL = change in VG /change in VD
at ID=1E-9 amps/µm
or 1.6E-8 amps for this
size transistor

= ~ (1.1957-1.1463)/(5-0.1)
= ~ 10mV/V

PUNCHTHROUGH



As the voltage on the drain increases the space charge associated with the drain pn junction increases. Current flow through the transistor increases as the source and drain space charge layers approach each other. The first indication is an increase in the sub threshold current and a decrease in the the subthreshold slope.



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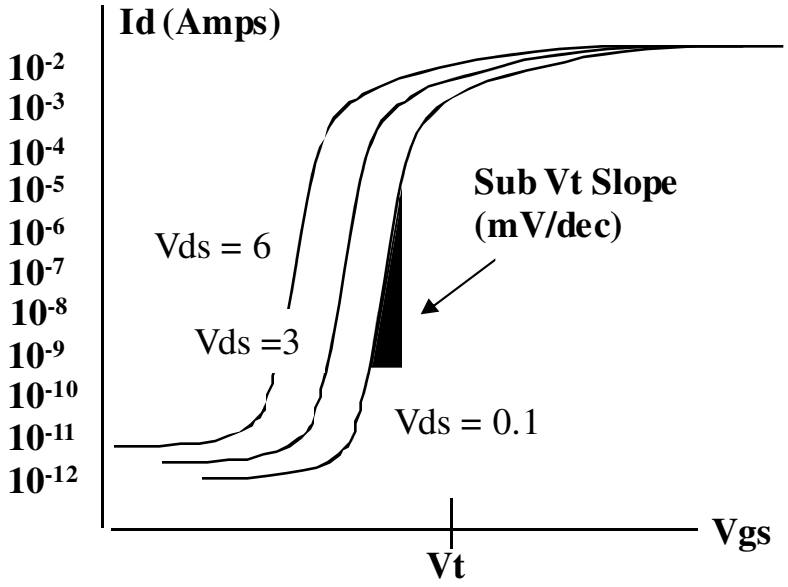
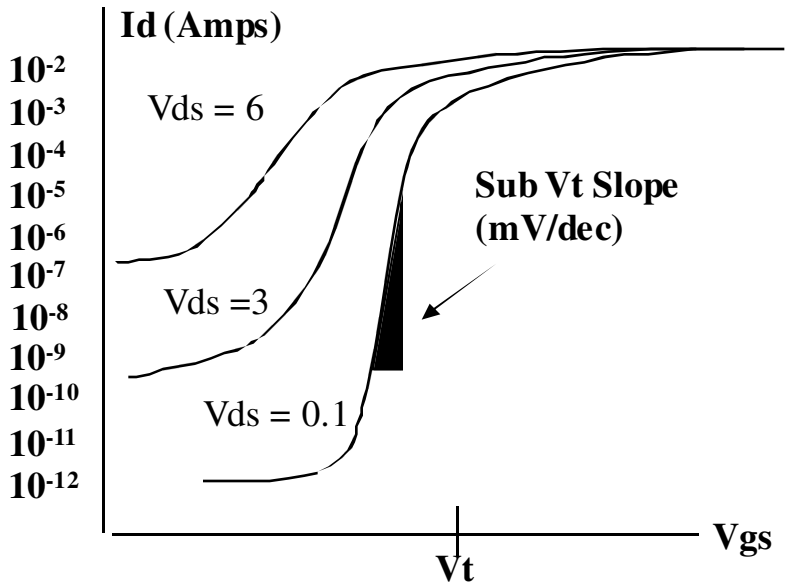
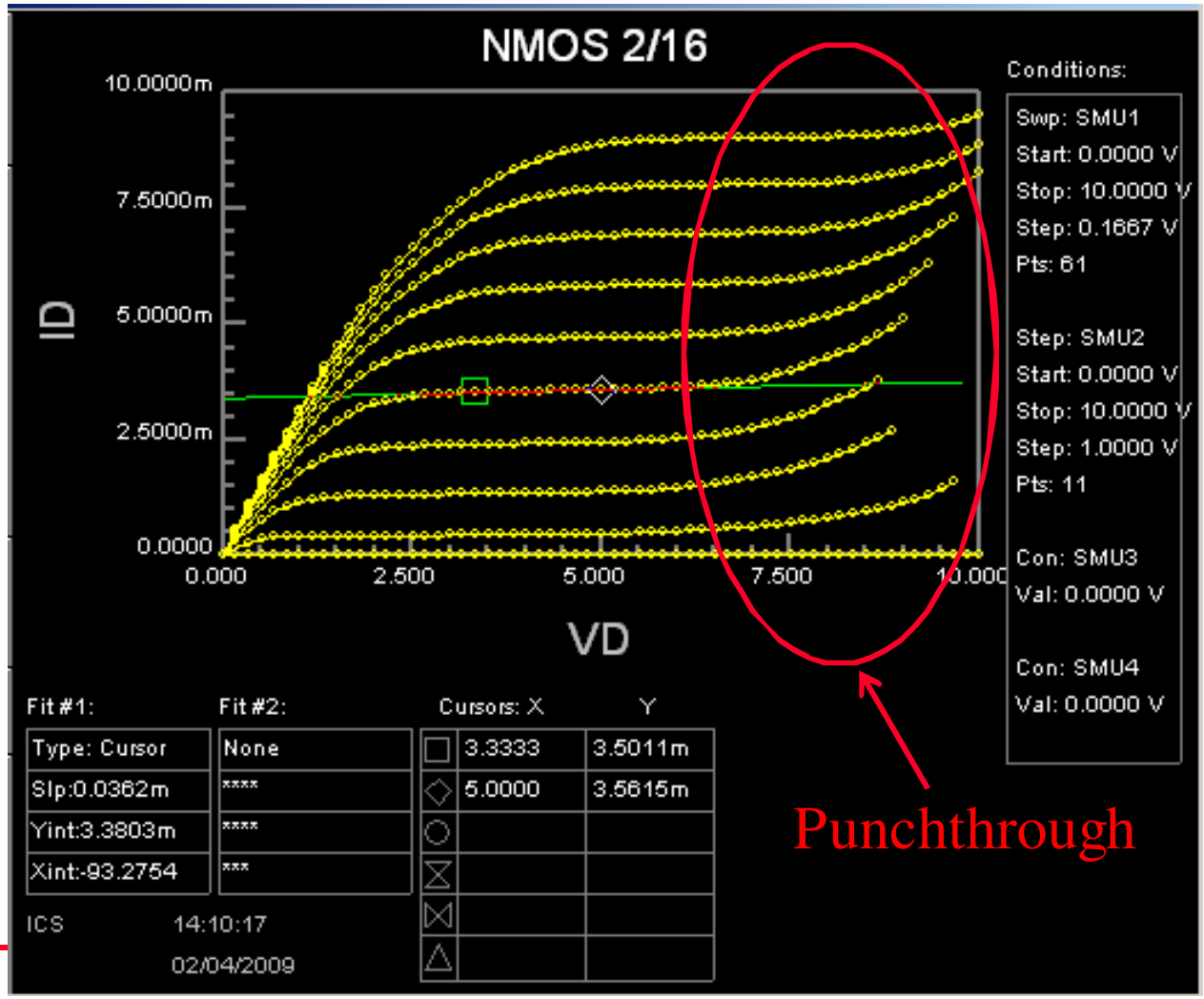


Long channel behavior

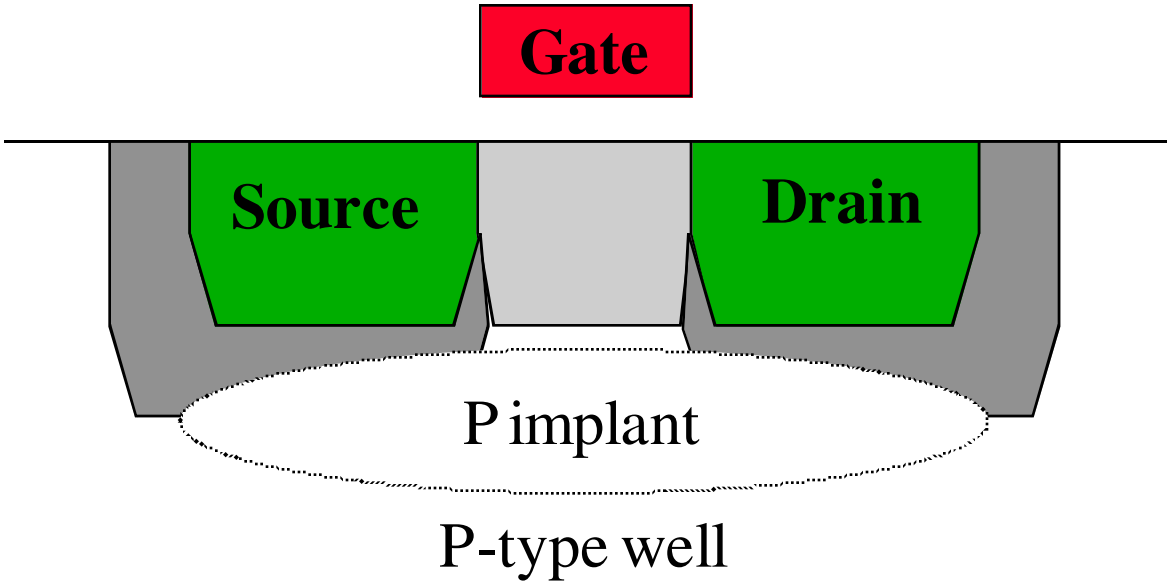


Short channel behavior
Punchthrough

MEASURED Id-Vds Family



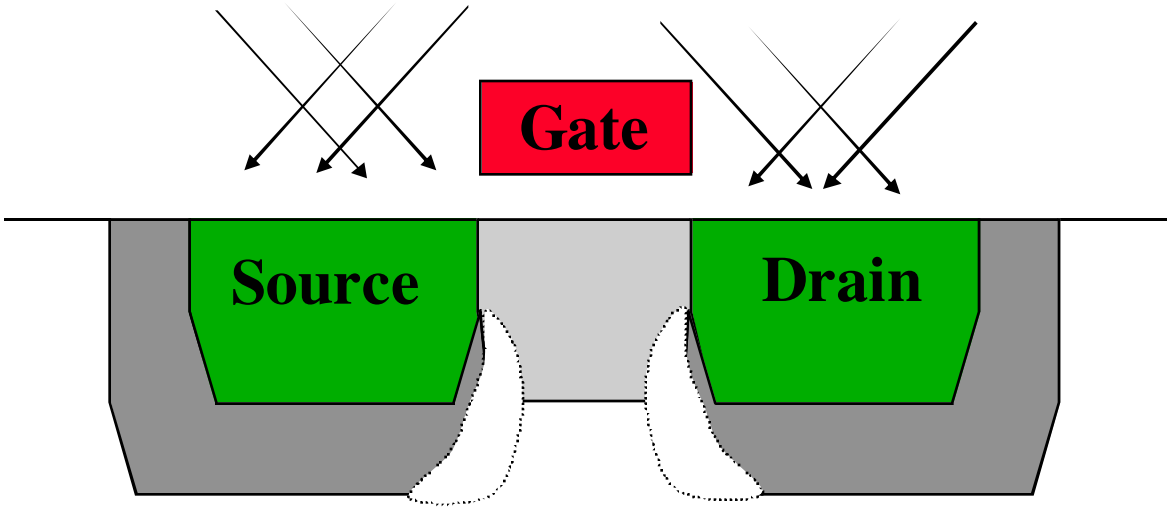
PUNCHTHROUGH IMPLANT



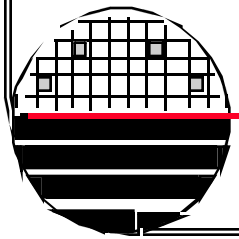
Punch through implant increases the well doping below the drain and source depth making the space charge layer smaller.

PUNCHTHROUGH HALO IMPLANT

Boron Implant at High Angle



P-type well



RETROGRADE WELL TO REDUCE PUNCHTHROUGH

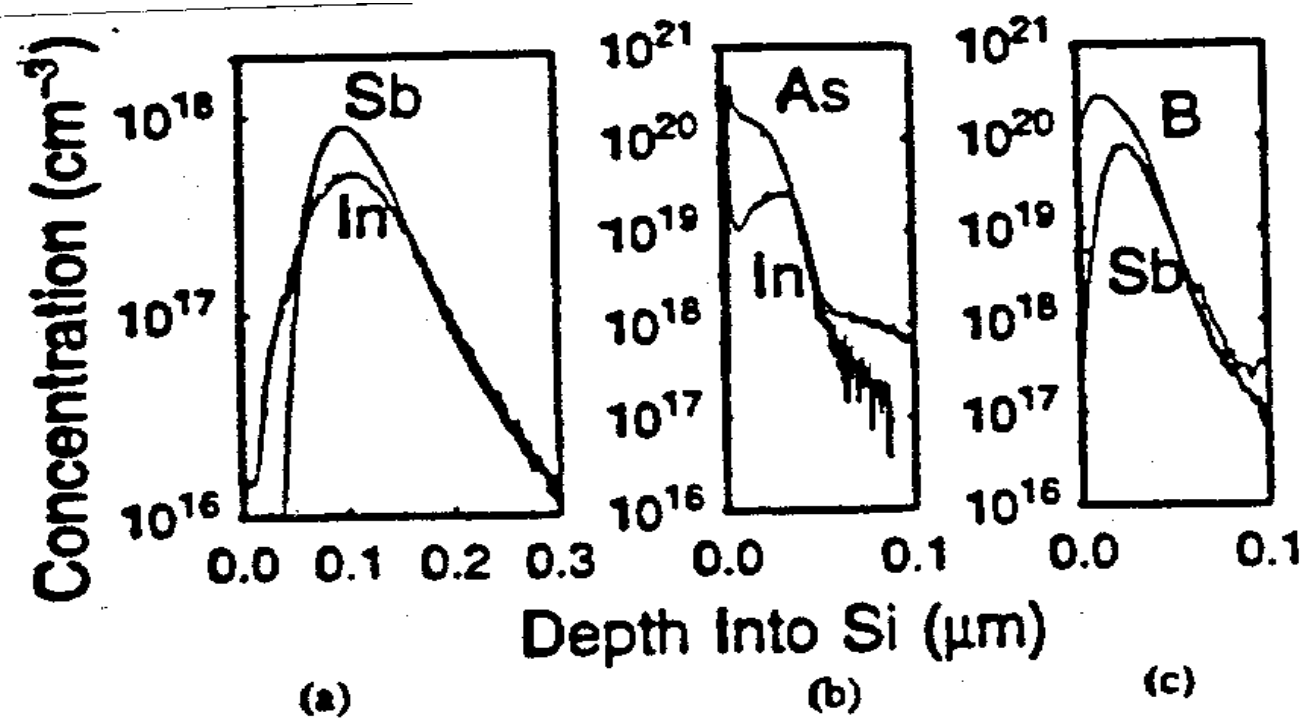


Fig. 1. SIMS measurement of the channel implant for nMOS and pMOS (a), and the source-drain extension/halo profiles for nMOS (b) and pMOS (c).

WHY THE D/S NEEDS TO BE SHALLOW

Sketch the three space charge layers

The Channel Space Charge

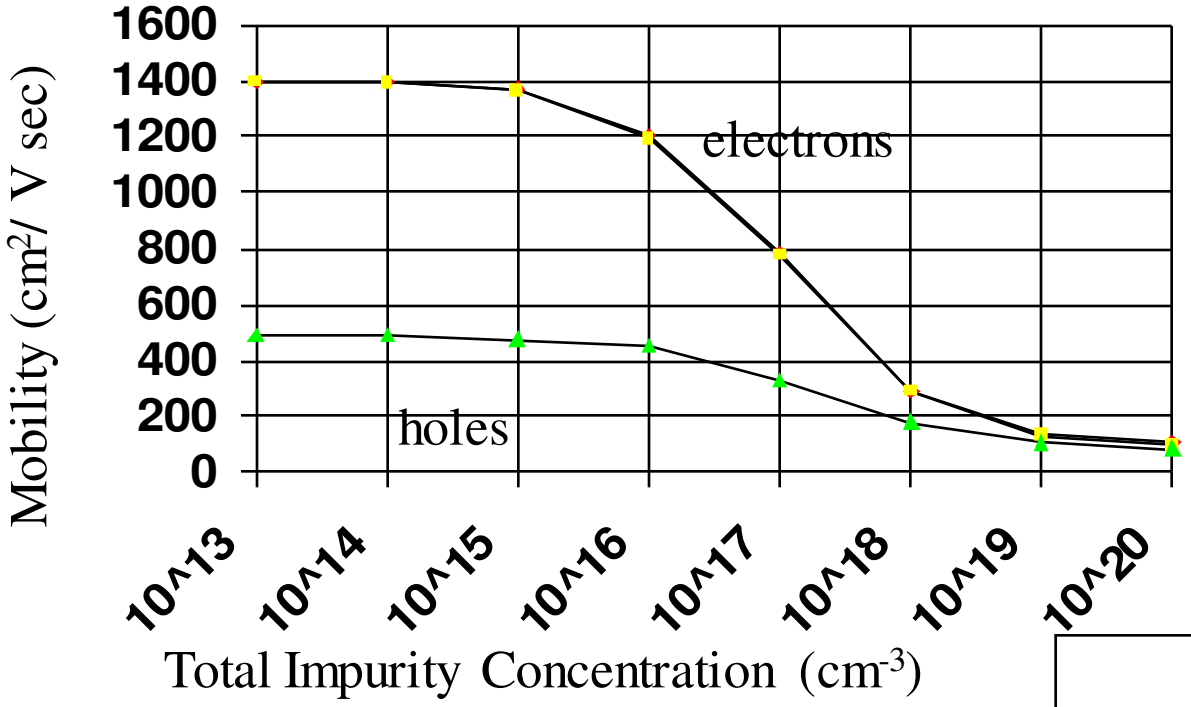
The Drain Space Charge

The Source Space Charge

Look at Punchthrough

Punchthrough will occur at lower drain voltages in the device with deeper D/S

MOBILITY



Electron and hole mobilities in silicon at 300 K as functions of the total dopant concentration (N). The values plotted are the results of the curve fitting measurements from several sources. The mobility curves can be generated using the equation below with the parameters shown:

$$\mu(N) = \mu_{mi} + \frac{(\mu_{max} - \mu_{min})}{\{1 + (N/N_{ref})^{\alpha}\}}$$

From Muller and Kamins, 3rd Ed., pg 33

Parameter	Arsenic	Phosphorous	Boron
μ_{min}	52.2	68.5	44.9
μ_{max}	1417	1414	470.5
N_{ref}	9.68X10^16	9.20X10^16	2.23X10^17
α	0.680	0.711	0.719

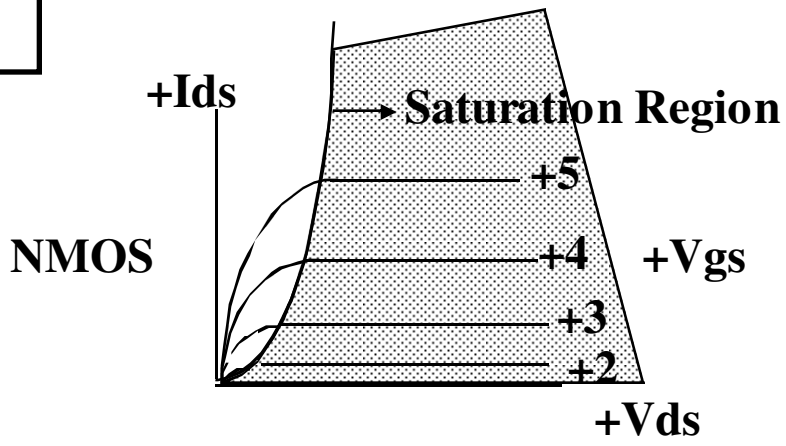
CURRENT DRIVE - MOBILITY

$$I_D = \frac{\mu W\, Cox'}{L}(Vg - Vt - V_d/2)V_d$$

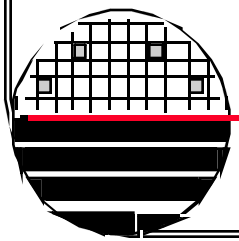
Non Saturation Region

$$I_{Dsat} = \frac{\mu W\, Cox'}{2L}(Vg - Vt)^2$$

Saturation Region

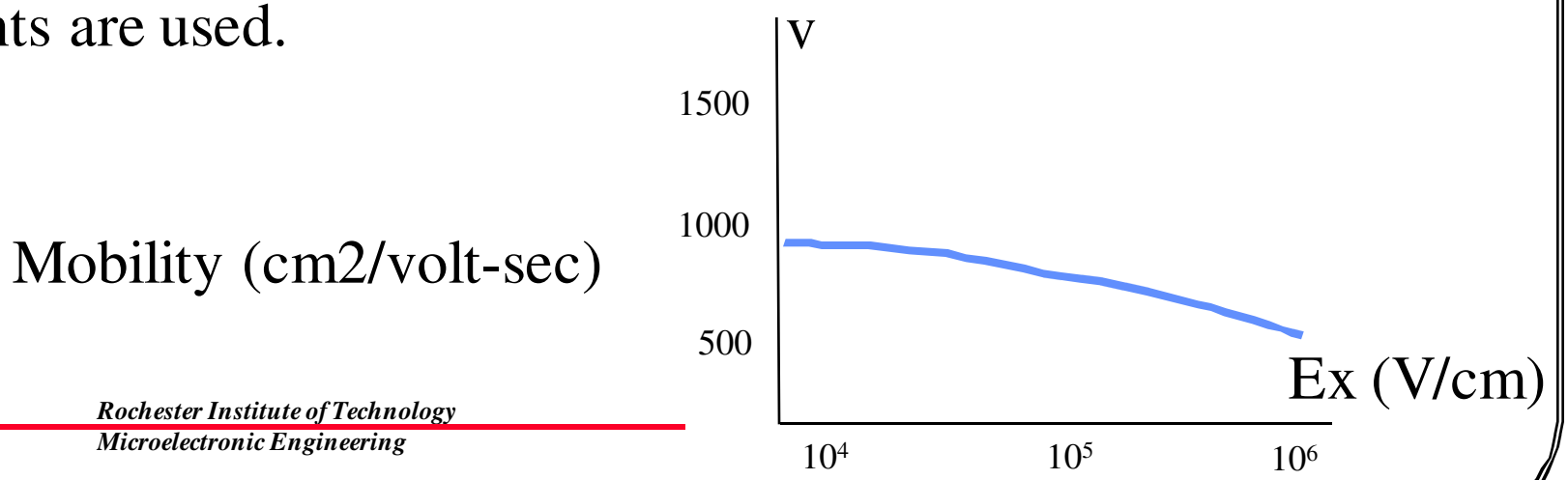


Mobility decreases with increase in doping concentration

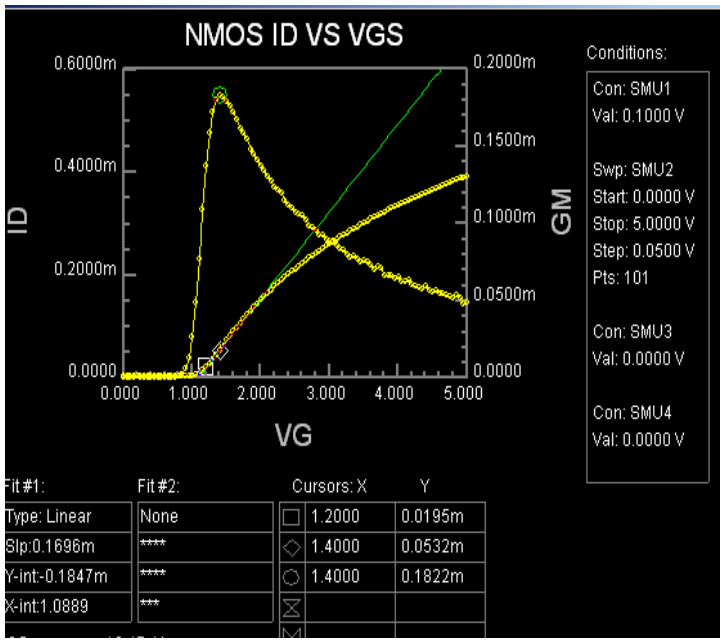


MOBILITY DEGRADATION

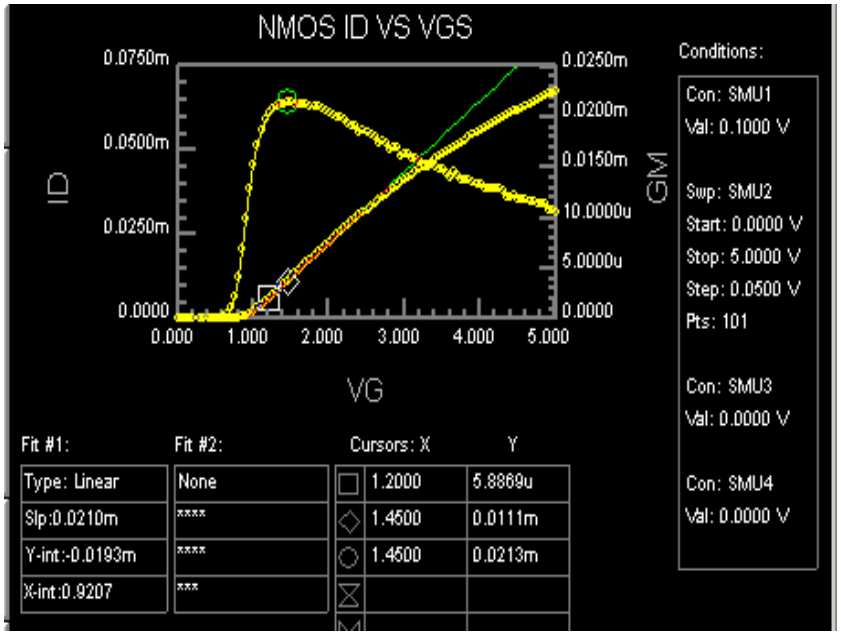
In a MOSFET the mobility is lower than the bulk mobility because of the scattering with the Si-SiO2 interface. The vertical electric field causes the carriers to keep bumping into the interface causing the mobility to degrade. The electric fields can be 1E5 or 1E6 V/cm and at that level the collisions with the interface reduce the mobility even more. The vertical electrical field is higher for heavier doped substrates and when Vt adjust implants are used.



MOBILITY DEGRADATION



short channel



long channel

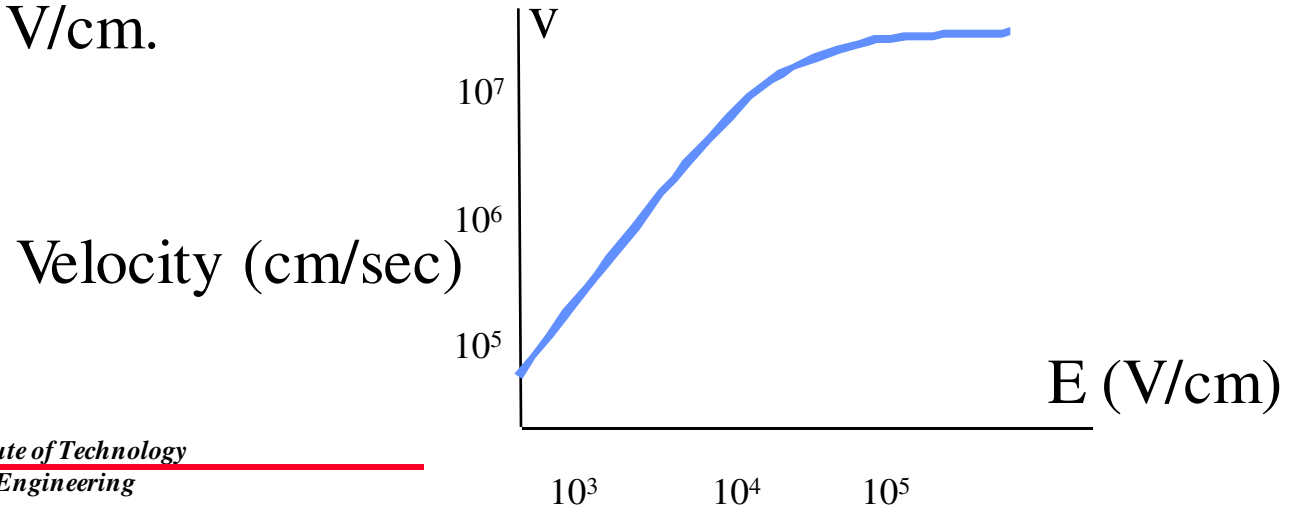
Note: Id should follow green line in long channel devices

VELOCITY-SATURATION

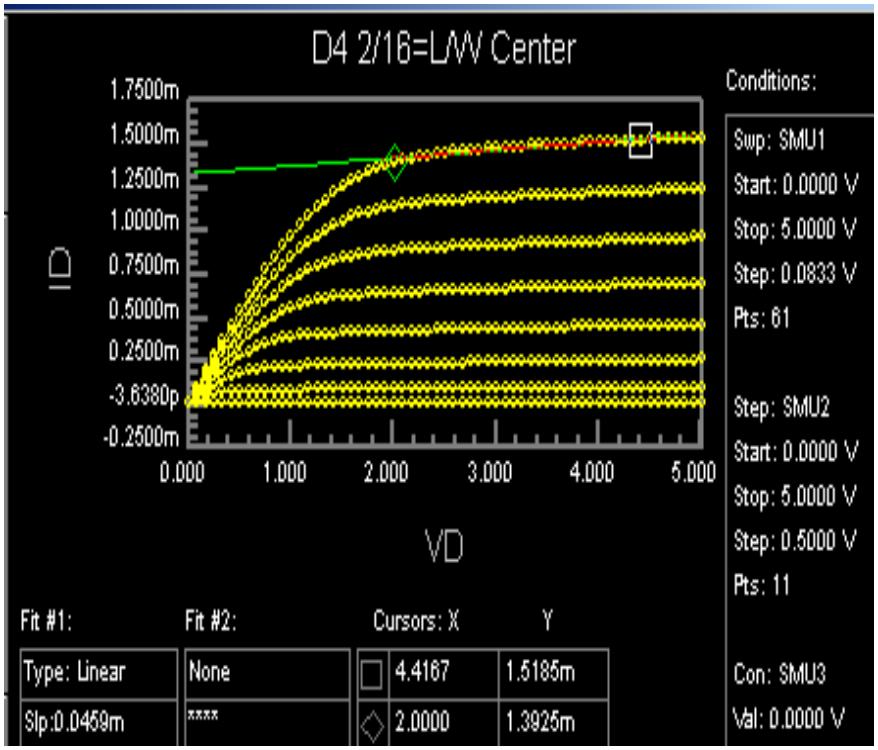
Carriers in semiconductors typically move in response to an applied electric field. The carrier velocity is proportional to the applied electric field. The proportionality constant is the mobility.

Velocity = mobility x electric field = μ E

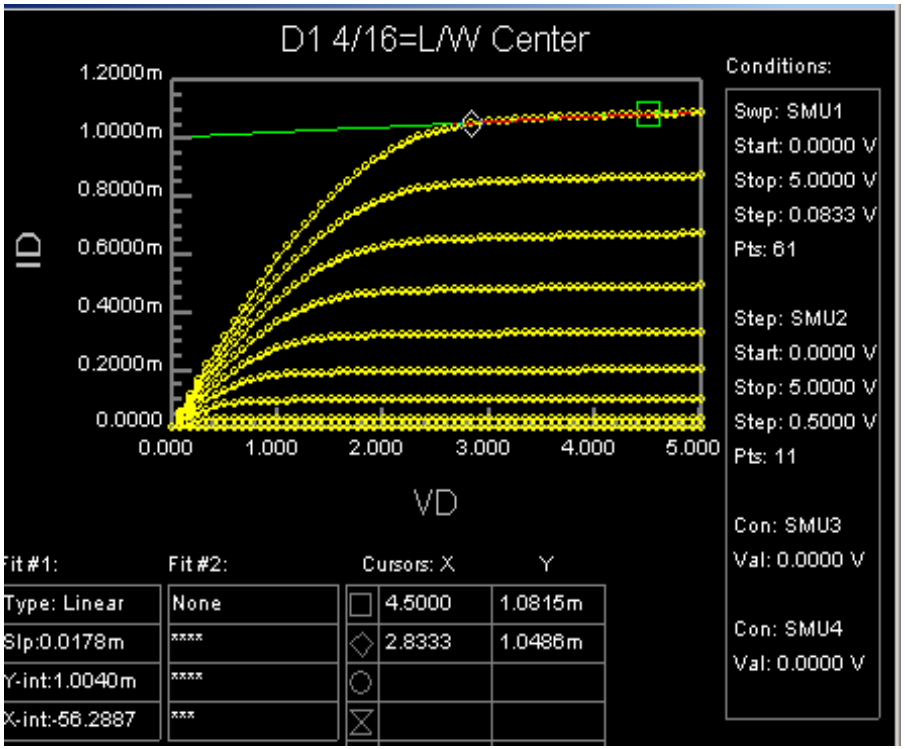
At very high electric fields this relationship ceases to be accurate. The carrier velocity stops increasing (or we say saturates) In a one micrometer channel length device with one volt across it the electric field is 1E4 V/cm.



VELOCITY SATURATION



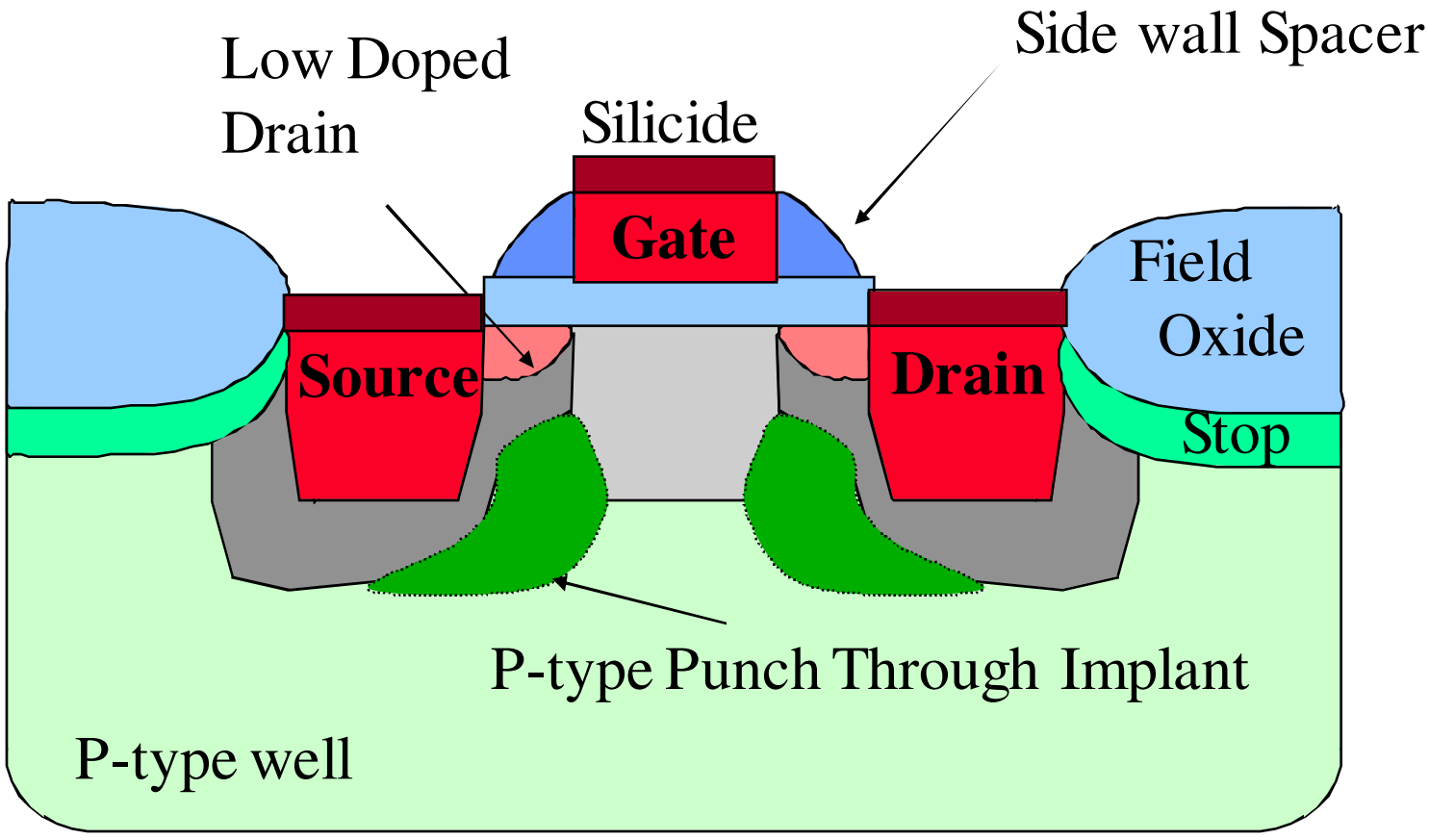
Short channel



long channel

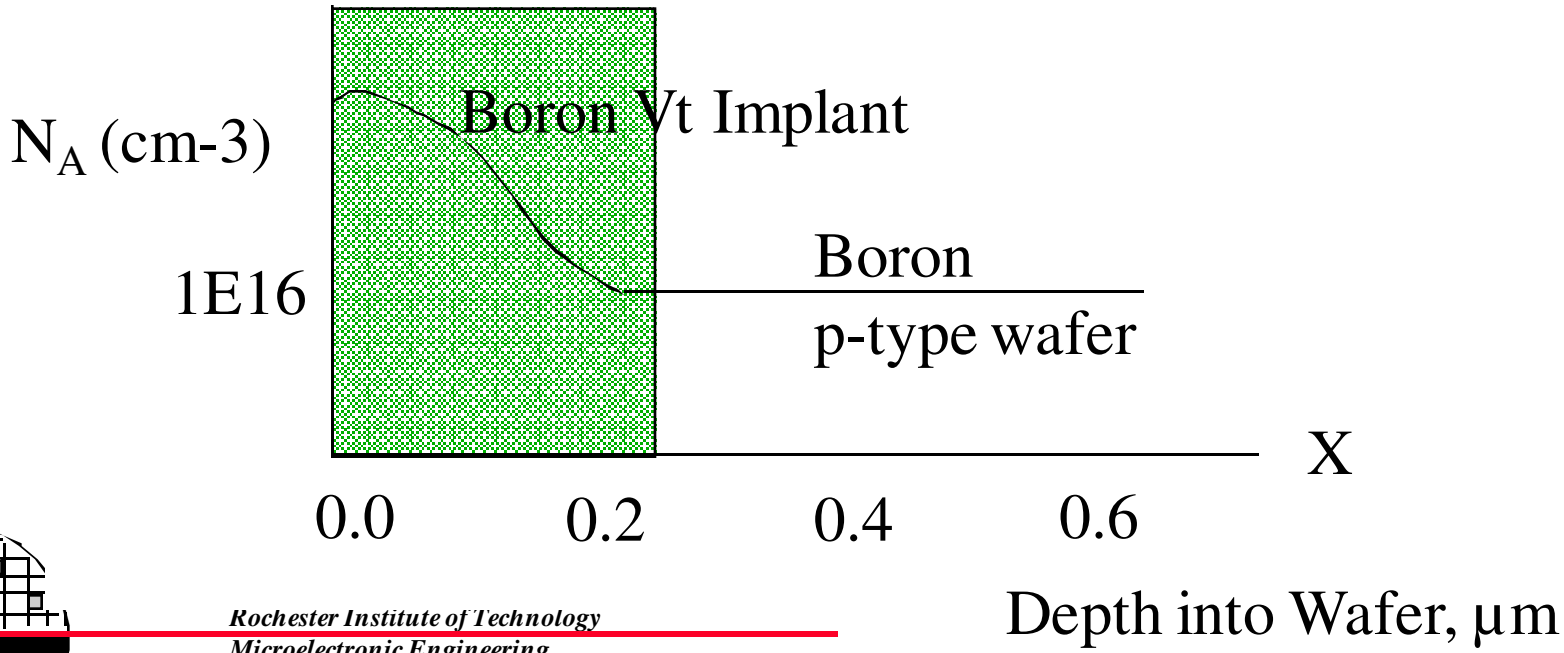
Note: Id should increase with $(Vgs-Vt)^2$ in long channel devices

LOW DOPED DRAIN REDUCES LATERAL FIELD



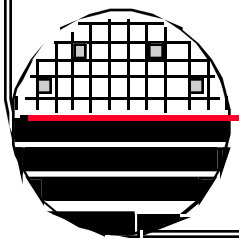
NMOS WITH N+ POLY GATE

- **Vt Is Typically Negative Or If Positive Near Zero**
- **Vt Adjust Implant Is Boron In A P-type Substrate Making The Nmos Transistor A Surface Channel Device**

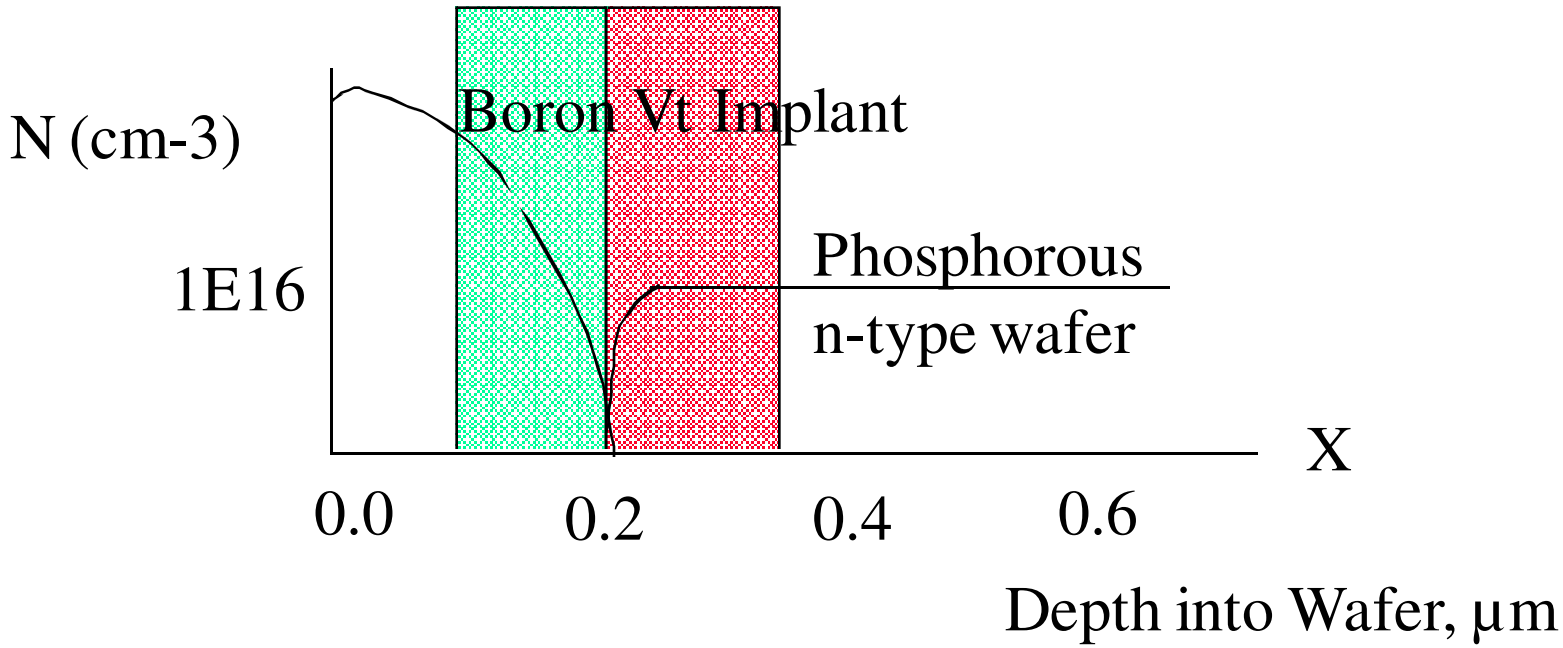


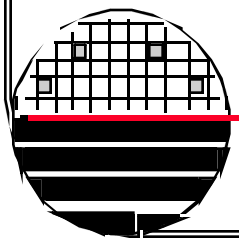
PMOS WITH N+ POLY GATE

- **Vt Can Not Be Positive Because All The Contributors To The Vt Are Negative. Even Making Qss=0 And Nd = Zero Does Not Make Vt Positive**
- **Vt Is Typically More Negative Than Desired Like -2 Volts**
- **Vt Adjust Implant Is Boron In An N-type Substrate Making The Pmos Transistor A Buried Channel Device (Charge Carriers Move Between Drain And Source At Some Distance Away From The Gate Oxide/Silicon Interface**



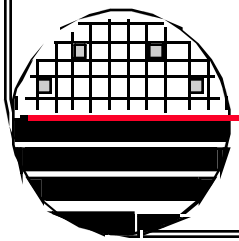
PMOS WITH N+ POLY GATE



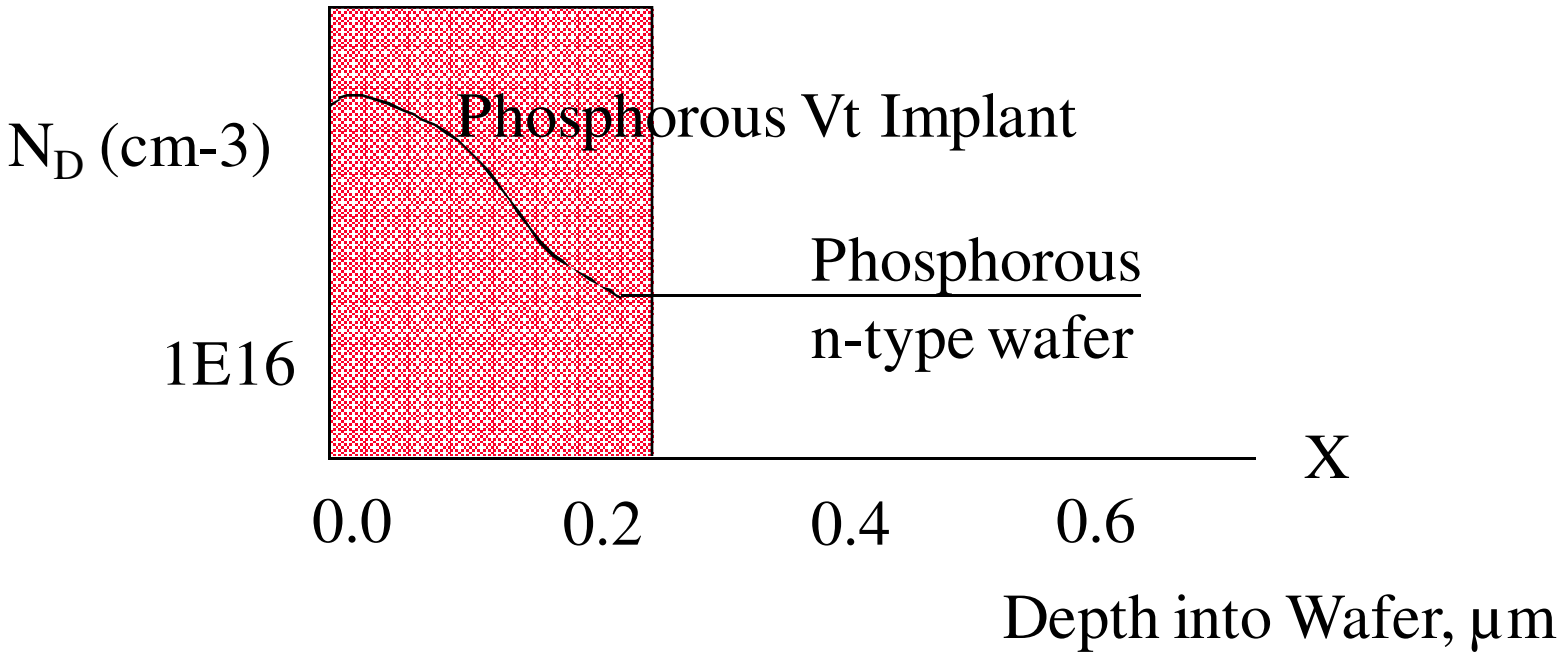


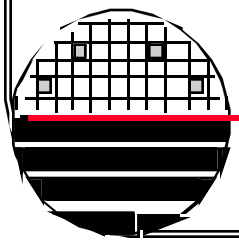
PMOS WITH P+ POLY GATE

- Changes Work Function Of The Metal
- Thus Metal-semiconductor Workfunction Differernce Becomes About +1 Volt Rather Than ~0 Volts.
- This Makes Vt More Positive Than Desired So An Ion Implant Of N-type Impurity Is Needed Making The Device A Surface Channel Device Rather Than A Buried Channel Device.



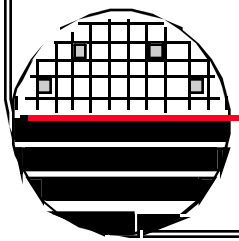
PMOS WITH P+ POLY GATE





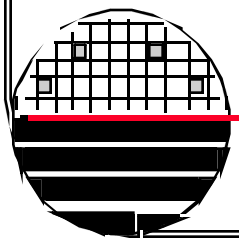
SURFACE CHANNEL VS BURIED CHANNEL

- Surface Channel Devices Exhibit Higher Subthreshold Slope
- Surface Channel Devices Are Less Sensitive To Punch Through
- Surface Channel Devices Have Less Severe Threshold Voltage Rolloff
- Surface Channel Devices Have Higher Transconductance
- Surface Channel Devices Have About 15% Lower Carrier Mobility



SCALING OF MICROCHIPS

Micron, Boise ID		Lmin	Chip Area
16 Meg DRAM	1992	0.5 µm	140.1 mm^2
	1993	0.43	96.2
	1994	0.35	57.0
single level metal	1995	0.35	59.6
	1996	0.35	43.6
	1996	0.30	38.3
	1996	0.25	30.6
	1997	0.30	29.2
64 Meg DRAM	1994	0.35	191.0
	1996	0.30	123.3
	1997	0.25	93.2



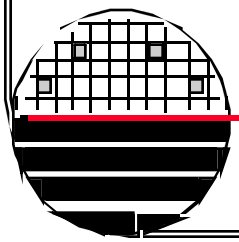
SCALING

Let the scaling factor K be: **K = SIZE OLD / SIZE NEW**

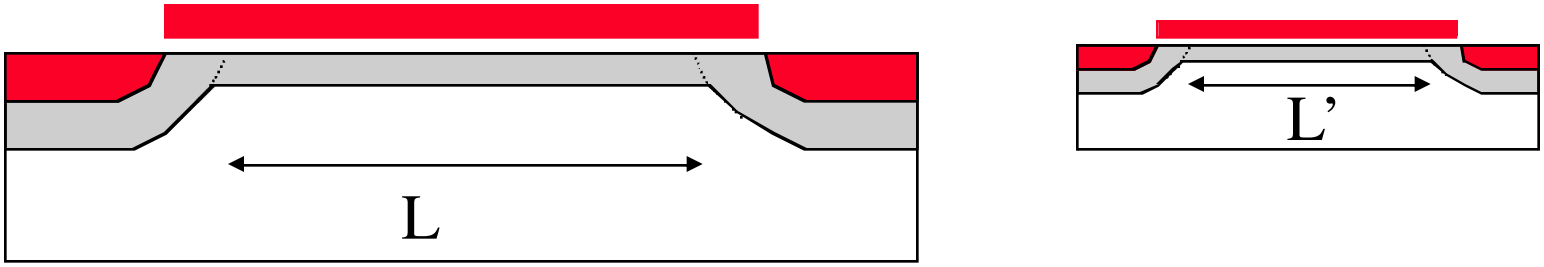
Example: to go from 1.0 µm to 0.8 µm

K = 1.0 / 0.8 = 1.25

To reduce the gate length we also need to reduce the width of the D/S space charge layers. This can done by increasing the substrate doping. Now that the substrate doping is increased the MOSFET Vt is harder to turn on; this can be corrected by decreasing the oxide thickness. Scaling a device in such a way as to keep the internal electric fields constant is called constant-field scaling



CONSTANT FIELD SCALING



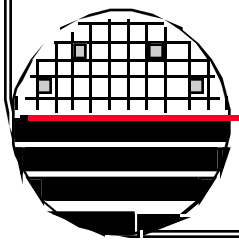
Quantity in Scaled Device = old Quantity times Scaling Factor

Dimensions (L', W', Xox', Xj')	1/K
Area	$1/K^2$
Packing Density	K^2
Doping Concentrations	K
Bias Voltages and Vt	1/K
Bias Currents	1/K
Power dissipation	$1/K^2$
Capacitance	$1/K^2$
Electric Field Intensity	1
Body Effect Coefficient	$1/K^{0.5}$
Transistor Transit Time	1/K
Transistor Power Delay Product	$1/K^3$

OTHER SCALING RULES

Quantity	Constant Field	Constant Voltage	Quasi-Constant Voltage	Generalized
W, L	1/K	1/K	1/K	1/K
Xox	1/K	1/β	1/K	1/K
N	K	K	K	K^2/β
V, Vt	1/K	1	1/β	1/β

$$1 < \beta < K$$



SCALING EXAMPLES

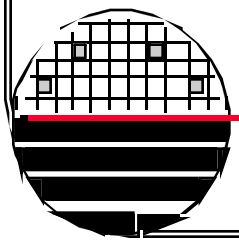
Example: 5 Volt, L=1.0 µm NMOS, Na = 5E16, Xox=250 Å
Scale to 0.8 µm NMOS. Constant Field Scaling

K = 1.0/0.8 = 1.25

Xox= 250/1.25 = 200 Å

N = 5E16 (1.25) = 2.5E17 cm^{-3}

Vsupply = 5Volts/ 1.25 = 4 Volts and Vt = 1/1.25 = 0.8 Volts

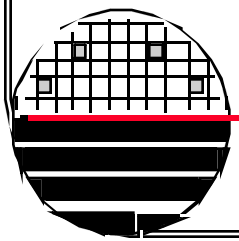


GATE OXIDE THICKNESS

The gate should be as thin as possible to reduce the short channel effects. In addition there is a limit imposed by considerations that affect the long term reliability of the gate oxide. This requirement imposes a maximum allowed electric field in the oxide under the long term normal operating conditions. This limit is chosen as 80% of the oxide field value at the on-set of Fowler-Nordheim (F-N) tunneling through the oxide. Since the latter is 5 MV/cm, a 4 MV/cm oxide field is considered as the maximum allowed for long term, reliable operation. For example:

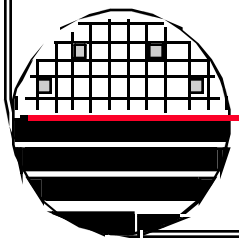
For 2.5 volt operation, Xox is set at: Xox = Vdd /Emax

=2.5 V/4MV/cm = 65Å



SALICIDE

Ti Salicide will reduce the sheet resistance of the poly and the drain and source regions. Salicide is an acronym for Self Aligned Silicide and Silicide is a material that is a combination of silicon and metal such as Ti, W or Co. These materials are formed by depositing a thin film of the metal on the wafer and then heating to form a Silicide. The Silicide forms only where the metal is in contact with the Silicon or poly. Etchants can remove the metal and leave the Silicide thus the term **S**elf **A**ligned Si**licide** or SALICIDE.

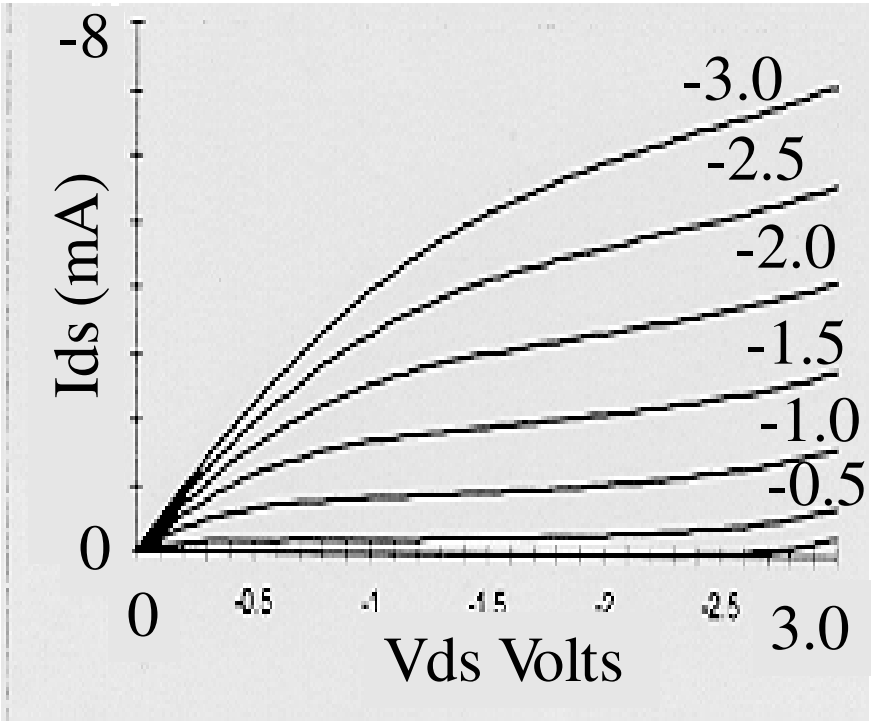


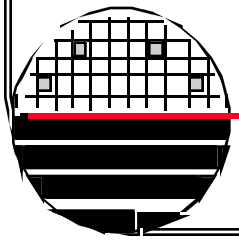
RIT's FIRST SUB MICRON TRANSISTOR

Mark Klare 7/22/94 Electron beam direct write on wafer, n-well process 5E12 dose, P+ Poly Gate PMOS, shallow BF2 D/S implant, no Vt adjust implant.

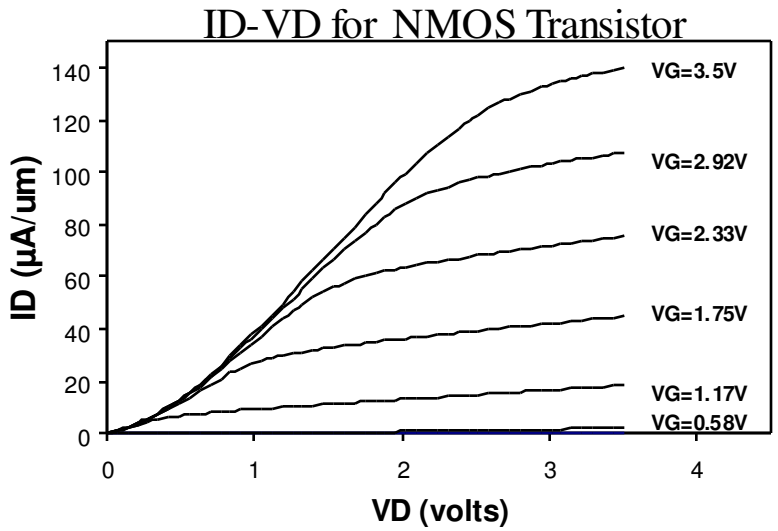
L=0.75 um
Xox=300 Å
D/S Xj = 0.25 µm
P+ poly
Nd well ~3E16

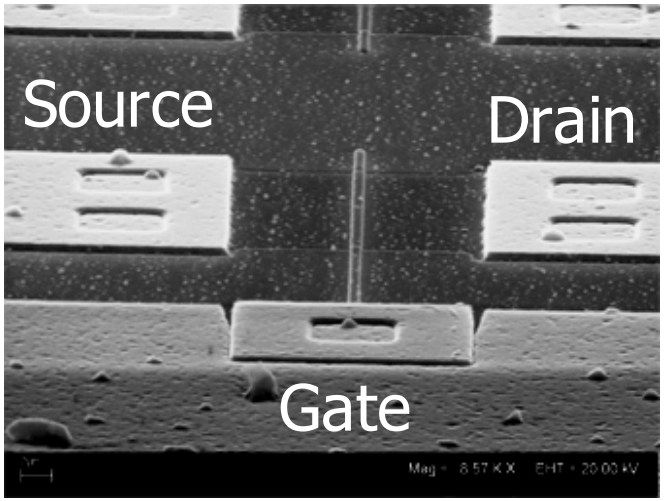
Vt = -0.15
Sub Vt Slope=130 mV/dec





RIT NMOS Transistor with Leffective = 0.4 µm

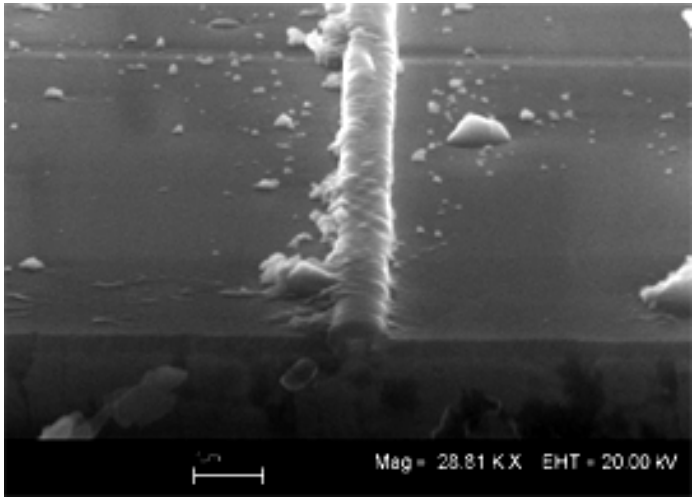


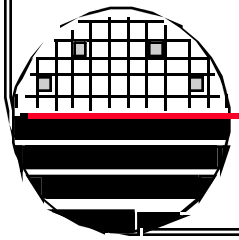


$L_{mask\ drawn} = 0.6\ \mu m$

$L_{effective} = 0.4\ \mu m$

This is RIT's first sub-0.5 µm Transistor

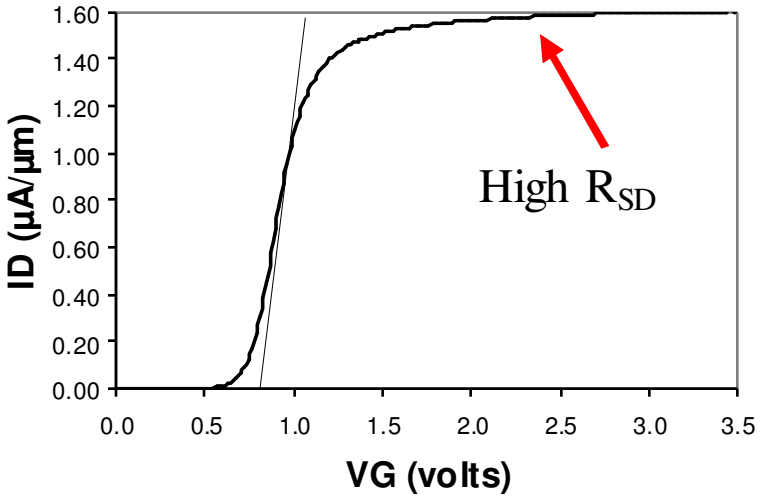




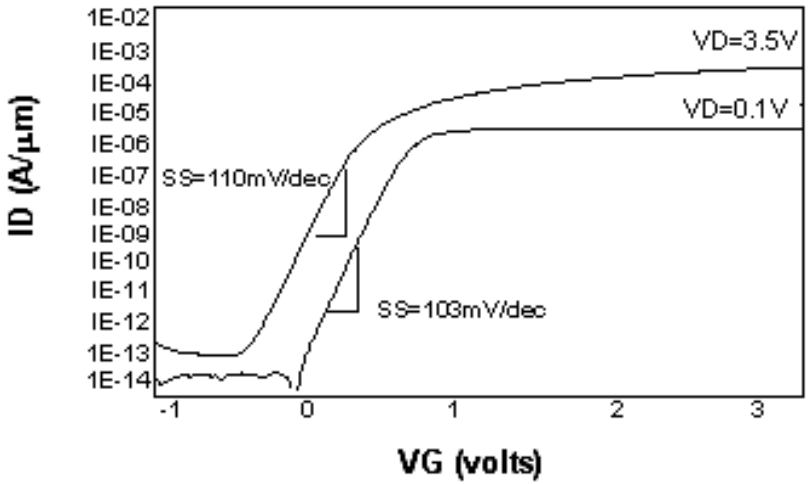
Mike Aquilino May 2004

RIT NMOS Transistor with Leffective = 0.4 µm

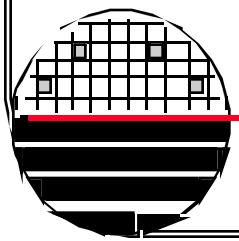
ID-VG Vt Sweep



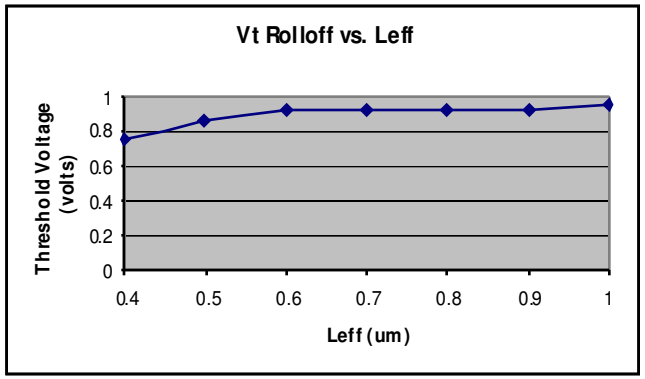
ID-VG Sub-Threshold Slope

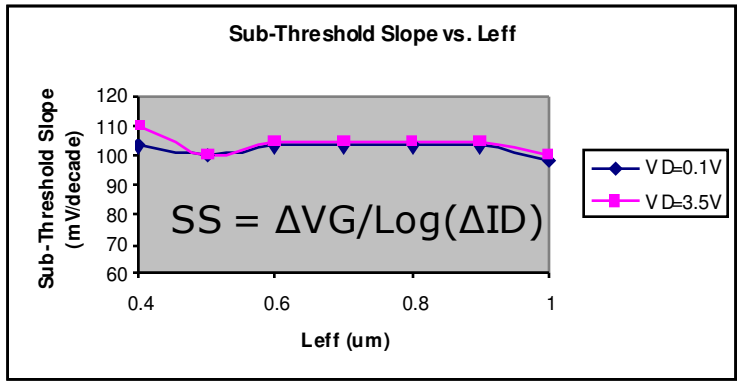


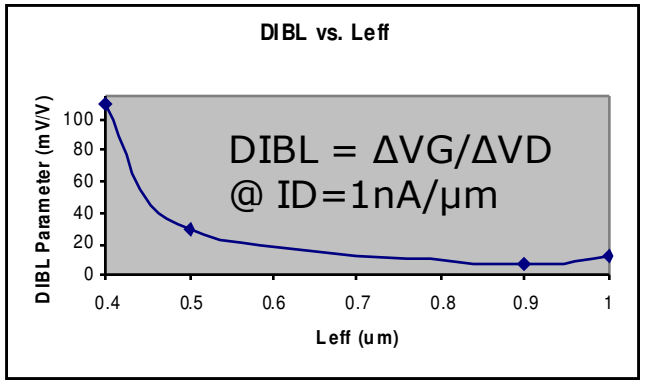
L_{eff} = 0.4 µm
ID @ (VG=VD=3.5V) = 140 µA/µm
Vt = 0.75V
SS = 103 mV/decade
Log (I_{on}/I_{off}) = 7.5 Orders of Magnitude



RIT NMOS Transistor with Leffective = 0.4 µm







L_{eff} (µm)	Vt (V)	SS (mV/dec)	DIBL (mV/V)
0.4	0.75	103	110
0.5	0.85	100	29

- 0.5 um exhibits well controlled short channel effects
- 0.4 um device can be used depending on off-state current requirements
- 33% Increase in Drive Current compared to 0.5 um device

Mike Aquilino May 2004

SUB 0.25µm NMOSFET

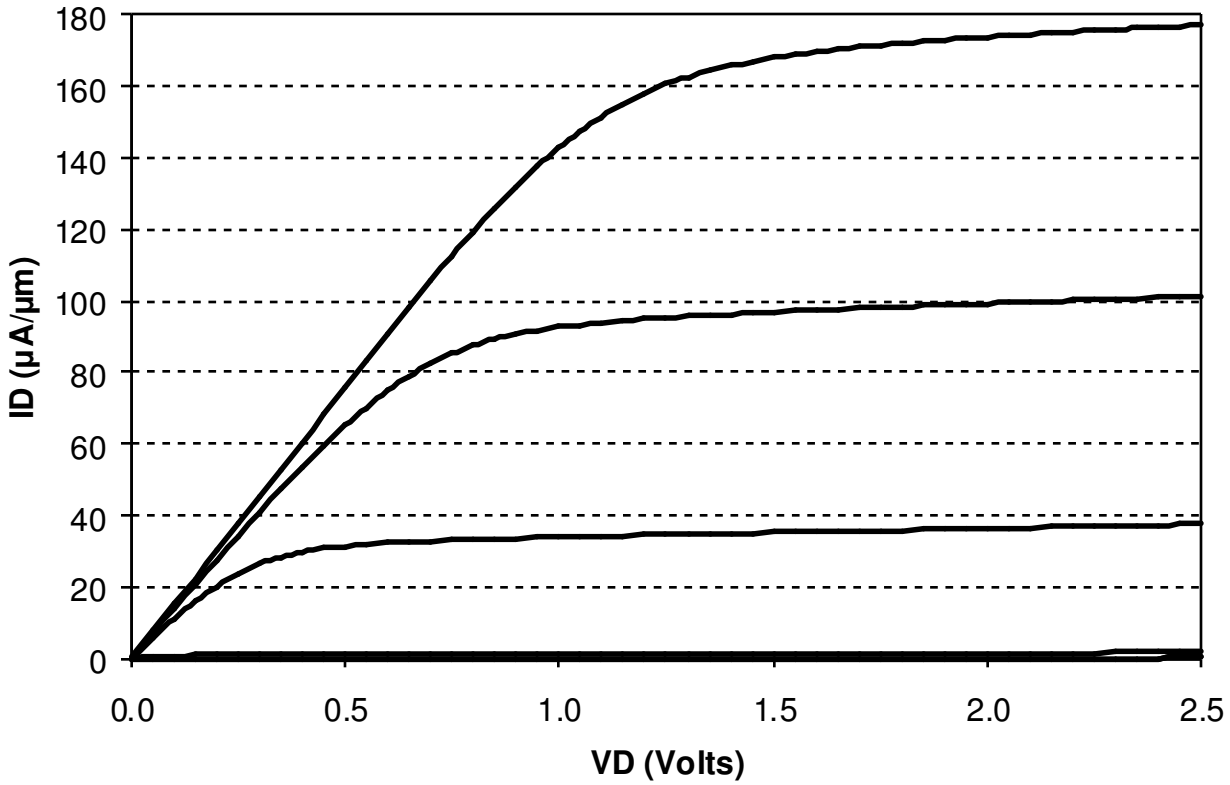


Figure 28: ID-VD for 0.25 µm NMOS Transistor

- L_{mask} = 0.5 µm
- L_{poly} = 0.25 µm
- $L_{effective}$ = 0.2 µm

Mike Aquilino
May 2006

- ID = 177 µA/µm @ VG=VD=2.5 V
- V_T = 1.0 V

*This is RIT's Smallest NMOS Transistor

SUB 0.25µm PMOSFET

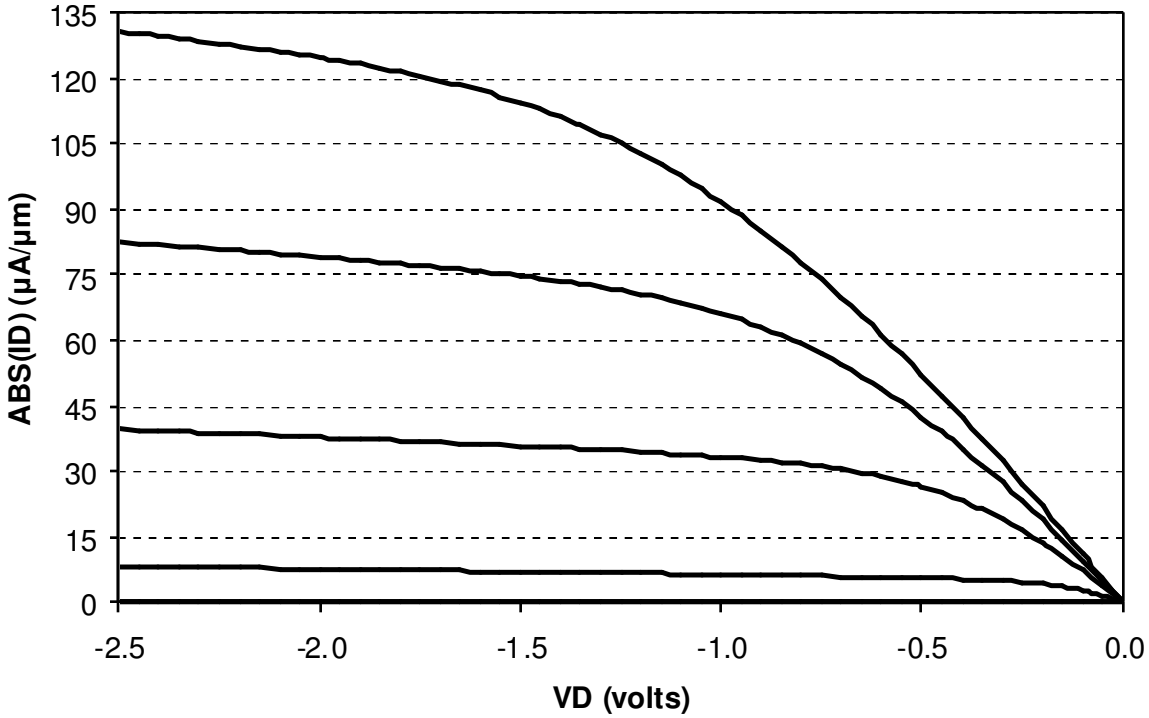


Figure 31: ID-VD for 0.25 µm PMOS Transistor

- o L_{mask} = 0.6 µm
- o L_{poly} = 0.25 µm
- o $L_{effective}$ = 0.2 µm

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May 2006

*This is RIT's Smallest PMOS Transistor

- o |ID| = 131 µA/µm @ VG=VD=-2.5 V
- o V_T = -0.75 V

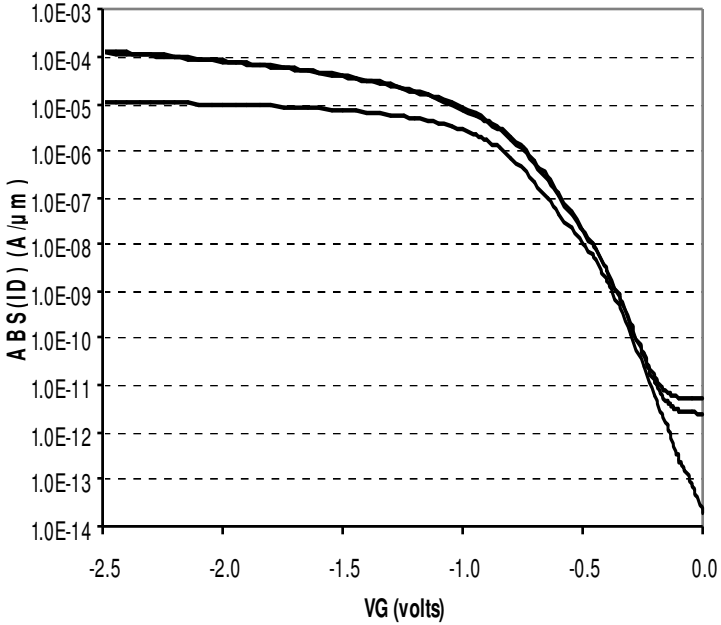
MORE DATA FOR 0.25µM MOSFET'S

0.25µm Leff NMOSFET

- o I_{off} = 13 pA/µm @ VD=0.1 V (with drain diode leakage removed)
- o I_{off} = 11 nA/µm @ VD=2.5 V (with drain diode leakage removed)
- o Log(I_{on}/I_{off}) = 4.2 decades
- o SS = 119 mV/decade @ VD=0.1 V

0.25µm Leff PMOSFET

- o I_{off} = -20 fA/µm @ VD=-0.1 V
- o I_{off} = -4.9 pA/µm @ VD=-2.5 V
- o Log(I_{on}/I_{off}) = 7.4 decades
- o SS = 75 mV/decade @ VD=-0.1 V
- o SS = 85 mV/decade @ VD=-2.5 V
- o DIBL = 8.3 mV/V @ ID=-1 nA/µm



ID-VG for 0.25 µm PMOS Transistor

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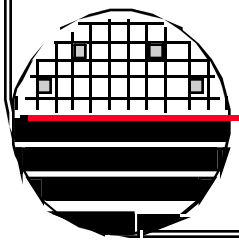

HOMEWORK – SHORT CHANNEL MOSFETs

1. In short channel devices the threshold voltage becomes less than expected for long channel devices. Why.
2. Explain reverse short channel effect.
3. What is the effect of narrow channel width on transistor device characteristics.
4. What is the purpose of low doped drain structures?
5. How does mobility degradation and velocity saturation effect transistor device characteristics?
6. Why is P+ doped poly used for PMOS transistors.
7. What is the difference between mask channel length and effective channel length.
8. What is punchthrough? What processing changes can be made to compensate for punchthrough?
9. When scaling from 2 um to 1.5 um give new values for: device dimensions W,L,Xox, doping concentration, bias voltages, bias currents, power dissipation, transit time.
10. What is SALICIDE process. Why is it used?