ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

RIT’s Advanced CMOS Process
λ=0.25 µm, L_{poly}= 0.5 µm, L_{eff} = 100nm

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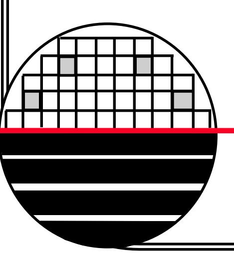
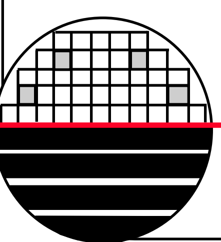


OUTLINE

Introduction
Advanced CMOS Process Details



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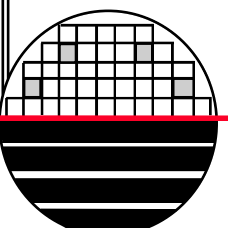
INTRODUCTION

RIT is supporting two different CMOS process technologies. The older p-well CMOS and SMFL-CMOS have been phased out. The SUB-CMOS process is used for standard 3 Volt Digital and Analog integrated circuits. This is the technology of choice for teaching circuit design and fabricating CMOS circuits at RIT. The ADV-CMOS process is intended to introduce our students to process technology that is close to industry state-of-the-art. This process is used to build test structures and develop new technologies at RIT.

RIT p-well CMOS	$\lambda = 4\ \mu m$	Lmin = 8 μm
RIT SMFL-CMOS	$\lambda = 1\ \mu m$	Lmin = 2 μm
RIT Subμ-CMOS	$\lambda = 0.5\ \mu m$	Lmin = 1.0 μm
RIT Advanced-CMOS	$\lambda = 0.25\ \mu m$	Lmin = 0.5 μm



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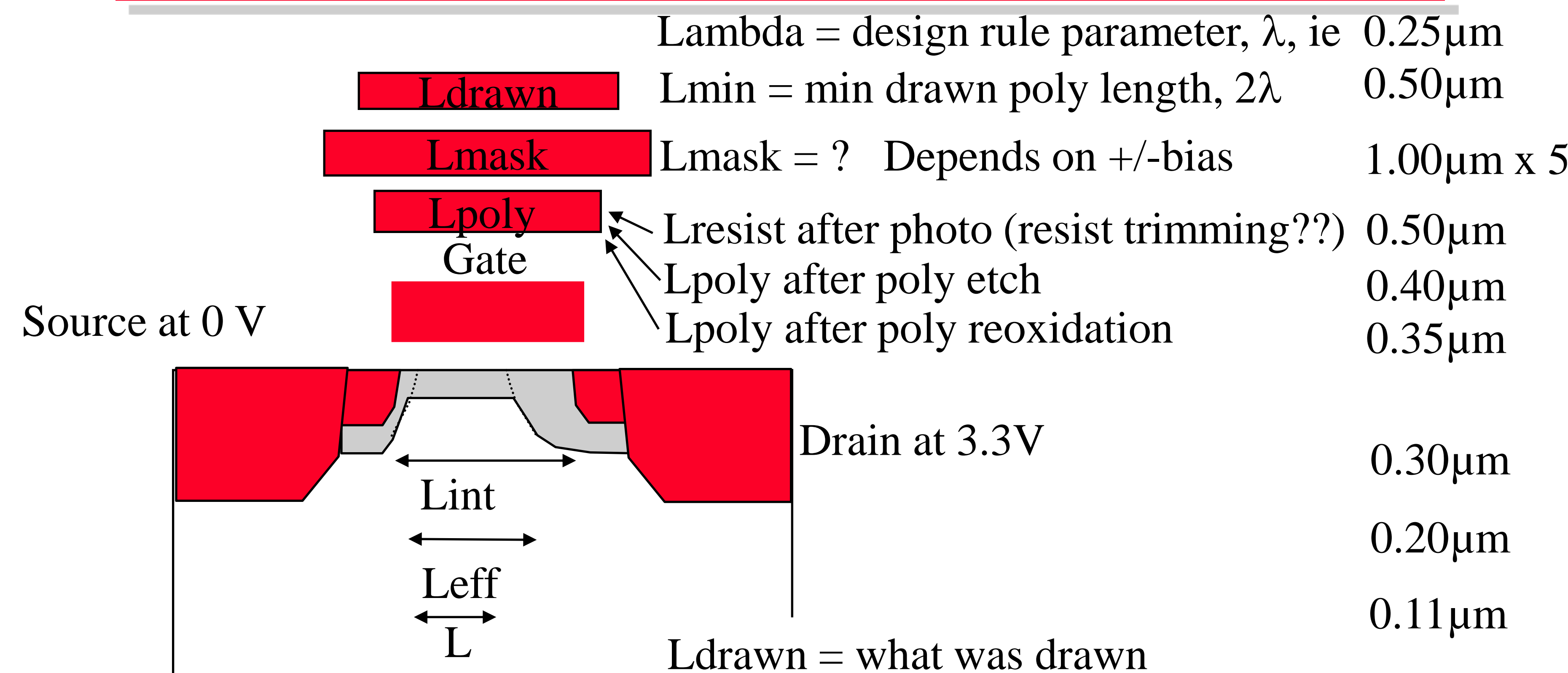
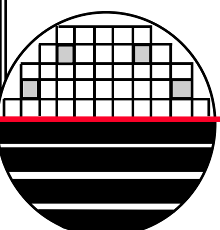
LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L



Internal Channel Length, Lint =distance between junctions, including under diffusion
Effective Channel Length, Leff = distance between space charge layers,Vd = Vs= 0
Channel Length, L, = distance between space charge layers, when Vd= what it is
Extracted Channel Length Parameters = anything that makes the fit good (not real)

INTRODUCTION

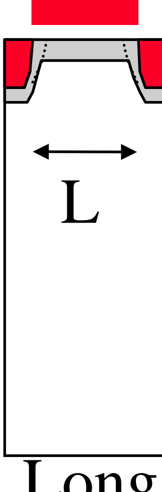
Advanced Processes Used:
Shallow Trench Etch with Endpoint
Trench PECVD TEOS fill and CMP
Silicide TiSi2, Recipes for Rapid Thermal Processor
Dual Doped Gate, Ion Implant and Mask Details
Anisotropic Poly Etch
100 Å Gate Oxide Recipe with N2O
Nitride Spacer, New Anisotropic Nitride Etch
Plasma Etch of Contacts and Vias
Aluminum Metal, W Plugs Deposition, CMP of Oxide
Canon and ASML Masks
Canon and ASML Stepper Jobs
MESA Process, Products, Instructions, Parameters



RIT ADVANCED CMOS VER 150

RIT Advanced CMOS

150 mm Wafers
Nsub = 1E15 cm-3 or 10 ohm-cm, p
Nn-well = 1E17 cm-3
Xj = 2.5 µm
Np-well = 1E17 cm-3
Xj = 2.5 µm
Shallow Trench Isolation
Field Ox (Trench Fill) = 4000 Å
Dual Doped Gate n+ and p+
Xox = 100 Å
Lmin = 0.5 µm , Lpoly = 0.35 µm, Leff = 0.11 µm
LDD/Nitride Side Wall Spacers
TiSi2 Salicide
Tungsten Plugs, CMP, 2 Layers Aluminum



Long Channel Behavior

Vdd = 3.3 volts
Vto=+- 0.75 volts

PROCESS CALCULATIONS

Built in Voltage: $\Psi_o = KT/q \ln (Na\ Nd/ni^2)$

Width of Space Charge Layer: $Wsc = [(2\varepsilon/q)(\Psi_o + V_R)(1/Na + 1/Nd)]^{1/2}$

$E_o = - [(2q/\varepsilon)(\Psi_o + V_R)(NaNd/(Na+Nd))]^{1/2}$

Example:

$\Psi_o = 0.026 \ln (1E17\ 1E17/1.45E10^2) = 0.82$

Wsc @ 0V=[(2(11.7)(8.85E–14)/1.6E-19)(0.82)(1/1E17 + 1/1E17)]$^{1/2}$

= 0.15 µm and 0.07 µm on each side of the junction

Wsc @ 3.3V=[(2(11.7)(8.85E-14)/1.6E-19)(0.82+3.3)(1/1E17)]$^{1/2}$

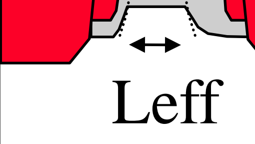
= 0.33 µm and 0.16 µm on each side of the junction

$E_o = - 2.5E5$ V/cm

Gate

Source at 0 V

Drain at 3.3V



Leff

$\varepsilon = \varepsilon_o \varepsilon_r = 8.85E\text{-}12\ (11.7)$ F/m

Leff = 0.5 - 0.07 - 0.16 = ~ 0.27 µm

RIT ADVANCED CMOS

NMOSFET

PMOSFET

N+ Poly

P+ Poly

N+ D/S

P+ D/S

p+ well contact

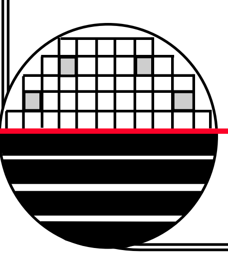
n+ well contact

LDD

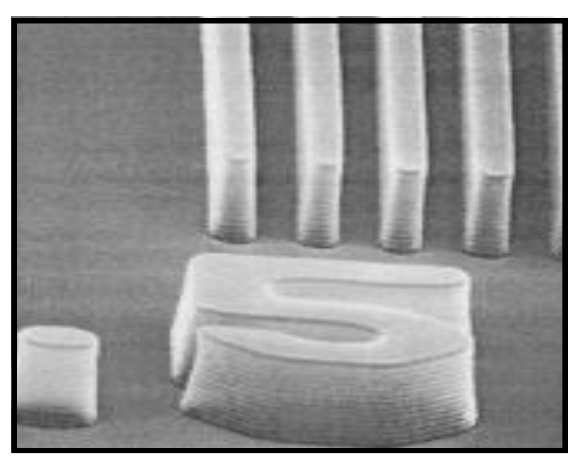
LDD

P-well

N-well



ASML 5500/200

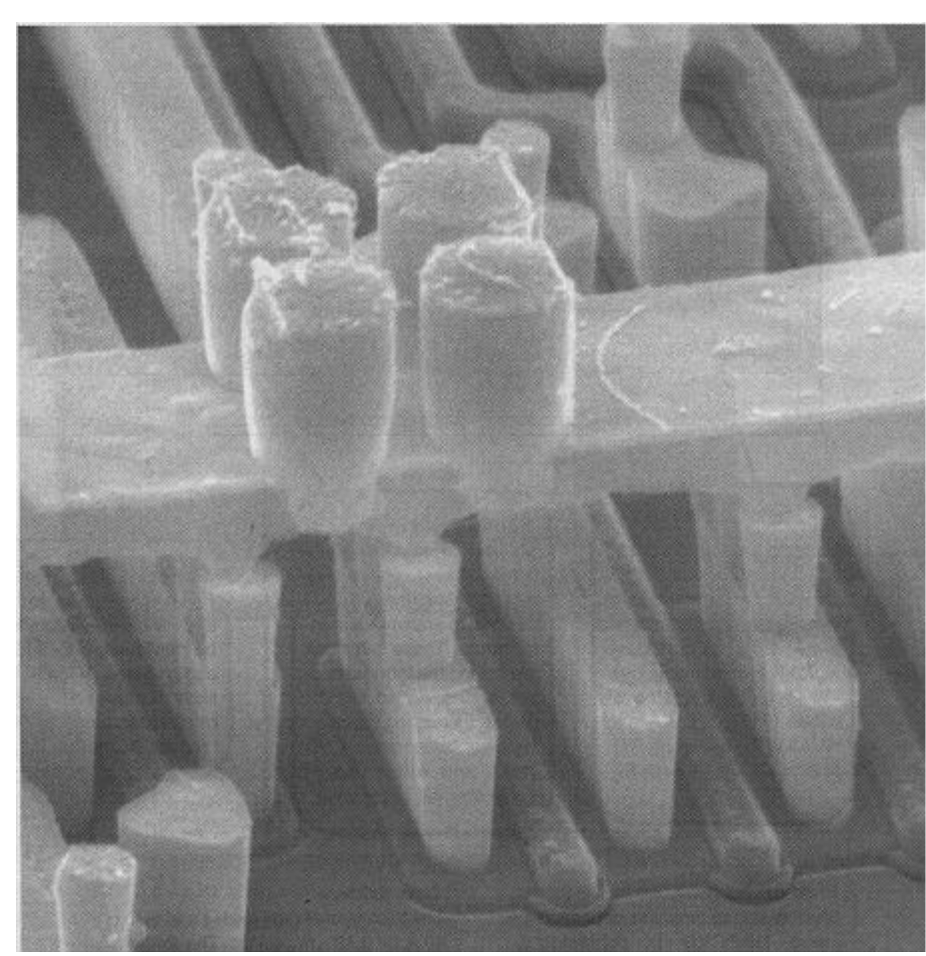


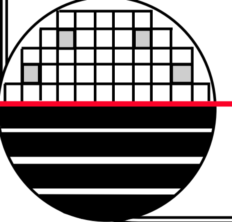
NA = 0.48 to 0.60 variable
σ= 0.35 to 0.85 variable
With Variable Kohler, or
Variable Annular illumination
Resolution = K1 λ/NA
= ~ 0.35µm
for NA=0.6, σ =0.85
Depth of Focus = k_2 $\lambda/(NA)^2$
= > 1.0 µm for NA = 0.6

i-Line Stepper λ = 365 nm
22 x 27 mm Field Size

MULTI- LAYER ALUMINUM, W PLUGS, CMP, DAMASCENE OF LOCAL W INERCONNECT

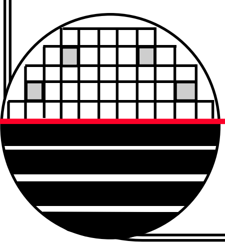
Multi-layer aluminum interconnect with tungsten plugs, CMP, and damascene of local tungsten interconnect.





JOHN GALT CMOS TESTCHIP

2010



MOSIS TSMC 0.35 2POLY 4 METAL PROCESS

http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html#tech-codes

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MOSIS SCMOS Technology Codes and Layer Maps

SCN4M and SCN4M_SUBM

This is the layer map for the technology codes SCN4M and SCN4M_SUBM using the MOSIS Scalable CMOS layout rules (SCMOS), and only for SCN4M and SCN4M_SUBM. For designs that are laid out using other design rules (or technology codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

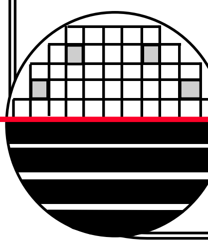
SCN4M: Scalable CMOS N-well, 4 metal, 1 poly, silicided. Silicide block and thick oxide option available only on the TSMC process.

SCN4M_SUBM: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

Fabricated on TSMC, AMIS, and Agilent/HP 0.35 micron process runs. See "Notes" section of layer map for foundry-specific options.

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	
ACTIVE	43	CAA		2	
THICK_ACTIVE	60	CTA		24	Optional for TSMC; not available for Agilent/HP nor AMIS
POLY	46	CPG		3	
SILICIDE_BLOCK	29	CSB		20	Optional for Agilent/HP; not available for AMI
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	
METAL3	62	CM3	CMT	15	
VIA3	30	CV3	CVT	21	
METAL4	31	CM4	CMQ	22	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME

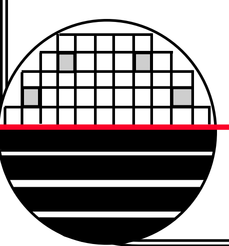


MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

MASK LAYER NAME	MENTOR NAME	GDS #	COMMENT
N WELL	N_well.i	42	
ACTIVE	Active.i	43	
POLY	Poly.i	46	
N PLUS	N_plus_select.i	45	
P PLUS	P_plus_select.i	44	
CONTACT	Contact.i	25	Active_contact.i 48 poly_contact.i 47
METAL1	Metal1.i	49	
VIA	Via.i	50	
METAL2	Metal2.i	51	

MORE LAYERS USED IN MASK MAKING

LAYER	NAME	GDS	COMMENT
	cell_outline.i	70	Not used
	alignment	81	Placed on first level mask
	nw_res	82	Placed on nwell level mask
	active_lettering	83	Placed on active mask
	channel_stop	84	Overlay/Resolution for Stop Mask
	pmos_vt	85	Overlay/Resolution for Vt Mask
	LDD	86	Overlay/Resolution for LDD Masks
	p plus	87	Overlay/Resolution for P+ Mask
	n plus	88	Overlay/Resolution for N+ Mask



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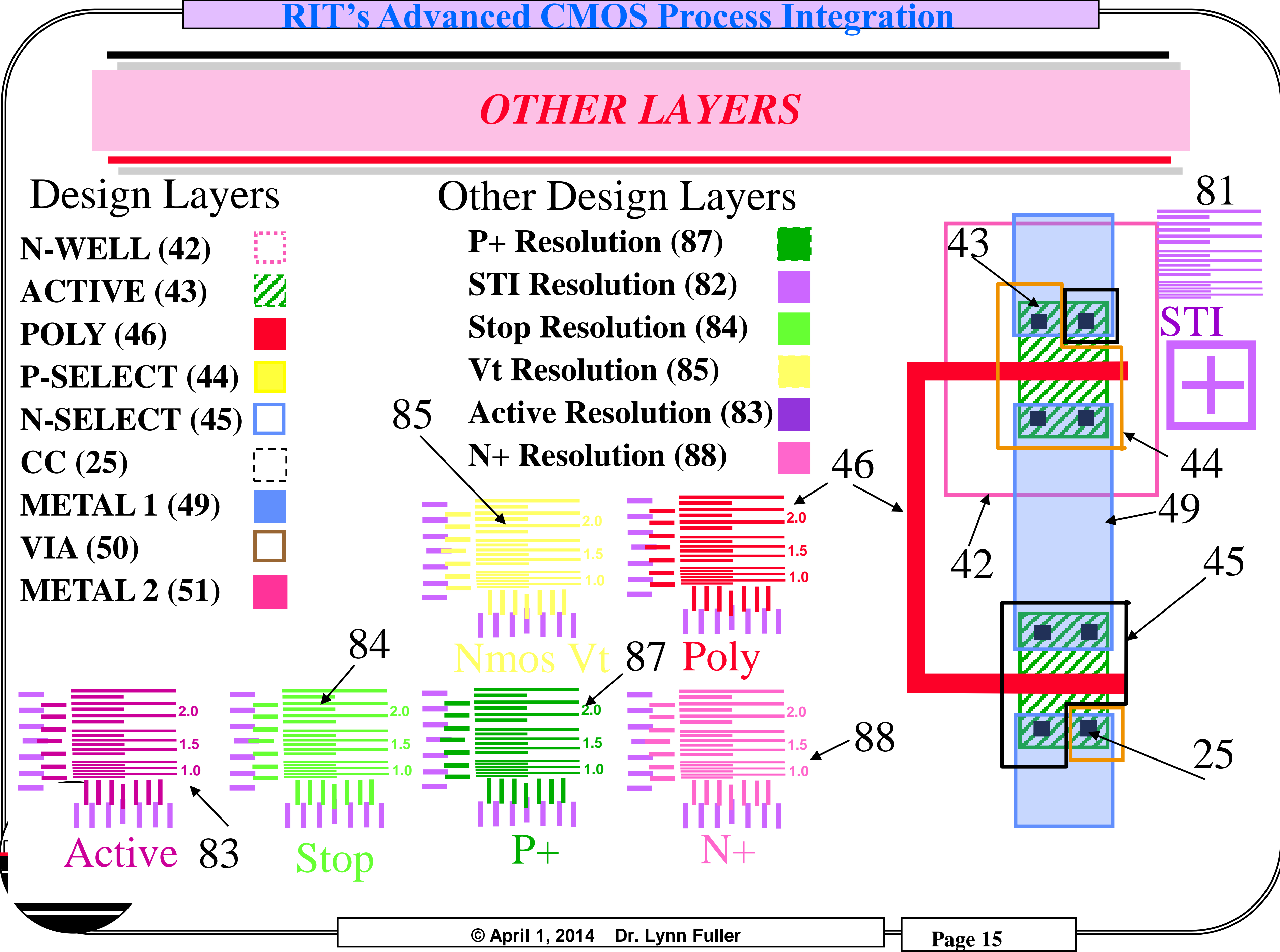

RIT's Advanced CMOS Process Integration
OTHER LAYERS
Design Layers
N-WELL (42)
ACTIVE (43)
POLY (46)
P-SELECT (44)
N-SELECT (45)
CC (25)
METAL 1 (49)
VIA (50)
METAL 2 (51)
Other Design Layers
P+ Resolution (87)
STI Resolution (82)
Stop Resolution (84)
Vt Resolution (85)
Active Resolution (83)
N+ Resolution (88)
81
STI
43
44
46
49
42
45
25
85
84
87
88
83
2.0
1.5
1.0
Nmos Vt
Poly
Active
Stop
P+
N+
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MASK ORDER FORM

RIT Mask order form is found at the following link:

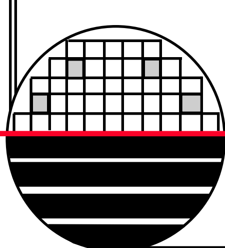
http://smfl.microe.rit.edu/forms/Order_Request.dot

Rochester Institute of Technology
Semiconductor & Microsystems Fabrication Laboratory

Mask Making
Order Request

Customer Information	
Name	
Company	
Department	
Street Address	
City, State and Zip Code	,
Phone Number	( ) -
Project Code	
E-mail Address	
Order Date	July 23, 2007
Order Due Date	

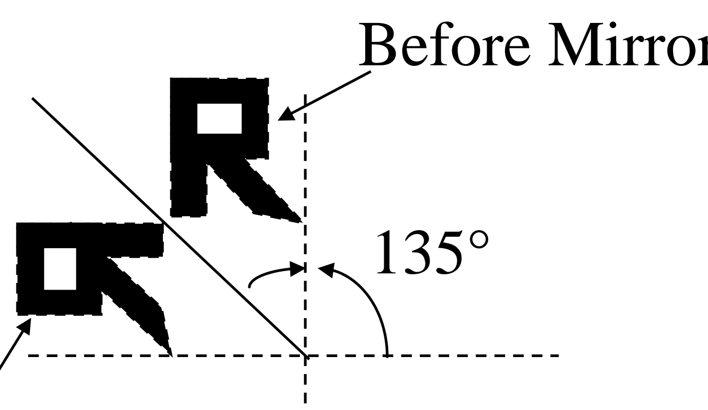
Mask Information		
SEE PAGE 2 FOR INSTRUCTIONS ON CREATING YOUR GDS FILE!		
Design Name	.gds	
Number of Design Layers in Layout		
Number of Mask Levels		
Cell Layout Size	X: µm	Y: µm
Alignment Key (Center of Die is Origin)	X: µm	Y: µm
Fracture Resolution	☐ 0.5µm	☐ µm
Scale Factor	5X	
Orientation	☐ Mirror135	☐
Rotation	☐ None	☐
Plate Size	5" x 5" x 0.090" – Email for other sizes	
Number of Levels on Plate	1	
Array	☐ None ☐ Array with rows and columns	



MASK ORDER CONTINUED

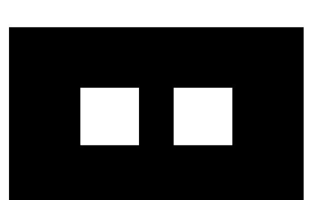
	Level	Mask #	Layer	GDS	Operation	Field
1	STI	1	Active.i	43	(43 OR 81 OR 83 or 82) plus Tilir	Clear Field
			alignment	81		
			active_lettering	83		
			nw_res	82		
2	NWELL	2	N_well.i	42	INVERT	Dark Field
3	PWELL	3	N_well.i	42	none	Clear Field
4	NVT	4	N_plus_select.i	45	(45 OR 85) INVERT	Dark Field
			pmos_vt	85		
	PVT	5	P_plus select.i	44	(44 OR 85) INVERT	Dark Field
			pmos_vt	85		
	POLY	6	Poly.i	46	none	Clear Field
	PLDD	7	P_plus select.i	44	(44 OR 86) INVERT	Dark Field
			LDD	86		
	NLDD	8	N_plus_select.i	45	(45 OR 86) INVERT	Dark Field
			LDD	86		
	N+DS	9	P_plus_select.i	44	(45 OR 88)	Clear Field
			n plus	88		
	P+DS	10	N_plus select.i	45	(45 OR 87)	Clear Field
			p plus	87		
	CC	11	contact	25	(25 OR 48 OR 47) INVERT	Dark Field
			Active_contact.i	48		
			Poly_contact.i	47		
	METAL1	12	metal1.i	49	none	Clear Field
	VIA	13	Via.i	50	INVERT	Dark Field
	METAL2	14	metal2.i	51	none	Clear Field

DATA PREP USING CATS

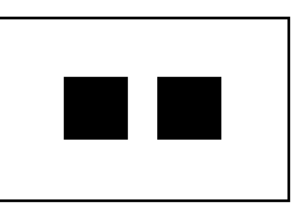


Input File: GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

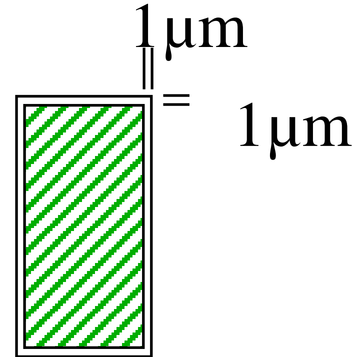
Output File: MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only



Dark Field: Black is chrome, White is Quartz.

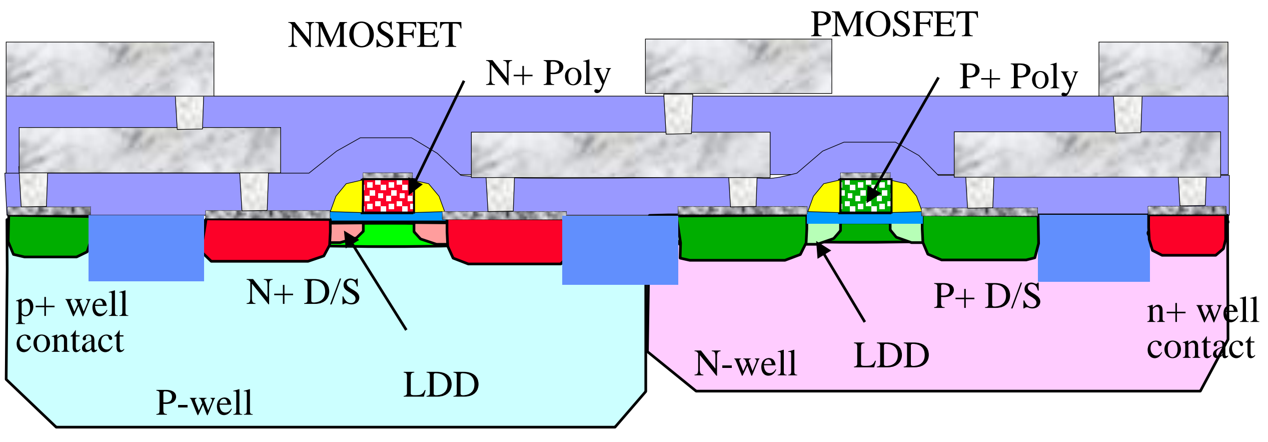


Light Field: Black is chrome, White is Quartz.

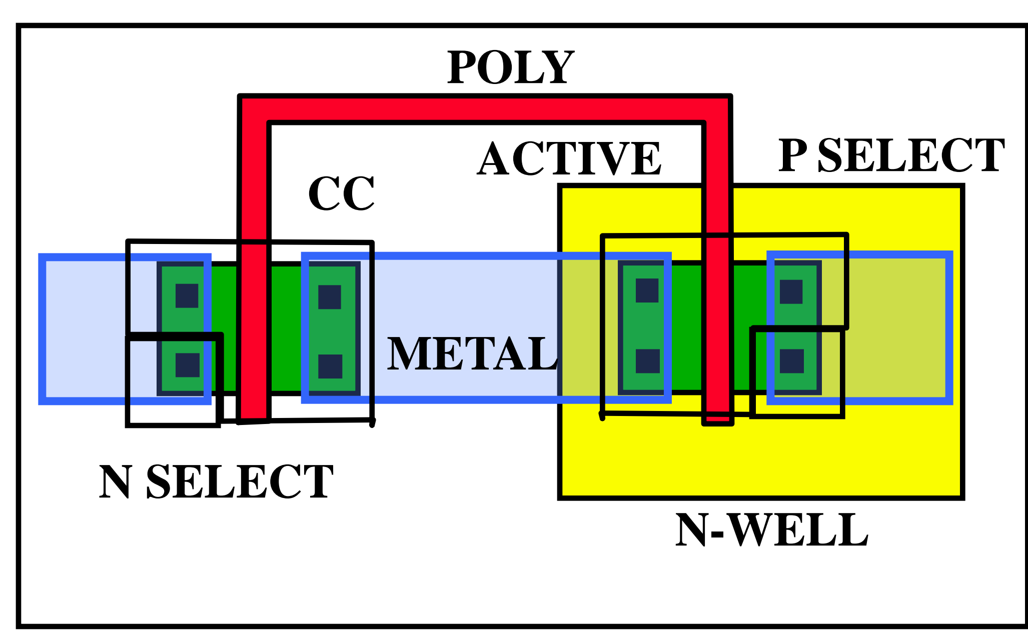


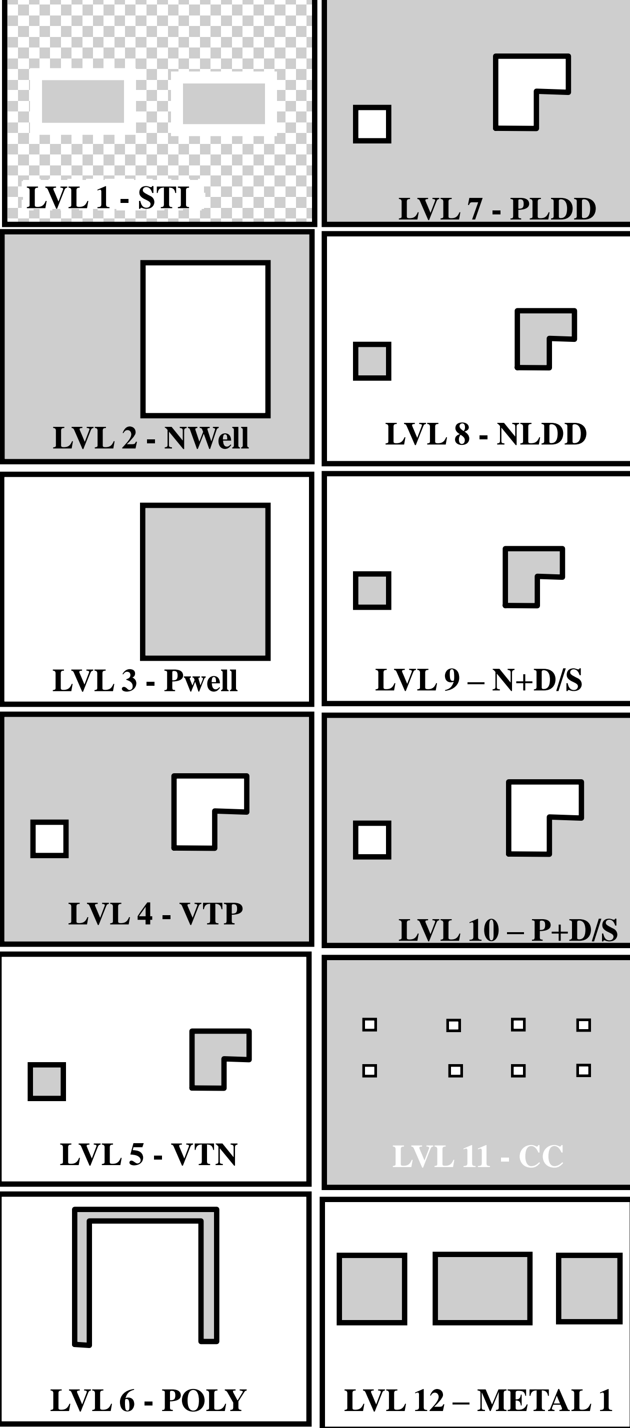
BIAS +1µm

RIT ADVANCED CMOS



12 PHOTO LEVELS + 2 FOR EACH ADDITIONAL METAL LAYER





ADV-CMOS 150 PROCESS

ADV-CMOS Versions 150, Two level Metal

1. OX05--- pad oxide 500 Å, Tube 4
2. CV02- 1500 Å Si_3N_4 Deposition
3. PH03 – level 1- STI
4. ET29 - etch Nitride
5. ET07 – ash
6. CL01 – RCA clean
7. OX04 – First Oxide Tube 1
8. ET06 – Etch Oxide
9. OX04 – 2nd Oxide Tube 1
10. ET19
11. PH03 – level 2 N-Well
12. IM01 – 3E13, P^{31}, 170 KeV
13. ET07 – ash
14. PH03 – level 3 – p-well
15. IM01 – 8E13, B^{11}, 80 KeV
16. ET07 – ash
17. OX06 – Well Drive, Tube 1
18. PH03 – NMOS Vt
19. IM01 – 3E12, B^{11}, 30KeV
20. ET07 - ash
21. PH03 – level 5 – PMOS V_T adjust
22. IM01 – 1.75E12, B^{11}, 60 KeV
23. ET07 – ash
24. ET06 – etch 500 Å pad oxide
25. CL01 – pre-gate oxide RCA clean
26. ET06 – etch native oxide
27. OX06 – 100 Å gate oxide, Tube 4
28. CV01 – poly deposition, 4000 Å
29. PH03 – level 6 – poly gate
30. ET08 – poly gate plasma etch
31. ET07 – ash
32. CL01 – RCA clean
33. OX05 – poly re-ox, 500 Å, Tube 4
34. PH03 – level 7 - p-LDD
35. IM01 – 4E13, B^{11}, 50 KeV
36. ET07 – ash
37. PH03 – level 8 – n-LDD
38. IM01 – 4E13, P^{31}, 60 KeV
39. ET07 – ash
40. CL01 – RCA clean
41. CV02 – nitride spacer 3500Å
42. ET39 – sidewall spacer etch
43. PH03 – level 9 - N+D/S
44. IM01 – 4E15, P^{31}, 60 KeV
45. ET07 – ash
46. PH03 – level 10 - P+ D/S
47. IM01 – 4E15, B^{11}, 50 KeV
48. ET07 – ash
49. CL01 – RCA clean
50. OX08 – DS Anneal, Tube2,3
51. ET06 – Silicide pad ox etch
52. ME03 – HF dip & Ti Sputter
53. RT01 – RTP 1 min, 650C
54. ET11 – Unreacted Ti Etch
55. RT02 – RTP 1 min,800C
56. CV03 – TEOS, P-5000
57. PH03 – level 11 - CC
58. ET06 – CC etch
59. ET07 – ash
60. CL01 – RCA clean
61. ME01 – Aluminum
62. PH03 – level 12-metal
63. ET15 – plasma Al Etch
64. ET07 – ash
65. CV03 – TEOS
66. PH03 – Via
67. ET26 Via Etch
68. ME01 Al Deposition
69. PH03 – Metal 2
70. ET07 - Ash
72. SI01 – sinter
73. SEM1
74. TE01
75. TE02
76. TE03
77. TE04

L = 0.5 µm
V_{DD} = 3.0 V
V_{TN} = 0.75 V
V_{TP} = - 0.75V

(Revision 3-19-14)

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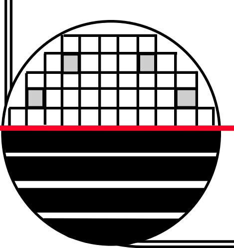
STARTING WAFER

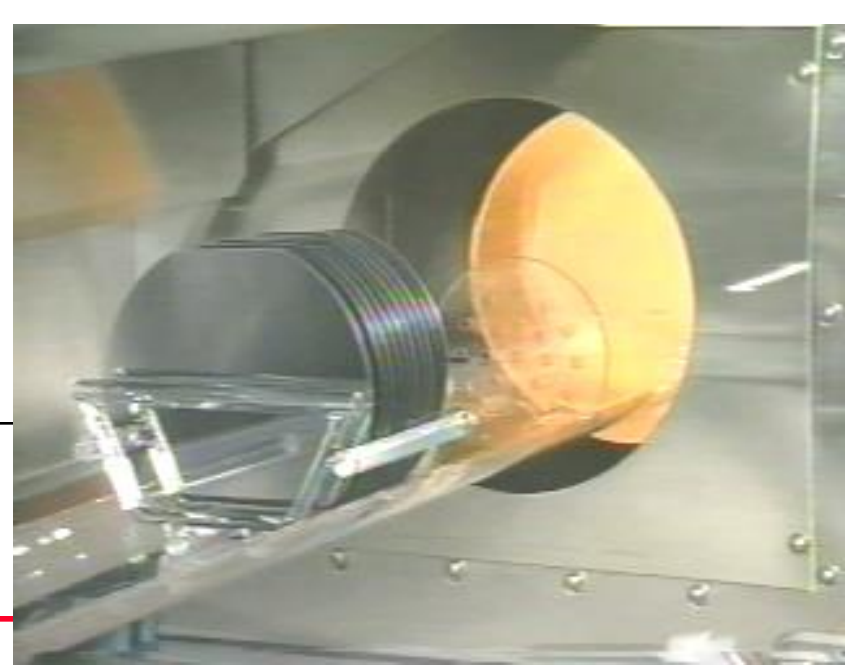
P-type Substrate 10 ohm-cm

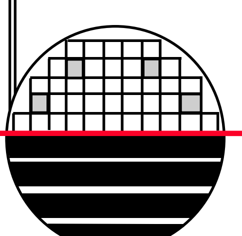


RCA CLEAN AND PAD OXIDE GROWTH

Pad Oxide, 500A
Bruce Furnace 04 Recipe 250
~45 min at 1000 °C

Substrate 10 ohm-cm





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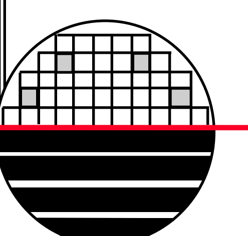
BRUCE FURNACE RECIPE 250 500Å DRY OXIDE

Recipe #250

	Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7
Step	Boat Out Load	Boat In Push	Stabilize	Ramp-Up	Soak	Anneal	Ramp-Down	Boat Out Pull
Temperature	25 °C	800 °C	800 °C		1000°C			800 °C
Time	Any	12 min	15 min	20 min	40min	5min	40 min	12 min
Flow	0 lpm	10 lpm	10 lpm	5 lpm	10 lpm	15 lpm	10 lpm	5 lpm
Gas	none	N2	N2	O2	O2	N2	N2	N2

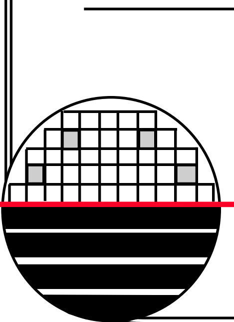
At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.



DEPOSIT SILICON NITRIDE

Recipe Nitride 810
Nitride, 1500A
LPCVD, 810C, ~30min

Substrate 10 ohm-cm



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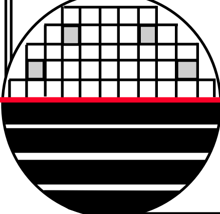
LEVEL 1 PHOTO - STI

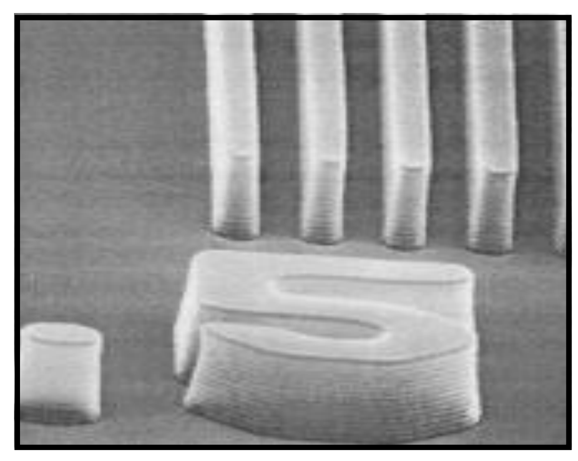
Substrate 10 ohm-cm

SSI COAT AND DEVELOP TRACK FOR 6" WAFERS

SSI coat and develop track



ASML 5500/200



NA = 0.48 to 0.60 variable
σ= 0.35 to 0.85 variable
With Variable Kohler, or
Variable Annular illumination
Resolution = K1 λ/NA
= ~ 0.35µm
for NA=0.6, σ =0.85
Depth of Focus = $k_2\ \lambda/(NA)^2$
= > 1.0 µm for NA = 0.6

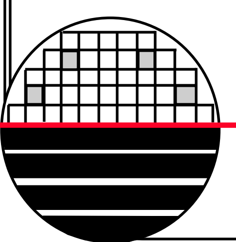
i-Line Stepper λ = 365 nm
22 x 27 mm Field Size

PLASMA ETCH NITRIDE/OXIDE/SILICON

STI Etch: SF_6 plasma

LAM 490 Etcher, Etch Rate ~1000 Å/min for Nitride
~ 500 Å/min for Oxide
~ 5000 Å/min for silicon

Substrate 10 ohm-cm



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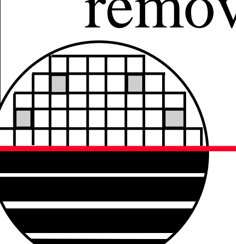
PLASMA ETCH TOOL

Lam 490 Etch Tool
Plasma Etch Nitride (~ 1500 Å/min)
SF6 flow = 200 sccm
Pressure= 260 mTorr
Power = 125 watts
Time=thickness/rate

Use end point detection capability
This system has filters at 520 nm (Channel 12) and 470 nm (Channel 13). In any case the color of the plasma goes from pink/blue to white/blue once the nitride is removed.



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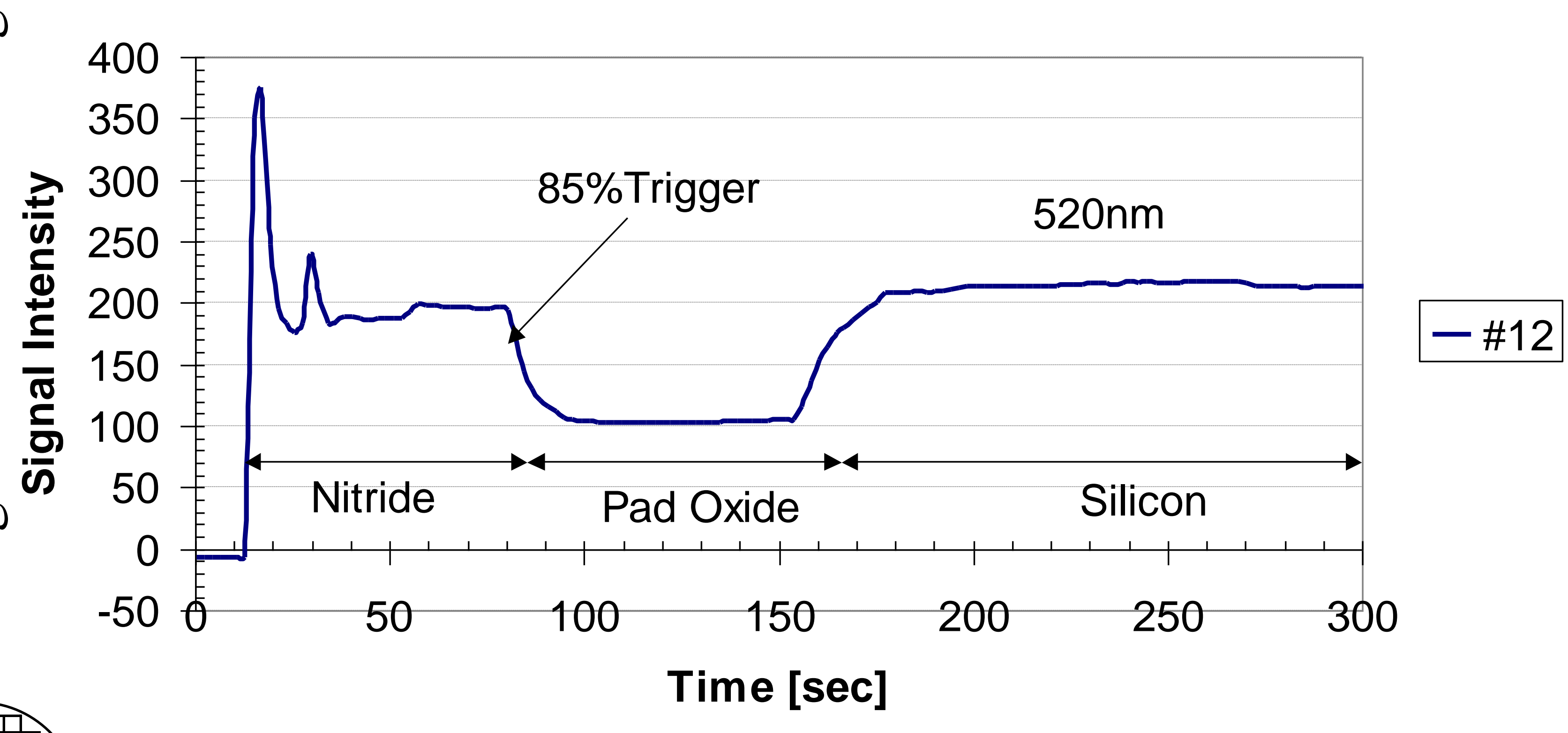
LAM 490 END POINT



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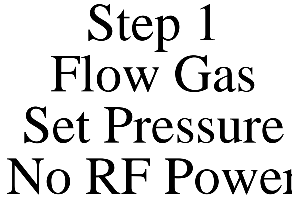
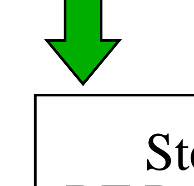
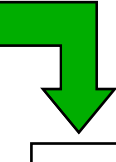
APPROACH FOR STI END POINT DETECTION

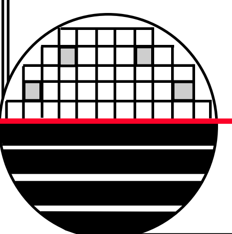




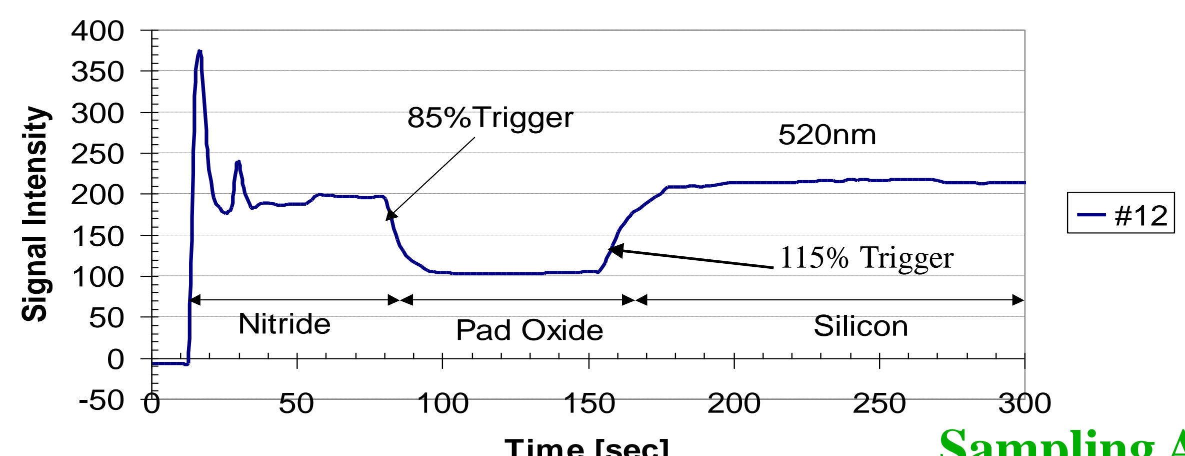
Step 3
RF Power On
Oxide
Endpoint



Step 3
RF Power On
Timed
Silicon Etch



SELECTING LAM 490 END POINT PARAMETERS



Nitride Etch (Step 2)
If no Endpoint is found then
Max Etch Time 100 sec

Sampling A only [520nm ch 12]
Active during Step 2
Delay 50 sec before normalizing
Normalize for 10 sec
Trigger @ 85% of normalized value

Oxide Etch (Step 3)
If no Endpoint is found then
Max Etch Time 50 sec

Sampling A only [520nm ch 12]
Active during Step 3
Delay 30 sec before normalizing
Normalize for 10 sec
Trigger @ 115% of normalized value

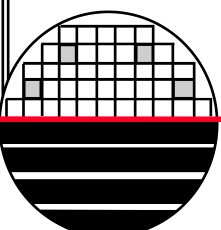
FINALIZE STI ETCH RECIPE

Process: Step 1 –
260mTorr; 0 watts
200sccm SF_6,
Max Time = 2 min
Time Only

Process: Step 2 –
260mTorr; 125 watts,
200sccm SF_6,
Max Time = 1min 40sec
Endpoint and Time
Sampling A (ch12 @ 520nm)
Active during step 02
Delay 50sec before normalizing
Normalize for 10sec
Trigger at 85%

Process: Step 3 –
260mTorr; 125 watts,
200sccm SF_6,
Max Time = 50sec
Endpoint and Time
Sampling A (ch12 @ 520nm)
Active during step 03
Delay 30sec before normalizing
Normalize for 10sec
Trigger at 115%

Process: Step 4 –
260mTorr; 125W,
200sccm SF_6,
Time Only,
Max Time = 50 sec



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CONTINUE THE ETCH THRU PAD OXIDE AND INTO THE SILICON

Substrate 10 ohm-cm

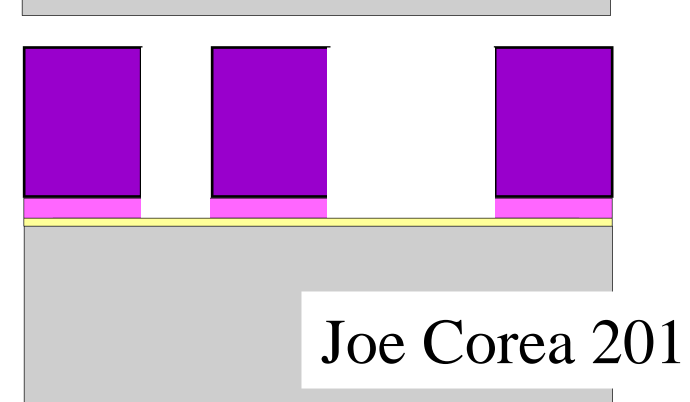
MEGASONIC RCA CLEAN, SRD & ASHER

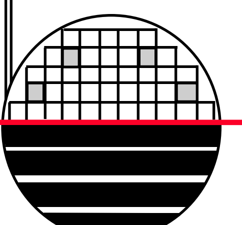
RCA Clean Bench

Asher

RECESSED OXIDE GROWTH PROCESS FLOW

- Grow 500A Pad Oxide (thermal)
- Deposit 1500A Si3N4 by LPCVD
- Level 1 Lithography to protect Active areas with photoresist
- Etch Nitride (Plasma)





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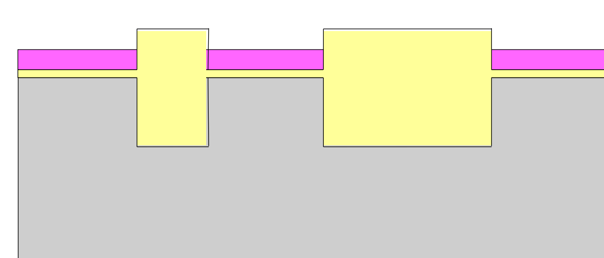
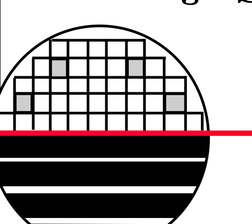
RECESSED OXIED GROWTH PROCESS FLOW

- Remove Photo Resist
- Grow First oxide (Thermal) 3650 Å



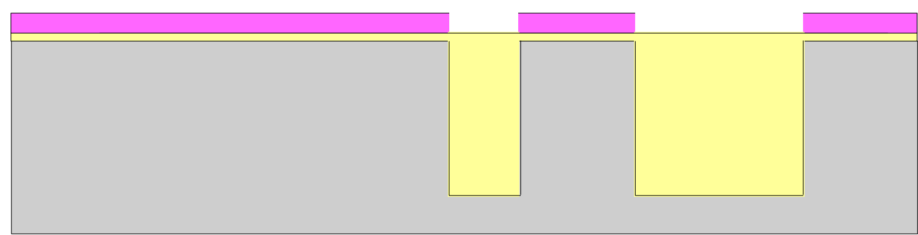
- Strip First oxide (Wet)

Joe Corea 2011



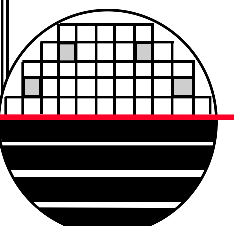
RECESSED OXIDE GROWTH PROCESS FLOW

§ **Grow second Oxide (Thermal) also 3650 Å**



Final oxide growth will give correct depth and thickness to achieve a phase shift, meet the previous pad oxide, and satisfy isolation criteria.

Joe Corea 2011



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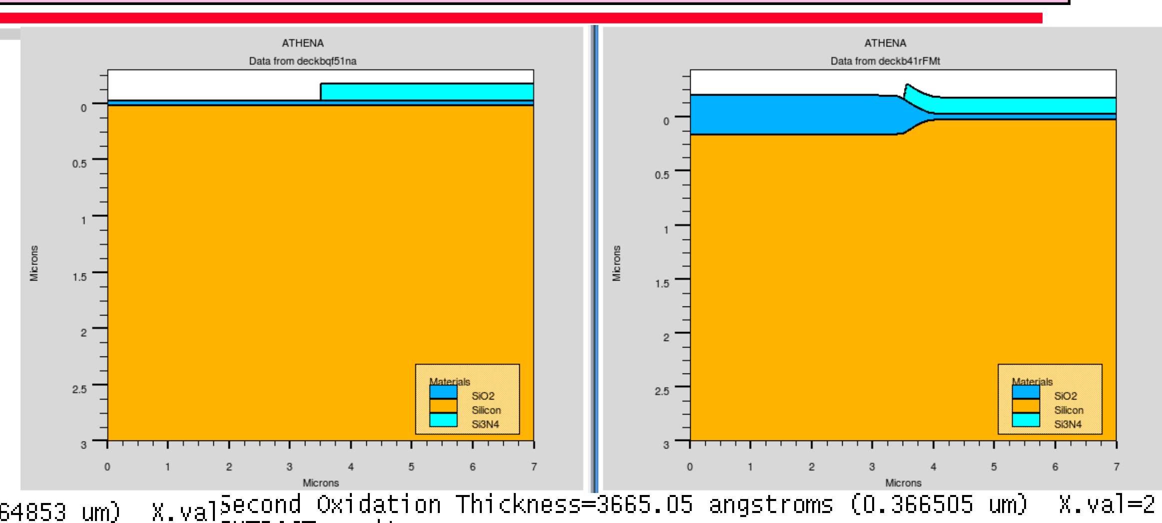
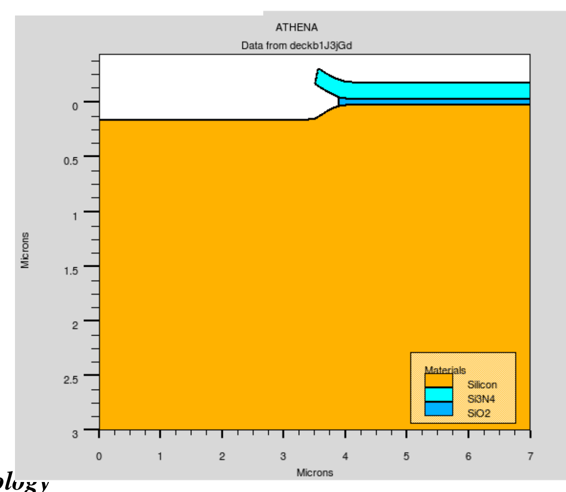
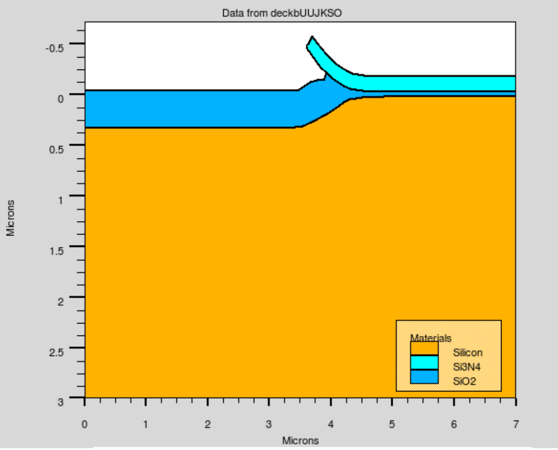
RECESSED OXIDE GROWTH SIMULATION

Simulation Output was analyzed and determined to be correct




```
First Oxidation Thickness=3648.53 angstroms (0.364853 um)  X.val
EXTRACT> quit
```





Joe Corea 2011

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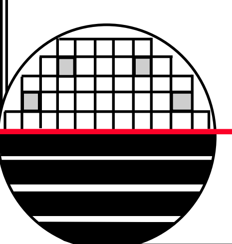
HOT PHOSPHORIC ACID NITRIDE ETCH

30s Dip in 5:1 BHF, Rinse
Hot Phosphoric Acid
Wet Nitride Etch.
Etch Rate ~80 Å/min
Etch ~20 min.

P-well

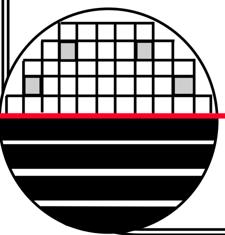
N-well

Substrate 10 ohm-cm



HOT PHOSPHORIC ACID ETCH BENCH

- Include D1-D3
- Warm up Hot Phos pot to 175º
- Use Teflon boat to place wafers in acid bath
    - Etch rate of ~80 Å/min
- Rinse for 5 minutes in Cascade Rinse
- SRD wafers



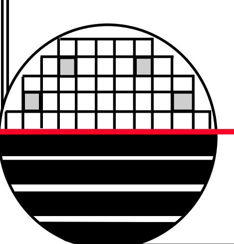
WELL DRIVE

6 hrs, 1100 °C

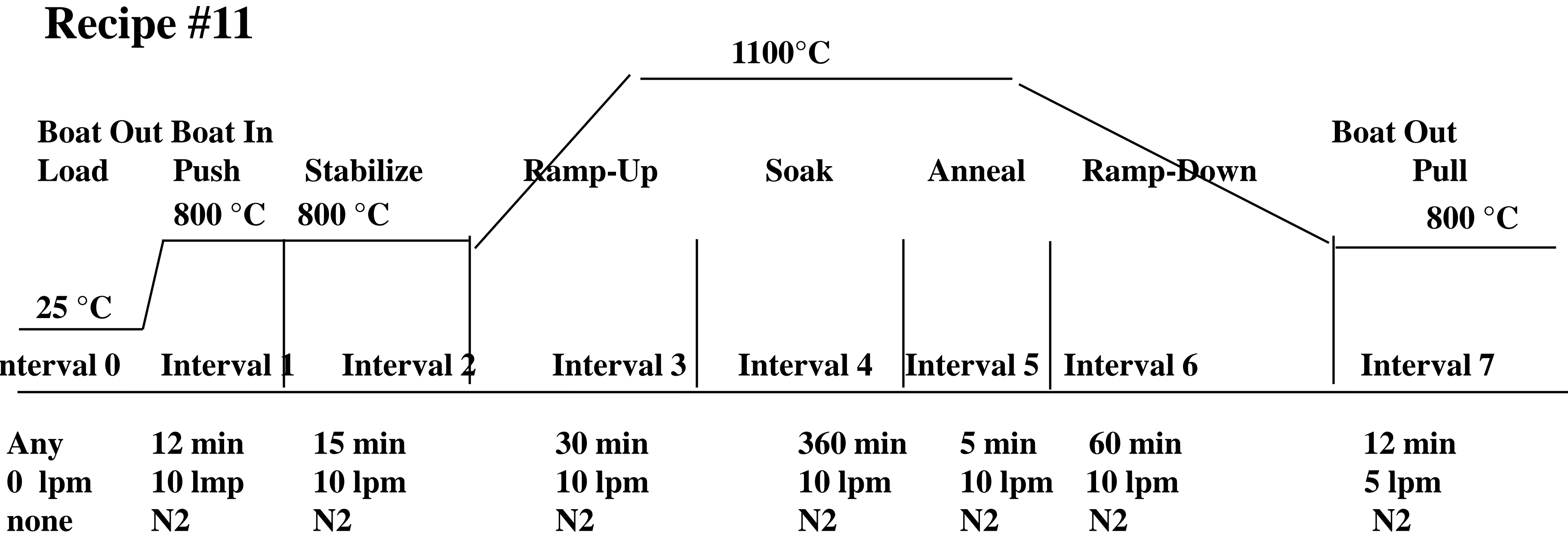
P-well

N-well

Substrate 10 ohm-cm



BRUCE FURNACE RECIPE 11 ADV-CMOS WELL DRIVE



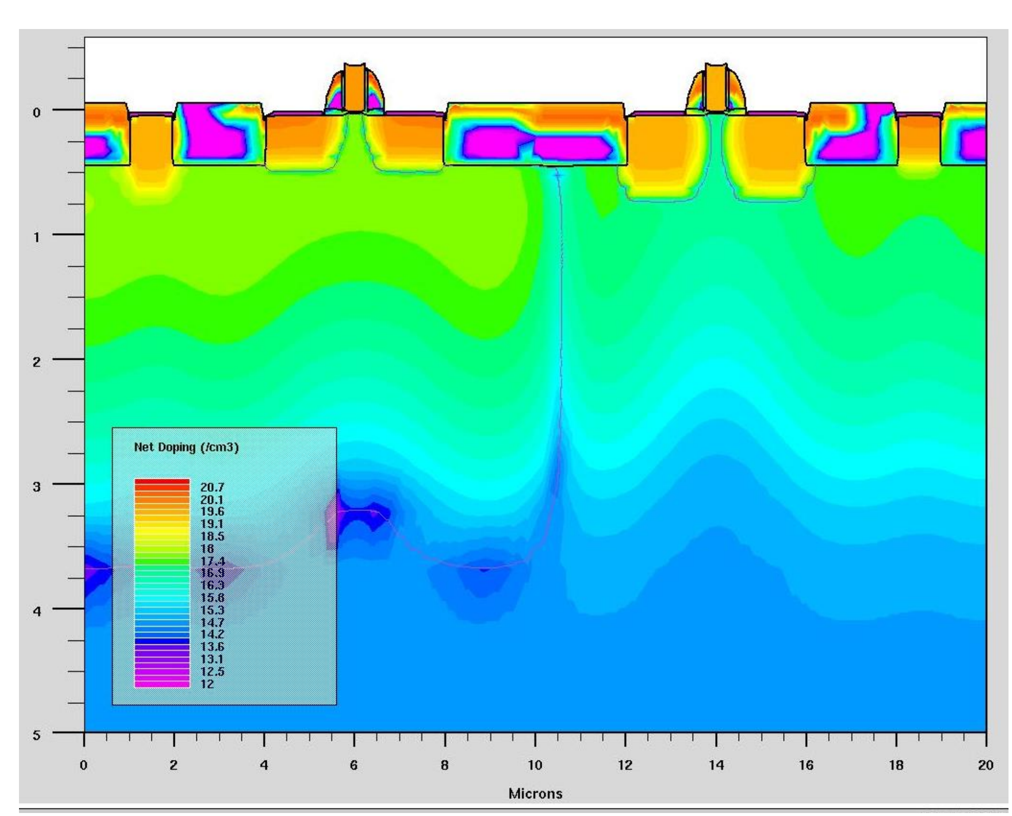
At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

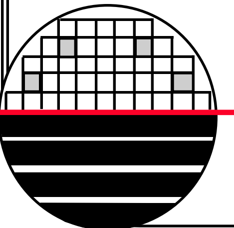
Adv-CMOS Well Drive, No Oxide Growth, Tube 1

CALCULATION OF NMOS AND PMOS VT ADJUST

Calculate using:

1. Hand Calculations
2. Silvaco Supreme (Athena)





Michael Latham, May 2005

NMOS CALCULATION

ROCHESTER INSTITUTE OF TECHNOLOGY MOSFETVT.XLS FILE3B
MICROELECTRONIC ENGINEERING 12/28/1995

CALCULATION OF MOSFET THRESHOLD VOLTAGE LYNN FULLER

To use this spreadsheet change the values in the white boxes. The rest of the sheet is protected and should not be changed unless you are sure of the consequences. The calculated results are shown in the purple boxes.

CONSTANTS			VARIABLES			CHOICES	1=yes, 0=No	
T=	300	K	Na =	1.00E+17	cm-3	Aluminum gate	0	Select one type of gate
KT/q =	0.026	volts	Nd =	1.00E+17	cm-3	n+ Poly gate	1	
ni =	1.45E+10	cm-3	Nss =	1.00E+11	cm-2	p+ Poly gate	0	
Eo =	8.85E-14	F/cm	Xox =	100	Ang	N substrate	0	Select one type of substrate
Er si =	11.7					P substrate	1	
Er SiO2 =	3.9							
E affinity =	4.15	volts				Desired VT	0.75	
q =	1.60E-19	coul				or		
Eg =	1.124	volts				Delta VT	20	
						Given Dose (Boron)	1.30E+12	

CALCULATIONS:		RESULTS				
METAL WORK FUNCTION	=	4.122988528	volts			
SEMICONDUCTOR POTENTIAL	= +/-	0.409409834	volts			
OXIDE CAPACITANCE / CM2	=	3.4515E-07	F/cm2	Wdmax =	0.103	µm
METAL SEMI WORK FUNCTION DIFF	=	-0.998421306	volts			
FLAT BAND VOLTAGE	=	-1.044777963	volts			
THRESHOLD VOLTAGE	=	0.25126959	volts			
DELTA VT = VTdesired - VT	=	0.49873041	volts			
IMPLANT DOSE	=	1.07586E+12	ions/cm2	x 2 =	2.15171E+12	

where + is Boron, - is Phosphorous

PMOS CALCULATION

ROCHESTER INSTITUTE OF TECHNOLOGY MOSFETVT.XLS FILE3B
MICROELECTRONIC ENGINEERING 12/28/1995

CALCULATION OF MOSFET THRESHOLD VOLTAGE LYNN FULLER

To use this spreadsheet change the values in the white boxes. The rest of the sheet is protected and should not be changed unless you are sure of the consequences. The calculated results are shown in the purple boxes.

CONSTANTS			VARIABLES			CHOICES	1=yes, 0=No
T=	300	K	Na =	1.00E+17	cm-3	Aluminum gate	0
KT/q =	0.026	volts	Nd =	1.00E+17	cm-3	n+ Poly gate	0
ni =	1.45E+10	cm-3	Nss =	1.00E+11	cm-2	p+ Poly gate	1
Eo =	8.85E-14	F/cm	Xox =	100	Ang	N substrate	1
Er si =	11.7					P substrate	0
Er SiO2 =	3.9						
E affinity =	4.15	volts				Desired VT	-0.75
q =	1.60E-19	coul				or	
Eg =	1.124	volts				Delta VT	20
						Given Dose (Boron)	1.30E+12

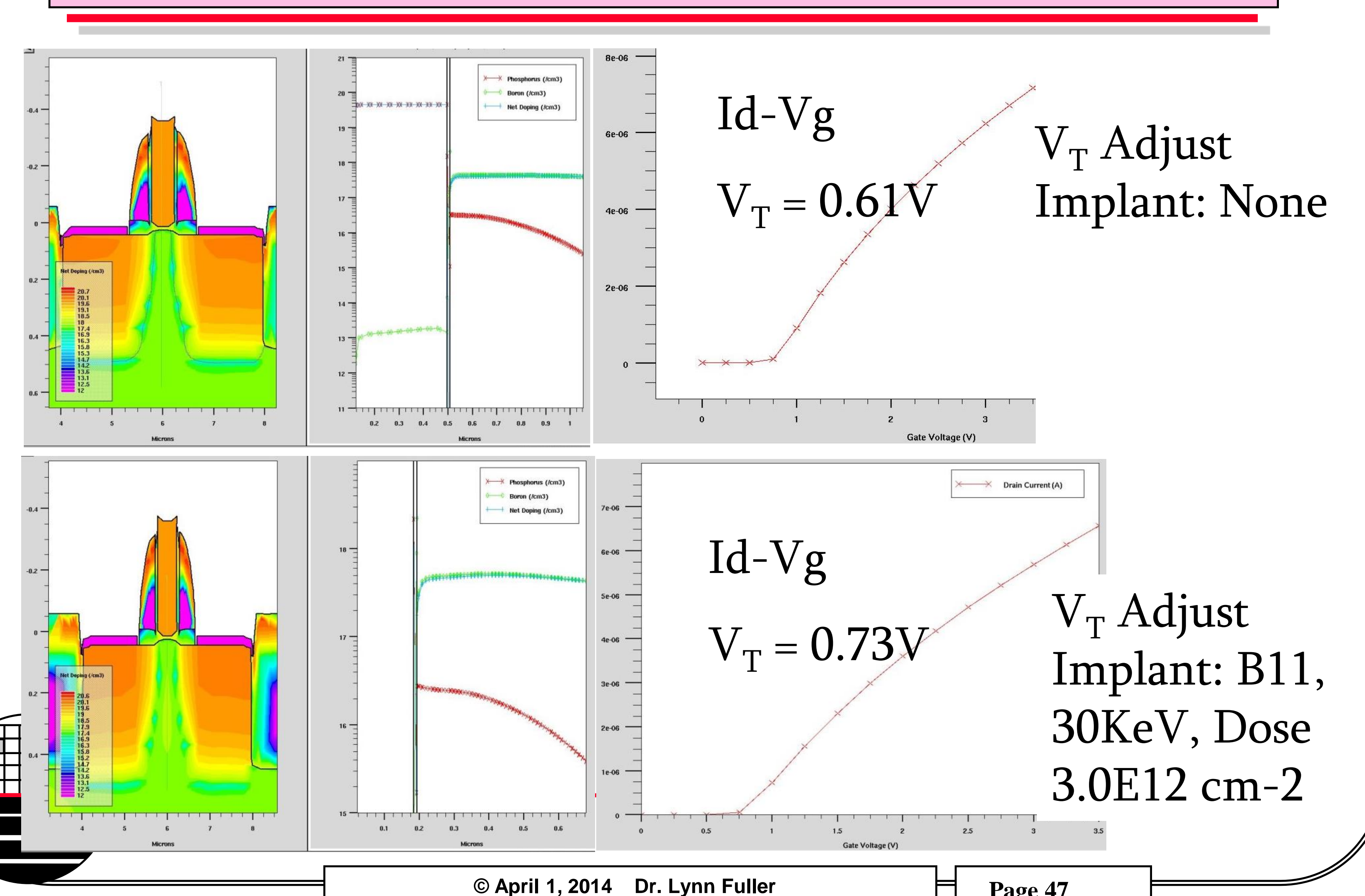
Aluminum gate / n+ Poly gate / p+ Poly gate: Select one type of gate

N substrate / P substrate: Select one type of substrate

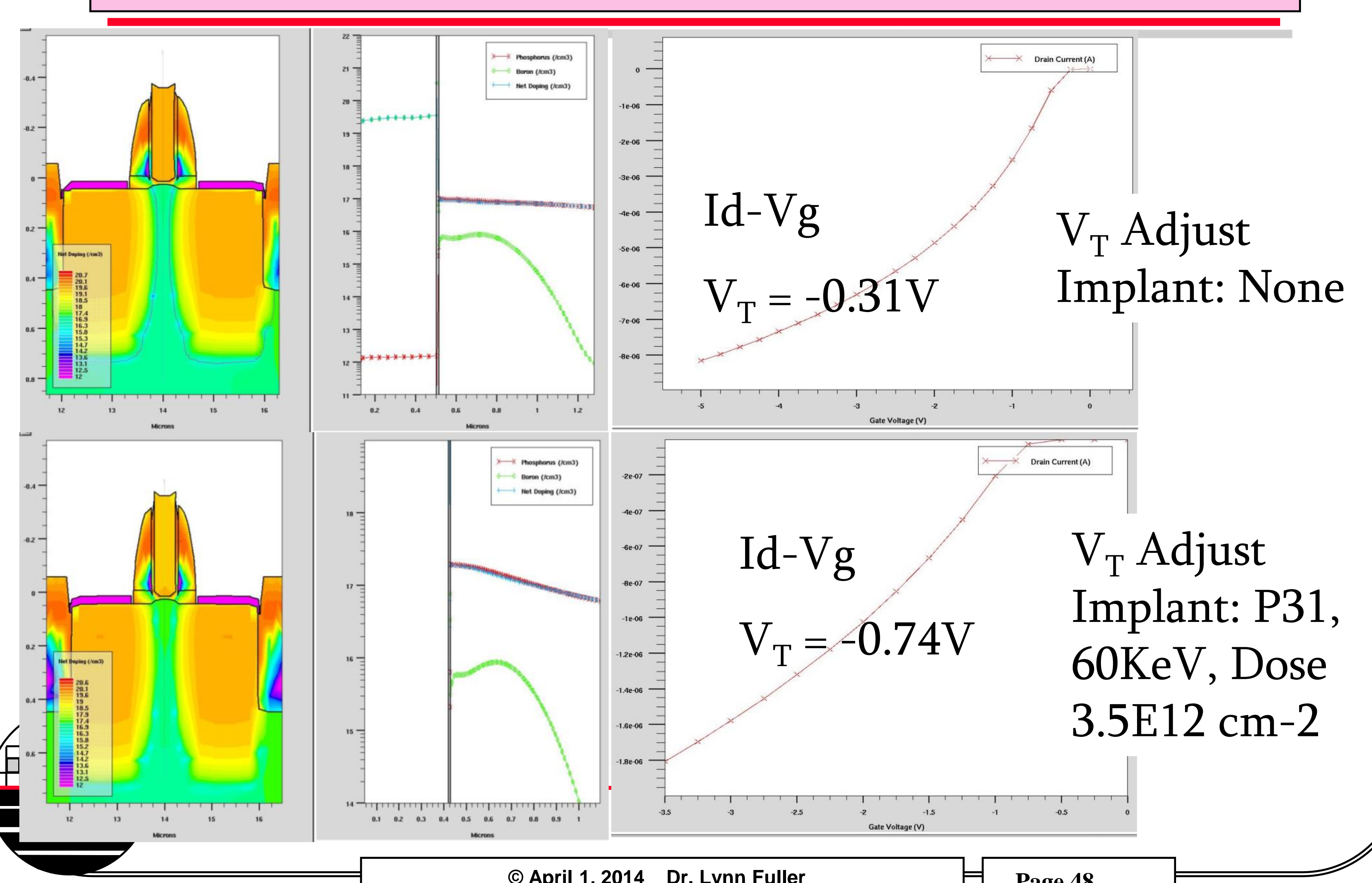
CALCULATIONS:		RESULTS				
METAL WORK FUNCTION	=	5.301011472	volts			
SEMICONDUCTOR POTENTIAL	= +/-	0.409409834	volts			
OXIDE CAPACITANCE / CM2	=	3.4515E-07	F/cm2	Wdmax =	0.103	µm
METAL SEMI WORK FUNCTION DIFF	=	0.998421306	volts			
FLAT BAND VOLTAGE	=	0.95206465	volts			
THRESHOLD VOLTAGE	=	-0.343982903	volts			
DELTA VT = VTdesired - VT	=	-0.406017097	volts			
IMPLANT DOSE	=	-8.75855E+11	ions/cm2	x 2 =	-1.75171E+12	

where + is Boron, - is Phosphorous

NMOS SIMULATIONS



PMOS SIMULATIONS



RESULTS OF CALCULATIONS AND SIMULATIONS

NMOS Desired 0.75, with No Adjust 0.61

From SUPREM 3.0E12 @30 KeV Boron B11

From Hand Calculations 2.15E12

PMOS Desired -0.75, with No Adjust -0.31

From SUPREM 3.5E12 @ 60KeV Phosphorous P31

From Hand Calculations 1.8E12

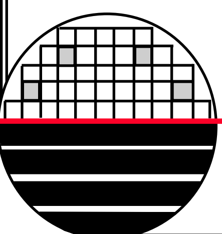


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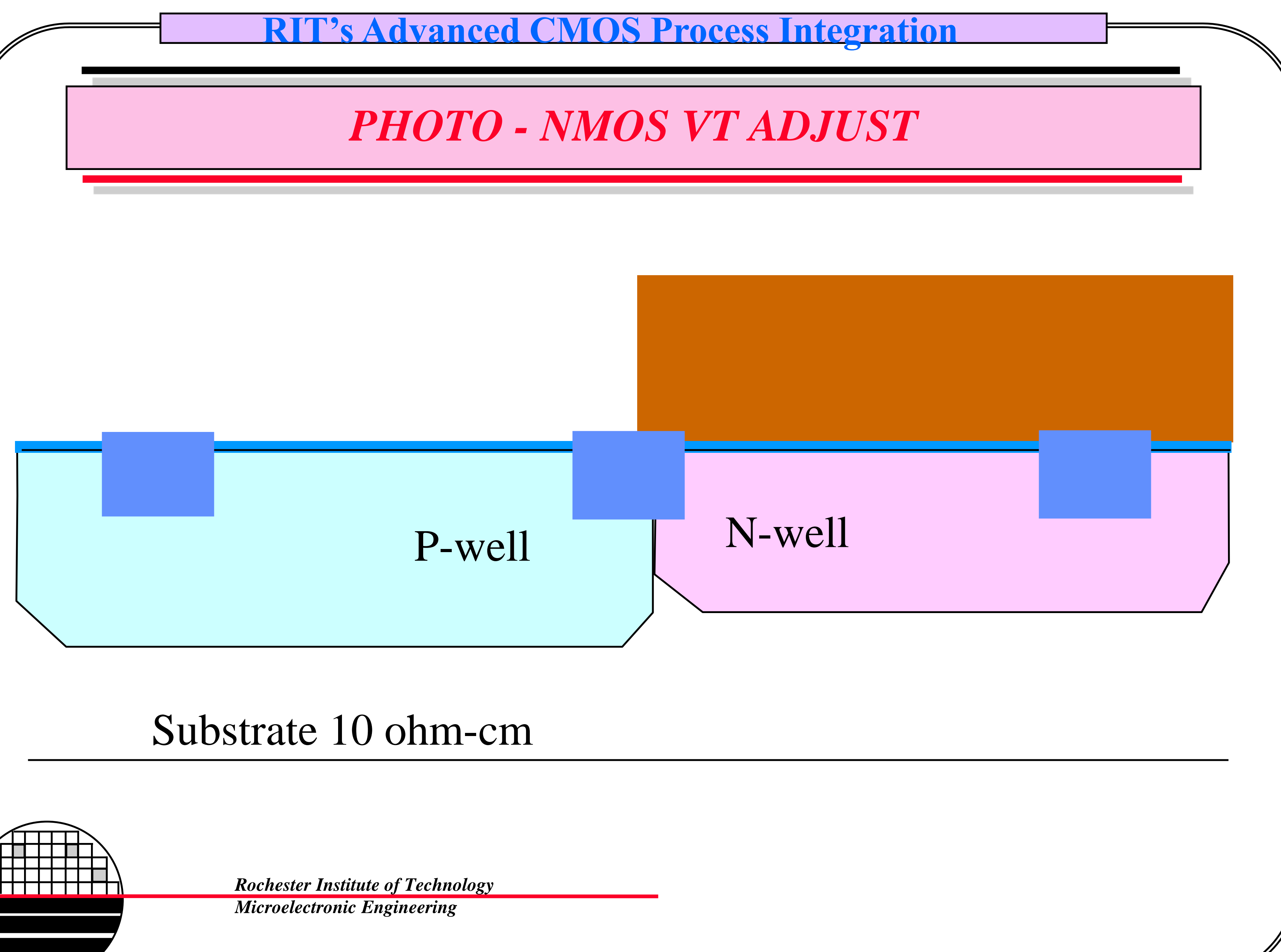
PHOTO - NMOS VT ADJUST



NMOS VT ADJUST IMPLANT

3.0e12, 30keV, B_{11}

P-well

N-well

Substrate 10 ohm-cm

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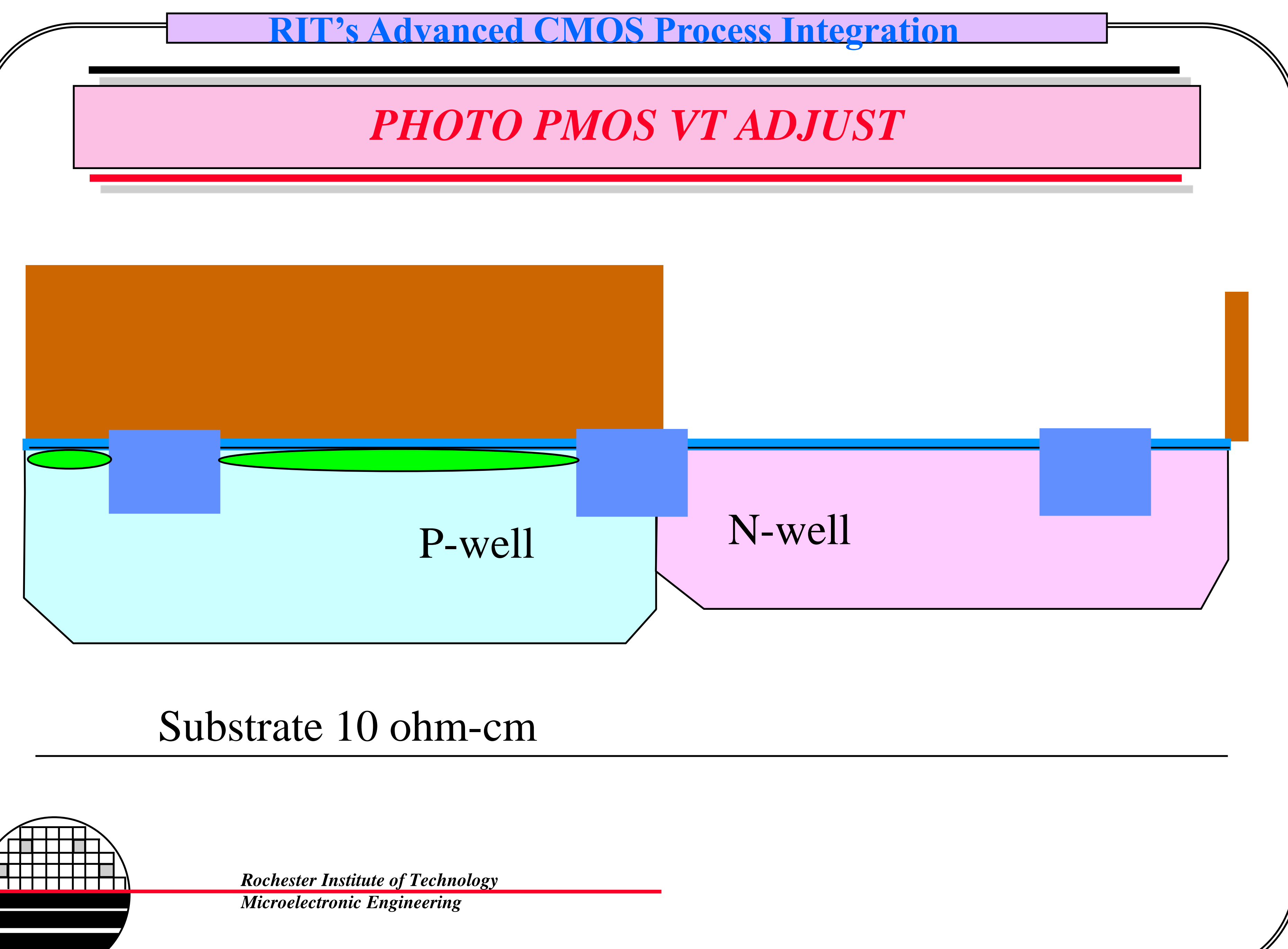
PHOTO PMOS VT ADJUST



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PMOS VT IMPLANT

3.5E12, 60keV, P_{31}

P-well

N-well

Substrate 10 ohm-cm

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STRIP RESIST

P-well

N-well

Substrate 10 ohm-cm

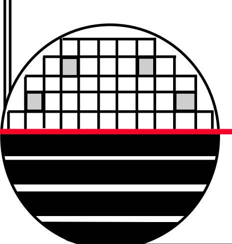
OXIDE ETCH

Etch in 10:1 BOE
45 seconds, Rinse, SRD

P-well

N-well

Substrate 10 ohm-cm



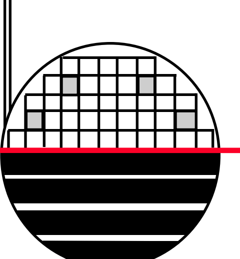
RCA CLEAN AND GROW GATE OXIDE

Just Prior to Gate Oxide Growth
Etch wafers in 50:1 HF, 1 min.
Grow Oxide, 100Å, Dry O_2
Bruce Furnace04 Recipe 213

P-well

N-well

Substrate 10 ohm-cm



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INCORPORATING NITROGEN IN THIN GATE OXIDES

In todays deep sub-micron transistors the pMOSFET normally has p+Poly for the gate material. The gate oxide is 100Å or less. The p+ dopant is normally Boron and Boron diffuses quickly (compared to Phosphorous) through oxides. Since the gate oxides are thin this could allow Boron to diffuse through the gate oxide and dope the channel causing the transistors to not function correctly. If some nitrogen is incorporated in the gate oxide the diffusion of Boron is much lower. This project involved developing a gate oxide recipe that will result in nitrogen incorporation in the gate oxide. The recipe included 30 min anneal in N2, 30 min oxynitride growth in N2O and 30 min oxide growth in O2, all at 900 °C. The gate oxides were evaluated at RIT using the ellipsometer (looking for index of refraction in between 1.45 (oxide) and 2.00 (nitride) and thickness near 100Å. The same wafers were also sent to Kodak for XPS analysis to give information on nitrogen content in the oxide.

BRUCE FURNACE RECIPE 213

Recipe #213

	Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7
Step	Boat Out Load	Boat In Push	Stabilize	Ramp-Up	Soak	Soak	Ramp-Down	Boat Out Pull
Temperature	25 °C	800 °C	800 °C		900°C			800 °C
Time	Any	12 min	30 min	30 min	30min	30 min	30 min	15 min
Flow	0 lpm	5 lpm	5 lmp	10 lpm	10 lpm	10 lpm	10 lpm	5 lpm
Gas	none	N2	N2	O2	N2O	O2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

Dry Oxide Growth with N2O, Target 100 Å

INCORPORATING NITROGEN IN THIN GATE OXIDES

XPS Compositional Depth Profiles of SiO_XN_Y

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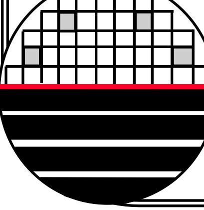
LOCATION FOR MEASUREMENT OF GATE OXIDE

Measure gate oxide thickness (~100A) in any white active area



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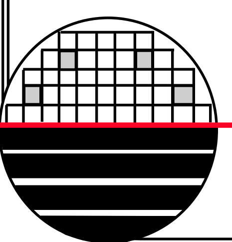
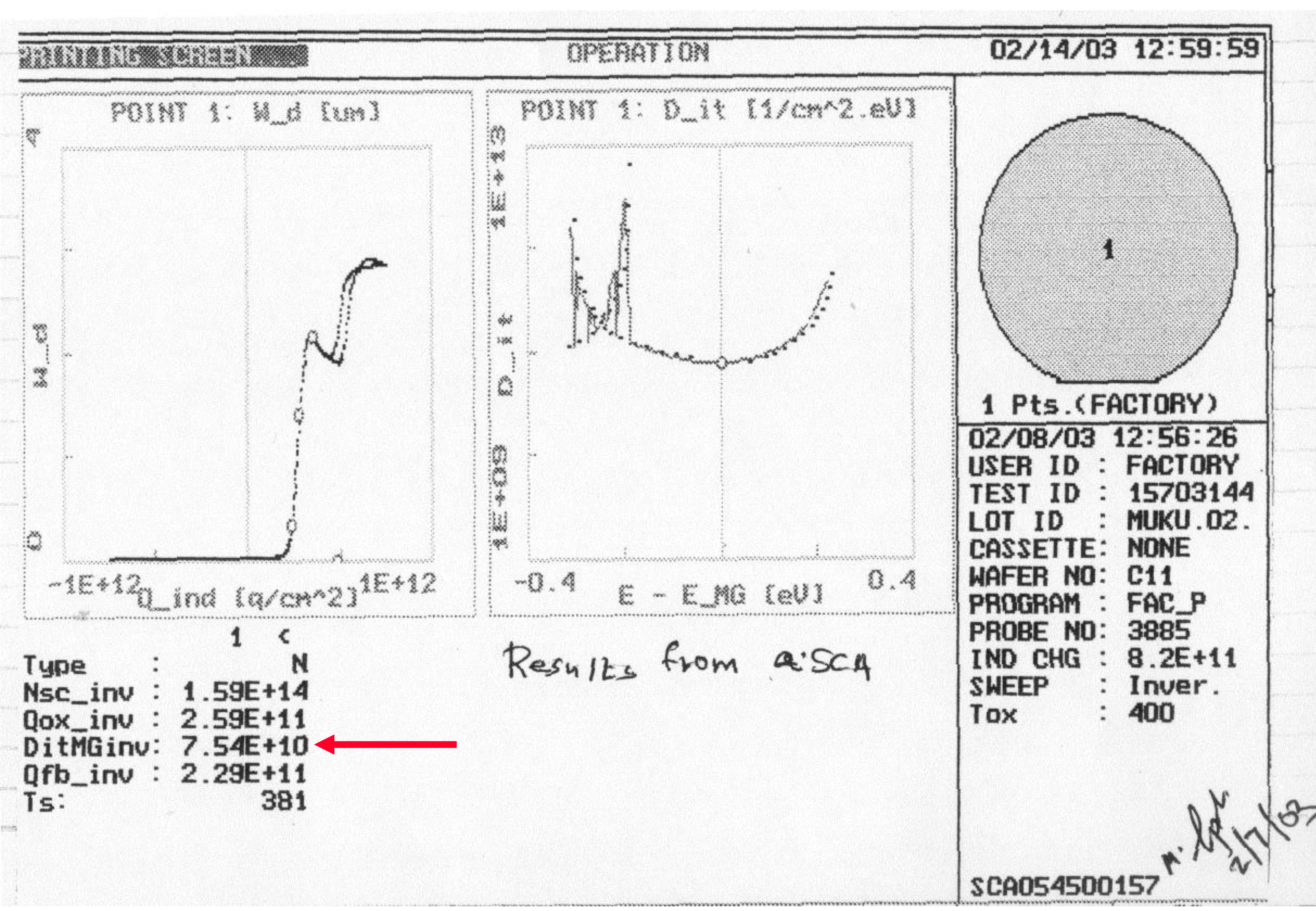
MEASURE GATE OXIDE ON SCA-2500

Login: FACTORY
Password: OPER
<F1> Operate
<F1> Test Center the wafer on the stage
Select (use arrow keys on the numeric pad (far right on the keyboard)
space bar, page up, etc)
PROGRAM = FAC-P or FAC-N
LOT ID = HAWAII
WAFER NO. = C1
TOX = 250 (from nanospec)
<F12> start test and wait for measurement
<Print Screen> print results
<F8> exit and log off
<ESC> can be used anytime, but wait for
current test to be completed



SCA MEASUREMENT OF GATE OXIDE



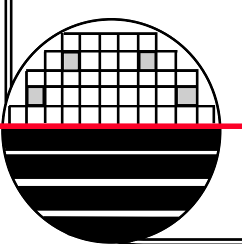
LPCVD POLY

Polysilicon, 4000A
LPCVD, 610C, ~55min
100 sccm of SiH4, 300 mTorr

P-well

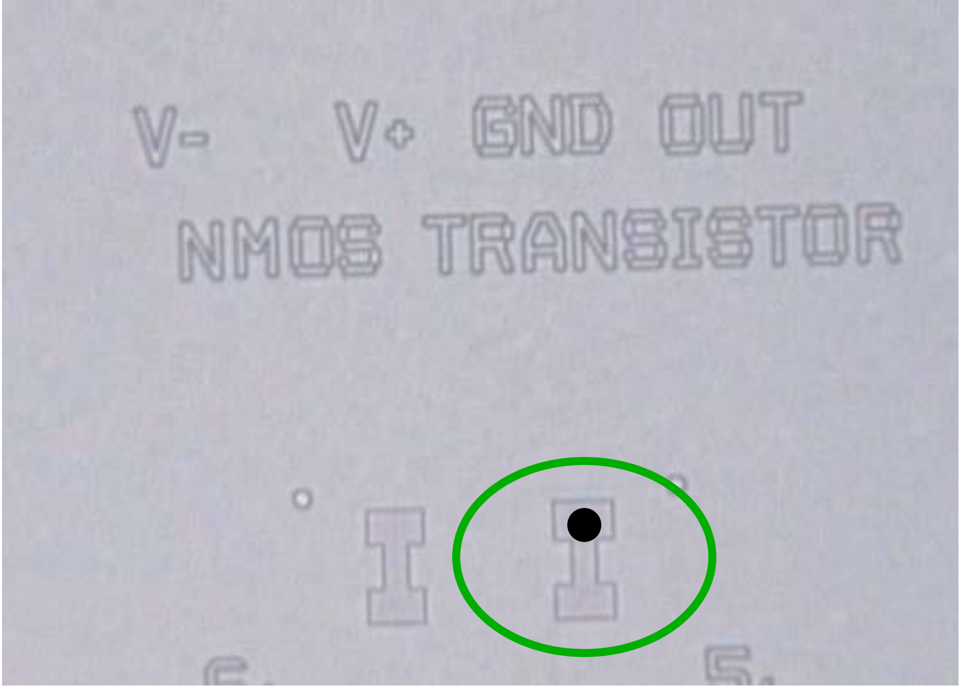
N-well

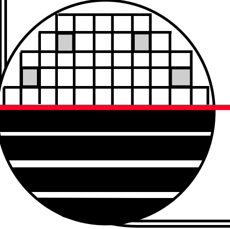
Substrate 10 ohm-cm

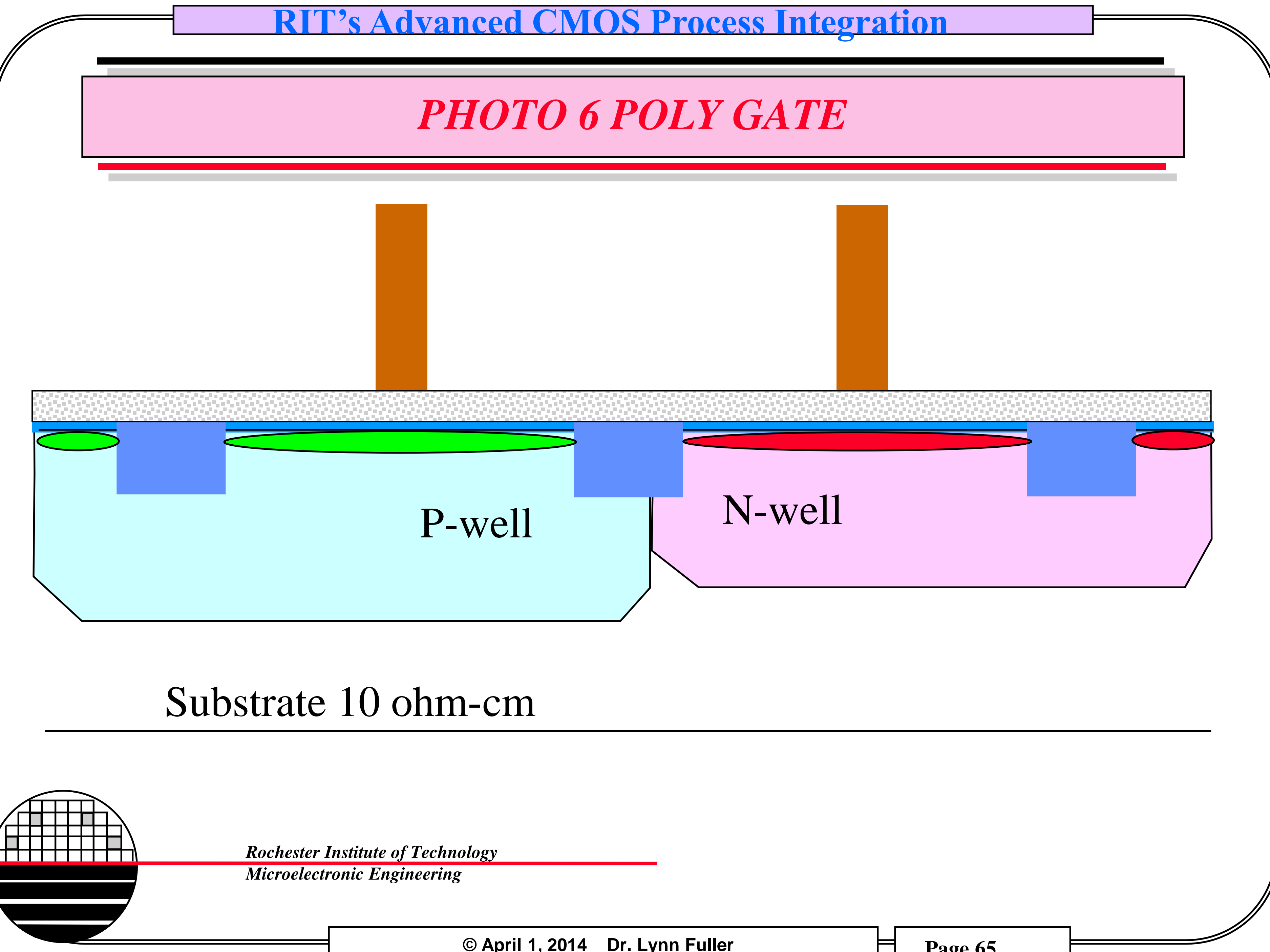


LOCATION FOR POLY THICKNESS MEASUREMENT

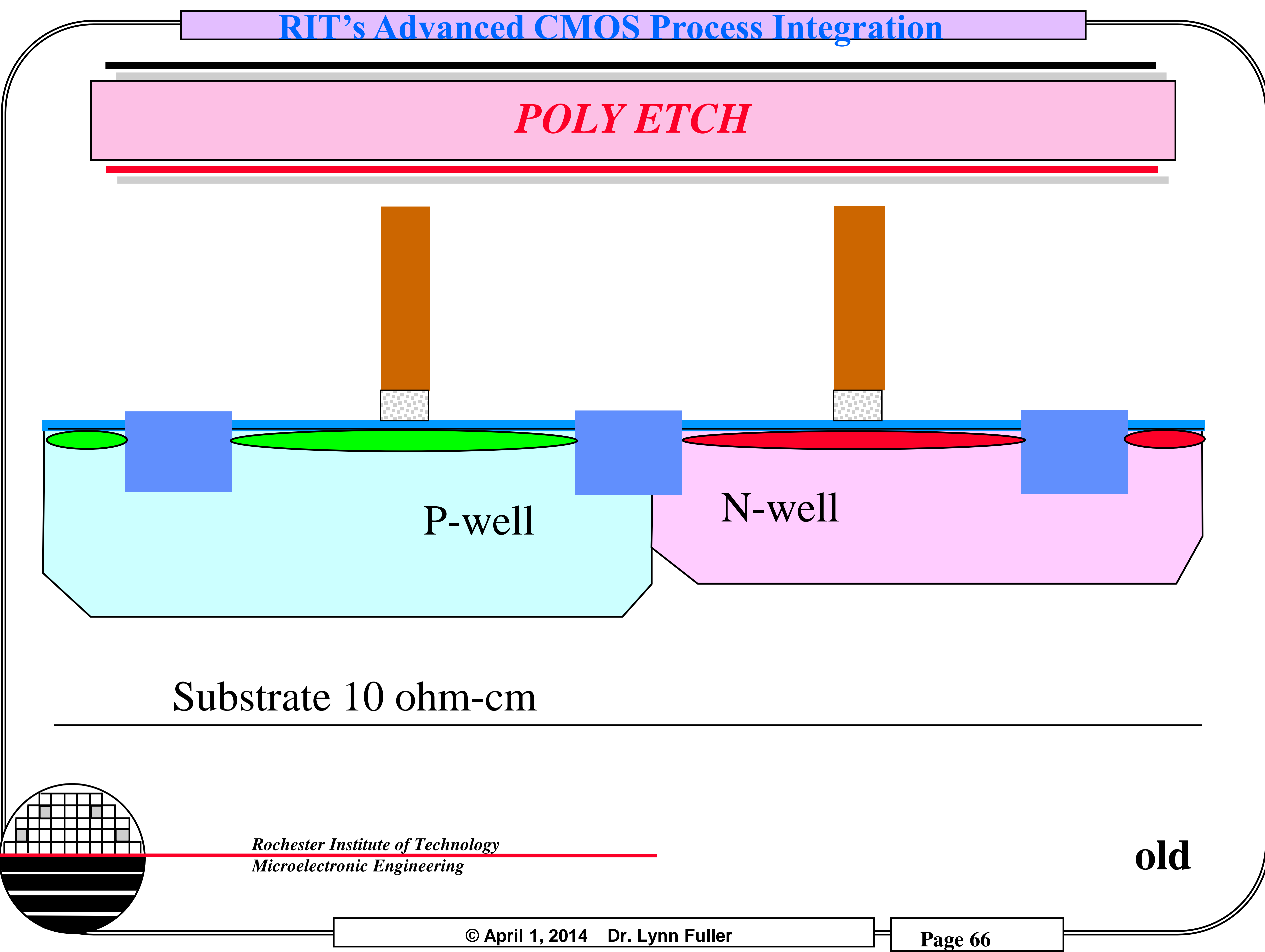
Measure poly thickness within any active area using thin film stack #4 on nanospec at 40X magnification






RIT's Advanced CMOS Process Integration
PHOTO 6 POLY GATE
P-well
N-well
Substrate 10 ohm-cm
Rochester Institute of Technology
Microelectronic Engineering
© April 1, 2014 Dr. Lynn Fuller
Page 65

POLY ETCH



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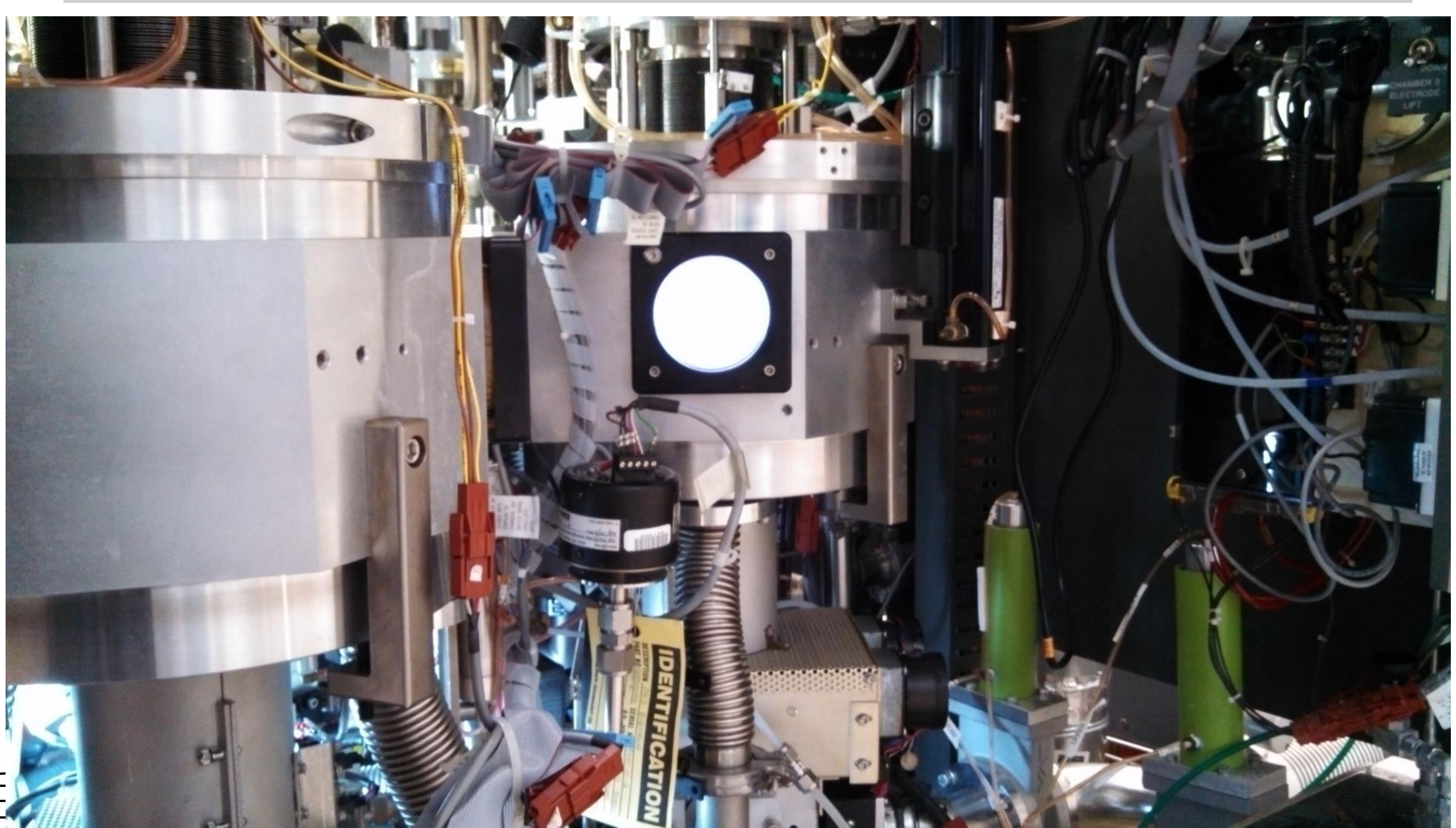
DRYTEK QUAD RIE TOOL

2 OF 4 CHAMBERS IN THE DRYTEK QUAD RIE TOOL



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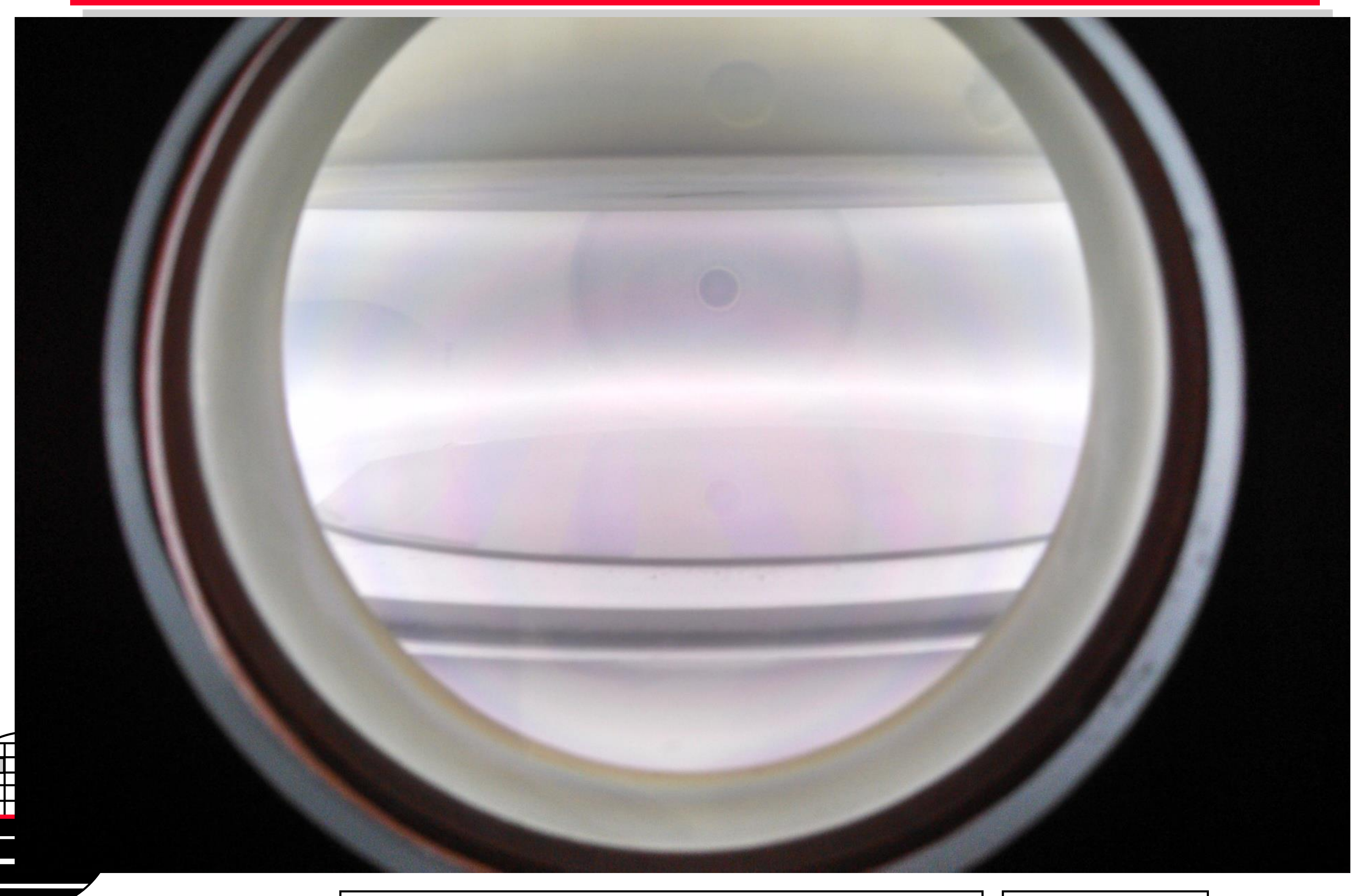
PLASMA ETCHING IN THE DRYTEK QUAD



ANISOTROPIC POLY GATE ETCH RECIPE

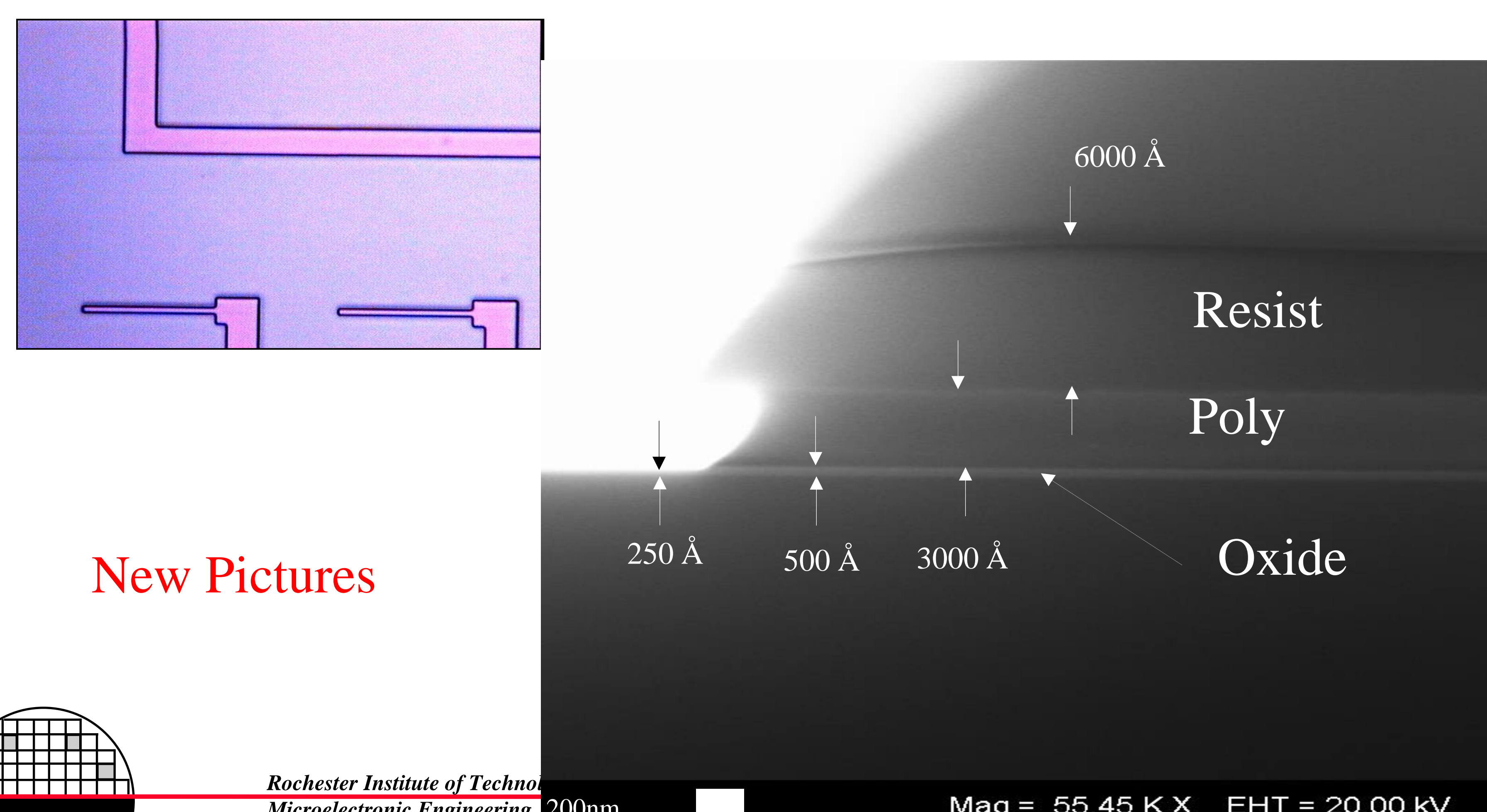
Anisotropic Poly Gate Etch Recipe

SF6 30 sccm, CHF3 30 sccm, O2 5 sccm, RF Power 160 w, Pressure 40 mTorr, 1900 A/min (Anisotropic), Resist Etch Rate 300 A/min, Oxide Etch Rate 200 A/min

Recipe Name:	FACPOLY Step 2
Chamber	2
Power	160 watts
Pressure	40 mTorr
Gas	SF6
Flow	30 sccm
Gas	CHF3
Flow	30 sccm
Gas	O2
Flow	5 sccm
Poly Etch Rate	1150 Å/min
Photoresist Etch Rate:	300 Å/min
Oxide Etch Rate:	200 Å/min

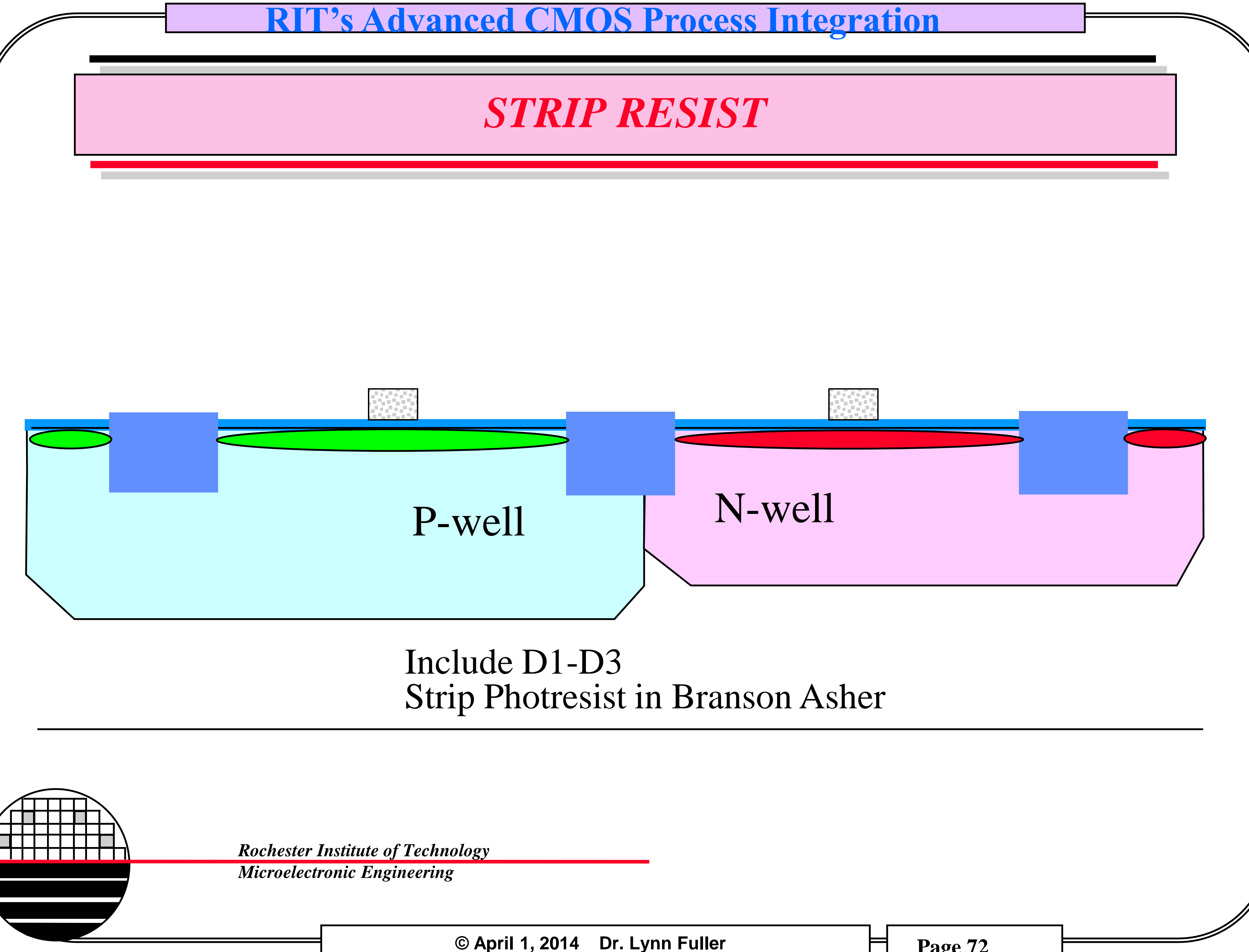
Endpoint See Video
http://people.rit.edu/lffeee/videos.htm

VERIFICATION



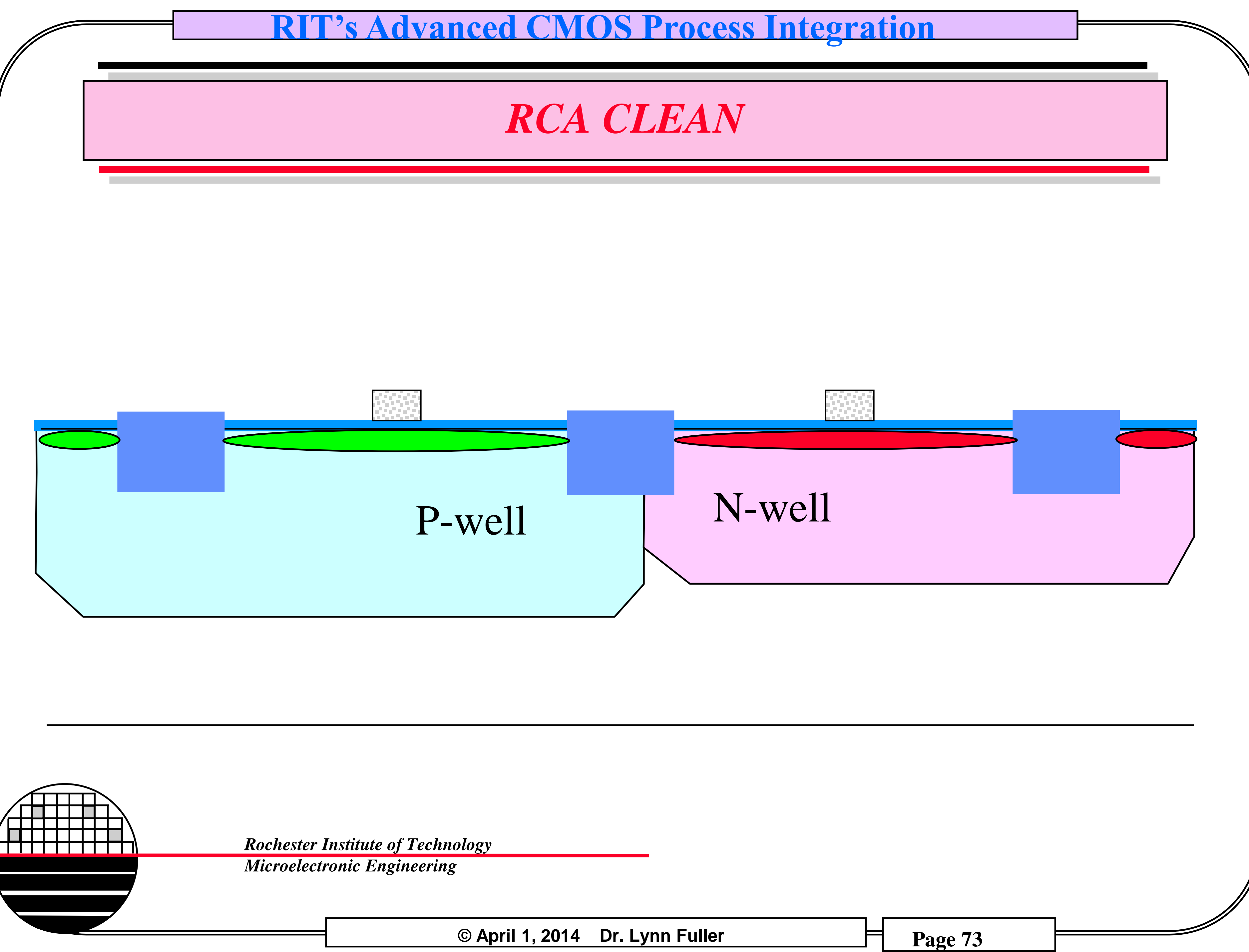
New Pictures

STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

RCA CLEAN



POLY REOX OXIDE

Oxide, 500A
Bruce Furnace 04 Recipe 250
~45 min at 1000 °C

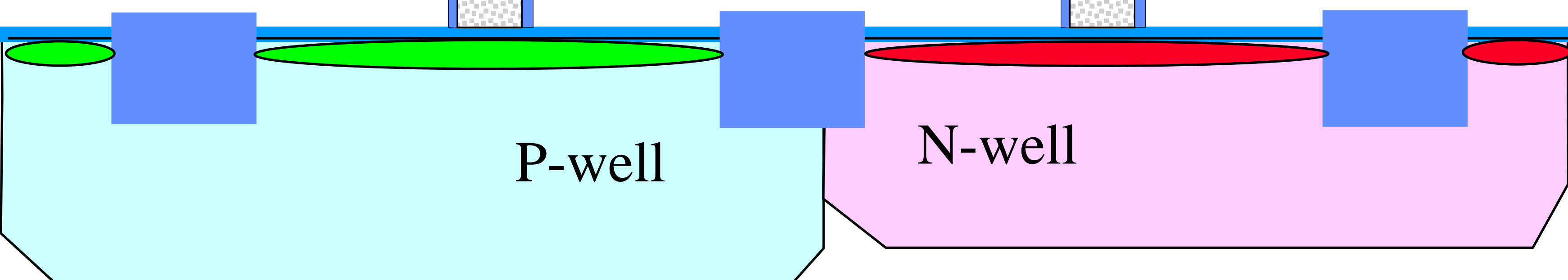
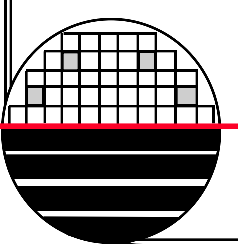


PHOTO 7 LDD P-TYPE IMPLANT



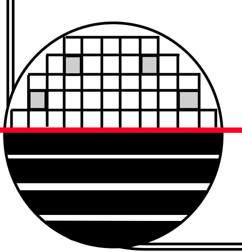
IMPLANT P-LDD

B11, Dose = 4E13, E = 50 KeV

P-well

N-well

Substrate 10 ohm-cm



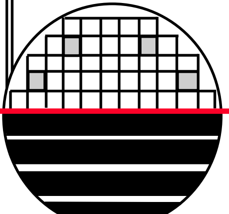
IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology			Lance Barron	
Microelectronic Engineering			Dr. Lynn Fuller	
11/20/04				

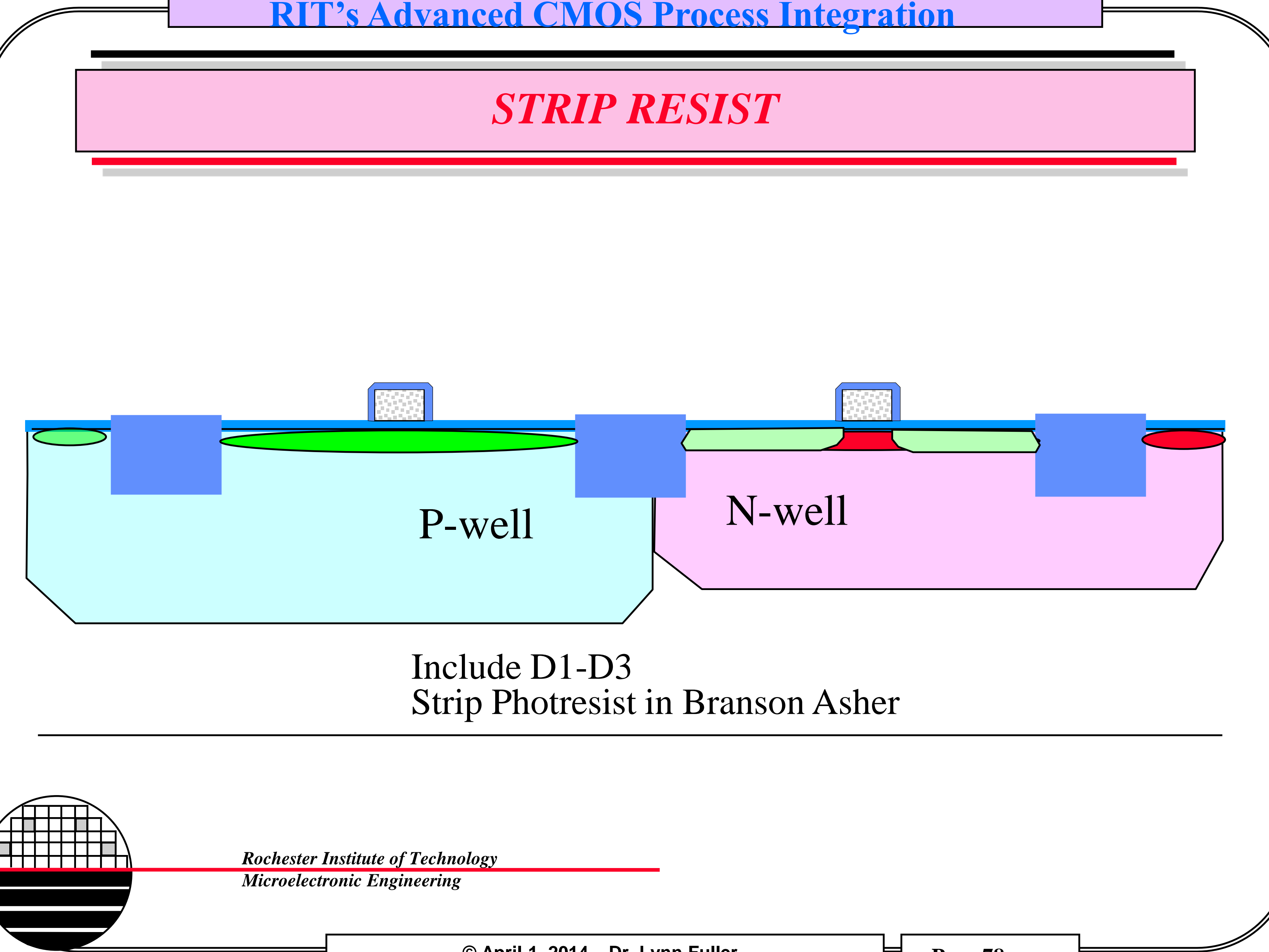
IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		MASK TYPE		ENERGY	
B11	1	Resist	0	50	KeV
BF2	0	Poly	1		
P31	0	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 3529.481 Angstroms



STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

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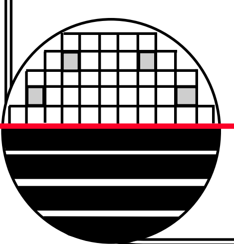
PHOTO 8 LDD N-TYPE IMPLANT

P-well

N-well

Substrate 10 ohm-cm



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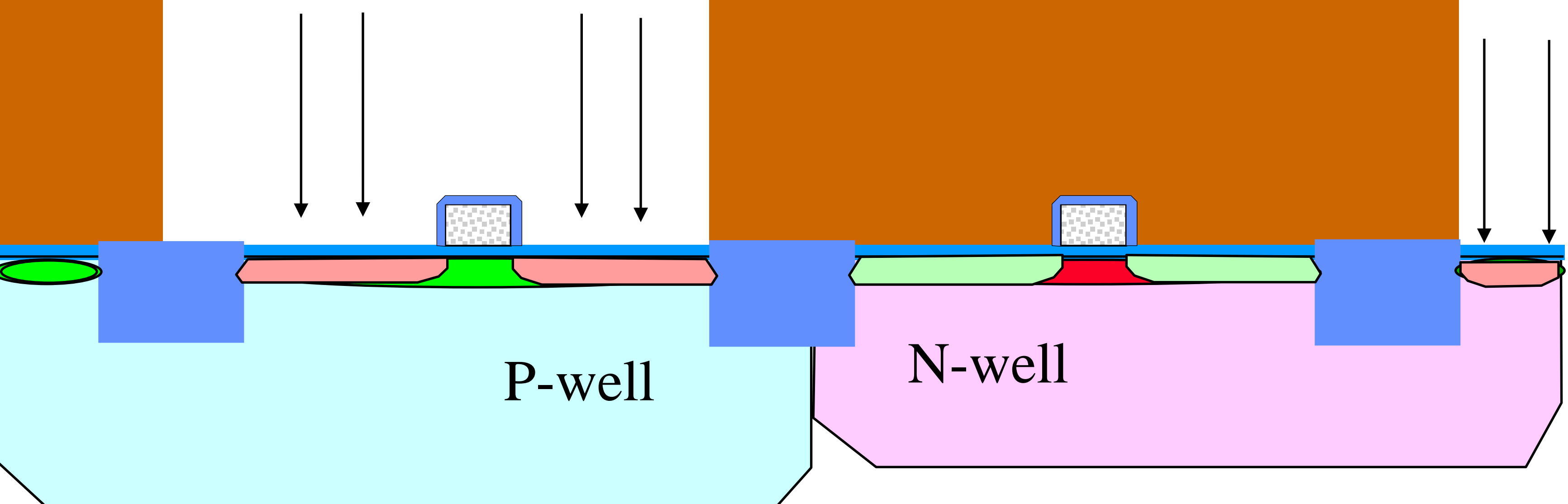
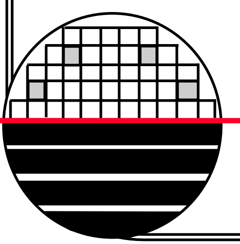
IMPLANT N-LDD

P31, Dose = 4E13, E = 60 KeV



Substrate 10 ohm-cm



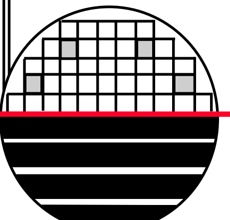
IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology			Lance Barron	
Microelectronic Engineering			Dr. Lynn Fuller	
11/20/04				

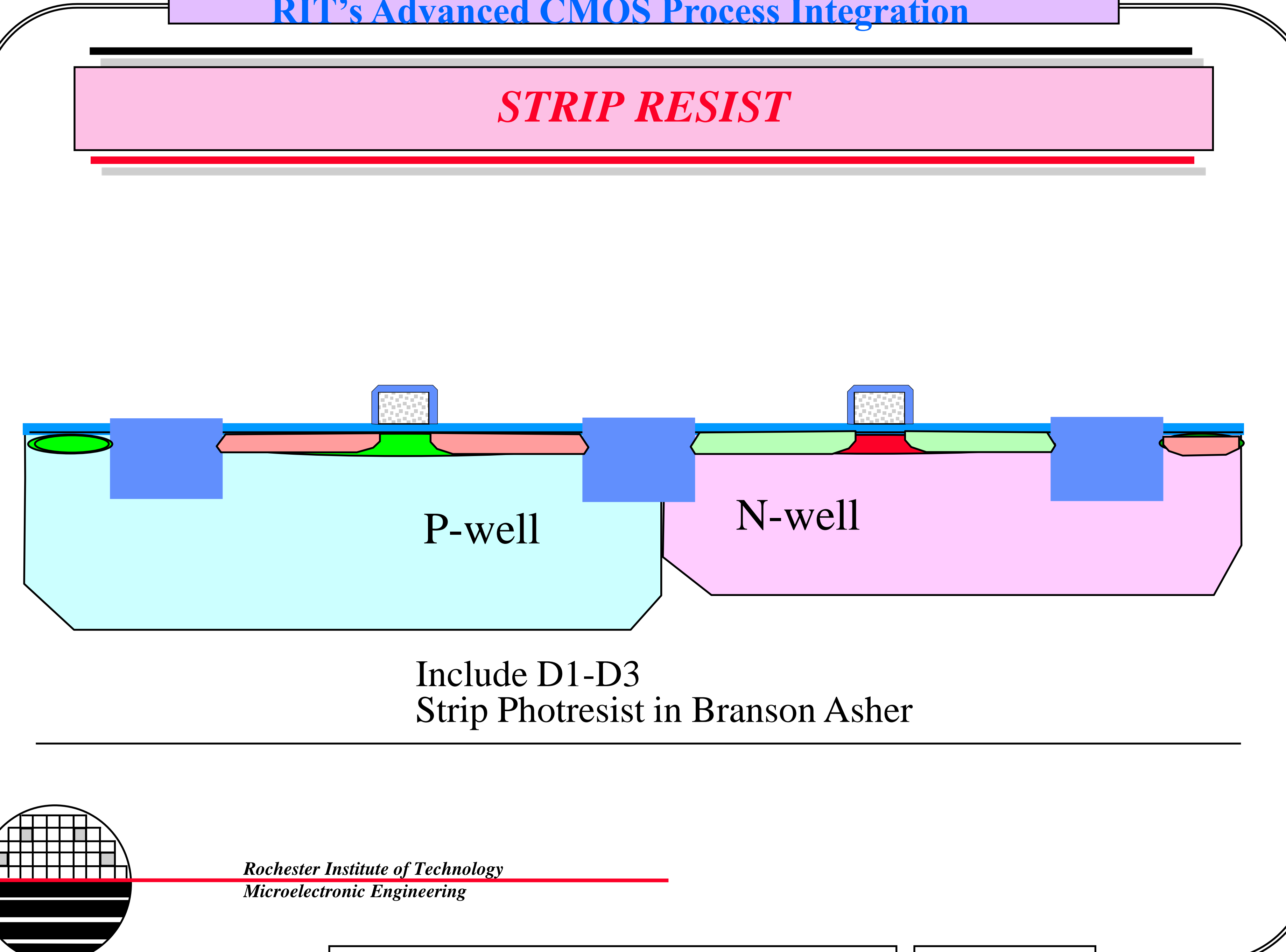
IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		**MASK TYPE**		**ENERGY**	
B11	0	Resist	0	60	KeV
BF2	0	Poly	1		
P31	1	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 2798.861 Angstroms



STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

RCA CLEAN AND LPCVD NITRIDE

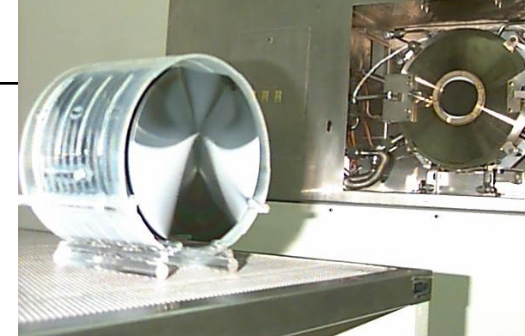
LPCVD Nitride 810°C
400 mTorr, NH_3 flow = 150 sccm
Dichlorosilane flow = 60 sccm

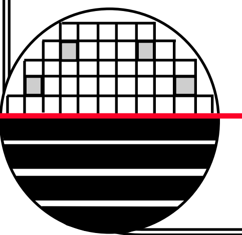
Target 3500 Å

P-well

N-well

ASM 6" LPCVD Tool





NITRIDE SIDE WALL SPACERS

Side Wall Spacer

Ion Implant

Nitride as a side wall spacer in deep sub micron transistor fabrication has some advantages over oxide side wall spacers. Nitride LPCVD is a more uniform and more conformal film than LTO. Nitride offers the possibility of end-point detection and higher selectivity during the plasma etch, while an oxide spacer does not.

Power	250 Watts
Pressure	40 mTorr
SF6	30 sccm
CHF3	30 sccm
Nitride Etch Rate	1250 A/min
Nitride Etch %NU	~ 4% *
Oxide Etch Rate	~ 950 A/min *
Oxide Etch %NU	~ 10% *
Selectivity Nitride:Oxide	1.3:1

Drytek Quad

NITRIDE SIDE WALL SPACERS

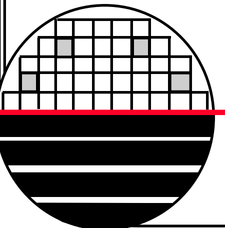
Polysilicon
Nitride Spacer
Silicon Dioxide
200nm
Mag = 146.32 K X EHT = 20.00 kV

Poly thickness = 2300 A
Oxide thickness = 1000A
Spacer Height = 2300 A
Spacer Width = 0.3 um

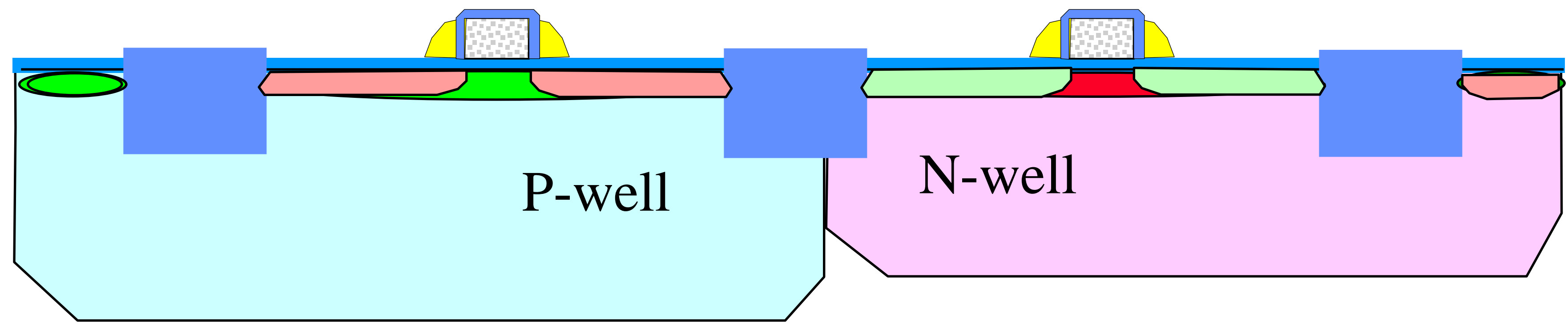
Special thanks to Dr. Sean Rommel for help in using the new LEO SEM

SIDE WALL SPACER ETCH IN DRYTEK QUAD

Anisotropic Nitride Etch
Drytek Quad
Recipe FACSPCR
30 sccm SF_6
30 sccm CHF_3
Power = 200 watts
Pressure = 50 mTorr
Etch Rate = 125 nm/min



AFTER ETCH NITRIDE TO FORM SIDE WALL SPACERS



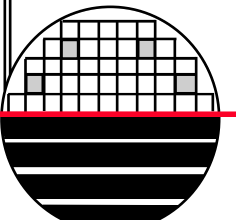
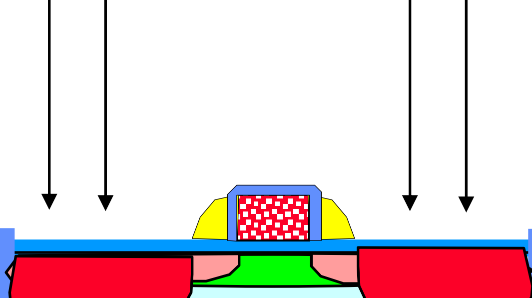


PHOTO 9 N+ D/S

P31, Dose = 4 E15, E = 60 KeV



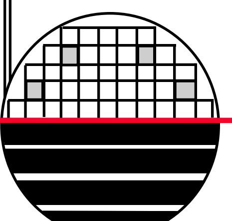
IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology			Lance Barron	
Microelectronic Engineering			Dr. Lynn Fuller	
11/20/04				

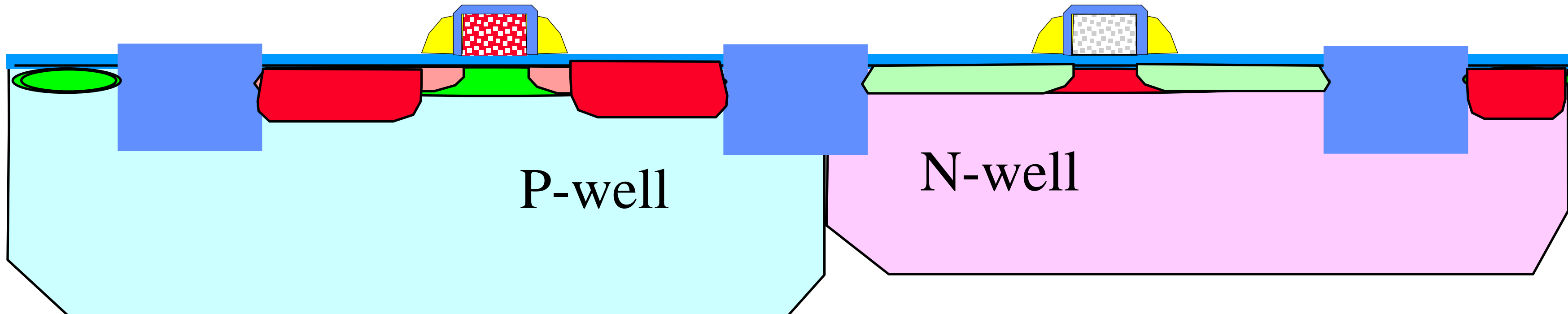
IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		MASK TYPE		ENERGY	
B11	0	Resist	0	60	KeV
BF2	0	Poly	1		
P31	1	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 2798.861 Angstroms



STRIP RESIST

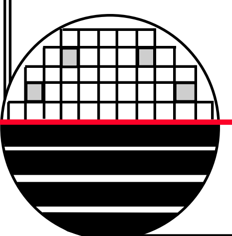


Include D1-D3
Strip Photresist in Branson Asher

PHOTO 10 P+ D/S

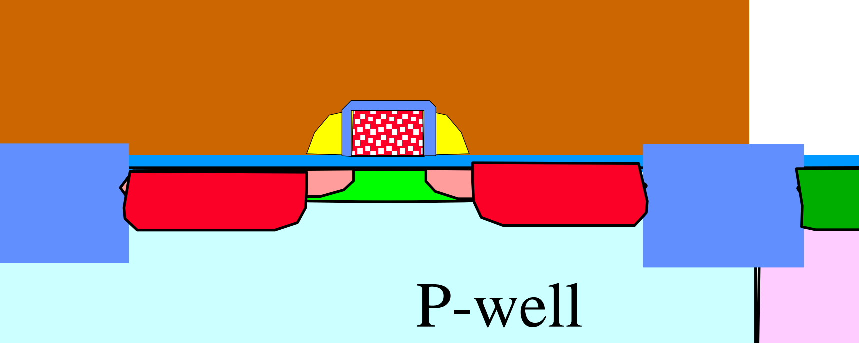
P-well

N-well



IMPLANT P+ D/S

B11, Dose = 4 E15, E = 50 KeV



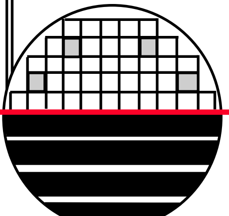
IMPLANT MASKING THICKNESS CALCULATOR

Rochester Institute of Technology			Lance Barron
Microelectronic Engineering			Dr. Lynn Fuller
11/20/2004			

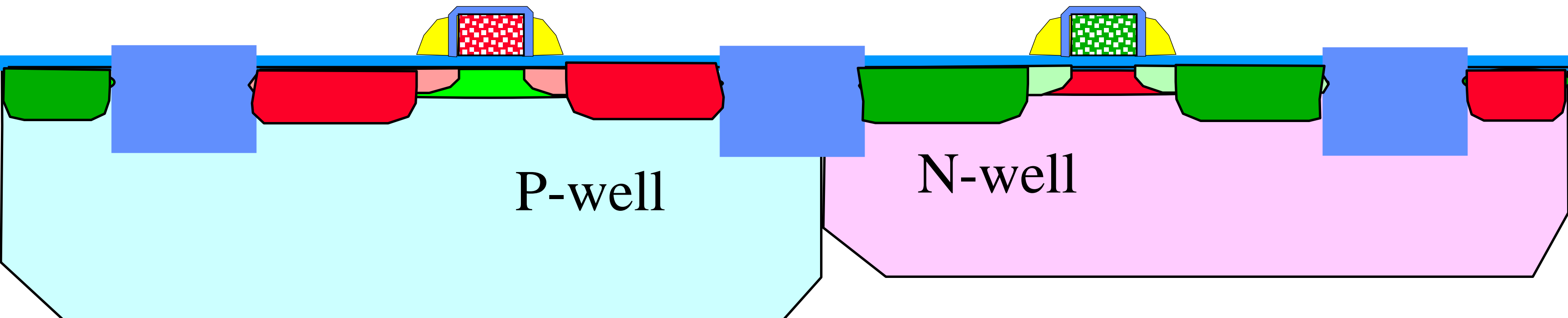
IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		**MASK TYPE**		**ENERGY**	
B11	1	Resist	0	50	KeV
BF2	0	Poly	1		
P31	0	Oxide	0		
		Nitride	0		

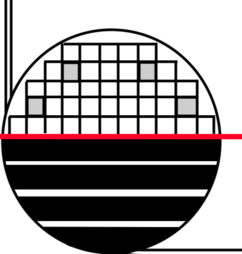
Thickness to Mask >1E15/cm3 Surface Concentration 3529.481 Angstroms



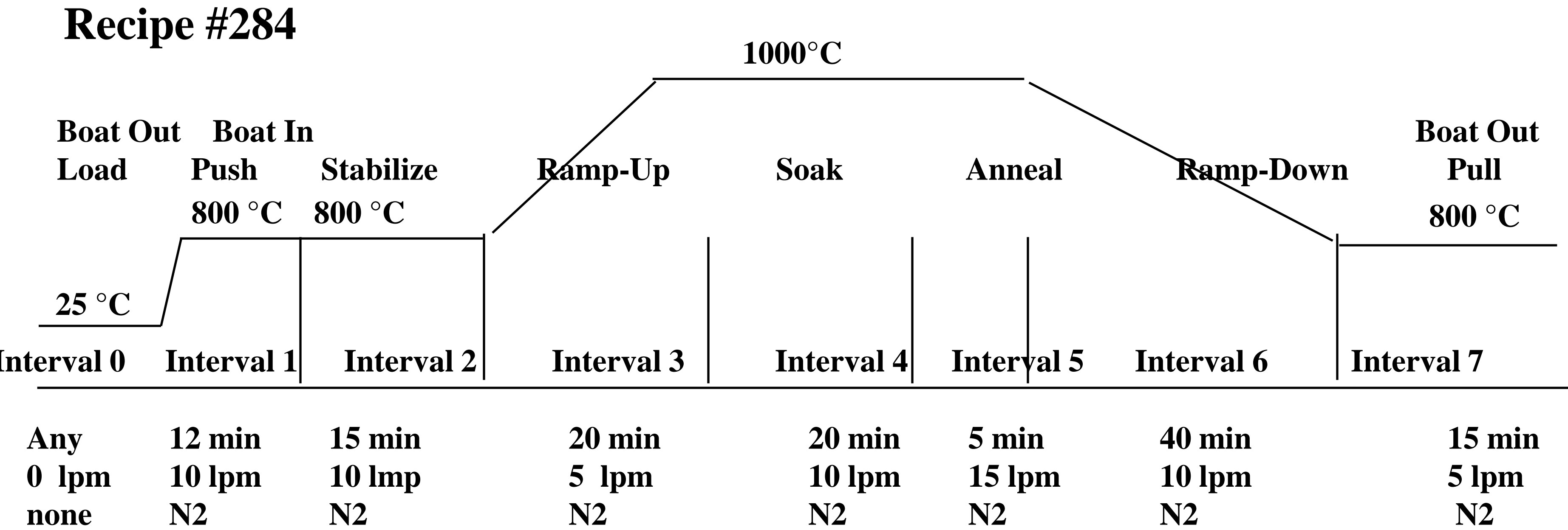
STRIP RESIST, RCA CLEAN



Include D1-D3
Strip Photresist in Branson Asher



BRUCE FURNACE RECIPE 284 – Adv-CMOS ANNEAL

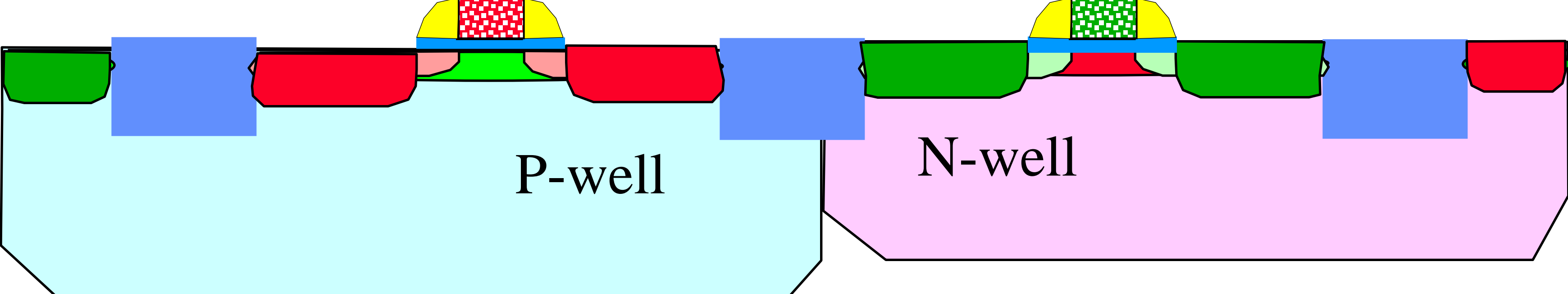


Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7
Any	12 min	15 min	20 min	20 min	5 min	40 min	15 min
0 lpm	10 lpm	10 lmp	5 lpm	10 lpm	15 lpm	10 lpm	5 lpm
none	N2	N2	N2	N2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

DS Implant Anneal, Oxide Growth

ETCH OXIDE



TiSi SALACIDE PROCESS

Forming a metal silicide helps reduce the resistance of the polysilicon interconnects and reduces the sheet resistance of the drain/source areas of the transistor. In deep sub-micron CMOS the nMOSFET transistor has n+ poly and the pMOSFET has p+ poly. Normally the poly is doped by ion implantation at the same time the drain and sources is implanted. In this case it is essential to form a silicide to reduce the sheet resistance of the poly and to connect n+ and p+ poly where ever they meet. SALICIDE is an acronym for self-aligned silicide and can be achieved with the following process. Ti (or some other metal) is sputtered on the wafer. It is heated in vacuum or N2 atmosphere to form TiSi where ever the Ti metal is in contact with silicon but not where it is in contact with silicon dioxide. The wafer is etched in sulfuric acid and hydrogen peroxide mixture which removes the metal from the oxide regions leaving TiSi self aligned on the silicon areas. Further heat treating at a higher temperature can convert TiSi to TiSi2 which is lower sheet resistance.

TiSi SALACIDE PROCESS

Sputtering of Titanium:

Dip in 50:1 HF, Spin Rinse Dry
Just prior to metal deposition.

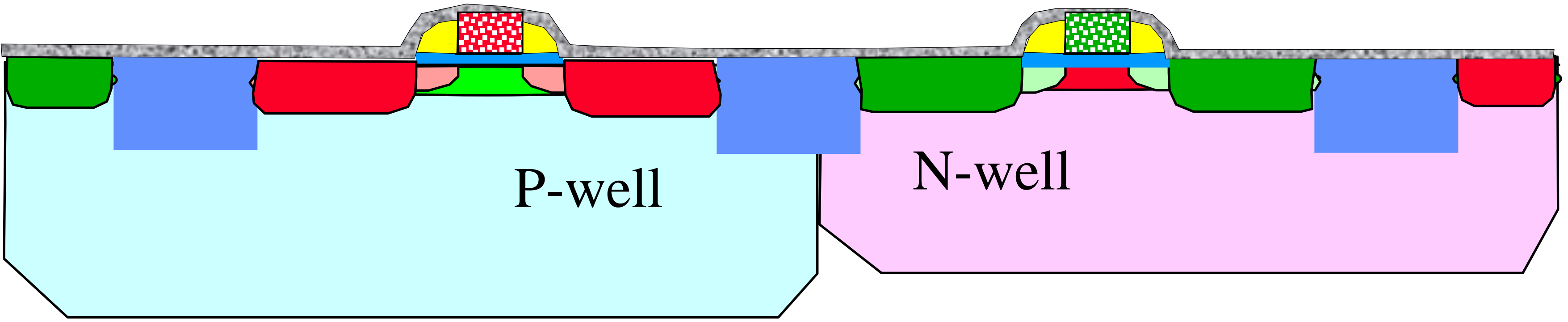
Ti Thickness = 1000Å

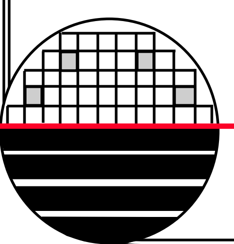
4" Target, 350 watts, 5 mTorr, 5 min pre-sputter, 10 min sputter, Rate = 100Å/min

8" Target, 750 watts, 5 mTorr, 5 min pre-sputter, 6 min sputter, Rate = ~176 Å/min

Heater time, 20 min., 300 C
Base Pressure <5E-6 Torr

AFTER Ti SPUTTER



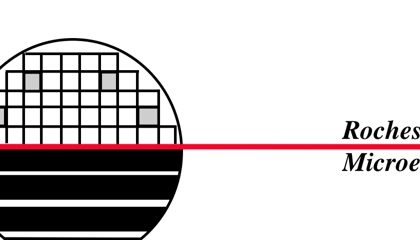


RTP TO FORM SILICIDE

AG Associates 610
N2
Recipe TISI1.RCP
Temp = ~650 C
Time = 1 min.

P-well

N-well



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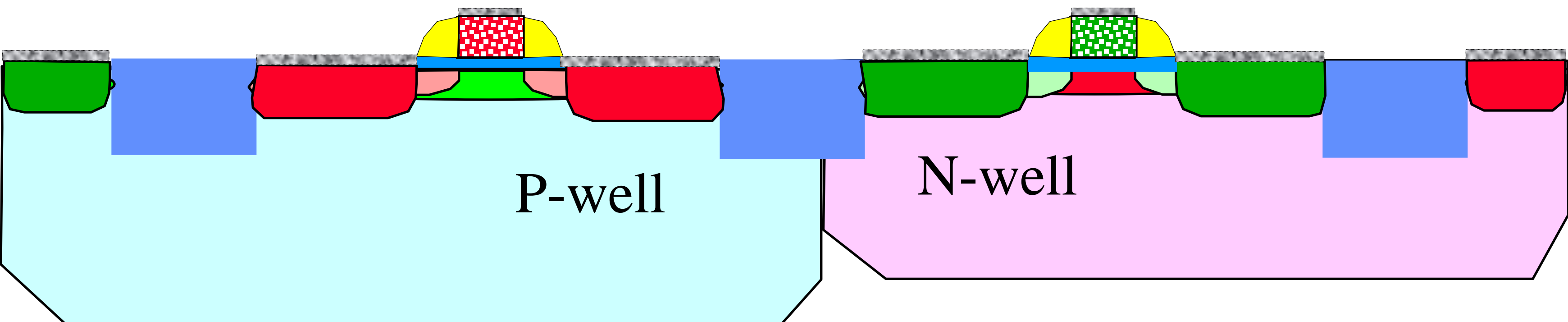
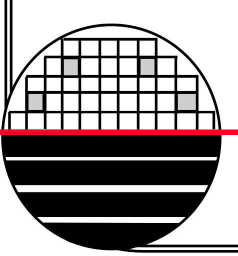
ETCH REMOVE Ti



Mix new chemicals in 9"x9" Pyrex Dish
Use hot plate set to 150 C but etch at 90 C
H2S04:H2O2 (1:2), Temp ~90C (self heating)
Etch Time = 2 min
Rinse, 5 min., Spin-Rinse Dry



TiSi SALACIDE PROCESS

Etching of Ti Metal:

Heat the Sulfuric Acid:Hydrogen Peroxide (1:2) mixture on a hotplate at 90°C (set plate temperature to 150°C)

Etch for 1 min 30 sec. This should remove the Ti that is on top of the silicon dioxide but not remove TiSi that was formed on the polysilicon and D/S regions. It also removes unreacted Ti metal over the TiSi on the poly and D/S regions.

Courtesy of SMFL

RTP TO FORM SILICIDE (TiSi2)

AG Associates 610
N2
Recipe TiSi2.RCP
Temp = ~800 C
Time = 1 min.

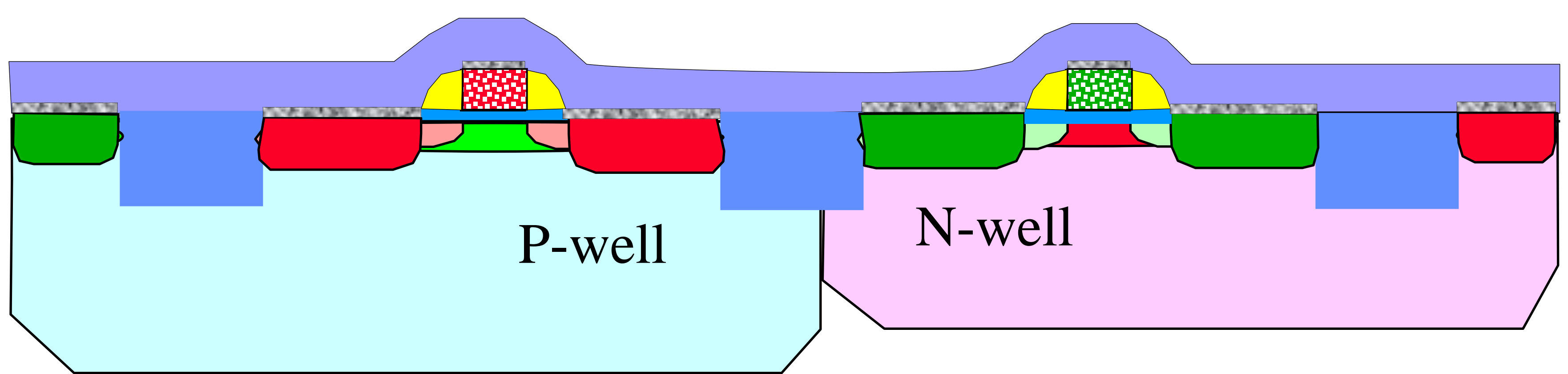
P-well

N-well

RTA

RCA CLEAN AND DEPOSIT LPCVD OXIDE

Target 4000 Å



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PECVD OXIDE FROM TEOS

TEOS Program: (Chamber A)

Step 1
- Setup Time = 15 sec
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 0 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 2 – Deposition
- Dep Time = 55 sec (5000 Å)
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 205 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 3 – Clean
- Time = 10 sec
- Pressure = Fully Open
- Susceptor Temperature= 390 C
- Susceptor Spacing= 999 mils
- RF Power = 50 watts
- TEOS Flow = 0 scc
- O2 Flow = 285 scc

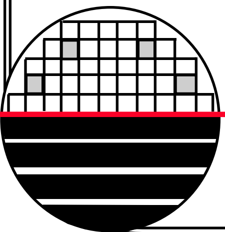


PHOTO 11 CONTACT CUTS

Increase Dose and Develop Time
Exposure Dose 185 mj/cm2
Use DEVFAC.RCP

ETCH CONTACT CUTS

P-well

N-well

Plasma Etch
Using FACCUT in Drytek Quad
200 Watt, 100 mTorr
50 sccm CHF3, 10 sccm CF4
100 sccm Ar

DRYTEK QUAD ETCH RECIPE FOR CC AND VIA

Recipe Name:		FACCUT
Chamber		3
Power		200W
Pressure		100 mTorr
Gas 1	CHF_3	50 sccm
Gas 2	CF_4	10 sccm
Gas 3	Ar	100 sccm
Gas 4	O_2	0 sccm
	(could be changed to N_2)	

TEOS Etch Rate	494	Å/min
Annealed TEOS	450	Å/min
Photoresist Etch Rate:	117	Å/min
Thermal Oxide Etch Rate:	441	Å/min
Silicon Etch Rate	82	Å/min
TiSi2 Etch Rate	1	Å/min

US Patent 5935877 - Etch process for forming contacts over titanium silicide

Drytek Quad

FACCCUT RECIPE

STEP: 1 PROCESS: FACCCUT

GAS STABILIZATION TIME (SECS) 30

SCAN DELAY/AUTO ZERO (MM:SS) 00:00

CF4	FLOW (CC)	10	ERROR RANGE %	20
CHF3	FLOW (CC)	50	ERROR RANGE %	20
O2	FLOW (CC)	0	ERROR RANGE %	20
AR	FLOW (CC)	75	ERROR RANGE %	20

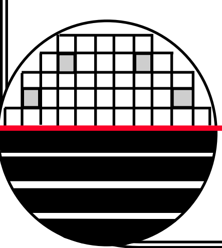
PRESSURE (mT)	100	ERROR RANGE %	40
TURBO PUMP (Y/N)	N		
RF POWER (W)	200	ERROR RANGE %	70
RF REFL. ERROR	100		
BIAS LOW ERROR	0	BIAS HI ERROR	1000

MODE	TIME	AUX. SIGNAL (Y/N)	N
PARAMETER	0	MAX TIME (MM:SS)	10:00
DELTA	0	START DELAY (MM:SS)	00:00
% OVERETCH	0	ABORT TIME (MM:SS)	23:30

GAS EVAC. TIME (SECS) 30

THIS STEP IS ALLOWED IN CHAMBER 3

PRESS 'HELP' KEY FOR ADDITIONAL INFORMATION



CONTACT CUT ETCH RECIPE

Theory: The CHF3 and CF4 provide the F radicals that do the etching of the silicon dioxide, SiO2. The high voltage RF power creates a plasma and the gasses in the chamber are broken into radicals and ions. The F radical combines with Si to make SiF4 which is volatile and is removed by pumping. The O2 in the oxide is released and also removed by pumping. The C and H can be removed as CO, CO2, H2 or other volatile combinations. The C and H can also form hydrocarbon polymers that can coat the chamber and wafer surfaces. The Ar can be ionized in the plasma and at low pressures can be accelerated toward the wafer surface without many collisions giving some vertical ion bombardment on the horizontal surfaces. If everything is correct (wafer temperature, pressure, amounts of polymer formed, energy of Ar bombardment, etc.) the SiO2 should be etched, polymer should be formed on the horizontal and vertical surfaces but the Ar bombardment on the horizontal surfaces should remove the polymer there. The O2 (O radicals) released also help remove polymer. Once the SiO2 is etched and the underlying Si is reached there is less O2 around and the removal of polymer on the horizontal surfaces is not adequate thus the removal rate of the Si is reduced. The etch rate of SiO2 should be 4 or 5 times the etch rate of the underlying Si. The chamber should be cleaned in an O2 plasma after each wafer is etched.

US Patent 5935877 - Etch process for forming contacts over Titanium Silicide

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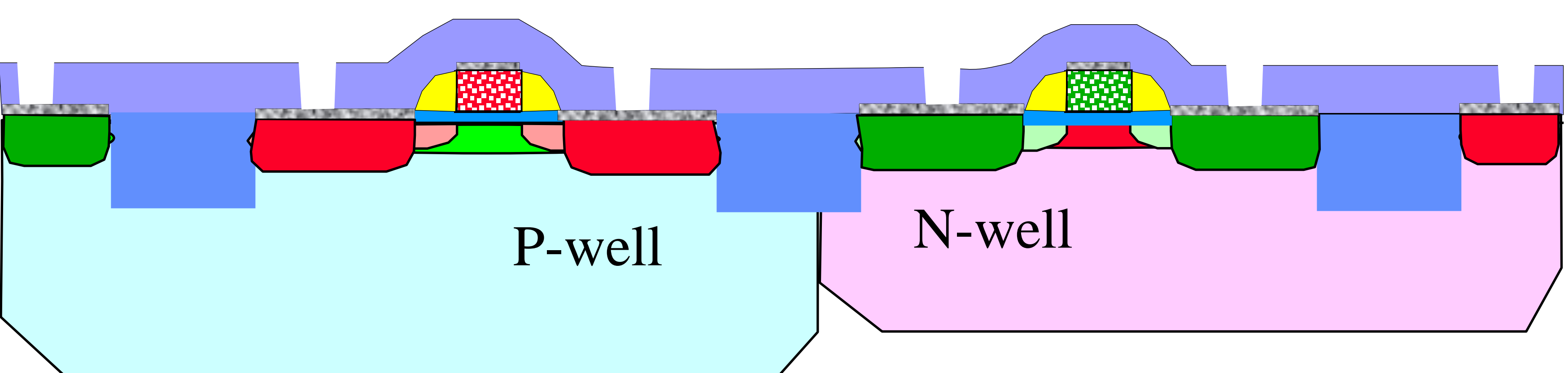
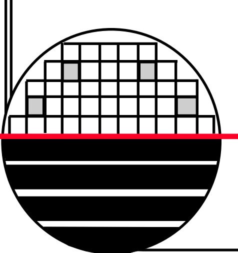
STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher



RCA CLEAN

APM

NH_4OH - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

→ DI water rinse, 5 min.

→ H_20 - 50
HF - 1
60 sec.

→ DI water rinse, 5 min.

→ HPM

HCL - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

→ DI water rinse, 5 min.

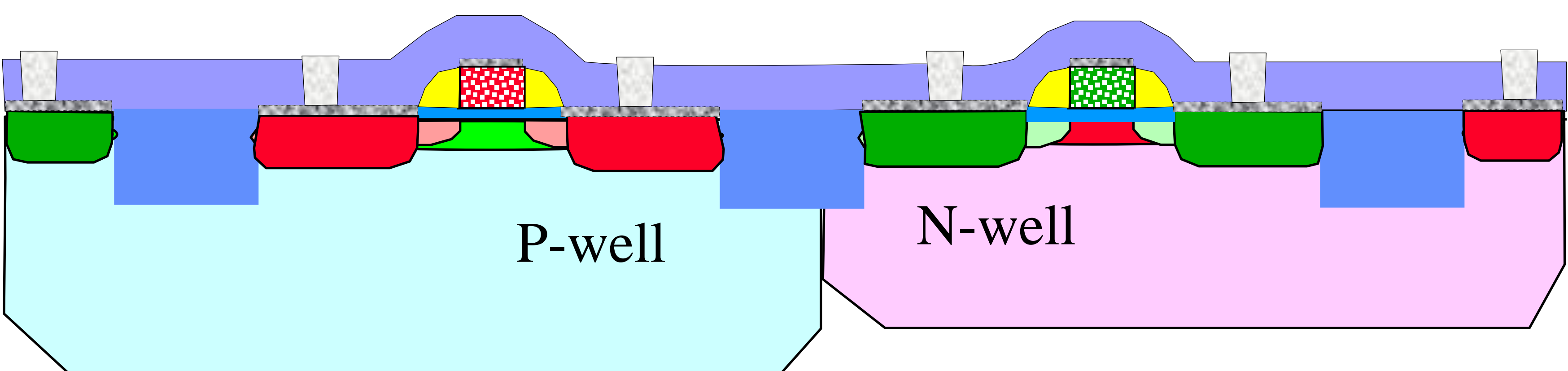
→ H_20 - 50
HF - 1
60 sec.

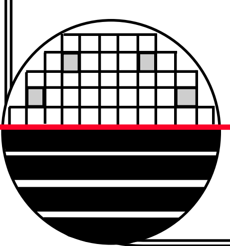
→ DI water rinse, 5 min.

→ SPIN/RINSE DRY

Clean includes 50:1 HF Dip twice once after each bath to remove chemically grown oxide

LPCVD TUNGSTEN PLUGS





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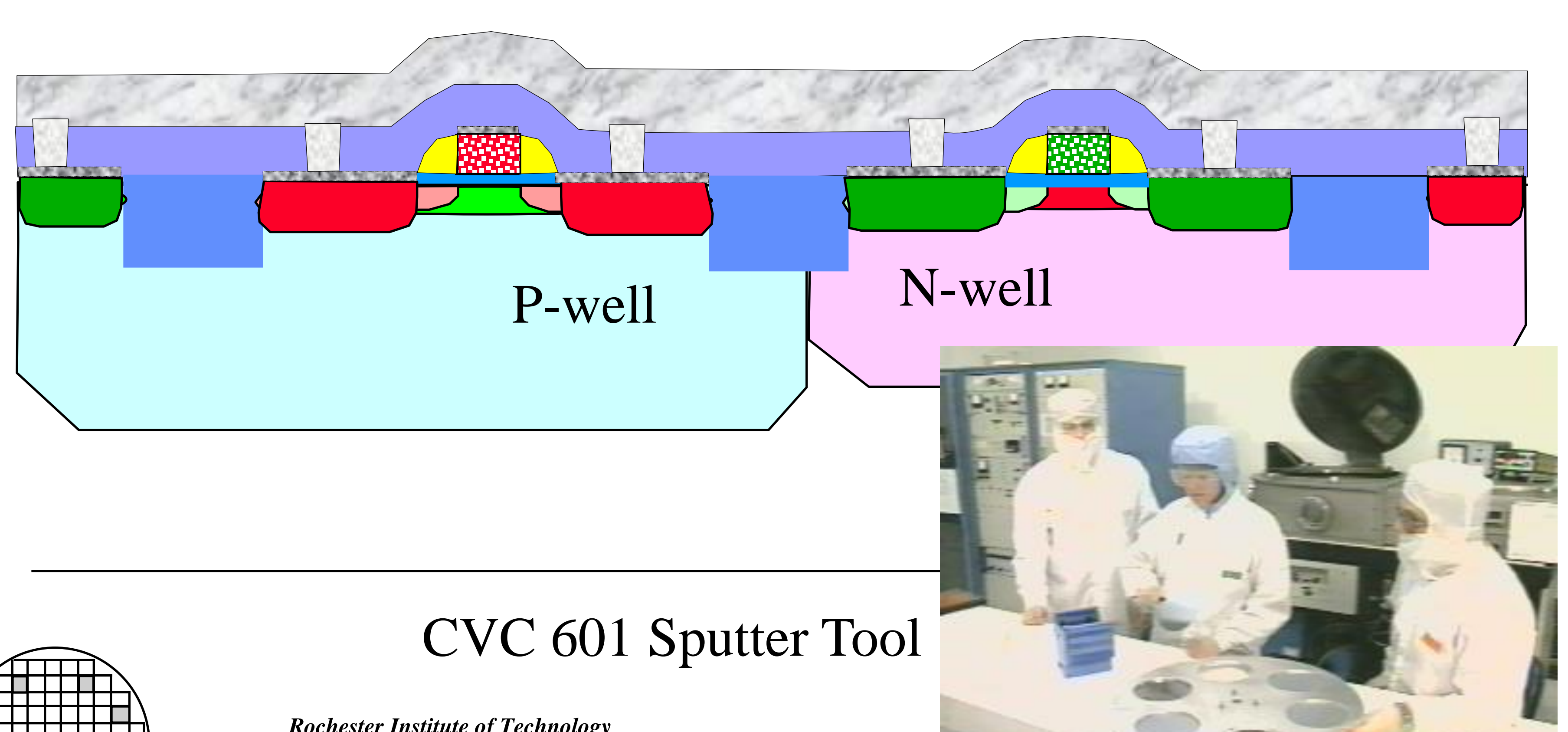
DEPOSIT ALUMINUM

0.75 µm Aluminum



CVC 601 Sputter Tool

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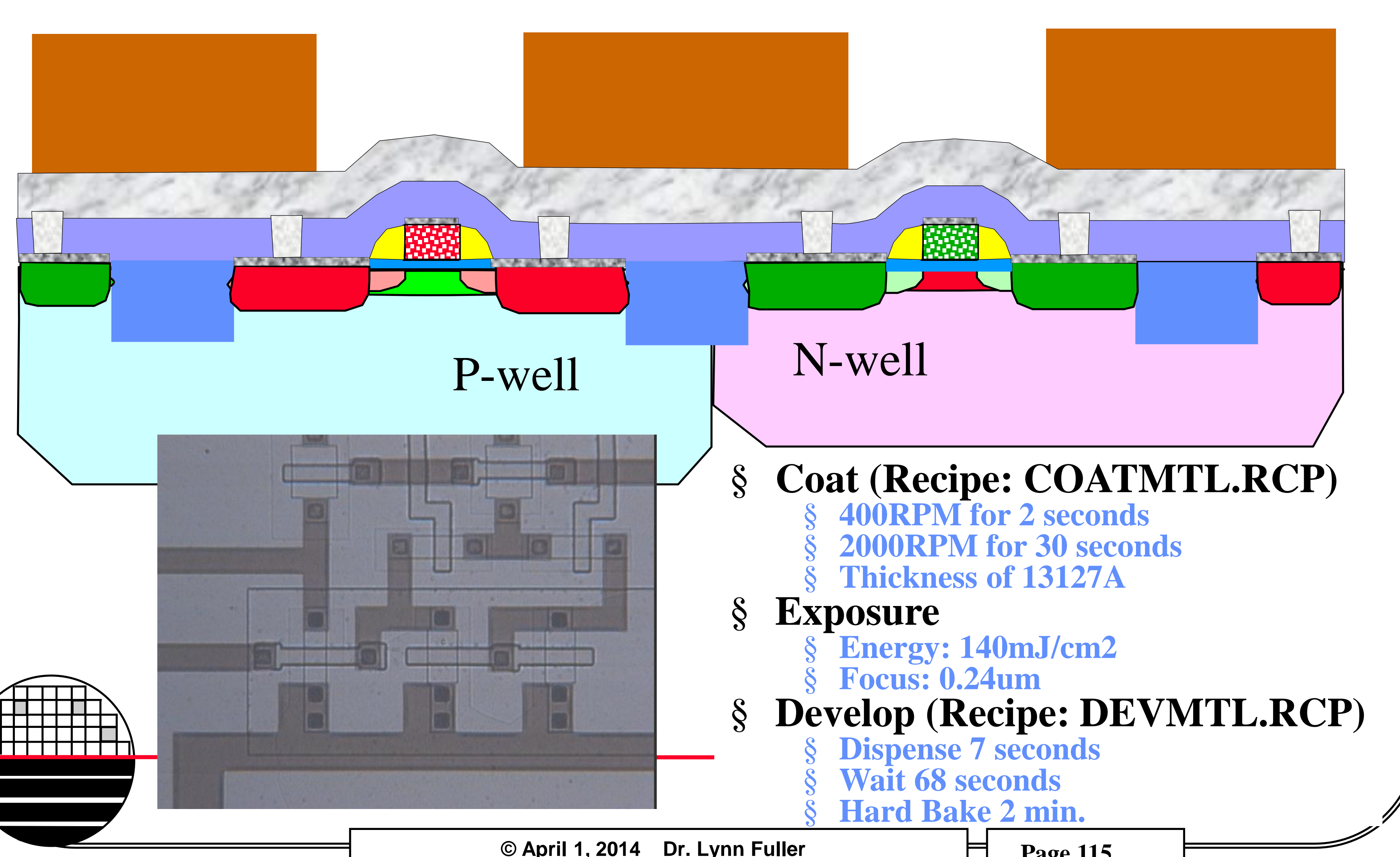
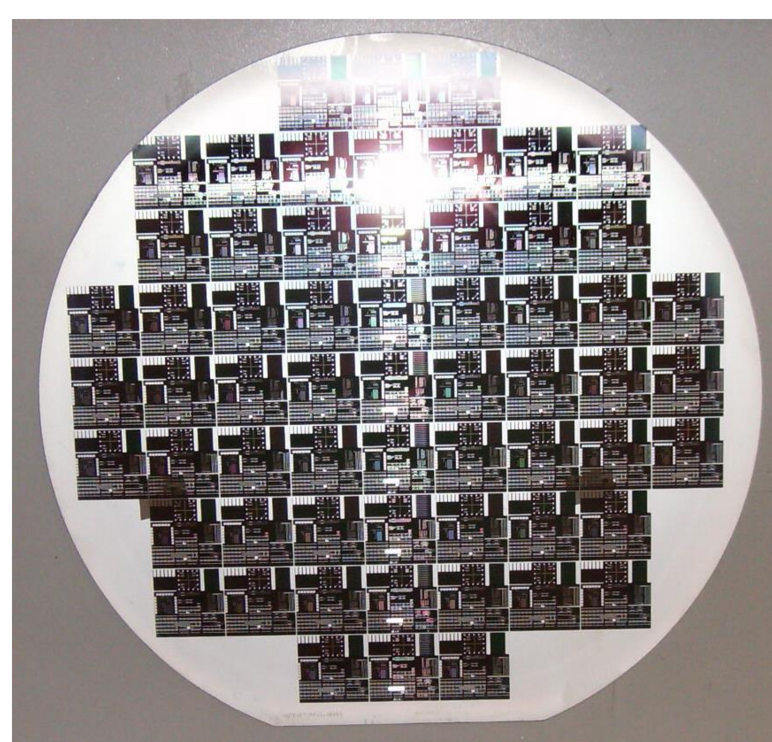
PHOTO 12 METAL ONE



- **Coat (Recipe: COATMTL.RCP)**
  - **400RPM for 2 seconds**
  - **2000RPM for 30 seconds**
  - **Thickness of 13127A**
- **Exposure**
  - **Energy: 140mJ/cm2**
  - **Focus: 0.24um**
- **Develop (Recipe: DEVMTL.RCP)**
  - **Dispense 7 seconds**
  - **Wait 68 seconds**
  - **Hard Bake 2 min.**

ALUMINUM ETCH USING LAM4600



Rochester Institute of Technology
Microelectronic Engineering

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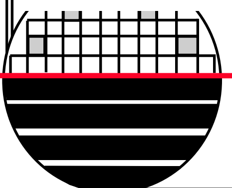
INTRODUCTION

The LAM4600 is a Reactive Ion Etch (RIE) Tool for Anisotropic Aluminum Plasma Etch. It is a load lock vacuum system to keep room air out of the main etch chamber. The entire system is heated slightly above room temperature because the byproducts of the etch (Aluminum/Chlorides) are volatile and can be pumped out of the chamber but at a slightly lower temperature the byproducts will deposit on the inside surfaces of the tool, pump lines, and pumps. The Gas Reactor Column (GRC) removes the chlorine byproducts from the gas that is exhausted to the outside world. Endpoint detection is available and is based on plasma brightness (similar to the LAM490 tool) Other materials can be etched with these chemicals. The tool has a built in water rinse station at the exit that can be used (or not) to reduce chlorine residue on the wafers. We do an external SRD rinse on the wafers after etching.



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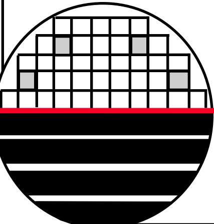
LAM 4600 ALUMINUM ETCHER

Aluminum Plasma Etch Chemistry

- Cl_2 – Reduces Pure Aluminum
- BCl_3 – Etches native Aluminum Oxide
  - -Increases Physical Sputtering
- N_2 – Dilute and Carrier for the chemistry
- Chloroform – Helps Anisotropy and reduces photoresist damage



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LAM4600 ANISOTROPIC ALUMINUM ETCH

Step	1	2	3	4	5
Pressure	**100**	**100**	**100**	**100**	**0**
RF Top (W)	**0**	**0**	**0**	**0**	**0**
RF Bottom	**0**	**250**	**125**	**125**	**0**
Gap (cm)	**3**	**3**	**3**	**3**	**5.3**
O2 111	**0**	**0**	**0**	**0**	**0**
N2 222	**13**	**13**	**20**	**25**	**25**
BCl 333	**50**	**50**	**25**	**25**	**0**
Cl2 444	**10**	**10**	**30**	**23**	**0**
Ar 555	**0**	**0**	**0**	**0**	**0**
CFORM 666	**8**	**8**	**8**	**8**	**8**
Complete	**Stabl**	**Time**	**Time**	**Oetch**	**Time**
Time (s)	**15**	**8**	**200**	**10%**	**15**

Rate ~38Å/s

Thickness = 7500Å

Various tool modifications resulted in different etch rates for different years

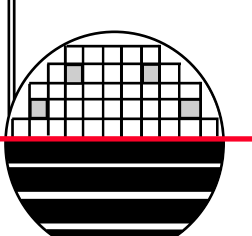
Channel	**B**
Delay	**130**
Normalize	**10 s**
Norm Val	**5670**
Trigger	**105%**
Slope	**+**

Endpoint (not used)

Fuller April 2013 – 200s

Fuller, January 2012 -300s

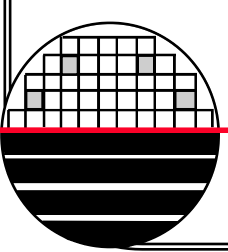
Fuller, March 2011 -230s



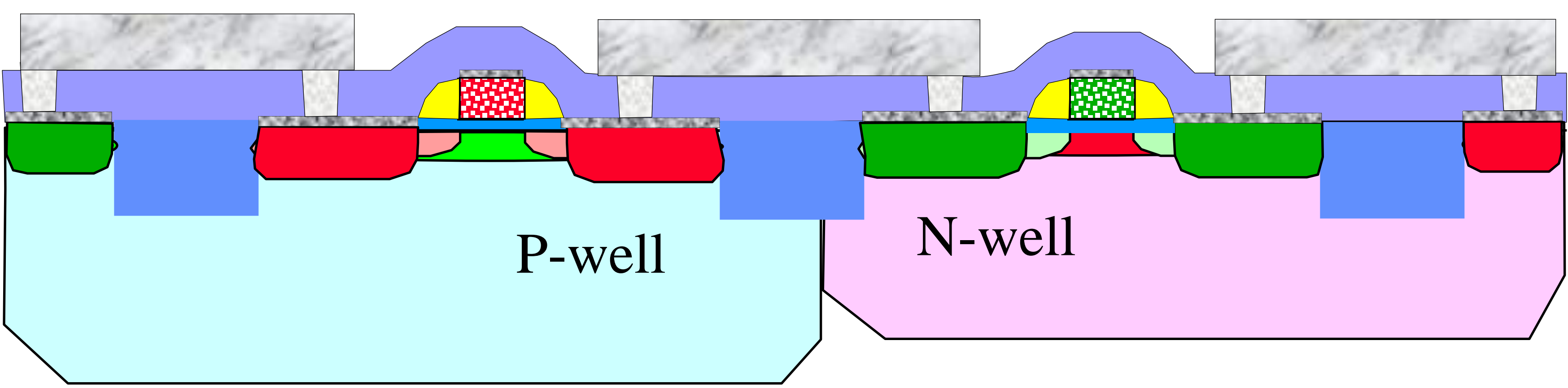
ALUMINUM ETCH

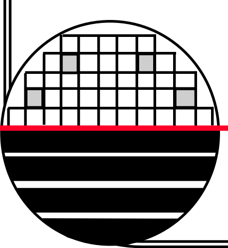
P-well

N-well

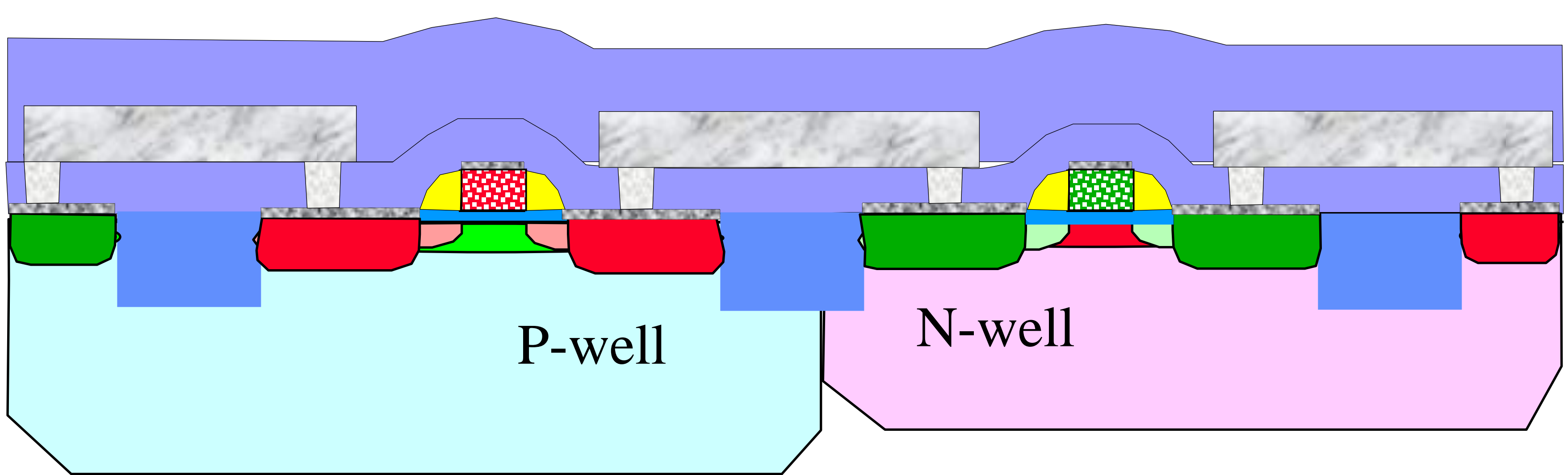


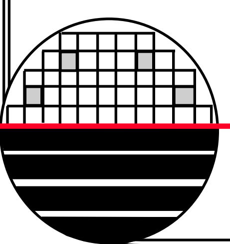
RESIST STRIP





LTO





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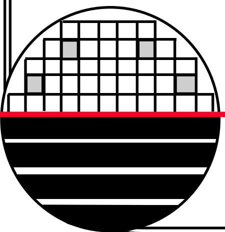
PECVD OXIDE FROM TEOS

TEOS Program: (Chamber A)

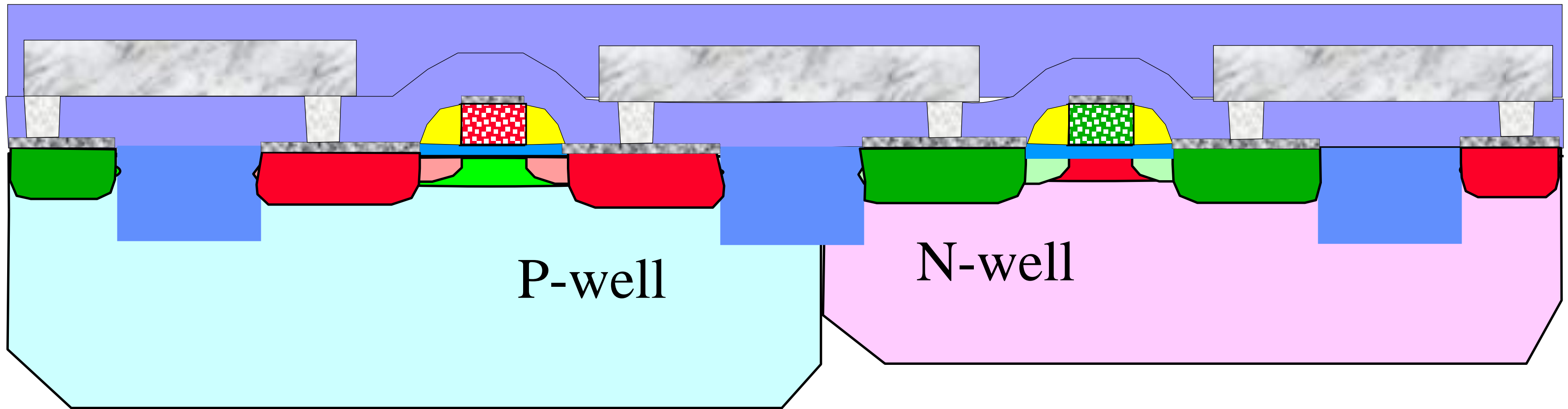
Step 1
- Setup Time = 15 sec
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 0 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 2 – Deposition
- Dep Time = 55 sec (5000 Å)
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 205 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 3 – Clean
- Time = 10 sec
- Pressure = Fully Open
- Susceptor Temperature= 390 C
- Susceptor Spacing= 999 mils
- RF Power = 50 watts
- TEOS Flow = 0 scc
- O2 Flow = 285 scc



CMP



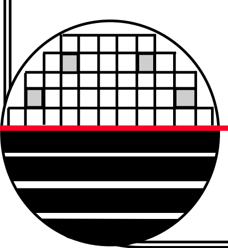


PHOTO FOR VIA, THEN VIA ETCH, RESIST STRIP

P-well

N-well

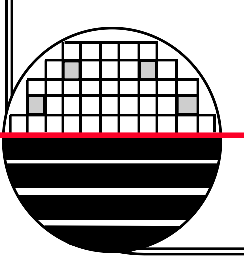
Plasma Etch
Using FACCC in Drytek Quad

METAL TWO

P-well

N-well

Aluminum deposition using PE4400
Base pressure: 1E-6 Torr
Sputter Etch 15 min.
Power: 400W for Aluminum target
Sputter pressure: 5 mTorr
Argon flow: 40 sccm
Deposition time: 200 min
Dep rate: 37 Å/min



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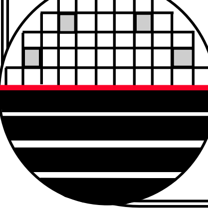
PE4400 SPUTTER / SPUTTER ETCH TOOL



PE4400 – AL THICKNESS NON UNIFORMITY

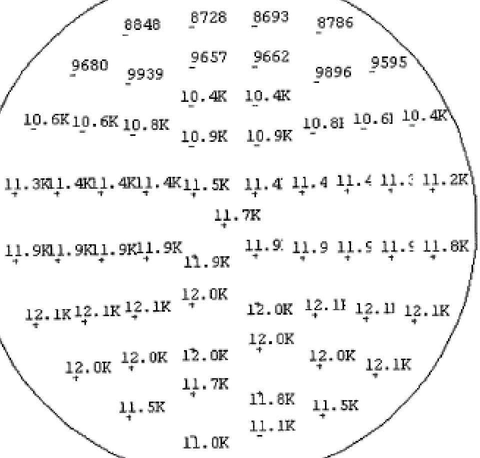
CDE ResMap FileName: C:\4P\Factory.prj\Al THK.rcp\0105I027.RsM
RunTitle CDE Demo

otID,WaferID MyLot MyWafer
unDate 08:02 01/05/10
ecip Name Factory Al THK
per|Engr[Equp]: CDE|Customer [ResMap]

afer No. SinglePrbCnfg
aferDia 150 Flat
dgeExclusn 12.0 FollowMajorFlat

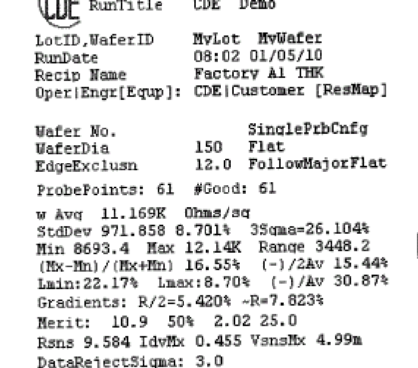
robePoints: 61 #Good: 61

Avg 11.169K Ohms/sq
tdDev 971.858 8.701% 3Sgma=26.104%
in 8693.4 Max 12.14K Range 3448.2
Mx-Mn)/(Mx+Mn) 16.55% (-)/2Av 15.44%
min:22.17% Lmax:8.70% (-)/Av 30.87%
radients: R/2=5.420% ~R=7.823%
erit: 10.9 50% 2.02 25.0
sns 9.584 IdvMx 0.455 VsnsMx 4.99m
ataRejectSigma: 3.0



Ave = 11.17K
Min = 8.69K
Max = 12.1K
Non Uniformity = 16.55%

Aluminum deposition using PE4400
Base pressure: 1E-6 Torr
Sputter Etch 15 min.
Power: 400W for Aluminum target
Sputter pressure: 5 mTorr
Argon flow: 40 sccm
Deposition time: 200 min
Dep rate: 37 Å/min

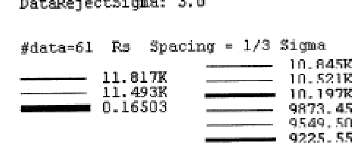

CDE ResMap FileName: C:\4P\Factory.prj\Al THK.rcp\0105I027.RsM
RunTitle CDE Demo

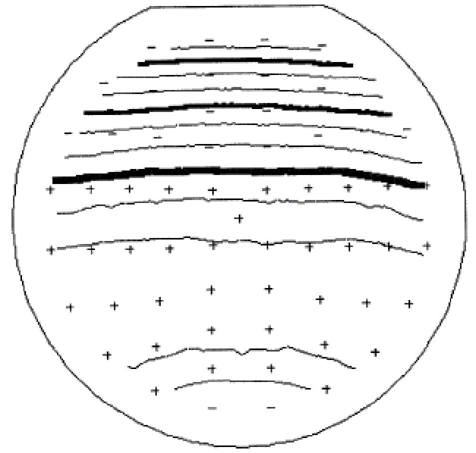
LotID,WaferID MyLot MyWafer
RunDate 08:02 01/05/10
Recip Name Factory Al THK
Oper|Engr[Equp]: CDE|Customer [ResMap]

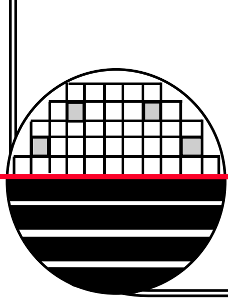
Wafer No. SinglePrbCnfg
WaferDia 150 Flat
EdgeExclusn 12.0 FollowMajorFlat

ProbePoints: 61 #Good: 61

w Avg 11.169K Ohms/sq
StdDev 971.858 8.701% 3Sgma=26.104%
Min 8693.4 Max 12.14K Range 3448.2
(Mx-Mn)/(Mx+Mn) 16.55% (-)/2Av 15.44%
Lmin:22.17% Lmax:8.70% (-)/Av 30.87%
Gradients: R/2=5.420% ~R=7.823%
Merit: 10.9 50% 2.02 25.0
Rsns 9.584 IdvMx 0.455 VsnsMx 4.99m
DataRejectSigma: 3.0







PE4400 SPUTTER ETCH RATE

	A	B	C	D	E	F	G	H	I	J
1										
2		Original	Post Etch			Original	Post Etch		Original	Post Etch
3	1	1992	1506		Average	2241.279	1685.459		2242.28	1685.8
4	2	2046	1543		Std. Dev	115.8784	86.18035		116.699	86.524
5	3	2059	1545		Min	1981	1500		1981.3	1500
6	4	2030	1518		Max	2414	1815		2417.3	1815
7	5	1981	1500		Range	433	315		436.05	315
8	6	2111	1597							
9	7	2155	1624		Etch Rate	18.52732	Å/min		18.54933	
10	8	2168	1629							
11	9	2172	1623							
12	10	2062	1542							
13	11	2252	1696							
14	12	2273	1709							
15	13	2007	1519							
16	14	2124	1604							
17	15	2238	1689							
18	16	2327	1752							
19	17	2349	1767							
20	18	2297	1722							
21	19	2213	1661							
22	20	2117	1585							
23	21	2069	1561							
24	22	2185	1645							
25	23	2273	1714							
26	24	2344	1766							
27	25	2388	1795							
28	26	2400	1802							
29	27	2370	1780							

~18Å/min

The sputter etch rate was calculated from measured aluminum thickness before and after sputter etch. Measurements were made using 4point probe thickness technique on the CDE resistivity mapper. The sputter etch rate of aluminum was 18 Å per minute.

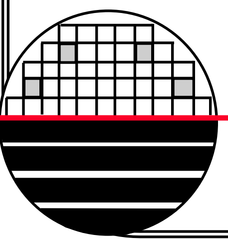
Power = 500 watts
Pressure = 5 mTorr
Flow = 20 sccm
Table Rotation = Yes

SUMMARY - FOR SPUTTERING IN PE4400

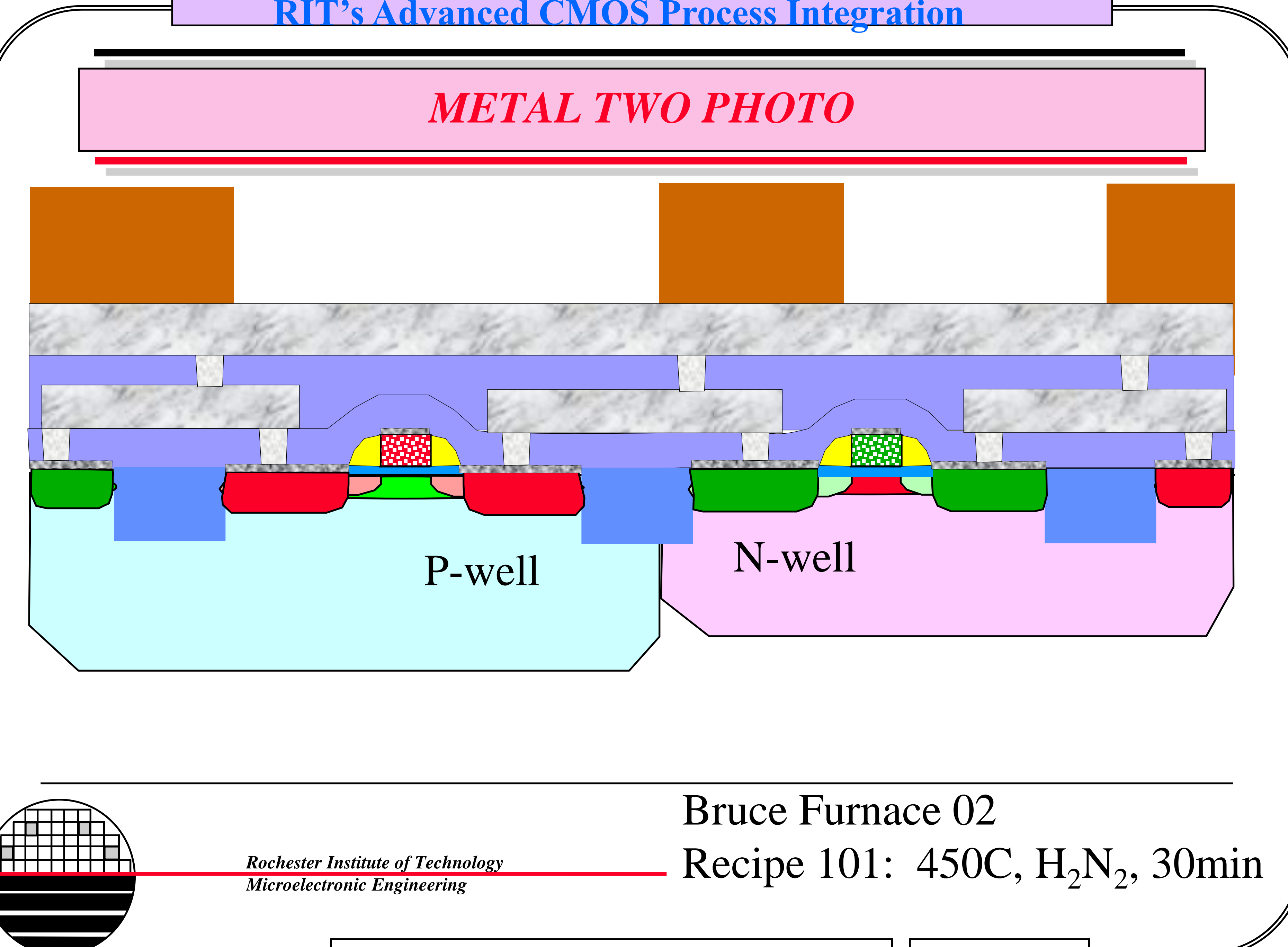
1. Smoother films can be deposited at lower powers.
2. Thinner films are smoother.
3. To quantify the roughness/smoothness the Veeco Wyco Optical Surface Profilometer is useful.
4. The deposition rate is lower at lower powers.
5. Deposition times become many hours for low power and film thickness approaching 1 micron.
6. Moving the wafers closer to the target increases sputter rate and surface roughness. (The height is as close as possible now “C”)
7. Rough films give problems for lithography and etching.
8. Surface roughness needs to be less than 10nm RMS for successful lithography and plasma etching.
9. Best conditions observed so far are, 300 watts, 5 mT, 40 sccm, to give a deposition rate of 37Å/min and surface roughness of ~11nm RMS for a film thickness of ~7500 Å. after 180 min sputter time.
10. Non uniformity is 22%. Wafers are thinner toward the flat.

VEECO WYCO NT1100 OPTICAL PROFILOMETER

Used to measure RMS surface roughness



METAL TWO PHOTO

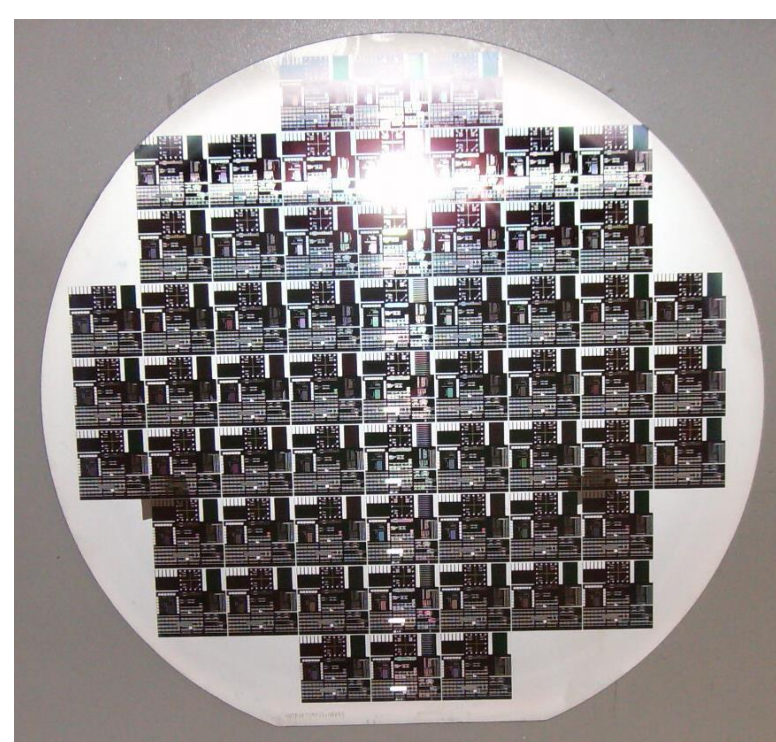


Bruce Furnace 02

Recipe 101: 450C, H_2N_2, 30min

ALUMINUM ETCH USING LAM4600

LAM4600



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LAM4600 ANISOTROPIC ALUMINUM ETCH

Step	1	2	3	4	5
Pressure	100	100	100	100	0
RF Top (W)	0	0	0	0	0
RF Bottom	0	250	125	125	0
Gap (cm)	3	3	3	3	5.3
O2 111	0	0	0	0	0
N2 222	13	13	20	25	25
BCl 333	50	50	25	25	0
Cl2 444	10	10	30	23	0
Ar 555	0	0	0	0	0
CFORM 666	8	8	8	8	8
Complete	Stabl	Time	Time	Oetch	Time
Time (s)	15	8	200	10%	15

Rate ~38Å/s

Thickness = 7500Å

Various tool modifications resulted in different etch rates for different years

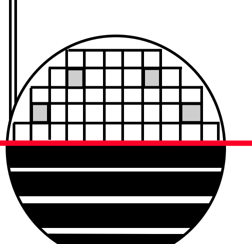
Channel	B
Delay	130
Normalize	10 s
Norm Val	5670
Trigger	105%
Slope	+

Endpoint (not used)

Fuller April 2013 – 200s

Fuller, January 2012 -300s

Fuller, March 2011 -230s



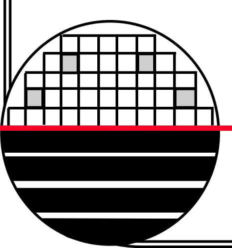
RESIST STRIP AND SINTER

P-well

N-well

Bruce Furnace 02

Recipe 101: 450C, H_2N_2, 30min



BRUCE FURNACE RECIPE 101 SINTER

SINTER Recipe #101

Verified:2-24-04

	Warm	Push	Stabilize	Soak	Anneal	Pull	
25 °C	450°C					25 °C	
Interval 0	**1**	**2**	**3**	**4**	**5**	**6**	
Any`	90	12	15	30	5	15	min
0 lmp	10	10	10	5	10	5	lpm
None	N2	N2/H2	N2/H2	N2/H2	N2	N2	

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

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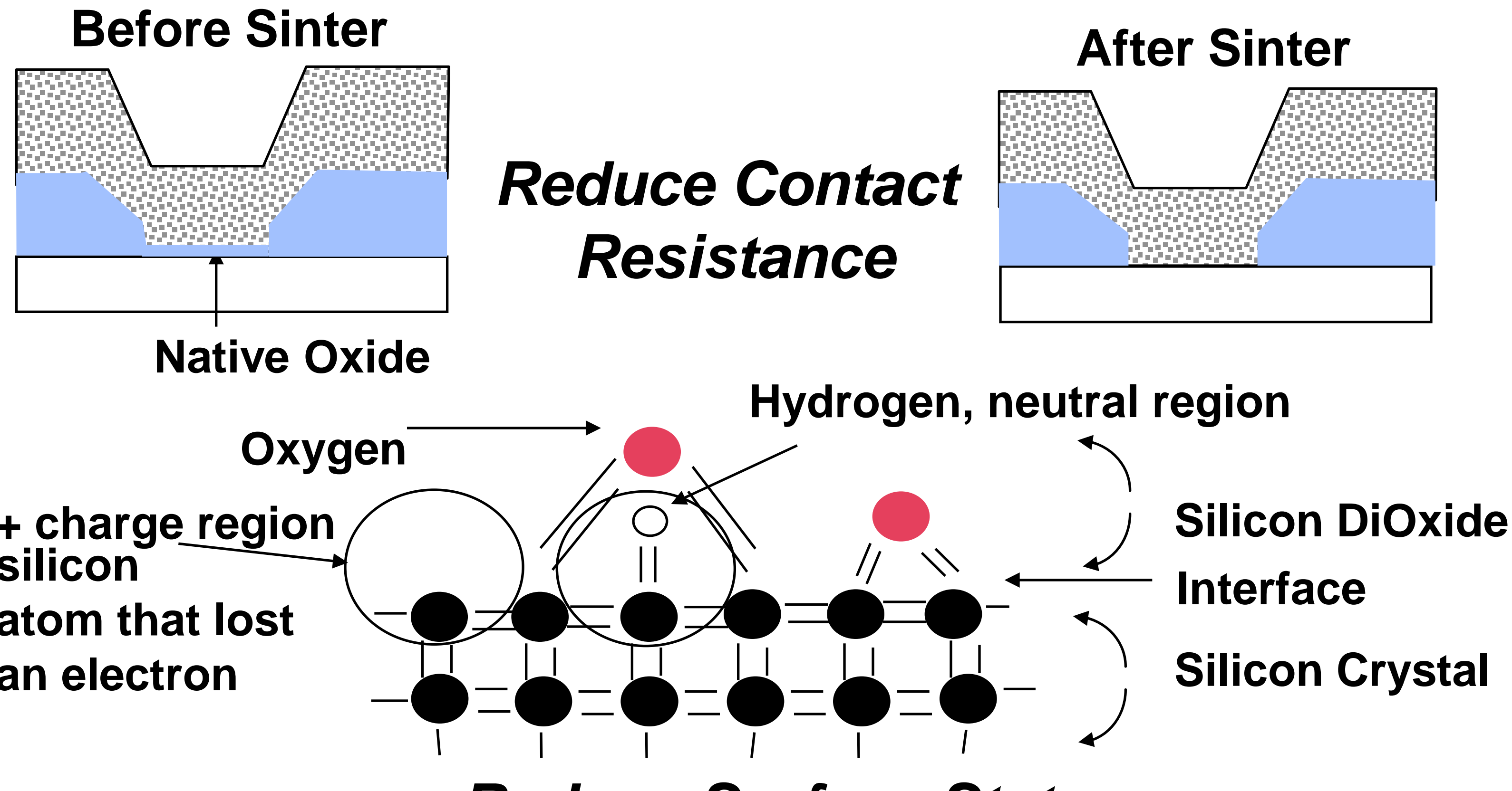
SINTER



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ADV-CMOS 150

NMOSFET

PMOSFET

N+ Poly

P+ Poly

N+ D/S

P+ D/S

p+ well contact

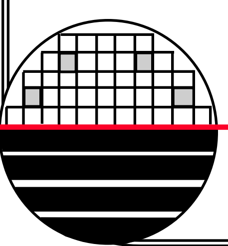
n+ well contact

LDD

LDD

P-well

N-well



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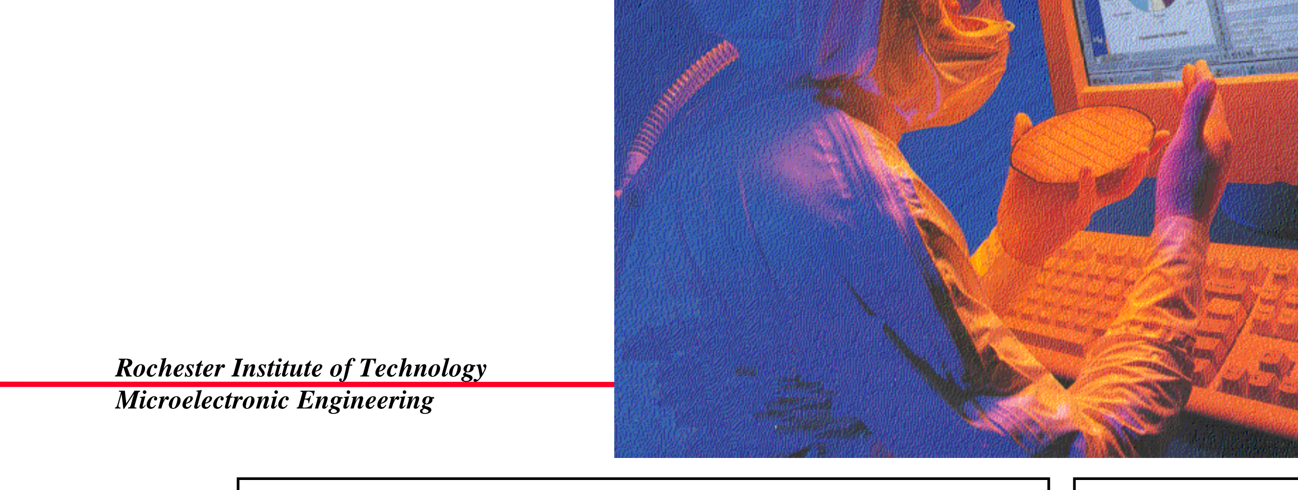
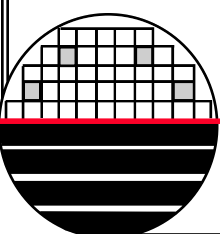
MESA WIPTRACKING SYSTEM

The process is long and complicated and will take many months to complete each lot. A computerized record keeping system is required to provide instructions and collect data. MESA (Manufacturing Execution System Application) from Camstar, Inc. runs on our AS/400 computer.



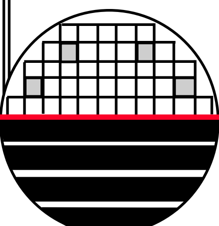
SUMMARY

The process described can be used down to ~0.25 µm gate length.



REFERENCES

1. Silicon Processing for the VLSI Era, Volume 1 – Process Technology, 2nd, S. Wolf and R.N. Tauber, Lattice Press.
2. The Science and Engineering of Microelectronic Fabrication, Stephen A. Campbell, Oxford University Press, 1996.



HOMEWORK – ADVCMOS PROCESS INTEGRATION

1. Why do we want the surface concentration under the shallow trench in the p-well to be above some given value?
2. Why are the well implant energies greater than 150 KeV?
3. When checking material thickness for the ability to block D/S implant, which implant type and which material is the most critical.
4. Why is a nitride spacer (instead of oxide) used.
5. What are the two main purposes of the silicide in this process?
6. Why is the gate doped N-type on the NMOS and P-type on the PMOS devices?
7. What is the poly sheet resistance?
8. What is the purpose of the N2O in the gate oxide growth recipe?