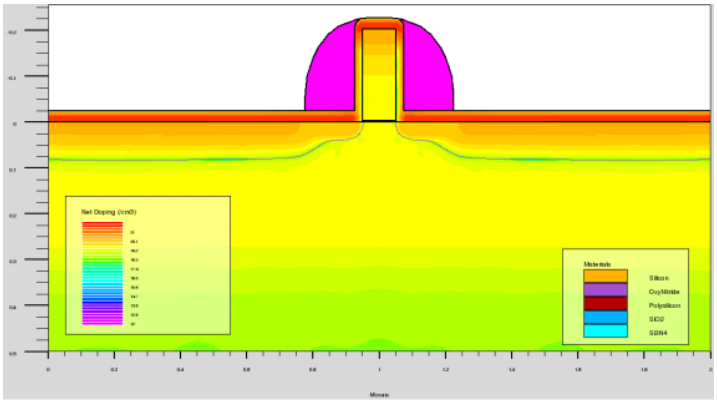
MODELING AND SIMULATION OF 100NM PMOS AND NMOS DEVICES ON ATHENA AND ATLAS



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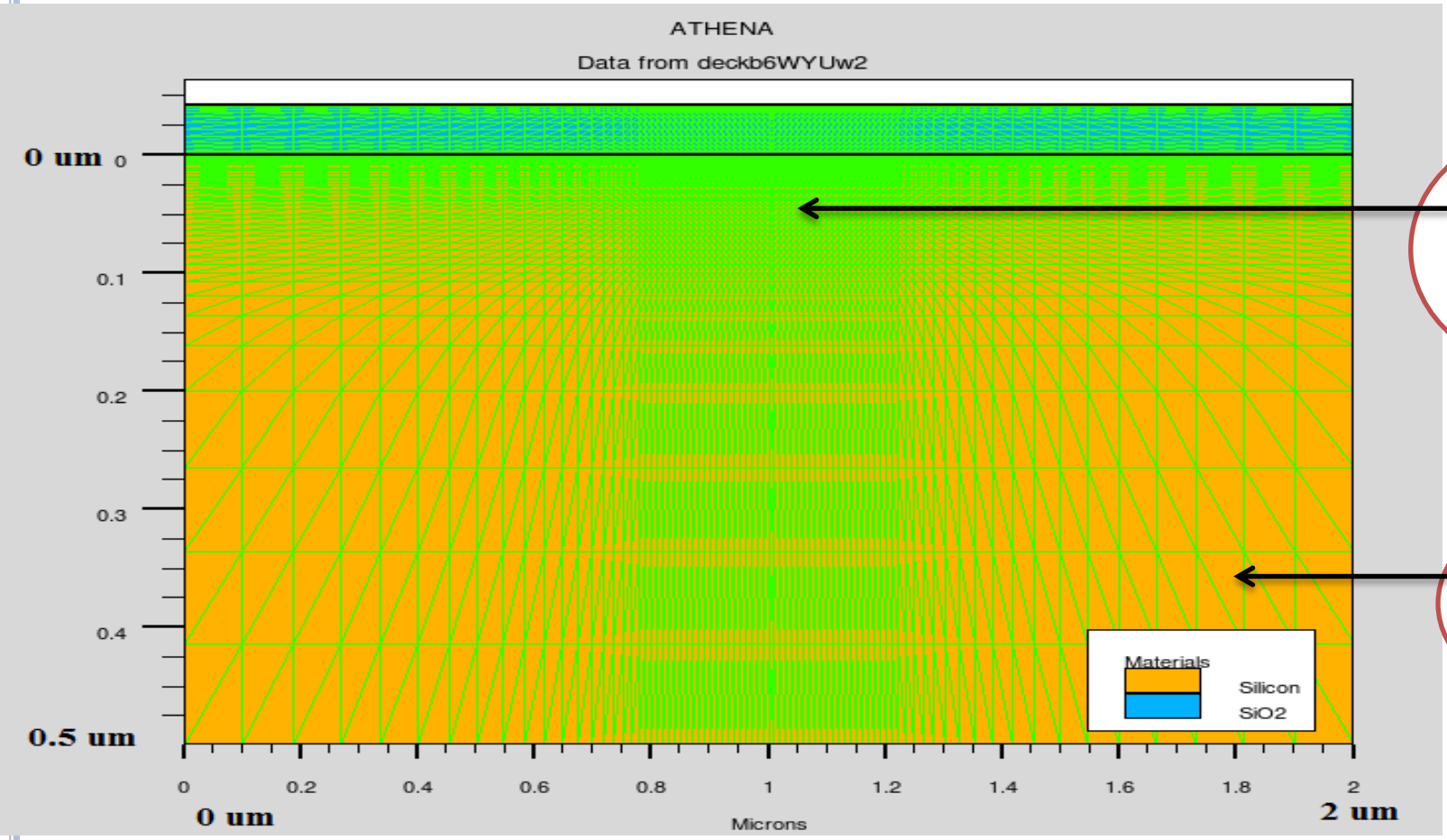
ASSUMPTIONS

- Underlying silicon simulation thickness considered in the following slides are 0.5μm.
- Background wafer thickness is increased to 1.8 μm to observe the dopant distribution after well drive in.
- Lithography steps are ignored since PMOS and NMOS devices are simulated as two separate devices.
- Recessed oxide growth is modeled separately from the device structure.
- Advanced diffusion and implant models are used in ATHENA modeling.

  Diffusion model – Fully coupled

  Implant model – Monte Carlo implant.

GRID SPACING



Grid spacing is very fine in the channel region.

Course in the bulk

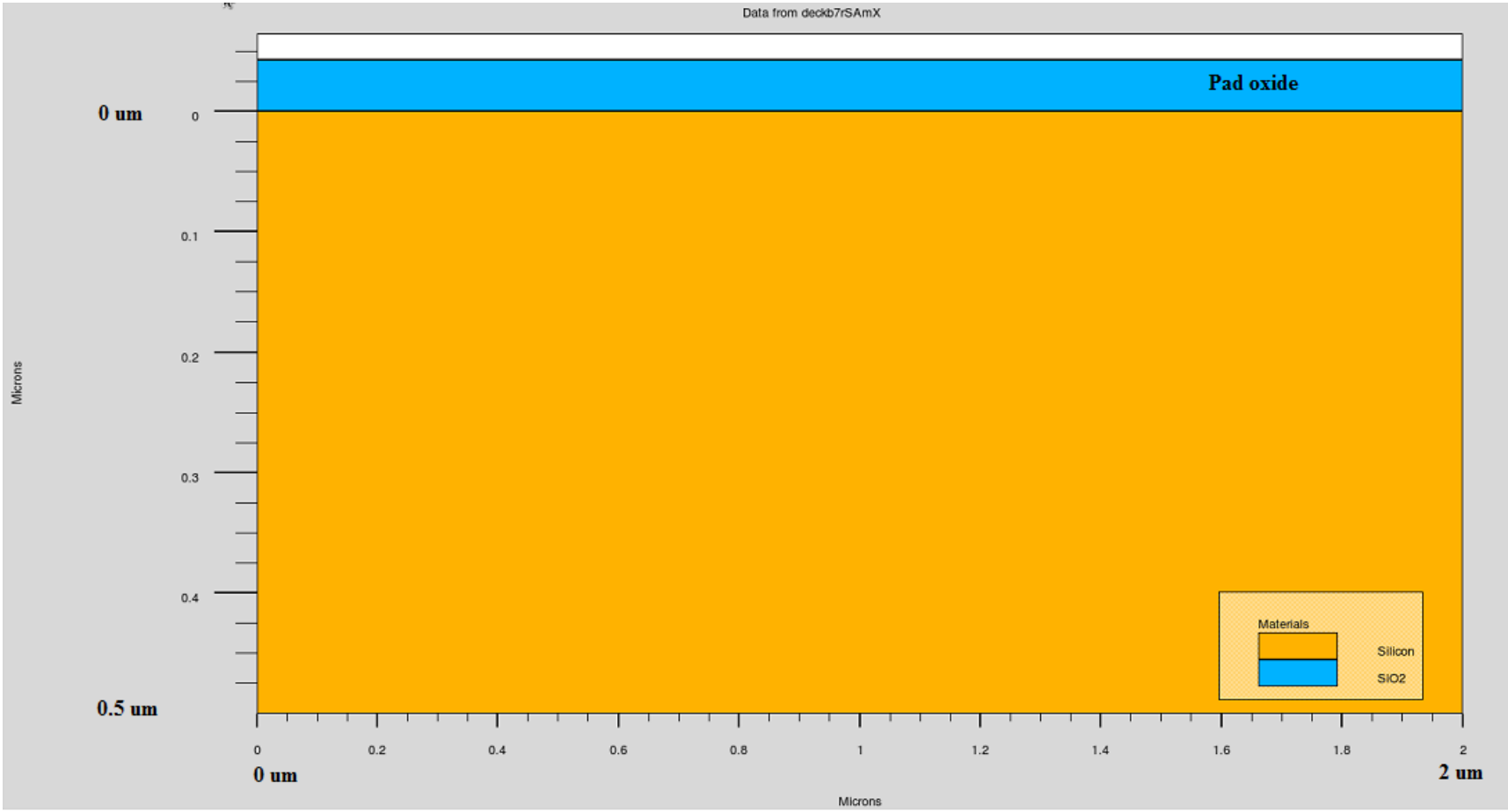
Grid parameter definition for both X and Y Co-ordinates

line x loc=0.00 spac=0.1
line x loc=0.8 spac=0.01
line x loc=1.0 spac=0.01

line y loc=0.00 spac=0.001
line y loc=0.1 spac=0.01
line y loc=0.2 spac=0.1
line y loc=0.5 spac=0.1

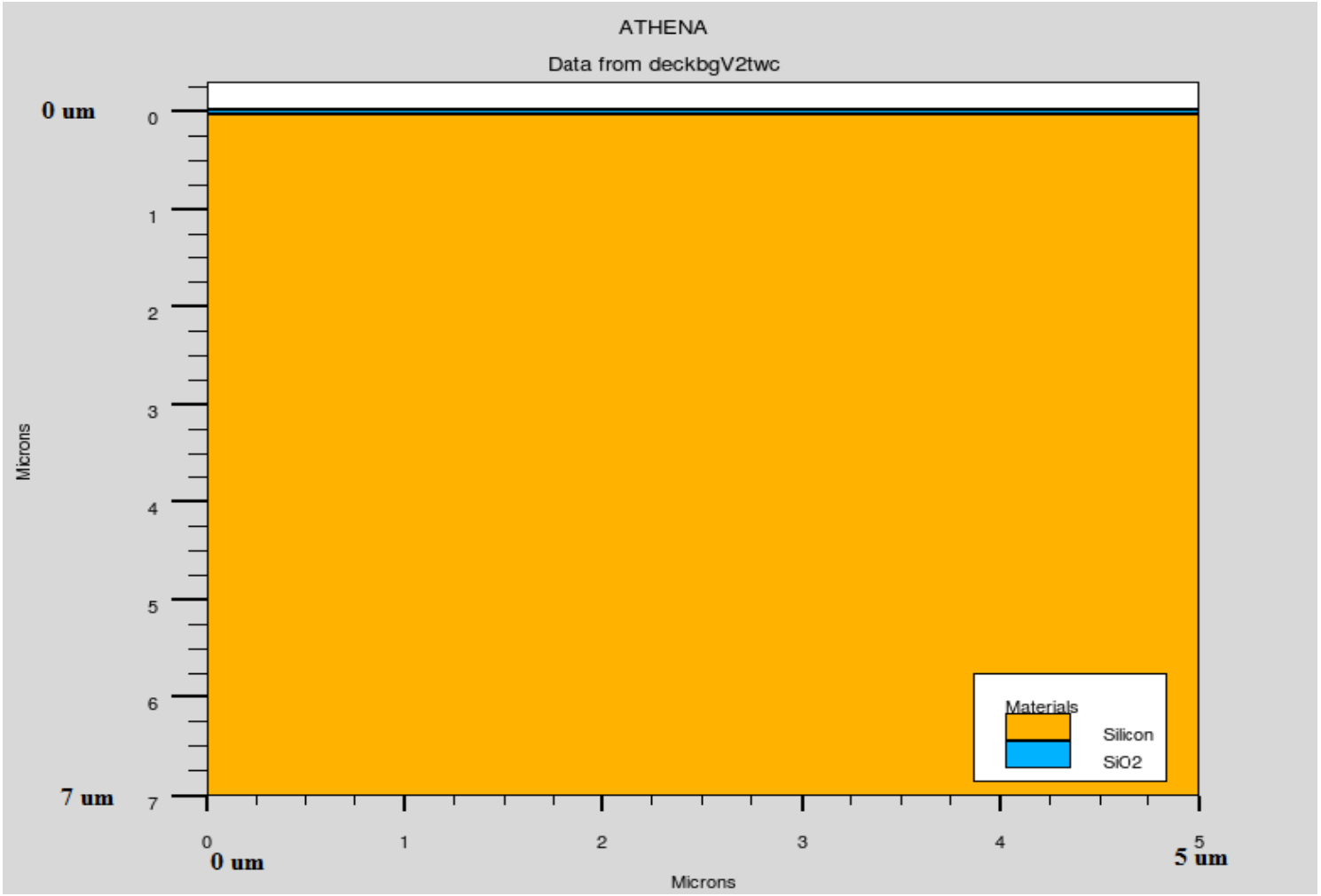
STARTING WAFER WITH PAD OXIDE

- Both NMOS and PMOS devices are modeled on P-type wafer, with resistivity = 20 Ω-*cm*.



The figure above is the starting wafer with Pad oxide grown on it using 500*Å* pad oxide growth recipe.

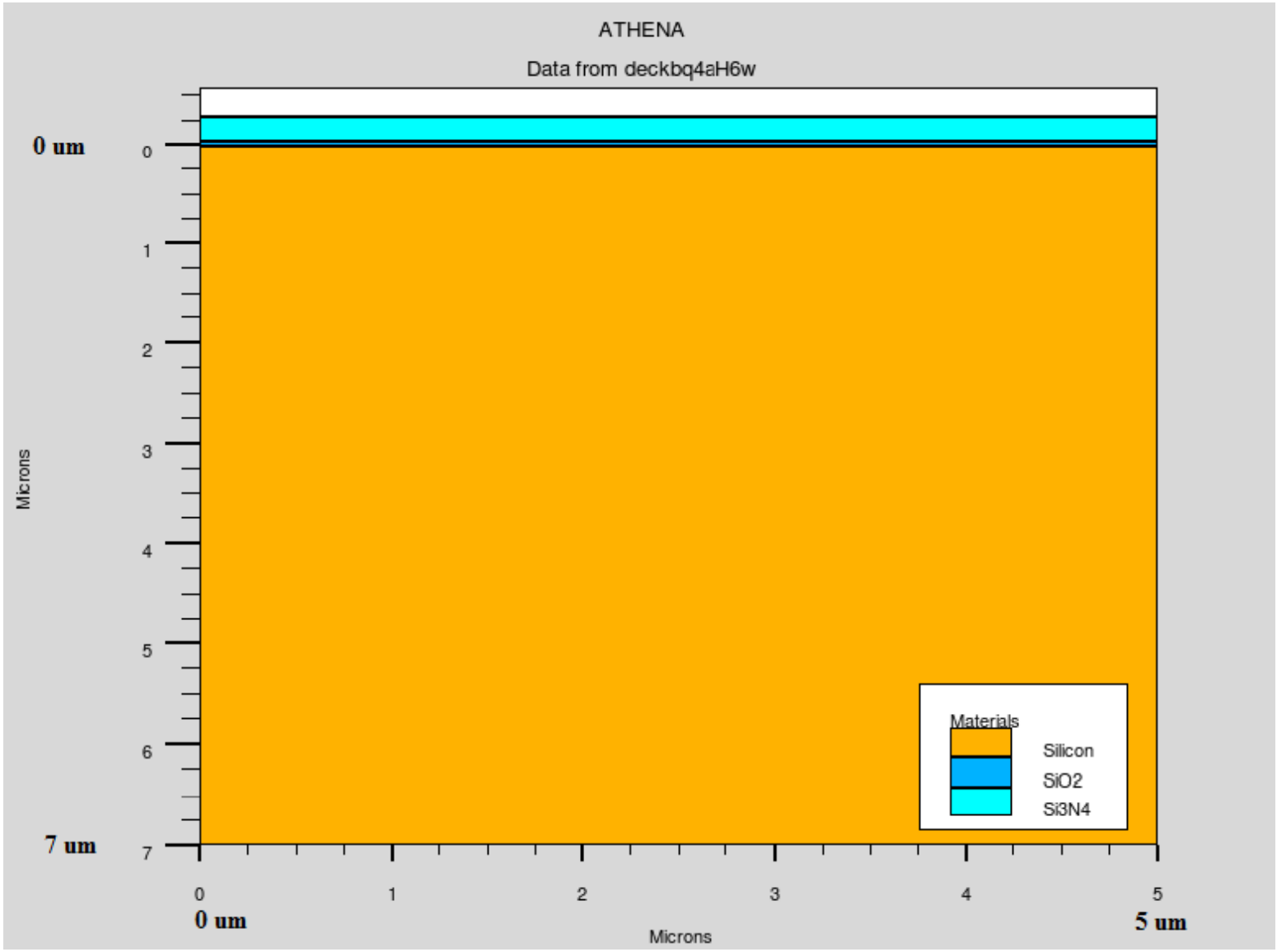
RECESSED OXIDE GROWTH SIMULATIONS



The grid is increased to **7 *μm* in X direction** and **5 *μm* in Y direction** for recessed oxide simulations.

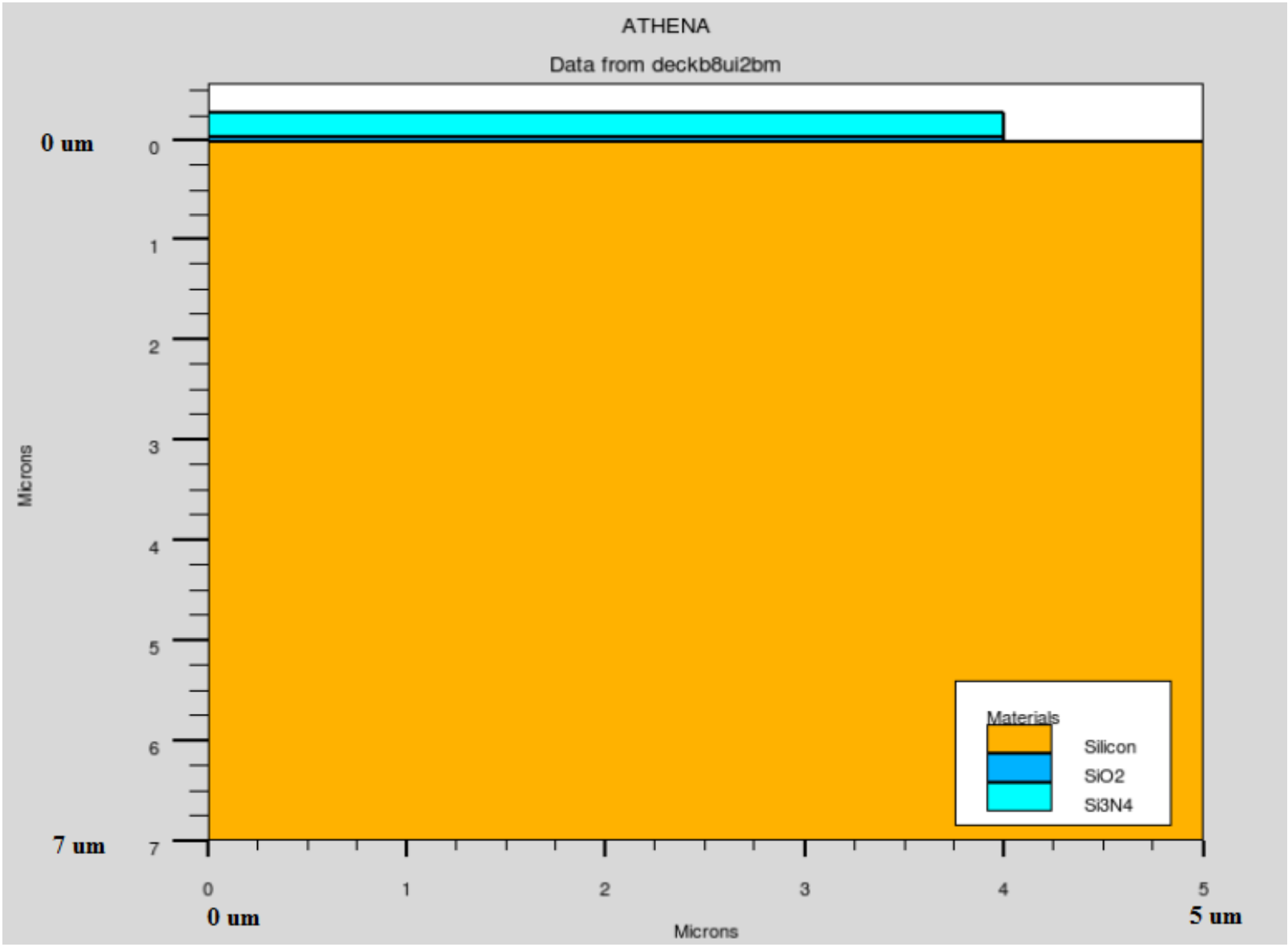
500 *Å* pad oxide is grown.

Recessed Oxide Growth Simulations



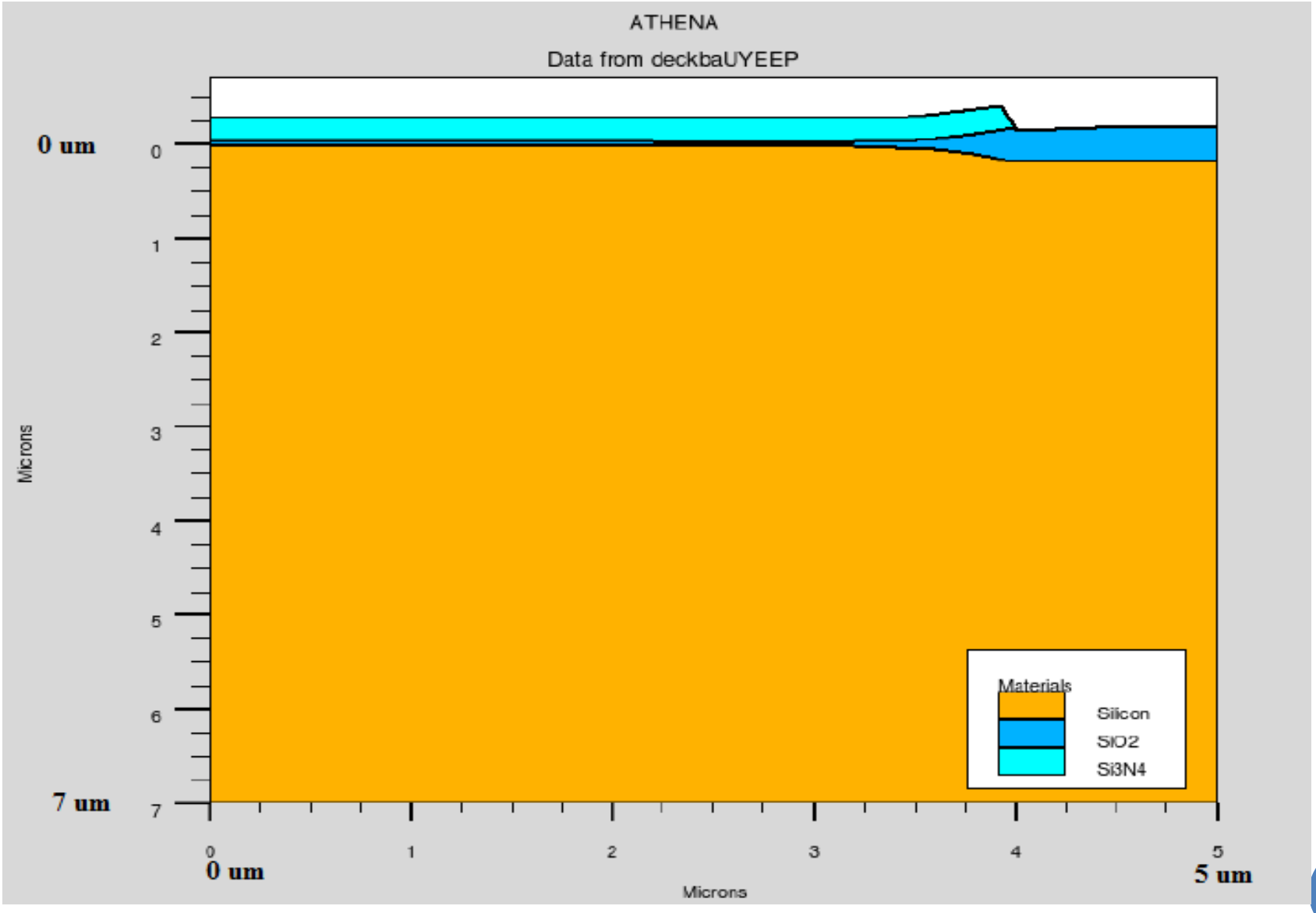
Deposit **1500** ***Å*** thick nitride.

Recessed Oxide Growth Simulations



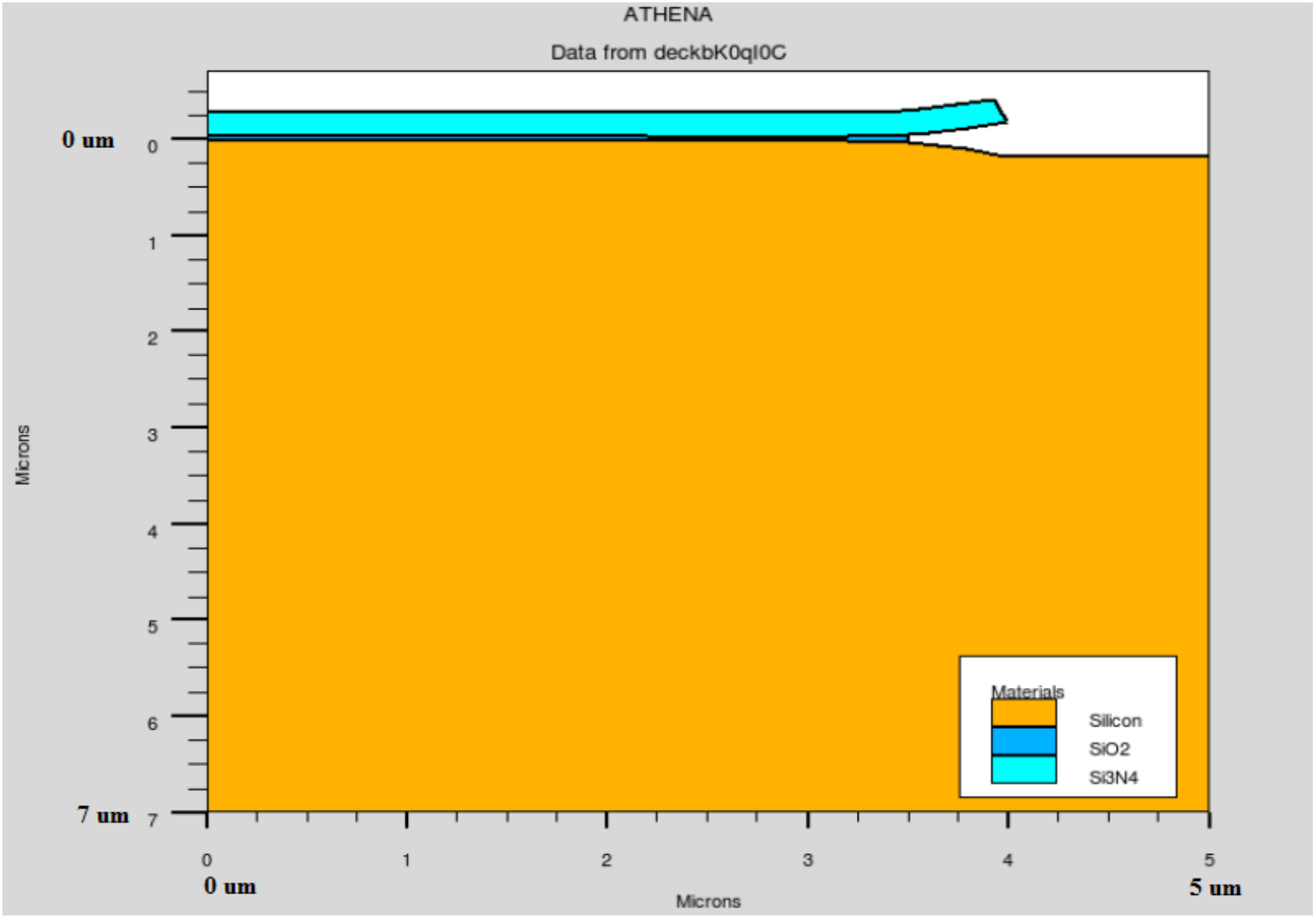
Etch nitride.

RECESSED OXIDE GROWTH SIMULATIONS



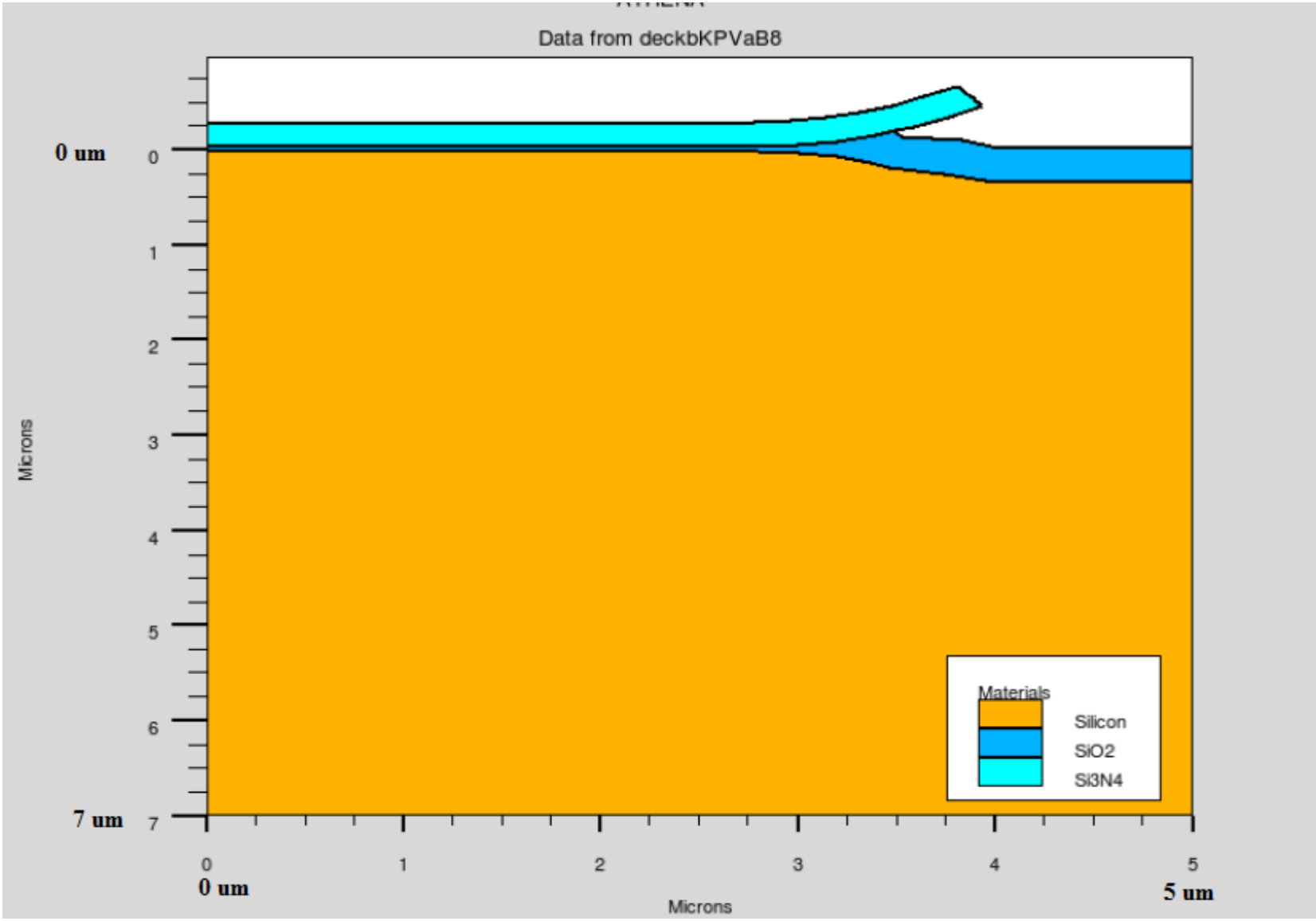
Grow **3500 *Å*** field oxide – First Wet Oxide Growth

RECESSED OXIDE GROWTH SIMULATIONS



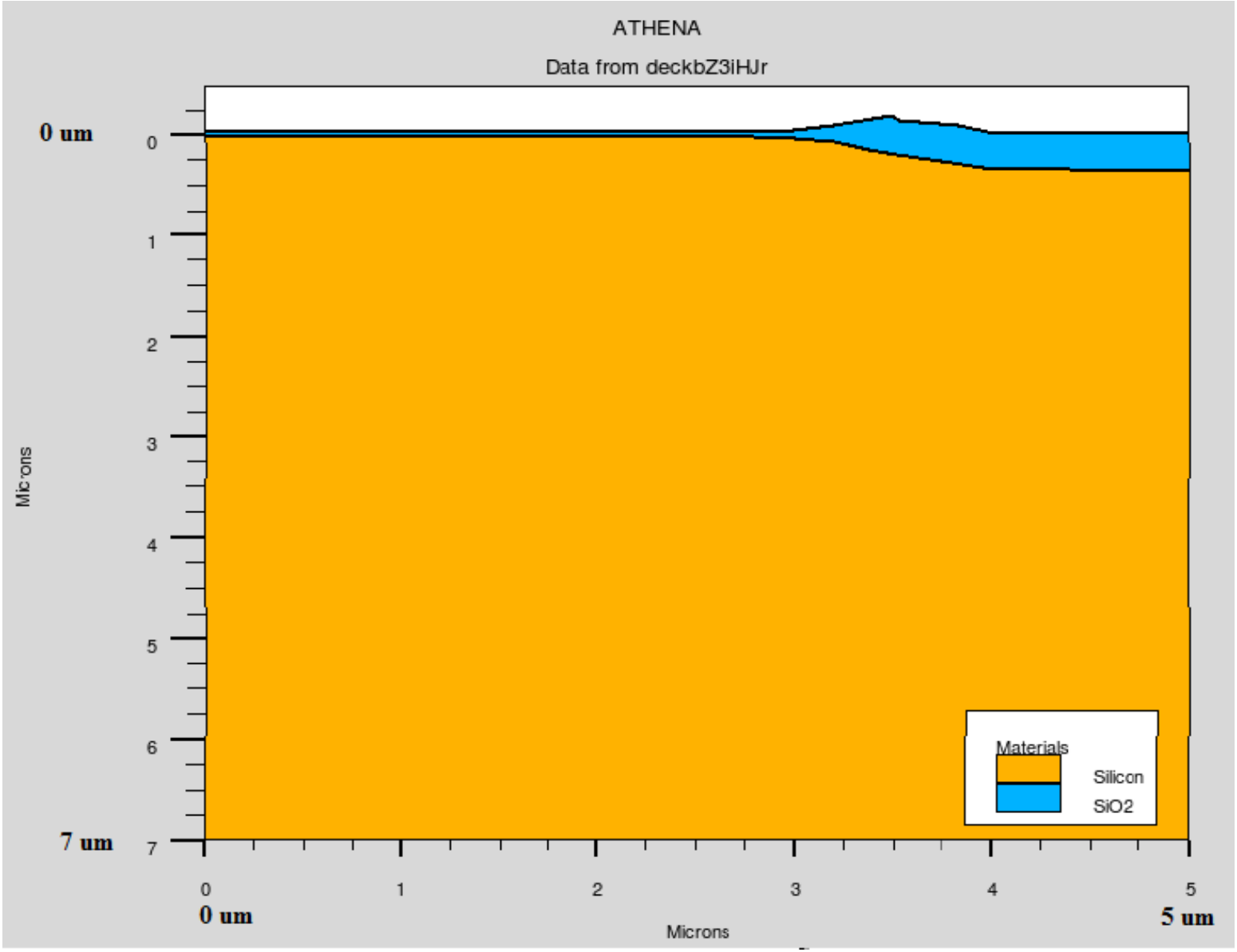
Etch oxide for a long time to get steeper undercut so that almost planar profile is obtained in the second oxide growth.

Recessed Oxide Growth Simulations



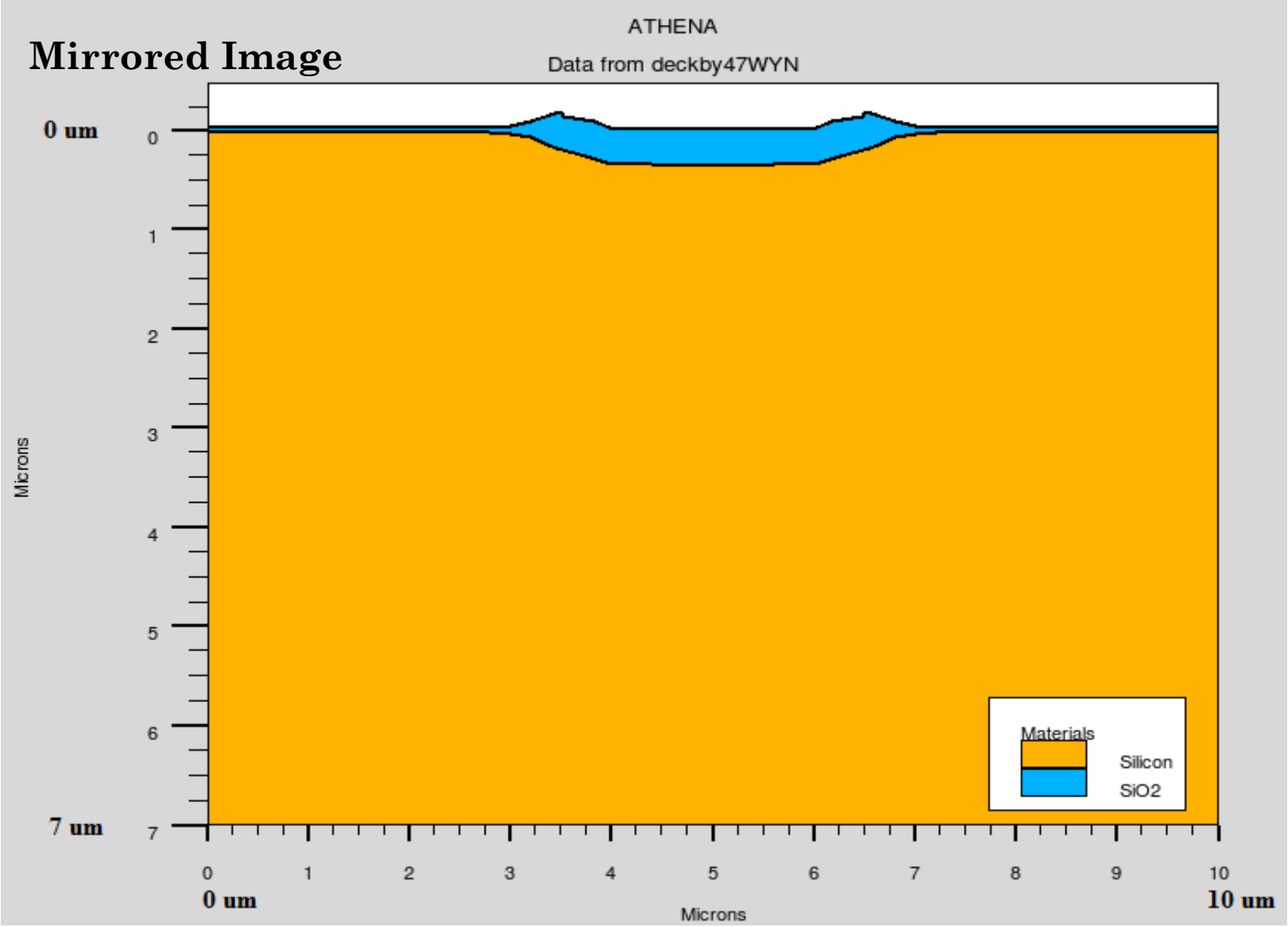
Grow **3500 *Å*** field oxide – Second Wet Oxide Growth

Recessed Oxide Growth Simulations

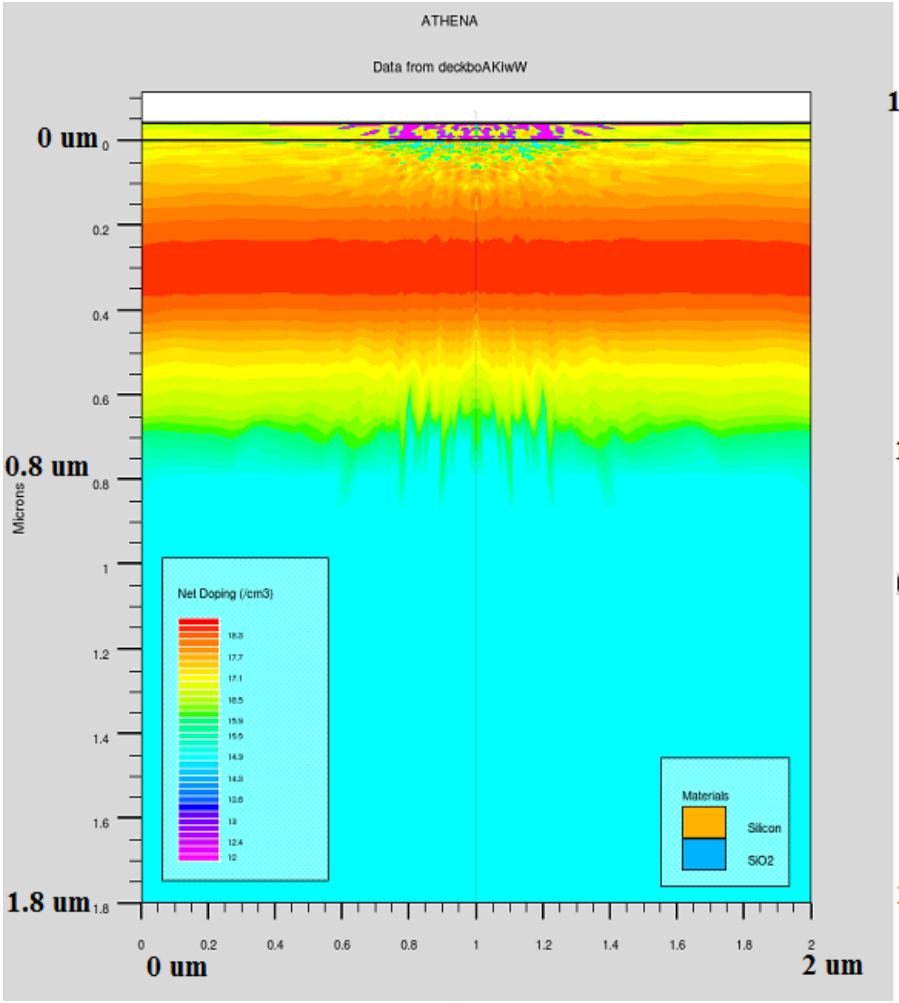


Etch all nitride.

Recessed Oxide Growth Simulations



WELL IMPLANTS-NMOS (PWELL)



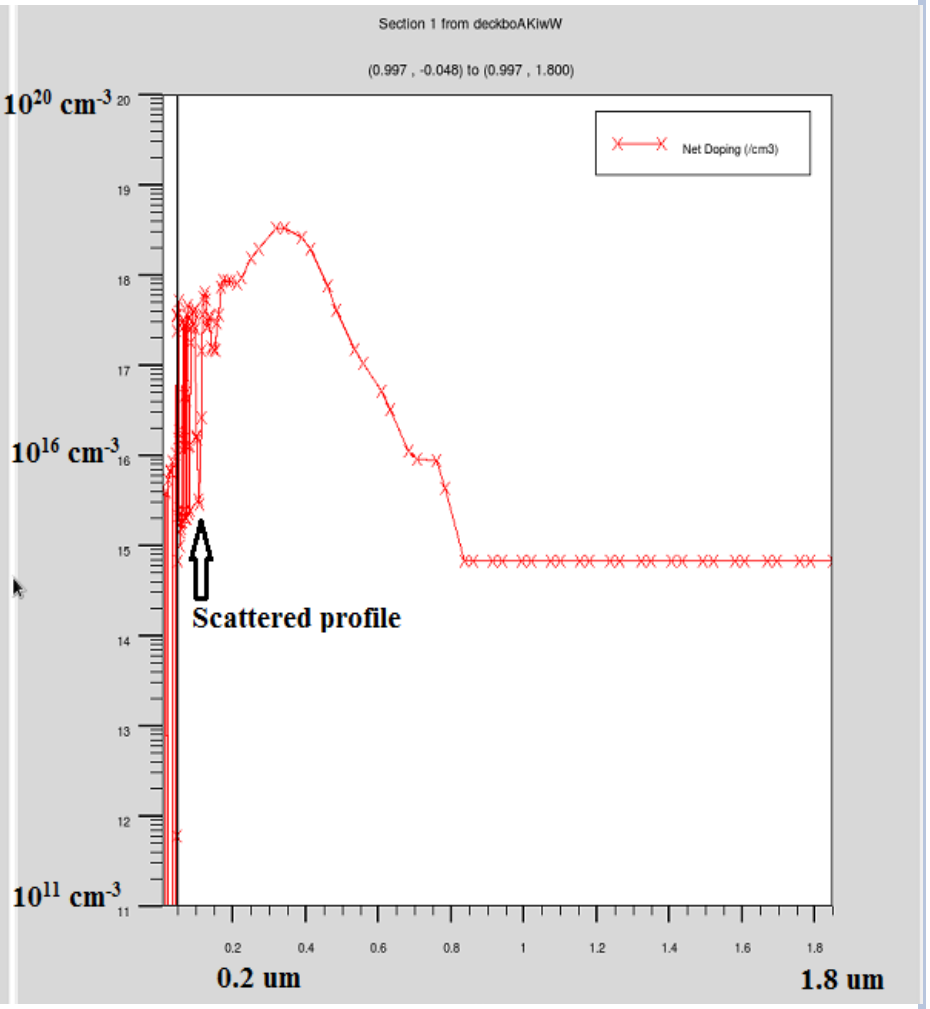


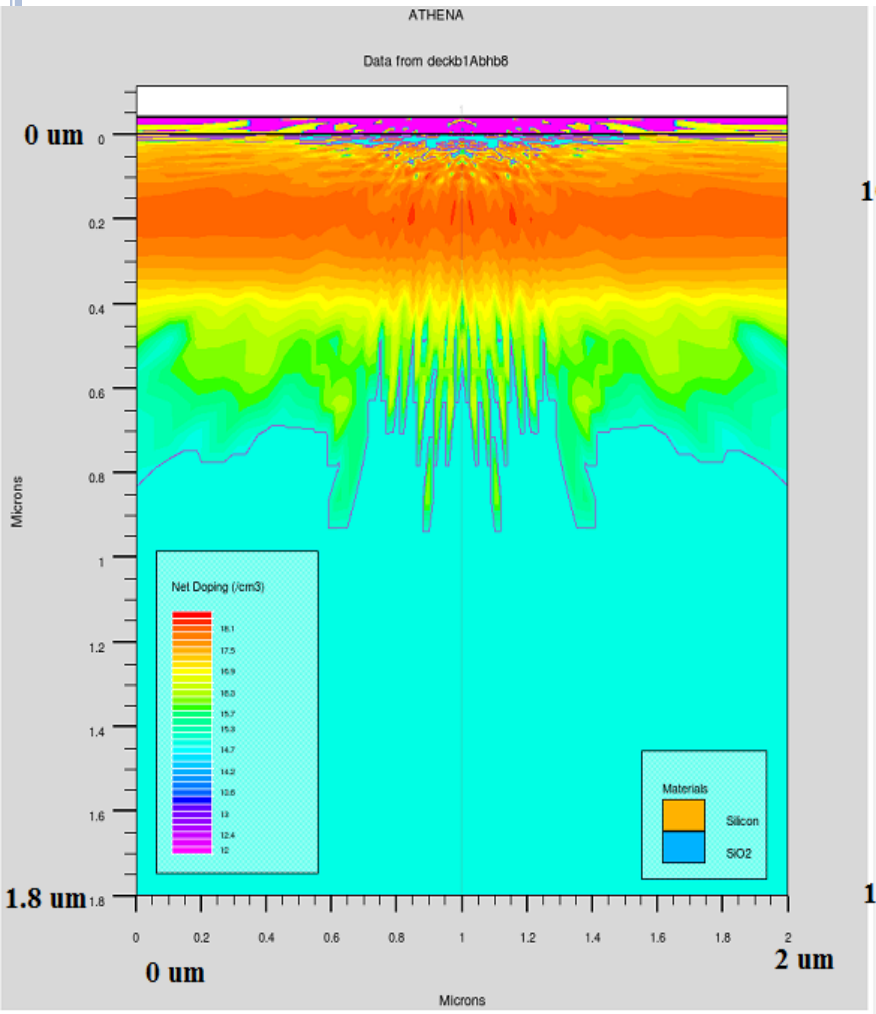
Figure on the left shows the scattering of impurities in Silicon and Figure on the right shows the scattered profile after well implant.

Impurity – Boron

Dose – 7.0e13 *cm*$^{-2}$

Energy – 100 *KeV*

WELL IMPLANTS-PMOS (N WELL)



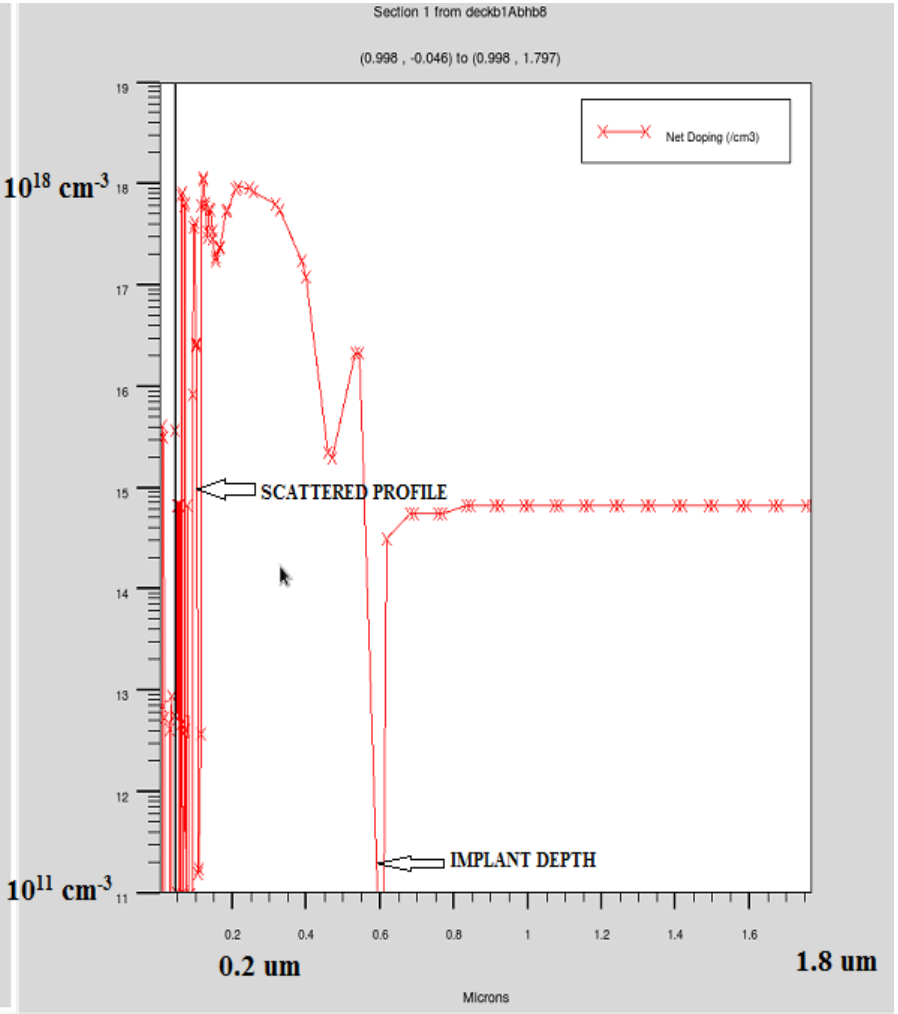


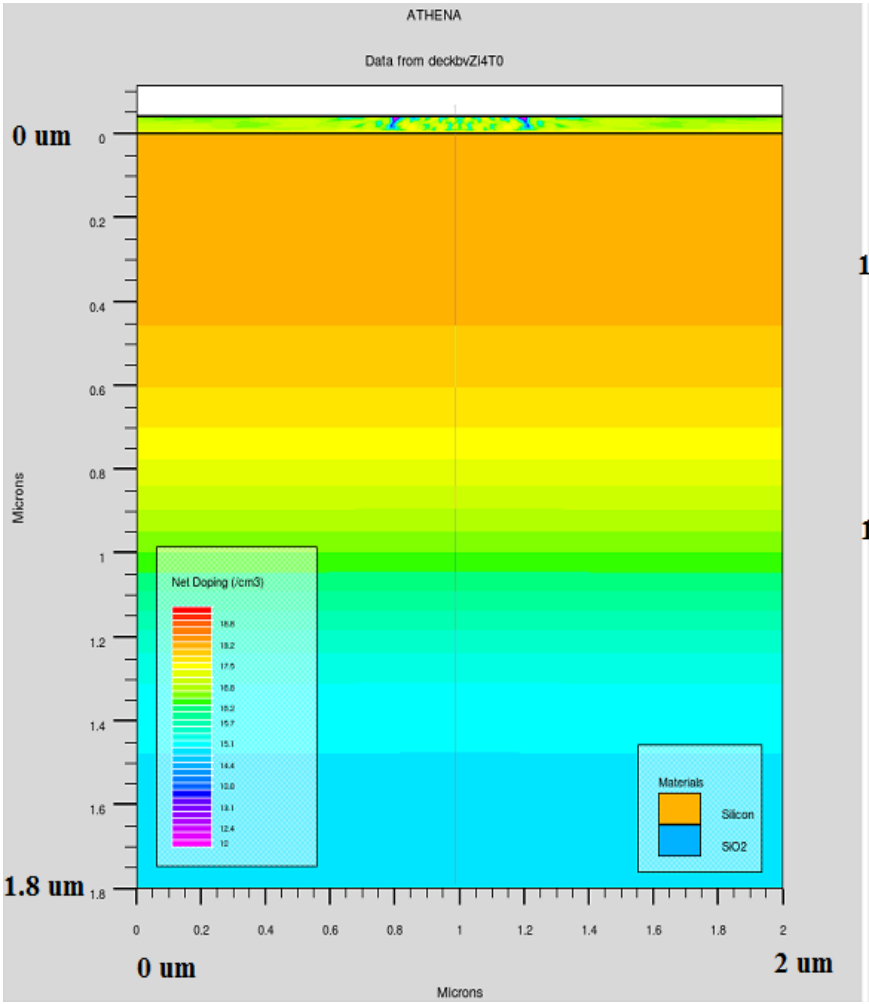
Figure on the left shows the scattering of impurities in Silicon and Figure on the right shows the scattered profile after well implant.

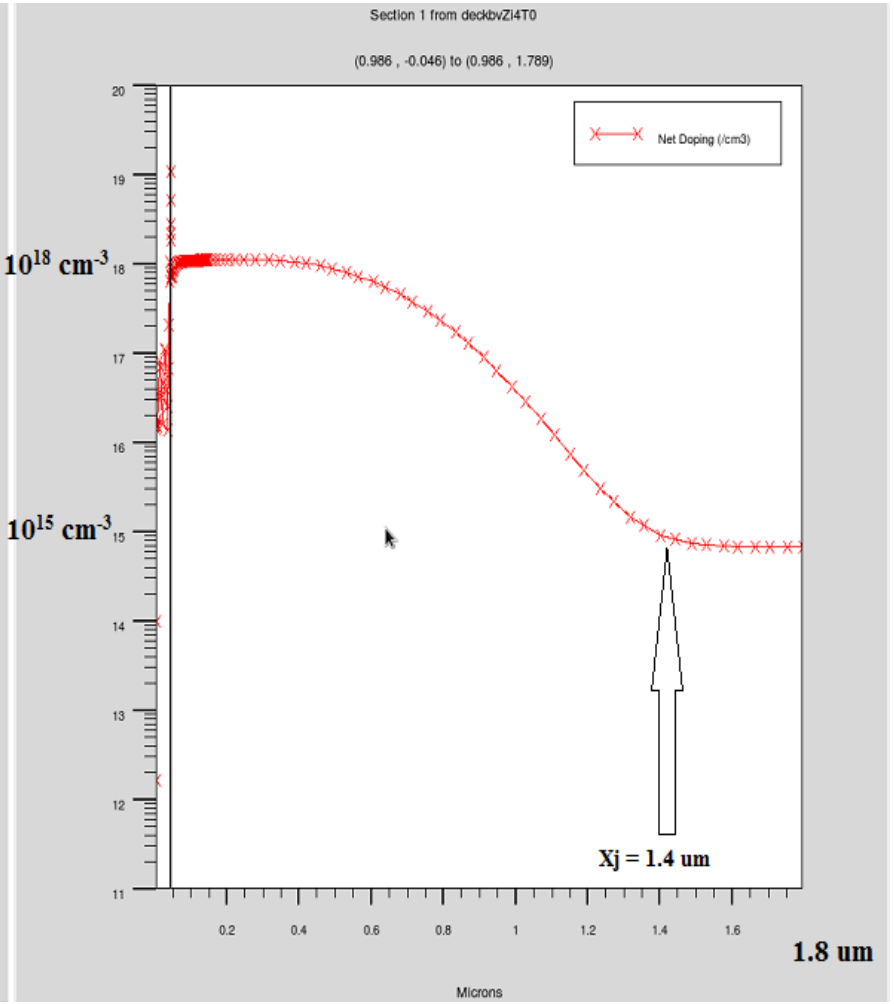
Impurity – Phosphorus

Dose – 5.0e13 *cm*$^{-2}$

Energy – 170 *KeV*

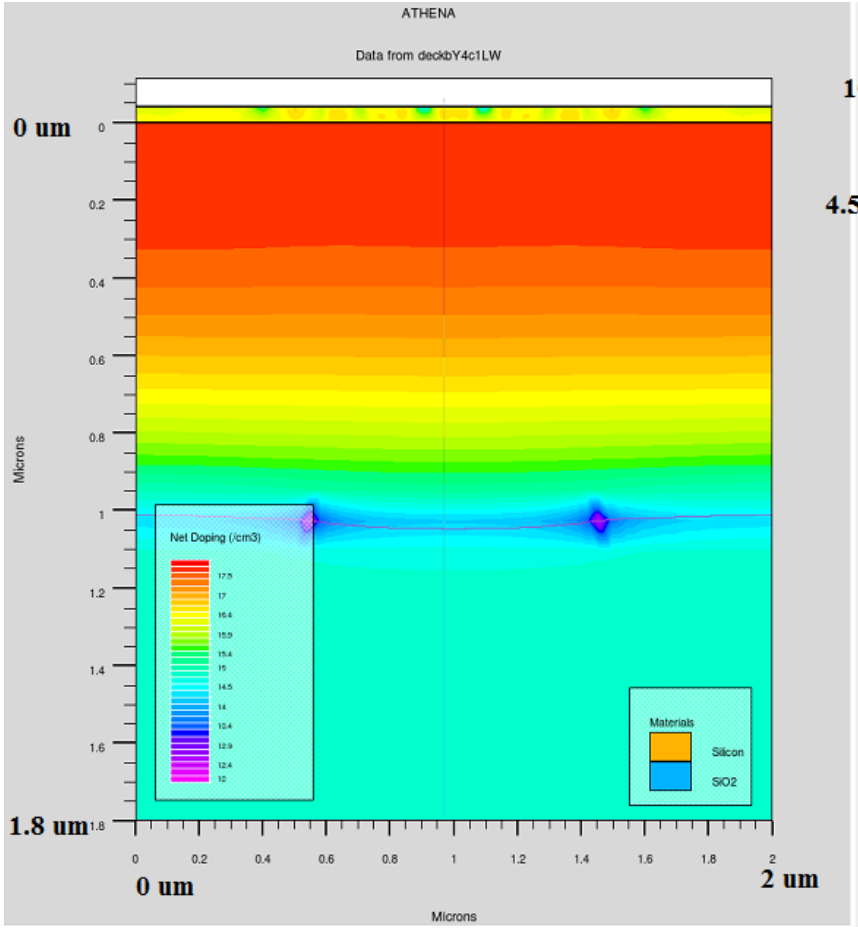
WELL DRIVE-IN: NMOS(PWELL)

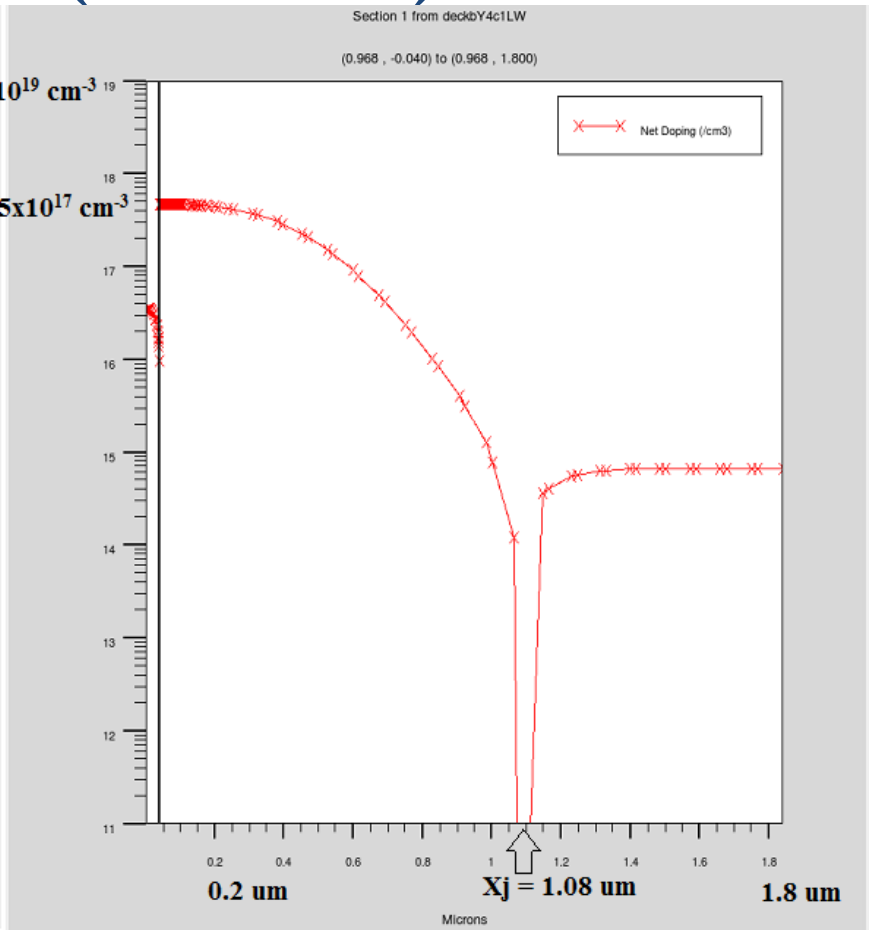




Well Drive-In:
4 hours soak: Nitrogen Ambient
Temp: 1000˚*C*
Junction depth: 1.4 *μm*

WELL DRIVE-IN: PMOS(NWELL)

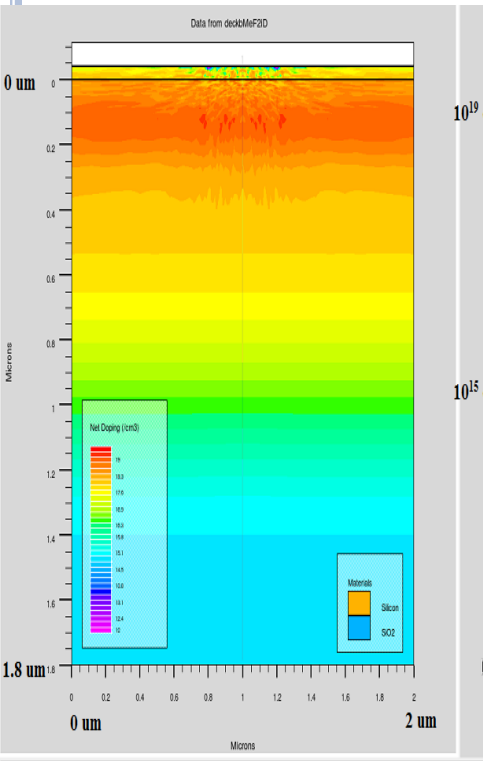


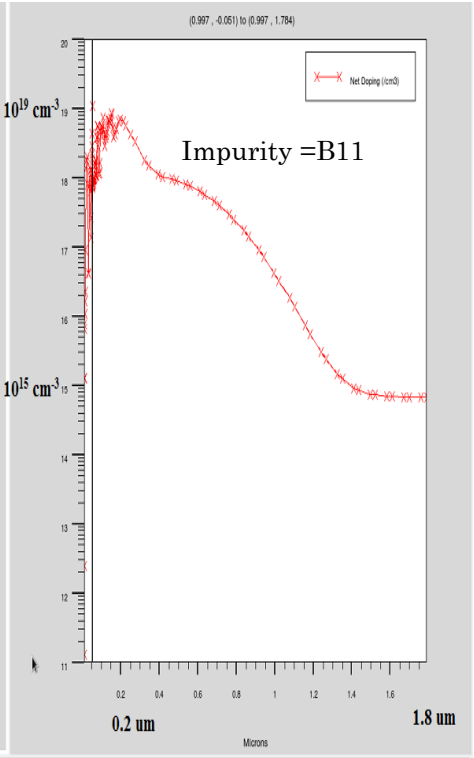


Well Drive-In:
4 hours soak: Nitrogen Ambient
Temp: 1000˚C
Junction depth: 1.08 *μm*

RETROGRADE WELL IMPLANT

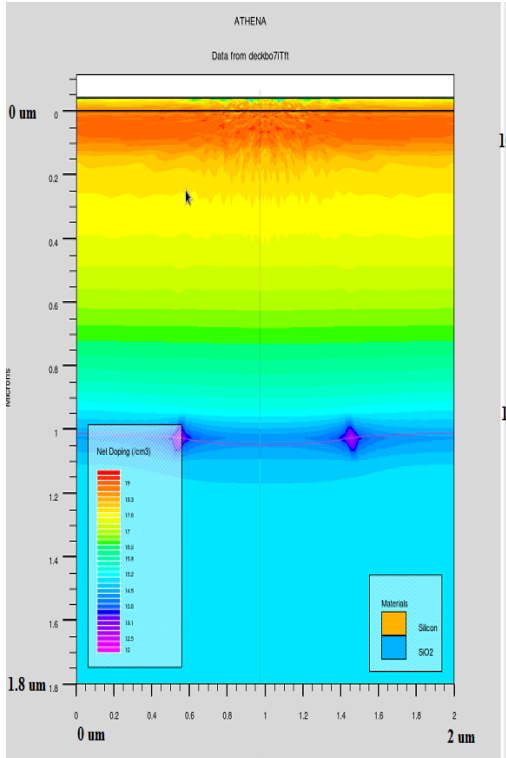
NMOS

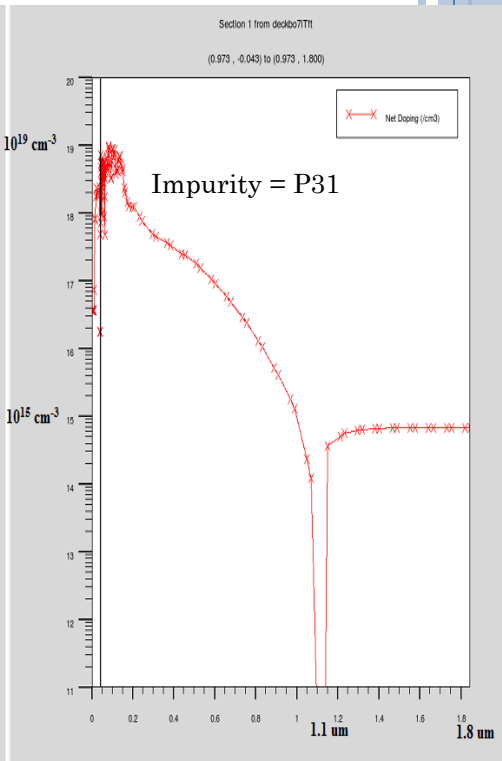




Retrograde Well Implant
Impurity: Boron
Dose: 1.0e14 *cm*$^{-2}$
Energy: 45 *KeV*

PMOS



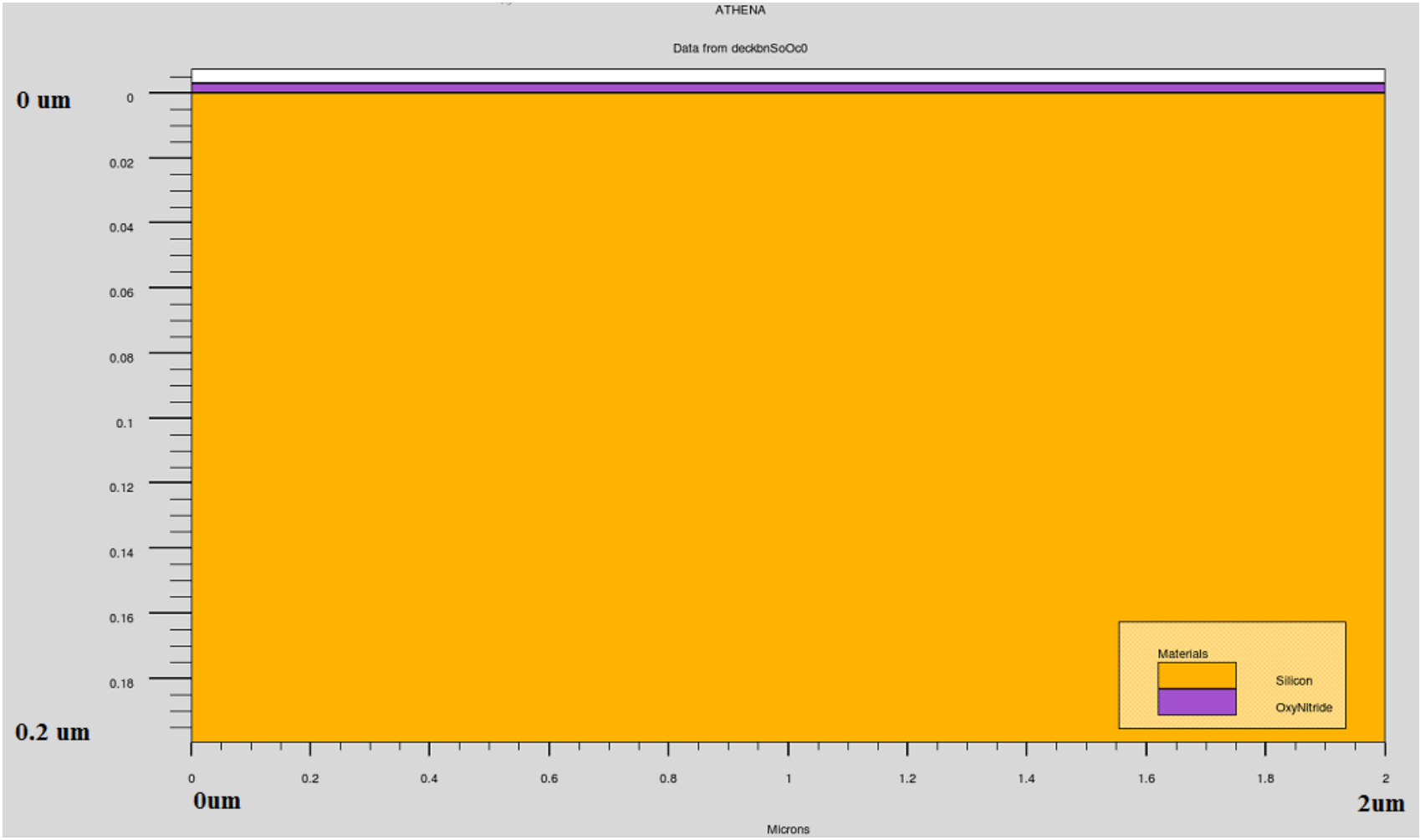


Retrograde Well Implant
Impurity: Phosphorus
Dose: 9.0e13 cm^{-2}
Energy: 70 KeV

Retrograde profile can be noticed after a thermal anneal or after a thermal oxide growth step

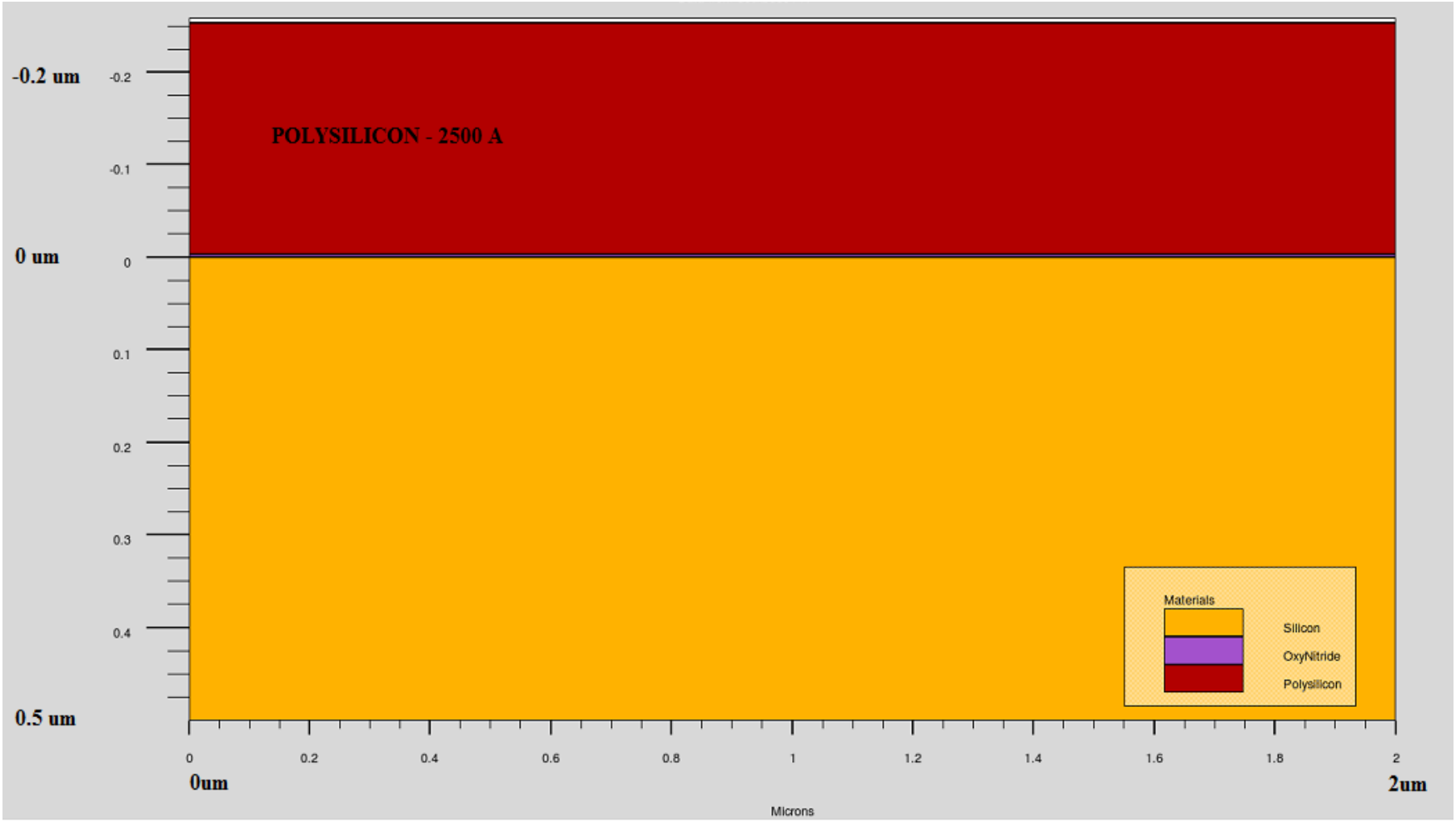
GATE OXIDE GROWTH

The thickness of the gate oxide is **30*Å***.



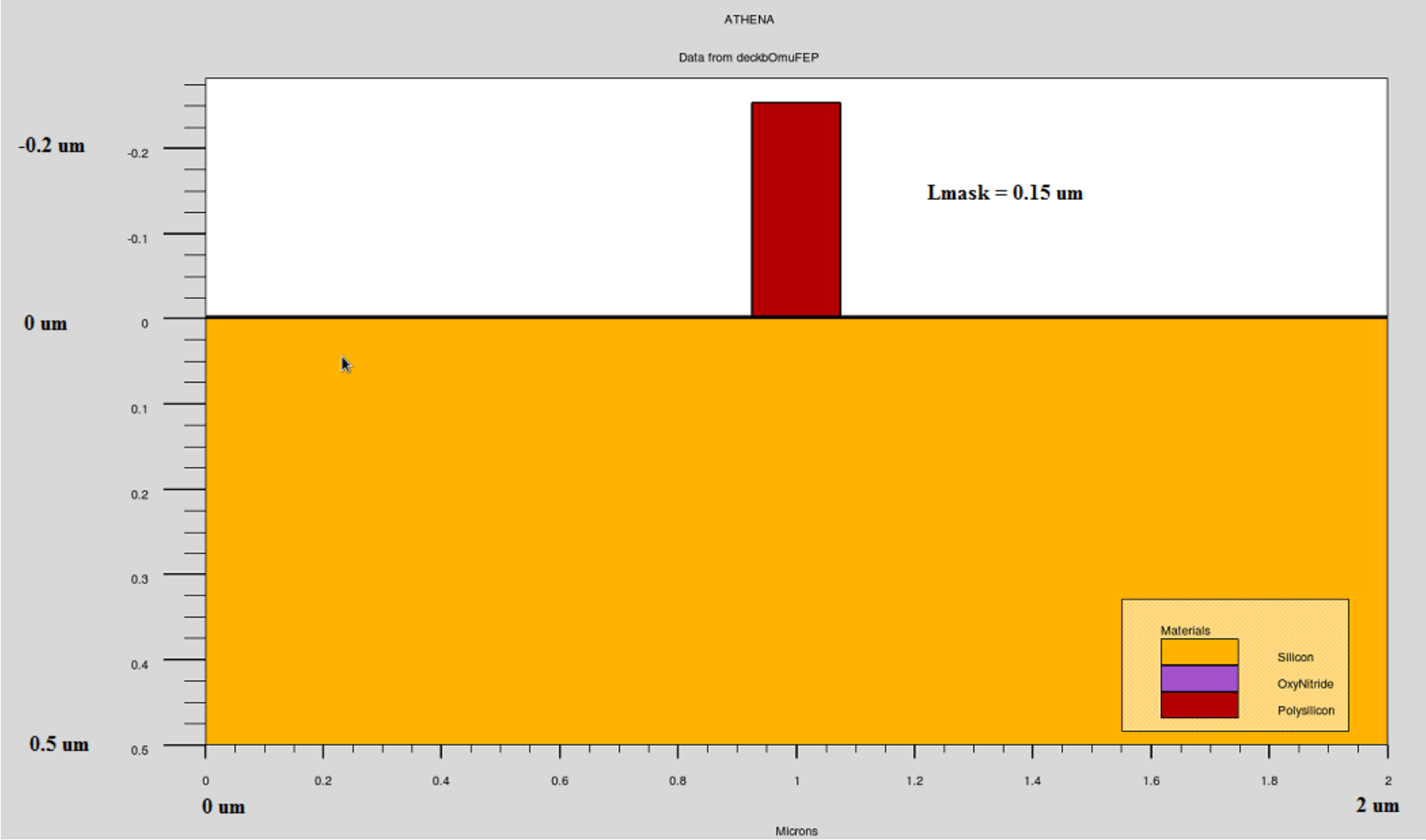
ATHENA does not model the incorporation of nitrogen in the gate oxide growth. So, Oxy-Nitride is deposited as a dielectric material in this model.

POLY-SILICON DEPOSITION



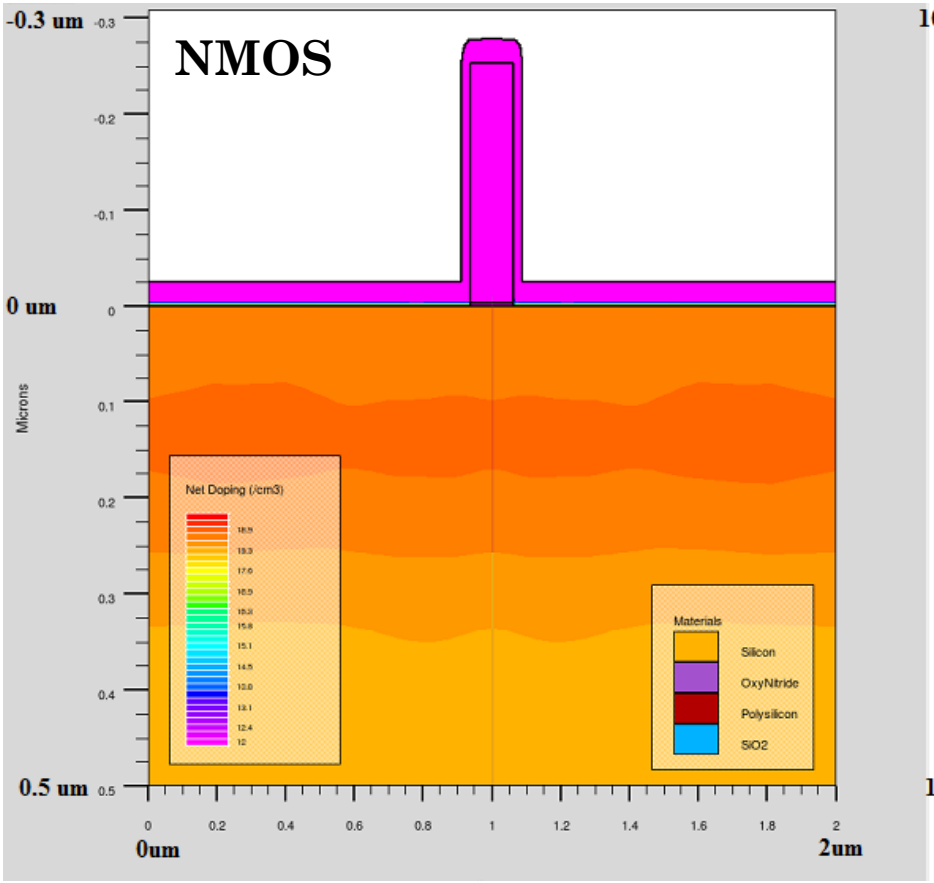
A layer of Poly-Silicon is deposited at 610ºC. Poly is **2500Å** thick.

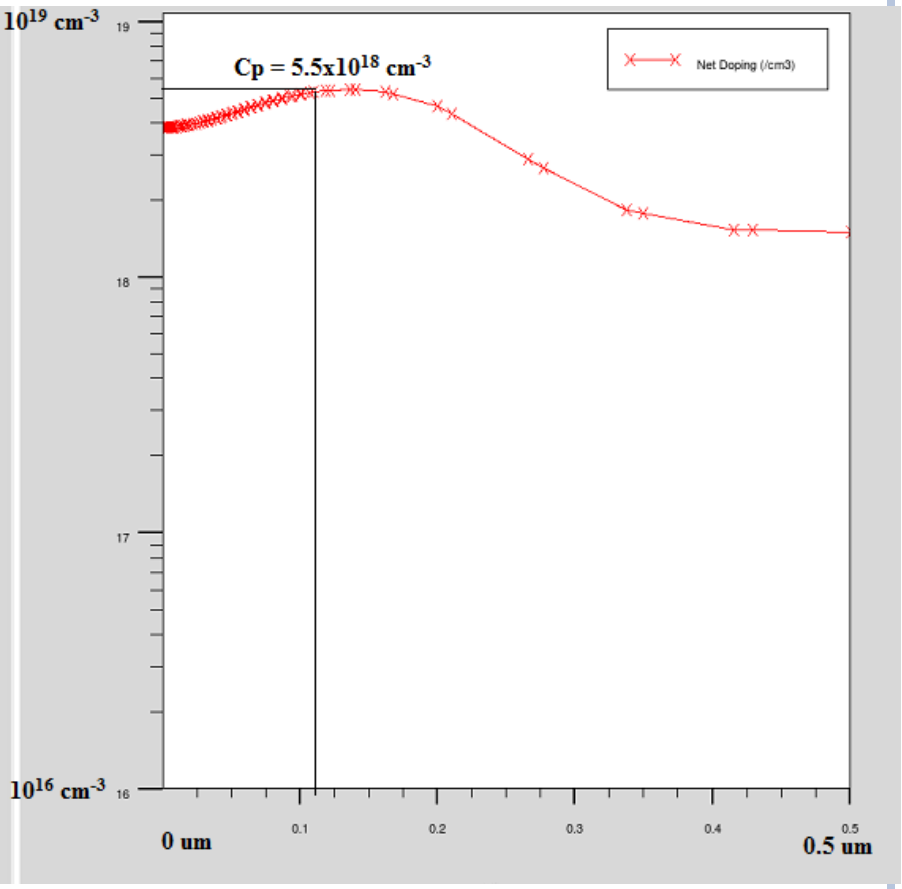
ETCH POLY-SILICON



The Mask length of Poly-Silicon is **150*nm***. And this length is achieved by double exposure in ASML Stepper.

POLY RE-OXIDATION AND RETROGRADE WELL PROFILE



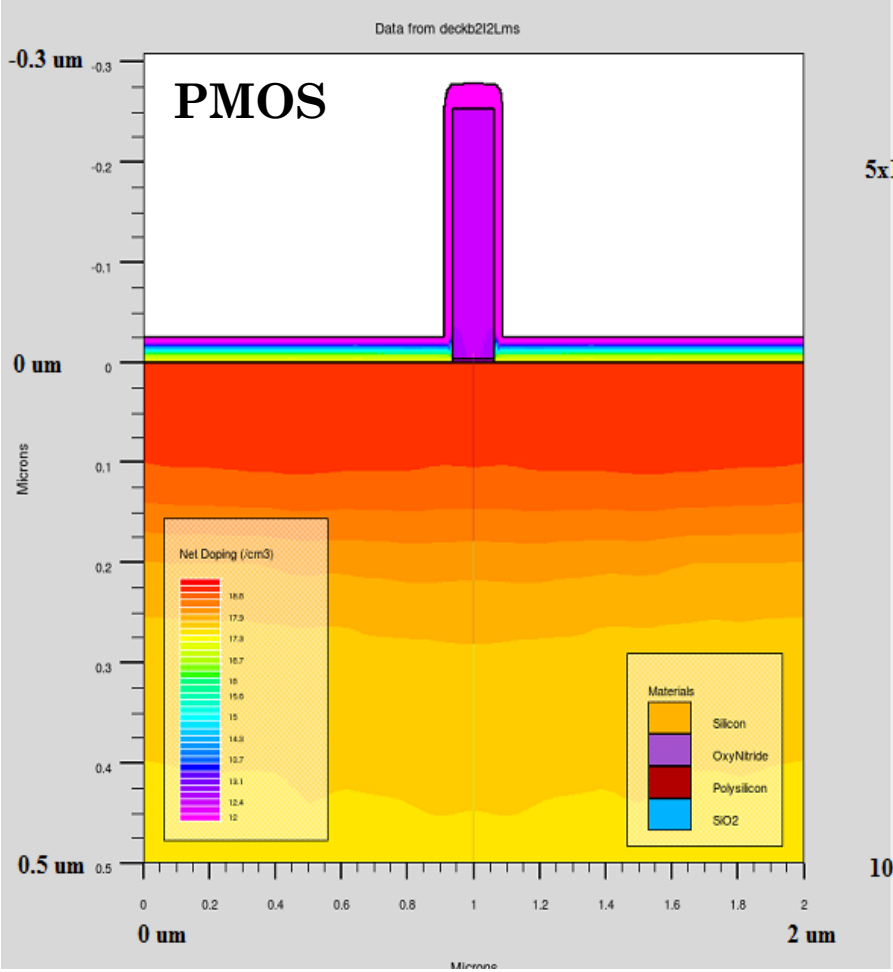


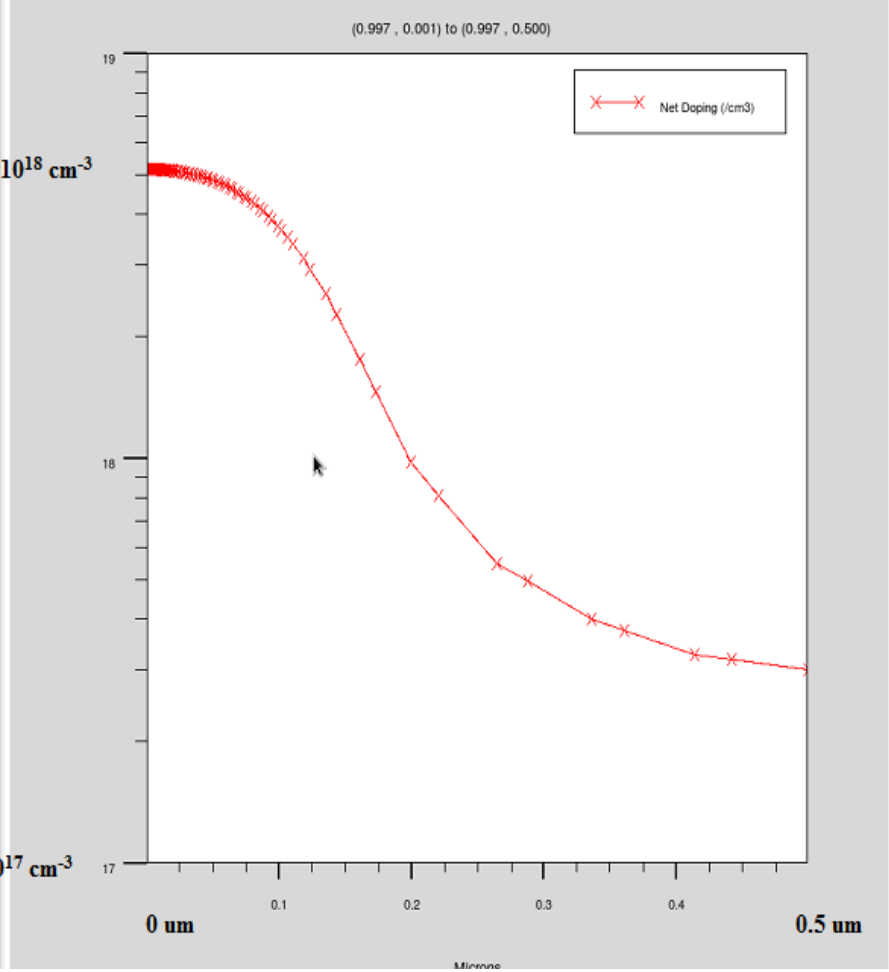
250Å thick oxide is grown and retrograde well profile is obtained during this oxidation step.

Concentration of impurities at the surface is comparatively greater than the concentration of impurities at the bulk (**0.2 µm** deep).

The mask length of the polysilicon (**150 *nm***) is reduced to ~**125 *nm*** after Poly-Reoxidation.

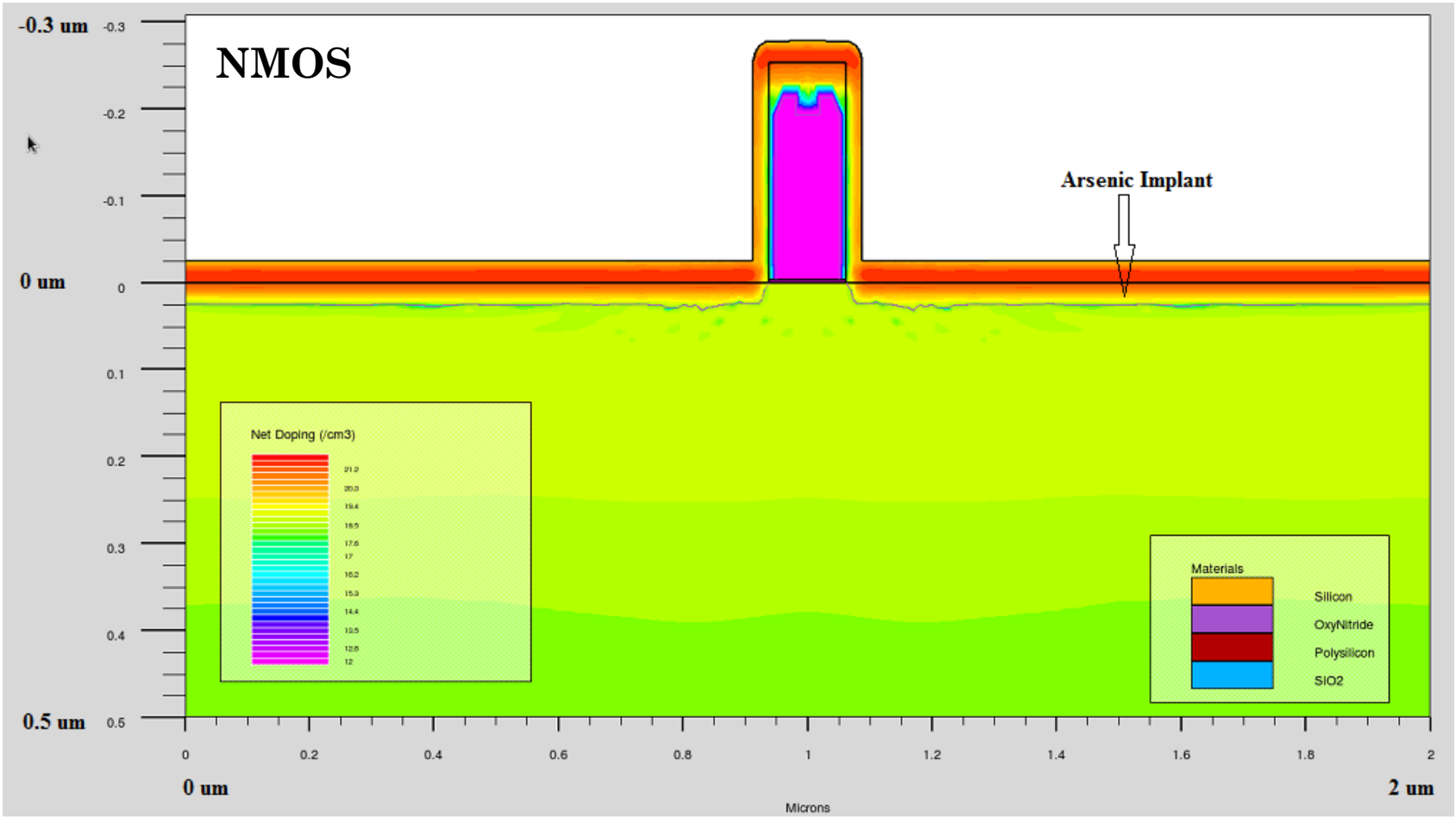
Poly Re-oxidation and Retrograde Well Profile





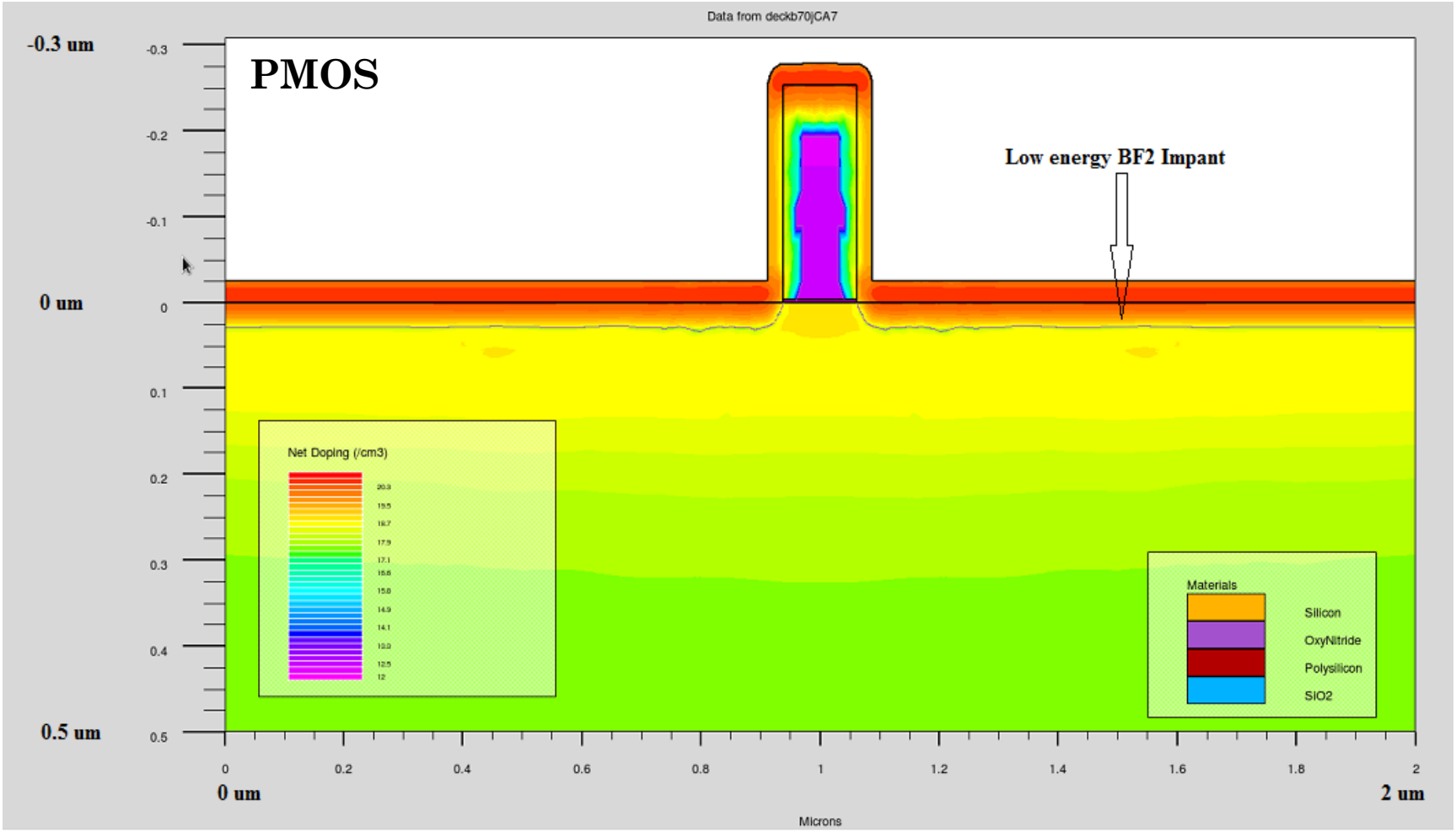
Concentration at the surface = 5e18cm^{-3}
Concentration at the bulk = ~3e17 cm^{-3}

Source/Drain Extensions Implant - nmos



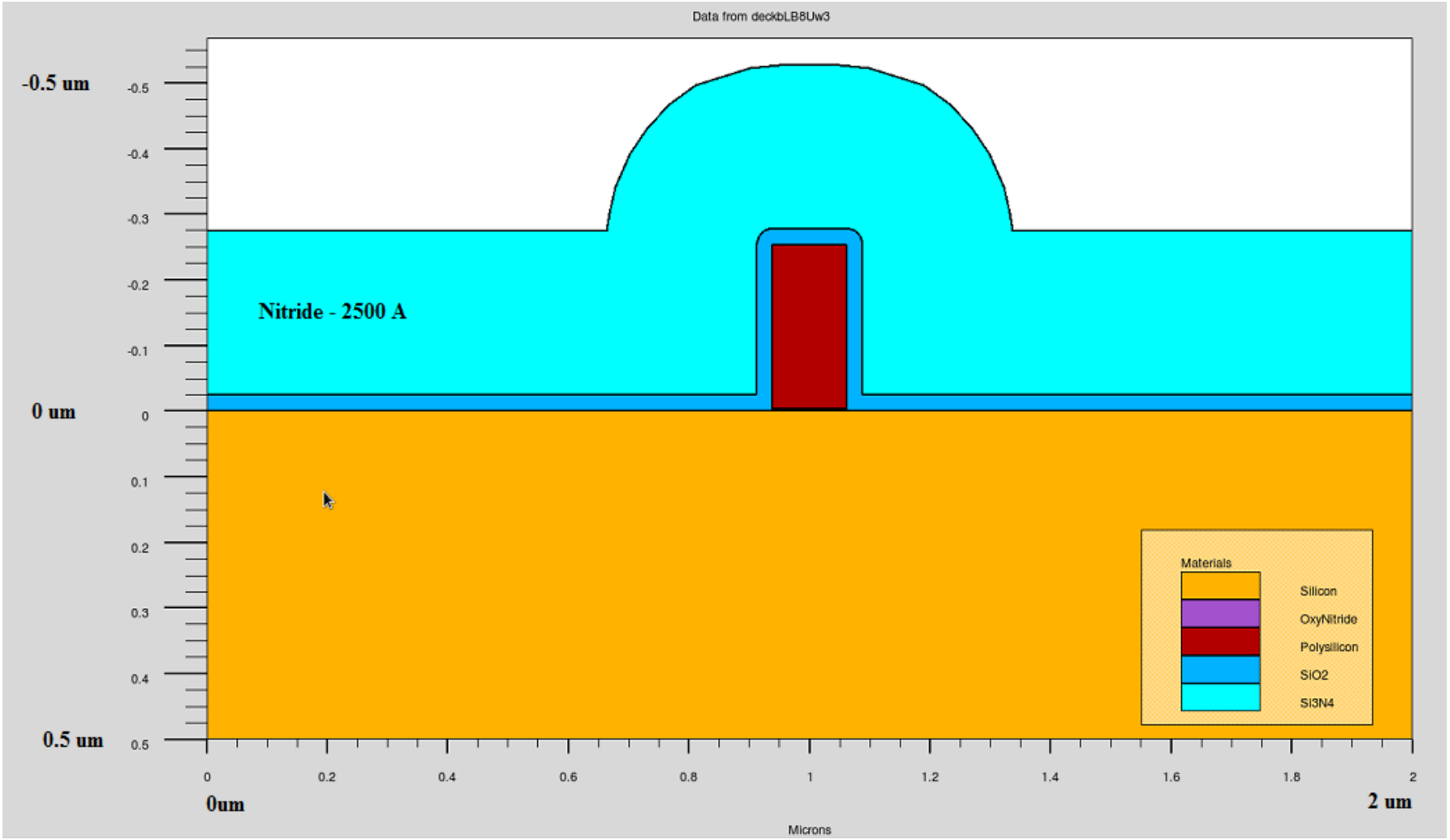
Impurity : **Arsenic**
Dose : 5e15 cm^{-2}
Energy: 20 *KeV*
Depth: 25 *nm* (**0.025 *μm***)

SOURCE/DRAIN EXTENSIONS IMPLANT - PMOS



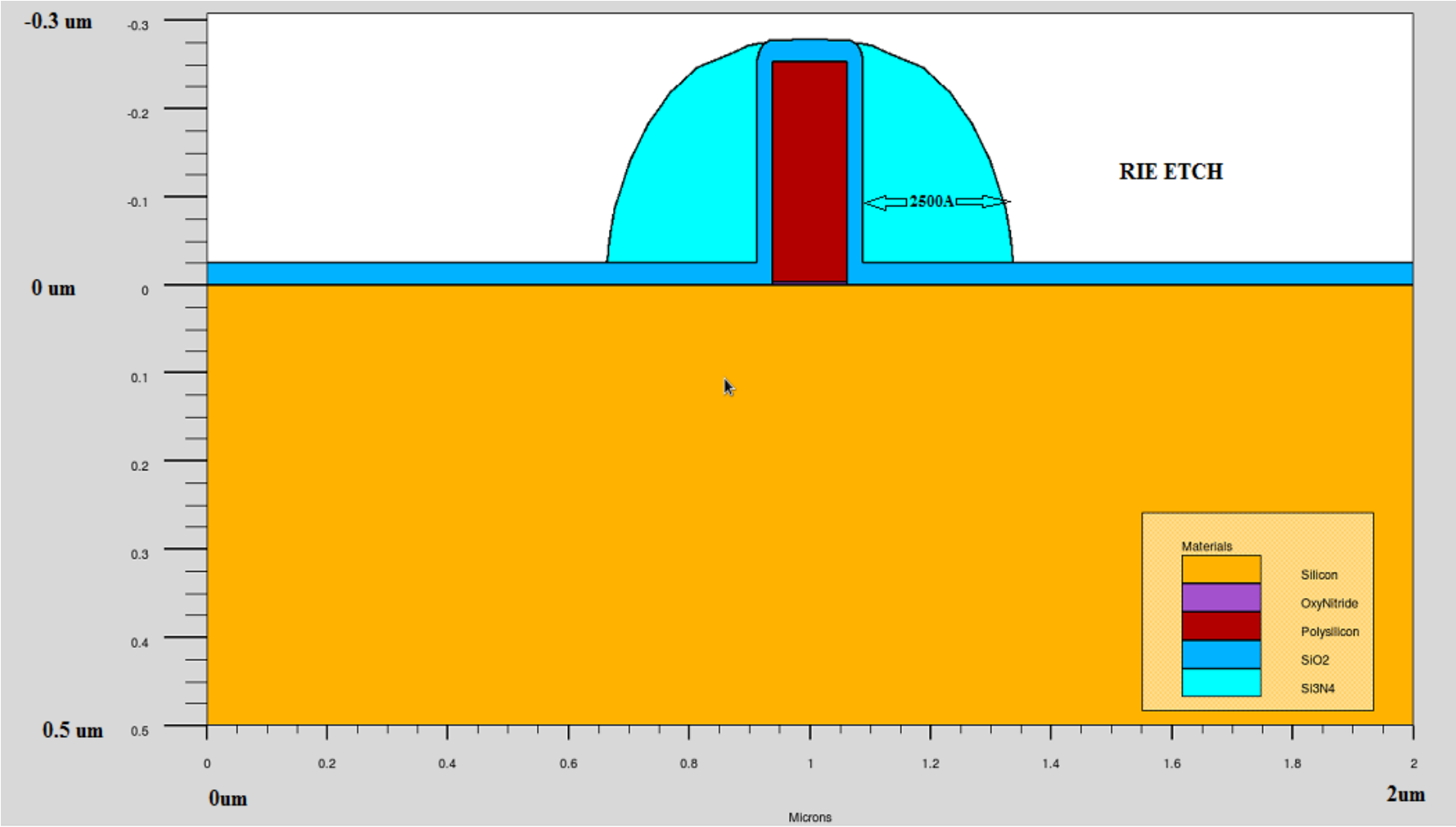
Impurity : **BF2**
Dose : 9e14 cm^{-2}
Energy: 20 *KeV*
Junction depth: 26 *nm* (**0.026 *μm***)

NITRIDE (SIDEWALL SPACER) DEPOSITION



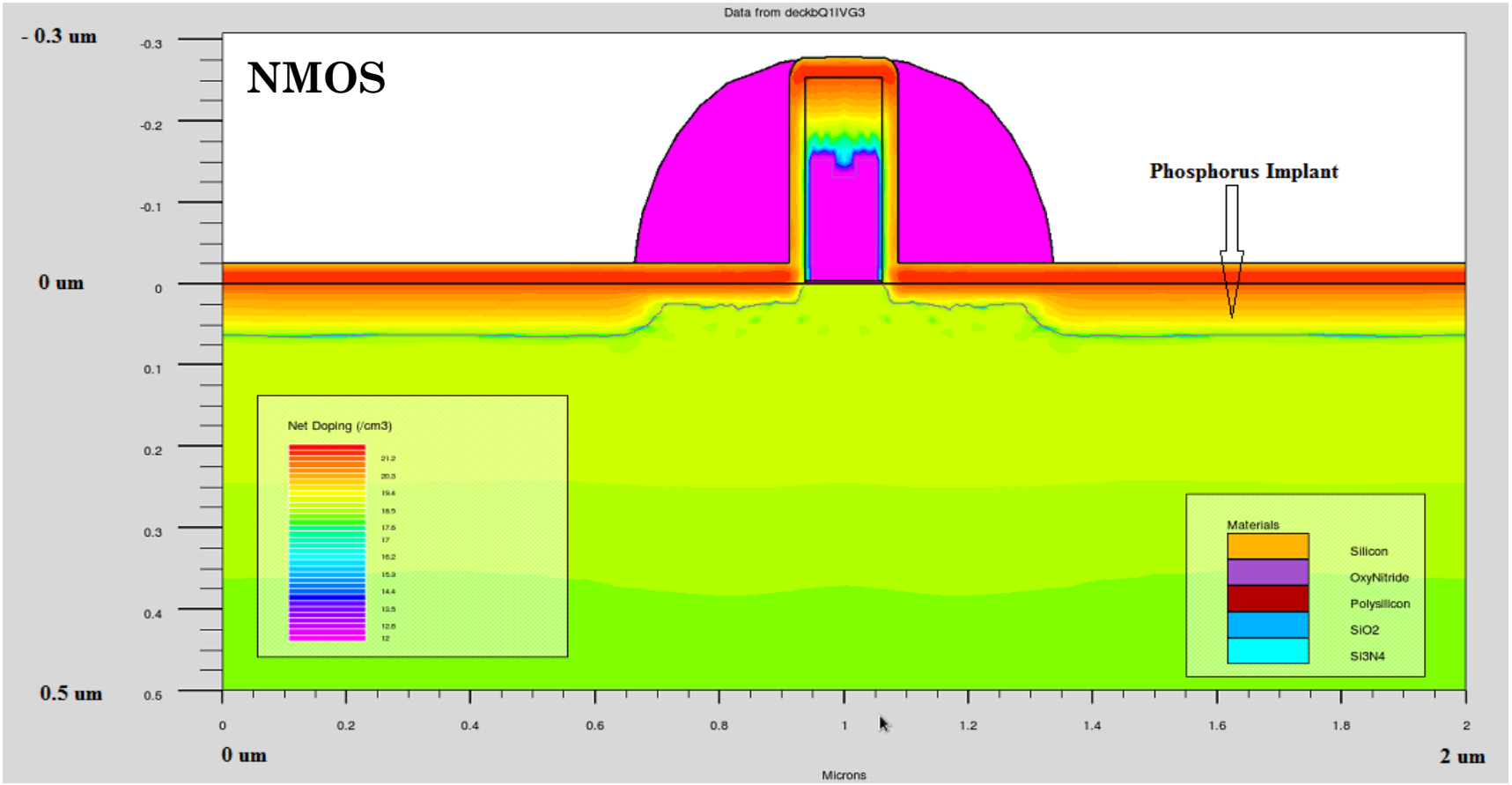
A layer of nitride is deposited for side wall spacers. The thickness of the nitride deposited is **2500*Å***.

SIDEWALL SPACER ETCH



Etch **2500Å** thick nitride. And the width of the nitride is defined by poly length **~2500Å**.

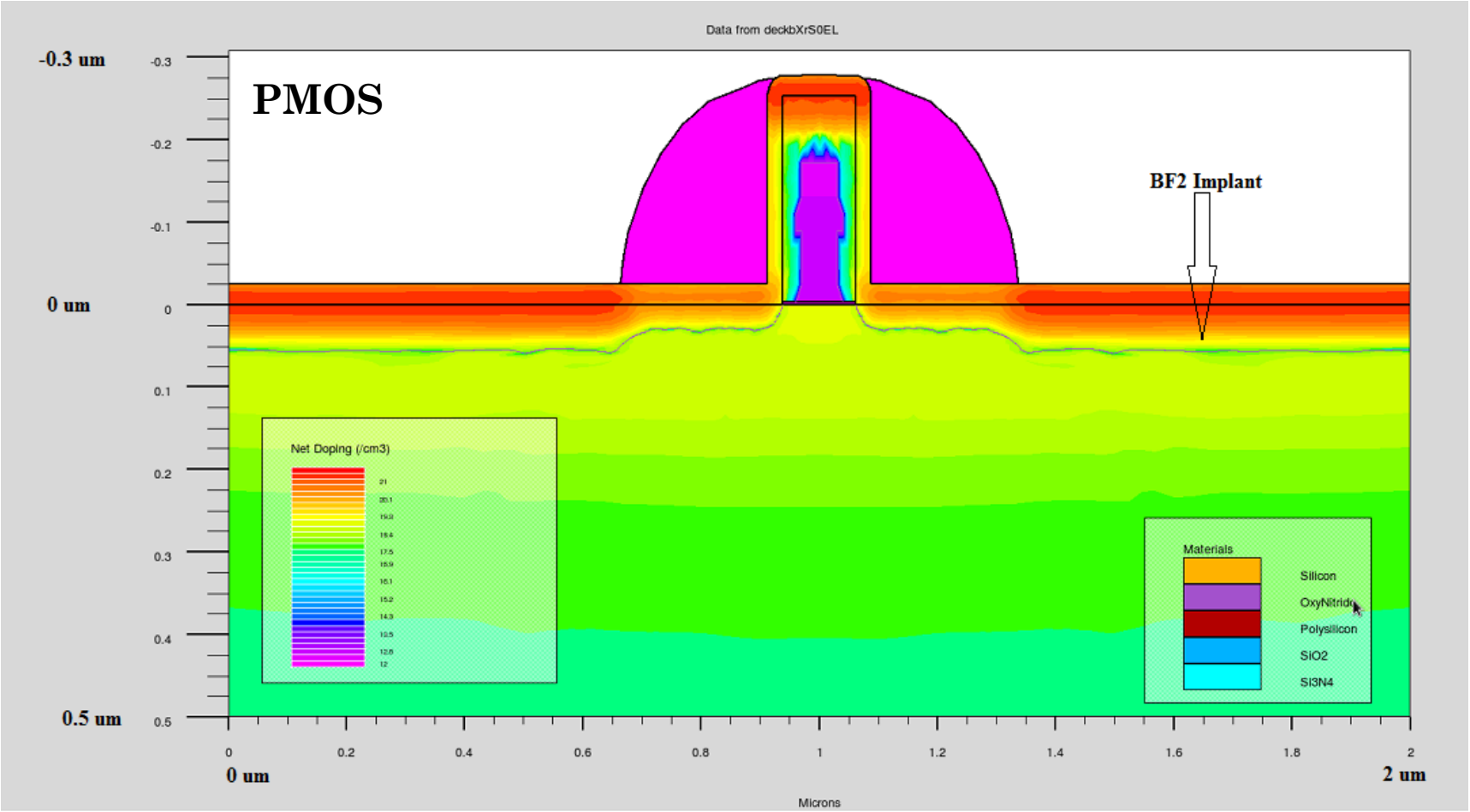
SOURCE/DRAIN IMPLANTS



Impurity: **Phosphorus**
Dose: 1e15 cm^{-2}
Energy: 25 *KeV*
Depth: **60 *nm*** (**0.06 *μm***)

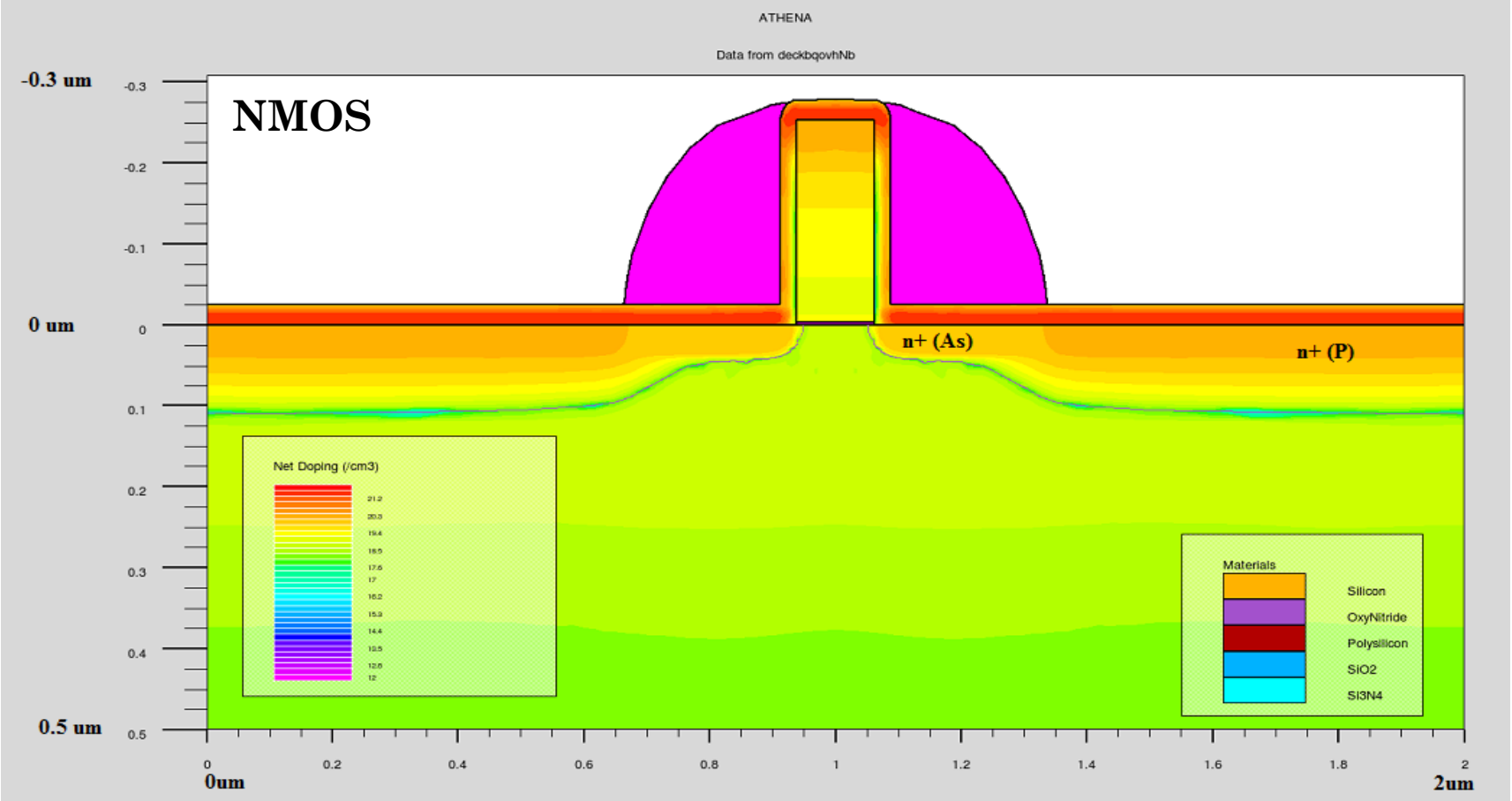
Dose of **S/D regions** with **Phosphorus** as the impurity in **NMOS** is comparatively less than the dose of **S/D extensions** with **Arsenic** as impurity because the **diffusivity** of Phosphorus **is more** in silicon compared to Arsenic.

SOURCE/DRAIN IMPLANTS



Impurity: **BF2**
Dose: 5e15 cm^{-2}
Energy: 27 *KeV*
Depth: **50 *nm*** (**0.05 *μm***)

SOURCE/DRAIN SPIKE ANNEALING



Spike Annealing is preferred over conventional furnace annealing to reduce the effects of transient enhanced diffusion (TED).

Effects of TED is significant at low temperatures (700˚C to 950˚C).

Anneal Recipe:

Ramp up – 700˚C to 1050˚C – 3 seconds

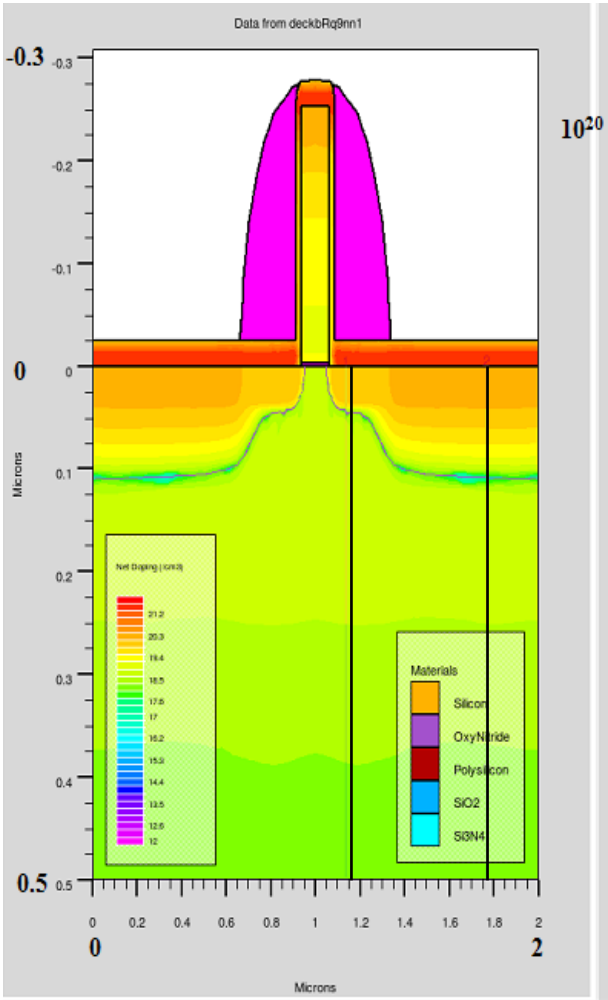
Soak – 1050˚C – 7 seconds (**Nitrogen ambient**)

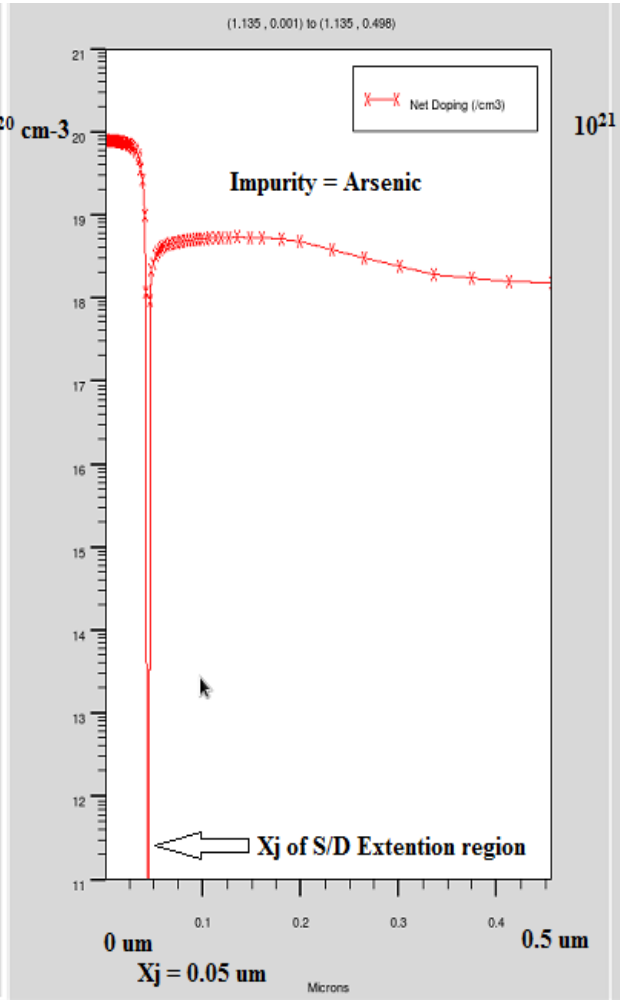
Ramp down - 1050˚C to 700˚C – 6 seconds

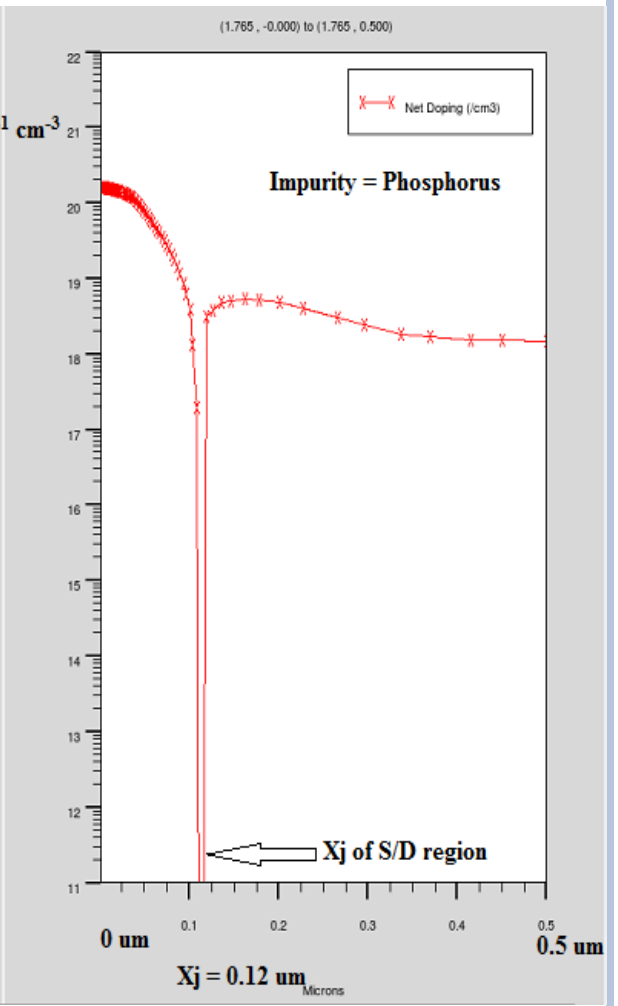
Junction depth after anneal:

NMOS (S/D regions): **105 *nm* (0.105 *μm*)**

JUNCTION PROFILE - NMOS





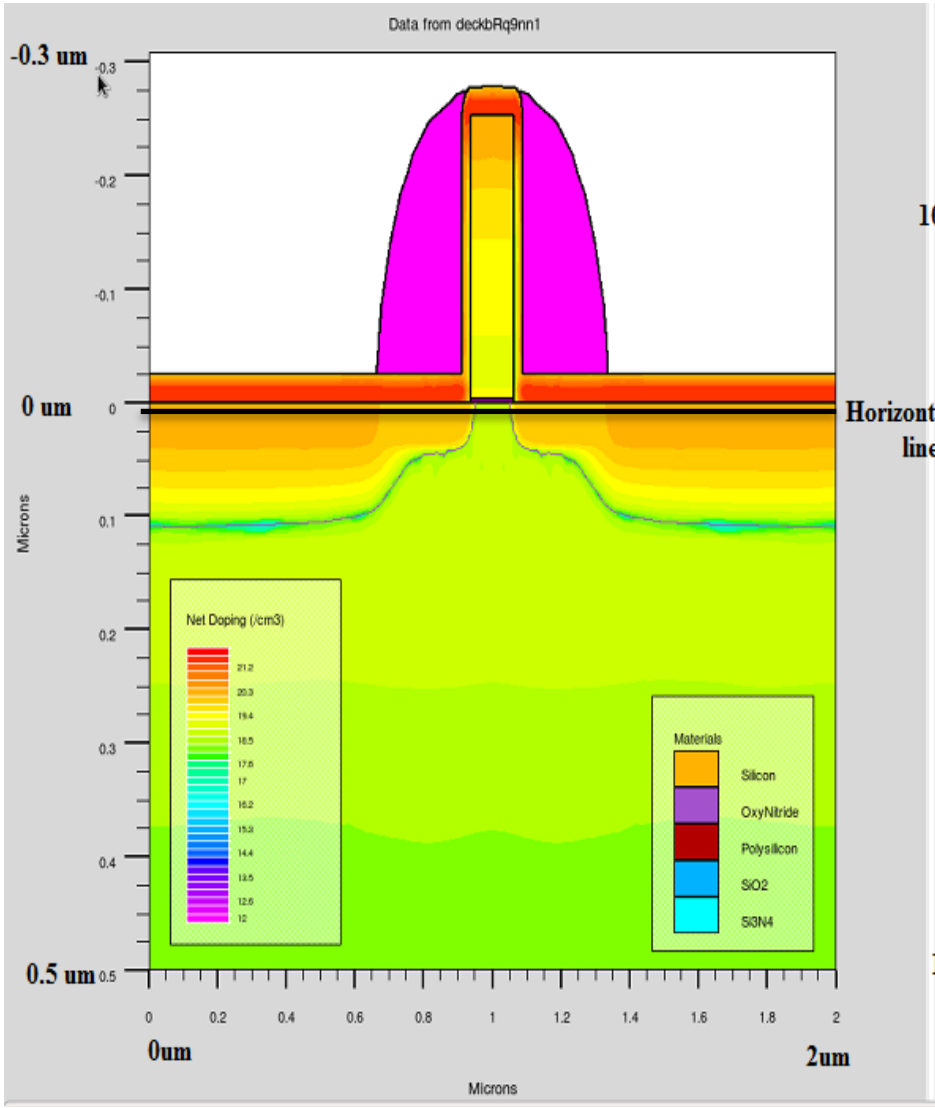


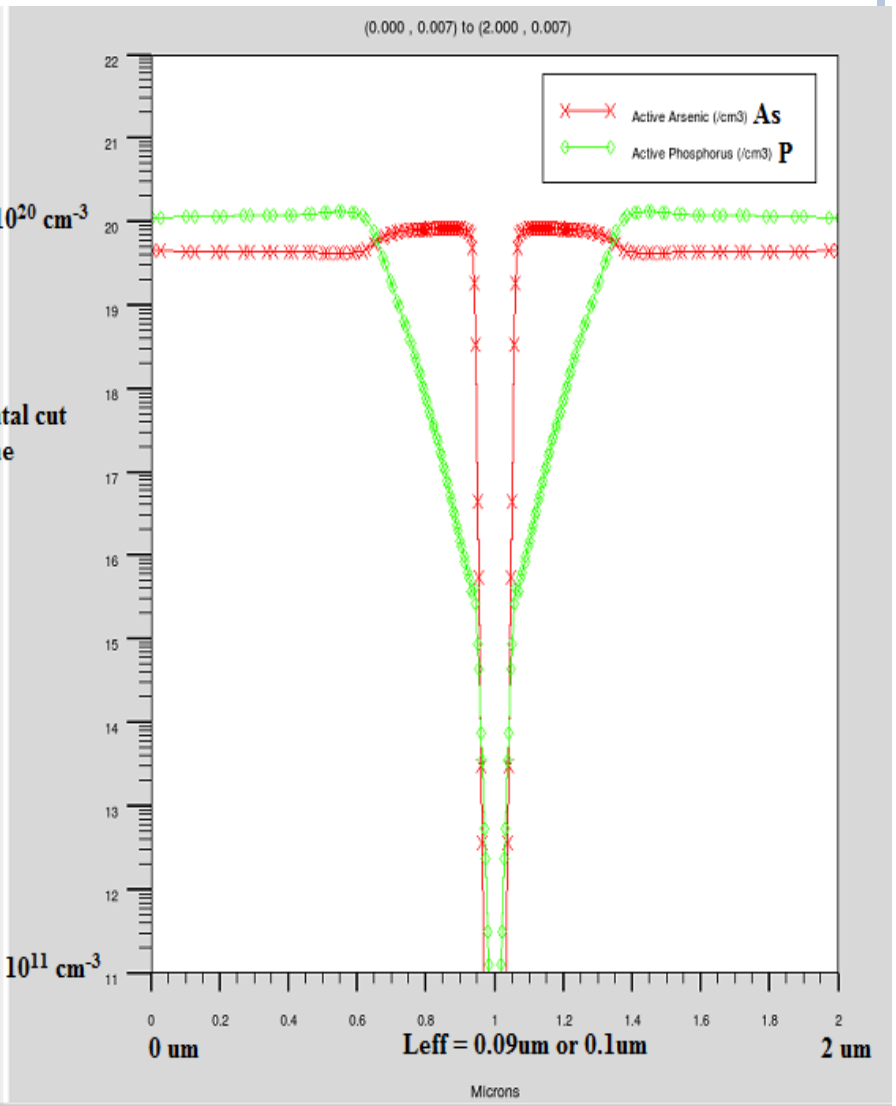
Vertical cut line

Junction depth (Source/Drain Extension) = 0.05 μm

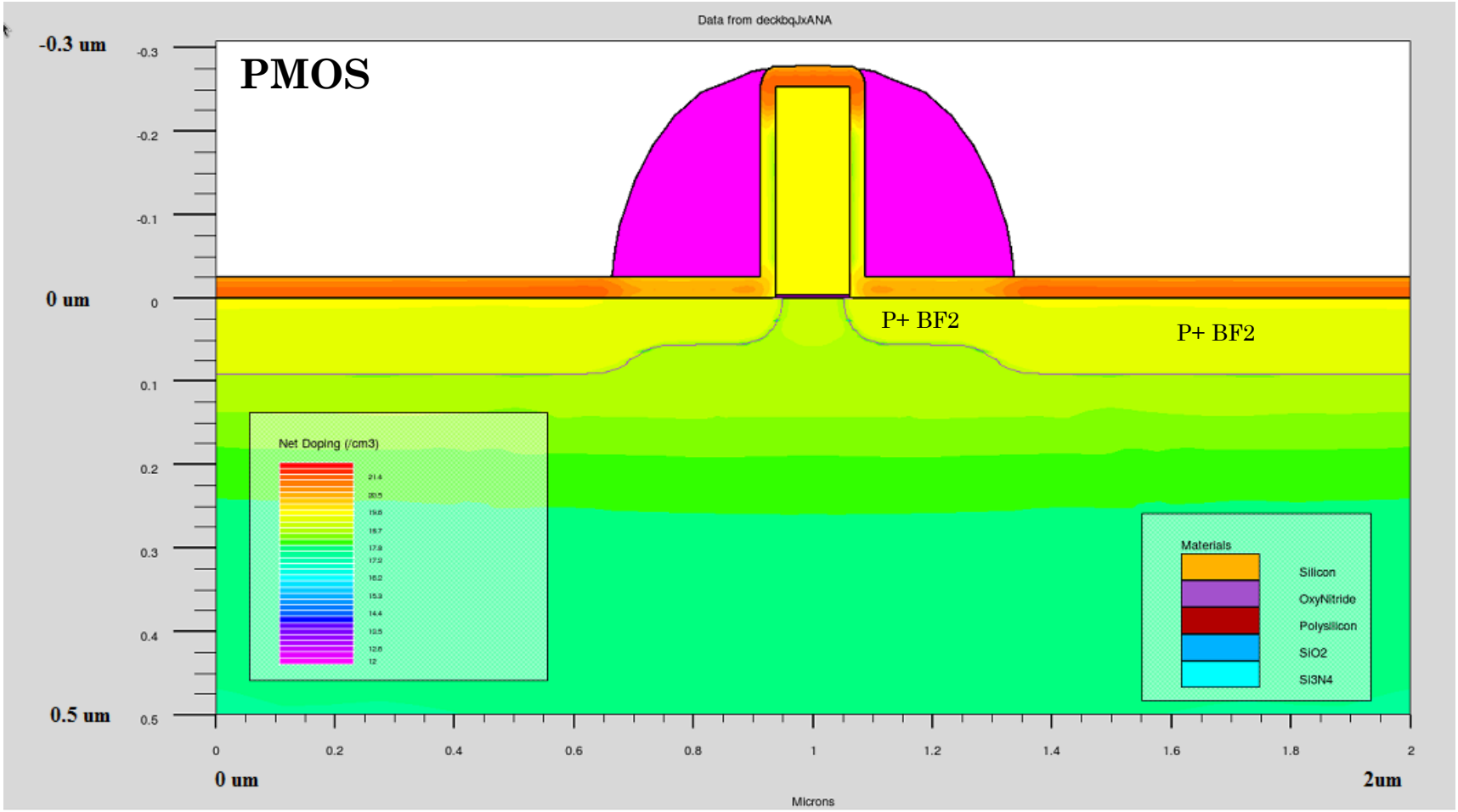
Junction depth (Source/Drain) = 0.12 μm

HORIZONTAL CUT-LINE - NMOS





SOURCE/DRAIN SPIKE ANNEALING



Anneal Recipe:

Ramp up – 700˚C to 1050˚C – 3 seconds

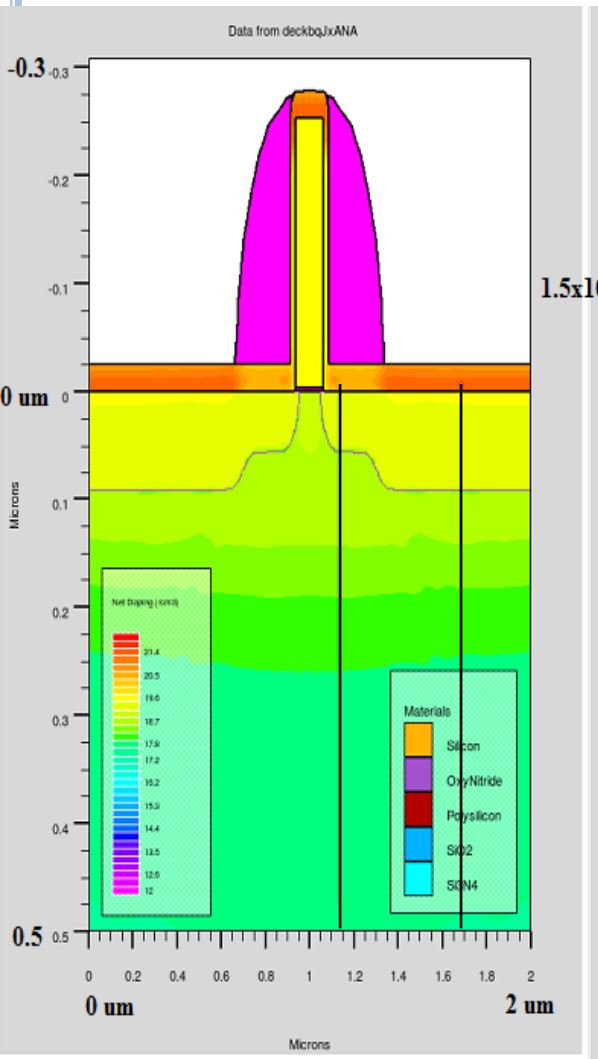
Soak – 1050˚C – 5 seconds (**Nitrogen ambient**)

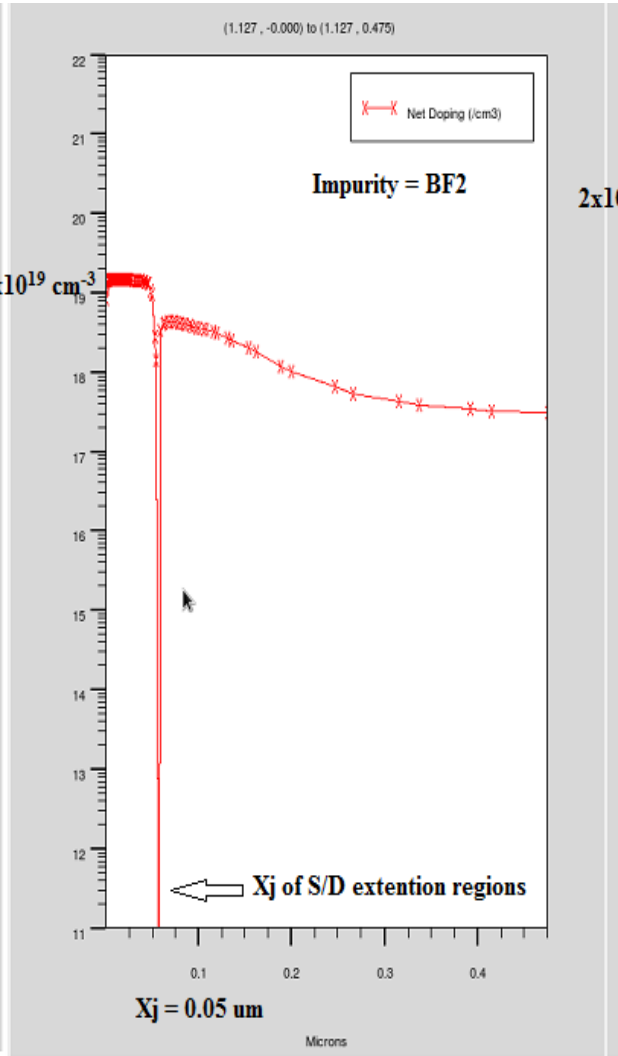
Ramp down - 1050˚C to 700˚C – 6 seconds

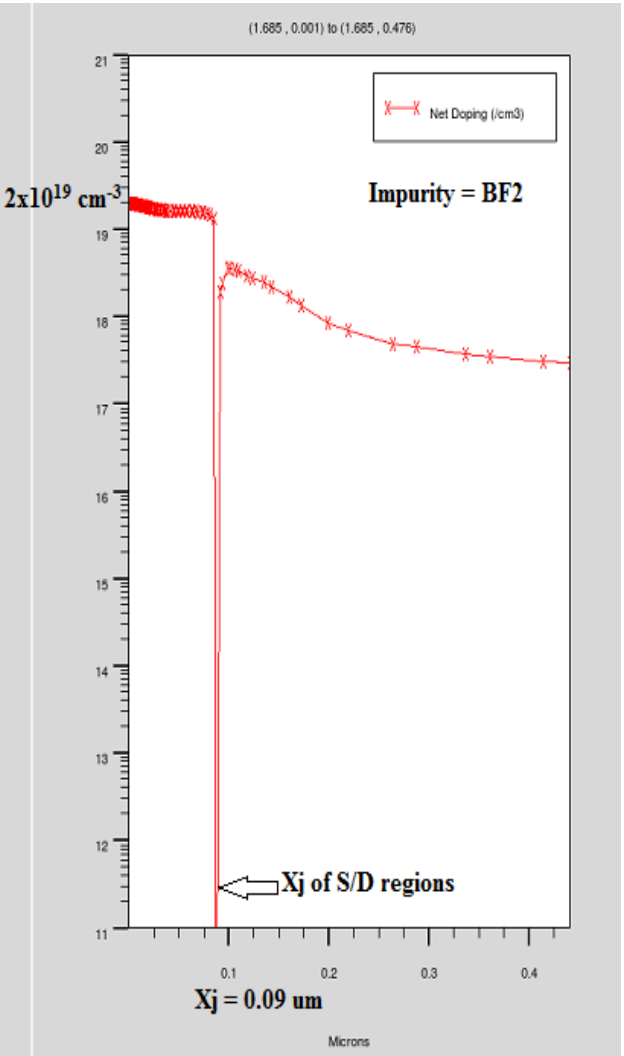
Junction depth after anneal:

PMOS (S/D regions): ~**100 *nm* (~0.1 *μm*)**

JUNCTION PROFILE - PMOS





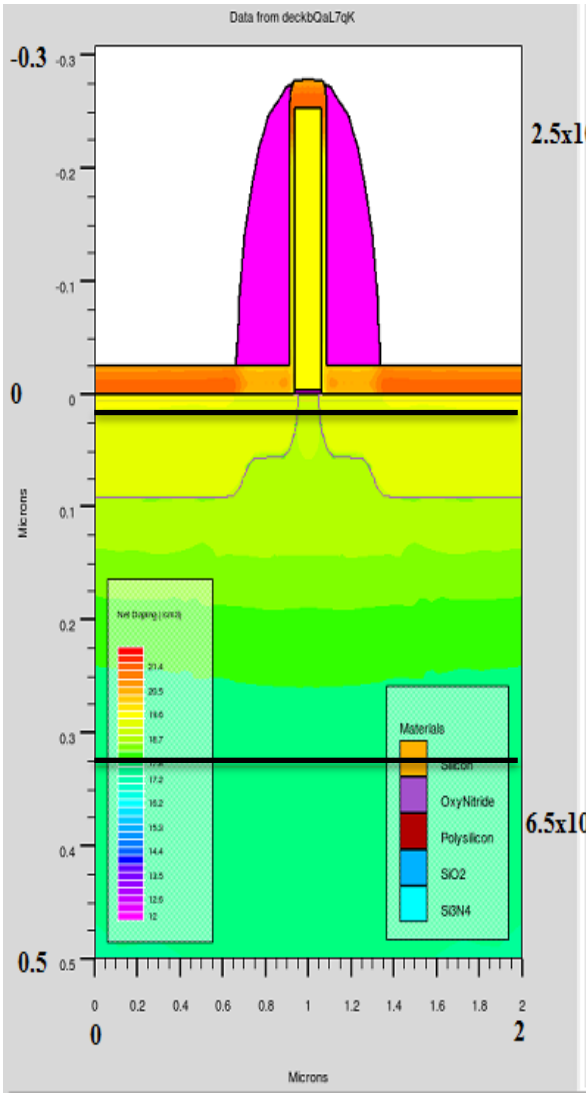


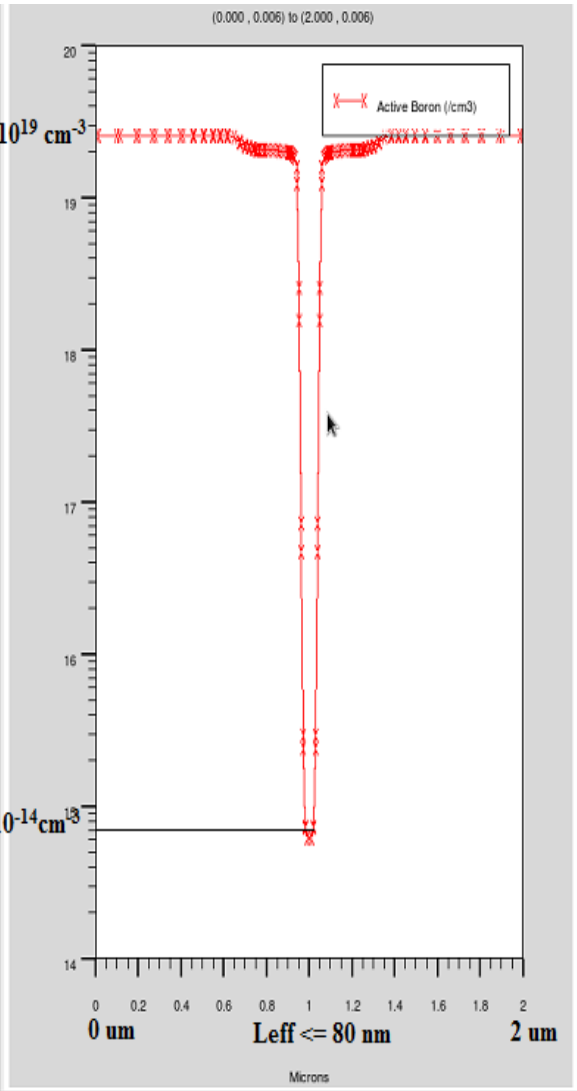
Vertical cut line

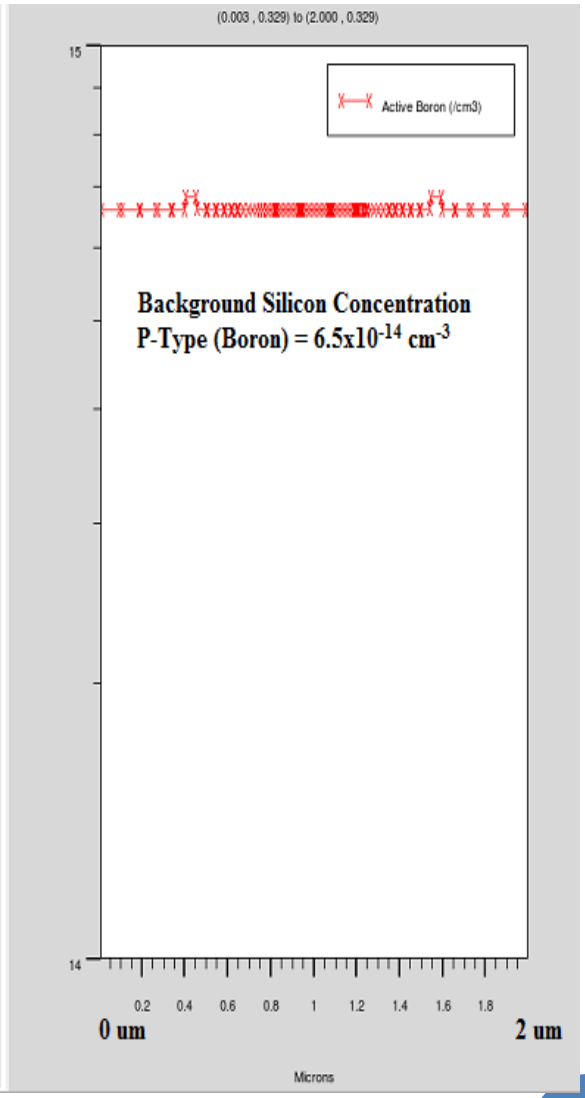
Junction depth (Source/Drain Extension) = 0.05 μm

Junction depth (Source/Drain) = 0.09 μm

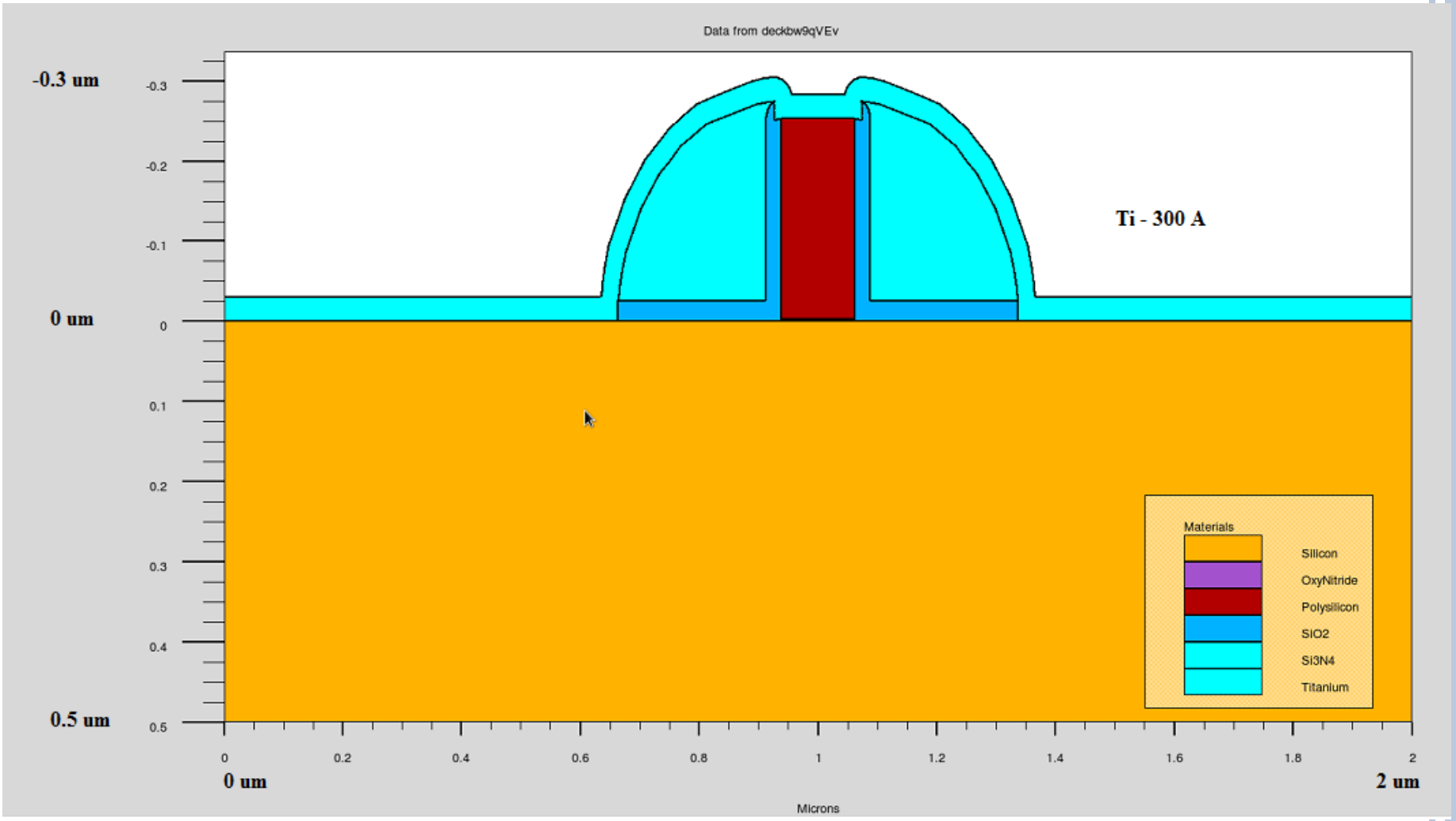
HORIZONTAL CUT-LINE - PMOS







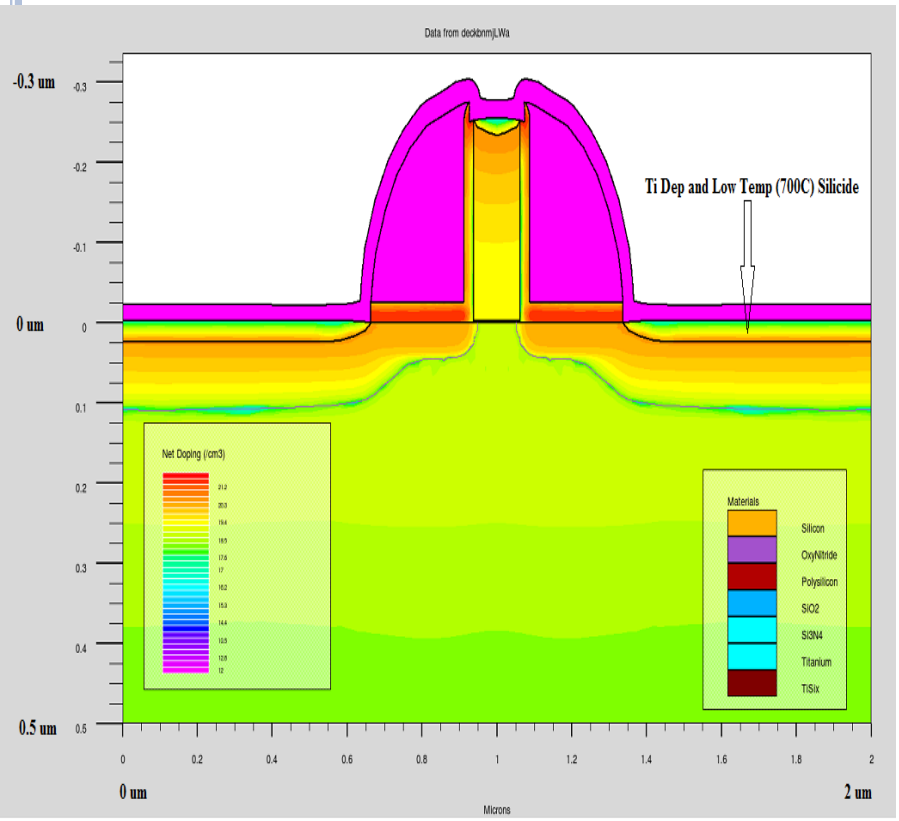
Titanium Deposition



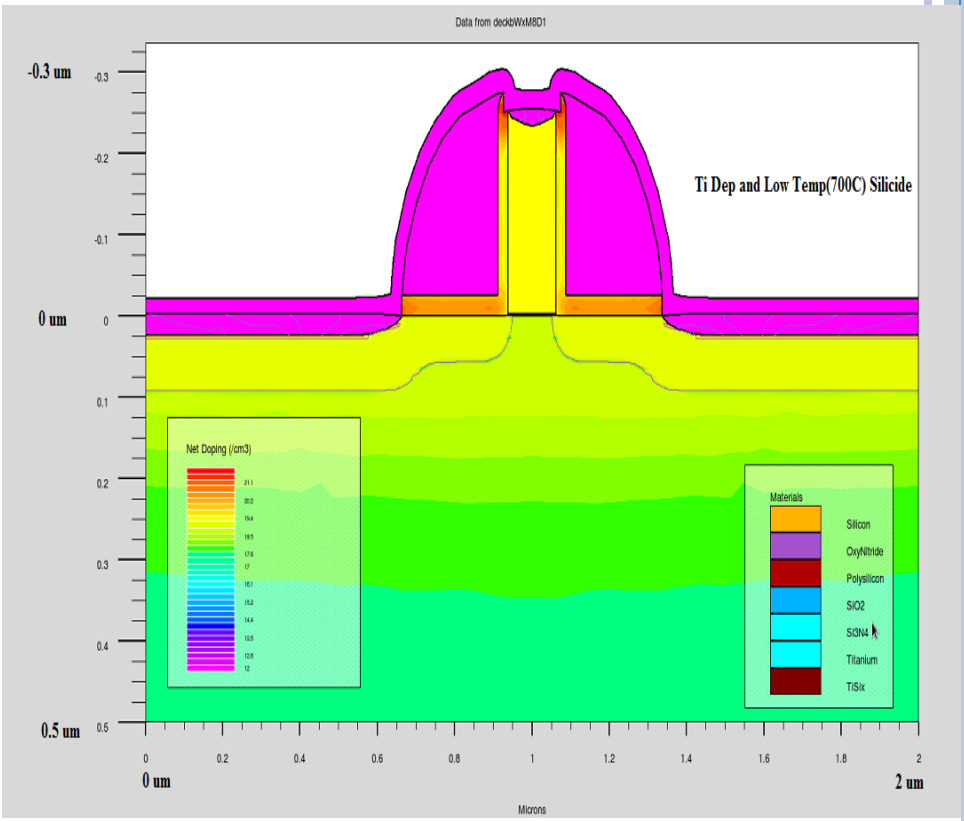
Etch oxide and sputter **300Å** thick Titanium to form Silicide.

SILICIDE (TiSi)

NMOS



PMOS



Silicide recipe:

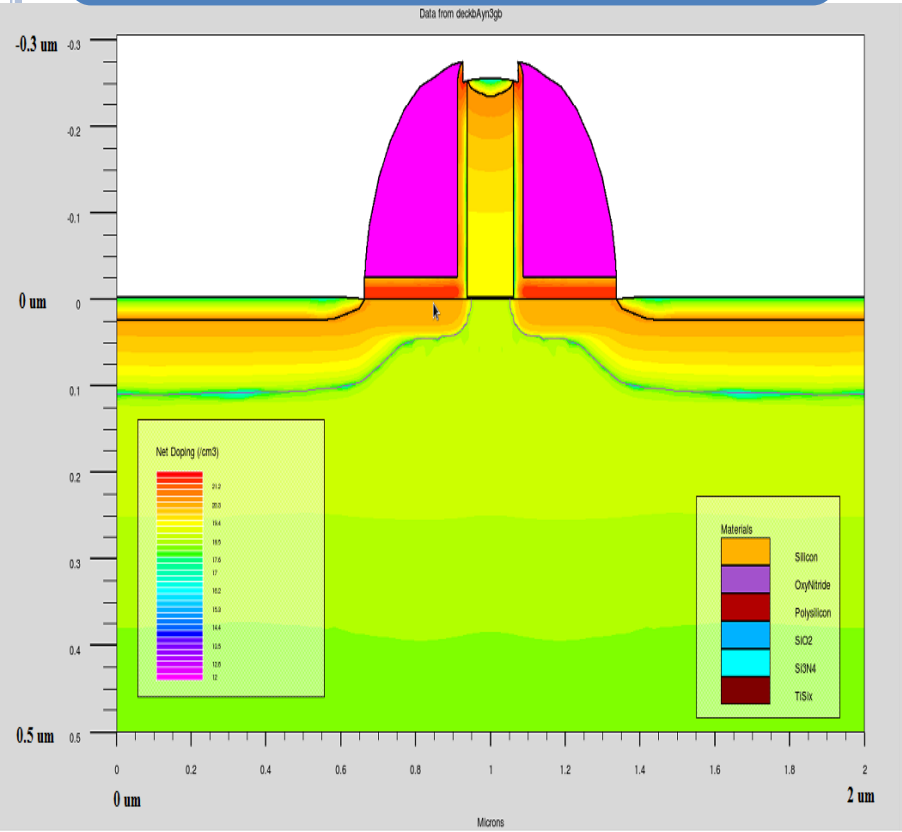
Ramp up – 25˚C to 650˚C – 5 seconds

Soak – 650˚C – 5 seconds (**Nitrogen ambient**)

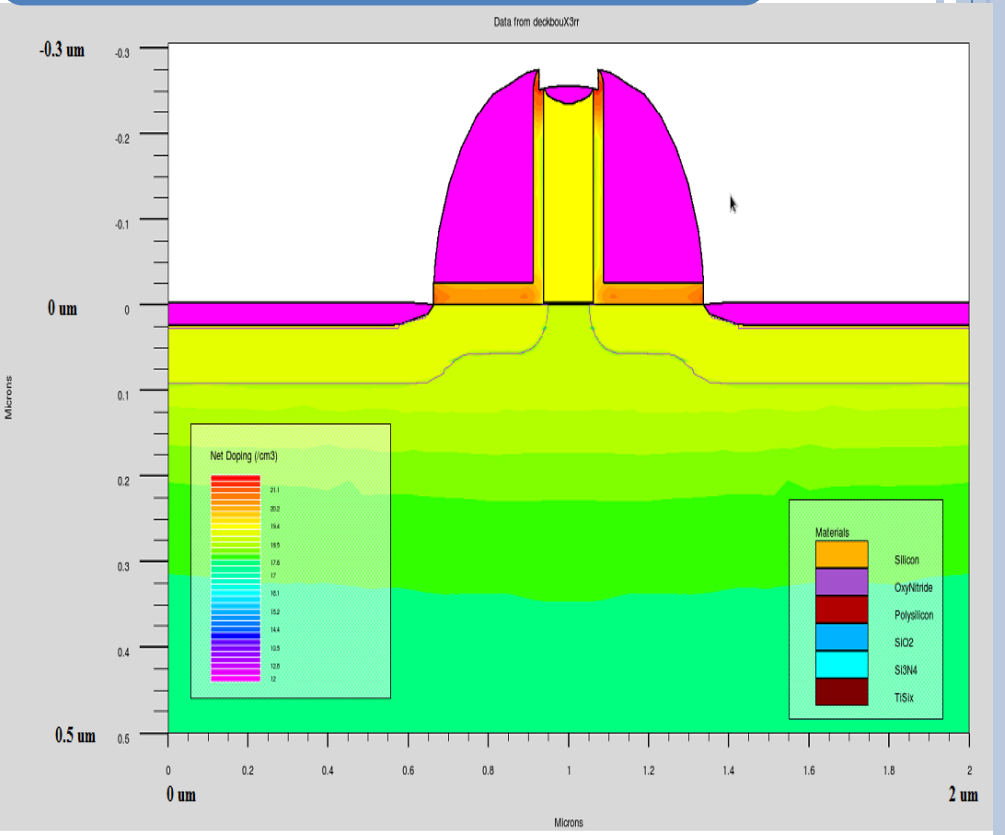
Ramp down – 650˚C to 25˚C – 5 seconds

Etch Titanium and Silicide (TiSi2)

NMOS



PMOS



Silicide recipe:

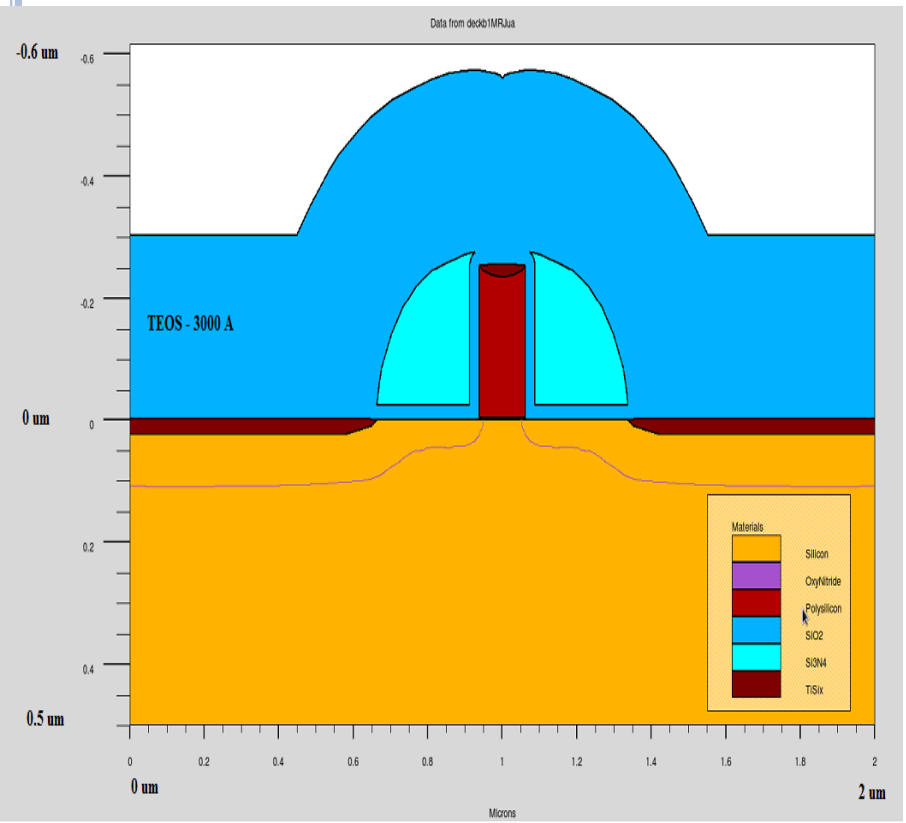
Ramp up – 25˚C to 700˚C – 5 seconds

Soak – 700˚C – 5 seconds (**Nitrogen ambient**)

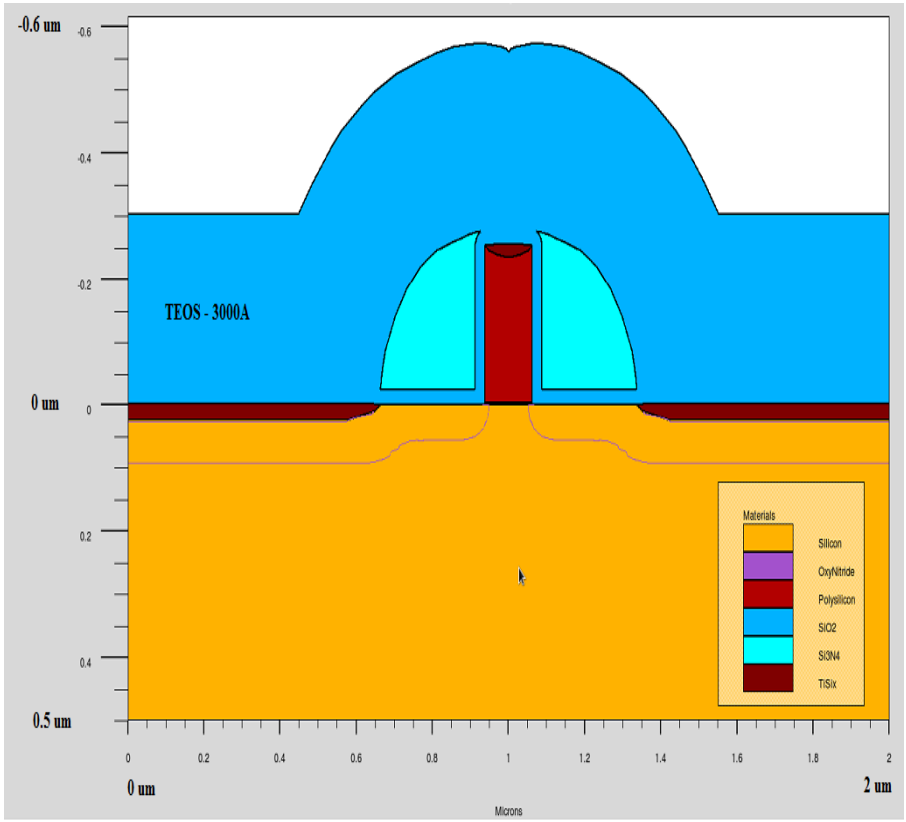
Ramp down – 700˚C to 25˚C – 10 seconds

TEOS Deposition

NMOS



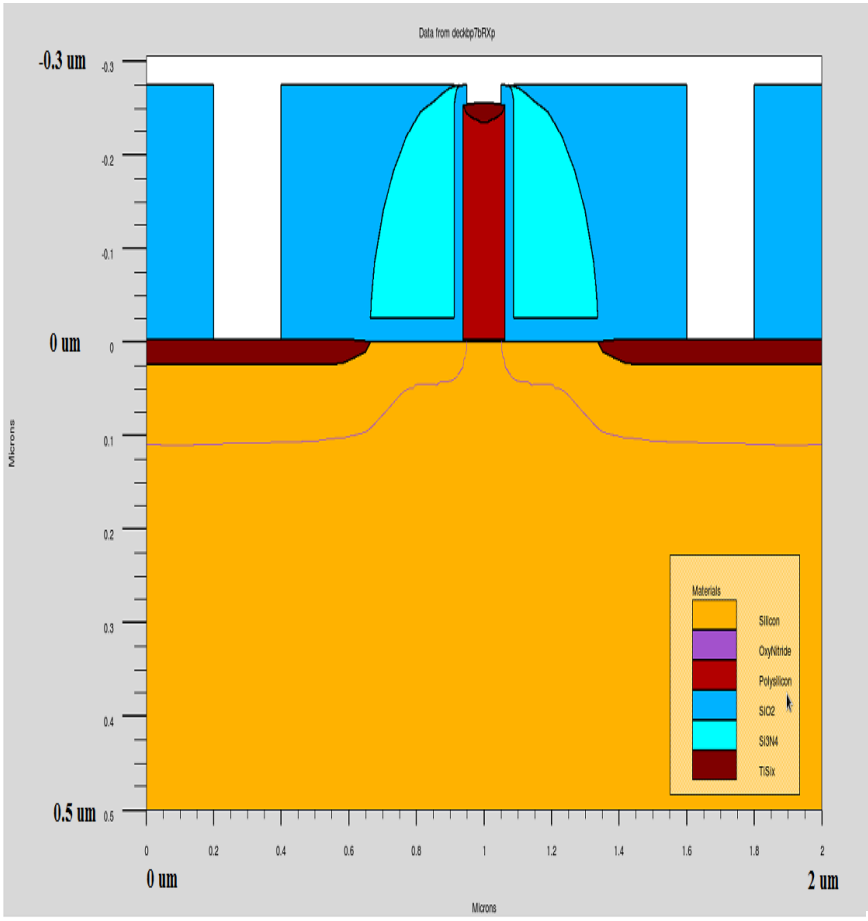
PMOS



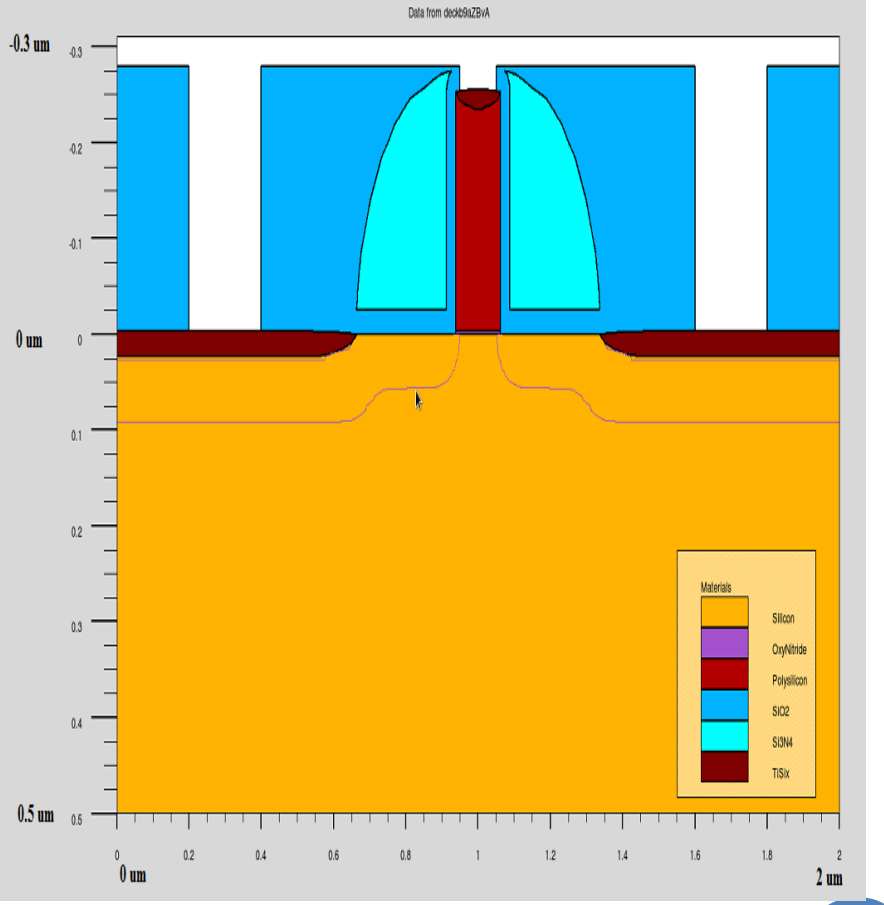
Deposit **3000Å** thick TEOS on P5000.

Contact Cut Etch (RIE)

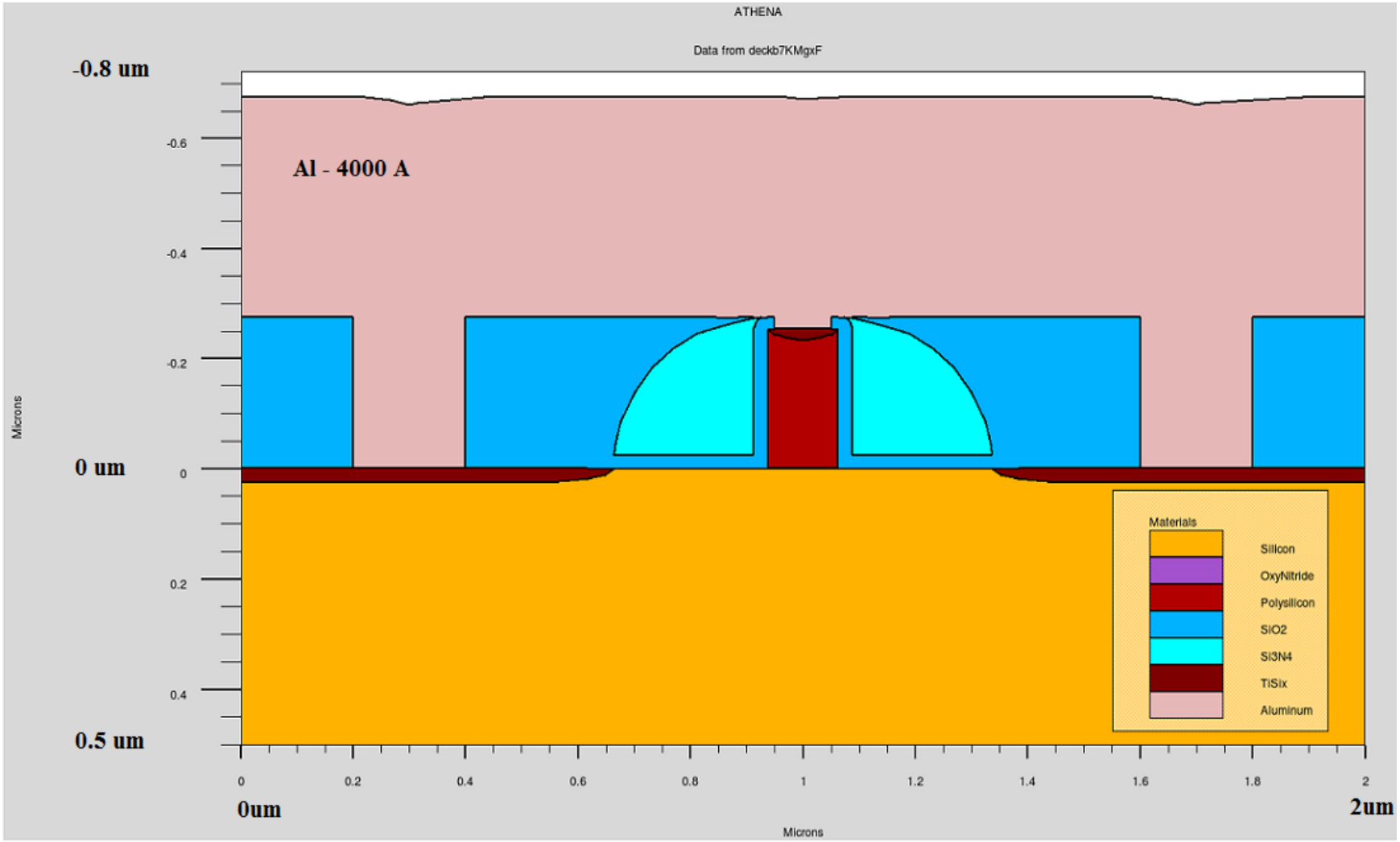
NMOS



PMOS



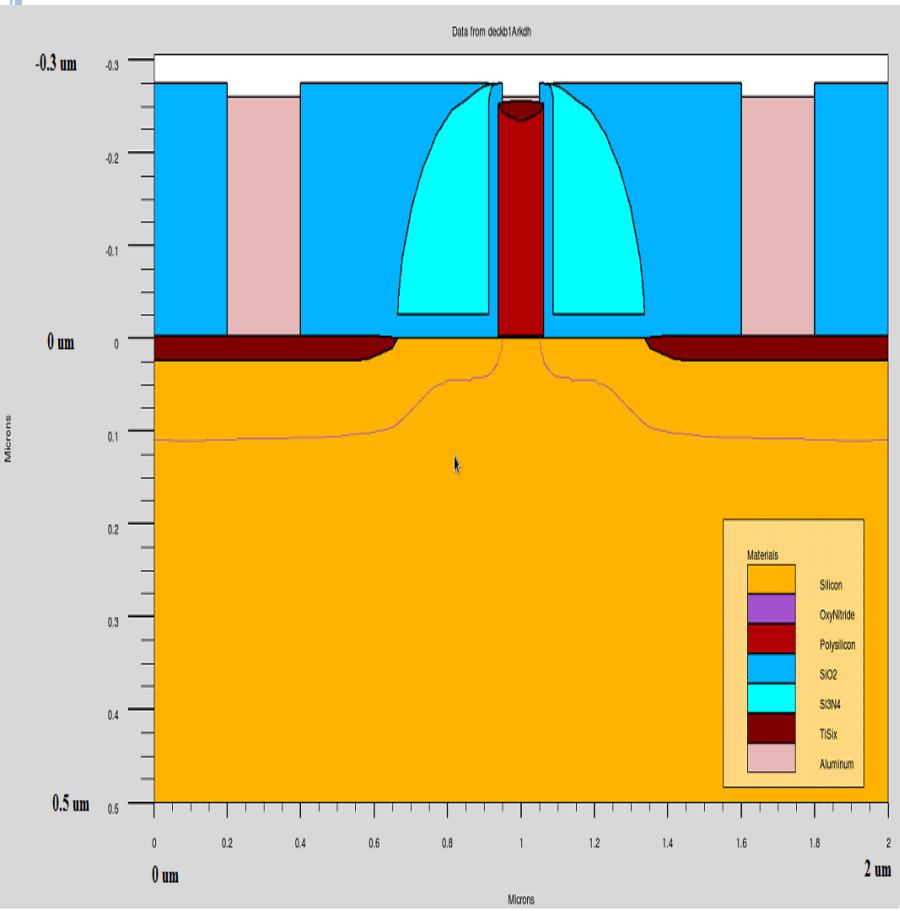
Aluminum Deposition



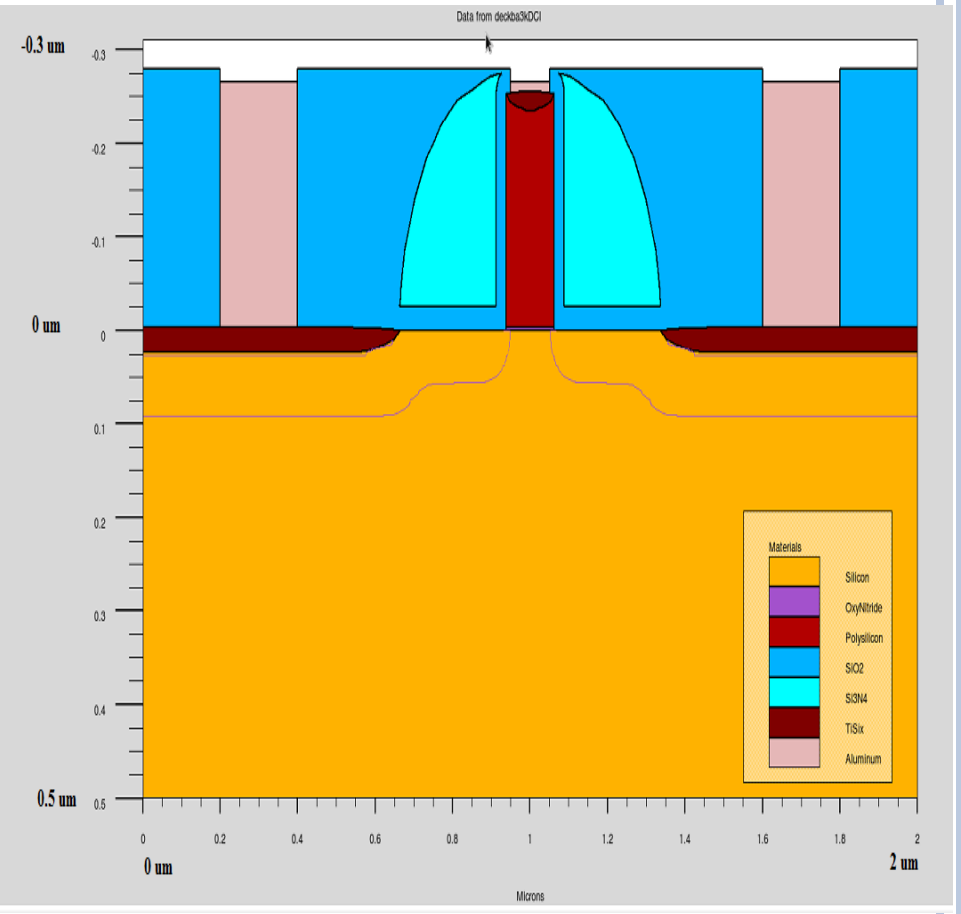
Sputter **4000Å** thick Aluminum.

Aluminum Etch

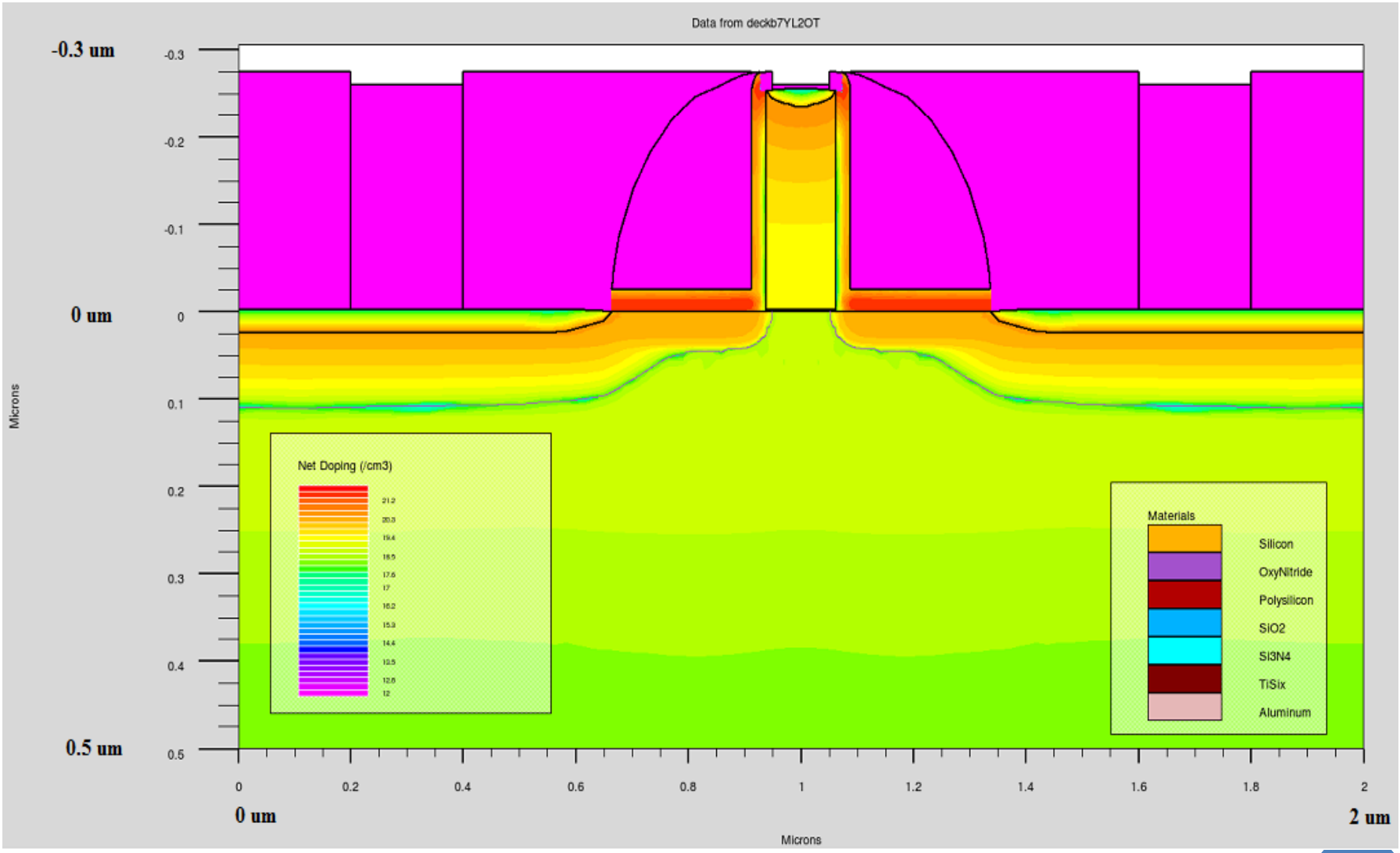
NMOS



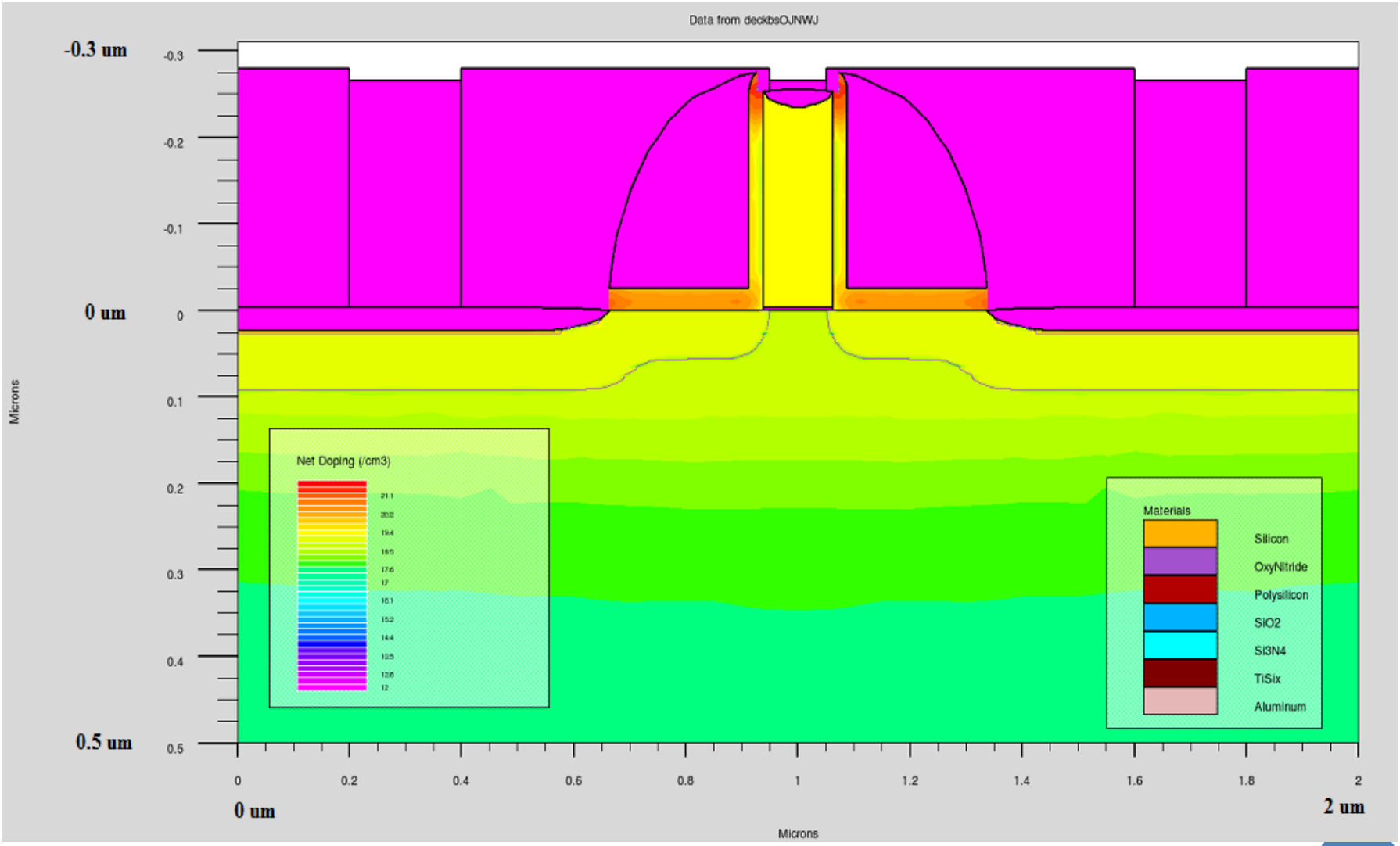
PMOS



Final NMOS Device



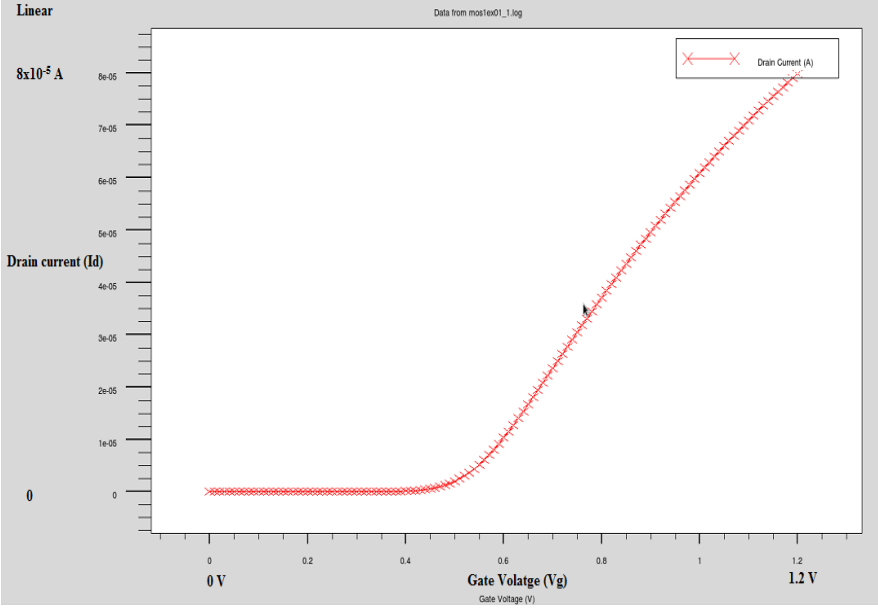
Final PMOS Device

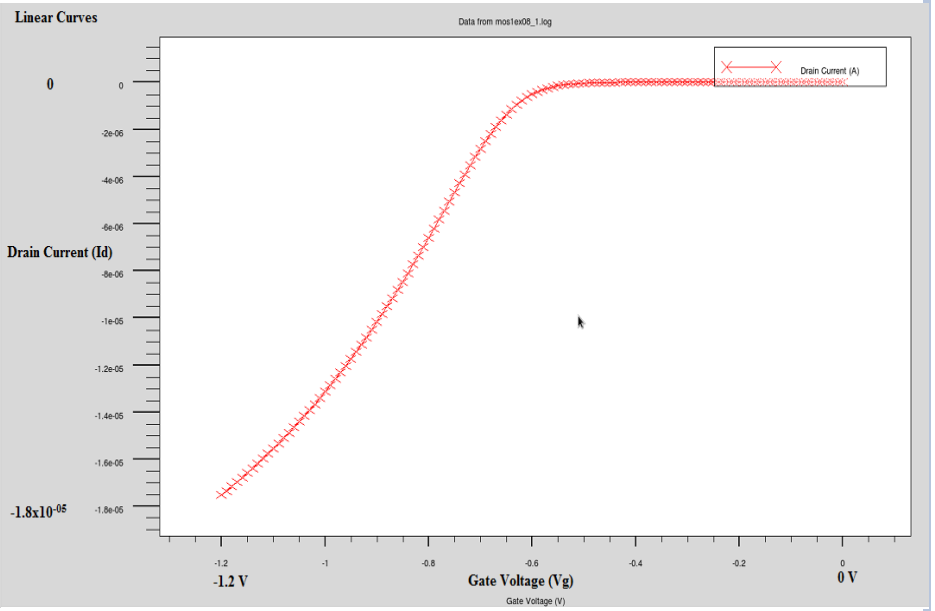


I-V Curves (Threshold Voltage Curves)

NMOS

PMOS





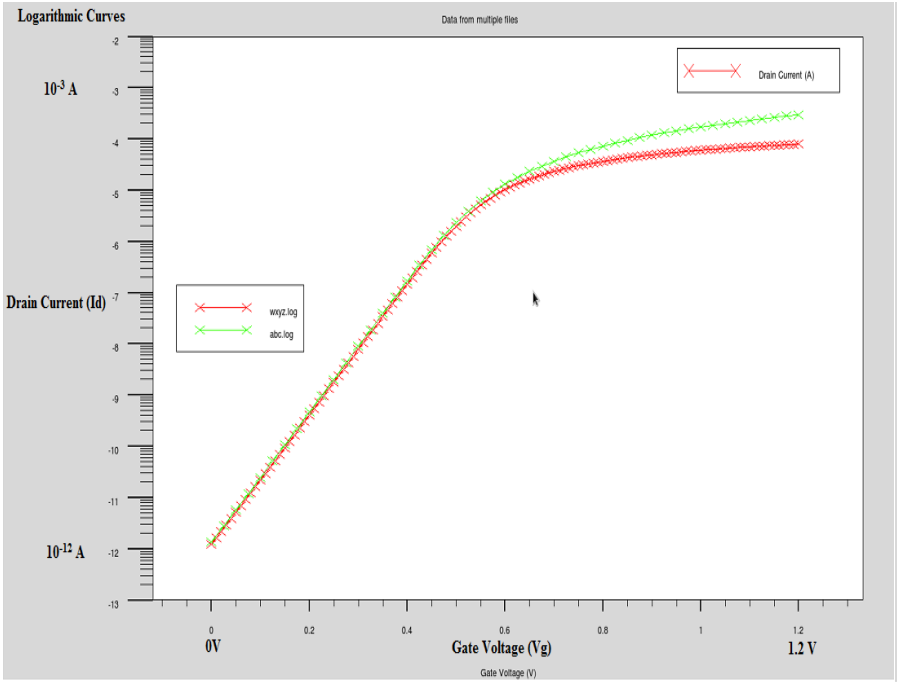
Models cvt srh print
Contact name=gate n.poly (NMOS) / p.poly (PMOS)
Interface qf=3e11

NMOS:
Threshold voltage: 0.4794V

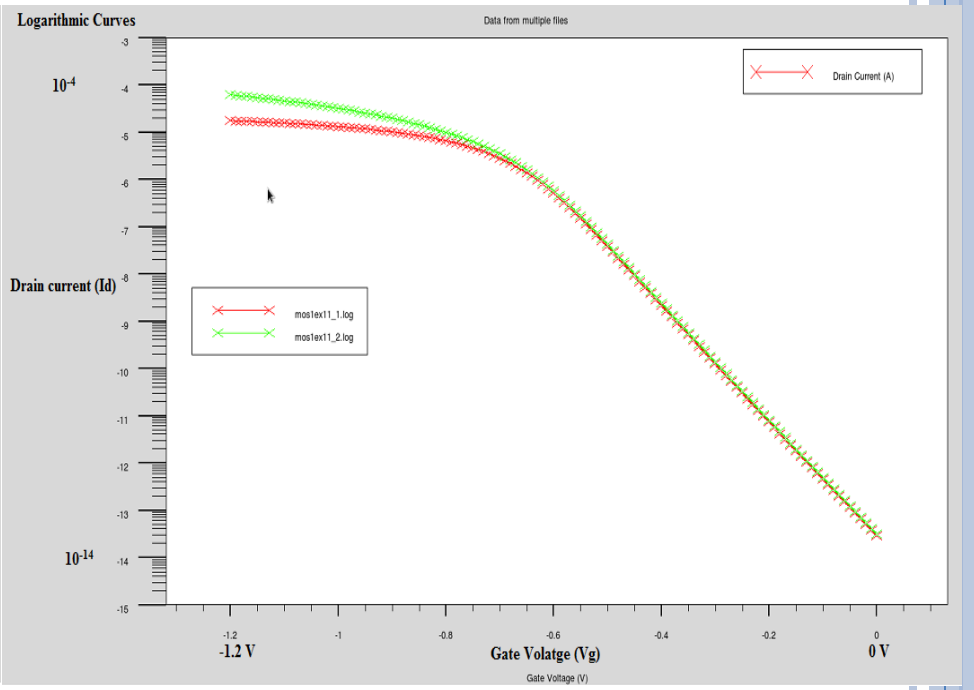
PMOS:
Threshold voltage: -0.58V

Drain Induced Barrier Lowering Curves

NMOS



PMOS



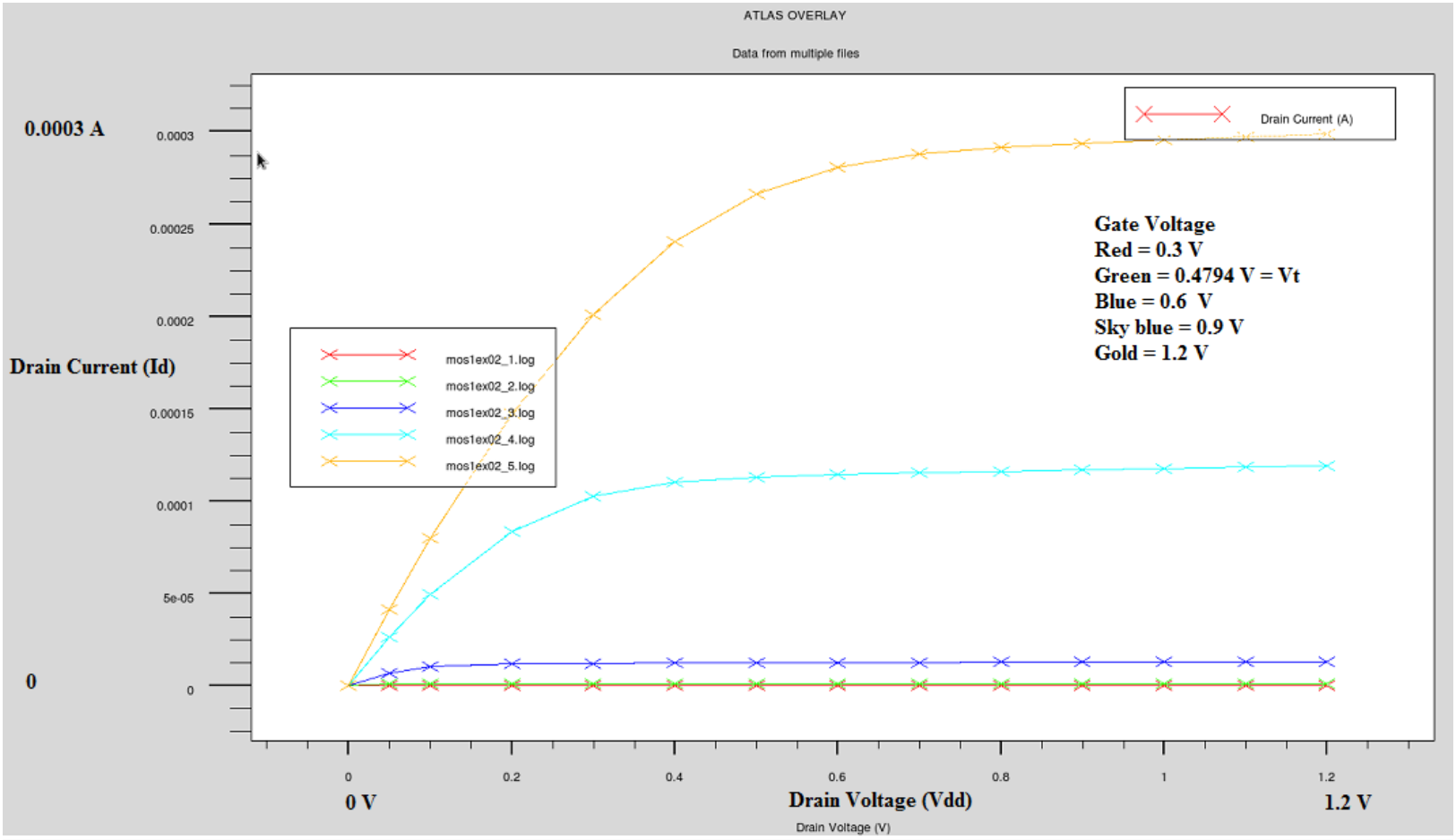
Models cvt srh print
Contact name=gate n.poly (NMOS) / p.poly (PMOS)
Interface qf=3e11

DIBL: 10.3 *mV/V*
Current at 0V ~ 10^{-12} *A/µm*
Sub-threshold Slope: 108 *mV/decade*

DIBL: 11.7 *mV/V*
Current at 0V ~ 10^{-14} *A/µm*
Sub-threshold Slope: 96 *mV/decade*

Family of Curves

NMOS

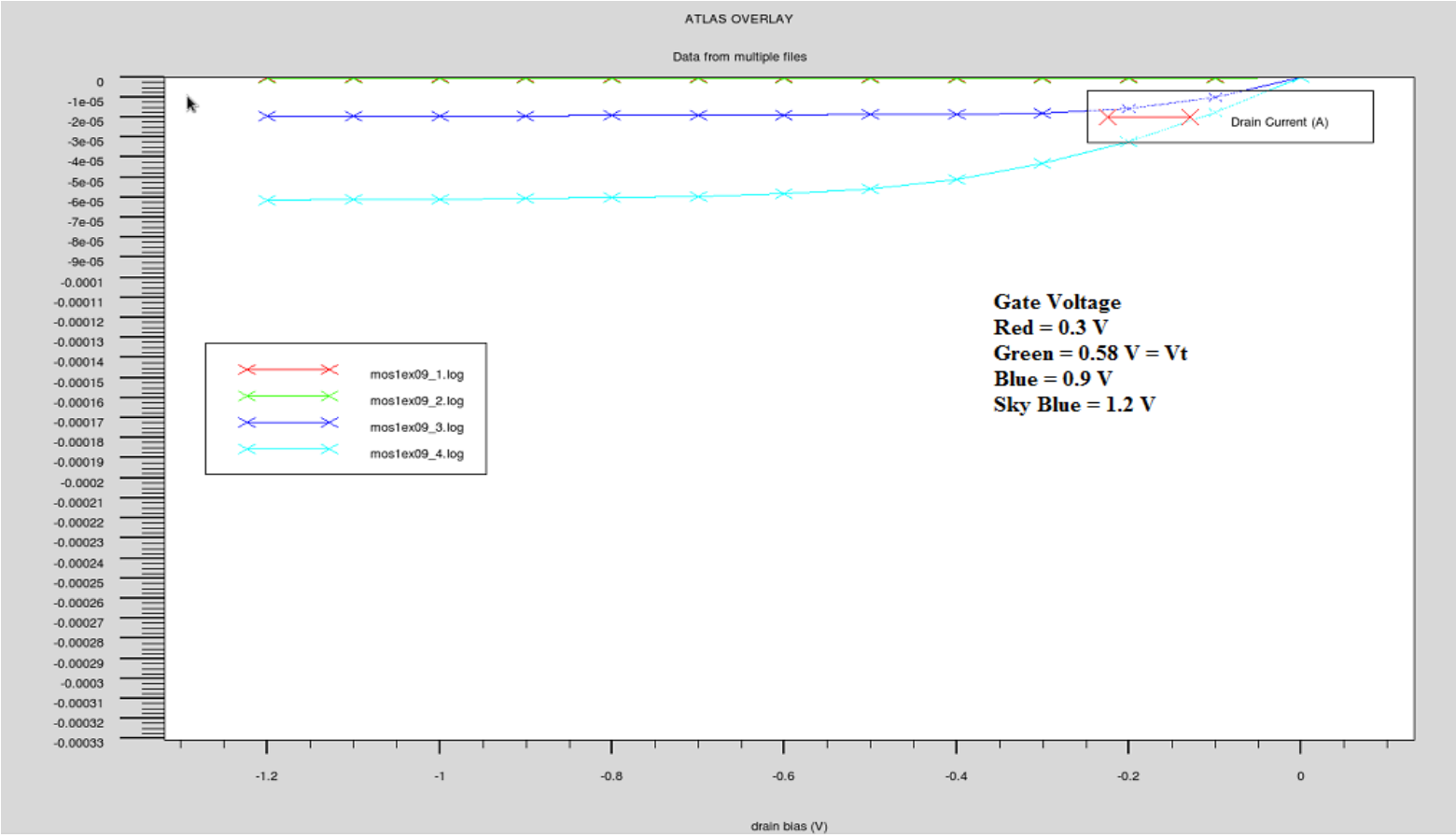


Models cvt srh print
Contact name=gate n.poly (NMOS) / p.poly (PMOS)
Interface qf=3e11

Id: **300 *μA/μm*** @ Vg=Vd= 1.2 *V*

Family of Curves

PMOS



Id: **63 *μA/μm*** @ Vg=Vd= -1.2 *V*

The reason for high carrier mobility in NMOS than in PMOS:

1. The mobility of electrons is greater than holes in silicon.
2. The dose of source/drain extension in NMOS (Arsenic:5e15 cm^{-2}) is greater than in PMOS (BF2: 9.0e14 cm^{-2}).

Changes Required

- Changes to be made in the existing process and in MESA are
  - Well implant dose and energy.
  - Reduction in anneal time from 5 hours to 4 hours (Thermal Budget).
  - Retrograde well implant
  - Removal of threshold adjust implants.
  - Develop a recipe to deposit a thin layer of gate oxide.
  - Develop recipes to deposit thin layer of Titanium.
  - Develop Source/drain anneal recipe on RTP tool for spike annealing.

References

- Bruce furnace recipes http://people.rit.edu/lffeee/Bruce_Furnace.pdf
- Diffusion and implant models, 'Athena user manual'
- Electrical simulation models, 'Atlas user manual'