CMOS Testing for the Student Run Factory

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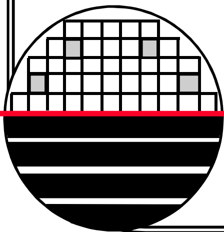

Revised 9-28-2009 cmostest.ppt

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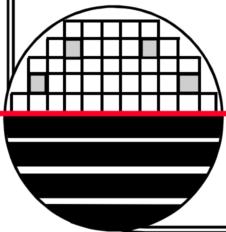
OUTLINE

Introduction
Test Structures
Test Equipment
Resistive Tests
Transistors
Integrated Circuits
Wafer Mapping



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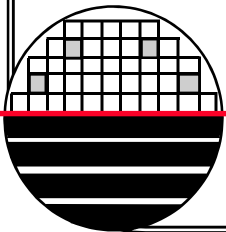
INTRODUCTION

Completed factory wafers are tested as part of the manufacturing process to capture data on processing parameters and transistor characteristics. Some simple integrated circuits are tested to verify functionality of more complex circuits. Uniformity is evaluated by measuring some parameters, such as threshold voltage, over the entire wafer.

These tests are broken into four tasks that can be completed in our normal three hour laboratory time: 1. sheet resistance and contact resistance, 2. transistors, 3. inverters, ring oscillator and op amp, and 4. wafer map of NMOSFET threshold voltage.

More complex digital and analog integrated circuits are tested outside of the factory by those who are interested.



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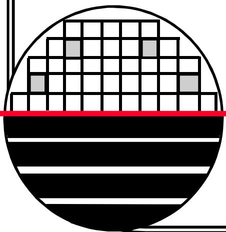
INTRODUCTION

Chip designs always include test structures for the factory in addition to the specific integrated circuit or microsystem being fabricated. The test structures are often located along the edges of the chip and might even be removed after testing during the wafer sawing process. These test structures are available as cells that can be easily added to the integrated circuit or microsystem design. The test setups can be used for all completed chips. Automated probing (rarely done at RIT) may require different setups if the test structures are in different locations on the wafer.

Three other documents provide additional details:

CMOSTestchip2008.pdf - description of latest factory chip
CMOSTEST_Manual.pdf –details for test equipment operation
TestResults.pdf – recent factory test results and template for reporting test results



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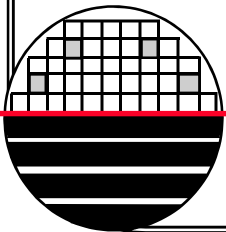
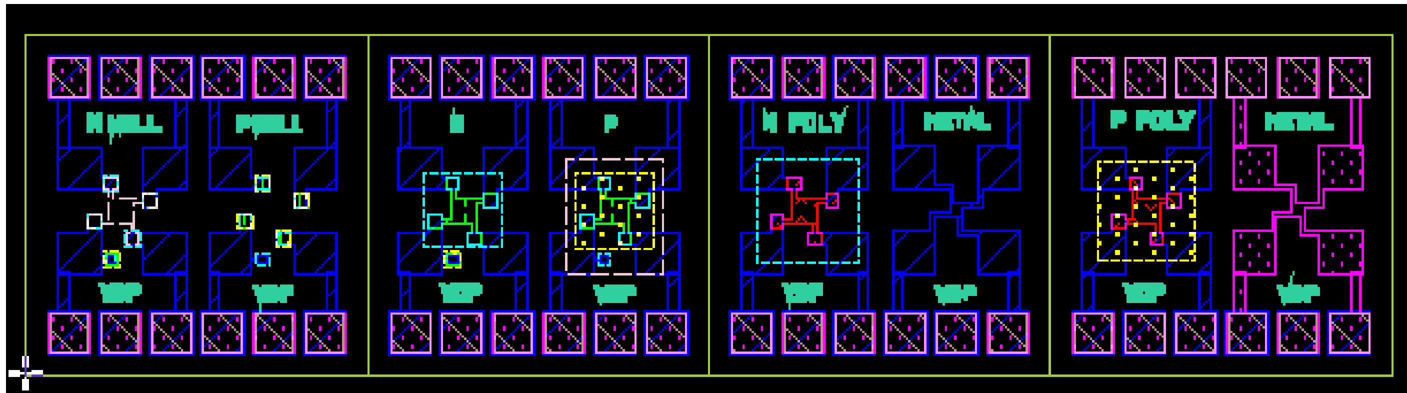
TEST STRUCTURES

List of factory test structures:

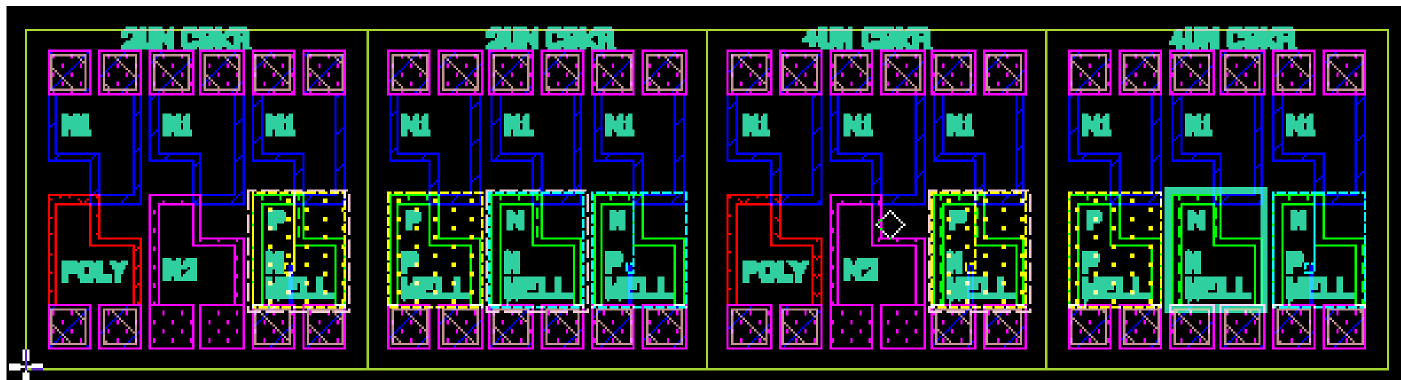
- Van Der Pauw's for sheet resistance
- CBKR's for contact resistance
- NMOS and PMOS transistors of various sizes
- Field Oxide NMOS and PMOS transistors
- Inverter
- Ring Oscillator
- Op Amp
- Metal serpentine's
- Via Chains



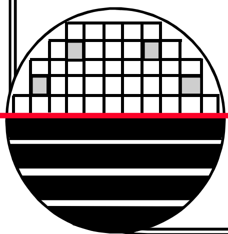
VAN DER PAUW's AND CBKR's



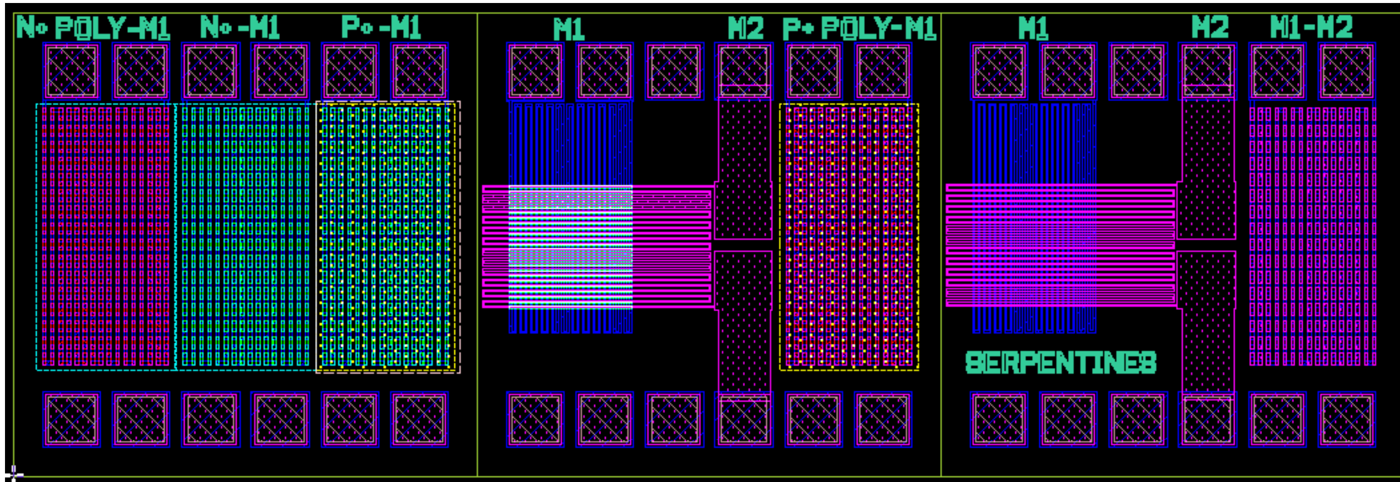
NWELL PWELL N+ P+ N-POLY M1 P-POLY M2



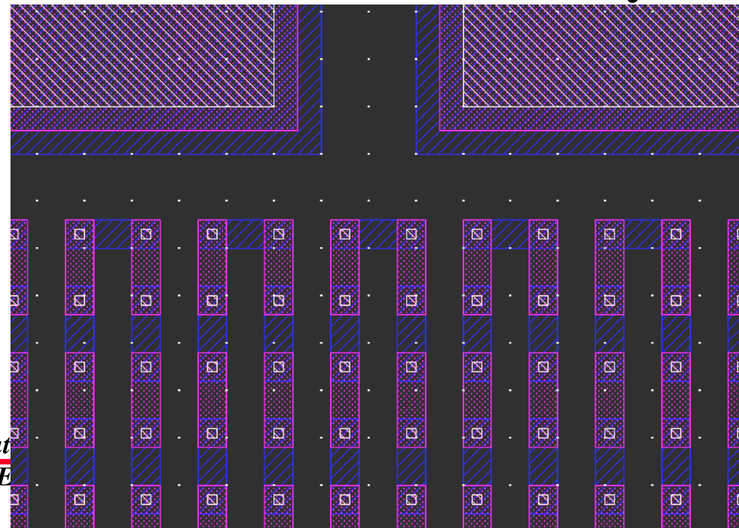
2µm M1toPoly	2µm M1toP+	4µm M1toPoly	4µm M1toP+
2µm M1toM2	2µm M1toN+	4µm M1toM2	4µm M1toN+
2µm M1toP+	2µm M1toN+	4µm M1toP+	4µm M1toN+

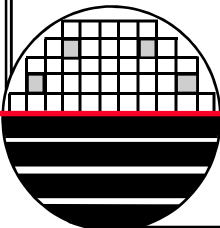


SERPENTINES, COMBS, AND VIA CHAINS



To evaluate metal1, metal2, CC and Via layer quality.





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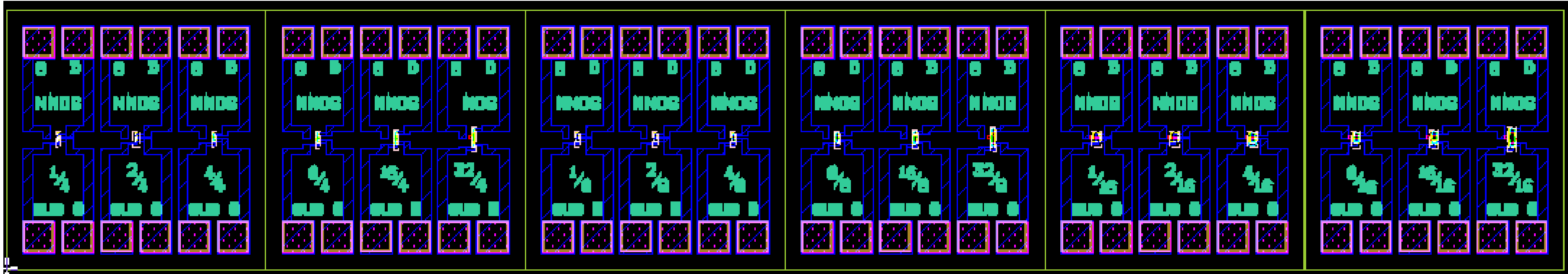
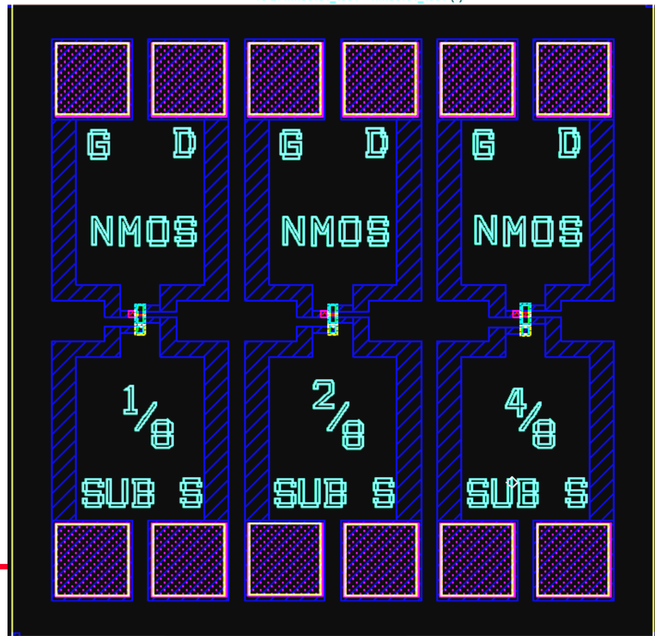
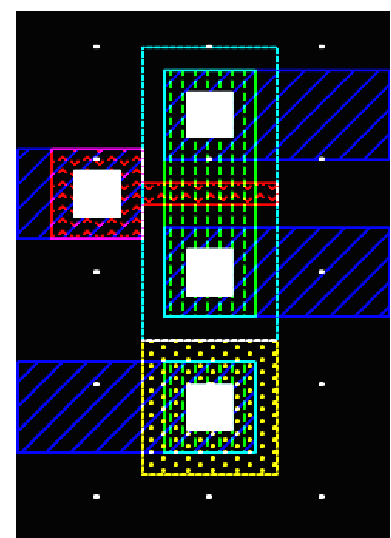
NMOS AND PMOS TRANSISTORS



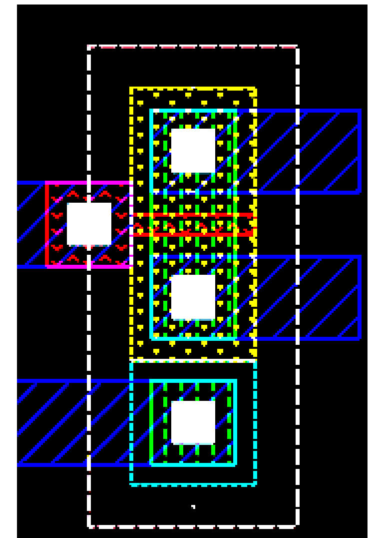
1/4 2/4 4/4 8/4 16/4 32/4 1/8 2/8 4/8 8/8 16/8 32/8 1/32 2/32 4/32 8/32 16/32 32/32

Various L/W Ratios

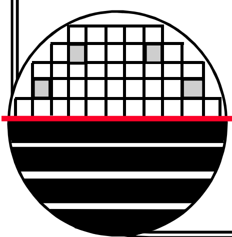




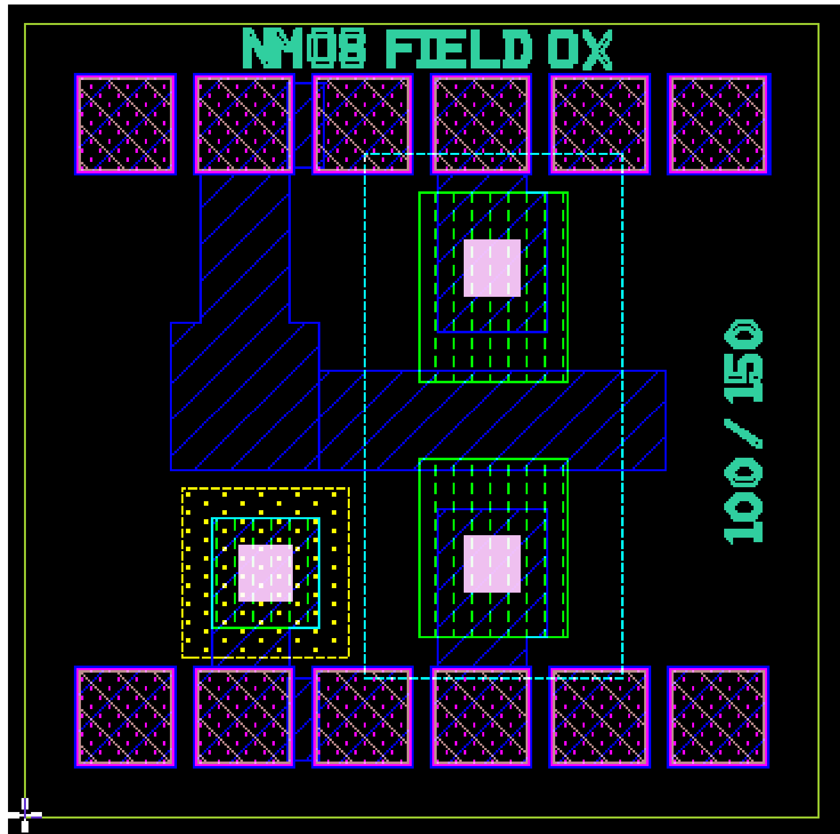
NMOS 2/8

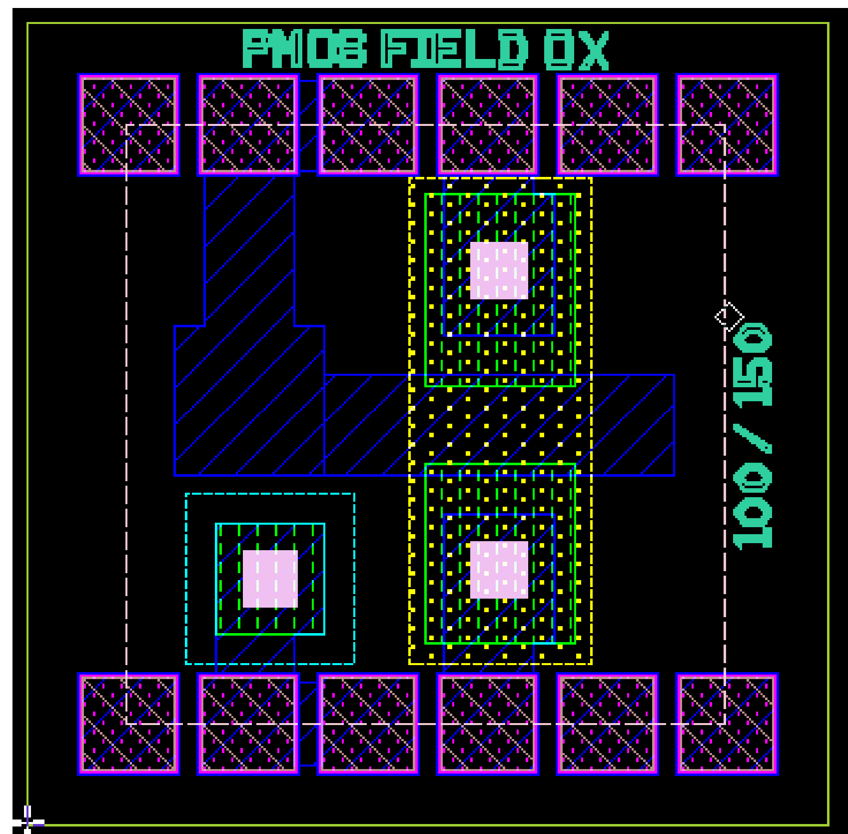


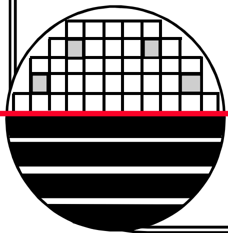
PMOS 2/8



FIELD OXIDE NMOS AND PMOS FET'S







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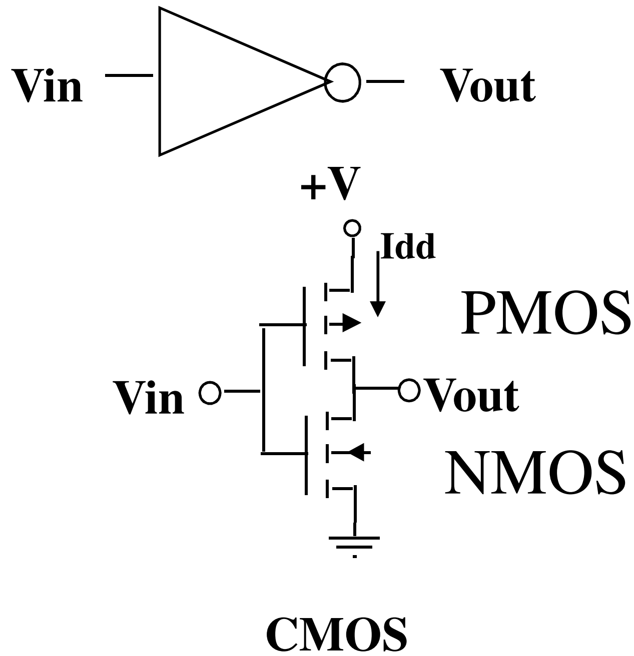
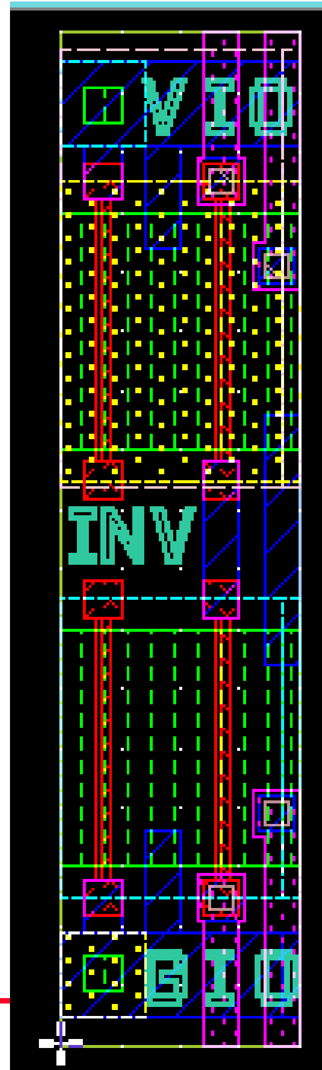
CMOS INVERTER

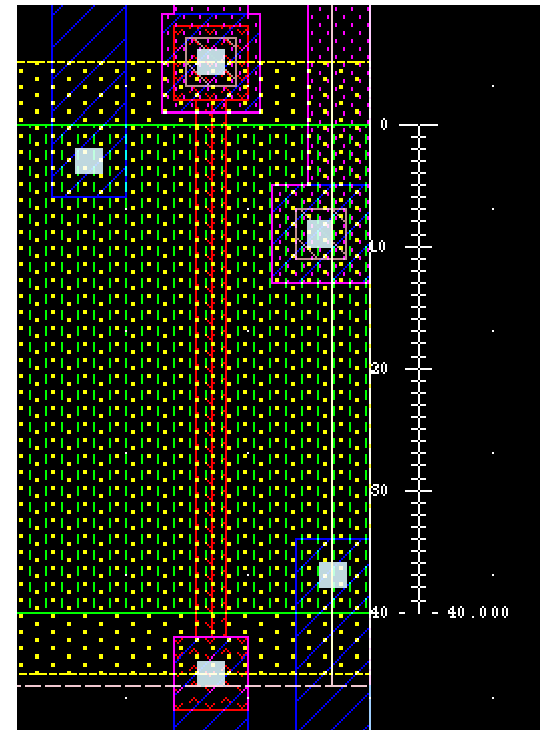


CMOS

TRUTH TABLE

VIN	VOUT
0	1
1	0



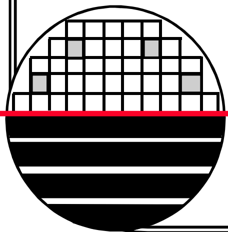


W = 40 µm

Ldrawn = 2.5µm

Lpoly = 1.0µm

Leff = 0.35 µm



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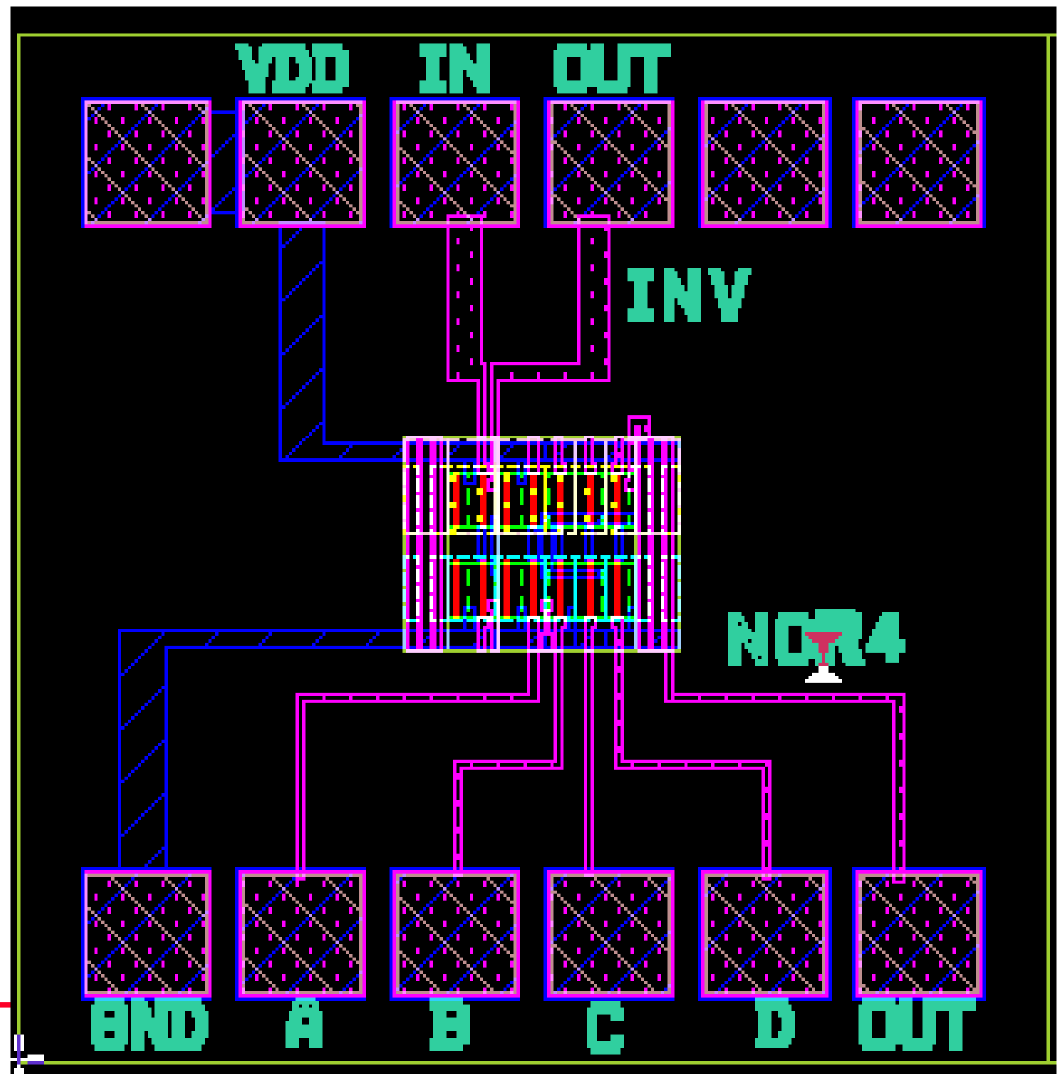
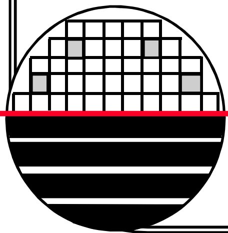
INVERTER WITH PADS

INV/NOR4





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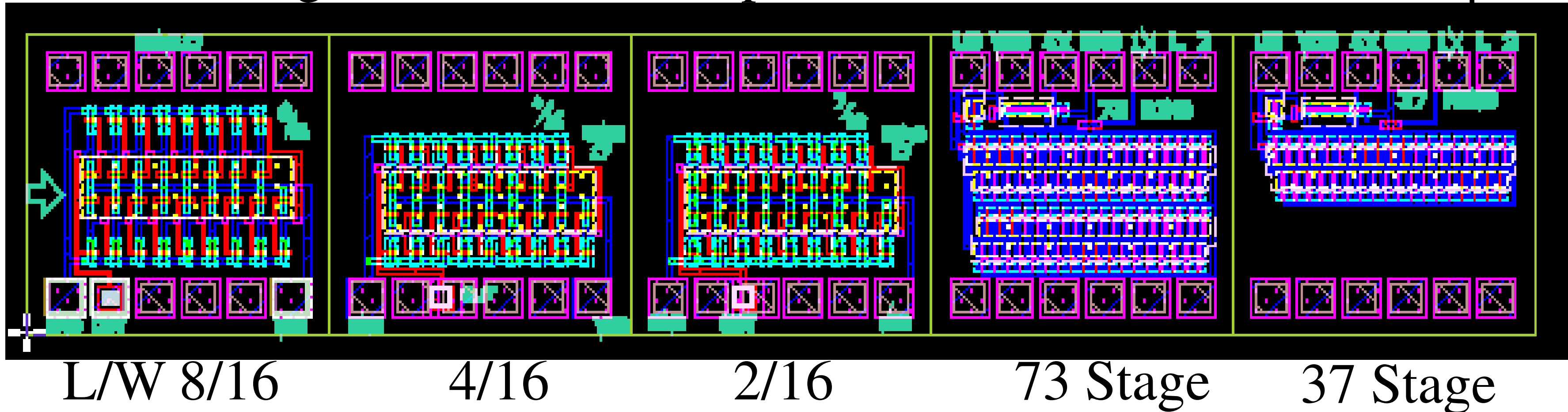
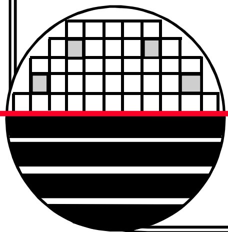
RING OSCILLATORS

17 Stage Un-buffered Output   L/W=2/30 Buffered Output



L/W 8/16   4/16   2/16   73 Stage   37 Stage



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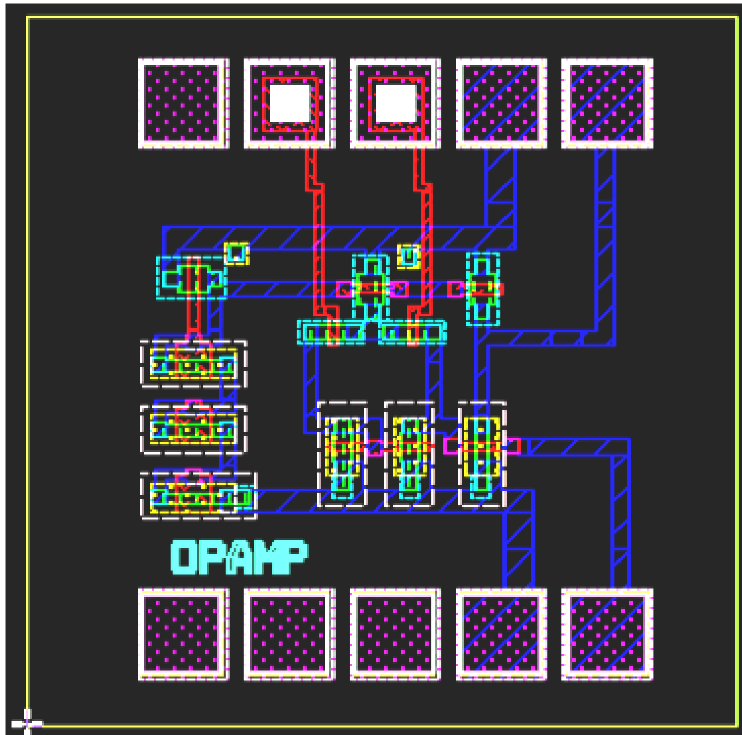
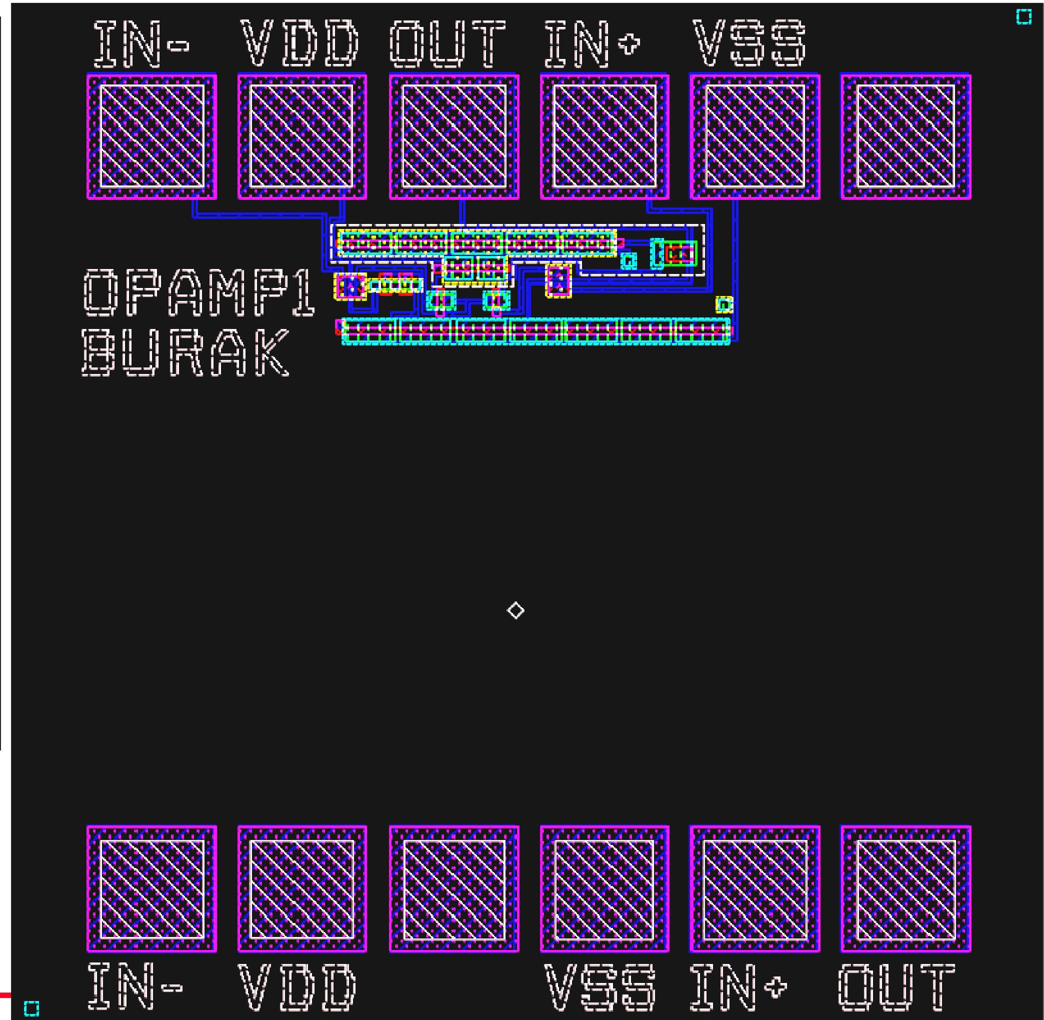
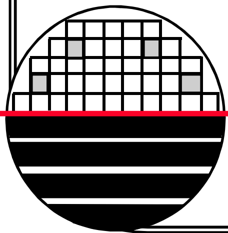
OPERATIONAL AMPLIFIERS

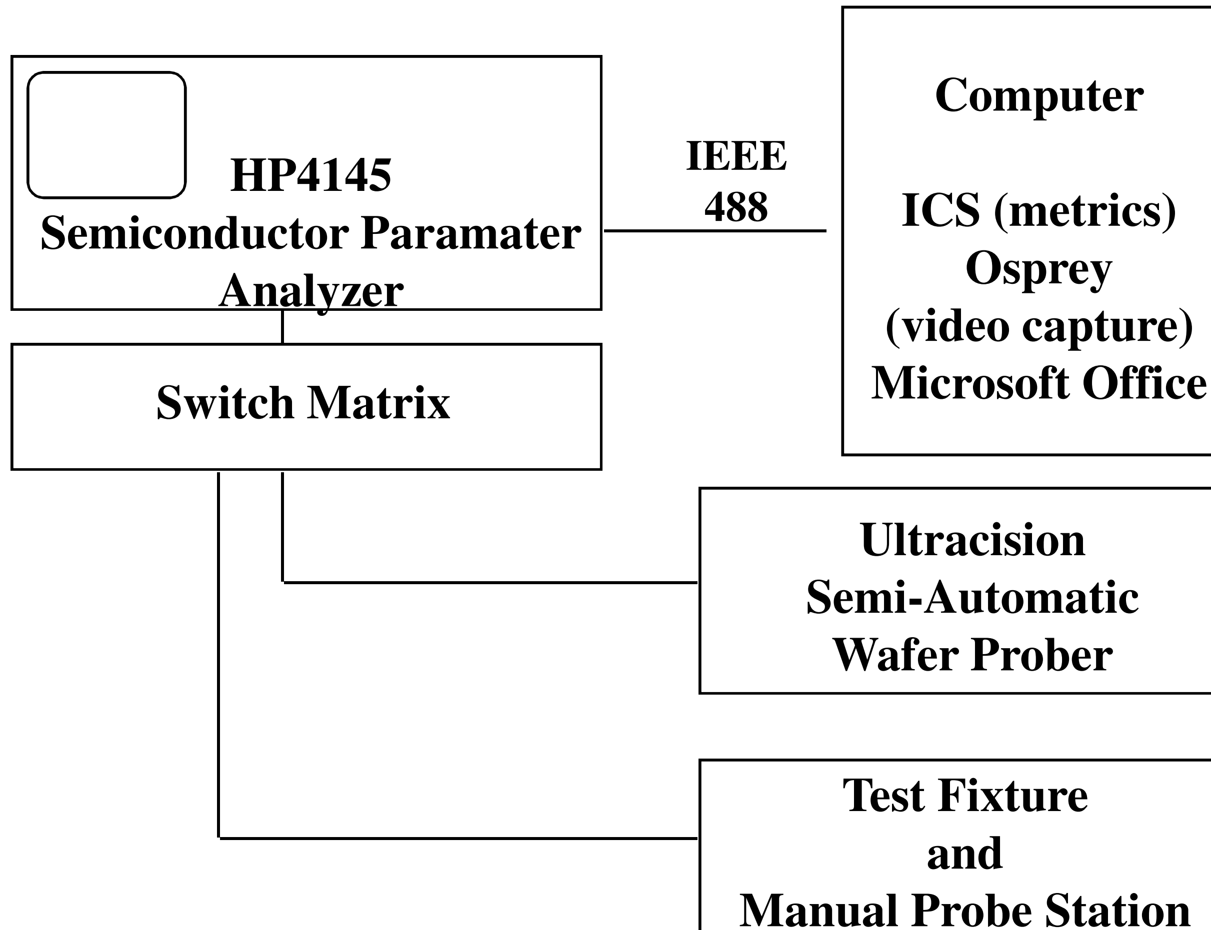


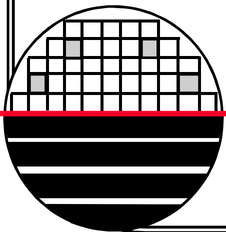
Version 1





TEST EQUIPMENT

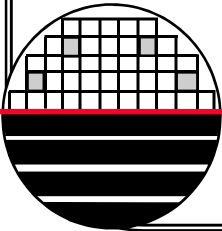




TEST EQUIPMENT

Automatic Prober

Semi-Automatic Prober



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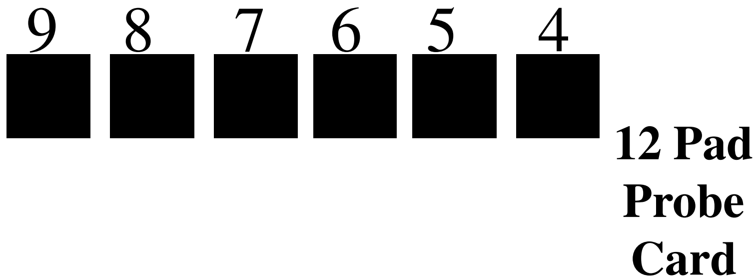
TEST EQUIPMENT

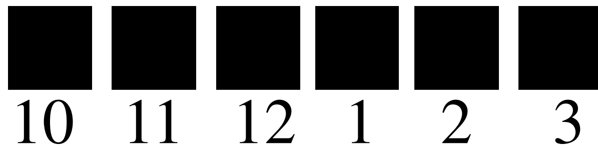
Manual Prober

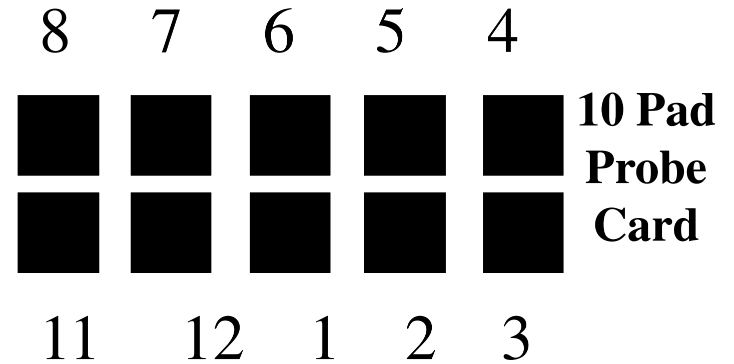
STANDARD PROBE CARDS & SWITCH MATRIX

Numbers indicate switch matrix column

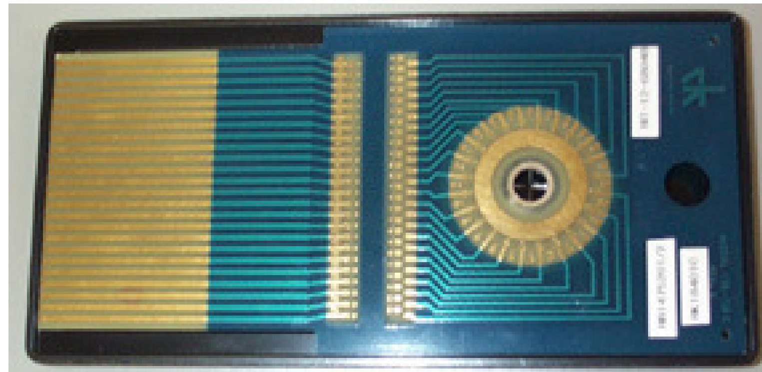


12 Pad Probe Card

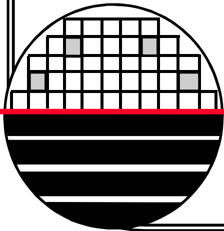




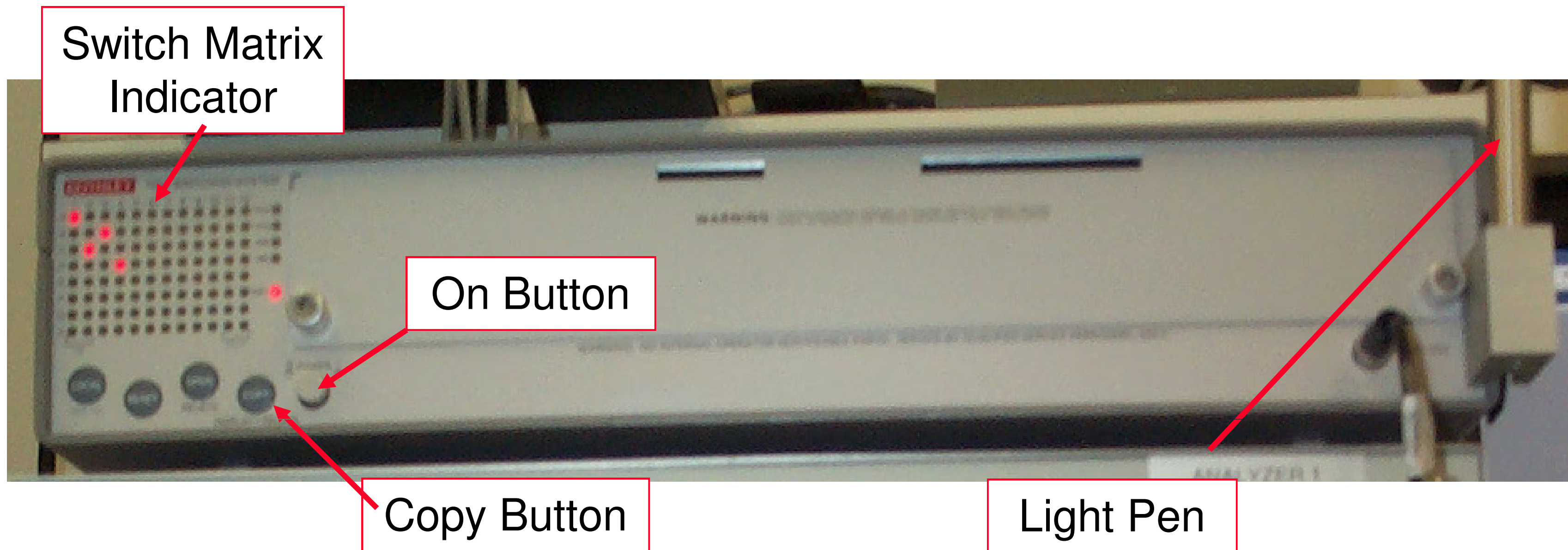
10 Pad Probe Card



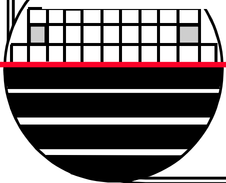
Probe Card



SWITCH MATRIX



The HP-4145 SMU-1 is connected to row 1, SMU-2 to row 2, SMU-3 to row 3 and SMU-4 to row 4. The probe pins are connected to the columns. The switch matrix indicator above shows SMU1 connected to col. 1 which is the 4th pin on the bottom row of the 12 pad probe card (see previous page)



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PROBING A NMOS TRANSISTOR

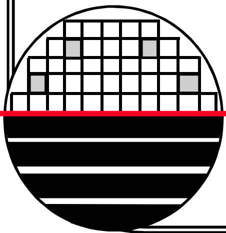
8 7
S D

Sub G
11 12

9 8 7 6 5 4

10 11 12 1 2 3

2/16 L/W NMOS FET



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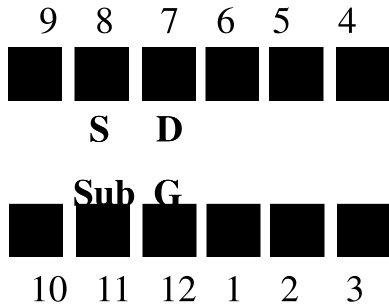
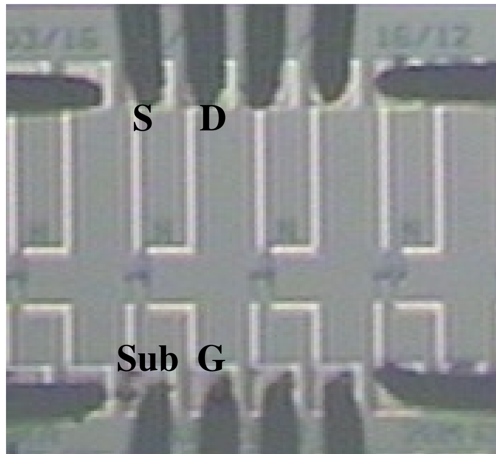
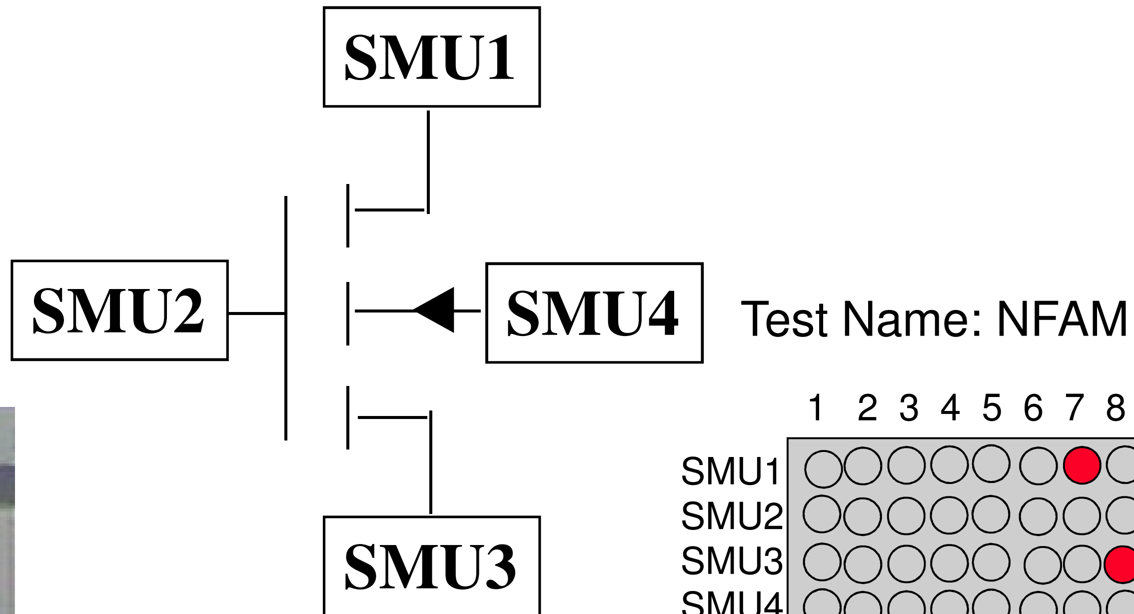
ICS TEST SET UP for NMOSFET FAMILY OF CURVES





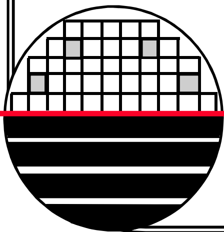


Test Name: NFAM

	1	2	3	4	5	6	7	8	9	10	11	12
SMU1	○	○	○	○	○	○	●	○	○	○	○	○
SMU2	○	○	○	○	○	○	○	○	○	○	○	●
SMU3	○	○	○	○	○	○	○	●	○	○	○	○
SMU4	○	○	○	○	○	○	○	○	○	○	●	○

Switch matrix

SMU1	Vds	Sweep 0 - 5 V, 101 steps
SMU2	Vgs	11 Steps 0 - 5V
SMU3	Com	Vs = 0
SMU4	Com	0 V



GENERAL TEST INSTRUCTIONS

Test die in the center of the wafer, then upper left, upper right, lower right, and lower left (about ½ way between center and edge). Extract parameter values from the test results.

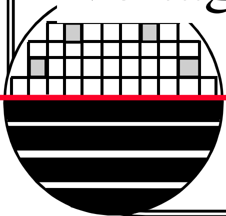
Create a PowerPoint document from **test_results.ppt** master (see example data powerpoint a few pages below) on Dr. Fullers webpage at http://people.rit.edu/lffeee/labnotes.htm (save as) record Lot#, Wafer#, Die location (center, top left,etc), pictures of die, test results graphs, extracted parameters and comments. Email to Dr. Fuller at Lynn.Fuller@rit.edu

Test 01 – Van Der Pauw and CBKR. Record Average of five tests
Test 02 – Transistors, test small transistors (L=2µm for SMFL, L=1µm for Sub-CMOS and Adv-CMOS). Record results in power point document.
Test 03 – Inverters, Ring Oscillator. Record Average of five tests.
Test 04 – NMOS VT wafer map

GENERAL TEST INSTRUCTIONS

Substrate or Well Connections: Most of the test structures incorporate diffusions. In Resistors, Van der Pauw's and Transistors the junctions between the diffusions and the substrate/wells are normally never forward biased. As a result the test engineer needs to evaluate the applied test voltages and connections to the substrate/wells and connections to the diffusions to ensure proper bias conditions.

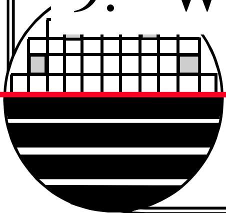
For example: a P+ Van der Pauw in an N-type Well requires that the Well connection always have the highest positive voltage that is applied. If a separate (5th pad) connection is available (not often because there are only 4 SMU's) that can be set to a high voltage. Otherwise the substrate is normally connected to one of the four pads of the Van der Pauw. This pad can be swept with positive voltage thus keeping the substrate/well junction reverse biased.



GENERAL TEST INSTRUCTIONS

Each test requires you to:

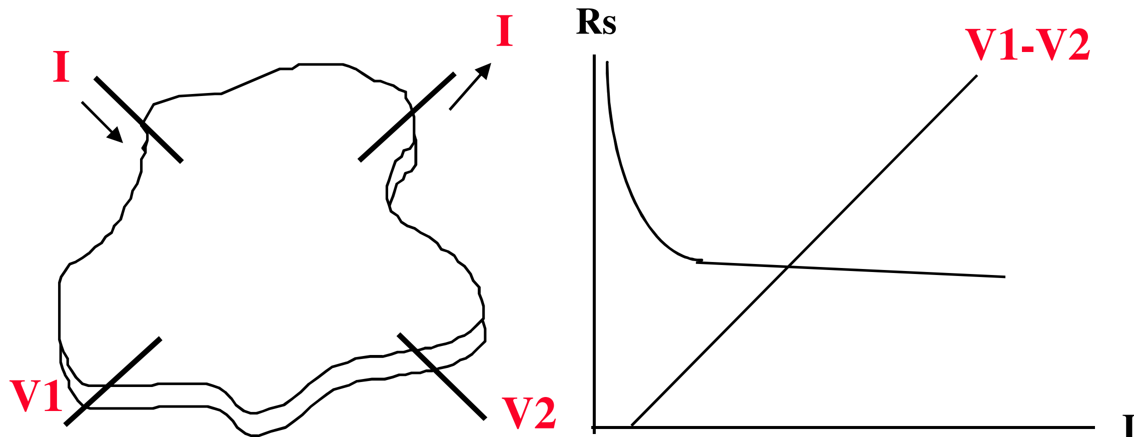
1. Find the structure you want to test
2. Place the probes
3. Open the test by restoring the “testname”-1 (example PFAM-1) in ICS, view the test setup to see what SMU’s do what.
4. Set the switch matrix for the HP4145 SMU’s to the probes you are using, consistent with the test setup.
5. Edit the graph by making changes in the title, moving the cursors to the correct location
6. Copy the plot using ctrl print screen, (paste into word, copy from word to power point, crop and paste in correct location)
7. Extract the data, such as threshold voltage or LAMBDA and enter the value in the data table in the powerpoint
8. Save the powerpoint, minimize the data plot on ICS
9. When done email the powerpoint to Lynn.Fuller@rit.edu

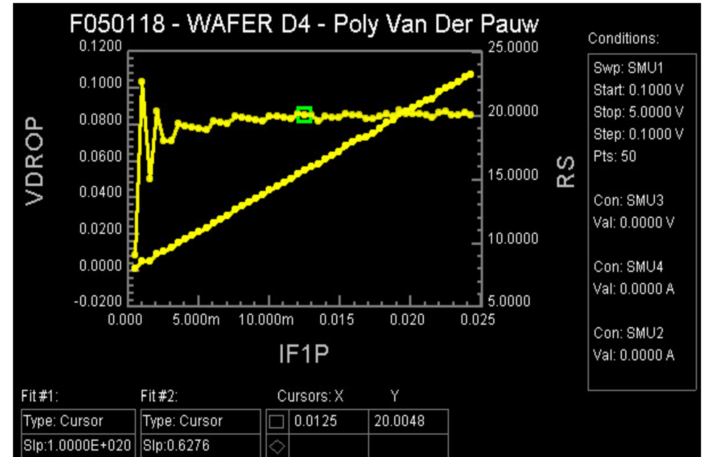


TE01 VAN DER PAUW AND CBKR

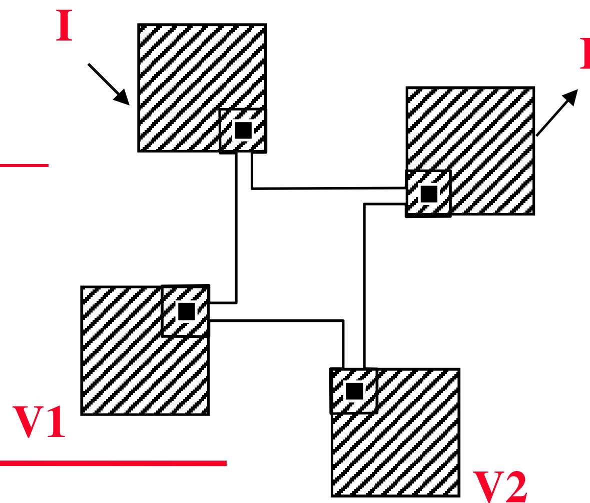
```
     5/04/06                      MESA                     IGMSINQ     S36801
     8:31:04            Instruction Group Inquiry          QPADEV000W    RIT

 Type information.  Then Enter.
   1=Display document, 5=Display detail

   Plant  . . . . . . . . :    RIT
   Instruction group  . .    SUB-CMOS-TE01           TEST COMPLETED WAFERS
     Revision . . . . . . .    150

   Opt  Subgroup   Text
    _              1.0 Test Resistive Devices
    _              2.0 Test Van Der Paw for Poly, Metal, n+/p+ Diffusion, Well
    _              3.0 Cross Bridge Kelvin Structures for contact resistance
    _              4.0 Via chain yes/no test (enter yes if via chain is good)
    _              5.0 See SPC chart for PolySi Resistance(PolySRes.pps)
    _              6.0 See SPC chart for NRRHOS (NTRHOS.pps)
    _              7.0 See SPC chart for WellRes (WellRes.pps)
    _              8.0 See SPC chart for PTRHOS (PTRHOS.pps)
    _              9.0 Record Rhos(poly, metal, p+, n+, well)
    _                  Gc(metal-to-poly)mhos-sq um, Gc(metal-to-p+)mhos-sq um
                                                                      Bottom
 F3=Exit   F4=Prompt   F5=Refresh   F10=View 2   F12=Cancel
```

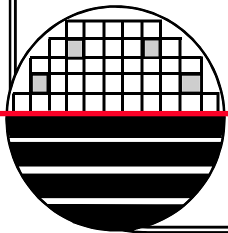
VAN DER PAUW STRUCTURES FOR SHEET RESISTANCE





$$Rs = \frac{(V1-V2)}{I}\frac{\Pi}{\ln 2}$$





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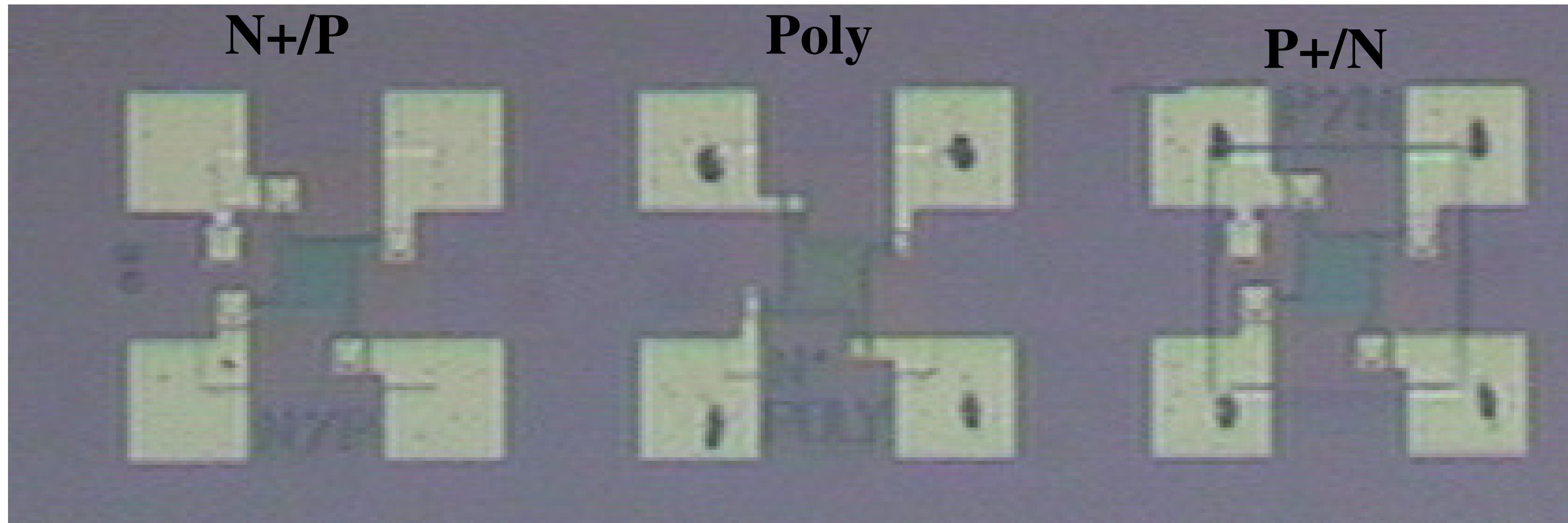
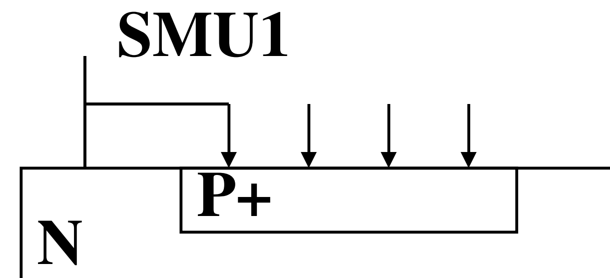
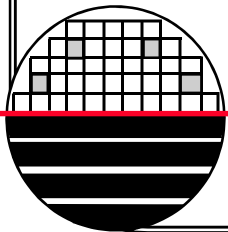
VAN DER PAUW WITH SUBSTRATE CONNECTIONS



Note: connection to N has to be to the highest voltage used to prevent P+/N junction from being forward biased





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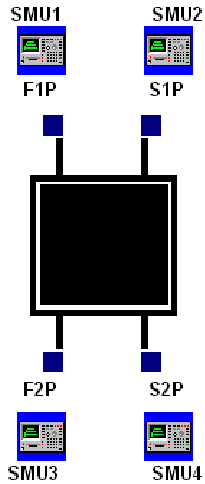
VAN DER PAUW WITH SUBSTRATE CONNECTIONS

Source: SMU1
- Stimulus: (•) Voltage, ( ) Current
- Measure: [x] Voltage VF1P, [x] Current IF1P
- Sweep Time: Hold 0.0000, Delay 0.0000
- Force Conditions: Mode SWEEP, Type LIN, Start 0.1000 Volts, Stop 5.0000 Volts, No. Points 50, Step Size 0.1000 Volts, Compl 0.1000
- Time Stim: (•) Voltage, ( ) Current
- Time Measurement Bias: Time Bias 0.0000 Volts, Compliance 0.1000

Source: SMU2
- Stimulus: ( ) Voltage, (•) Current
- Measure: [x] Voltage VS1P, [ ] Current
- Sweep Time: Hold 0.0000, Delay 0.0000
- Force Conditions: Mode CONST, Value 0.0000 Amps, Compl 1.0000
- Time Stim: (•) Voltage, ( ) Current
- Time Measurement Bias: Time Bias 0.0000 Volts, Compliance 0.1000



Transform Editor

Setup Name: VDPP   Edit Constants...

Transform:

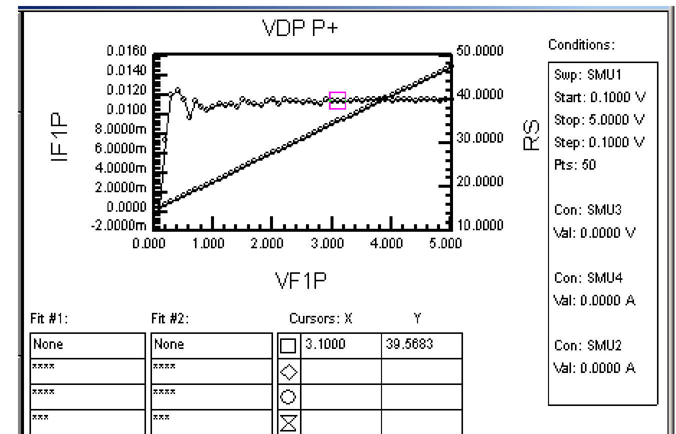
VDROP=VS1P-VS2P
RS=4.532*VDROP/IF1P

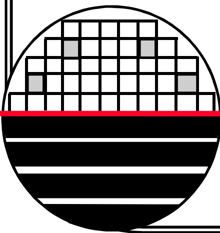
(,) <- Backspace + - * /

Functions:	Vectors:	Constants:
ABS	VF1P	PI [rad]
ARCCOS	IF1P	K [J/K]
ARCSIN	VS1P	Q [C]
ARCTAN	VS2P	MO [kg]
AT	VDROP(+)	EV [J]
AVG	RS(+)	UO [H/m]

Source: SMU3
- Stimulus: (•) Voltage, ( ) Current
- Measure: [ ] Voltage, [ ] Current
- Sweep Time: Hold 0.0000, Delay 0.0000
- Force Conditions: Mode CONST, Value 0.0000 Volts, Compl 0.1000
- Time Stim: (•) Voltage, ( ) Current
- Time Measurement Bias: Time Bias 0.0000 Volts, Compliance 0.1000

Source: SMU4
- Stimulus: ( ) Voltage, (•) Current
- Measure: [x] Voltage VS2P, [ ] Current
- Sweep Time: Hold 0.0000, Delay 0.0000
- Force Conditions: Mode CONST, Value 0.0000 Amps, Compl 1.0000
- Time Stim: (•) Voltage, ( ) Current
- Time Measurement Bias: Time Bias 0.0000 Volts, Compliance 0.1000





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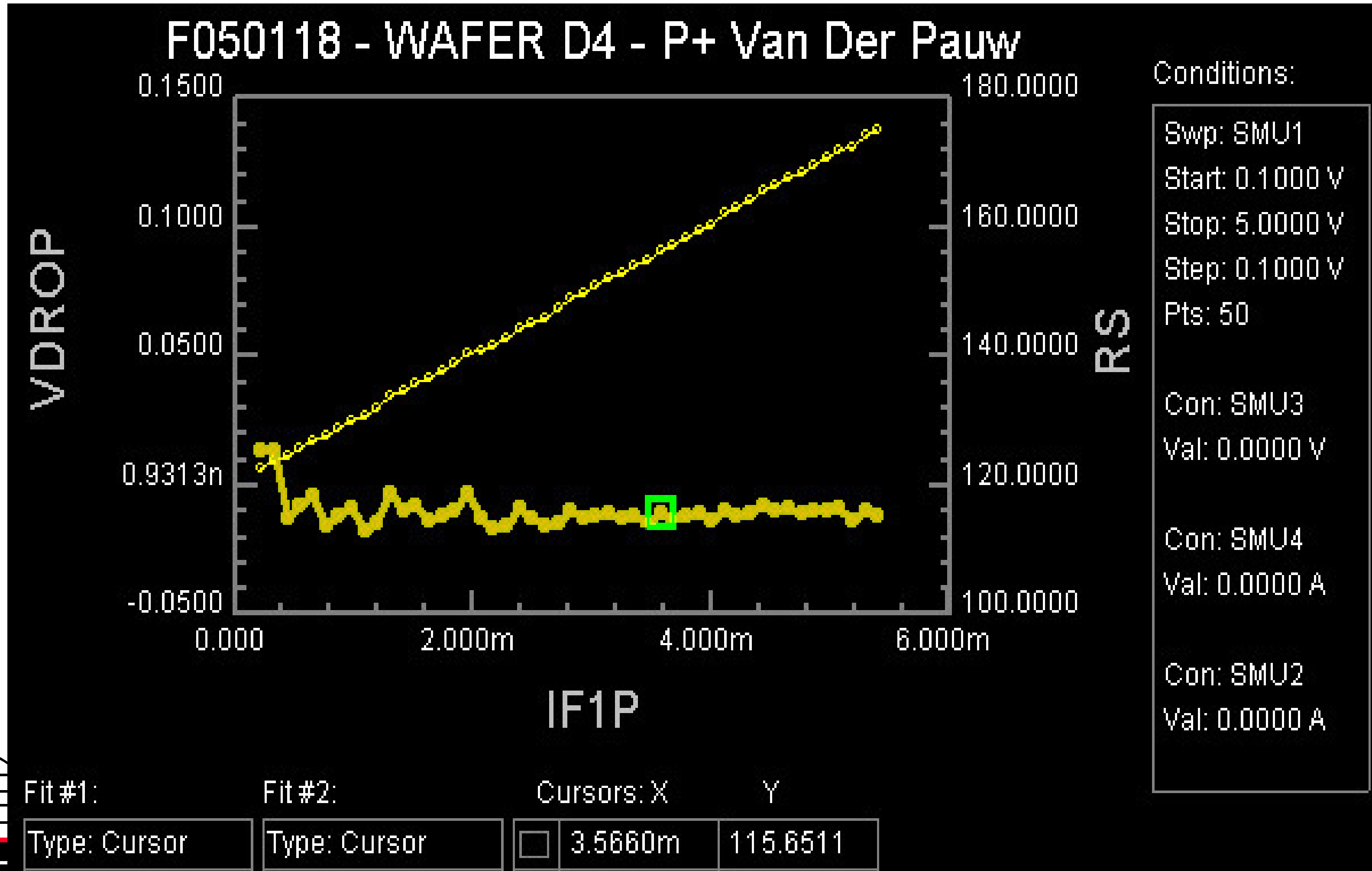
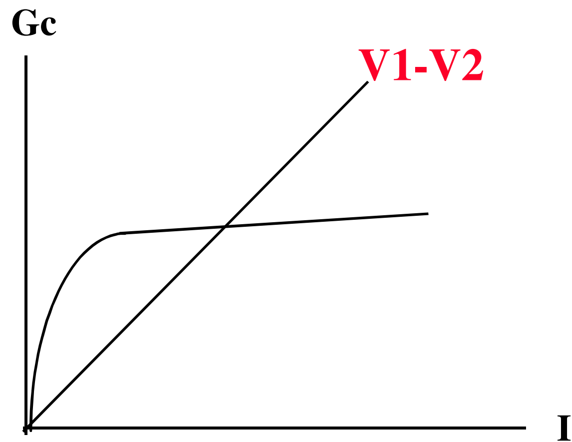
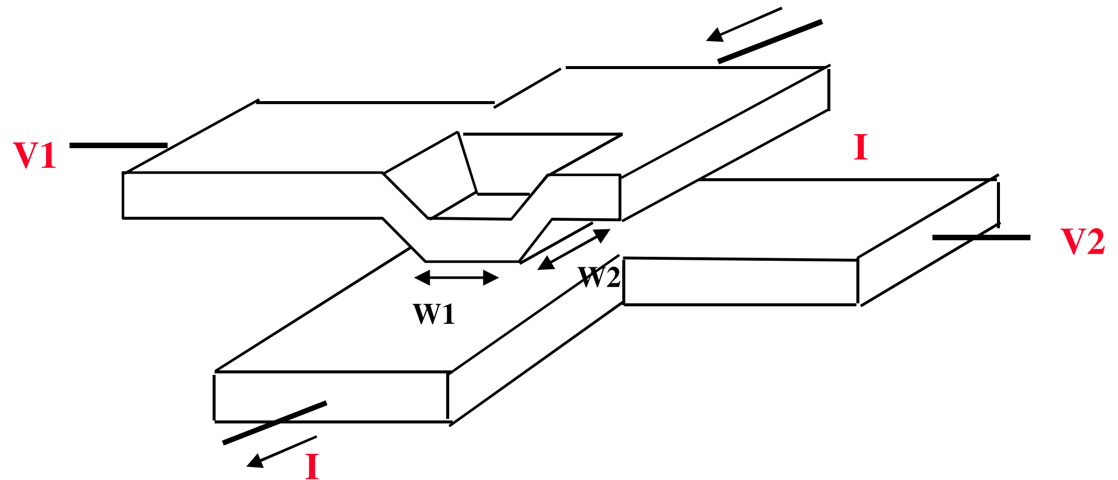
HP 4145 OUTPUT PLOT



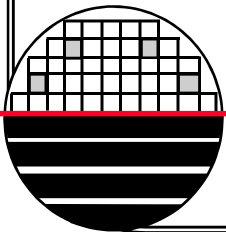
CROSS BRIDGE KELVIN RESISTANCE TEST STRUCTURES FOR CONTACT RESISTANCES





$$Rc = \frac{(V1-V2)}{I} \quad \text{ohms}$$

$$Gc = \frac{I}{(V1-V2)} \frac{1}{W1 \times W2} \quad \text{mhos}/\mu m^2$$



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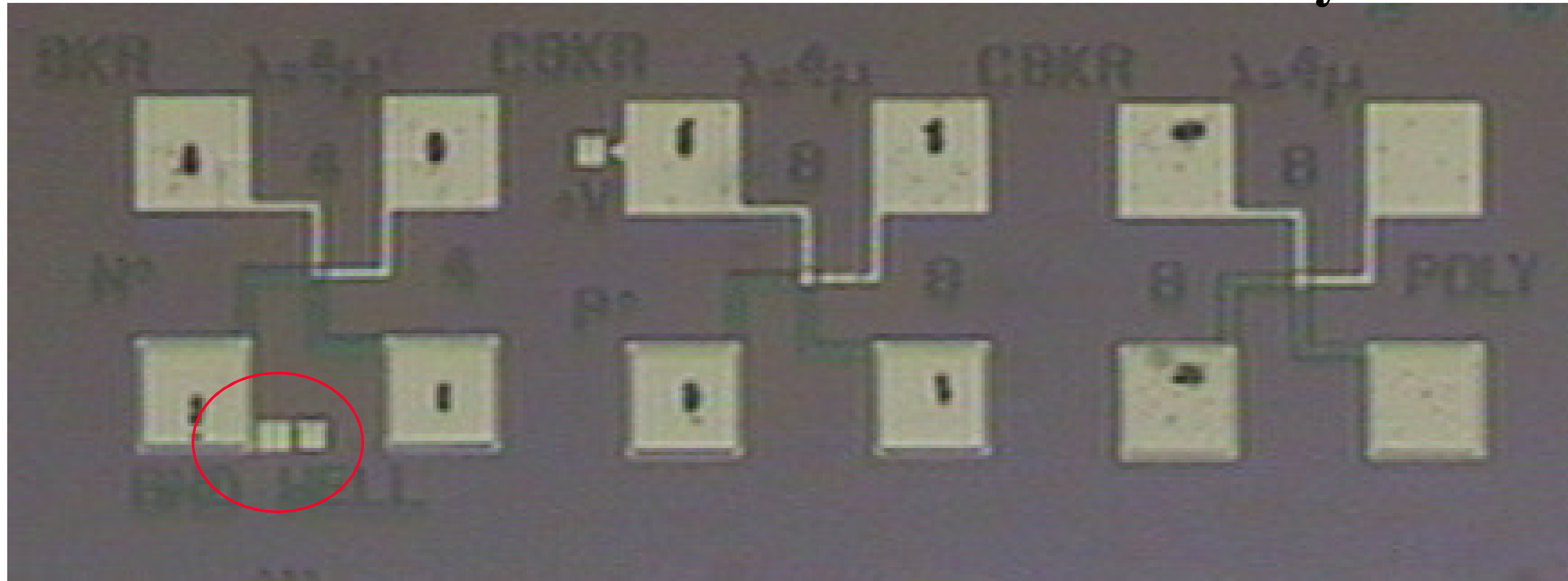
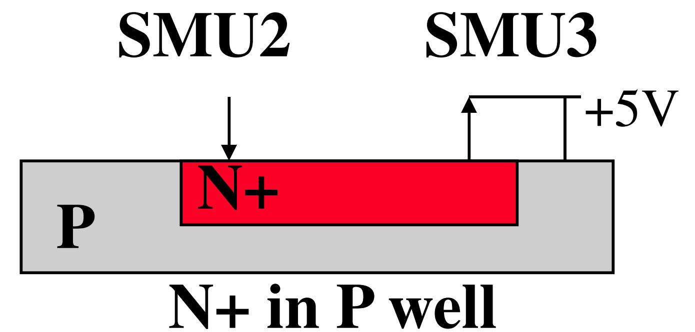
CBKR WITH SUBSTRATE CONNECTIONS

N+ in P well P+ in N well Poly



Note: connection to N+ has to be to the highest voltage used to prevent N+/P junction from being forward biased. SMU2 is swept from 0 to +5V, SMU3 is fixed at +5V



see next page.

HP 4145 OUTPUT PLOT

2UM X 2UM M1 TO P+ CBKR

VDROP_CBKR: 0.0000, -0.0250, -0.0500, -0.0750, -0.1000

GC: -0.0200, -0.0300, -0.0400, -0.0500

IS1P: 0.000, 1.000m, 2.000m, 3.000m, 4.000m

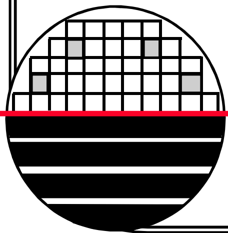
Conditions:

Con: SMU1
Val: 0.0000 A

Con: SMU4
Val: 0.0000 A

Swp: SMU2
Start: 1.0000 V
Stop: 5.0000 V
Step: 0.0500 V
Pts: 81

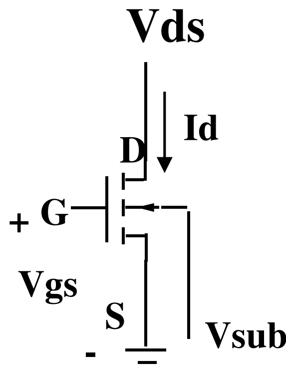
Fit #1:	Fit #2:	Cursors: X	Y
None	None	2.0191m	-0.0421
****	****		



TE02 TRANSISTORS

```
    5/04/06                    MESA                    IGMSINQ     S36801
    8:35:54          Instruction Group Inquiry         QPADEV000W    RIT

Type information.  Then Enter.
  1=Display document, 5=Display detail

  Plant . . . . . . . . :    RIT
  Instruction group  . .    SUB-CMOS-TE02         TEST COMPLETED WAFERS
    Revision . . . . . . .    150

  Opt  Subgroup   Text
   _              1.0 Test PMOS and NMOS Transistors
   _                  for threshold voltage, tranconductance, lambda,
   _                  subthreshold slope, min and max current value on the
   _                  subthreshold test
   _              2.0 Record VTn,VTp,gmn,gmp,sub-Vt-slope,Isub-min,Isub-max,
   _                  Lambda,transistor width&length for nmos & pmos, Vt field

                                                                      Bottom
F3=Exit   F4=Prompt   F5=Refresh   F10=View 2   F12=Cancel
```

TRANSISTOR FAMILY OF CURVES, ID-VDS



Lambda = slope/Idsat

D1 2/16=L/W Top Right NMOS

ID axis: 6.0000m, 4.0000m, 2.0000m, -0.0582n, -2.0000m

VD axis: 0.000, 1.000, 2.000, 3.000, 4.000, 5.000

Conditions:

Swp: SMU1
Start: 0.0000 V
Stop: 5.0000 V
Step: 0.0833 V
Pts: 61

Step: SMU2
Start: 0.0000 V
Stop: 5.0000 V
Step: 0.5000 V
Pts: 11

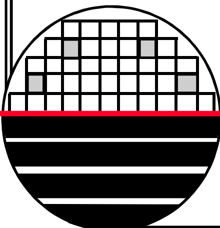
Con: SMU3
Val: 0.0000 V

Con: SMU4
Val: 0.0000 V

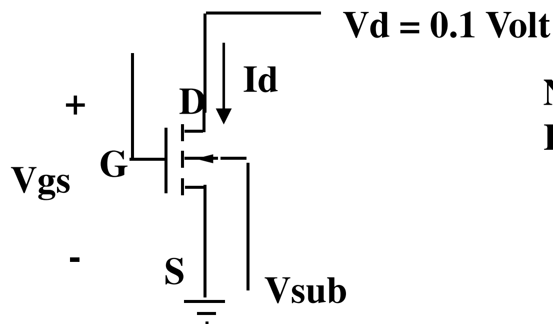
Fit #1:	Fit #2:
Type: Cursor	None
Slp:0.1576m	****
Yint:4.6770m	****
Xint:-29.6693	***

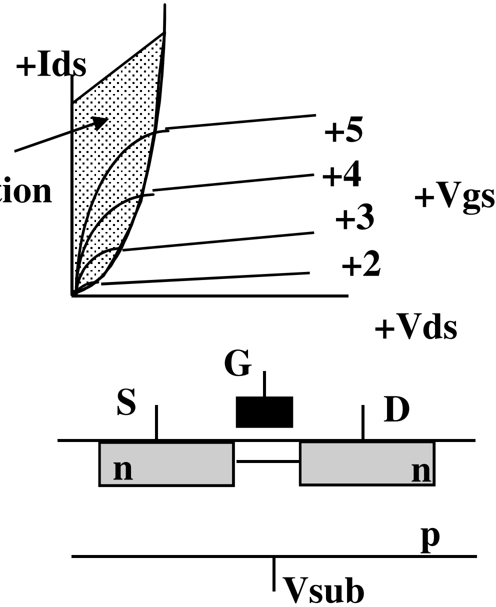
Cursors:	X	Y
□	2.8333	5.1236m
◇	4.6667	5.4126m
○		
⧗		
⋈		

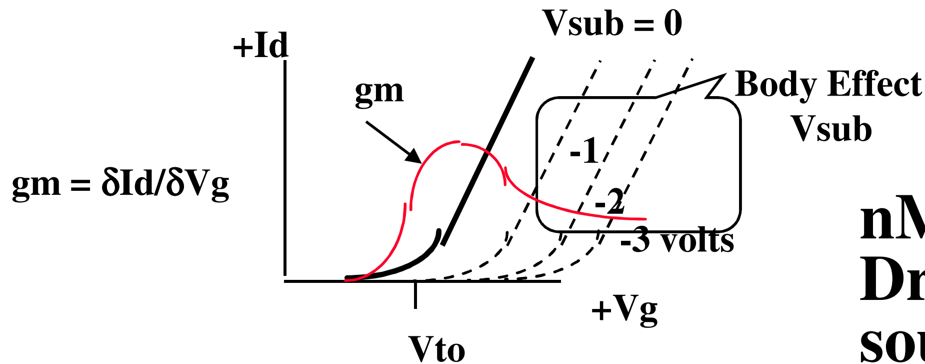
ICS 15:38:28



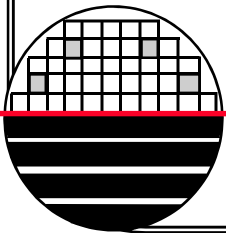
TRANSISTOR LINEAR REGION VT, GM







nMOSFET with Vt=1, since the Drain is at 0.1 volts and the source is at zero. Both drain and source will be on at gate voltages greater than 1.1 volt. the transistor will be in the non saturation region.



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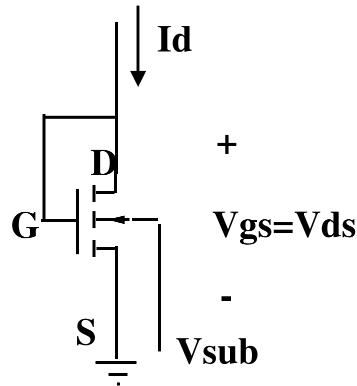
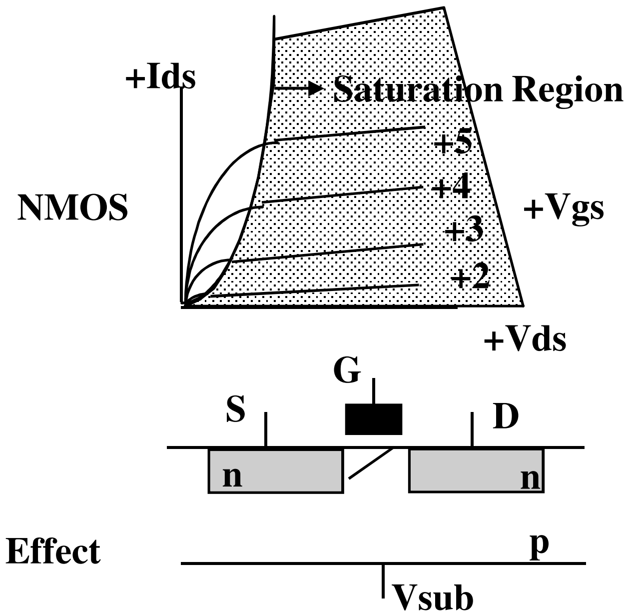
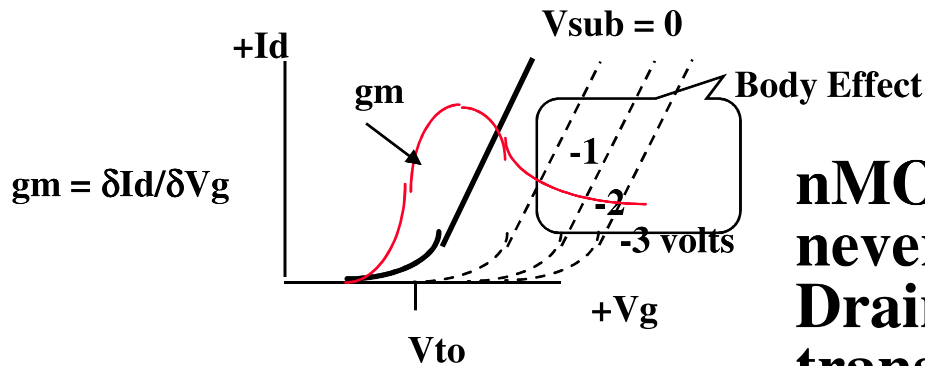
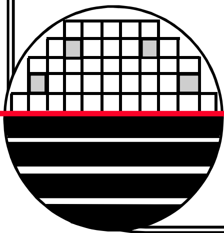
TRANSISTOR SATURATION REGION VT, GM



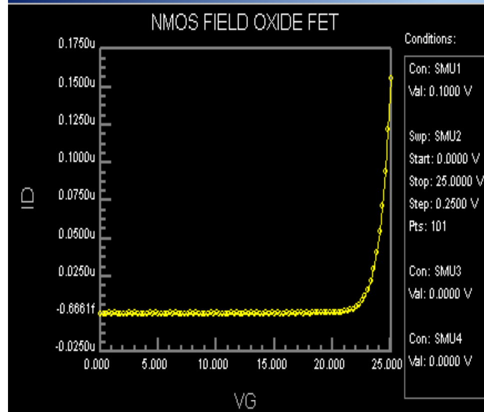




nMOSFET with Vt=1, Drain end is never on because Voltage Gate to Drain is Zero. Therefore this transistor is always in Saturation Region if the gate voltage is above the threshold voltage.



NMOS ID-VGS TEST



Same test for field oxide threshold voltage

gm = 0.16 mmho/16µm
= 0.010 S/mm

Vt = 0.507 volts

NMOS ID VS VGSL/W = 2/16

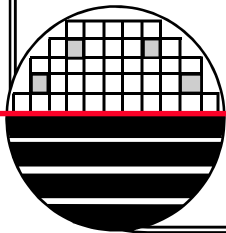
ID: 0.5000m, 0.4000m, 0.3000m, 0.2000m, 0.1000m, 6.0633p, -0.1000m

GM: 0.2000m, 0.1500m, 0.1000m, 0.0500m, 0.0000, -0.0500m

VG: 0.000, 1.000, 2.000, 3.000, 4.000, 5.000

Conditions:
Con: SMU1
Val: 0.1000 V
Swp: SMU2
Start: 0.0000 V
Stop: 5.0000 V
Step: 0.0500 V
Pts: 101
Con: SMU3
Val: 0.0000 V
Con: SMU4
Val: 0.0000 V

Fit #1:	Fit #2:	Cursors: X	Y
Type: Linear	None	□ 1.0000	0.0782m
Slp:0.1588m	****	◇ 1.2000	0.1099m
Y-int:-0.0805m	****	○ 1.1000	0.1592m
X-int:0.5070	***	⧗	



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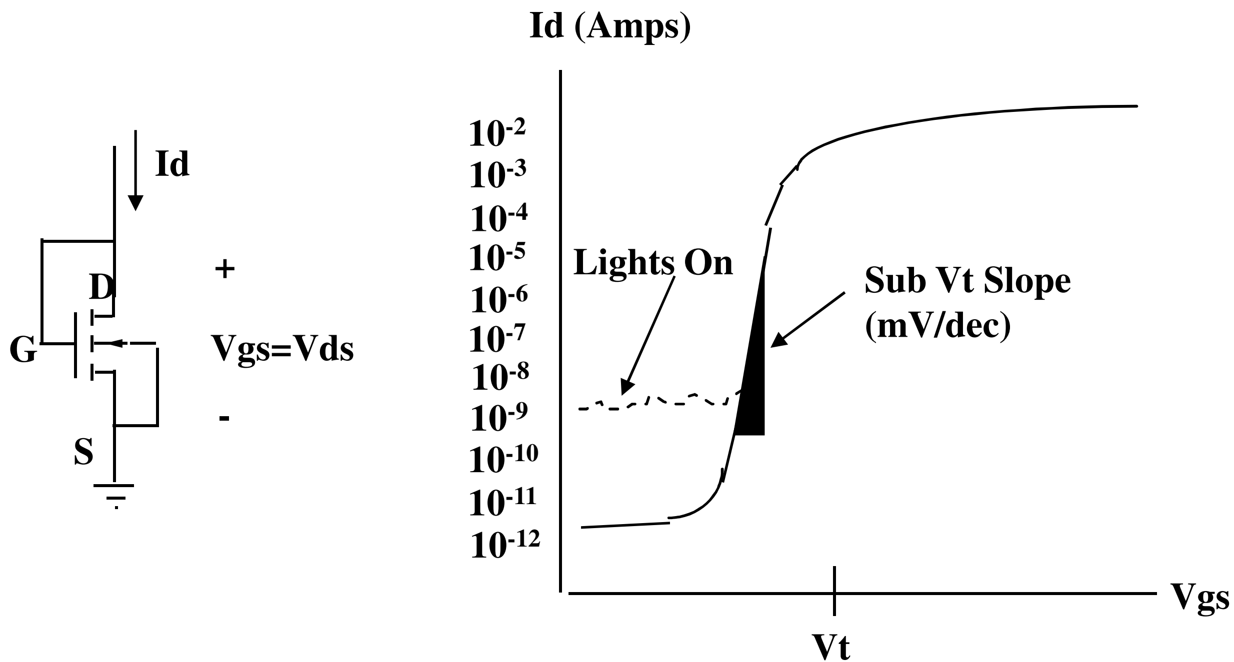
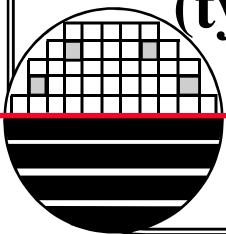
TRANSISTOR SUB THRESHOLD ID-VGS



The subthreshold characteristics are important in VLSI circuits because when the transistors are off they should not carry much current since there are so many transistors. (typical value about 100 mV/decade)

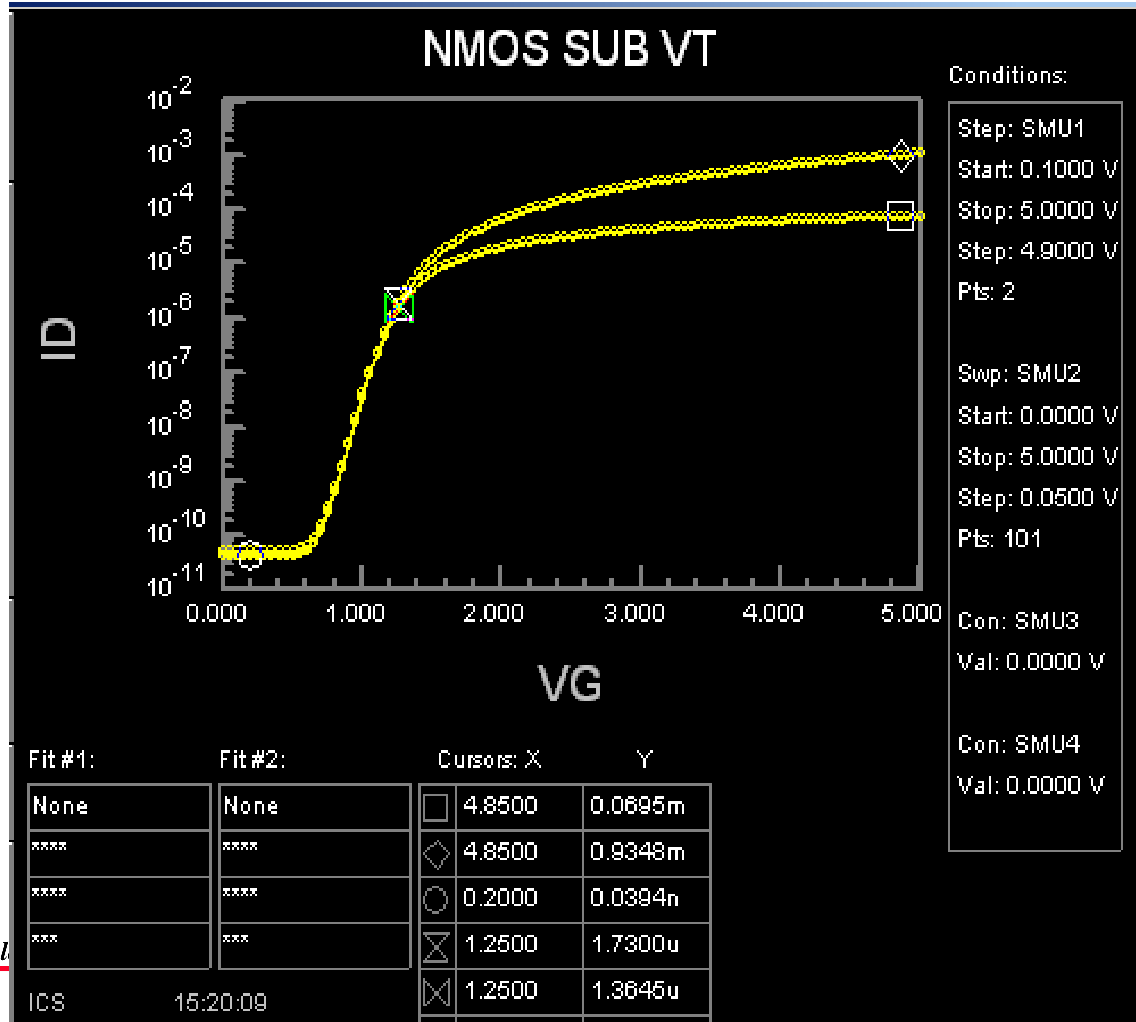


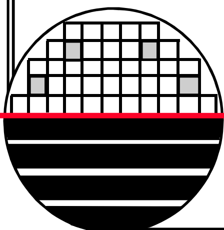
SUB THRESHOLD CHARACTERISTICS

Ion/Ioff = ~6 Decades

Swing = ~100 mV/dec

DIBL@1nA/µm
= ΔVg/ΔVd
= 0 mV/V





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TE03 INTEGRATED CIRCUITS

```
    5/04/06                         MESA                     IGMSINQ    S36801
    8:37:20               Instruction Group Inquiry          QPADEV000W   RIT

 Type information.  Then Enter.
   1=Display document, 5=Display detail

   Plant . . . . . . . . :    RIT
   Instruction group . .      SUB-CMOS-TE03           TEST COMPLETED WAFERS
     Revision . . . . . .     150

   Opt  Subgroup   Text
    _              1.0 Test Inverters and Ring Oscillator
    _              2.0 Record ViL, ViH, VoL, VoH, Vinv, Imax, Ring Oscillator
    _                  Frequency, Number of Stages

                                                                        Bottom
 F3=Exit   F4=Prompt   F5=Refresh   F10=View 2   F12=Cancel
```


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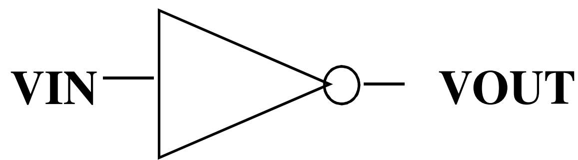
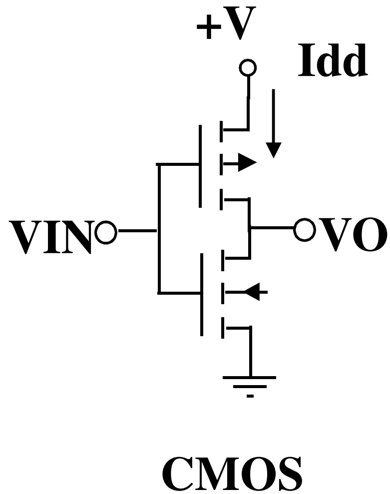
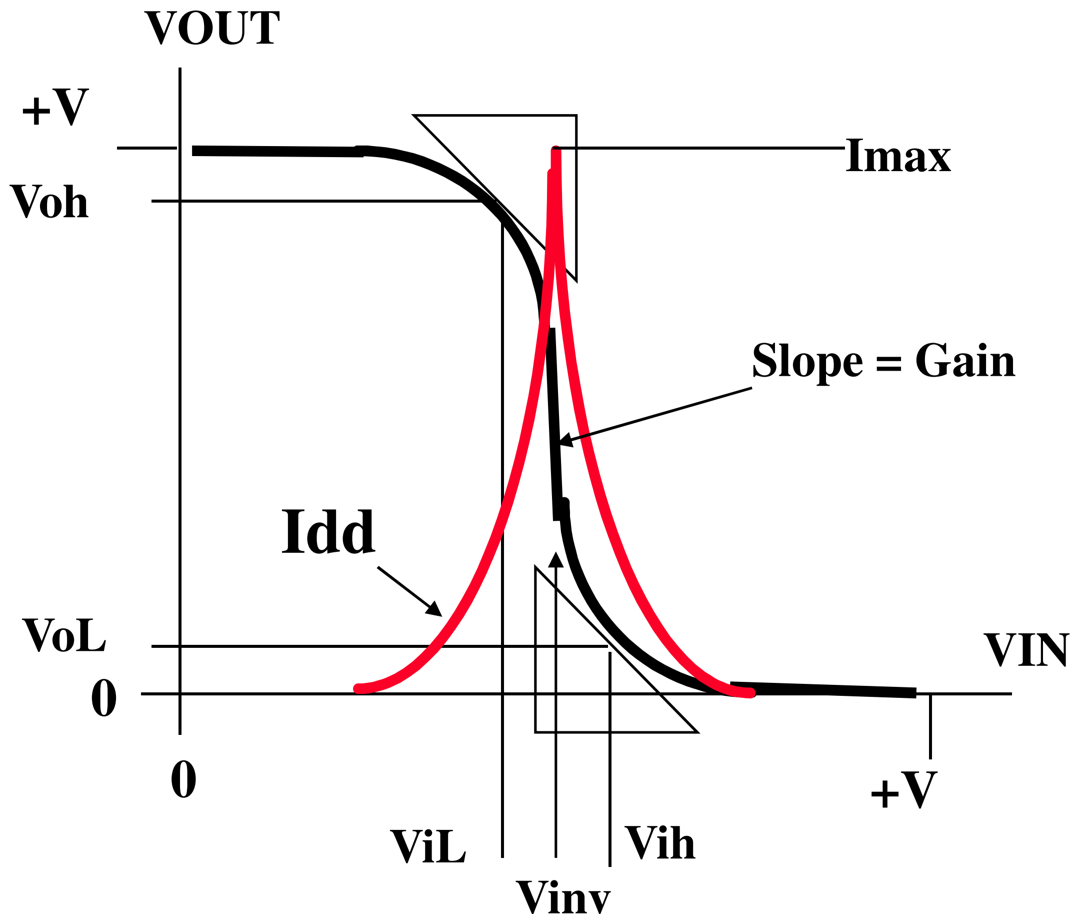
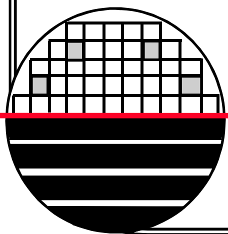
INVERTERS









Δ0 noise margin=ViL-VoL
Δ1 noise margin=VoH-ViH

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CMOS INVERTER VOUT VS VIN

CMOS INVERTER

VS2P: 5.0000, 4.0000, 3.0000, 2.0000, 1.0000, 0.0000

IF1P: 0.6000m, 0.4000m, 0.2000m, 0.0000

VS1P: 0.000, 1.000, 2.000, 3.000, 4.000, 5.000

Conditions:

Con: SMU1
Val: 5.0000 V

Con: SMU2
Val: 0.0000 A

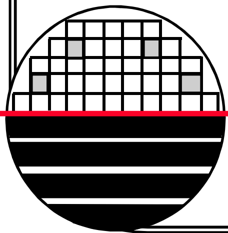
Con: SMU4
Val: 0.0000 V

Swp: SMU3
Start: 0.0000 V
Stop: 5.0000 V
Step: 0.0500 V
Pts: 101

Fit #1:	Fit #2:
None	None
****	****
****	****
***	***

Cursors	X	Y
□	2.6500	3.1079
◇	2.4500	4.5320
○	2.7500	0.4641m
⧗	2.9000	0.4350
⋈	2.7000	2.0320
△		

ICS 15:47:02
10/16/2006

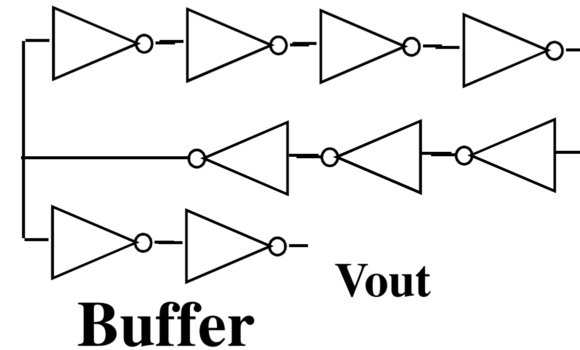


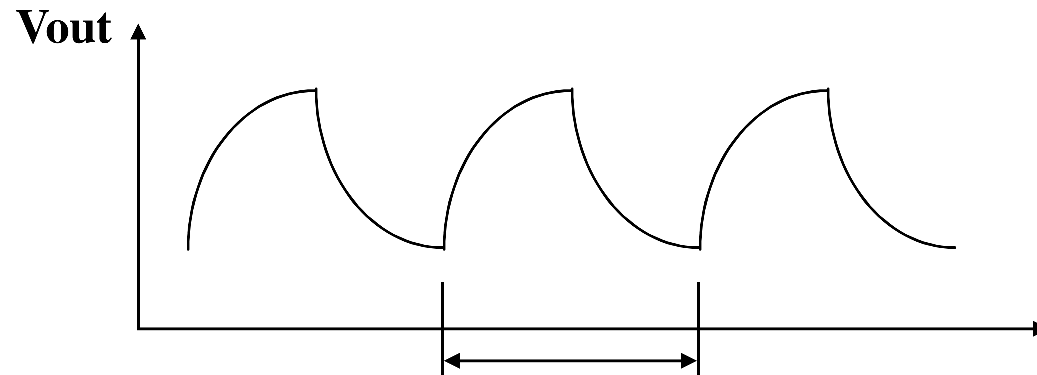
RING OSCILLATOR, td

Seven stage ring oscillator with two output buffers

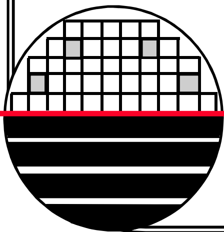
td = T / 2 N

td = gate delay
N = number of stages
T = period of oscillation





T = period of oscillation



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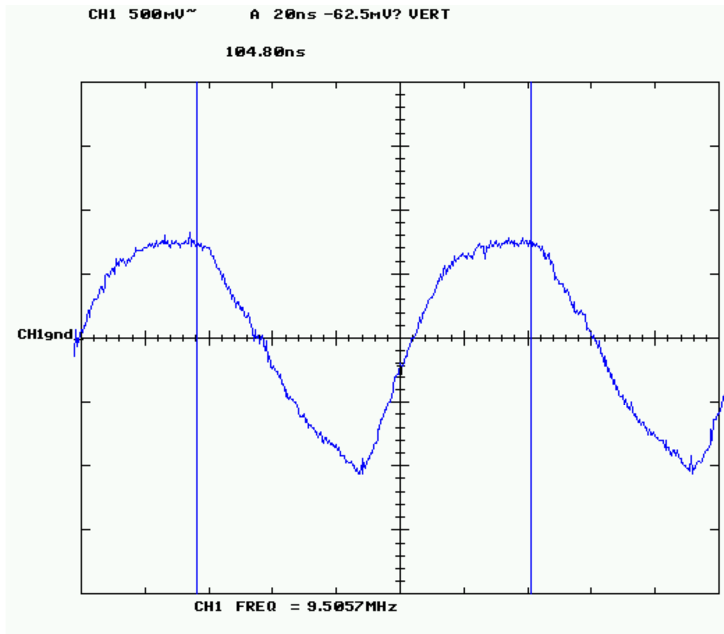
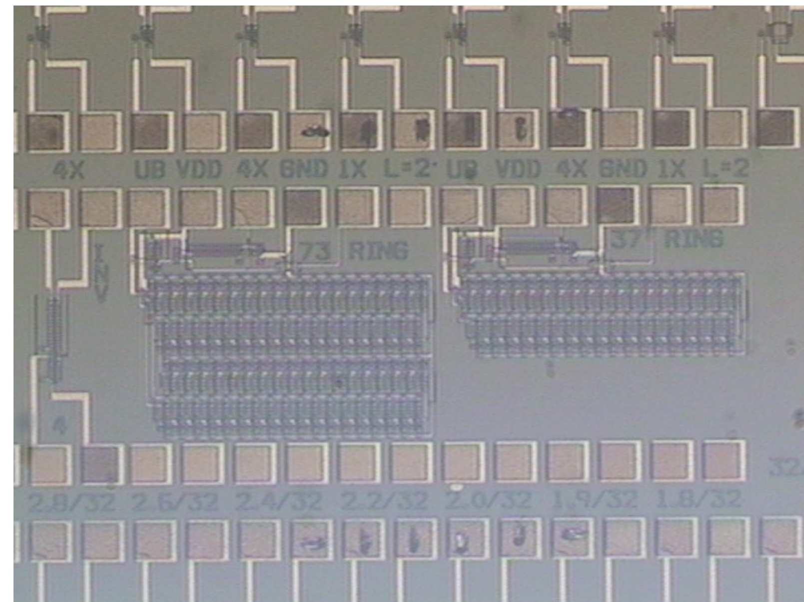
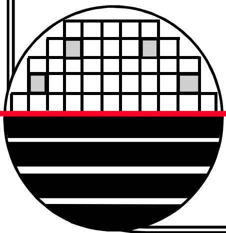
RING OSCILLATOR MEASUREMENTS



73 Stage Ring at 5V, td = 0.712ns





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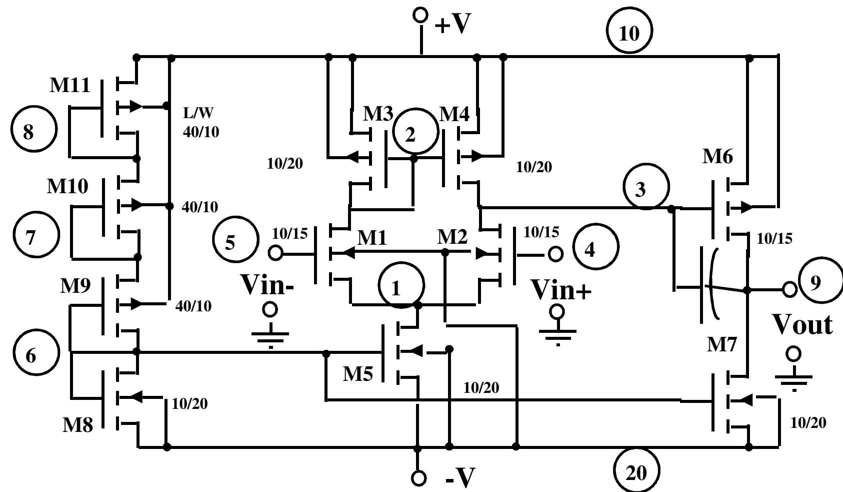
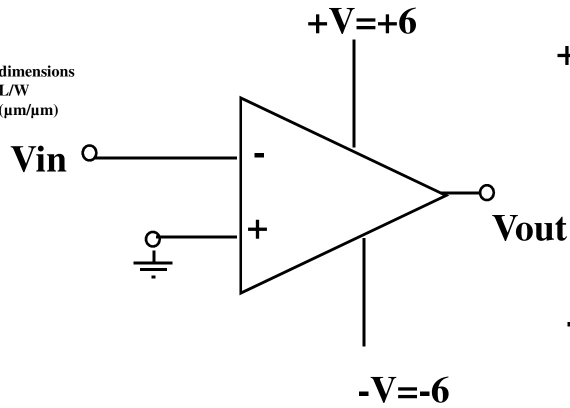
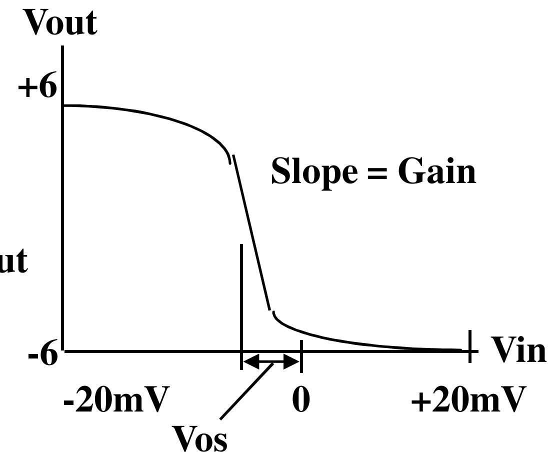
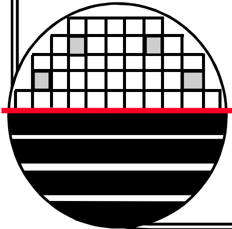
OPERATIONAL AMPLIFIER



dimensions
L/W
(μm/μm)







Rochester Institute of Technology
Microelectronic Engineering

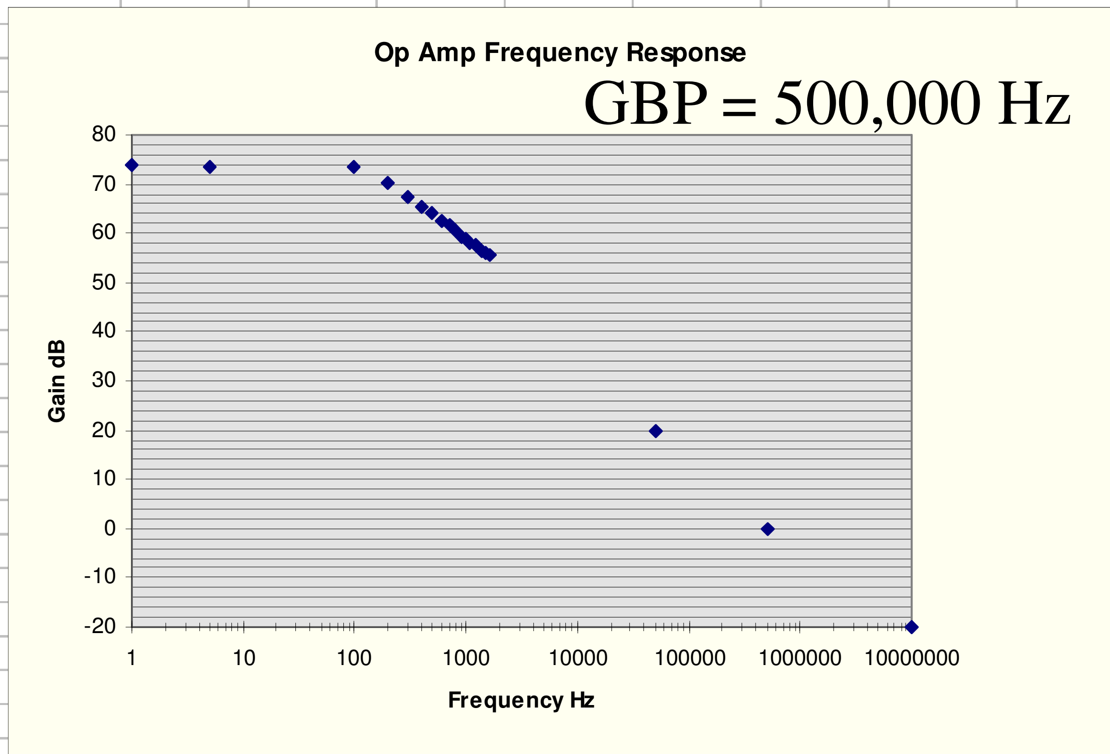
Set up the HP 4145 to sweep the Vin from -20 mV to +20 mV in 0.001V steps. Measure Gain and Input offset voltage.

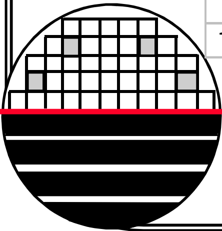
AC TEST RESULTS

ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING — LFF OPAMP.XLS FILE3B

LOT F960319 OPAMP TEST RESULTS - 1-29-97

Frequency	Gain	Vout	Vin
hZ	dB	V	mV
1	73.9794	10	2
5	73.53387	9.5	2
100	73.33036	9.28	2
200	70.31748	6.56	2
300	67.53154	4.76	2
400	65.48316	3.76	2
500	63.97314	3.16	2
600	62.41148	2.64	2
700	61.51094	2.38	2
800	60.34067	2.08	2
900	59.46256	1.88	2
1000	58.68997	1.72	2
1100	58.0618	1.6	2
1200	57.50123	1.5	2
1300	57.14665	1.44	2
1400	56.5215	1.34	2
1500	56.1236	1.28	2
1600	55.56303	1.2	2
50000	20	0.02	2
500000	0	0.002	2
10000000	-20	0.0002	2





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OPERATIONAL AMPLIFIER

OP Amp

VVO

8.0000
6.0000
4.0000
2.0000
0.0000
-2.0000

-1.500 -1.250 -1.000 -0.750 -0.500

VN

Conditions:

Con: SMU1
Val: 6.0000 V

Swp: SMU3
Start: -1.5000 V
Stop: -0.5000 V
Step: 1.0000m V
Pts: 1001

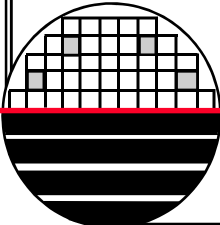
Con: SMU2
Val: -6.0000 V

Con: SMU4
Val: 0.0000 A

Fit #1:	Fit #2:
Type: Linear	None
Slp:-4.5393K	0****
Y-int:-5.3212K	****
X-int:-1.1722	***

Cursors:	X	Y
□	-1.1720	-1.0640
◇	-1.1730	3.4750
○		
⧖		

Vos =-1.72 volts
Av = 2410



TE04

```
   3/09/08                        MESA                  IGMSINQ    S36801
  12:59:49           Instruction Group Inquiry          QPADEV001H   RIT

Type information.  Then Enter.
  1=Display document, 5=Display detail

  Plant  . . . . . . . . . :   RIT
  Instruction group  . .       TE04                  WAFER MAP OF VT
    Revision . . . . . . .     ____

  Opt  Subgroup    Text
   _               1.0 Take data for wafer map of Vt, test all transistors
   _               (see wafermap.pps)
   _               2.0 Compute +/- 10%, 20%, 30%, 40% of target:
   _                     CMOS Targets are +/-1.0
   _                     Record data row by row, each character in a row
   _                     represents a different column (die), the value will be
   _                     5 if within 10% of target
   _                     4 if between -30% and -10% of target
   _                     6 if between +10% and +30% of target
   _                     3 if between -50% and -30% of target, etc.
                                                                         Bottom
 F3=Exit    F4=Prompt    F5=Refresh    F10=View 2    F12=Cancel
```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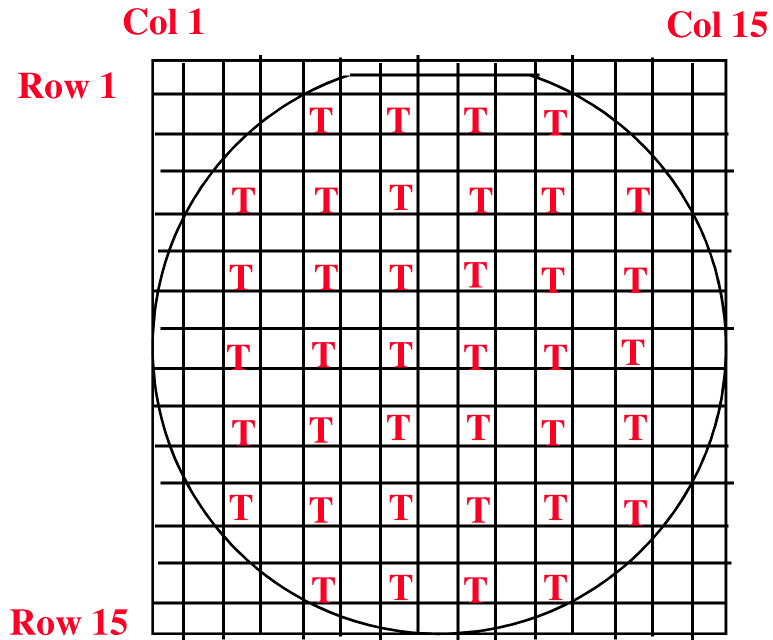
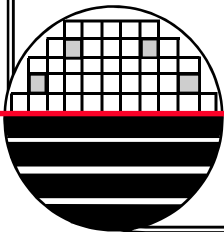
WAFER MAPS FOR MESA

nmos Vt target +1
000000000000000
000050505050000
000000000000000
005060507050700
000000000000000
004040304030300
000000000000000
004040404040400
000000000000000
004050405090600
000000000000000
005050606060700
000000000000000
000050505050000
000000000000000



row 1 is the first row in which a full die is located
column 1 is the first column in which a full die is located



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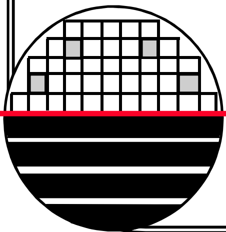
WAFER MAPS FOR MESA

Code	
0	no die
1	value<(Target-70%)
2	(Target-70%)<value<(Target-50%)
3	(Target-50%)<value<(Target-30%)
4	(Target-30%)<value<(Target-10%)
5	(Target-10%)<value<(Target+10%)
6	(Target+10%)<value<(Target+30%)
7	(Target+30%)<value<(Target+50%)
8	(Target+50%)<value<(Target+70%)
9	(Target+70%)<value



WAFER MAP

Wafer Map Generator

Robert Manley, April 6, 2007

Die #	Enter Value
2	41.5743
3	45.3252
4	50.3482
7	41.5575
8	45.329
9	45.3527
10	50.3377
11	47.8361
13	42.7587
14	41.551
15	45.3116
16	47.8679
17	47.7949
18	49.103
19	51.5933
20	42.7823
21	42.7843
22	44.0555
23	47.8541
24	46.5718
25	47.8439
26	52.8681
27	42.8304
28	44.065
29	45.3343
30	49.1166
31	46.5419
32	50.3617
33	51.5929
35	45.3247
36	47.8316
37	47.8832
38	51.5937
39	50.3843
42	47.8326
43	49.0811

Map Physical Layout

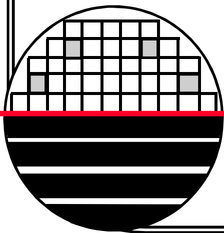
	1	2	3	4	5	6	7
1			2	3	4		
2		7	8	9	10	11	
3	13	14	15	16	17	18	19
4	20	21	22	23	24	25	26
5	27	28	29	30	31	32	33
6		35	36	37	38	39	
7			42	43	44		

Max	52.8681
Min	41.551
Range	11.3171
# Inc.	11
Inc. Size	1.02883

Wafer Flat

Range		
52.87	to	51.84
51.84	to	50.81
50.81	to	49.78
49.78	to	48.75
48.75	to	47.72
47.72	to	46.70
46.70	to	45.67
45.67	to	44.64
44.64	to	43.61
43.61	to	42.58
42.58	to	41.55

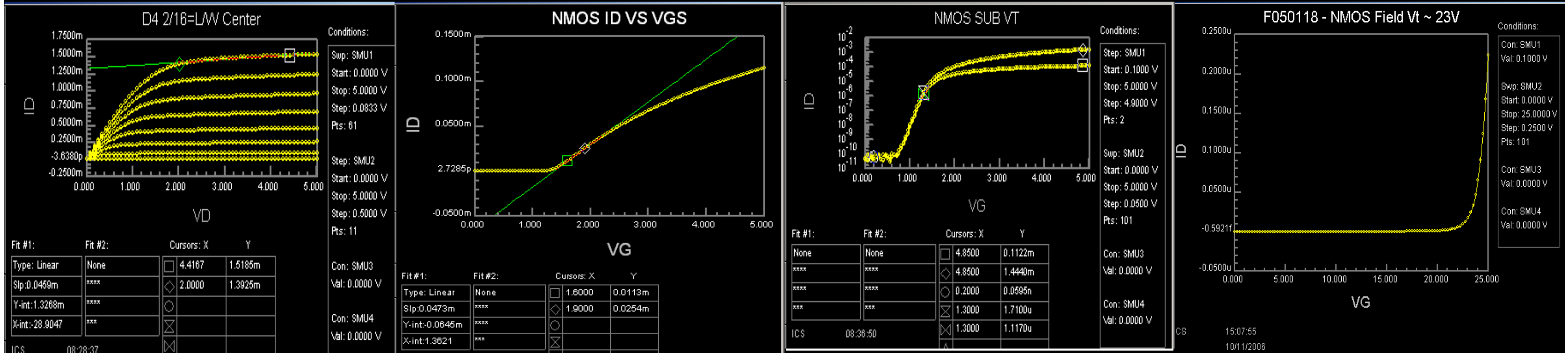
Example: Given a wafer with test chips located as shown and nmos threshold voltage data encoded and stored in MESA as shown. Reconstruct a wafer map using EXCELL spreadsheet.



MOSFET IV CHARACTERISTICS

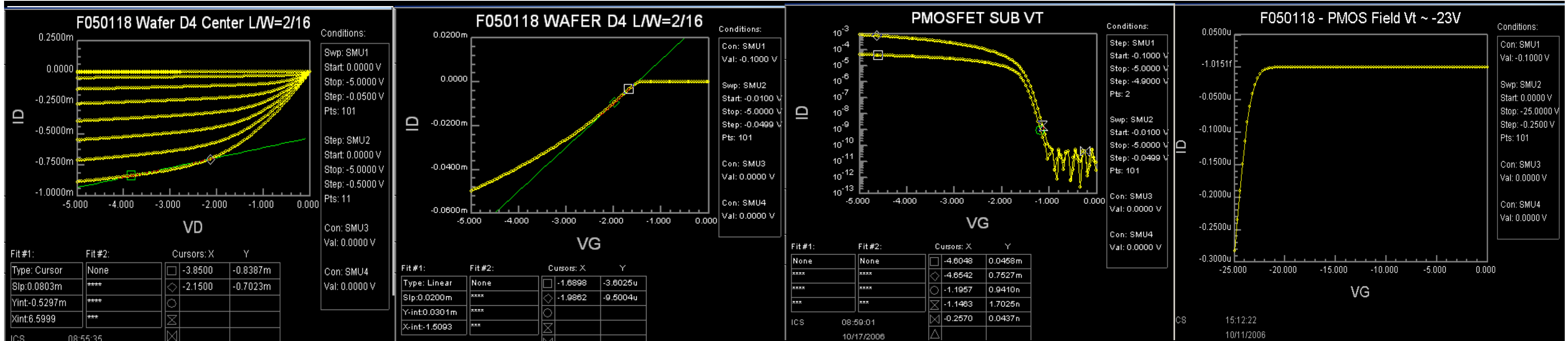
Lot Number = F050118	Wafer Number = D4	Date = 11-17-2006
Process = SMFL CMOS	Product = DAC03	

NMOS L/W = 2/16



NFAM NVT NSUB NFIELD

PMOS L/W = 2/16



PFAM PVT PSUB PFIELD

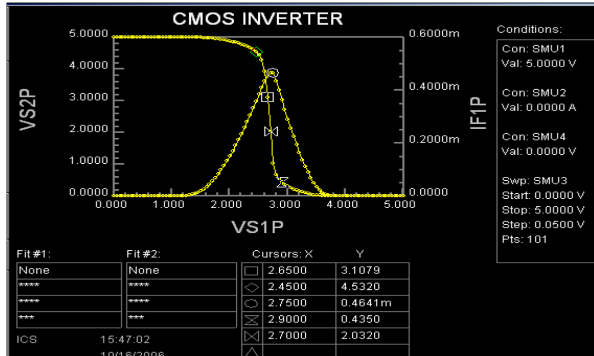
MOSFET EXTRACTED PARAMETERS

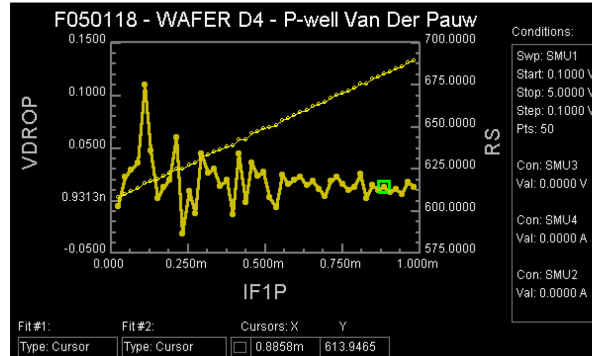
Lot Number = F050118 – Wafer Number = D4, Die Location R= , C=

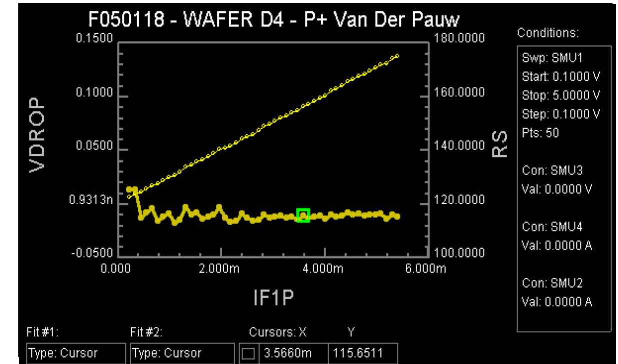
	PMOS	NMOS	Units
Mask Length / Width	**2/16**	**2/16**	**µm**
VT	**-1.51**	**1.36**	**V**
Lambda (for Vgs = Vdd)	**0.115**	**0.0417**	V^{-1}
Max gm / mm of channel width	**21.3**	**31.3**	**S/mm**
Idrive	**54.4**	**93.8**	**µA/µm**
Ion/Ioff @ Vd = 0.1V	**6**	**5**	**Decades**
Ion/Ioff @ Vd = 5V	**7**	**6**	**Decades**
Ioff @ Vd = 0.1V	**5.9e-11**	**5.0e-10**	**A/µm**
Ioff @ Vd = 5V	**5.9e-11**	**5.0e-10**	**A/µm**
Sub-Vt Slope @ Vd = 0.1V	**90**	**190**	**mV/Dec**
Sub-Vt Slope @ Vd = 5 V	**90**	**190**	**mV/Dec**
DIBL@1nA/µm $=\Delta V_g/\Delta V_d$	**0**	**0**	**mV/V**
Field VT	**-23**	**23**	**V**

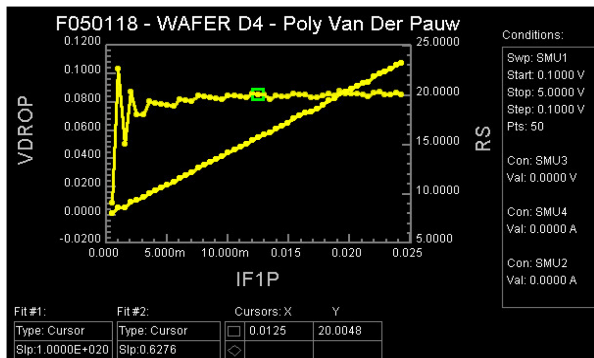
INVERTERS, VAN DER PAUW AND CBKR

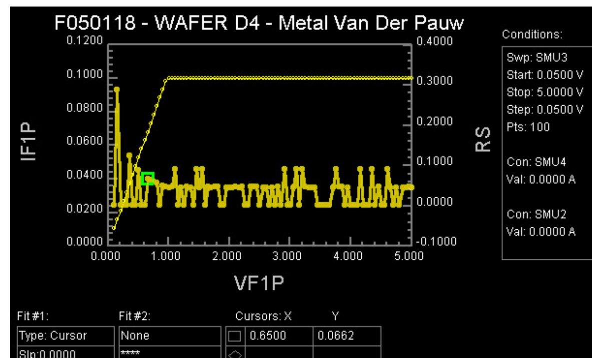
Lot Number = F050118 – Wafer Number = D4 , Die Location R= , C=

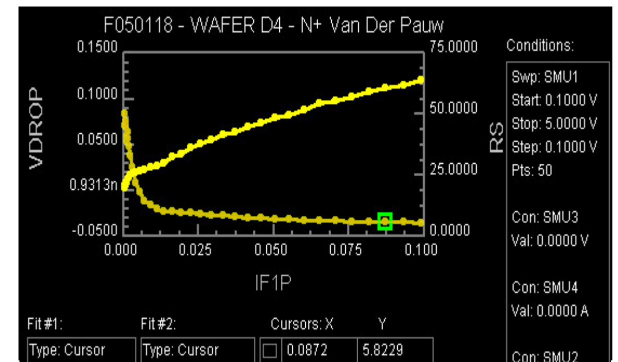


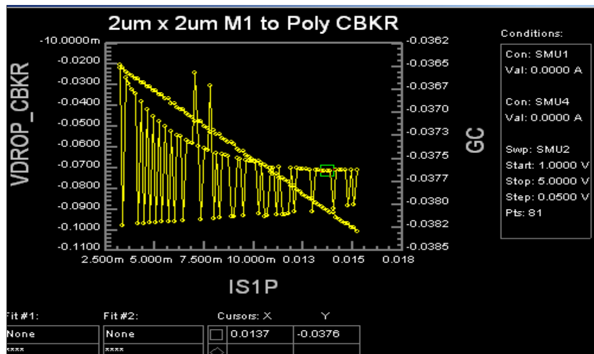


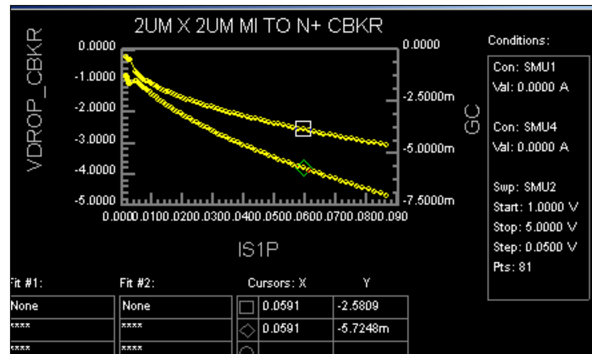


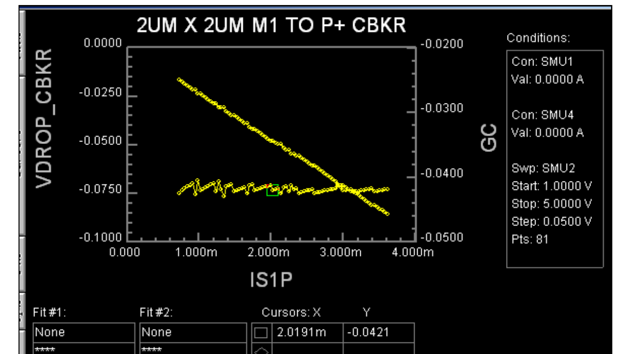












EXTRACTED PARAMETERS FROM INVERTERS, VAN DER PAUW AND CBKR

Lot Number = F050118 – Wafer Number = D4 , Die Location R= , C=

Contact Gs	CBKR	
P+	42	mmho/μm²
N+	8	mmho/μm²
poly	37	mmho/μm²

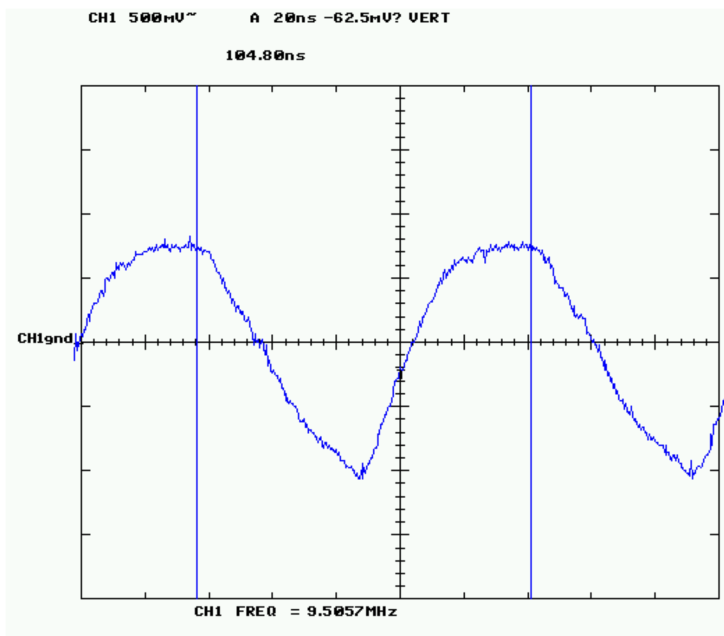
	Ring Oscillator	Vdd=5 V
# Stages	73	
Period	104	nsec
td	0.712	nsec

Rhos	Van der Pauw	
P+	115	Ohms
N+	5.8	Ohms
well	614	Ohms
Poly	20.0	Ohms
Al	0.0662	Ohms

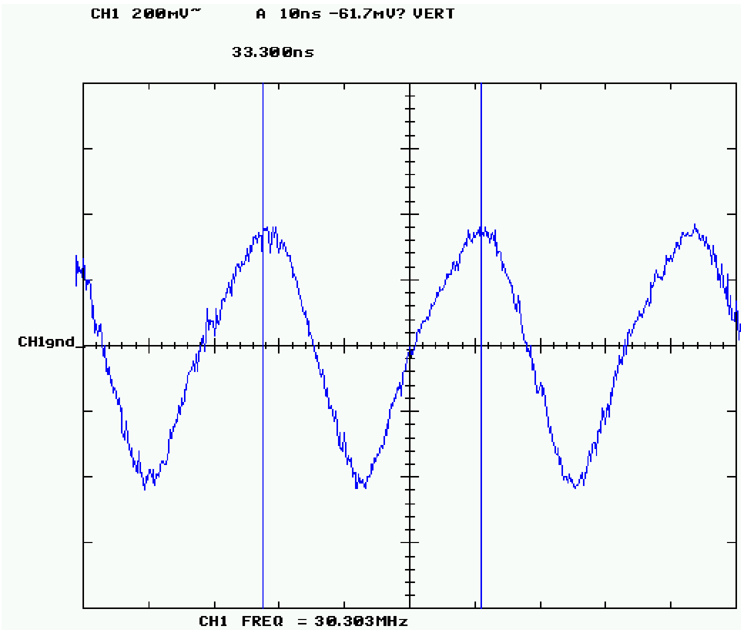
	Inverter	
VinL	2.4	V
VinH	3	V
VoL	0.4	V
VoH	4.5	V
Vinv	2.6	V
Imax	4.5	mA
Gain	-21.5	
Δ0=ViL-VoL	2.0	V
Δ1=VoH-ViH	1.5	V

	OpAmp	
Gain	None	
Offset	None	mVolts
GBW	None	Hz

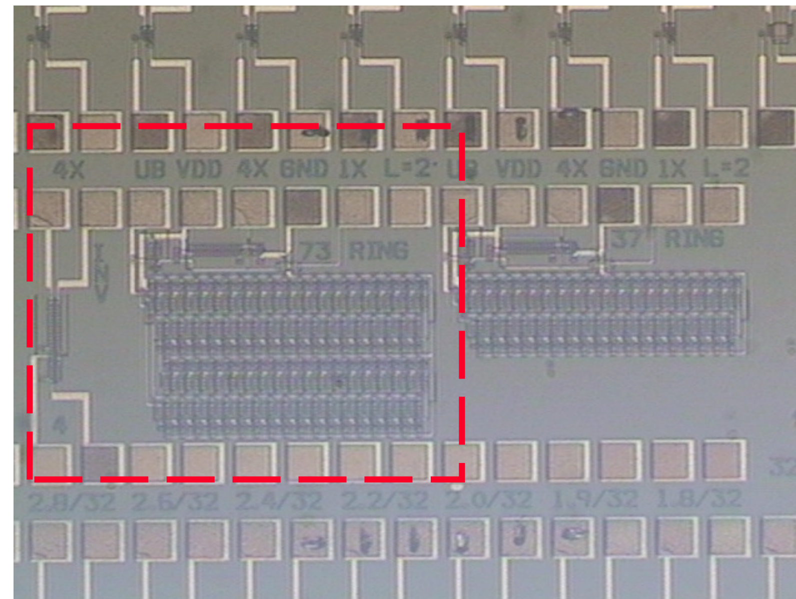
	VIA CHAIN	
M1-P+	None	ohms
M1-M2	None	ohms



73 Stage Ring at 5V, td = 0.712ns

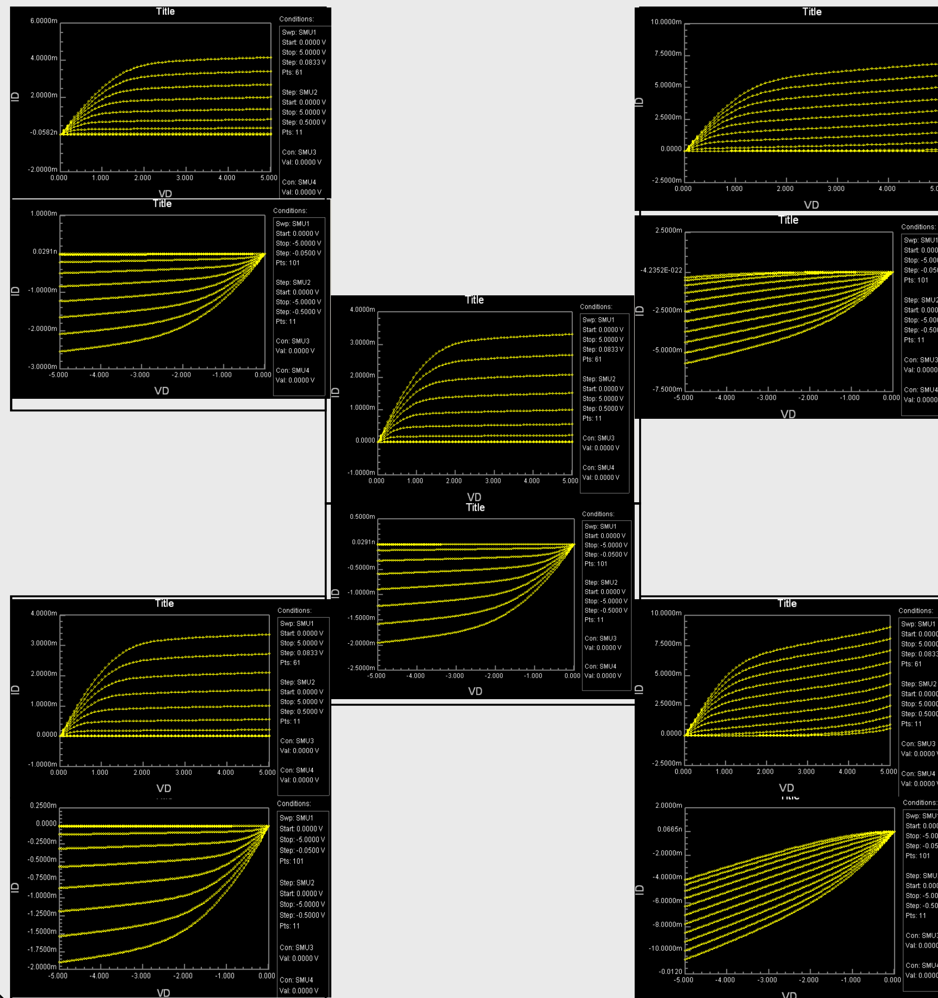


73 Stage Ring at 6V, td = 0.228ns



Lot Number = F050118
Wafer Number = D4

Family of curves for L=2μm MOSFETs



2μm/32μm L/W NMOS AND PMOS

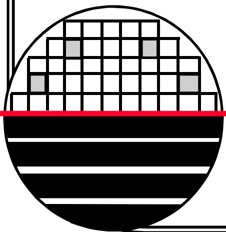
RESULTS

A test specification has been developed

- Sheet Resistance of Poly, Metal, P+ DS, N+ DS, Well
- Transistor Vt, gm, sub threshold slope, Lambda, field Vt
- ICs, inverter, ring oscillator, opamp

A history/data base has been built

Analog parametric tests for some devices has been developed (much more to do)



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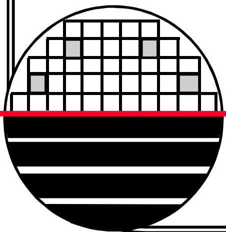
FUTURE WORK

More Automation
Improved Wafer Mapping
More Complete Testing
Improved Analog Testing
Improved Digital Testing



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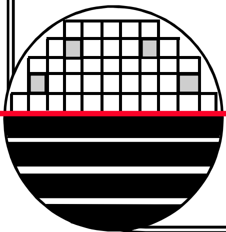
CONCLUSION

Testing is very time consuming. It takes us 9 hours to do all the specified tests and even then we only test a few devices on a wafer.

Currently we test about 1% of the devices



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HOMEWORK – CMOS TEST

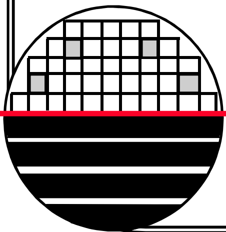
1. How is Lambda, Vt and gm found from the transistor family of curves? Show example calculations.

2. How are Vt and gm found from the Id-Vgs plot?

3. Explain how sub threshold swing, Ion/Ioff, and DIBL are found. Show example calculations and correct units of measure.

4. What is the significance of inverter noise margin.

5. What is the purpose of the ring oscillator test structure.



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