RIT Factory CMOS Electrical Test

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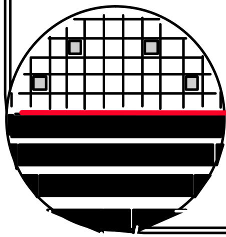

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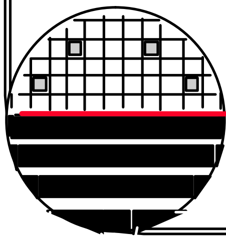
INTRODUCTION

- **Motivation**
  - **Most students taking Factory class are not yet familiar with the test equipment used in the test lab.**
- **Goal**
  - **Create a PowerPoint Manual, and electrical tests, so that most people will be able to easily perform the electrical tests, and extract the necessary data.**
- **Assumptions**
  - **Operator has a base knowledge of:**

    1) The electrical tests being done

    2) How to extract necessary information from the generated curves.



TEST EQUIPMENT

Automatic Prober

Semi-automatic Prober

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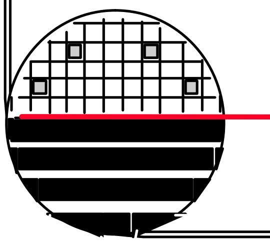
TEST EQUIPMENT

Manual Prober



TEST STATION

Light Source

CCD Camera

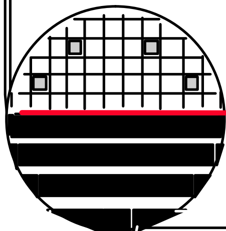
PC Interface

Switch Matrix

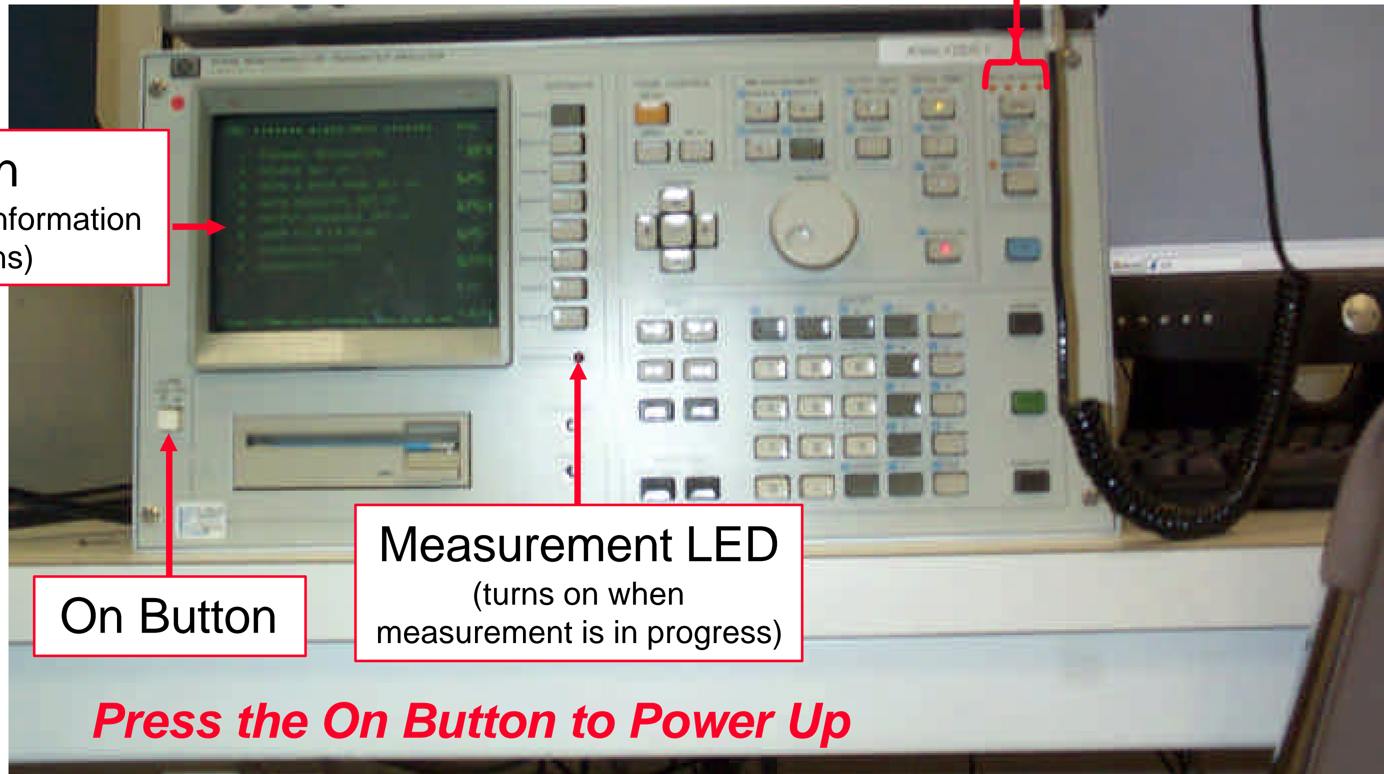
Microscope

HP4145 tester

Semi-Auto Probe Station



HP4145 – PRESS THE ON BUTTON TO POWER UP



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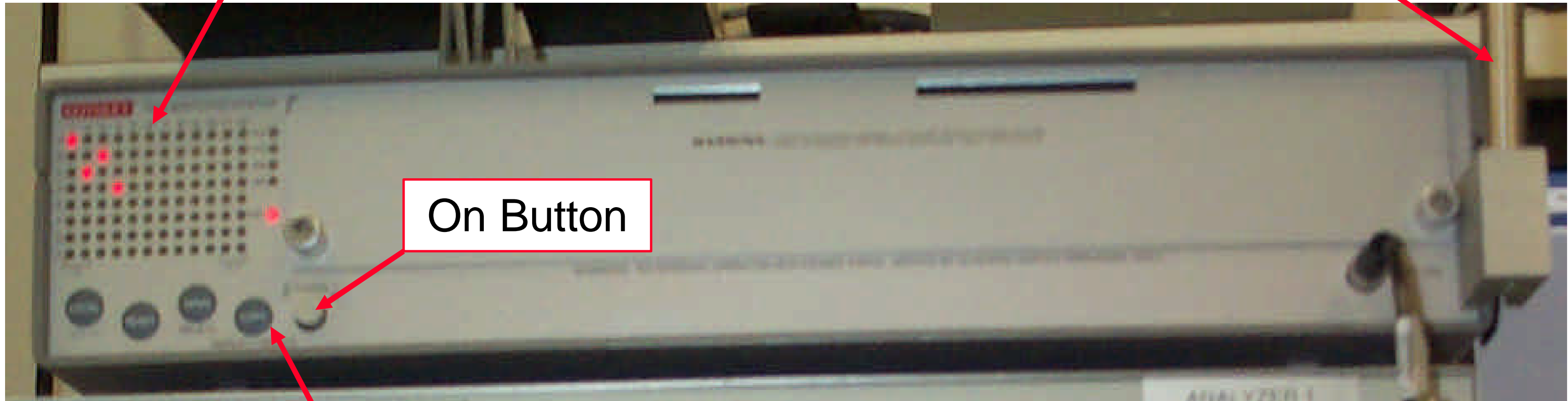
SWITCH MATRIX - PRESS THE ON BUTTON TO POWER UP

Switch Matrix Indicator

Light Pen



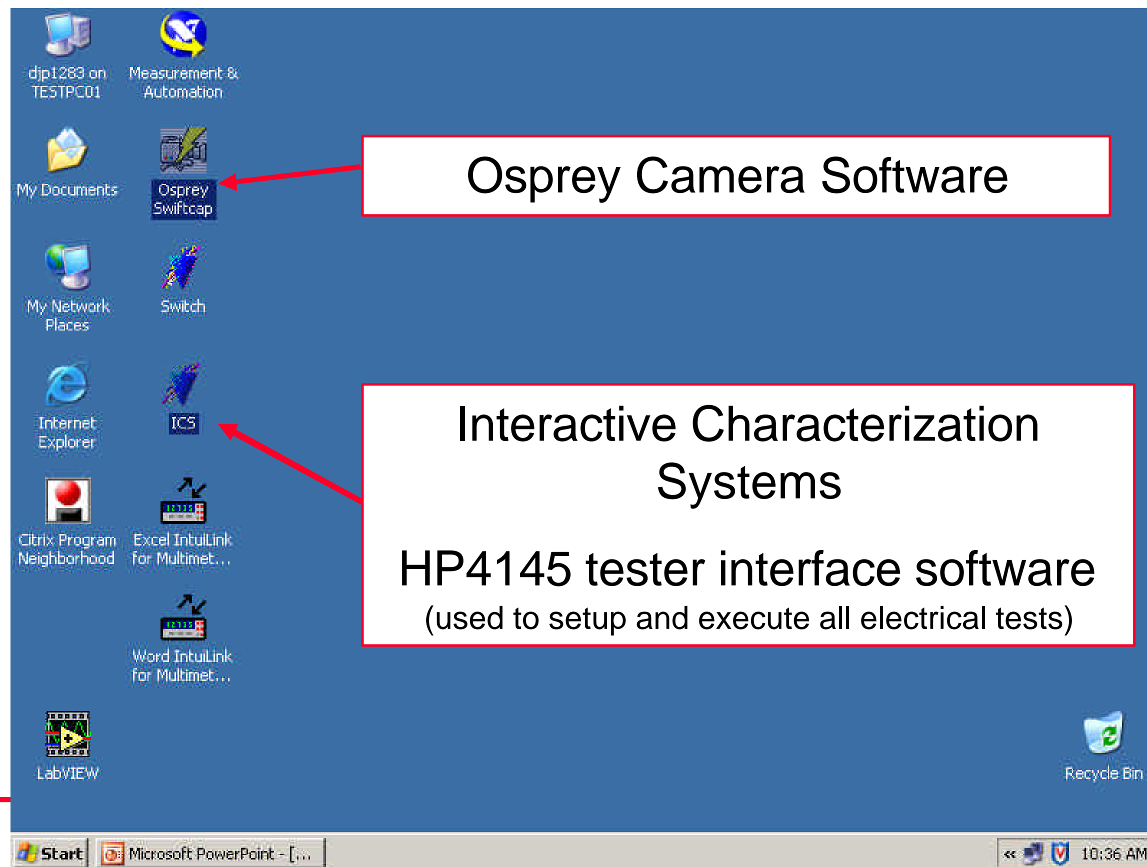
On Button

Copy Button

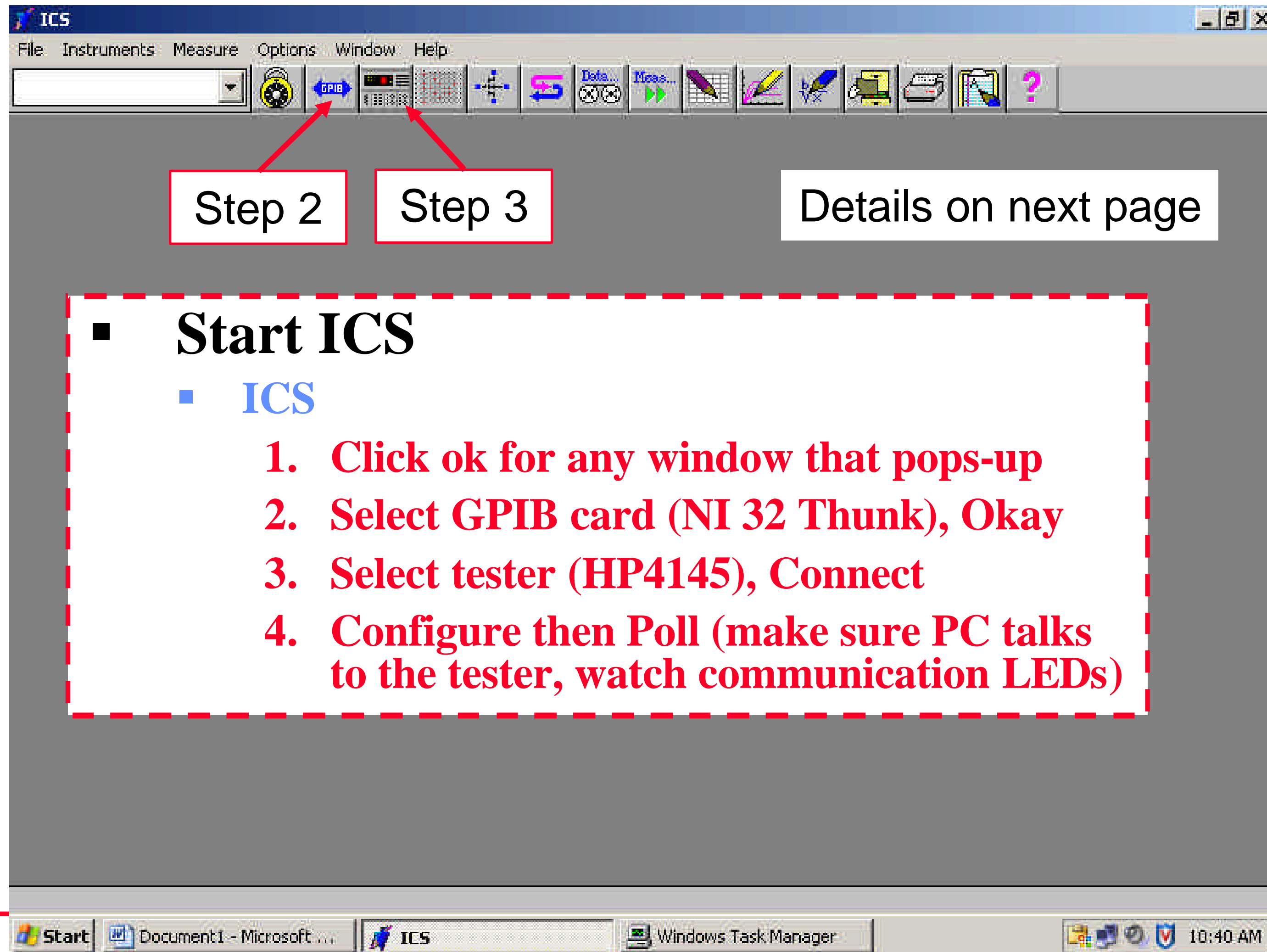
Press the On Button to Power Up

PC DESKTOP

- Log onto PC, locate the two icons shown below, Double click on ICS icon



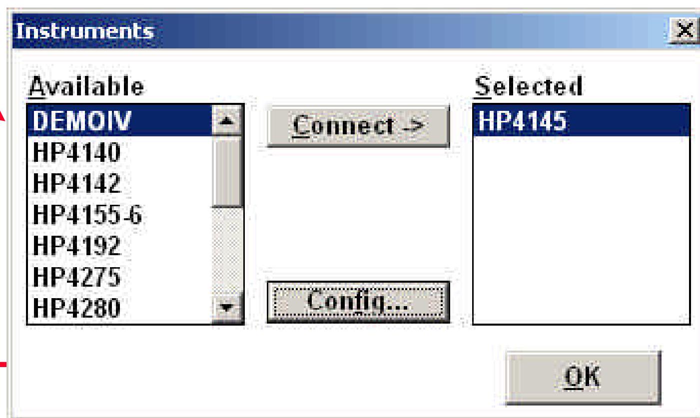
ICS SETUP



- **Start ICS**
  - ICS
    1. Click ok for any window that pops-up
    2. Select GPIB card (NI 32 Thunk), Okay
    3. Select tester (HP4145), Connect
    4. Configure then Poll (make sure PC talks to the tester, watch communication LEDs)

ICS SETUP DETAILS

- **ICS Setup**
  1. Select GPIB card (NI 32 Thunk)
  2. Select tester (HP41545)
  3. click Config… button on the Instruments window then Poll



ICS LOAD ELECTRICAL TESTS

ICS
File Instruments Measure Options Window Help
NFAM

- Load electrical tests
  1. Download ICS_Test_Setups.dat file from Dr. Fuller's webpage: http://www.rit.edu/~lffeee/labnotes.htm
  2. Right Click, Save As, Save to desktop Location highest level, then [docume~1], then [your username], then [desktop]
  3. In ICS Click File → Import
  4. Navigate to the desktop C:/documn~1/username/desktop
  5. Open "FAC_SUB.dat"

PSUB-1 NSUB NSUB-1
CBKRPOLY CBKRPOLY-1 CBKRP CBKRP-1 PSUB
NFIELD-1 PFIELD PFIELD-1 VDP_MET VDP_MET-1
CBKRN CBKRN-1 INV INV-1 NFIELD
NVT-1 PVT PVT-1 VDP VDP-1
NFAM NFAM-1 PFAM PFAM-1 NVT

Start ICS 9:52 AM

LIST OF ELECTRICAL TESTS

Test Name	Description	Parameters to be extracted	Units
VDP-POLY	Poly Van Der Pauw	Poly Sheet Resistance	ohms/square
VDP-MET	Metal Van Der Pauw	Metal Sheet Resistance	ohms/square
VDP-N	N+ Van Der Pauw	N+ Sheet Resistance	ohms/square
VDP-P	P+ Van Der Pauw	P+ Sheet Resistance	ohms/square
VDP-PWELL	P-well Van Der Pauw	P-Well Sheet Resistance	ohms/square
CBKR-N	CBKR Metal to N+ silicon	Specific Contact Conductance for metal to N+ silicon	mmho/µm2
CBKR-P	CBKR Metal to P+ silicon	Specific Contact Conductance for metal to P+ silicon	mmho/µm2
CBKR-POLY	CBKR Metal to Poly	Specific Contact Conductance for metal to Poly	mmho/µm2
NFAM	NMOS Family of Curves	Lambda	1/Volts
NVT	NMOS ID - Vgs	Max gm	mho/µm of channel width
		Vtn	Volts
NSUB	NMOS Sub Threshold ID-Vgs	Sub Threshold Slope	mV/decade
		Imax/Imin	# of decades
PFAM	PMOS Family of Curves	Lambda	1/Volts
PVT	PMOS ID - Vgs	Max gm	mho/µm of channel width
		Vtn	Volts
PSUB	PMOS Sub Threshold ID-Vgs	Sub Threshold Slope	mV/decade
		Imax/Imin	# of decades
NFIELD	NMOS Family of Curves	N Well Field Vt	Volts
PFIELD	PMOS Family of Curves	P Well Field Vt	Volts
INV	Inverter Vout versus Vin	Imax	Amps
		Vinv, Voh, Vol, Vih, Vil	Volts

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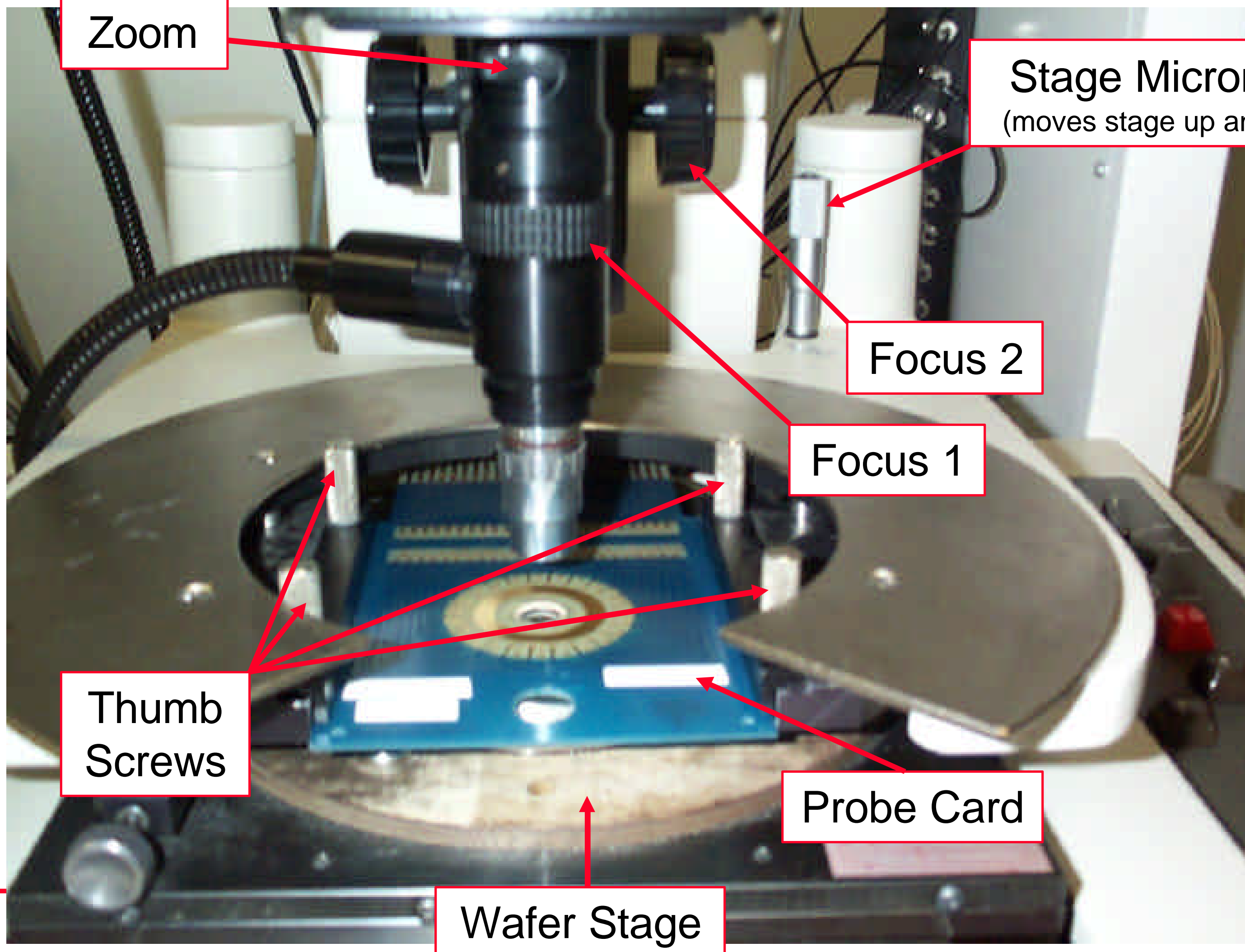
ICS – SELECTING AND RUNNING A TEST

- **Display the "Measure" window**
  1. **Click the Measure button (8th from the left)**
  2. **Use drop-down box to select a test**
     - PFAM
     - NVT
     - PVT
     - NSUB
     - PSUB
     - NFAM
     - VDP-POLY, VDP-METAL, etc.
     - CBKR-N, CBKR-P, CBKR-POLY
     - INV
     - FIELD_NMOS_VT
     - FIELD_PMOS_VT
  3. **Click the "Single" button to run the selected electrical test**

PROBE STATION – SHOULD ALWAYS BE POWERED ON



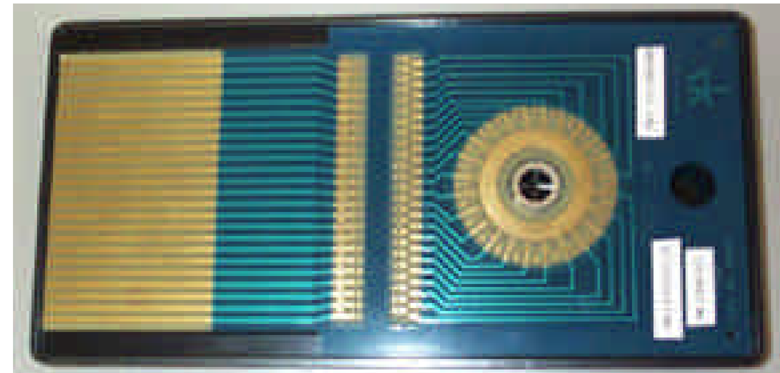
INSERTING PROBE CARD

- **Choose Probe Card**
  - There are 2 types: 1) 10 pin card, & 2) 12 pin card

    Sub-CMOS: 10 pin probe card

    DAC lots: 12 pin probe card

    Adv-CMOS: 10 pin probe card
- **Probe Card Slot**
  - Remove Probe Card (If one is in the probe station already)
    1. Twist Micrometer "up" (couple turns)
    2. Loosen 4 thumb screws
    3. Remove card
  - Insert Desired Probe Card
    1. Push card into the slot
    2. Tighten 4 thumb screws



Probe Card

PROBE STATION – SHOULD ALWAYS BE POWERED ON

Y-Axis & X-Axis indexing distances

Index/Jog toggle Switch

Index: move the stage a large distance indicated by the user .

Jogg: moves the stage a small distance.

Home & Load/Center Buttons

Probes Up/Down

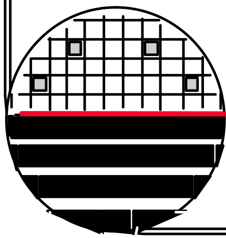
Vacuum On/Off

Thumb Screws

Wafer Stage

Probe Card

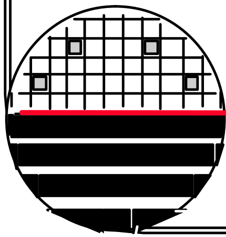
Stage Movement



LOAD WAFER

- **Move Stage to the Load Position**
  - **Press the “Load/Center” button (moves stage out)**
- **Load the Wafer**
  - **Make sure the vacuum switch is turned off**
  - **Load the wafer onto the center of the chuck**

    Wafer flat towards front of the tool
  - **Turn on the vacuum**
  - **Press the “Home” button**
  - **Wafer is loaded and ready for viewing using Osprey**



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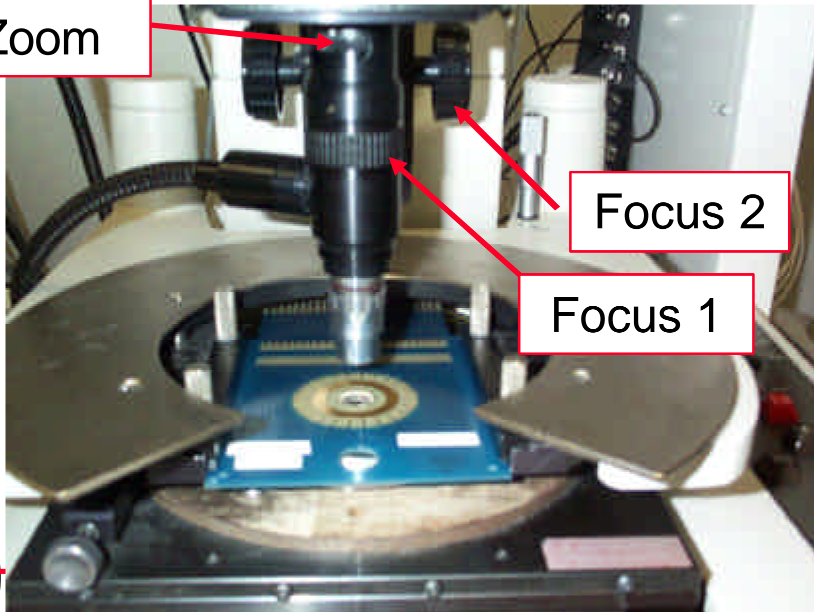
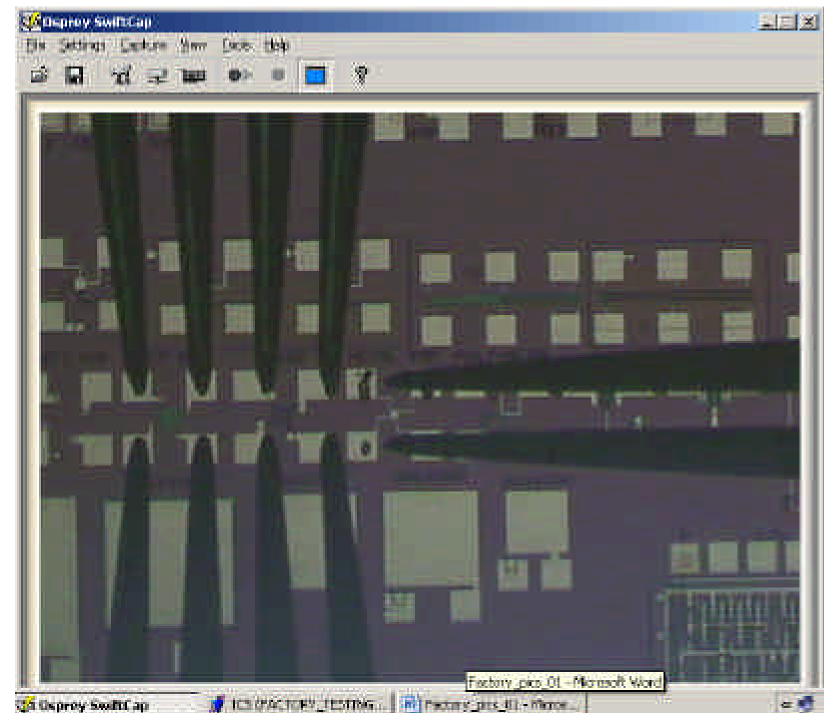
OSPREY – VIDEO IMAGING SETUP

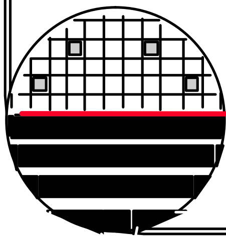
- Turn the Light on
  - Turn the dial on the light source clockwise until optimal brightness is achieved
- Start Osprey Software on your Desktop
  - Click “close” on the window that pops-up.
  - Second window is a video image of the microscope imaging.
  - Window cannot be resized but magnification (zoom) can be changed
- Adjust zoom and focus



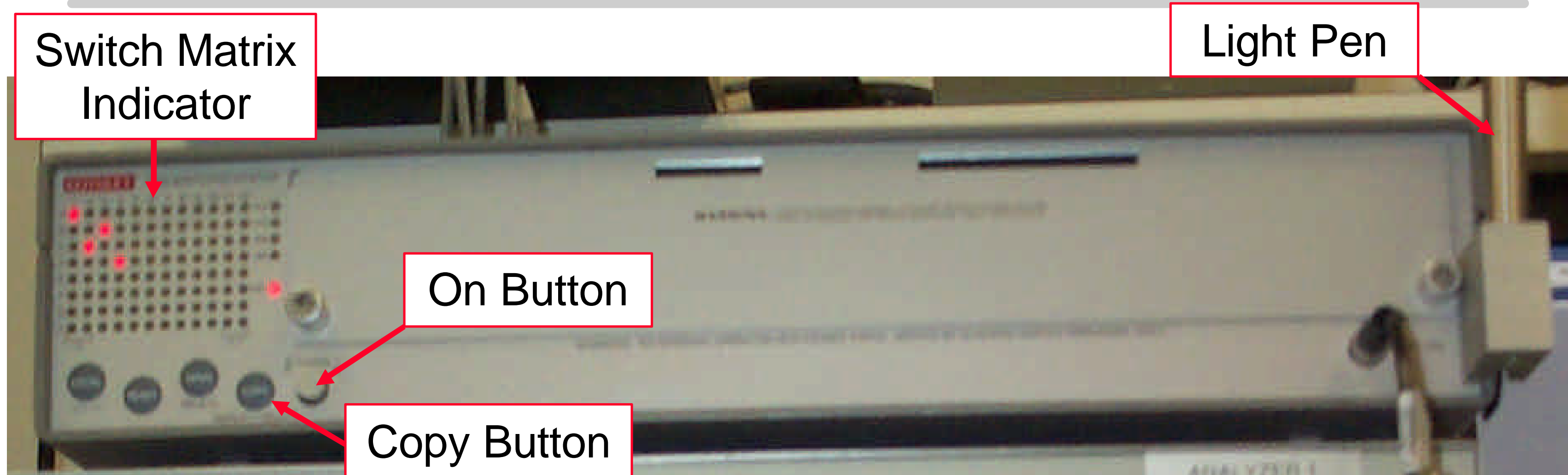


SETUP STAGE HIGHT

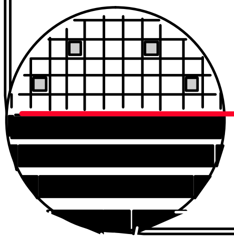
- **Maneuver probes over empty street**
  1. Set Index/Jog switch to Jog
  2. Use arrow buttons appropriately
  3. Stop when over street (empty space between die)
- **Make probes contact Aluminum in the street**
  1. Toggle Probes down (set separate/contact switch to contact)
  2. Use micrometer to move probe card down
  3. When probes slide (very small amount) stop moving micrometer
  4. Toggle probes up (separate)
  5. Move station small amount, and look for probe marks
     - Black marks where the probes scratched the aluminum
     - Marks should be small elongated dots (Ex.)
  6. Repeat As needed (move micrometer up if needed)



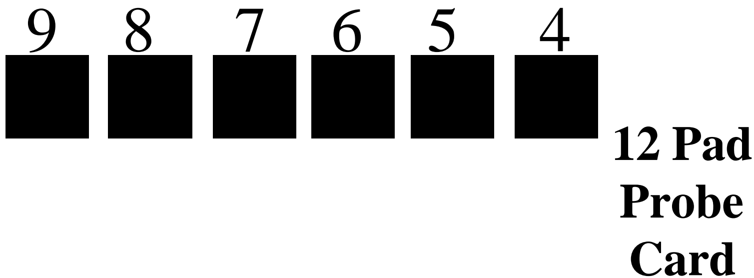
SWITCH MATRIX

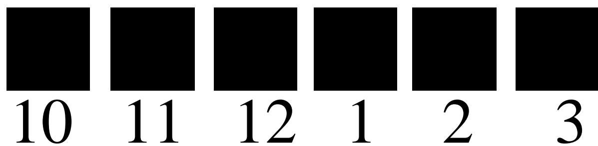


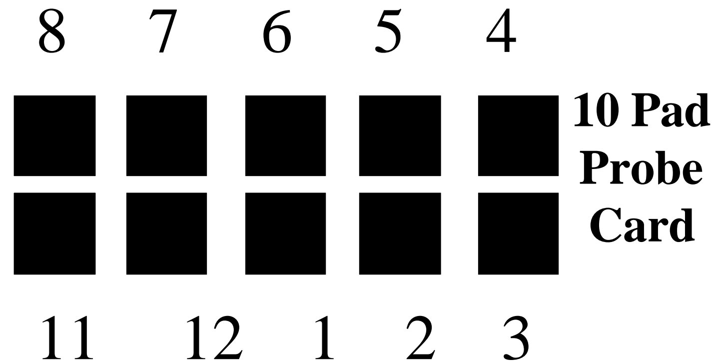
- **Turn on Switch Matrix (should be on from page 5)**
- **Use Light wand to activate different switches**
  - **Point wand at a circle on the indicator.**
  - **Push button on the light wand.**
  - **LED should toggle on and off.**
  - **Columns indicate pin number on the probe card.**
  - **Rows indicate SMU number (A = SMU 1, B = SMU 2, etc.).**
- **Push the Copy Button.**
  - **Activates the appropriate switches (LED is on) so that indicated probe pins and SMUs are connected.**
  - **Leave this button turned on.**



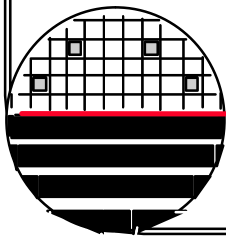
STANDARD PROBE CARDS





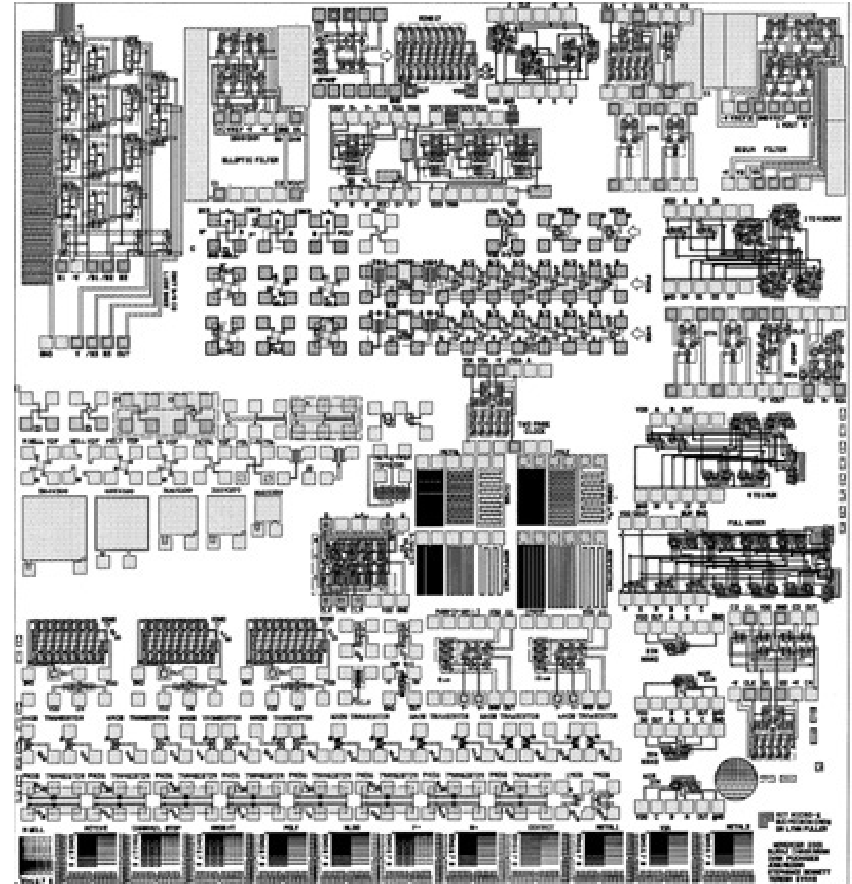


Numbers indicate switch matrix column



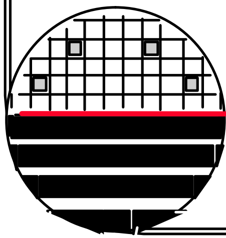
SUB-CMOS MIXED CMOS TEST CHIP

Layout of CMOS test chip for microelectronic engineering manufacturing courses. This chip has transistors down to 0.5 µm gate length, a variety of test structures, digital and analog circuit building blocks including A-to-D and D-to-A converters, operational amplifiers, transconductance amplifiers, and filters of various types.



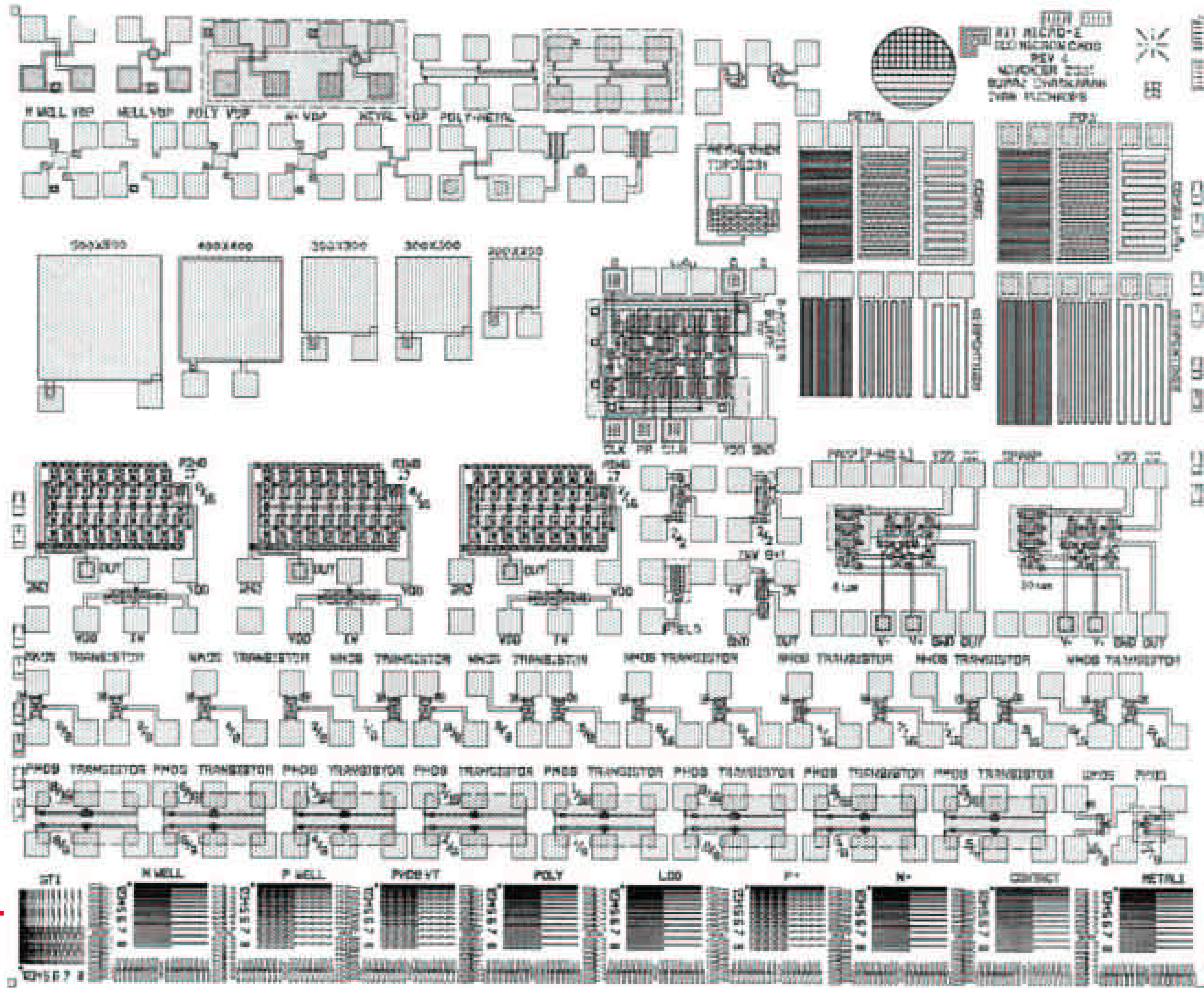
Dr. Lynn Fuller, Lisa Bonanno 2003

SUB-CMOS Die Photograph

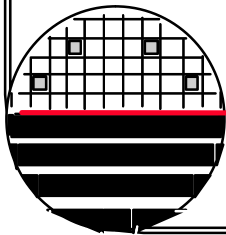


Roches
Microe

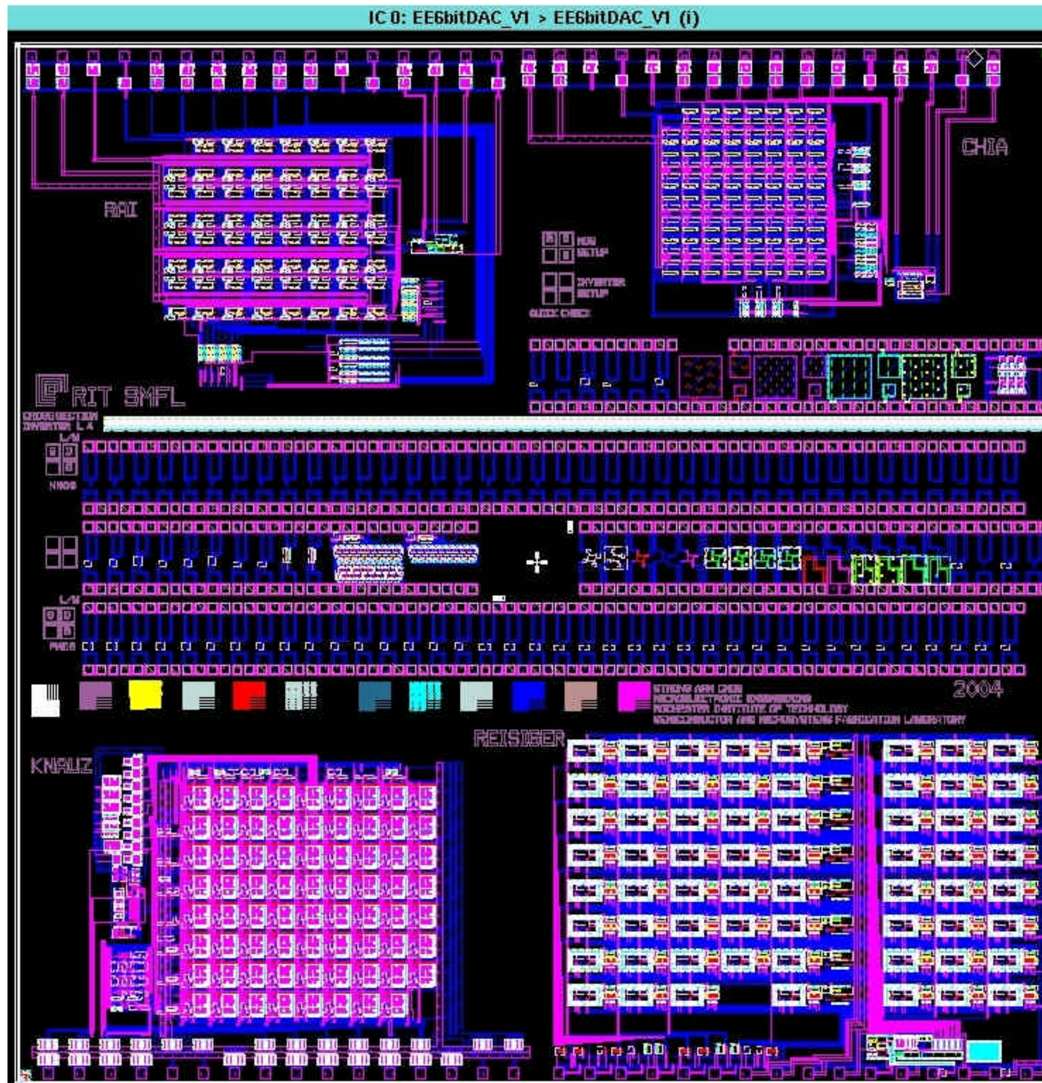
ADVANCED CMOS TEST CHIP



SPICE PARAMETRIC CMOS TEST CHIP



DAC 2003 PROJECT CHIP



GENERAL TEST INSTRUCTIONS

Test die in the center of the wafer, then upper left, upper right, lower right, and lower left (about ½ way between center and edge). Extract parameter values from the test results.

Create a PowerPoint document from **test_results.ppt** master (see example data powerpoint a few pages below) on Dr. Fullers webpage at http://www.rit.edu/~lffeee/labnotes.htm (save as) record Lot#, Wafer#, Die location (center, top left,etc), pictures of die, test results graphs, extracted parameters and comments. Email to Dr. Fuller at lffeee@rit.edu

Test 01 – Van Der Pauw and CBKR. Record Average of five tests
Test 02 – Transistors, test small transistors (L=2µm for SMFL, L=1µm for Sub-CMOS and Adv-CMOS). Record results in power point document.
Test 03 – Inverters, Ring Oscillator. Record Average of five tests.
Test 04 – NMOS VT wafer map

GENERAL TEST INSTRUCTIONS

Substrate or Well Connections: Most of the test structures incorporate diffusions. In Resistors, Van der Pauw's and Transistors the junctions between the diffusions and the substrate/wells are normally never forward biased. As a result the test engineer needs to evaluate the applied test voltages and connections to the substrate/wells and connections to the diffusions to ensure proper bias conditions.

For example: a P+ Van der Pauw in an N-type Well requires that the Well connection always have the highest positive voltage that is applied. If a separate (5th pad) connection is available (not often because there are only 4 SMU's) that can be set to a high voltage. Otherwise the substrate is normally connected to one of the four pads of the Van der Pauw. This pad can be swept with positive voltage thus keeping the substrate/well junction reverse biased.

GENERAL TEST INSTRUCTIONS

Each test requires you to:

1. Find the structure you want to test
2. Place the probes
3. Open the test by restoring the "testname"-1 (example PFAM-1) in ICS, view the test setup to see what SMU's do what.
4. Set the switch matrix for the HP4145 SMU's to the probes you are using, consistent with the test setup.
5. Edit the graph by making changes in the title, moving the cursors to the correct location
6. Copy the plot using ctrl print screen, (paste into word, copy from word to power point, crop and paste in correct location)
7. Extract the data, such as threshold voltage or LAMBDA and enter the value in the data table in the powerpoint
8. Save the powerpoint, minimize the data plot on ICS
9. When done email the powerpoint to Lynn.Fuller@rit.edu

TE01 Van Der Pauw and CBKR

```
5/04/06                          MESA                      IGMSINQ     S36801
8:31:04               Instruction Group Inquiry            QPADEV000W   RIT

Type information.  Then Enter.
  1=Display document, 5=Display detail

  Plant . . . . . . . . . :   RIT
  Instruction group . . .     SUB-CMOS-TE01        TEST COMPLETED WAFERS
    Revision . . . . . . .    150

  Opt Subgroup  Text
   _            1.0 Test Resistive Devices
   _            2.0 Test Van Der Paw for Poly, Metal, n+/p+ Diffusion, Well
   _            3.0 Cross Bridge Kelvin Structures for contact resistance
   _            4.0 Via chain yes/no test (enter yes if via chain is good)
   _            5.0 See SPC chart for PolySi Resistance(PolySRes.pps)
   _            6.0 See SPC chart for NRRHOS (NTRHOS.pps)
   _            7.0 See SPC chart for WellRes (WellRes.pps)
   _            8.0 See SPC chart for PTRHOS (PTRHOS.pps)
   _            9.0 Record Rhos(poly, metal, p+, n+, well)
   _                Gc(metal-to-poly)mhos-sq um, Gc(metal-to-p+)mhos-sq um
                                                                      Bottom
F3=Exit   F4=Prompt   F5=Refresh   F10=View 2   F12=Cancel
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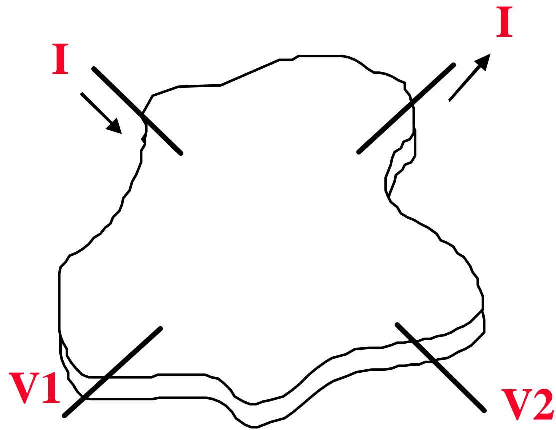
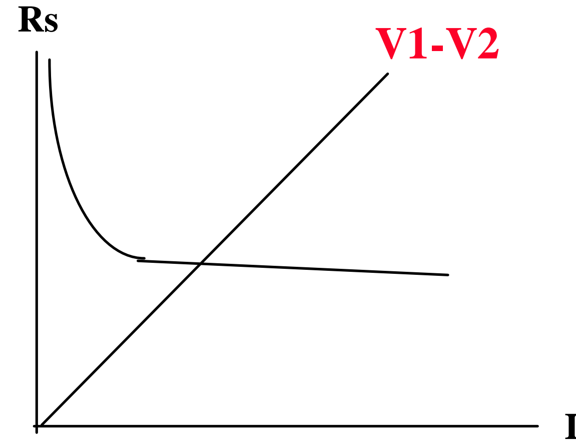
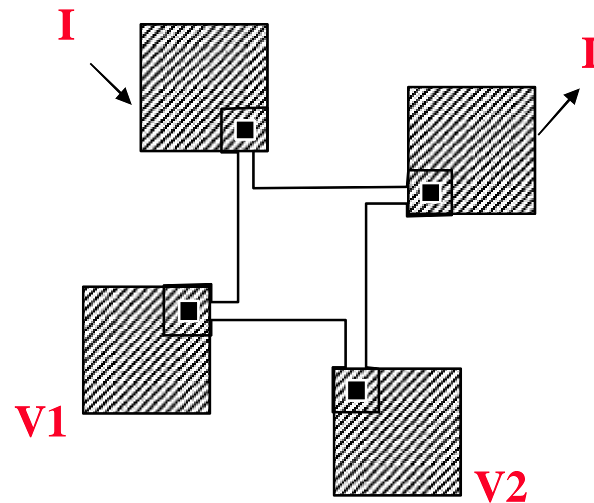
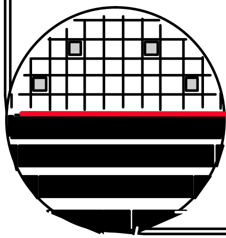
VAN DER PAUW TEST STRUCTURES FOR SHEET RESISTANCE



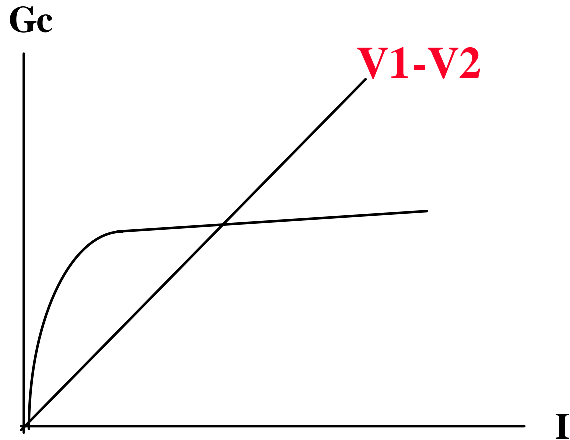


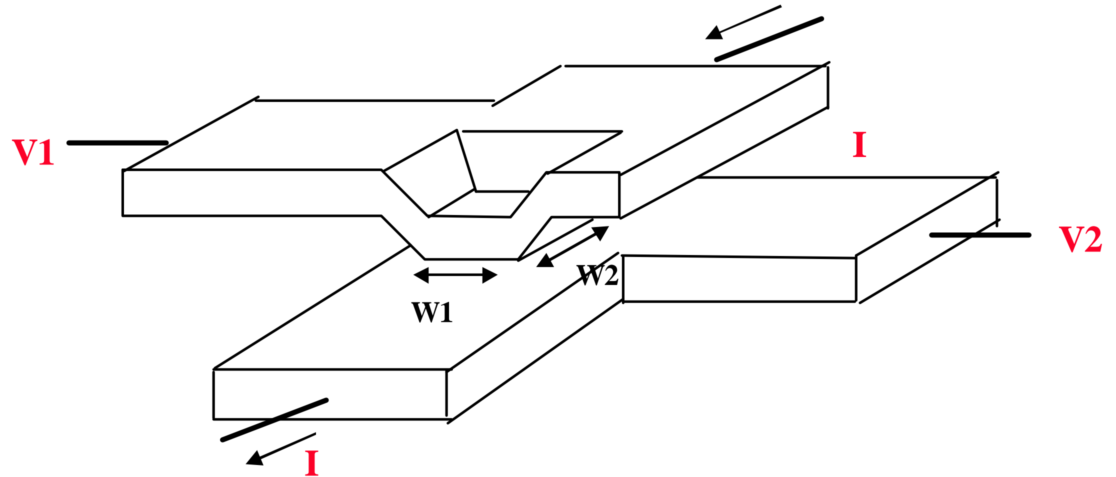
$$Rs = \frac{(V1-V2)}{I} \frac{P}{\ln 2}$$





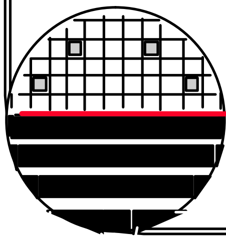
CROSS BRIDGE KELVIN RESISTANCE TEST STRUCTURES FOR CONTACT RESISTANCES





$$Rc = \frac{(V1\text{-}V2)}{I} \quad \text{ohms}$$

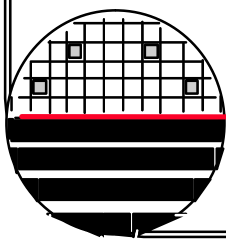
$$Gc = \frac{I}{(V1\text{-}V2)} \frac{1}{W1 \times W2} \quad \text{mhos}/\mu m^2$$



TE01 Test Structures for SUB-CMOS Process MIXED Product

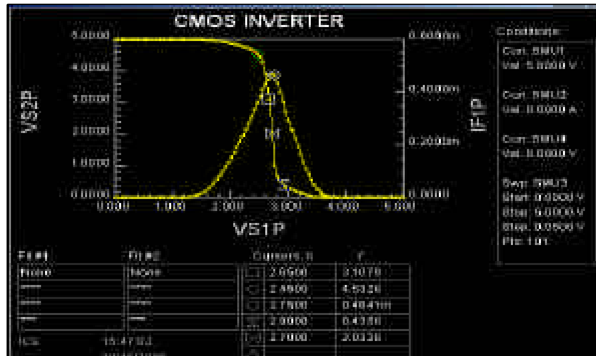
Then Here

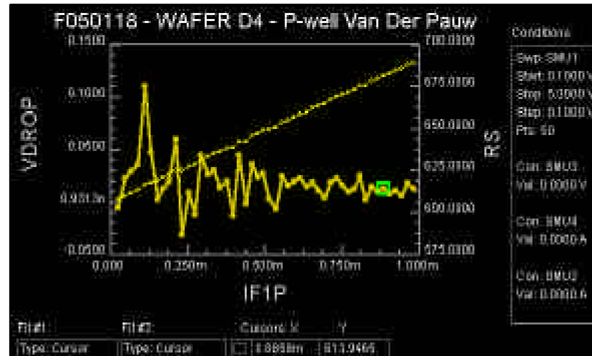
Start Here

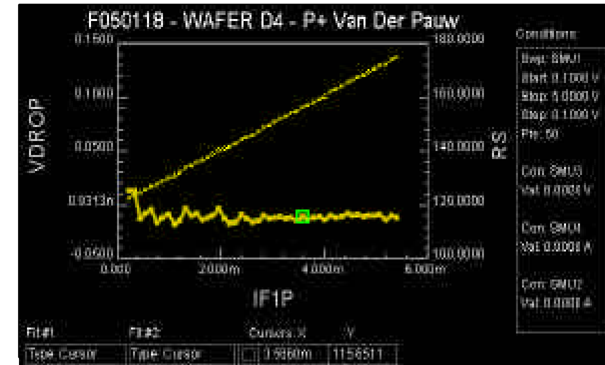


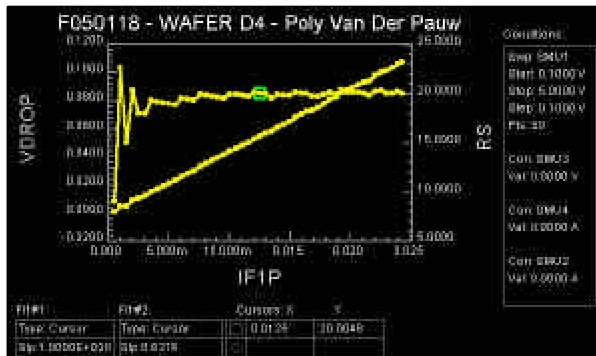
INVERTERS, VAN DER PAUW AND CBKR

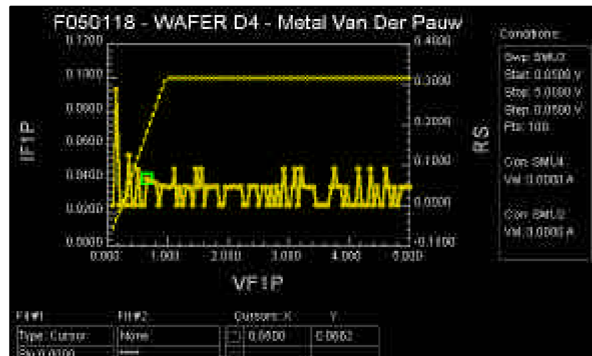
Lot Number = F050118 – Wafer Number = D4 , Die Location R= , C=

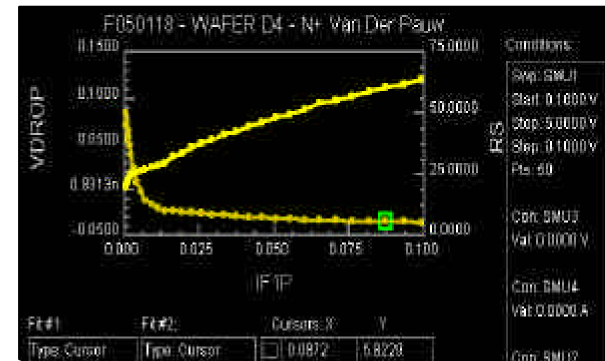


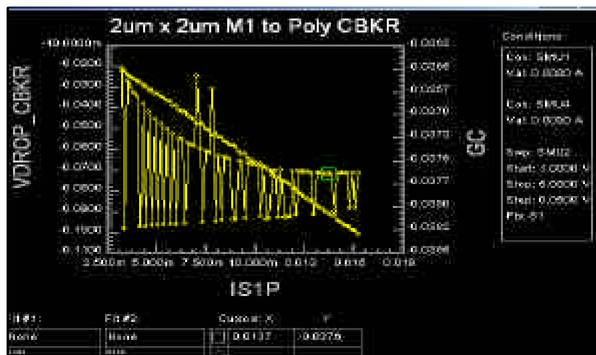


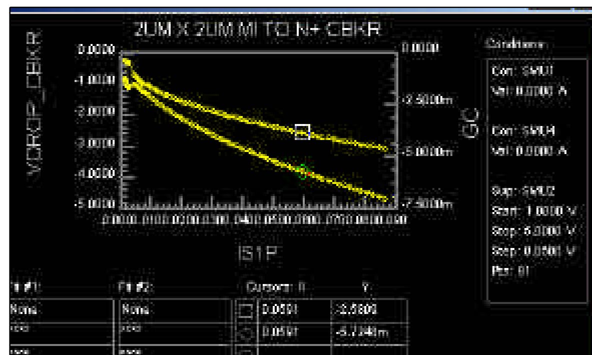


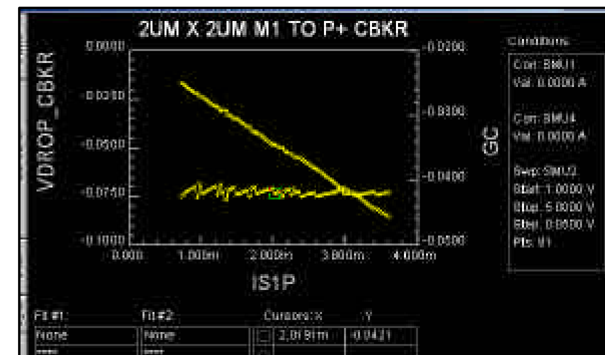












EXTRACTED PARAMETERS FROM INVERTERS, VAN DER PAUW AND CBKR

Lot Number = F050118 – Wafer Number = D4 , Die Location R= , C=

Contact Gs	CBKR	
P+	42	mmho/µm^2
N+	8	mmho/µm^2
poly	37	mmho/µm^2

	Ring Oscillator	Vdd=5V
# Stages	73	
Period	104	nsec
td	0.712	nsec

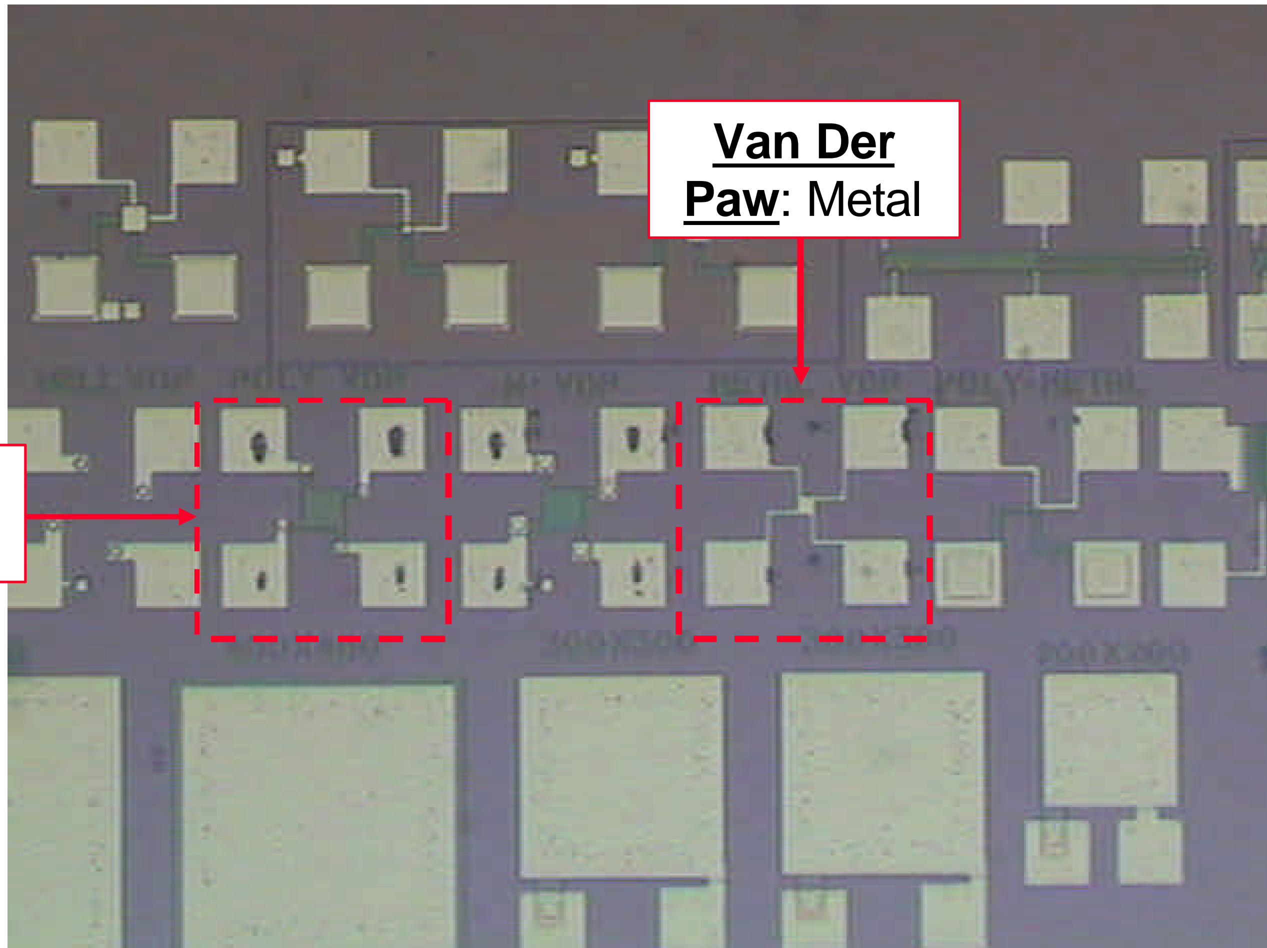
Rhos	Van der Pauw	
P+	115	Ohms
N+	5.8	Ohms
well	614	Ohms
Poly	20.0	Ohms
Al	0.0662	Ohms

	Inverter	
VinL	2.4	V
VinH	3	V
VoL	0.4	V
VoH	4.5	V
Vinv	2.6	V
Imax	4.5	mA
Gain	-21.5	
D0=ViL-VoL	2.0	V
D1=VoH-ViH	1.5	V

	OpAmp	
Gain	None	
Offset	None	mVolts
GBW	None	Hz

	VIA CHAIN	
M1-P+	None	ohms
M1-M2	None	ohms

TE01 Test Structures for SUB-CMOS Process MIXED Product



Van Der Paw: Poly

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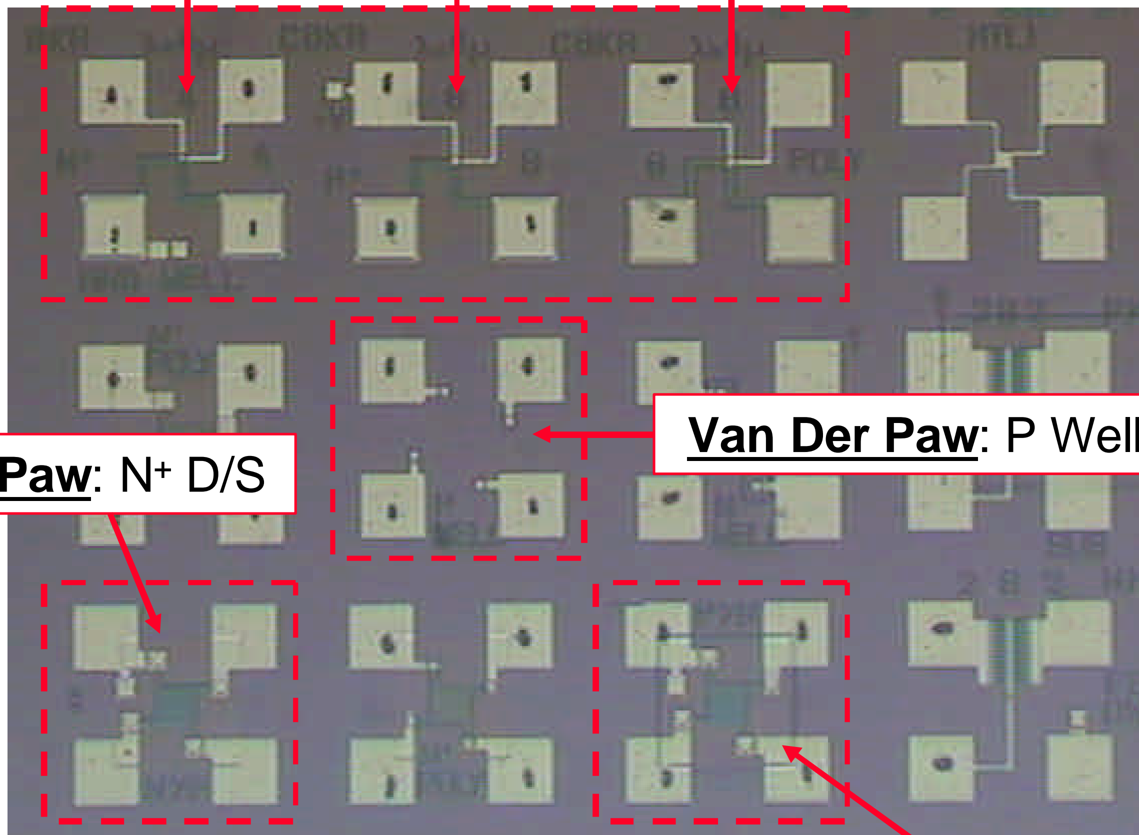
TE01 Test Structures for SUB-CMOS Process MIXED Product

Cross Bridge Kelvin : N+ P+ POLY



Van Der Paw: P Well

Van Der Paw: N+ D/S

Van Der Paw: P+ D/S

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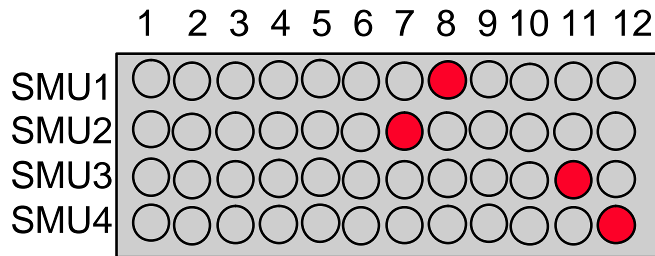
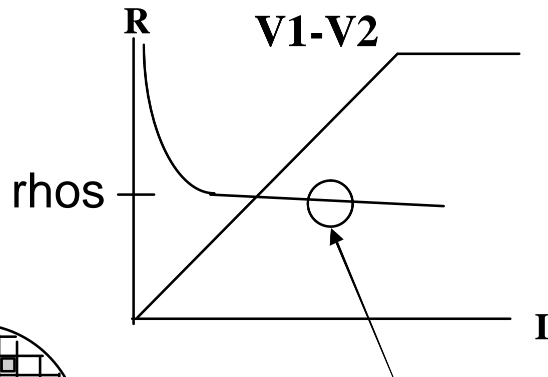
TEST SET UP FOR POLY VAN DER PAUW (SUB-CMOS, MIXED) CHIPS

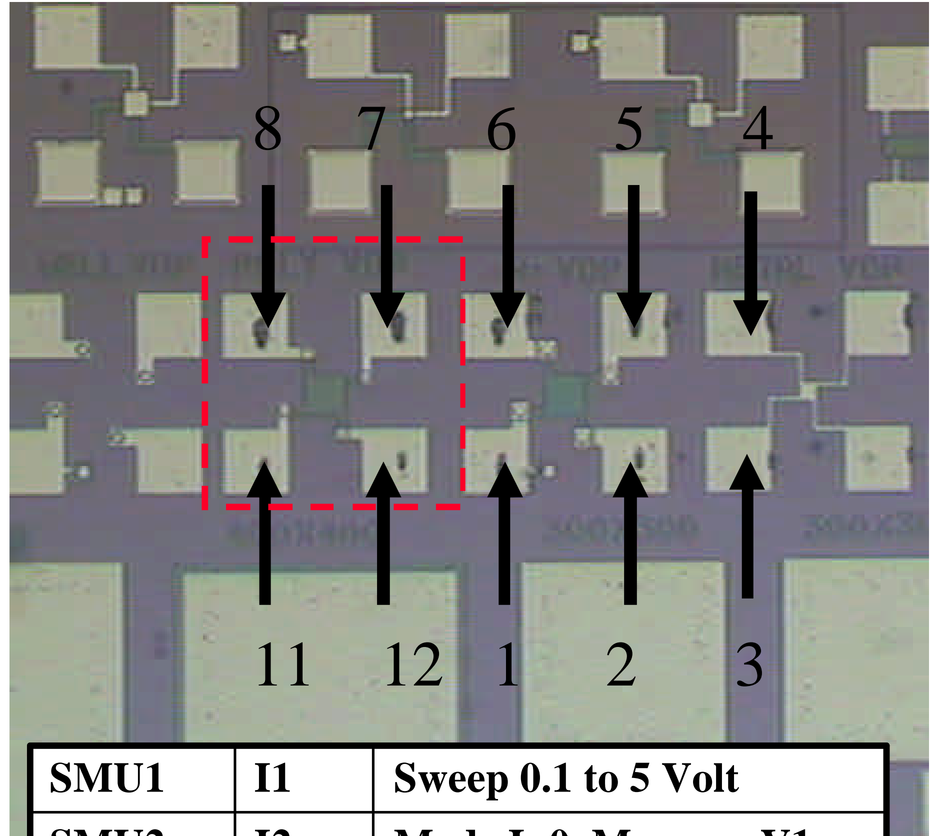
Test Name: VDP-POLY



Switch matrix



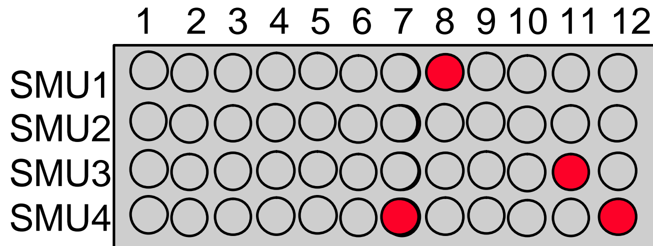
Place a cursor on the graph here to extract rhos value



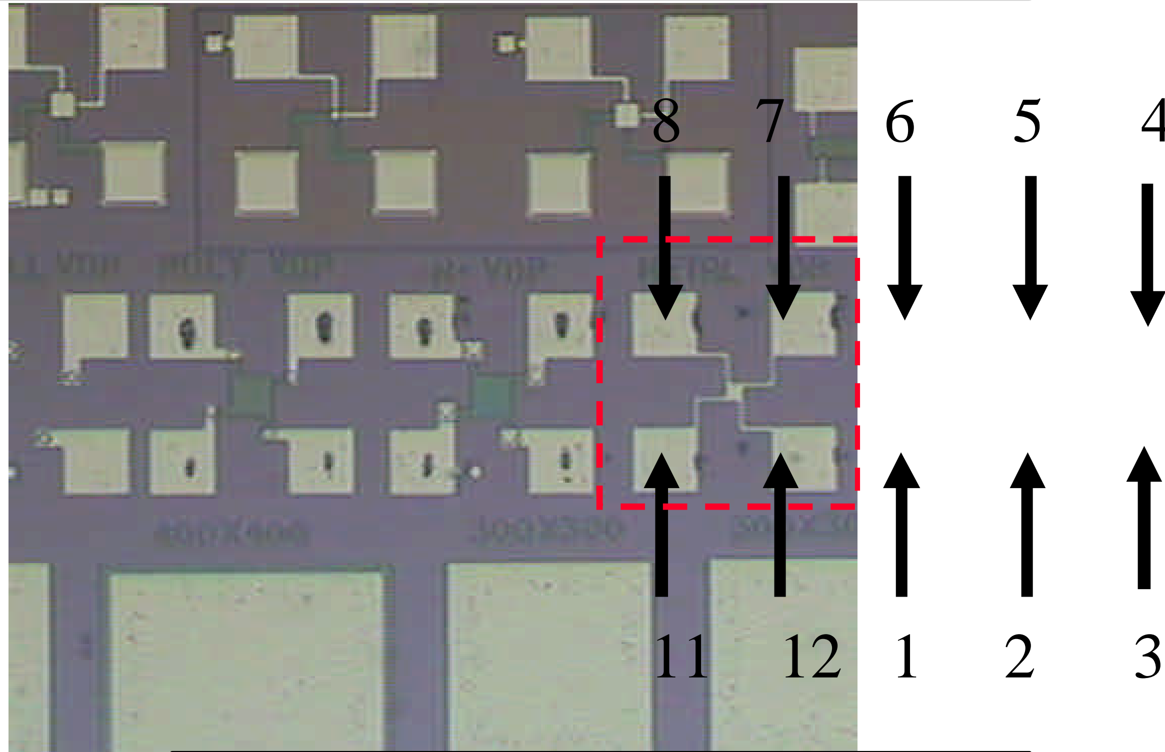
SMU1	I1	Sweep 0.1 to 5 Volt
SMU2	I2	Mode I=0, Measure V1
SMU3	V1	Com
SMU4	V2	Mode I=0, Measure V2
USER F	Rhos	= 4.532 (V1-V2)/I1

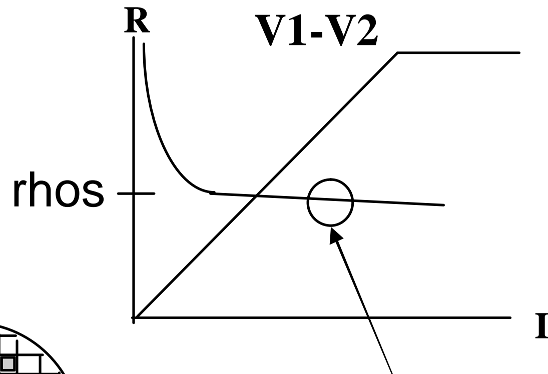
TEST SET UP FOR METAL VAN DER PAUW

Test Name: VDP-MET



Switch matrix



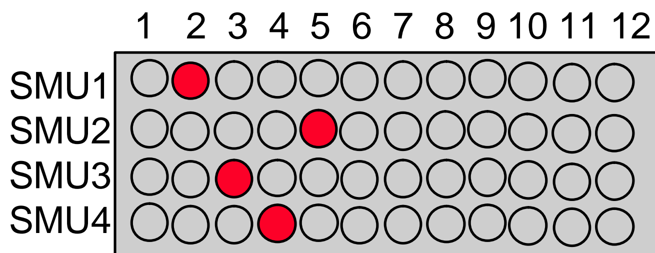


Place a cursor on the graph here to extract rhos value

SMU1	I1	Sweep 0.05 to 5 Volt
SMU2	I2	Mode I=0, Measure V1
SMU3	V1	Com
SMU4	V2	Mode I=0, Measure V2
USER F	Rhos	= 4.532 (V1-V2)/I1

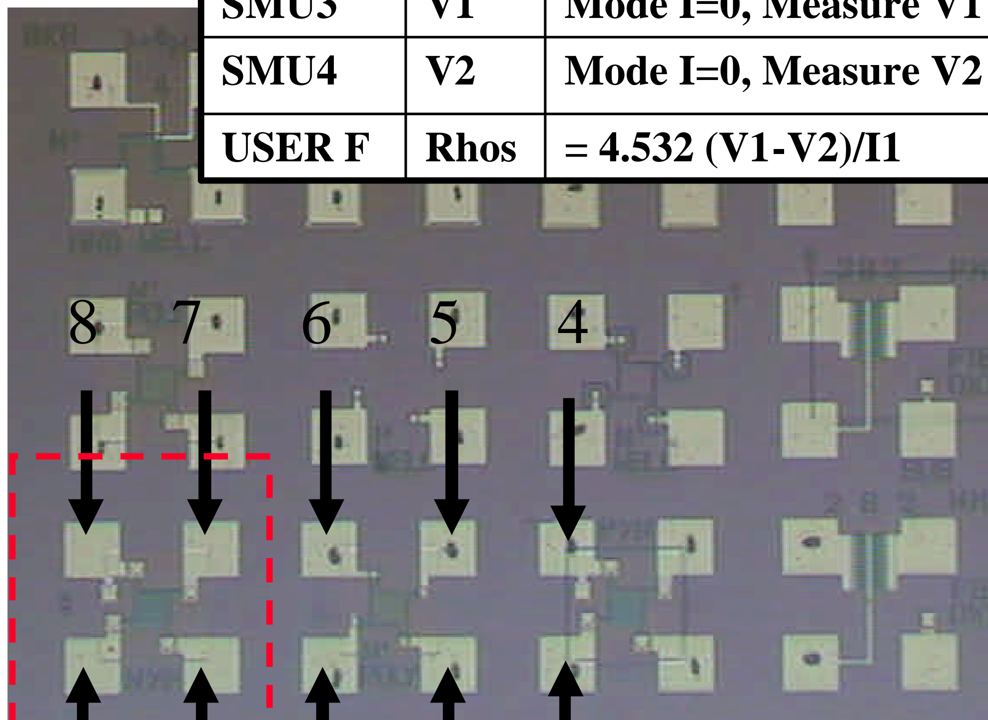
TEST SET UP FOR N+DS VAN DER PAUW

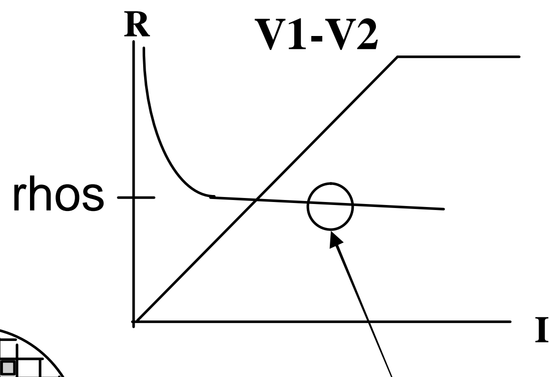
Test Name: VDP-N+

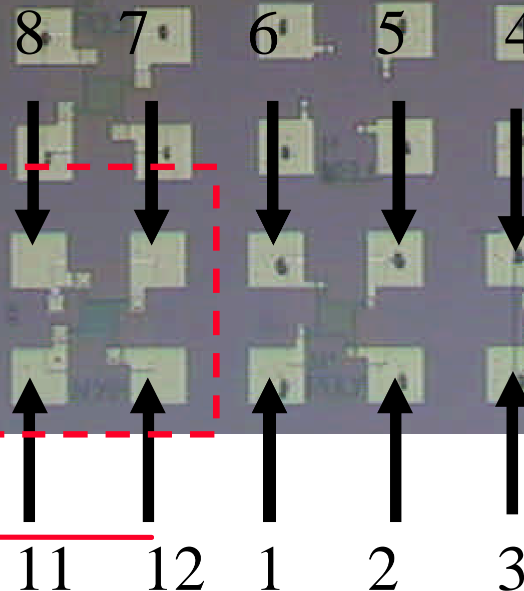


Switch matrix

SMU1	I1	Sweep 0-10mA
SMU2	I2	Com
SMU3	V1	Mode I=0, Measure V1
SMU4	V2	Mode I=0, Measure V2
USER F	Rhos	= 4.532 (V1-V2)/I1



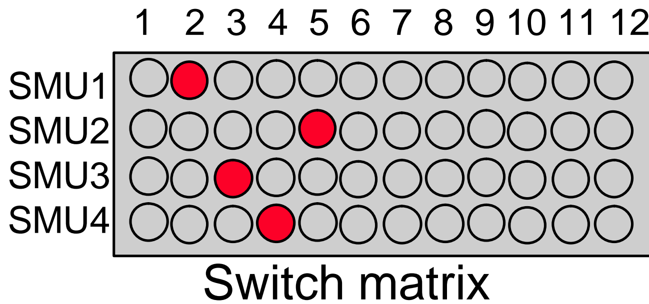




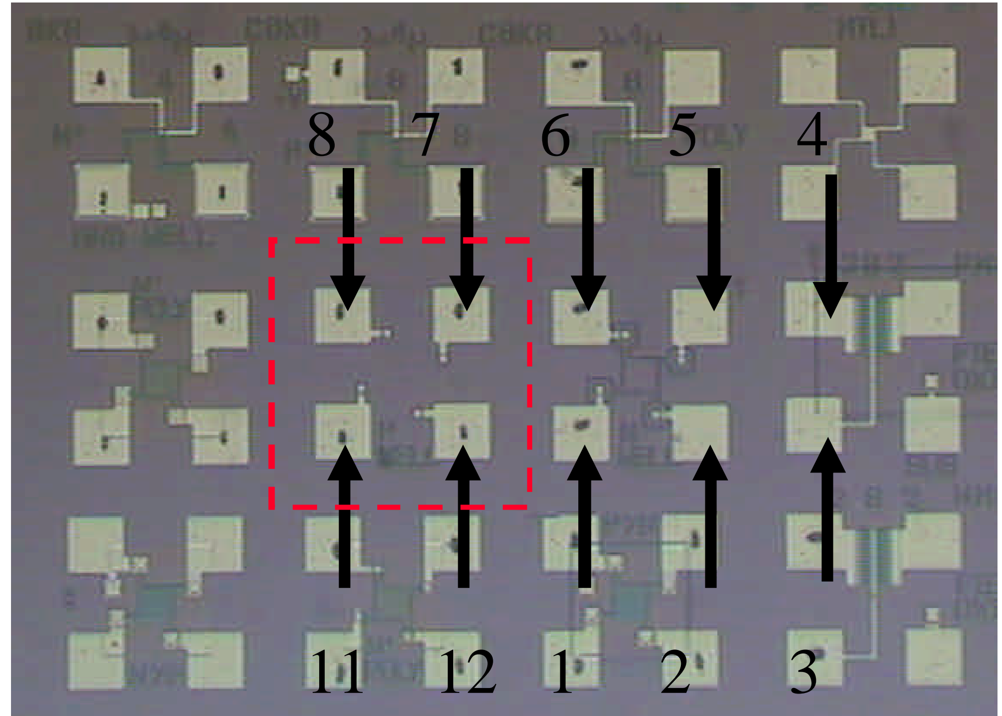
Place a cursor on the graph here to extract rhos value

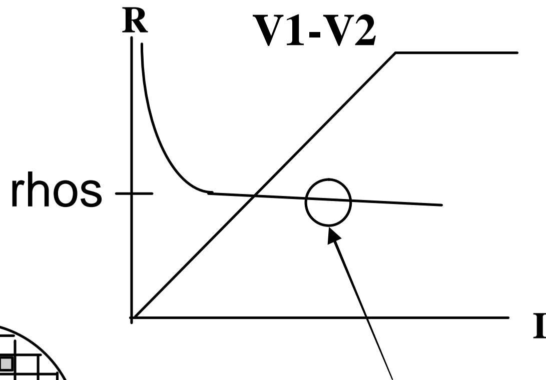
TEST SET UP FOR PWell VAN DER PAUW

Test Name: VDP-PWell



Switch matrix



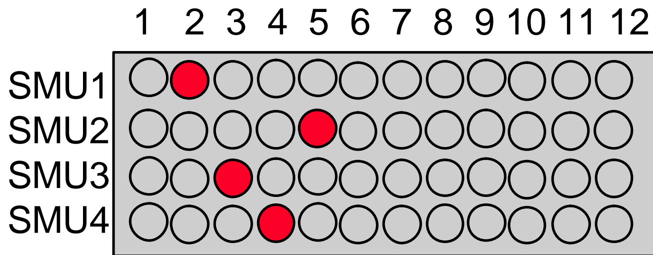


Place a cursor on the graph here to extract rhos value

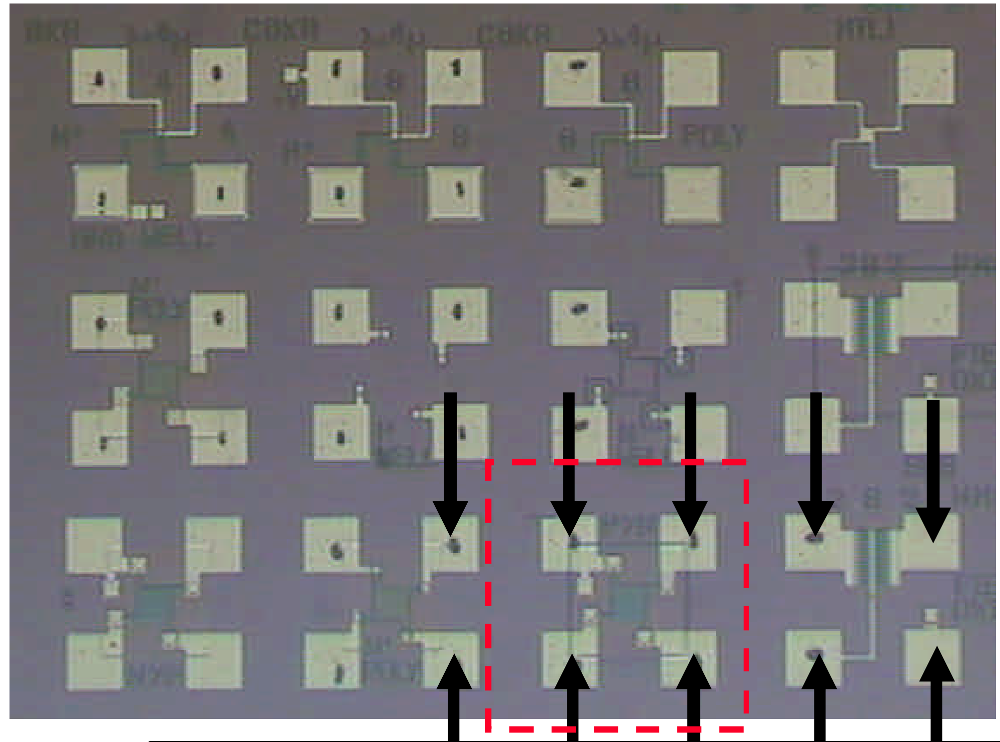
SMU1	I1	Sweep 0-10mA
SMU2	I2	Com
SMU3	V1	Mode I=0, Measure V1
SMU4	V2	Mode I=0, Measure V2
USER F	Rhos	= 4.532 (V1-V2)/I1

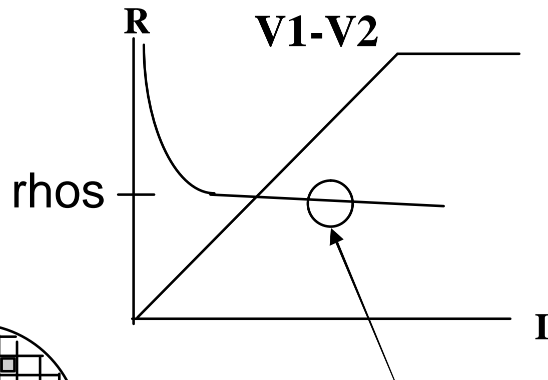
TEST SET UP FOR P+DS VAN DER PAUW

Test Name: VDP-P+



Switch matrix



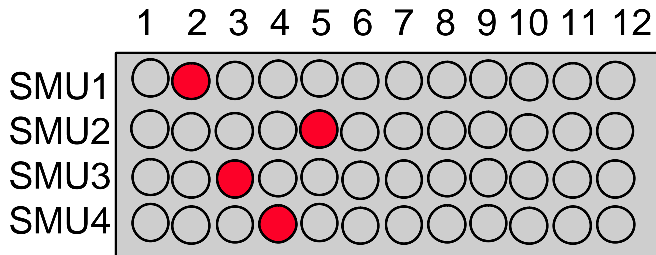


Place a cursor on the graph here to extract rhos value

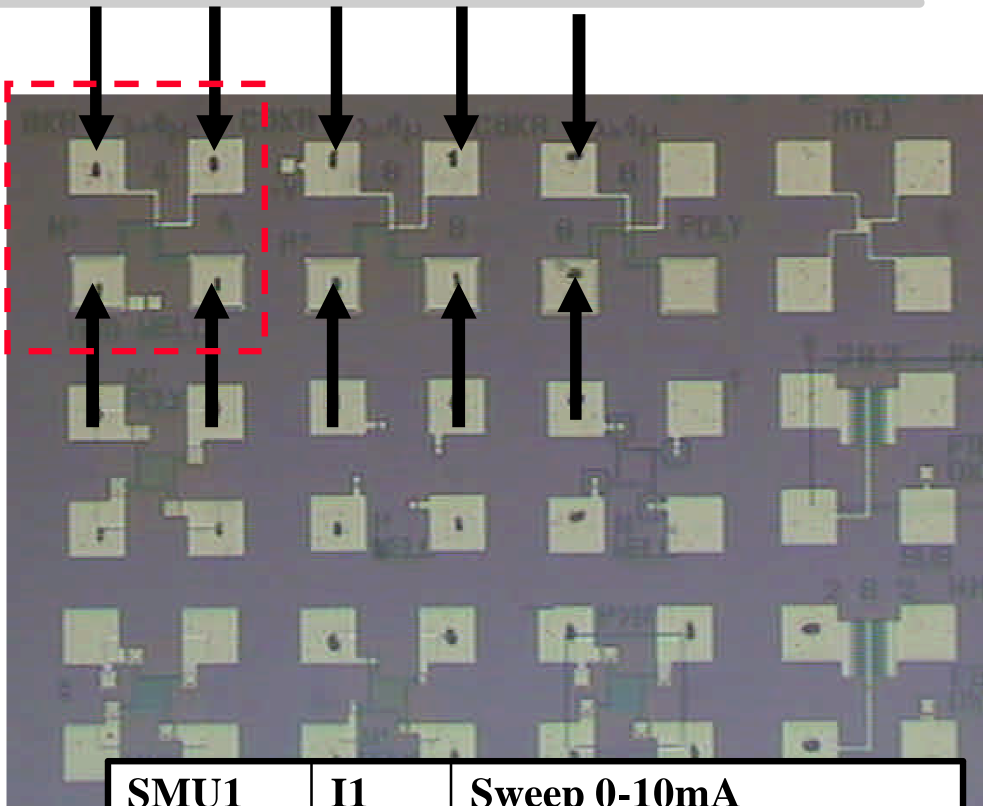
SMU1	I1	Sweep 0-10mA
SMU2	I2	Com
SMU3	V1	Mode I=0, Measure V1
SMU4	V2	Mode I=0, Measure V2
USER F	Rc	= 4.532 (V1-V2)/I1

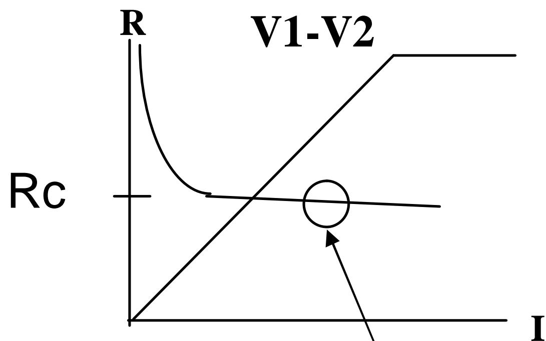
TEST SET UP FOR N+ CBKR

Test Name: CBKR-N



Switch matrix



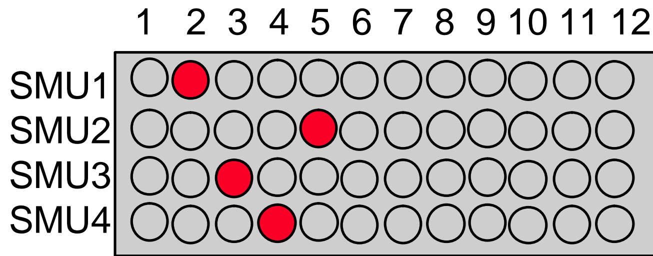


Place a cursor on the graph here to extract Specific Contact Conductance value

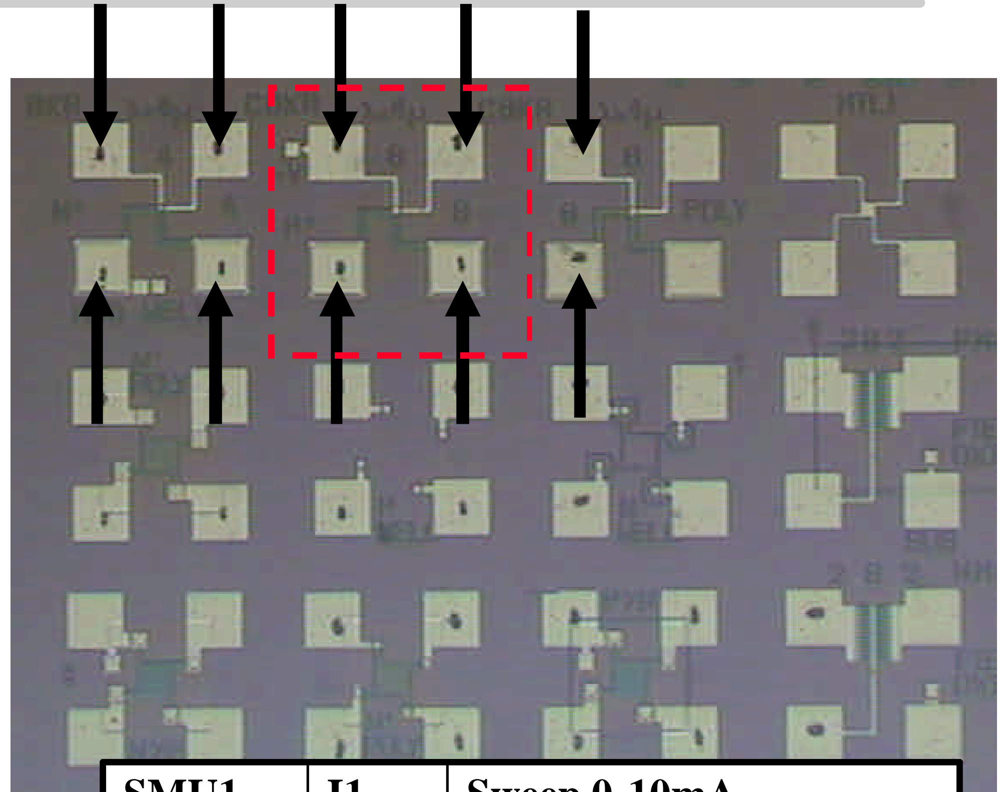
SMU1	I1	Sweep 0-10mA
SMU2	I2	Com
SMU3	V1	Mode I=0, Measure V1
SMU4	V2	Mode I=0, Measure V2
USER F	Rc	= (V1-V2)/I1

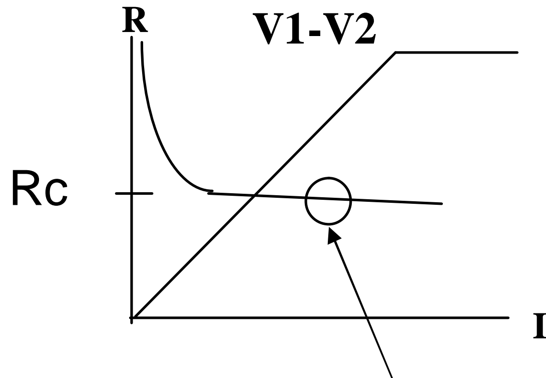
TEST SET UP FOR P+ CBKR

Test Name: CBKR-P



Switch matrix



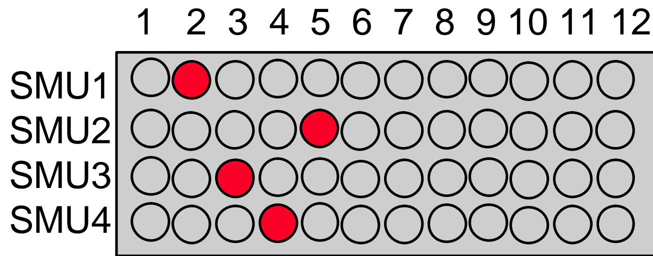


Place a cursor on the graph here to extract Specific Contact Conductance value

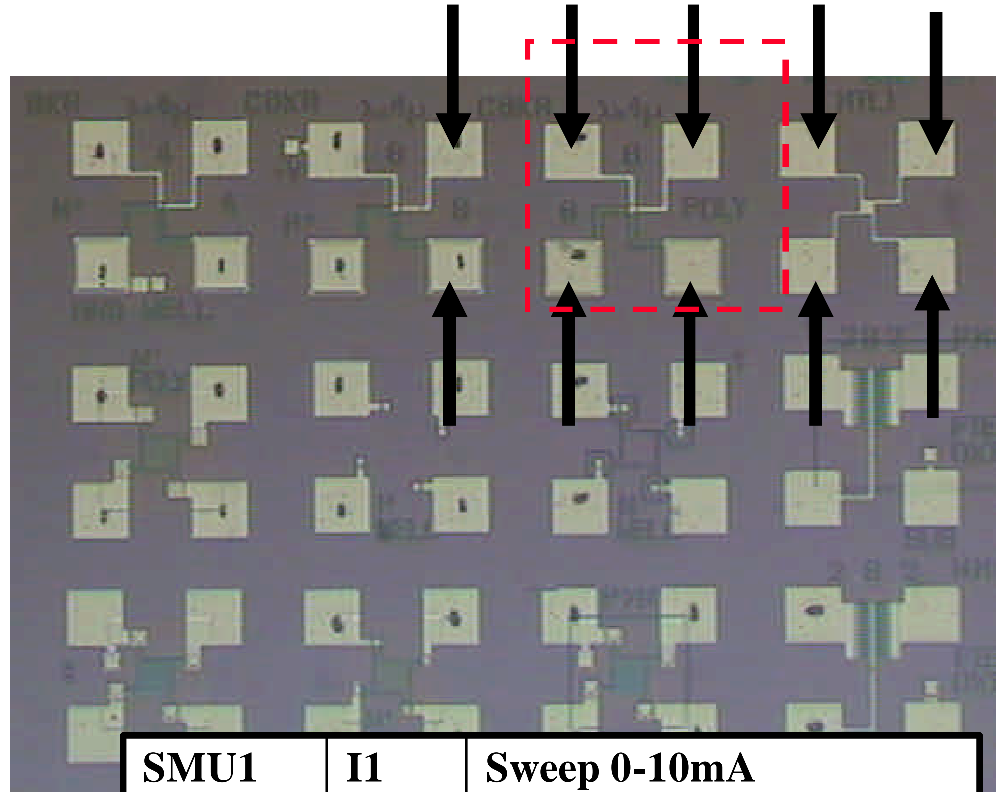
SMU1	I1	Sweep 0-10mA
SMU2	I2	Com
SMU3	V1	Mode I=0, Measure V1
SMU4	V2	Mode I=0, Measure V2
USER F	Rc	= (V1-V2)/I1

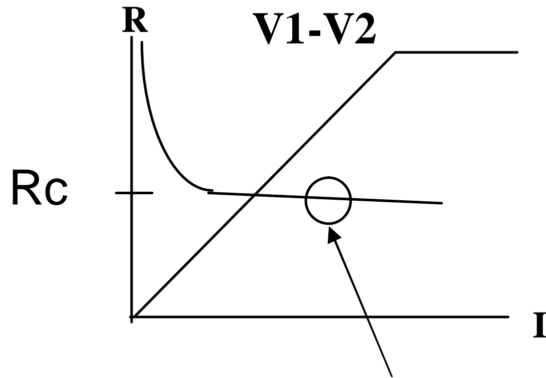
TEST SET UP FOR POLY CBKR

Test Name: CBKRPOLY



Switch matrix





Place a cursor on the graph here to extract Specific Contact Conductance value

SMU1	I1	Sweep 0-10mA
SMU2	I2	Com
SMU3	V1	Mode I=0, Measure V1
SMU4	V2	Mode I=0, Measure V2
USER F	Rhos	= (V1-V2)/I1

TE02 TRANSISTORS

```
5/04/06                              MESA                          IGMSINQ    S36801
8:35:54                   Instruction Group Inquiry               QPADEV000W   RIT

Type information.  Then Enter.
  1=Display document, 5=Display detail

  Plant . . . . . . . . . :   RIT
  Instruction group . .   SUB-CMOS-TE02           TEST COMPLETED WAFERS
    Revision . . . . . . .   150

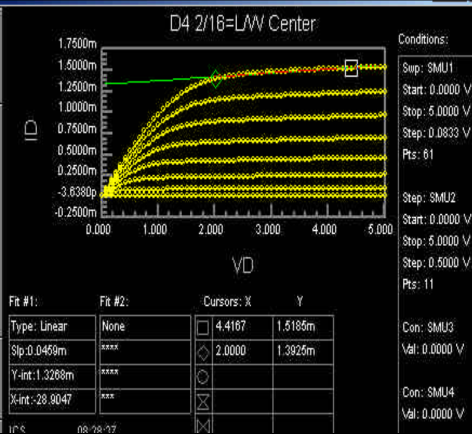
  Opt Subgroup   Text
   _             1.0 Test PMOS and NMOS Transistors
   _                 for threshold voltage, tranconductance, lambda,
   _                 subthreshold slope, min and max current value on the
   _                 subthreshold test
   _             2.0 Record VTn,VTp,gmn,gmp,sub-Vt-slope,Isub-min,Isub-max,
   _                 Lambda,transistor width&length for nmos & pmos, Vt field

                                                                        Bottom
F3=Exit   F4=Prompt   F5=Refresh   F10=View 2   F12=Cancel
```

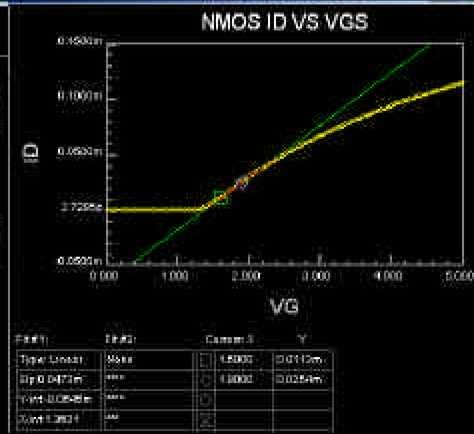
MOSFET IV CHARACTERISTICS

Lot Number = F050118	Wafer Number = D4	Date = 11-17-2006
Process = SMFL CMOS	Product = DAC03	

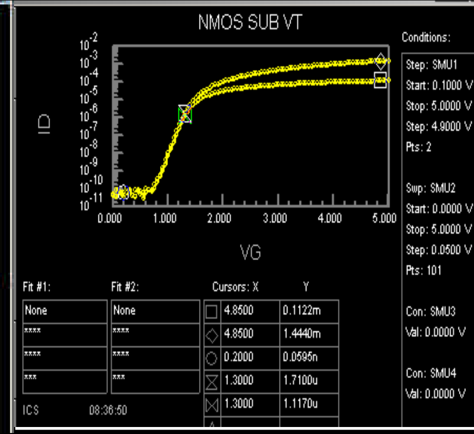
NMOS L/W = 2/16



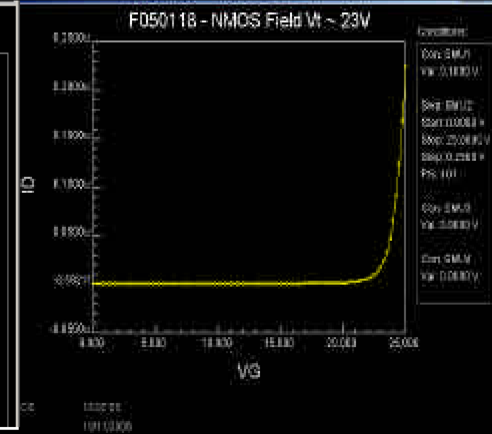
NFAM



NVT

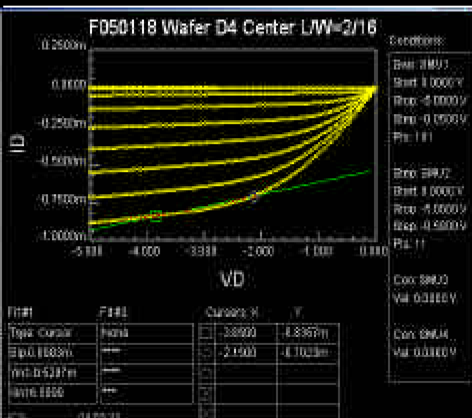


NSUB

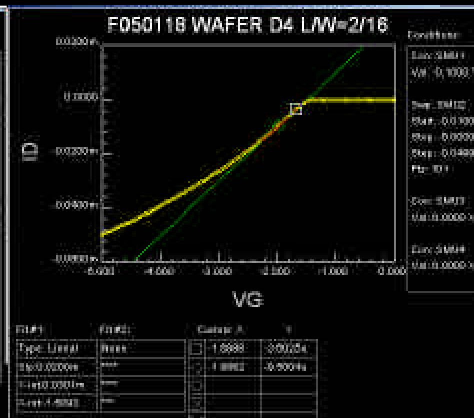


NFIELD

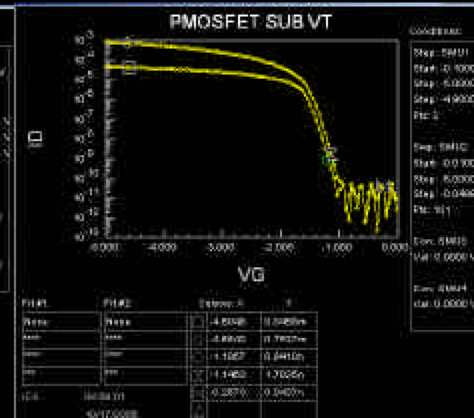
PMOS L/W = 2/16



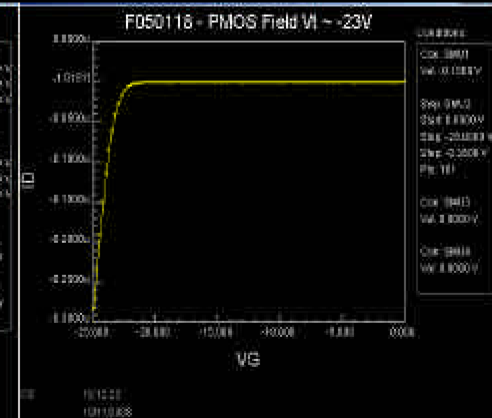
PFAM



PVT



PSUB



PFIELD

MOSFET EXTRACTED PARAMETERS

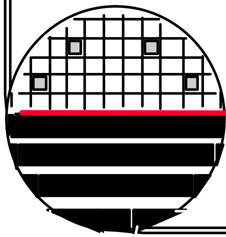
Lot Number = F050118 – Wafer Number = D4, Die Location R= , C=

	PMOS	NMOS	Units
Mask Length / Width	**2/16**	**2/16**	**µm**
VT	**-1.51**	**1.36**	**V**
Lambda (for Vgs = Vdd)	**0.115**	**0.0417**	**V^{-1}**
Max gm / mm of channel width	**21.3**	**31.3**	**S/mm**
Idrive	**54.4**	**93.8**	**µA/µm**
Ion/Ioff @ Vd = 0.1V	**6**	**5**	**Decades**
Ion/Ioff @ Vd = 5V	**7**	**6**	**Decades**
Ioff @ Vd = 0.1V	**5.9e-11**	**5.0e-10**	**A/µm**
Ioff @ Vd = 5V	**5.9e-11**	**5.0e-10**	**A/µm**
Sub-Vt Slope @ Vd = 0.1V	**90**	**190**	**mV/Dec**
Sub-Vt Slope @ Vd = 5 V	**90**	**190**	**mV/Dec**
DIBL@1nA/µm =$\Delta V_g/\Delta V_d$	**0**	**0**	**mV/V**
Field VT	**-23**	**23**	**V**

TE02 TEST STRUCTURES

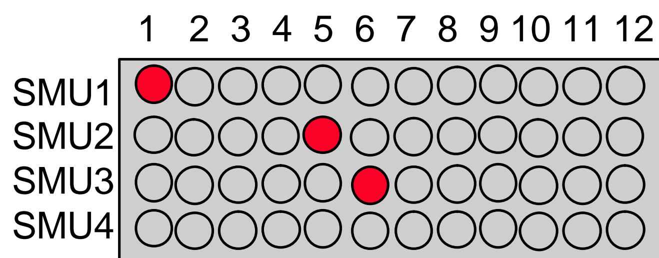
Field FETs

NMOS & PMOS test transistors

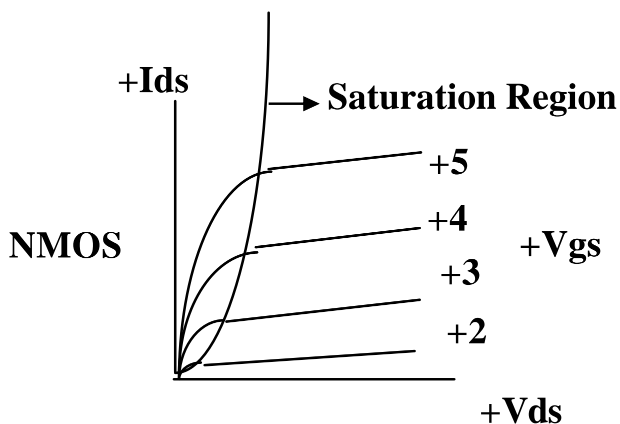


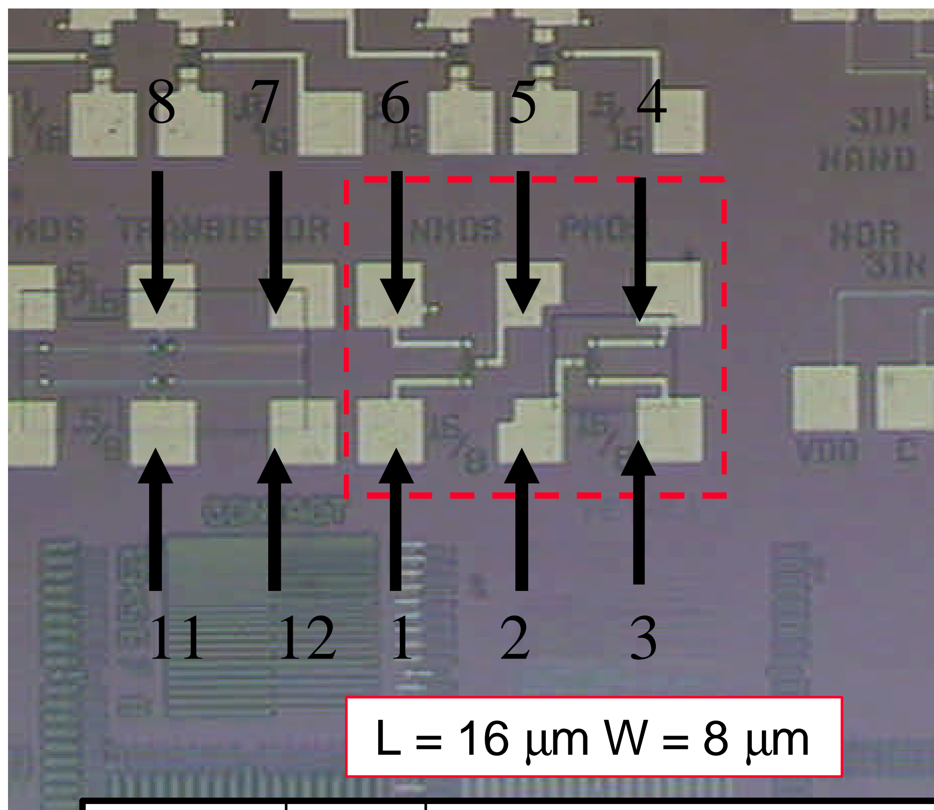
LARGE NMOS FAMILY OF CURVES

Test Name: NFAM



Switch matrix



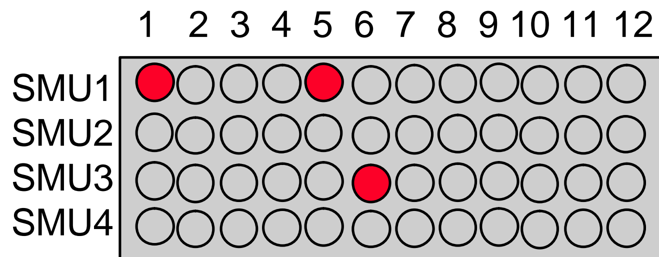


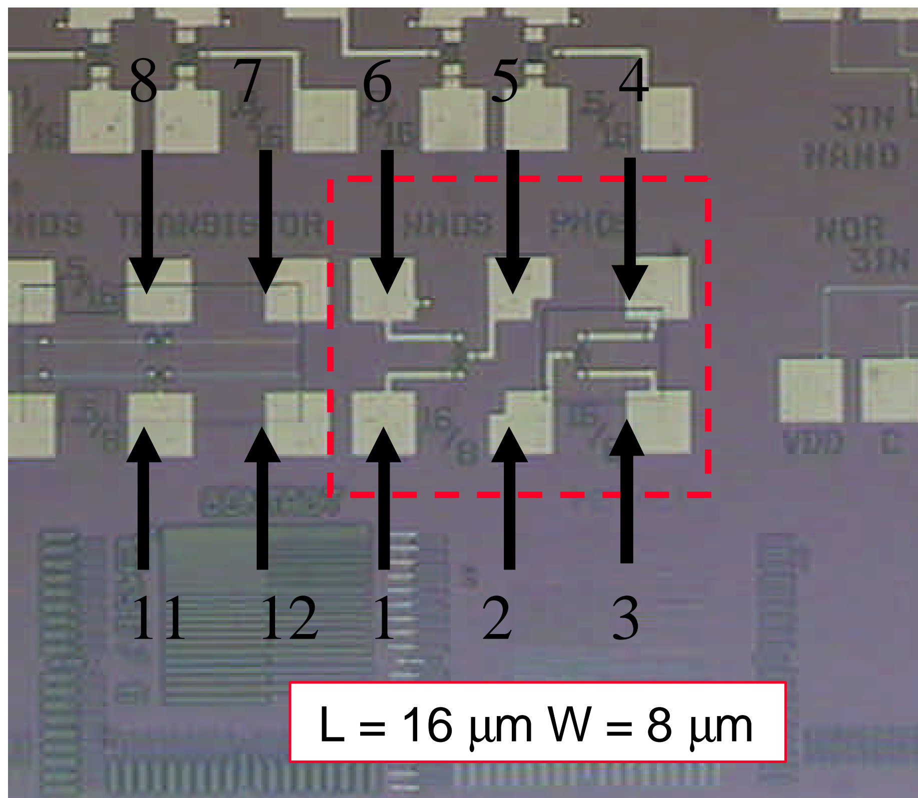
SMU1	Vds	Sweep 0 - 5 V, 101 steps
SMU2	Vgs	11 Steps 0 - 5V
SMU3	Com	Vs = 0
SMU4		

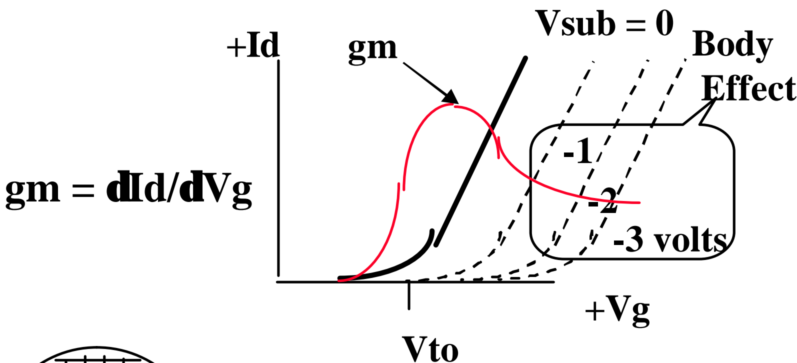
Extract: Lambda

LARGE NMOS ID-VGS

Test Name: NVT





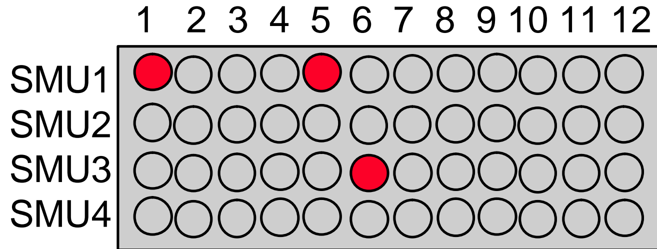


SMU1	Vgs	Sweep 0- 5 V, 101 steps
SMU2		
SMU3	Com	Vs = 0
SMU4		

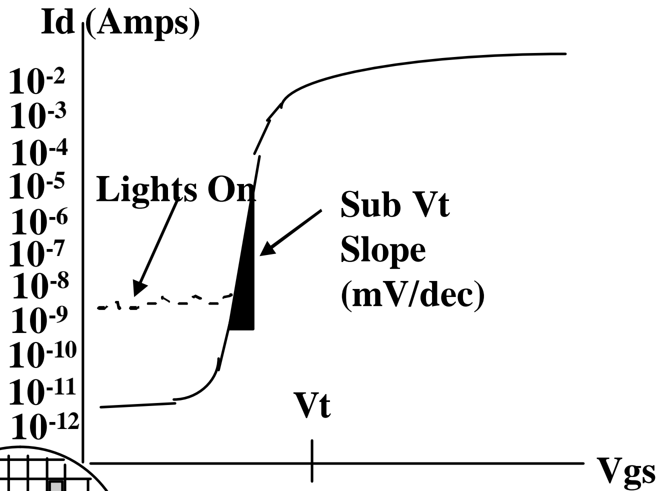
Extract: Max gm, Vto

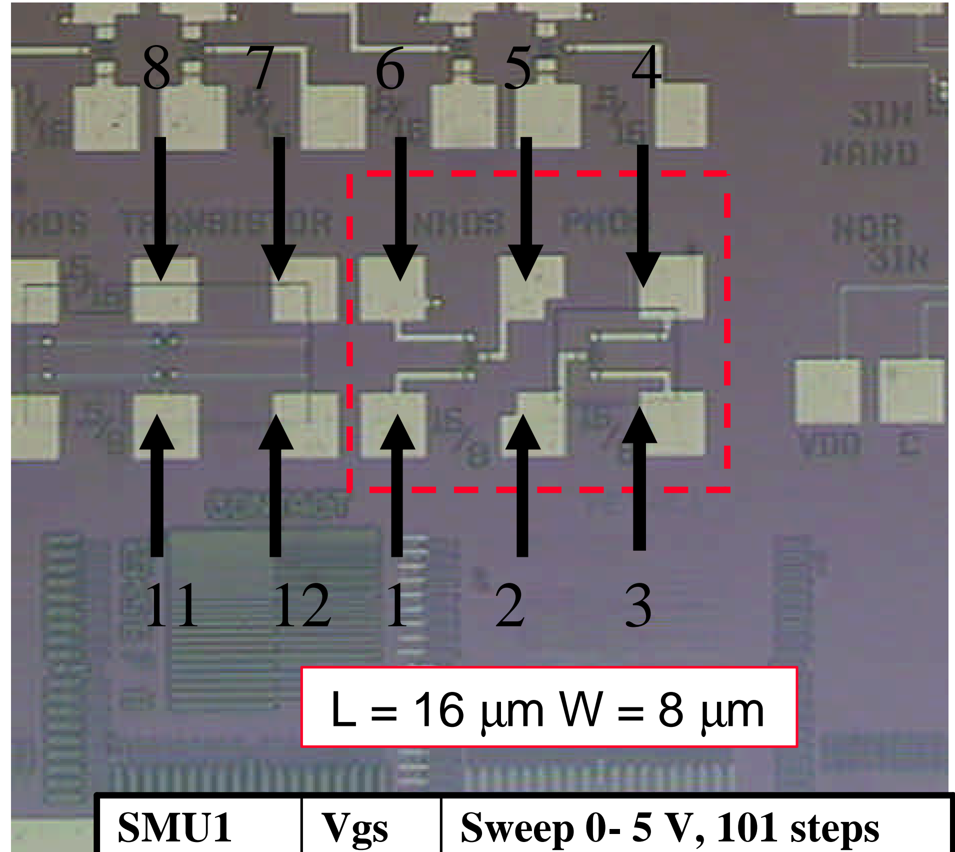
LARGE NMOS SUBTHRESHOLD

Test Name: NSUB



Switch matrix



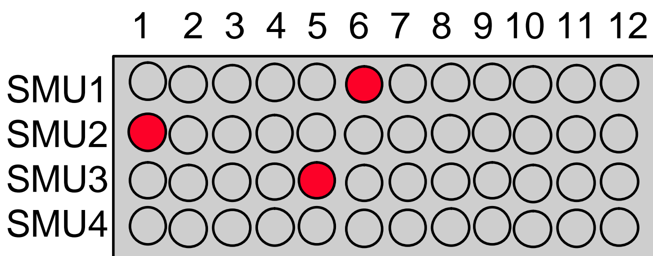


Extract: Imax, Imin, Sub Slope

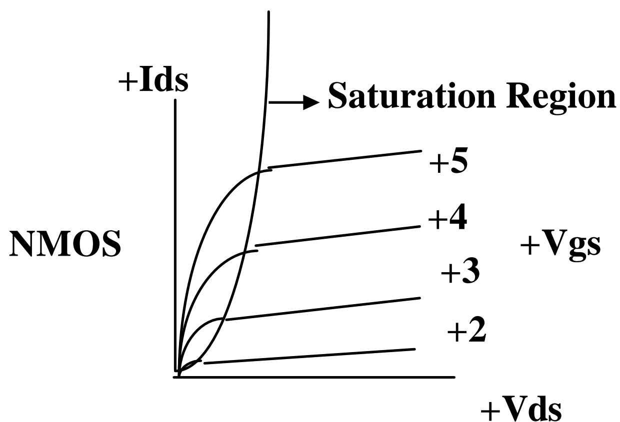
SMU1	Vgs	Sweep 0- 5 V, 101 steps
SMU2		
SMU3	Com	Vs = 0
SMU4		

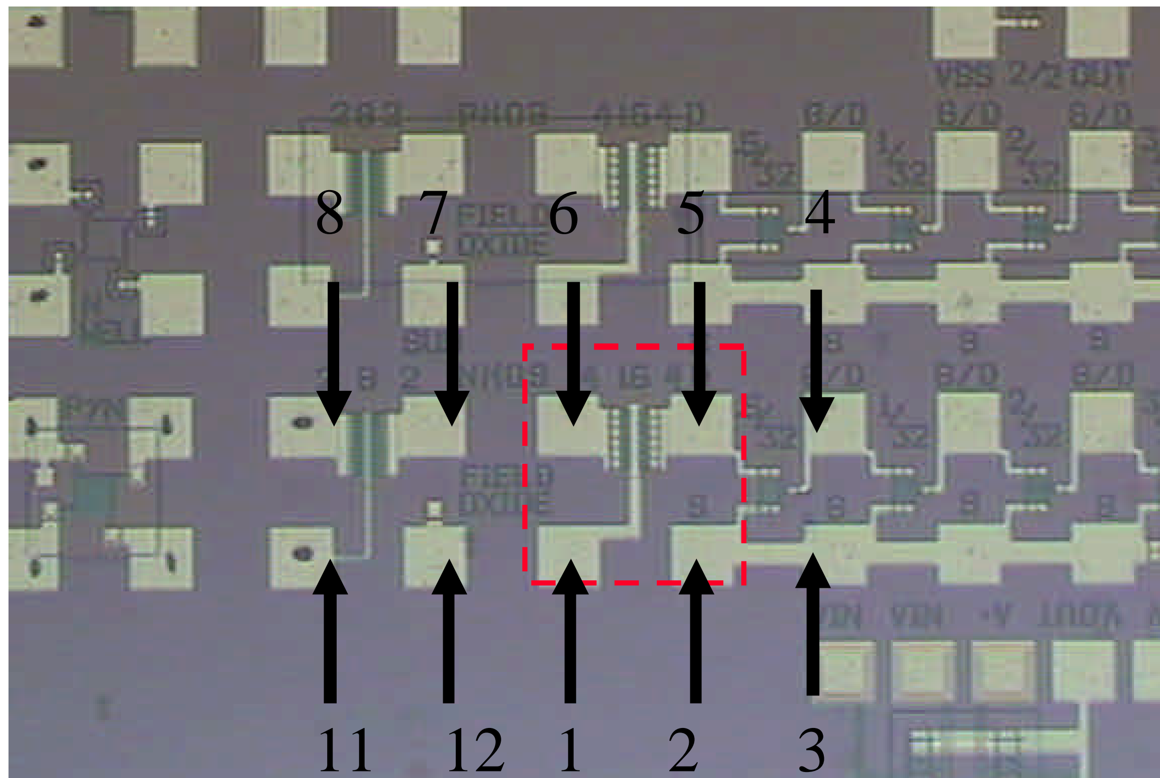
NMOS FIELD VT

Test Name: NFIELD

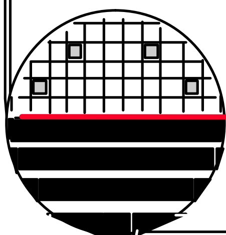


Switch matrix





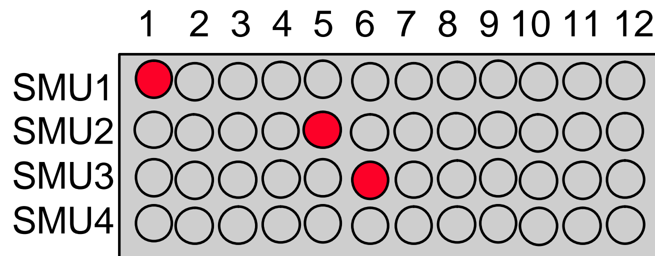
SMU1	Vds	Sweep 0 to 20 V, 101 steps
SMU2	Vgs	11 Steps 0 to 20V
SMU3	Com	Vs = 0
SMU4		



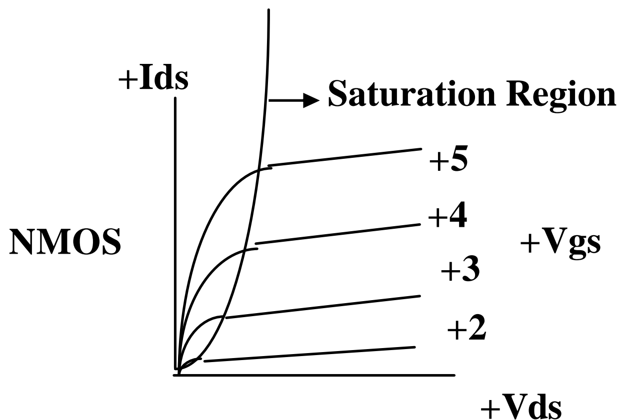
Extract: ~Vt

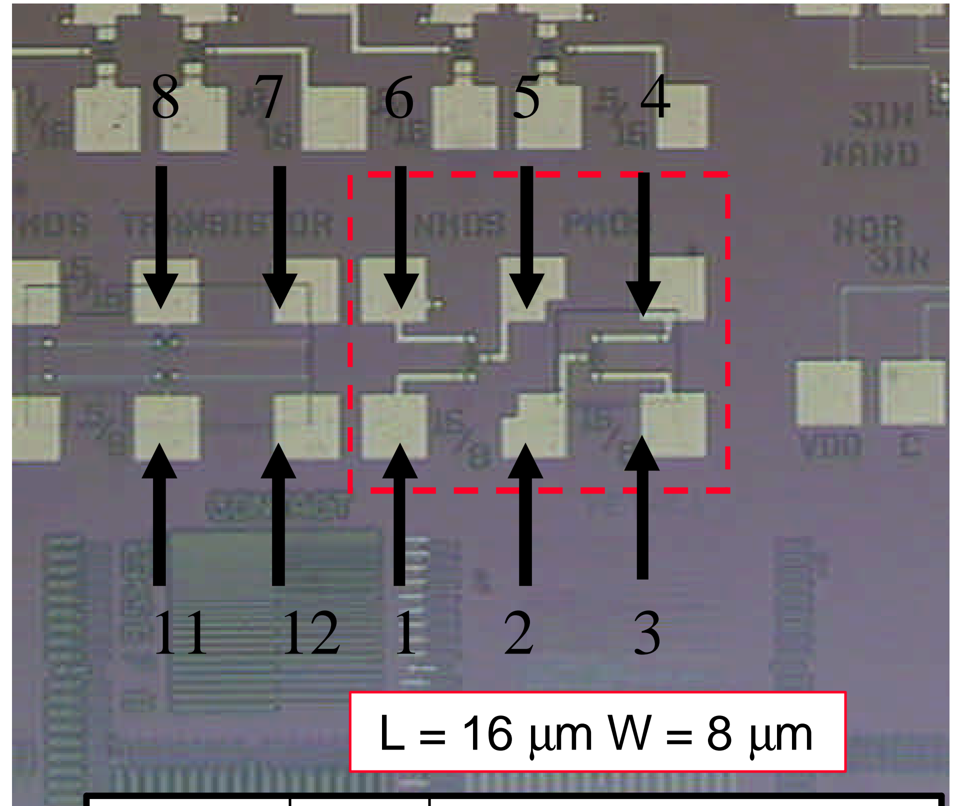
LARGE PMOS FAMILY OF CURVES

Test Name: PFAM



Switch matrix



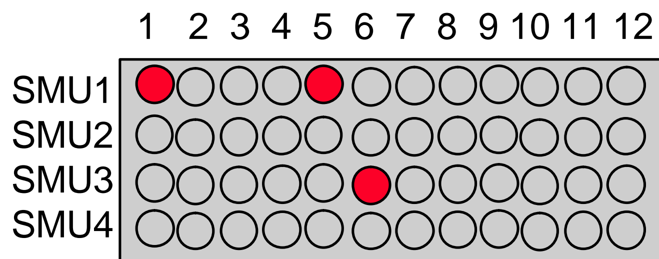


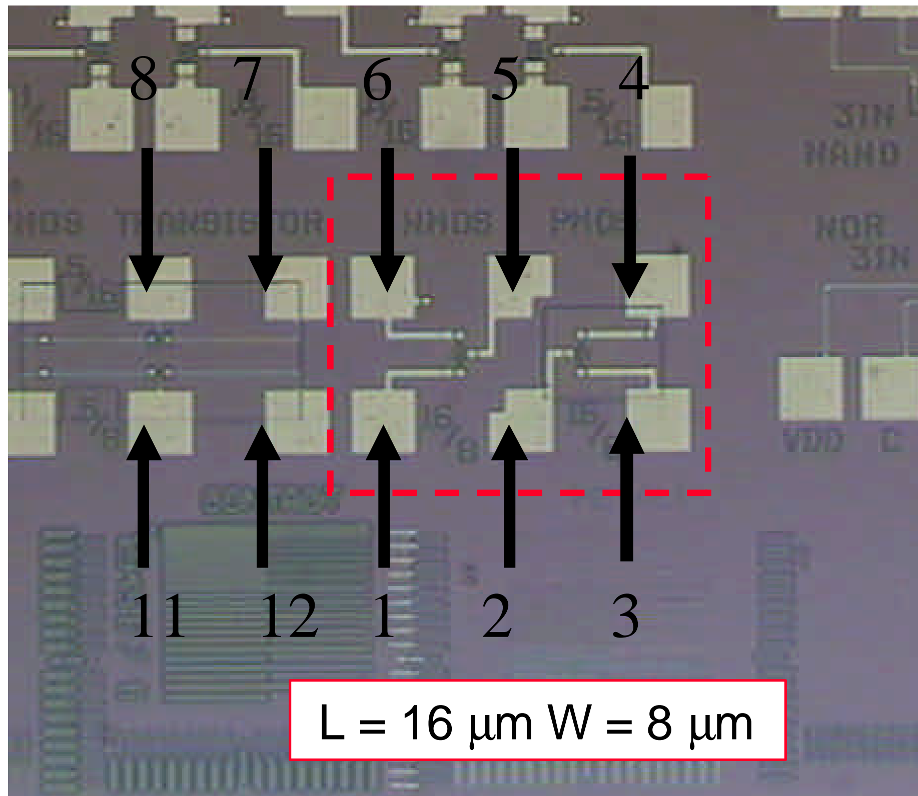
SMU1	Vds	Sweep 0 - 5 V, 101 steps
SMU2	Vgs	11 Steps 0 - 5V
SMU3	Com	Vs = 0
SMU4		

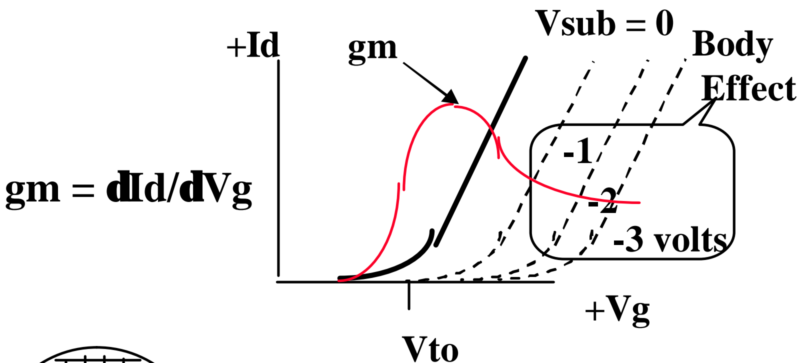
Extract: Lambda

LARGE PMOS ID-VGS

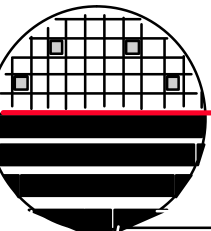
Test Name: PVT







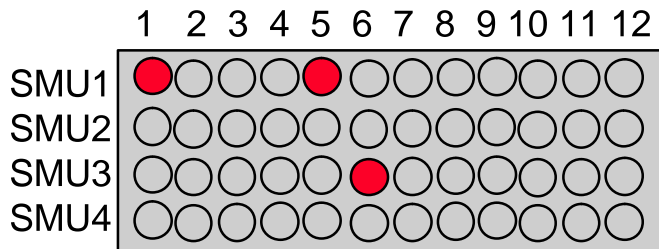
SMU1	Vgs	Sweep 0- 5 V, 101 steps
SMU2		
SMU3	Com	Vs = 0
SMU4		



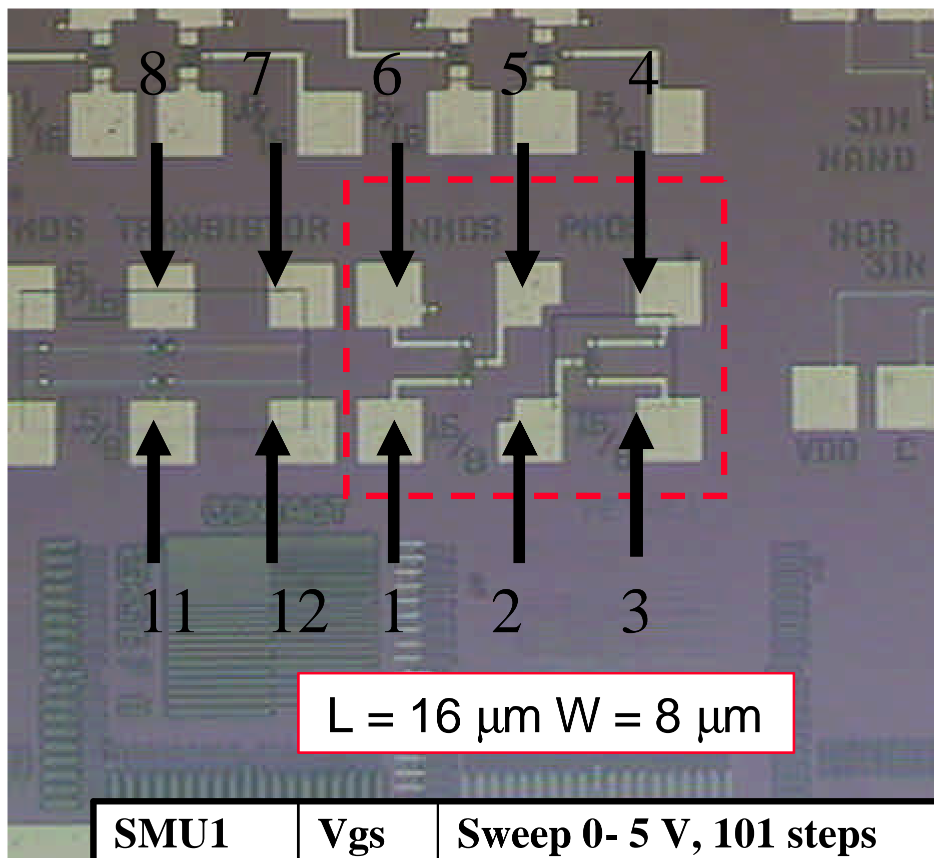
Extract: Max gm, Vto

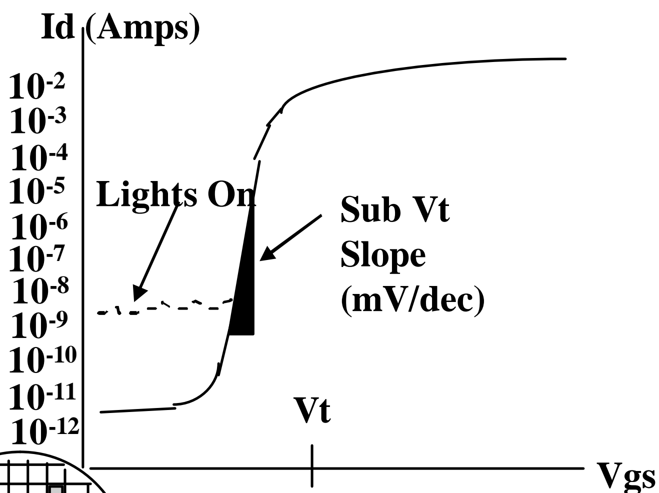
LARGE PMOS SUBTHRESHOLD

Test Name: PSUB



Switch matrix



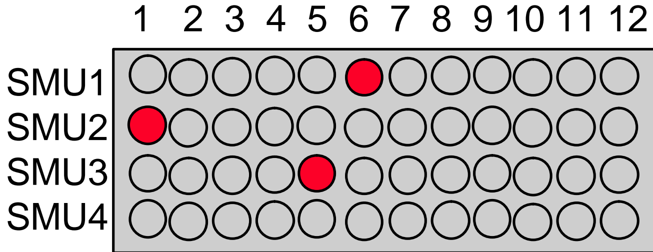


SMU1	Vgs	Sweep 0- 5 V, 101 steps
SMU2		
SMU3	Com	Vs = 0
SMU4		

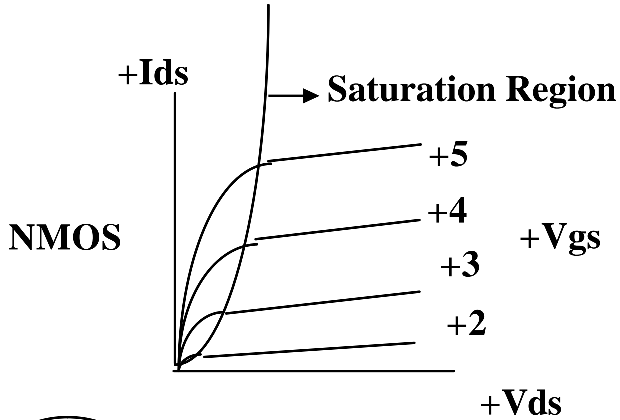
Extract: Imax, Imin, Sub Slope

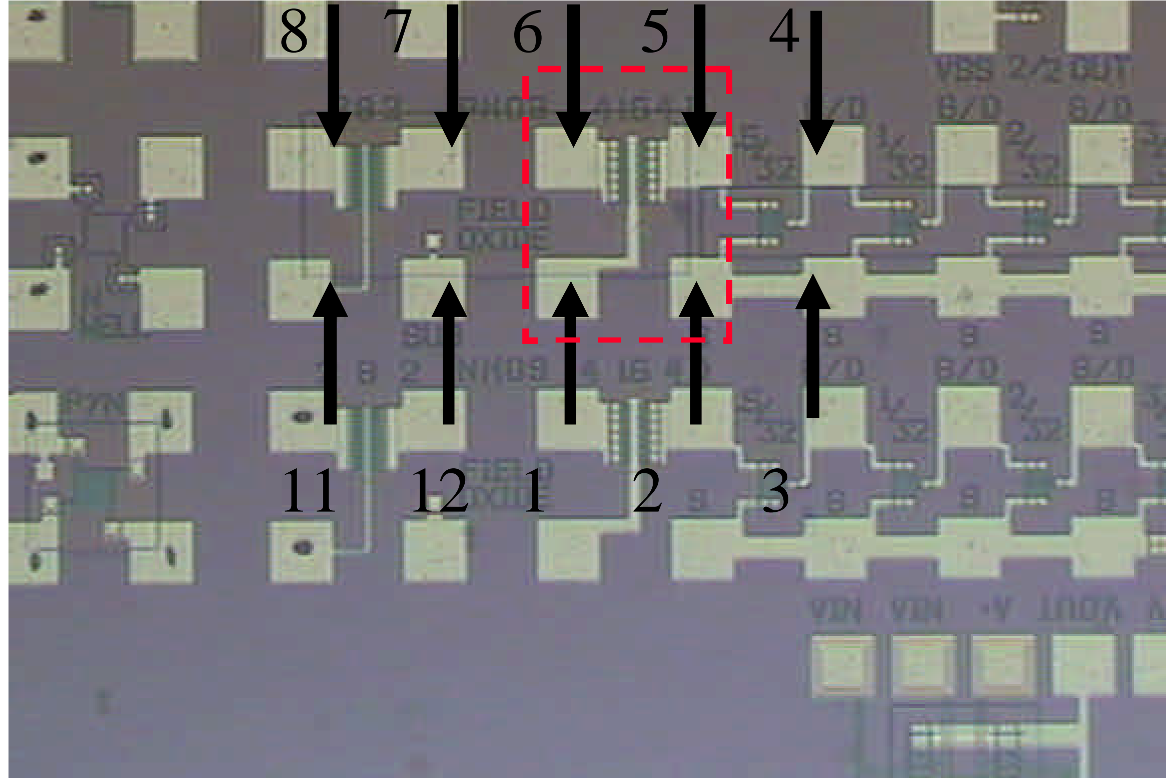
PMOS FIELD VT

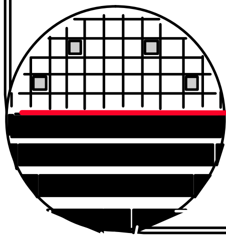
Test Name: PFIELD



Switch matrix







Extract: ~Vt

SMU1	Vds	Sweep 0 to -20 V, 101 steps
SMU2	Vgs	11 Steps 0 to - 20V
SMU3	Com	Vs = 0
SMU4		

TE03 INTEGRATED CIRCUITS

```
   5/04/06                        MESA                       IGMSINQ     S36801
   8:37:20              Instruction Group Inquiry            QPADEV000W    RIT

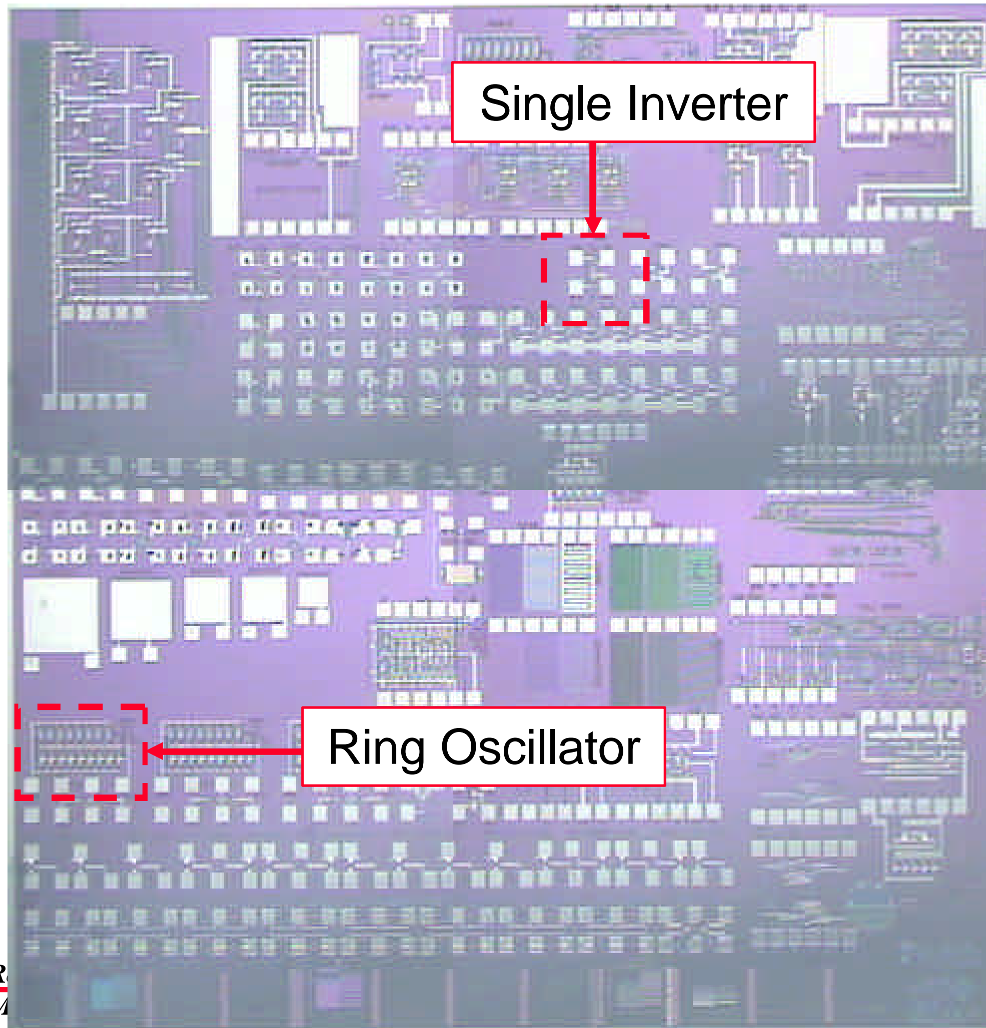
 Type information.  Then Enter.
   1=Display document, 5=Display detail

   Plant . . . . . . . . :   RIT
   Instruction group  . .    SUB-CMOS-TE03         TEST COMPLETED WAFERS
     Revision . . . . . .    150

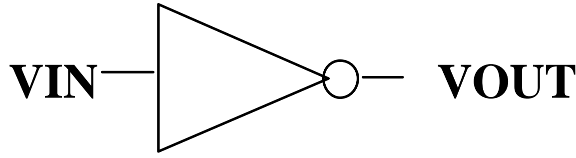
   Opt Subgroup   Text
    _             1.0 Test Inverters and Ring Oscillator
    _             2.0 Record ViL, ViH, VoL, VoH, Vinv, Imax, Ring Oscillator
    _                 Frequency, Number of Stages

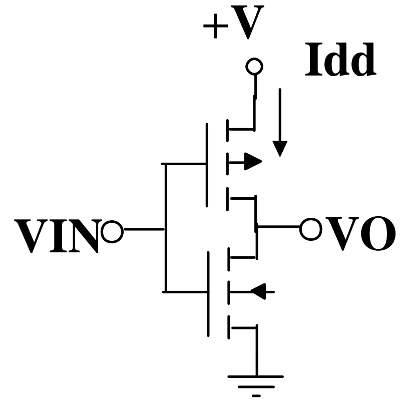
                                                                        Bottom
 F3=Exit   F4=Prompt   F5=Refresh   F10=View 2   F12=Cancel
```

TE03 TEST STRUCTURES



INVERTERS





CMOS

VOUT

+V

Voh

Imax

Slope = Gain

Idd

VoL

0

VIN

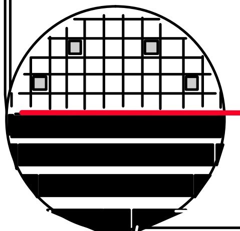
0

+V

ViL

Vih

Vinv

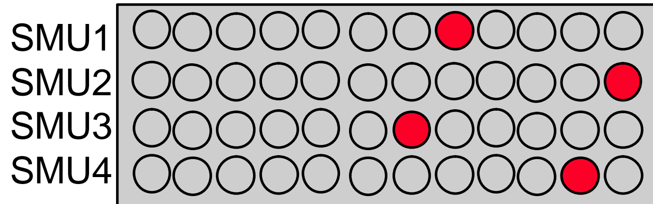


D0 noise margin=ViL-VoL

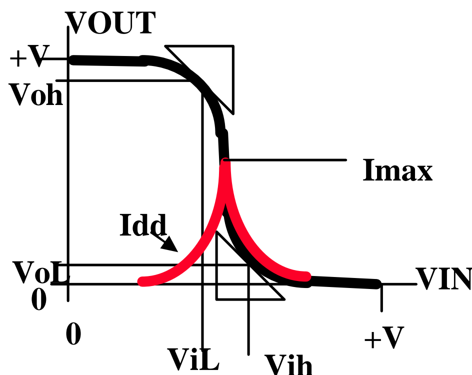
D1 noise margin=VoH-ViH

INVERTER TEST SETUP

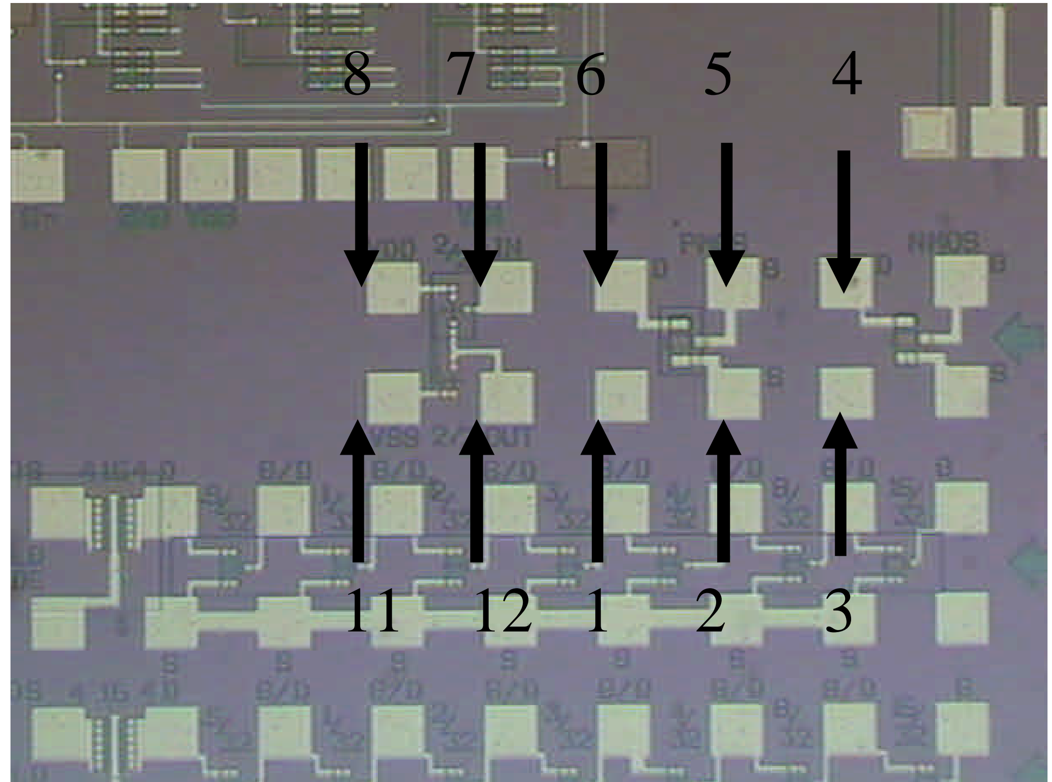
Test Name: INV



Switch matrix



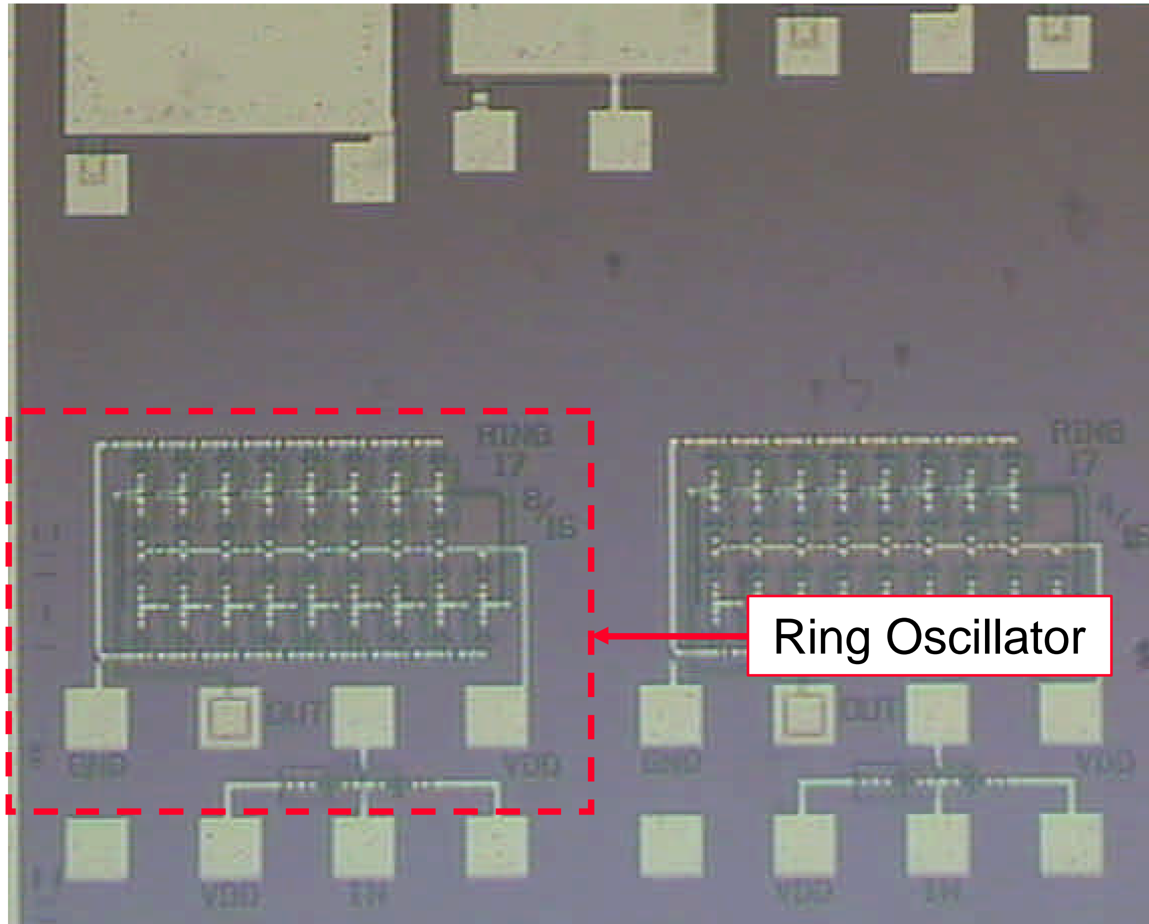
D0 noise margin=ViL-VoL
D1 noise margin=VoH-ViH



SMU1	Vdd	Constant +5 V
SMU2	Vin	Sweep 0 to +5V, 101 steps
SMU3	Vout	I mode, measure Vout
SMU4	Com	0 Volts

Extract: Voh, Vol, Vih, Vil, Vinv, Imax, Gain

TE03 RING OSCILLATOR



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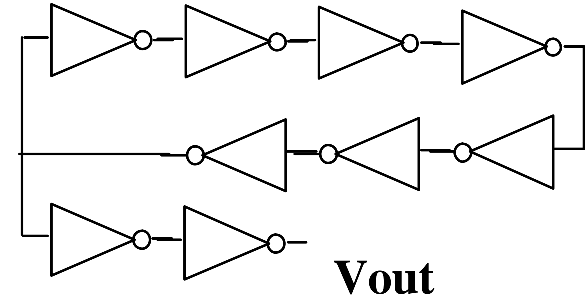
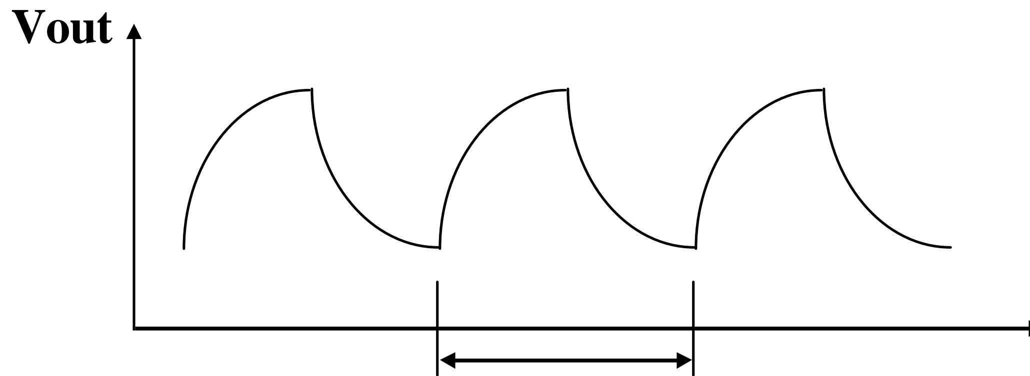
RING OSCILLATOR, td

Seven stage ring oscillator with two output buffers

td = T / 2 N

td = gate delay
N = number of stages
T = period of oscillation





T = period of oscillation

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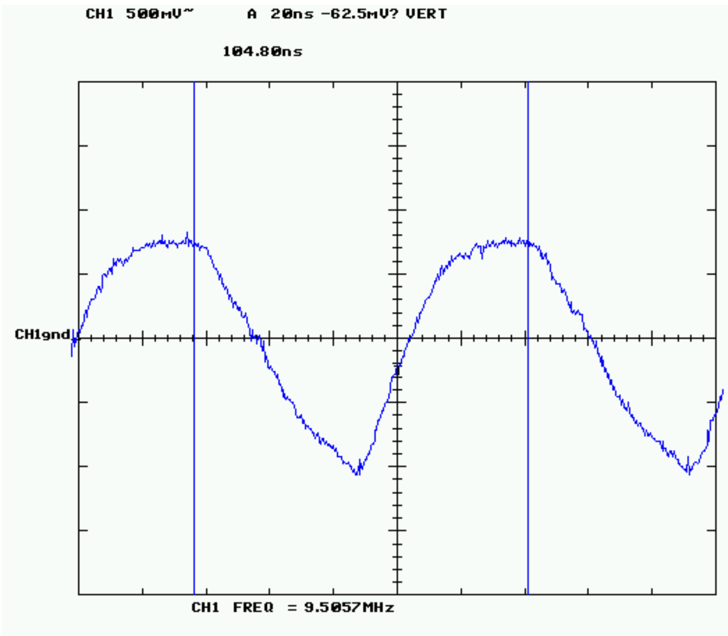
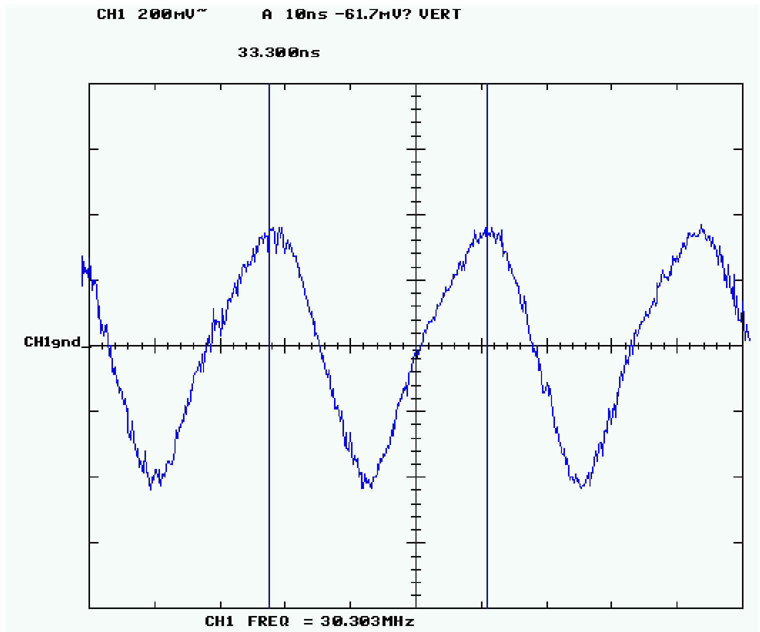
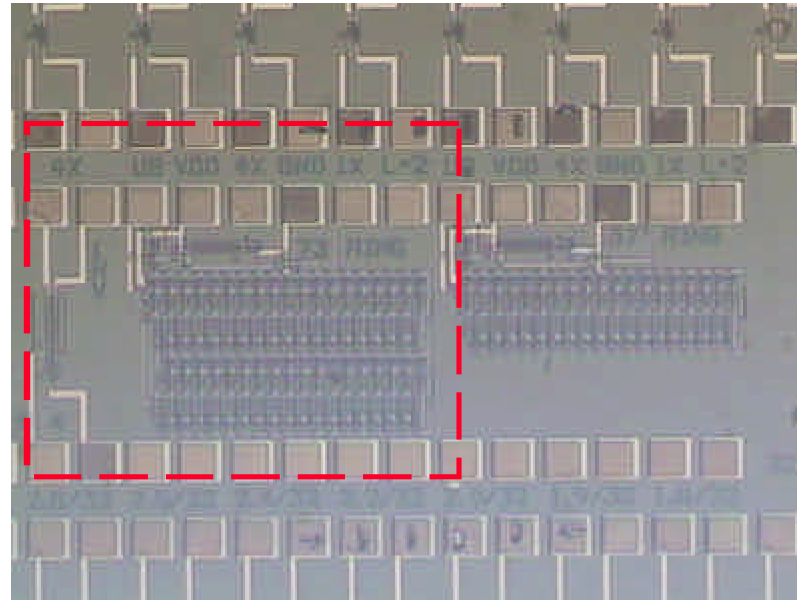


73 Stage Ring at 5V, td = 0.712ns



73 Stage Ring at 6V, td = 0.228ns

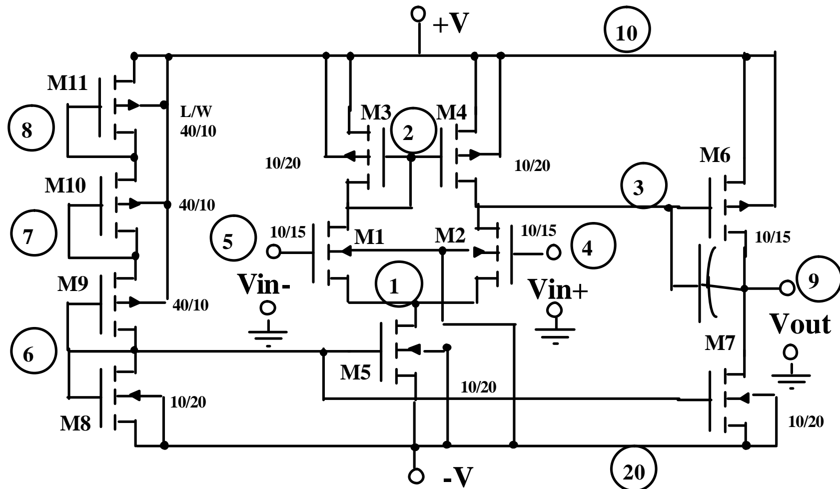


TE03 INSTRUCTIONS

- Move to manual probe station.
- Place wafer on stage and apply vacuum.
- Move stage such that Ring Oscillator is in the field of view.
- Move manual probes to make contact with the "GND", "OUT", and "VDD" probe pads.
- Use a DC power supply to supply 5 V to VDD, and 0 V to GND.
- Use the oscilloscope to view & measure the frequency.
- 17, 37 or 73 stages.

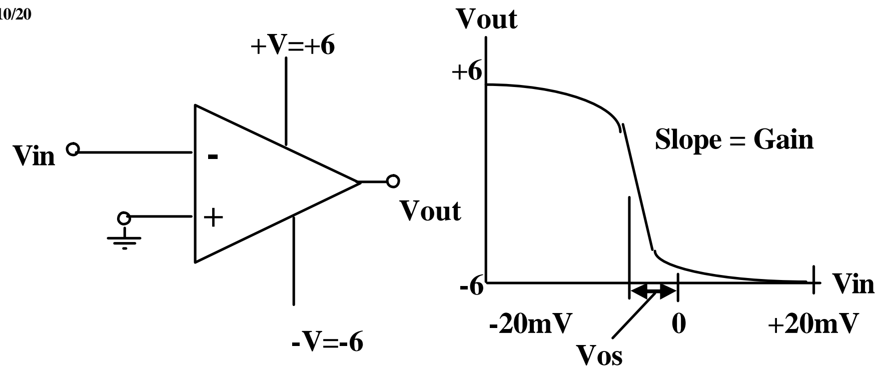
Output:
Open Folder name: Textronixoutput on desktop
Open Program 7470 (DOS)
Click Aquire; Request address number 7
Data will download to computer and plot will update
Print plot or save as: filename.gif

OPERATIONAL AMPLIFIER



p-well CMOS

dimensions
L/W
(µm/µm)



Set up the HP 4145 to sweep the Vin from -20 mV to +20 mV in 0.001V steps. Measure Gain and Input offset voltage.

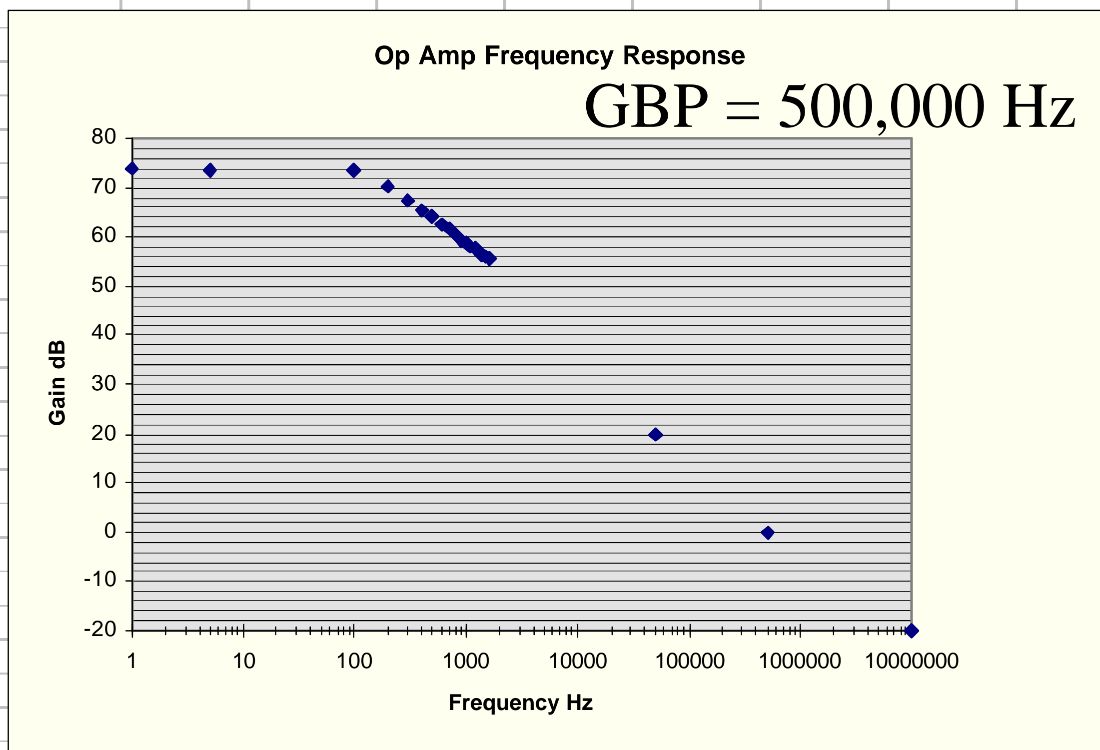
AC TEST RESULTS

ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

LFF OPAMP.XLS FILE3B

LOT F960319 OPAMP TEST RESULTS - 1-29-97

Frequency hZ	Gain dB	Vout V	Vin mV
1	73.9794	10	2
5	73.53387	9.5	2
100	73.33036	9.28	2
200	70.31748	6.56	2
300	67.53154	4.76	2
400	65.48316	3.76	2
500	63.97314	3.16	2
600	62.41148	2.64	2
700	61.51094	2.38	2
800	60.34067	2.08	2
900	59.46256	1.88	2
1000	58.68997	1.72	2
1100	58.0618	1.6	2
1200	57.50123	1.5	2
1300	57.14665	1.44	2
1400	56.5215	1.34	2
1500	56.1236	1.28	2
1600	55.56303	1.2	2
50000	20	0.02	2
500000	0	0.002	2
10000000	-20	0.0002	2



TE04

```
   5/04/06                         MESA                      IGMSINQ     S36801
   8:38:46               Instruction Group Inquiry           QPADEV000W    RIT

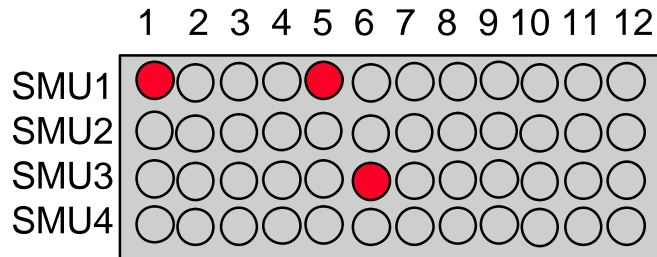
Type information.  Then Enter.
  1=Display document, 5=Display detail

  Plant . . . . . . . . . :     RIT
  Instruction group . .         TE04                 WAFER MAP OF VT
    Revision . . . . . . .      ____

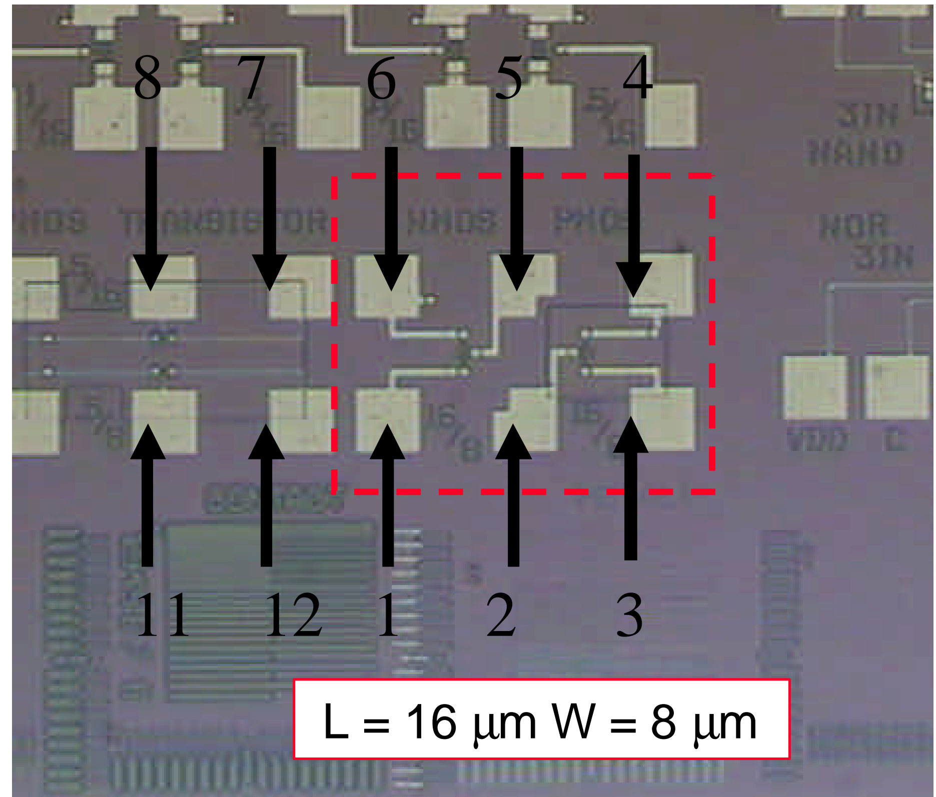
  Opt Subgroup   Text
   _             1.0 Take data for wafer map of Vt, test all transistors
   _             (see wafermap.pps)
   _             2.0 Compute +/- 10%, 20%, 30%, 40% of target:
   _                   CMOS Targets are +/-1.0, PMOS Target is -2.0 volts
   _                   Record data row by row, each character in a row
   _                   represents a different column (die), the value will be
   _                   5 if within 10% of target
   _                   4 if between -20% and -10% of target
   _                   6 if between +10% and +20% of target
   _                   3 if between -30% and -20% of target, etc.
                                                                         Bottom
F3=Exit   F4=Prompt   F5=Refresh   F10=View 2   F12=Cancel
```

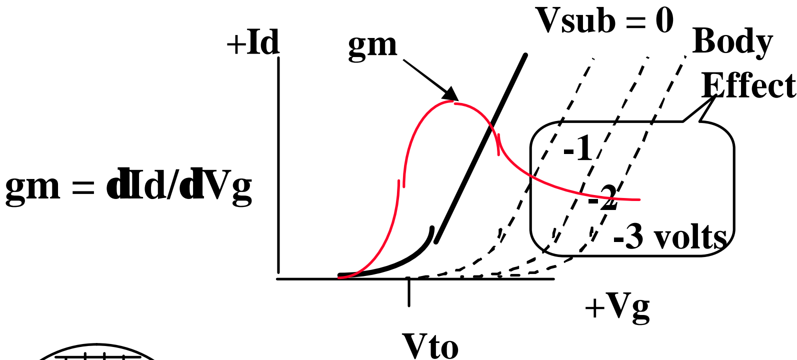
NMOS ID-VGS

Test Name: NVT



Switch matrix





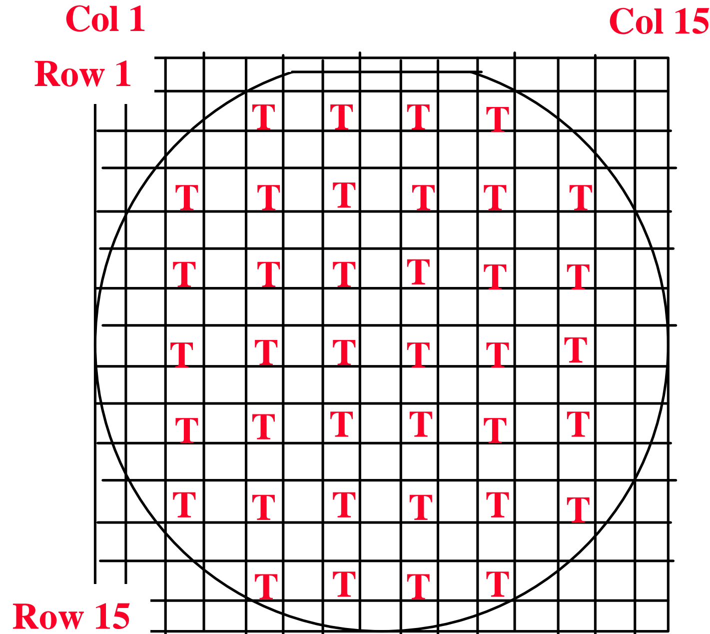
SMU1	Vgs	Sweep 0- 5 V, 101 steps
SMU2		
SMU3	Com	Vs = 0
SMU4		

Extract: Vto

TE04 INSTRUCTIONS – WAFER MAP

- **Measure Vt for NFET on each die in a 15 x 15 array centered on the wafer.**
- **Record information in MESA and on an excel spreadsheet using the Binning described in below.**

Code	
0	no die
1	value<(Target-70%)
2	(Target-70%)<value<(Target-50%)
3	(Target-50%)<value<(Target-30%)
4	(Target-30%)<value<(Target-10%)
5	(Target-10%)<value<(Target+10%)
6	(Target+10%)<value<(Target+30%)
7	(Target+30%)<value<(Target+50%)
8	(Target+50%)<value<(Target+70%)
9	(Target+70%)<value

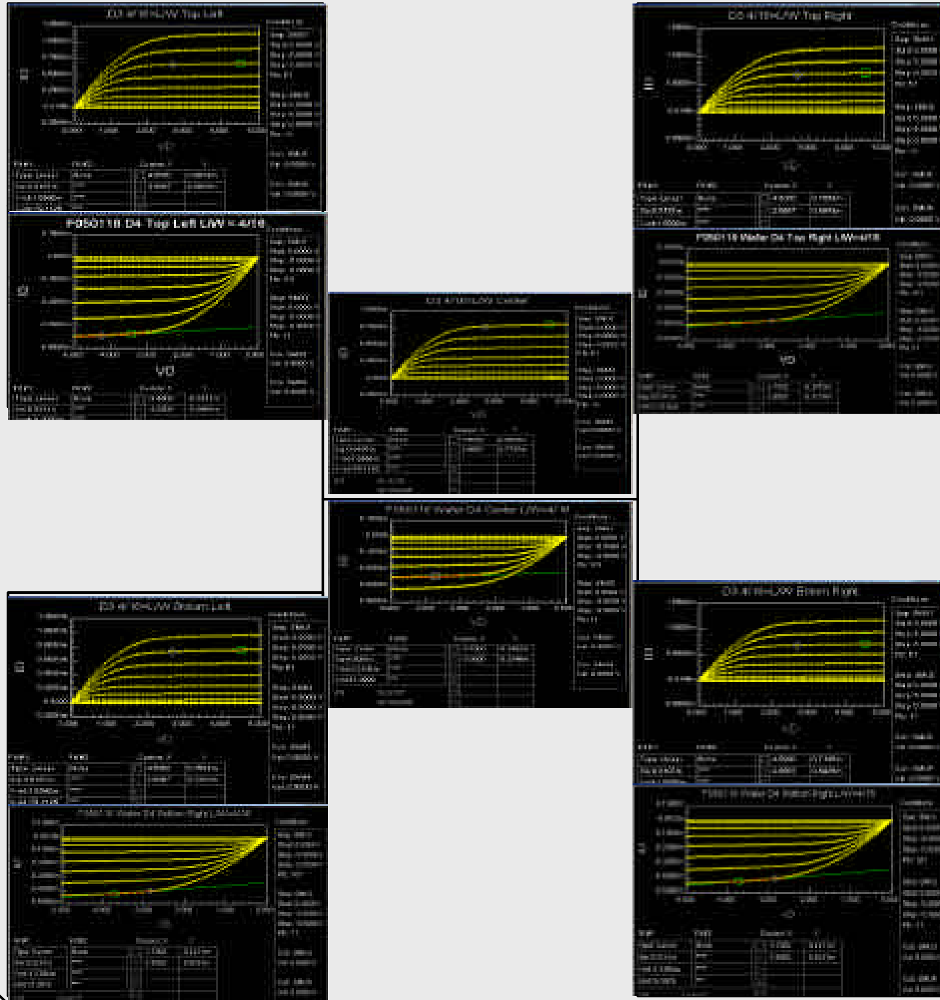


Example Data

nmos Vt target +1
000000000000000
000050505050000
000000000000000
005060507050700
000000000000000
004040304030300
000000000000000
004040404040400
000000000000000
004050405090600
000000000000000
005050606060700
000000000000000
000050505050000
000000000000000

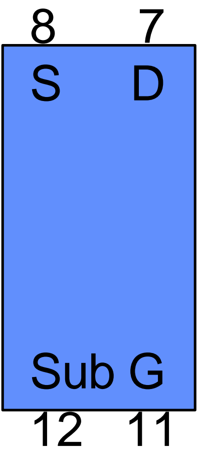
Lot Number = F050118
Wafer Number = D3

Family of curves for L=4µm MOSFETs

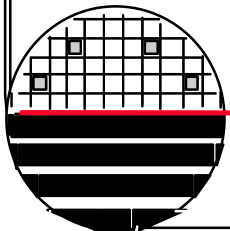


2µm/32µm L/W NMOS AND PMOS

SMFL CMOS DAC TEST STRUCTURES



2/16 L/W NMOS FET



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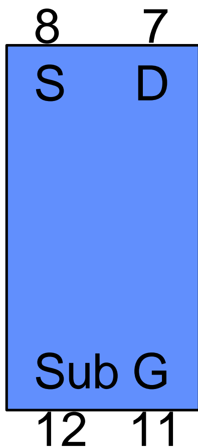
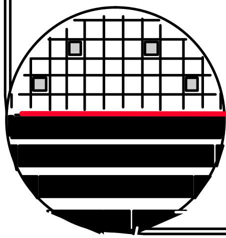
SMFL CMOS DAC TEST STRUCTURES

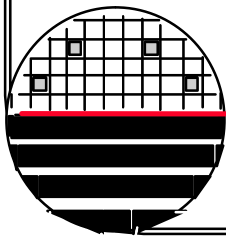


2/16 L/W PMOS FET

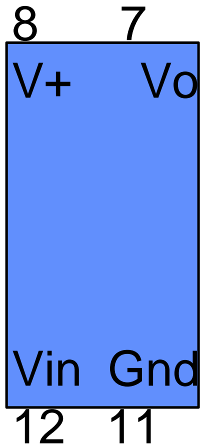


SMFL CMOS DAC TEST STRUCTURES

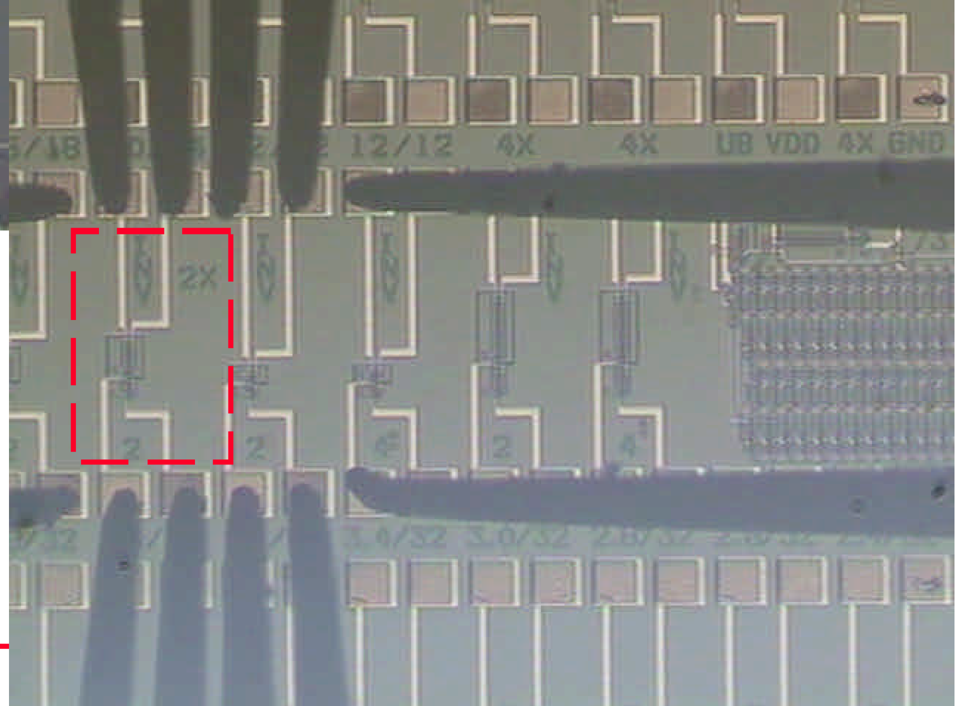
VAN DER PAUW AND CBKR

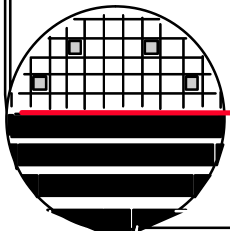


SMFL CMOS DAC TEST STRUCTURES

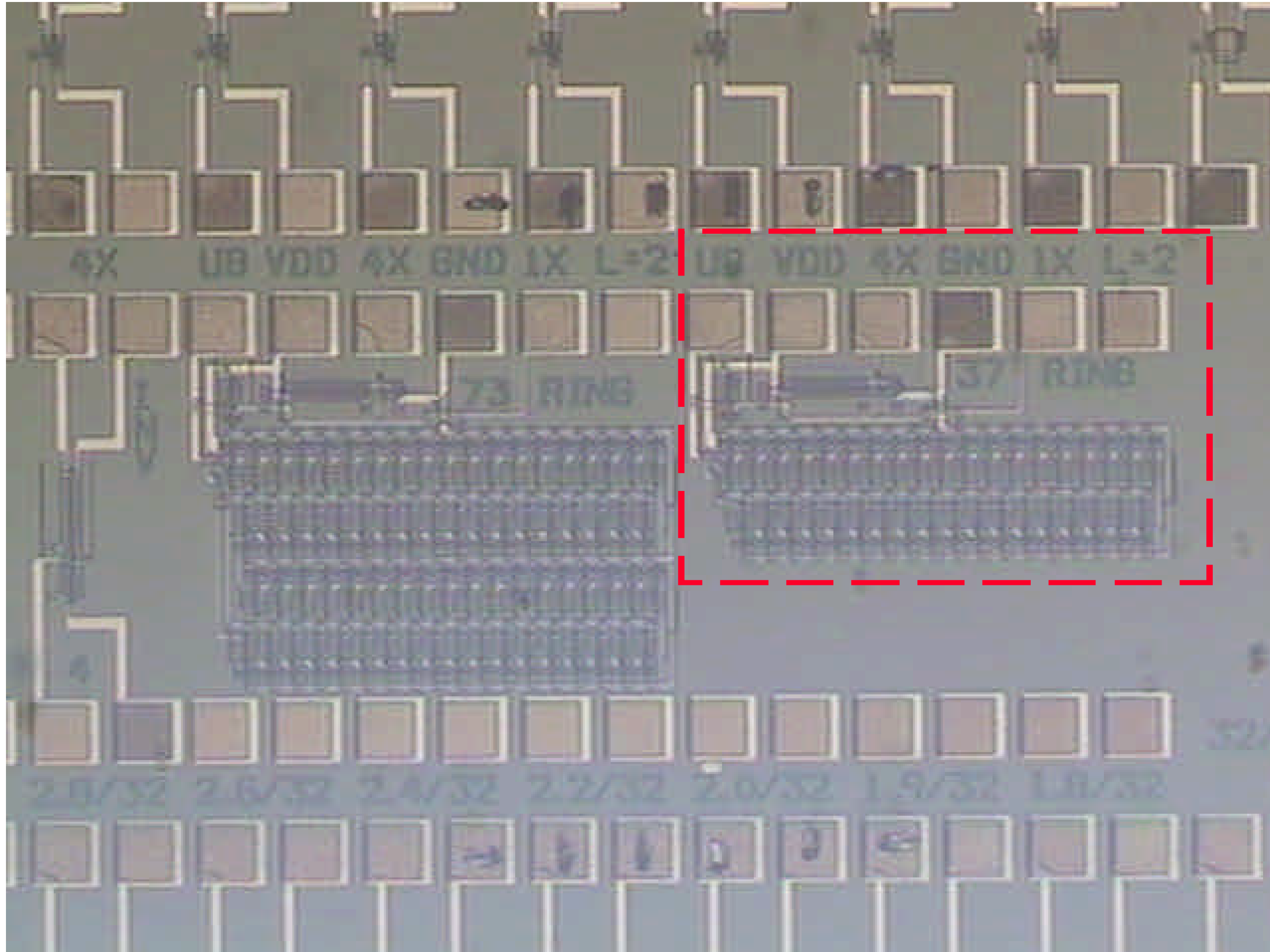


L = 2um INVERTERS





SMFL CMOS DAC TEST STRUCTURES



37 STAGE 2um RING OSCILLATOR

Rochester Institute of Technology
Microelectronic Engineering