CMOS Testchip 2009

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1-2-2010 CMOSTestchip2009.ppt

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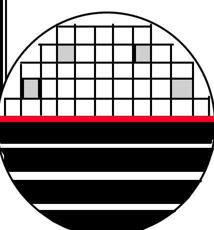
OUTLINE

Introduction
Process Technology
Design Rules
Chip Floor Plan
Structures for Fabrication Process and Evaluation
Sensors
Digital Circuits
Analog Circuits
Projects
References



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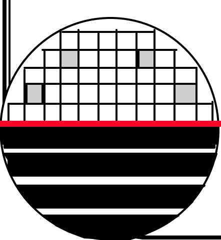
INTRODUCTION

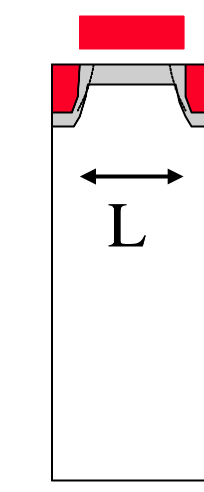
This document will describe a new CMOS test chip. The test chip will be used to develop CMOS process technology and to verify analog and digital circuit designs. In addition the test chip includes a variety of CMOS compatible sensors and signal processing electronics for those sensors. A section of the chip is for manufacturing process characterization and transistor parametric characterization. Other sections of the chip have basic digital and analog circuits, chip scale packaging designs and projects to evaluate various Microsystems architectures. For example a variable frequency oscillator, binary counter and shift register allows for capacitor sensor measurement and Blue-Tooth wireless transmission of data to a remote host. The test chip will be used with RIT's SUB-CMOS and ADV-CMOS processes.



RIT SUBμ CMOS

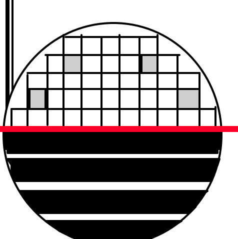
RIT Subμ CMOS

150 mm wafers
Nsub = 1E15 cm-3
Nn-well = 3E16 cm-3
Xj = 2.5 μm
Np-well = 1E16 cm-3
Xj = 3.0 μm
LOCOS
Field Ox = 6000 Å
Xox = 150 Å
Lmin= 1.0 μm
LDD/Side Wall Spacers
2 Layers Aluminum



Long
Channel
Behavior

3.3 Volt Technology
VT's = +/- 0.75 Volt
Robust Process (always works)
Fully Characterized (SPICE)



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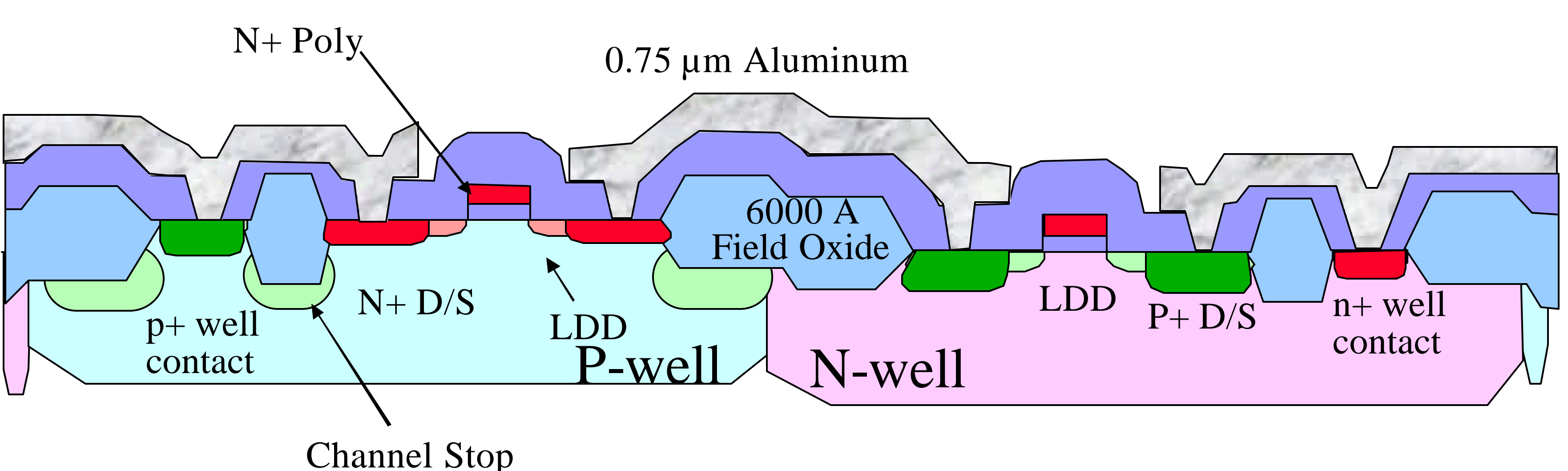
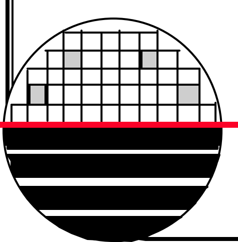
RIT SUBμ CMOS



N-type Substrate 10 ohm-cm



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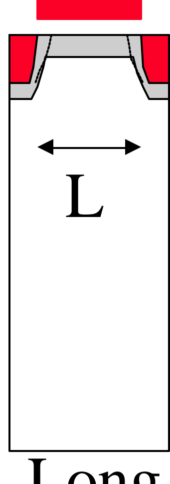
RIT ADVANCED CMOS VER 150

RIT Advanced CMOS

150 mm Wafers
Nsub = 1E15 cm-3 or 10 ohm-cm, p
Nn-well = 1E17 cm-3
Xj = 2.5 µm
Np-well = 1E17 cm-3
Xj = 2.5 µm
Shallow Trench Isolation
Field Ox (Trench Fill) = 4000 Å
Dual Doped Gate n+ and p+
Xox = 100 Å
Lmin = 0.5 µm , Lpoly = 0.35 µm, Leff = 0.11 µm
LDD/Nitride Side Wall Spacers
TiSi2 Salicide
Tungsten Plugs, CMP, 2 Layers Aluminum



Long Channel Behavior

Vdd = 3.3 volts
Vto=+- 0.75 volts

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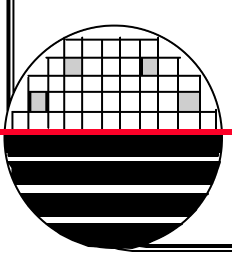
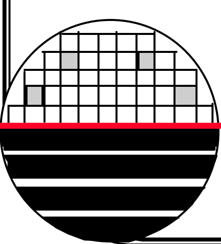
RIT ADVANCED CMOS



DESIGN RULES

We will use a modified version of the MOSIS TSMC 0.35 2P 4M design rules. Eventually we hope to be compatible with MOSIS but new process technology needs to be developed at RIT to do that (PECVD Tungsten, improved lithography overlay, 4 layer metal). We plan to use one layer of poly and two layers of metal. We will use the same design layer numbers with additional layers as defined on the following pages for manufacturing/maskmaking enhancements. Many of the designs will use minimum drawn poly gate lengths of 2µm where circuit architecture is the main purpose of the design. Minimum size devices (Drawn Poly = 0.5µm, etc.) are included to develop manufacturing process technology. These transistors (0.5µm drawn) yield 0.35µm Leff and are equivalent to the TSMC 0.35µm transistors.



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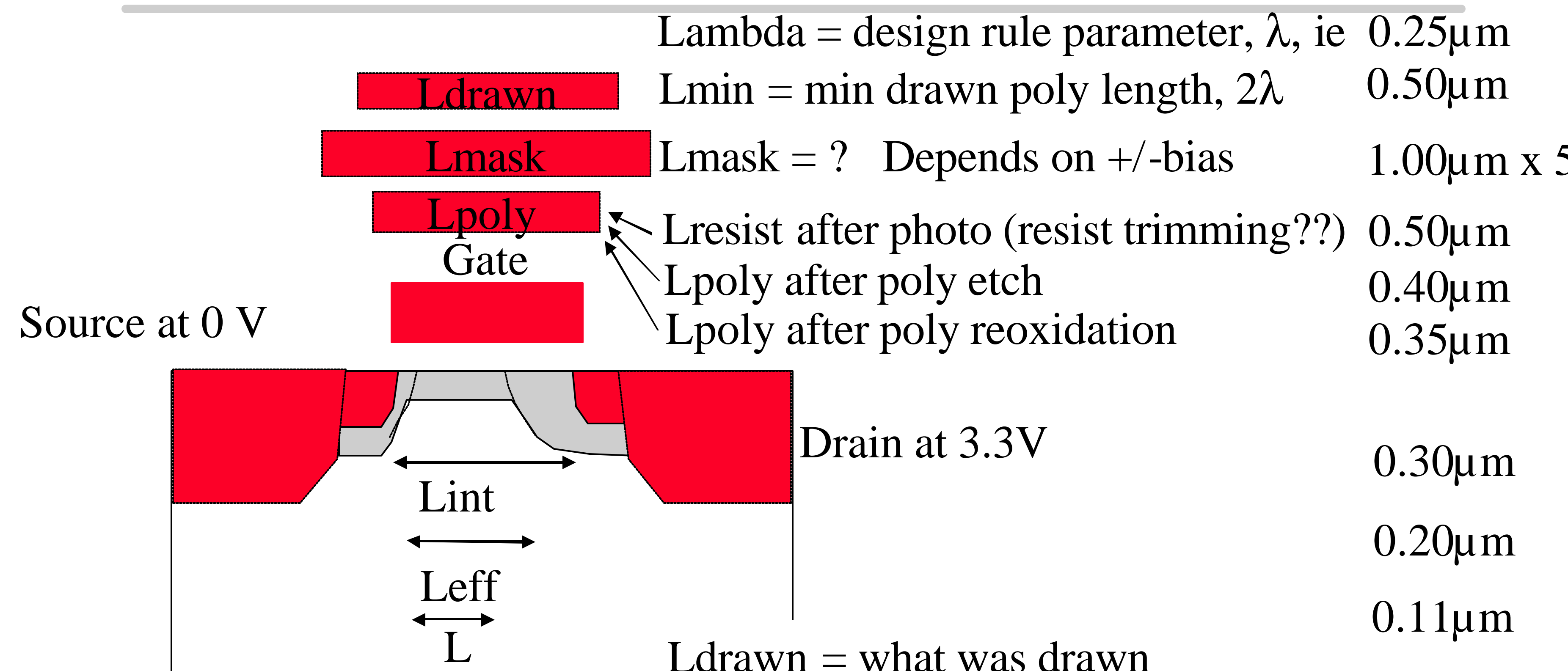
LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L



Internal Channel Length, Lint =distance between junctions, including under diffusion
Effective Channel Length, Leff = distance between space charge layers,Vd = Vs= 0
Channel Length, L, = distance between space charge layers, when Vd= what it is
Extracted Channel Length Parameters = anything that makes the fit good (not real)

MOSIS TSMC 0.35 2POLY 4 METAL PROCESS

http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html#tech-codes

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Project Status
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MOSIS SCMOS Technology Codes and Layer Maps

SCN4M and SCN4M_SUBM

This is the layer map for the technology codes SCN4M and SCN4M_SUBM using the MOSIS Scalable CMOS layout rules (SCMOS), and only for SCN4M and SCN4M_SUBM. For designs that are laid out using other design rules (or technology codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

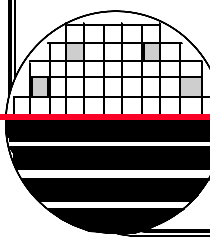
SCN4M: Scalable CMOS N-well, 4 metal, 1 poly, silicided. Silicide block and thick oxide option available only on the TSMC process.

SCN4M_SUBM: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

Fabricated on TSMC, AMIS, and Agilent/HP 0.35 micron process runs. See "Notes" section of layer map for foundry-specific options.

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	
ACTIVE	43	CAA		2	
THICK_ACTIVE	60	CTA		24	Optional for TSMC; not available for Agilent/HP nor AMIS
POLY	46	CPG		3	
SILICIDE_BLOCK	29	CSB		20	Optional for Agilent/HP; not available for AMI
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	
METAL3	62	CM3	CMT	15	
VIA3	30	CV3	CVT	21	
METAL4	31	CM4	CMQ	22	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME



MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

MASK LAYER NAME	MENTOR NAME	GDS #	COMMENT
N WELL	N_well.i	42	
ACTIVE	Active.i	43	
POLY	Poly.i	46	
N PLUS	N_plus_select.i	45	
P PLUS	P_plus_select.i	44	
CONTACT	Contact.i	25	Active_contact.i 48 poly_contact.i 47
METAL1	Metal1.i	49	
VIA	Via.i	50	
METAL2	Metal2.i	51	
VIA2	Via2.i	61	Under Bump Metal
METAL3	Metal3.i	62	Solder Bump

These are the main design layers up through metal two

MORE LAYERS USED IN MASK MAKING

LAYER	NAME	GDS	COMMENT
	cell_outline.i	70	Not used
	alignment	81	Placed on first level mask
	nw_res	82	Placed on nwell level mask
	active_lettering	83	Placed on active mask
	channel_stop	84	Overlay/Resolution for Stop Mask
	pmos_vt	85	Overlay/Resolution for Vt Mask
	LDD	86	Overlay/Resolution for LDD Masks
	p plus	87	Overlay/Resolution for P+ Mask
	n plus	88	Overlay/Resolution for N+ Mask
	tile_exclusion	89	Areas for no STI tiling

These are the additional layers used in layout and mask making

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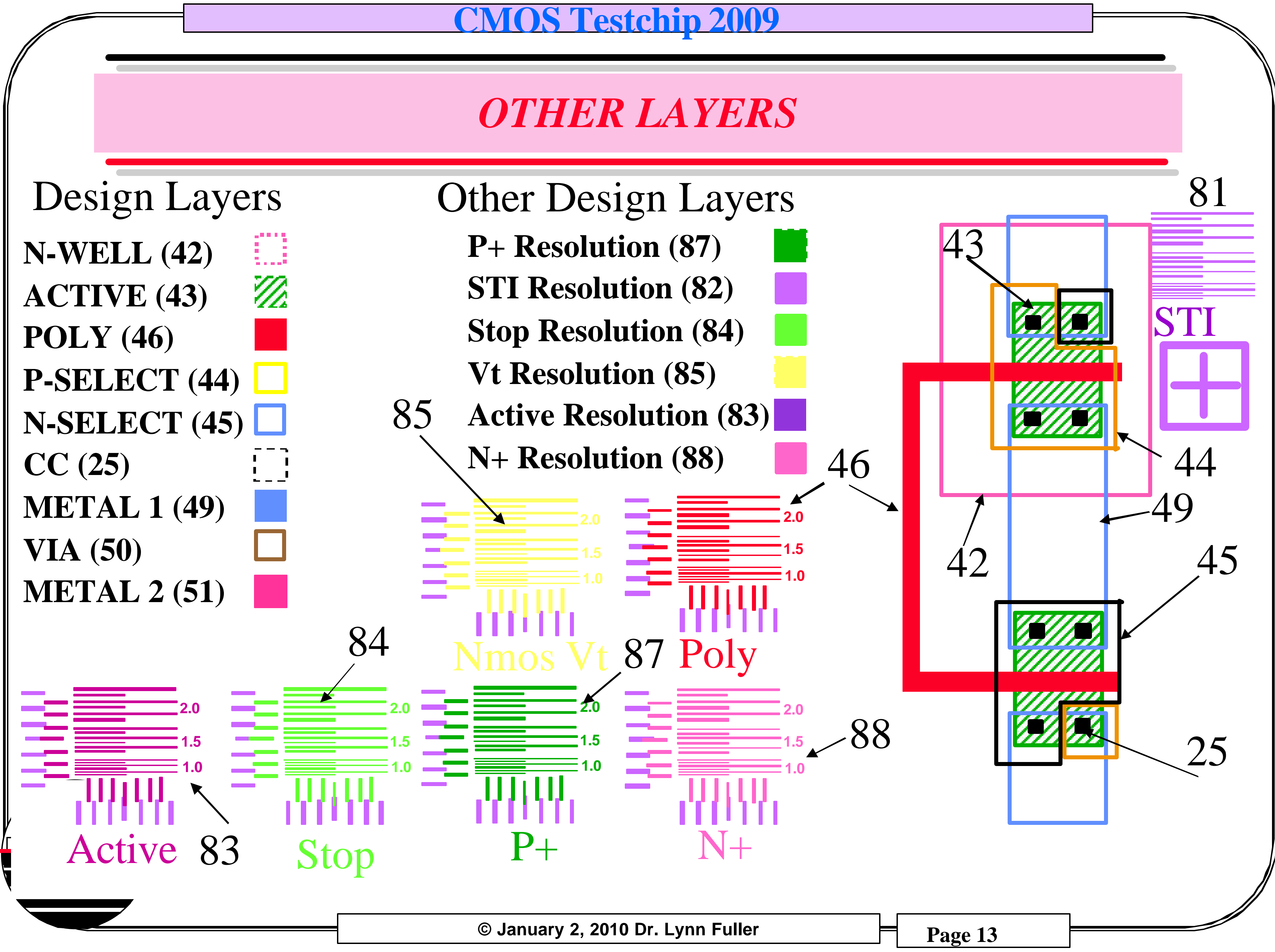
OTHER LAYERS



MASK ORDER FORM

Rochester Institute of Technology
Microelectronic Engineering

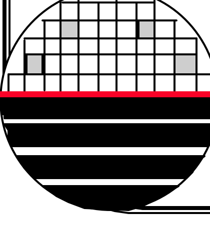
Date 6/25/2008
Requester Dr. Lynn Fuller

Attachment for Mask Order Form

Design Descripti CMOS_TESTCHIP_2008_final **gds File:** /shared/cmostestchip_2007/CMOS_TESTCHIP_2008_final.g

cture Resolution	0.5	**Mirror**	135	**Plate Size**	5"x5"x0.090"
Scale Factor	5X	**Rotate**	none	**# of levels/plate**	1
Array	none				

Design Layer Name	Design Layer Number	Mask Level Name	Mask Level Number	Boolean Function	Comments
NWELL	1	n-well.i	42	(42 OR 81 OR 82) INVERT	Dark Field Mask
		alignment	81		
		nw_res	82		
ACTIVE	2	active-area.i	43	(43 OR 83)	Clear Field Mask
		active-area.e	83		
STOP	3	n-well.i	42	(42 OR 84)	Clear Field Mask
		channel_stop	84		
PMOSVT	4	p_plus_select.i	44	(44 OR 85)	Dark Field Mask
		pmos_vt	85		
POLY	5	poly.i	46	none	Clear Field Mask, Bias layer 6 +0.5µm
LDD-N	6	n_plus_select.i	45	(45 OR 86) INVERT	Dark Field Mask
		LDD	86		
LDD-P	7	p_plus_select.i	44	(44 OR 86) INVERT	Dark Field Mask
		LDD	86		
N+DS	8	n_plus_select.i	45	(45 OR 88) INVERT	Dark Field Mask
		n plus	88		
P+DS	9	p_plus_select.i	44	(44 OR 87) INVERT	Dark Field Mask
		p plus	87		
CC	10	contact	25	(25 OR 87 OR 47) INVERT	Dark Field Mask
		Active_contact	48		
		Poly_contact.i	47		
METAL1	11	metal1.i	49	none	Clear Field Mask
VIA	12	Via.i	50	INVERT	Dark Field Mask
METAL2	13	metal2.i	51	none	Clear Field Mask
VIA2	14	Via2	61	none	Dark Field Mask
METAL3	15	metal3	62	none	Clear Field Mask



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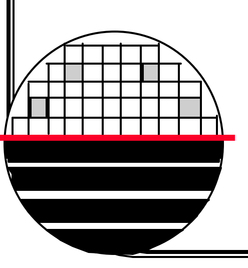
FLOORPLAN AND HIERARCHY

- CMOSTestchip2007
  - Process
  - Digital
    - Primitive Cells
    - Basic Cells
    - Macro Cells
  - Analog & Mixed
  - Projects
    - Packaging
    - MEMS
    - Project 1
    - Project2

Packaging Project	Packaging Project	Project 2 MEMS
Project 1	Analog and Mixed	Digital Macro Cells
Process & Manufacturing Structures	Sensors	Digital Cells

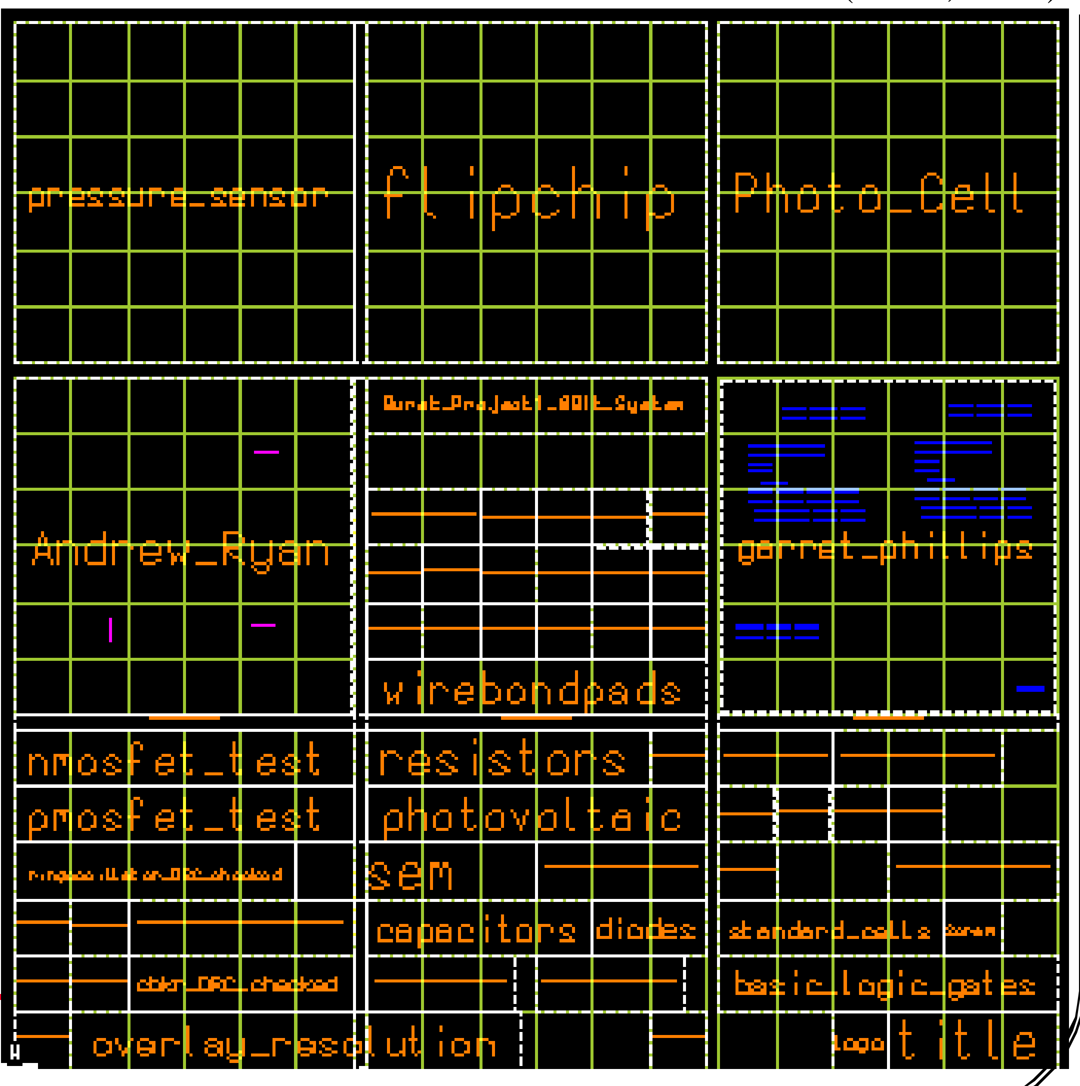
Alignment, Resolution, Overlay, Logo, Title



OVERALL CHIP LAYOUT

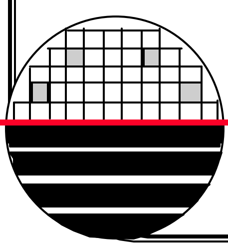
The test chip is divided into nine cells each 5 mm by 5 mm. The cells are divided into 36 individual tiny cells each 800 µm by 800 µm in size plus 200 µm sawing streets. Most structures fit into the tiny cells including a 12 probe pad layout for probe card testing. The overall chip size is 14800 µm by 14800µm plus 200 µm sawing street to give x and y step size of 15 mm by 15 mm.

(14800,14800)



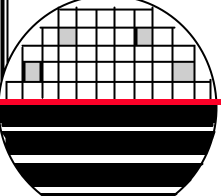
JOHN GALT CMOS TESTCHIP

2009



4-BIT MICROPROCESSOR

ANDREW RYAN
4bit
MicroProcessor



ANALOG TO DIGITAL CONVERTER

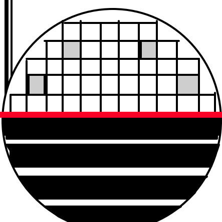
Output Register

Comp

DAC

Ref Buf

Successive Approximation Register



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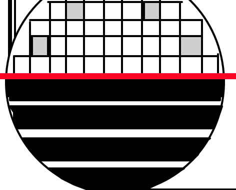
TINY CELL

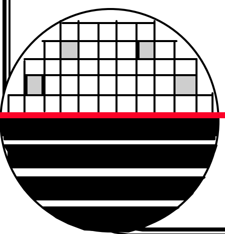
800µm by 800µm

$36 \times 9 = 324$



STRUCTURES FOR FAB PROCESS & EVALUATION

Alignment Structures
Overlay and Resolution Structures
Big areas for measurement (Big Transistors)
SEM Structures
CC Chains
Serpentines and Fingers for M1-M2 open and shorts
Van Der Pauw's
CBKR's
NMOS and PMOS Transistors of Various Sizes
Fully Scaled Sub-Micron Transistors
Field Oxide Transistors
Ring Oscillators
Package Test Structures



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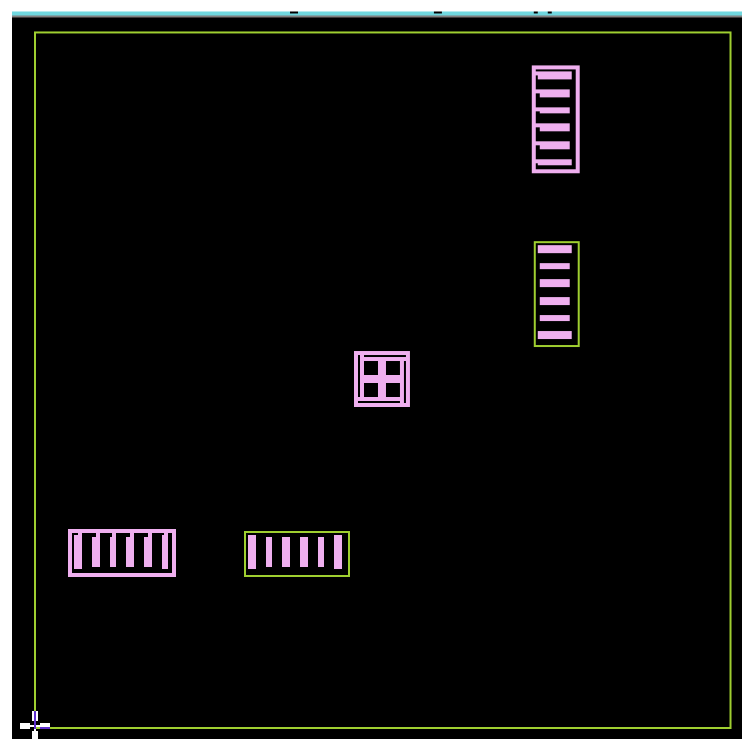
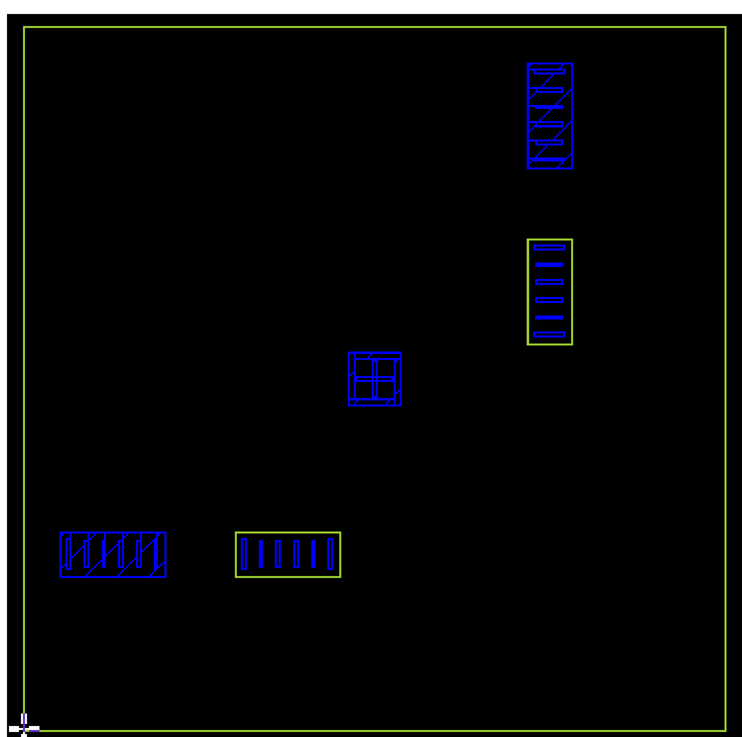
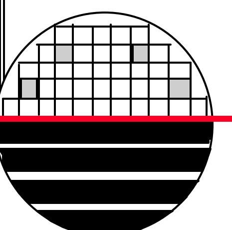
ALIGNMENT KEYS



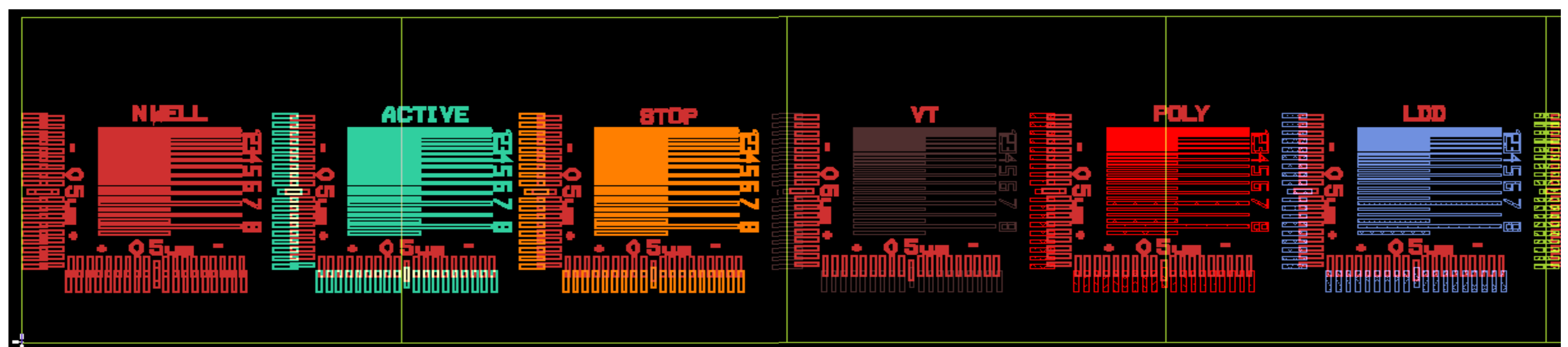
On First Level Nwell or STI

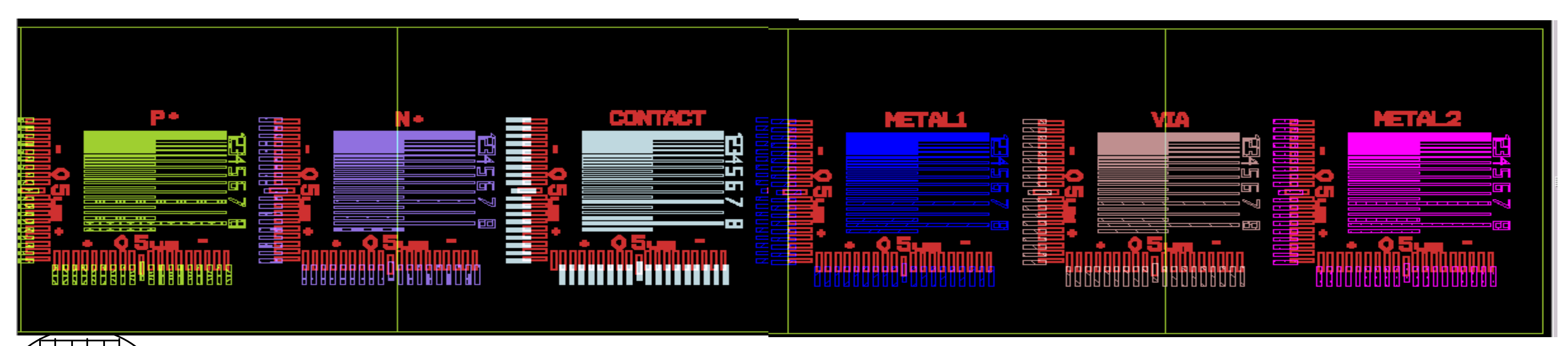


On Metal 1

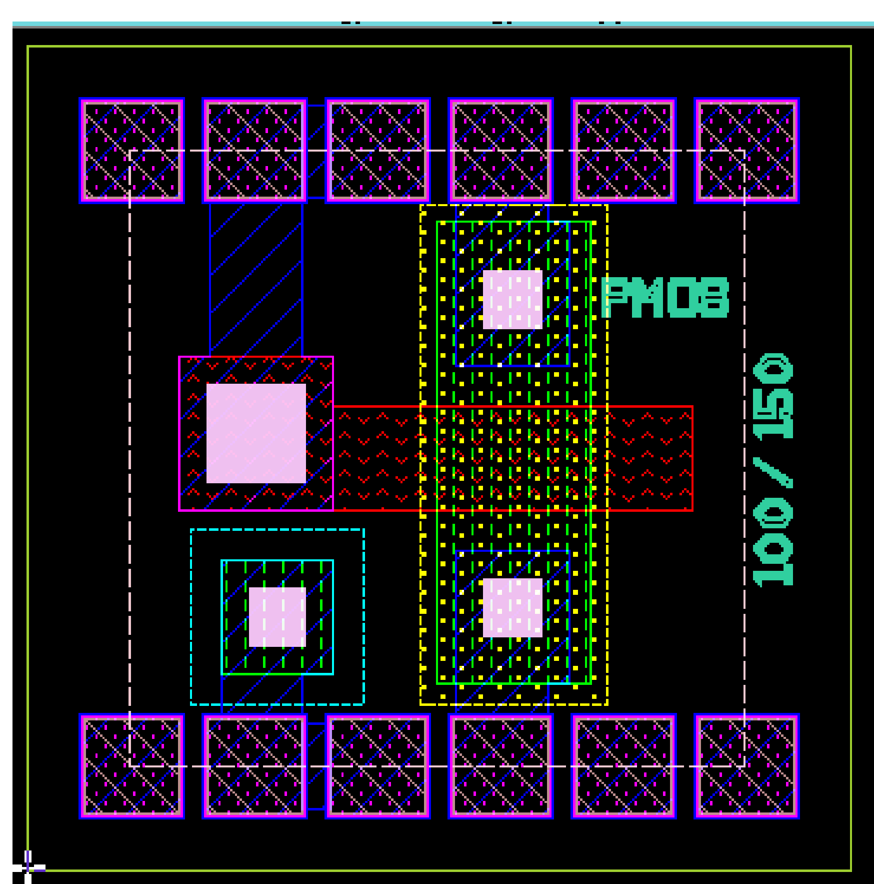


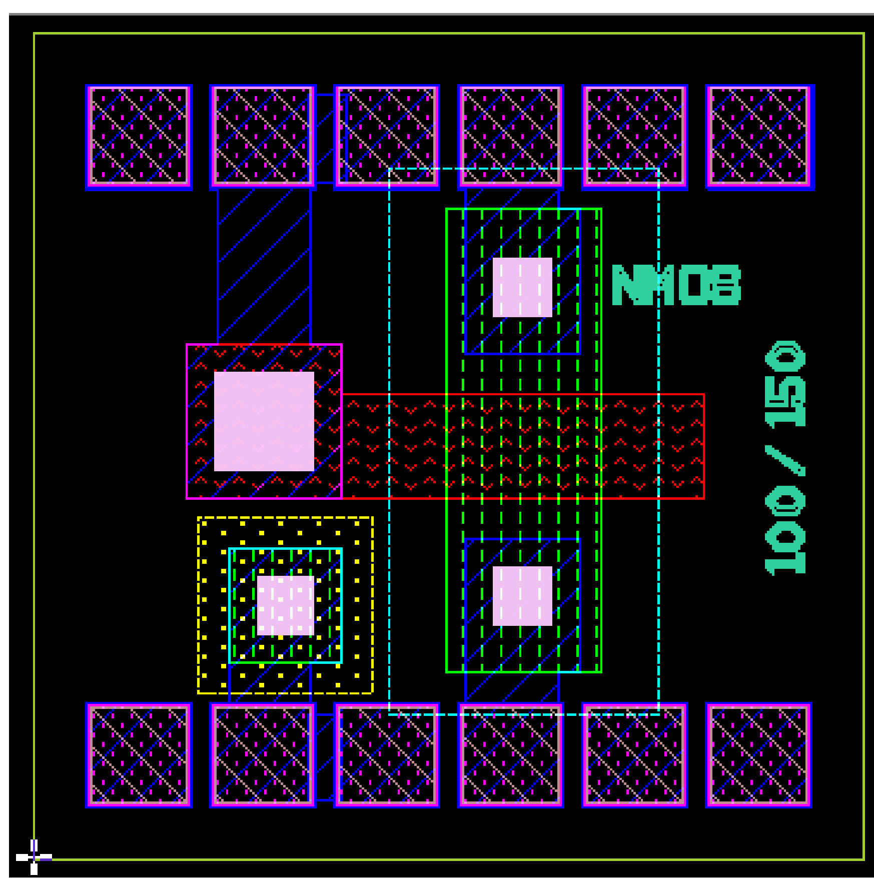
RESOLUTION AND OVERLAY





BIG NMOS AND PMOS FETS





L/W = 100µm/150µm

Big enough for easy Nanospec Measurements

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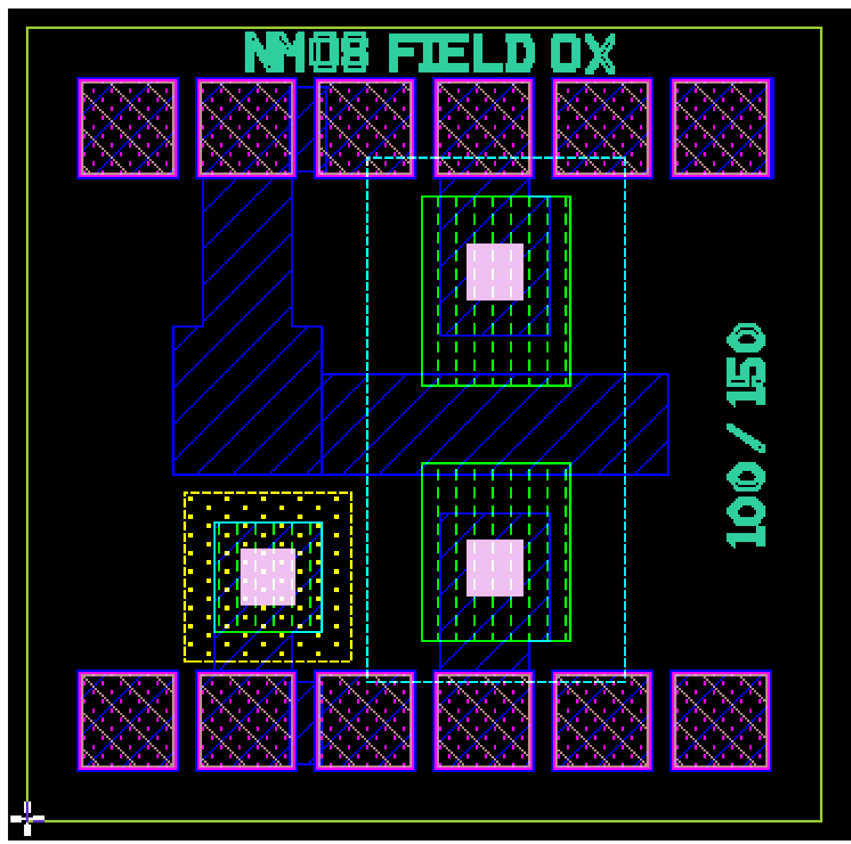
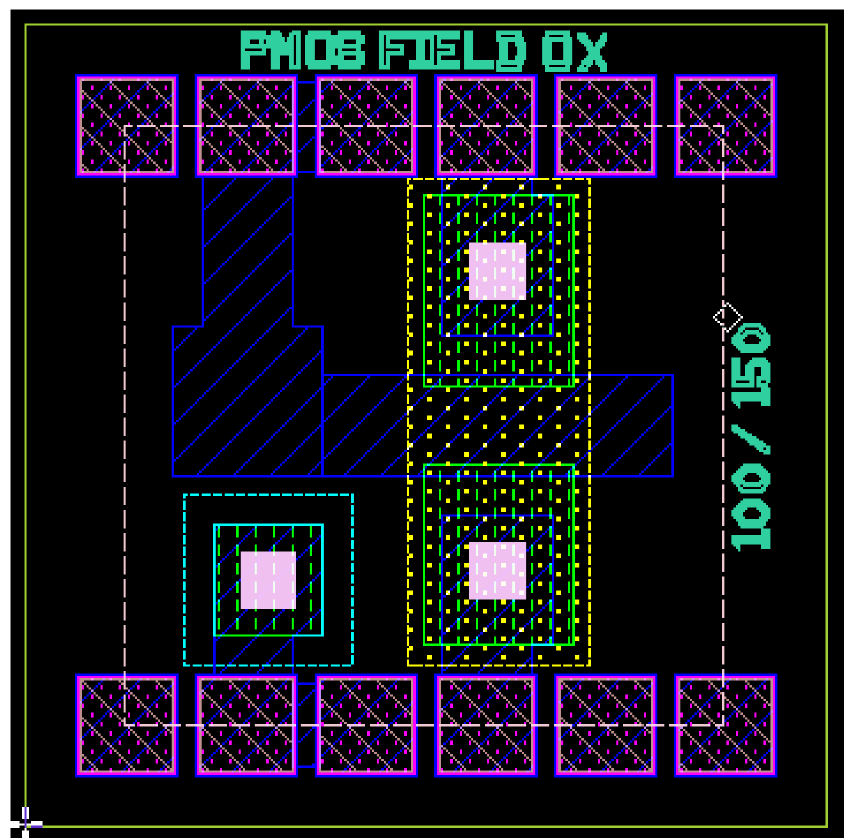
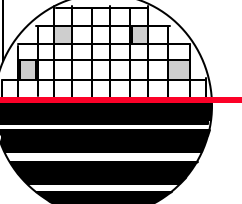
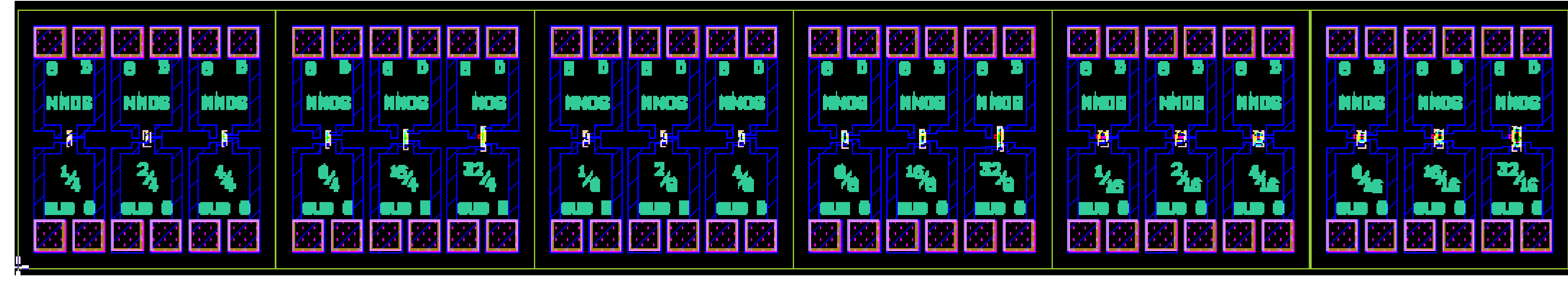
FIELD OXIDE NMOS AND PMOS FET'S





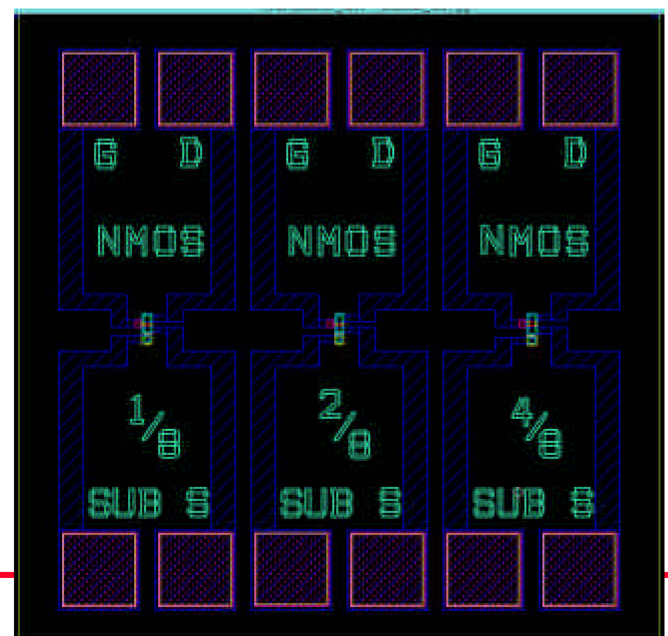


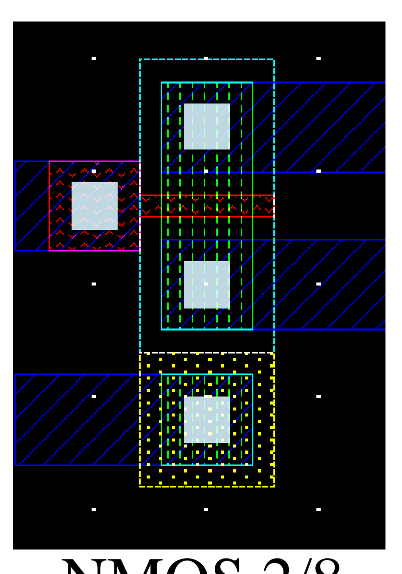
NMOS AND PMOS TRANSISTORS



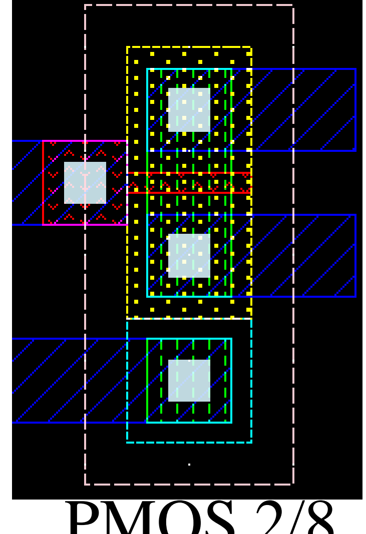
1/4 2/4 4/4 8/4 16/4 32/4 1/8 2/8 4/8 8/8 16/8 32/8 1/32 2/32 4/32 8/32 16/32 32/32

Various L/W Ratios





NMOS 2/8



PMOS 2/8

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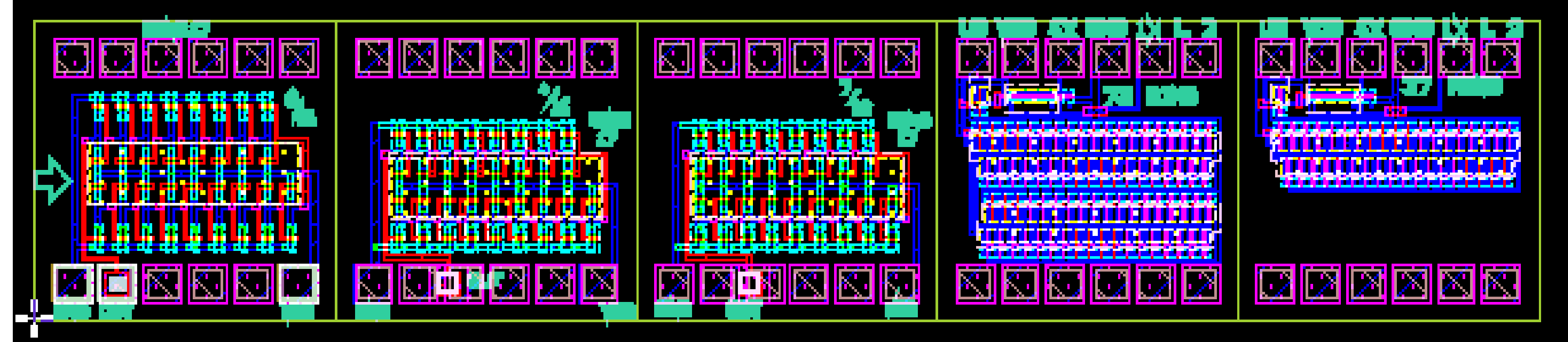
FULLY SCALED SUB MICRON TRANSISTORS

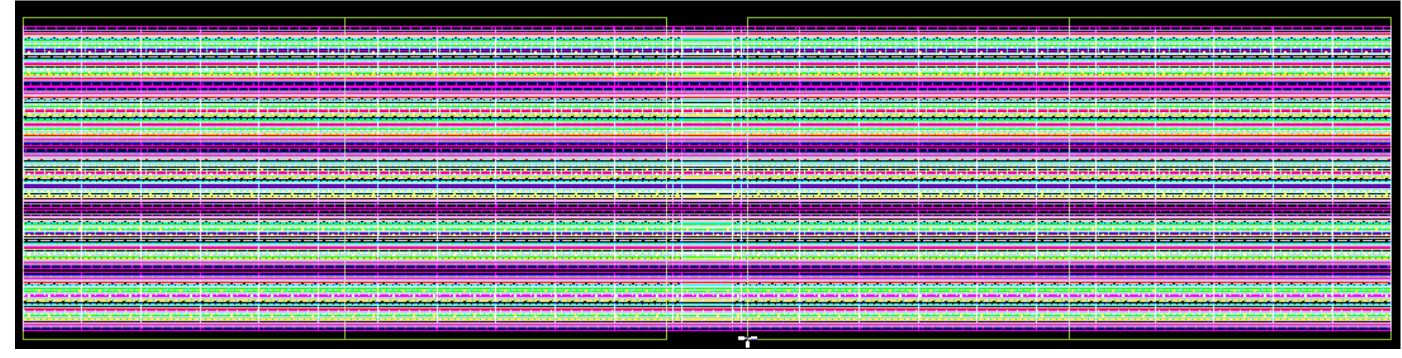
RING OSCILLATORS AND SEM STRUCTURES

17 Stage Un-buffered Output

L/W=2/30 Buffered Output



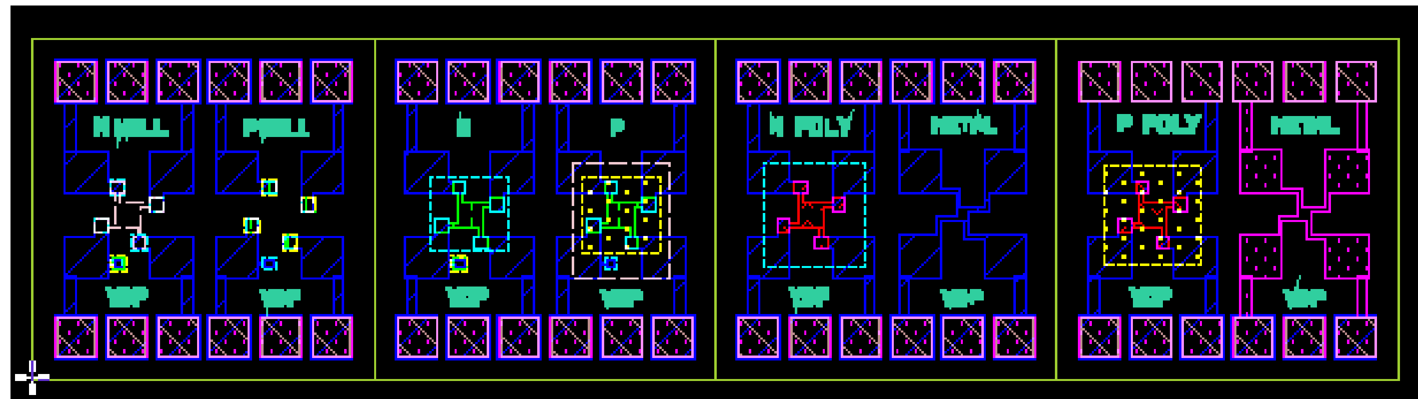
L/W 8/16 4/16 2/16 73 Stage 37 Stage



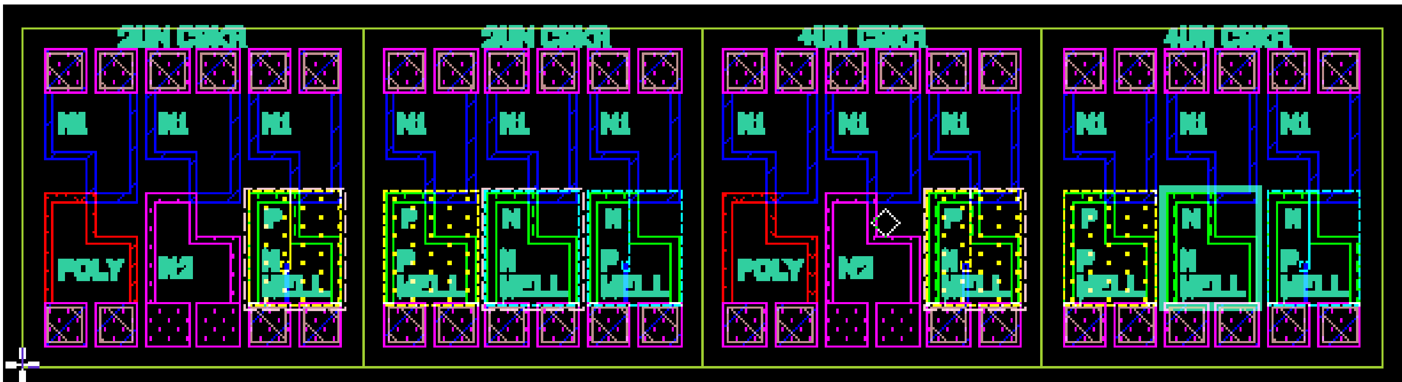
SEM Structures

CMOS Inverter Crossection

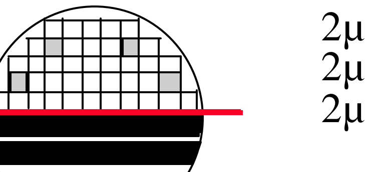
VAN DER PAUWS AND CBKR's



NWELL PWELL N+ P+ N-POLY M1 P-POLY M2



2µm M1toPoly	2µm M1toP+	4µm M1toPoly	4µm M1toP+
2µm M1toM2	2µm M1toN+	4µm M1toM2	4µm M1toN+
2µm M1toP+	2µm M1toN+	4µm M1toP+	4µm M1toN+



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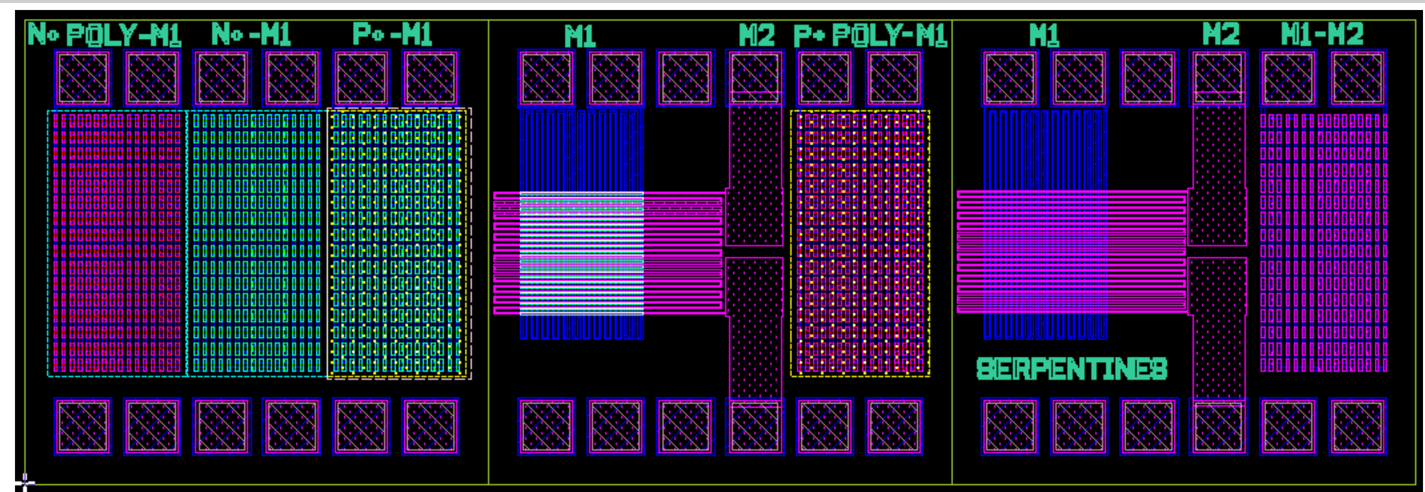
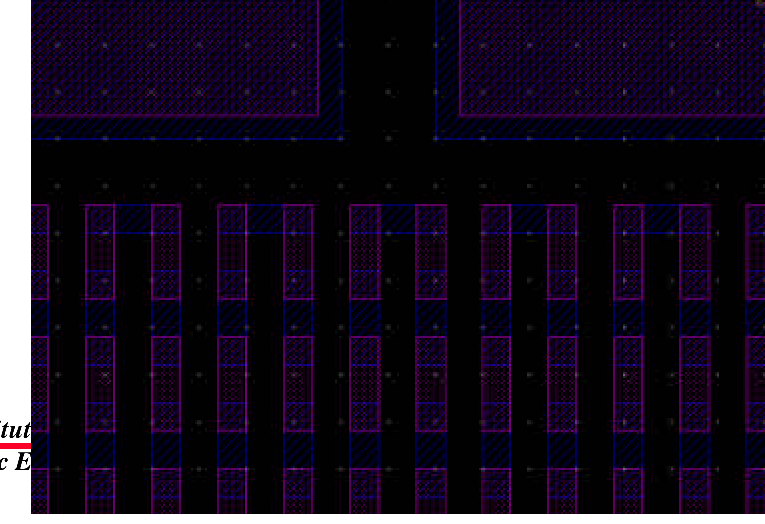
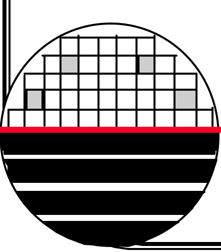
SERPENTINES, COMBS, AND VIA CHAINS



To evaluate metal1, metal2, CC and Via layer quality.

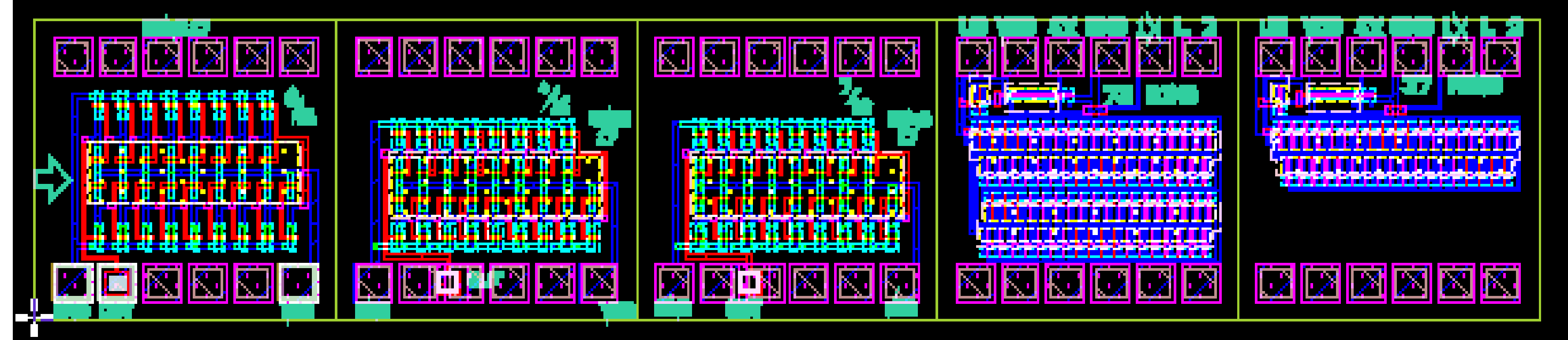




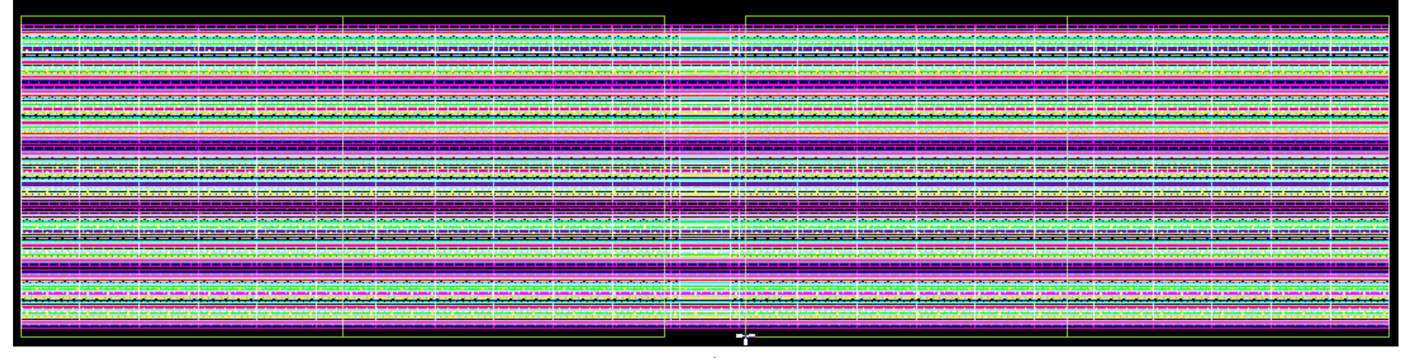
RING OSCILLATORS AND SEM STRUCTURES

17 Stage Un-buffered Output

L/W=2/30 Buffered Output



L/W 8/16 | 4/16 | 2/16 | 73 Stage | 37 Stage



SEM Structures

CMOS Inverter Crossection

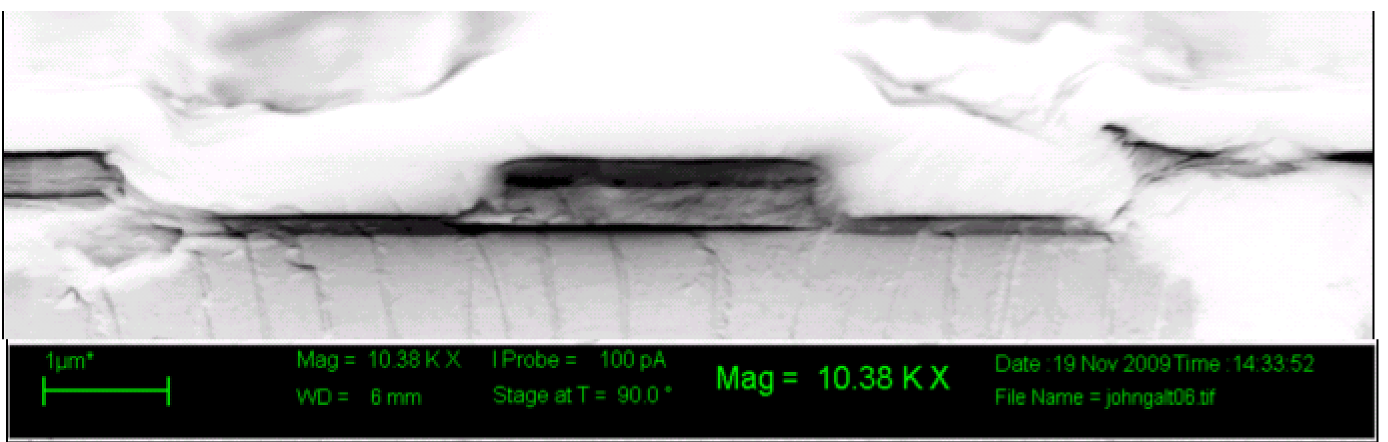
SEM CROSSECTION OF INVERTER

NMOSFET

PMOSFET

P-well

N-well



Need to polish, etch then SEM

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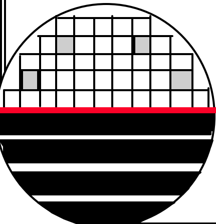
SENSORS

Interdigitated and Plate Capacitors
Diodes and Heaters
Resistors
Photovoltaic Cells, 1x, 2x, 4x
Two side by side pn diode sensors for differential readout



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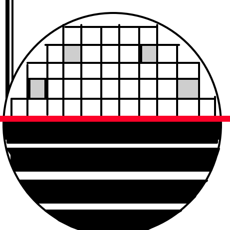
CAPACITORS

M2 M1 M1 to M2 M1 to Poly

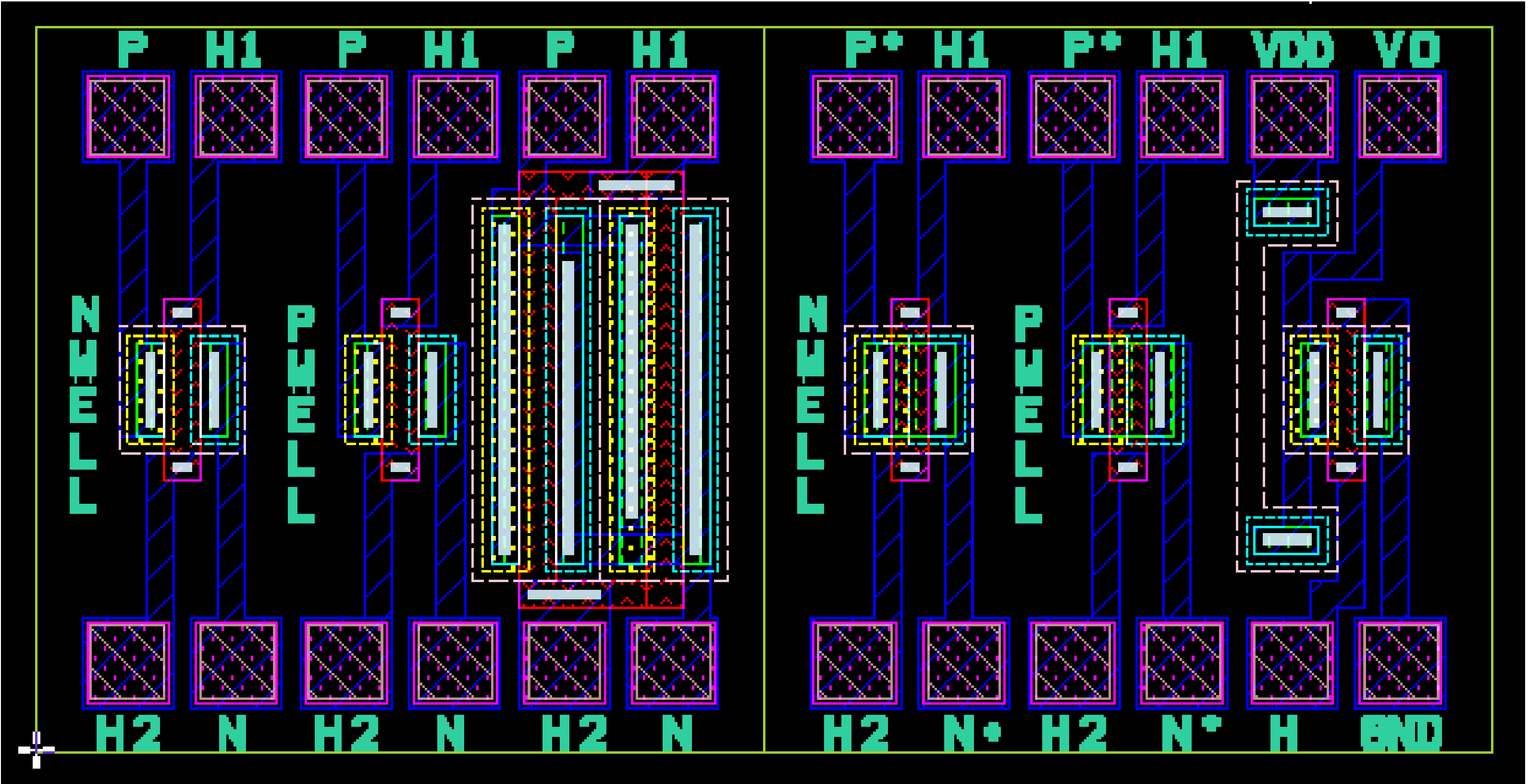
120 Fingers gives ~0.3 pF

670µm/470µm Plate
~3 pF



DIODES AND HEATERS

Poly Heater on top of Diodes



Integrated series well resistor.

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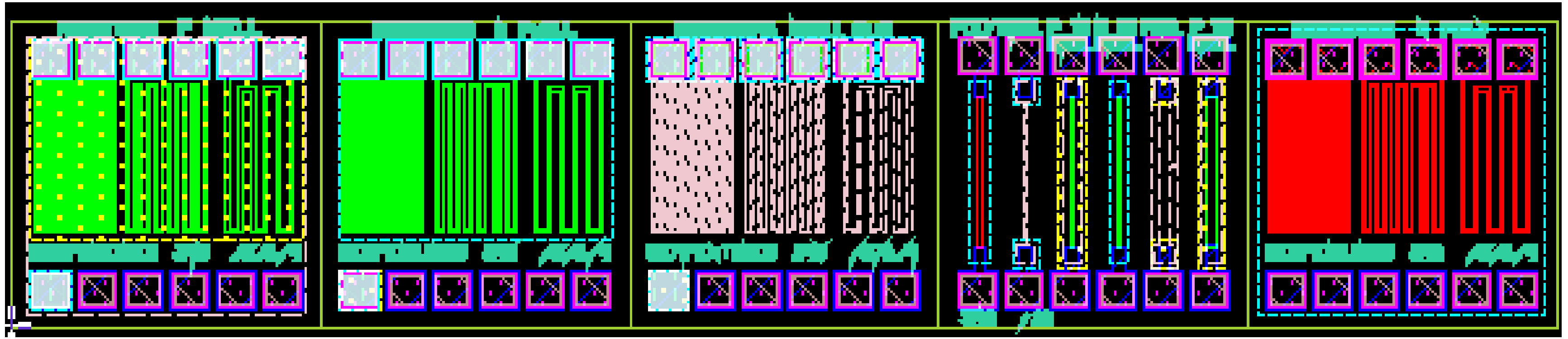
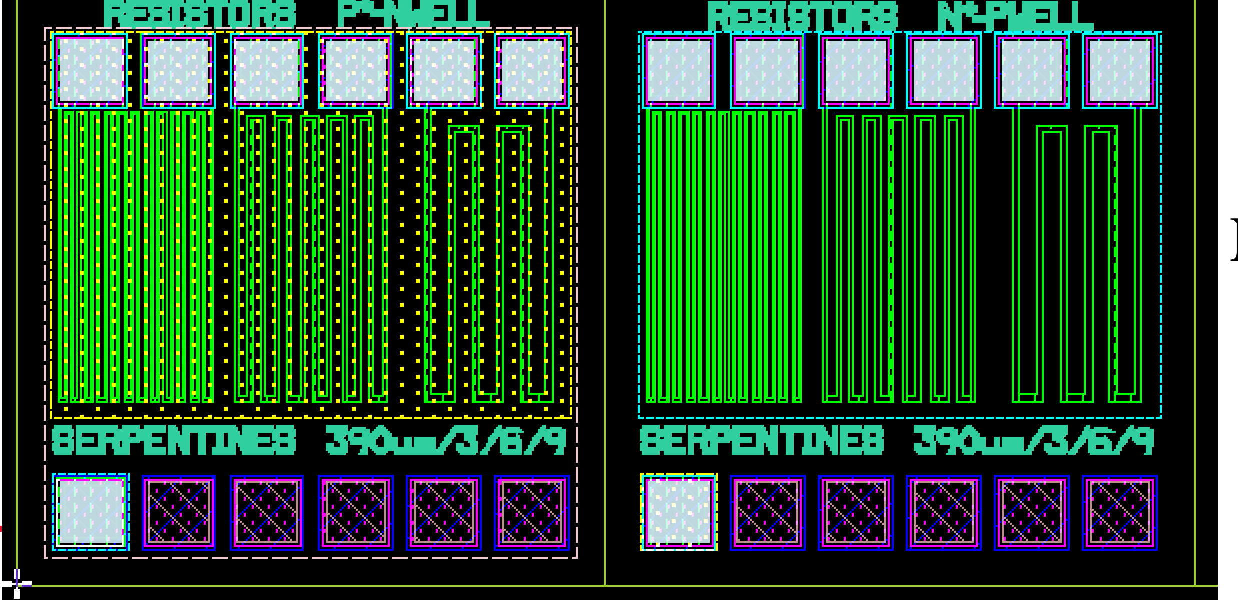
RESISTORS



P+ in Nwell



N+ in Pwell

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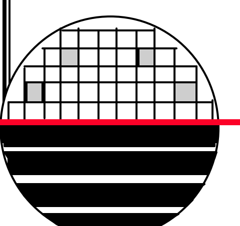
RESISTORS

RESISTORS NWELL-SUB
POLY NWEL P+IN NWEL N+IN PWEL PWEL P+IN NWEL
RESISTORS N+POLY
SERPENTINES 390um/3/6/9
390um/10
SERPENTINES 390um/3/6/9

Nwell in P substrate

6 different
Resistor Designs

N+ Poly



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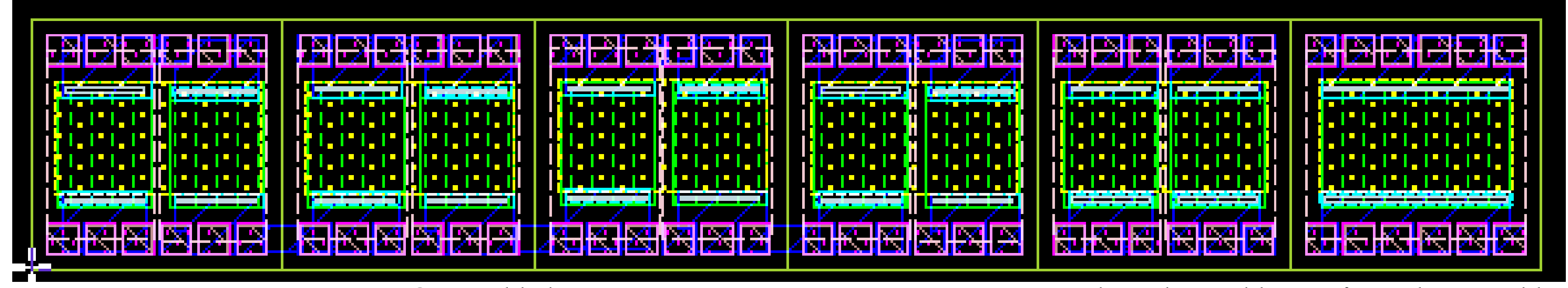
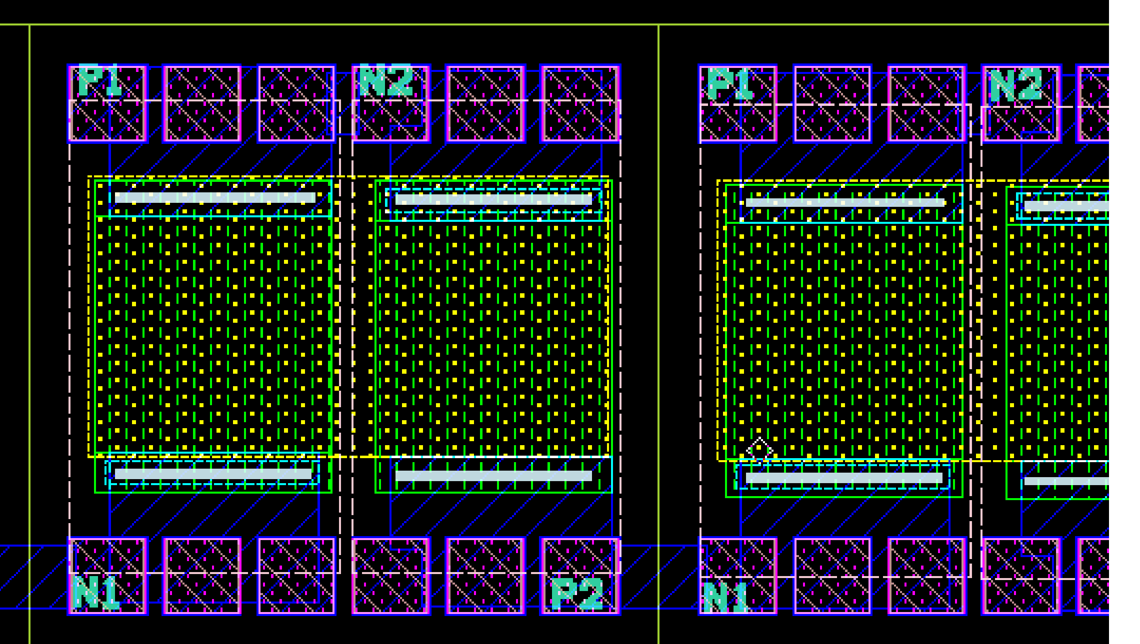
PHOTOVOLTAIC DEVICES



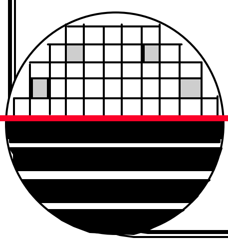
8 cell battery dual cells single cell

P+ in Nwell



~350µm by ~350µm

BIG PHOTO VOLTAIC CELL



DIGITAL CIRCUITS

Primitive Cells

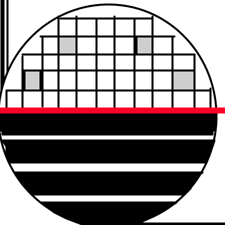
INVERTER, NAND2,3,4, NOR2,3,4, NULL

Basic Cells

XOR, MUX, DEMUX, ENCODER, DECODER
FULL ADDER, FLIP FLOPS

Macro Cells

BINARY COUNTER
SRAM



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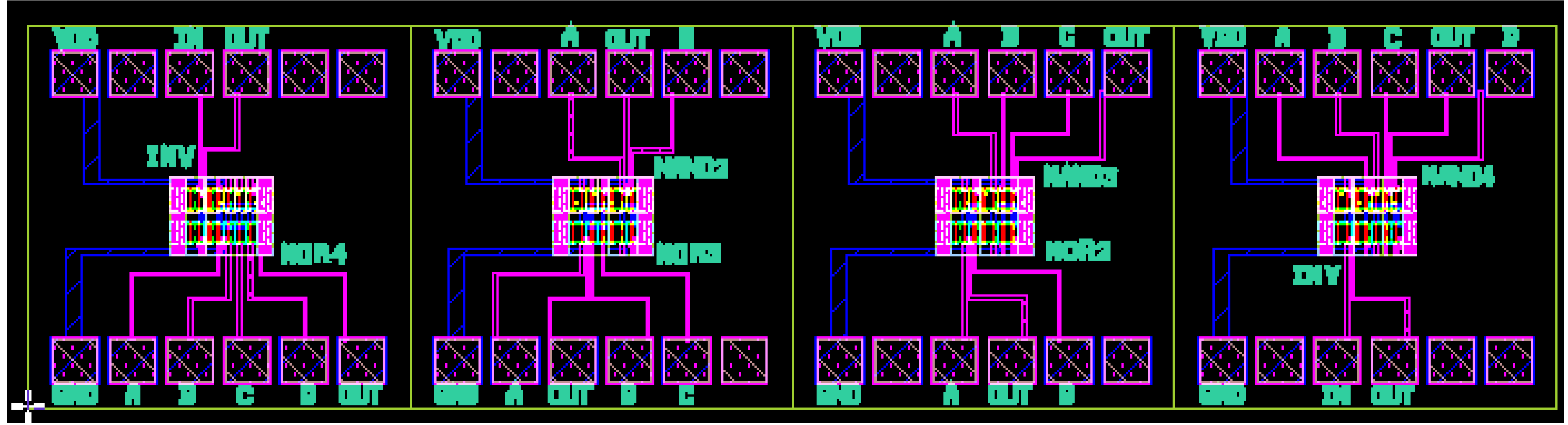
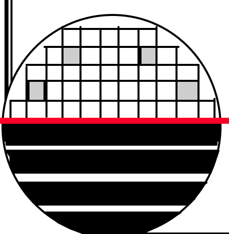
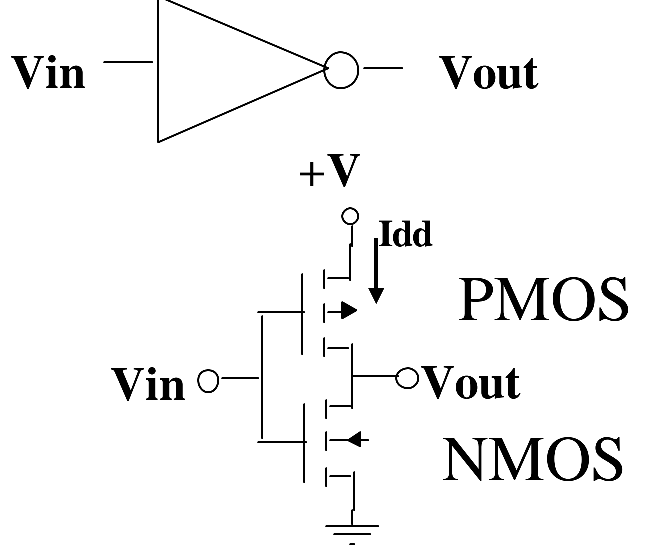
PRIMITIVE CELLS WITH PADS



INV/NOR4 NOR3/NAND2 NOR2/NAND3 INV/NAND4



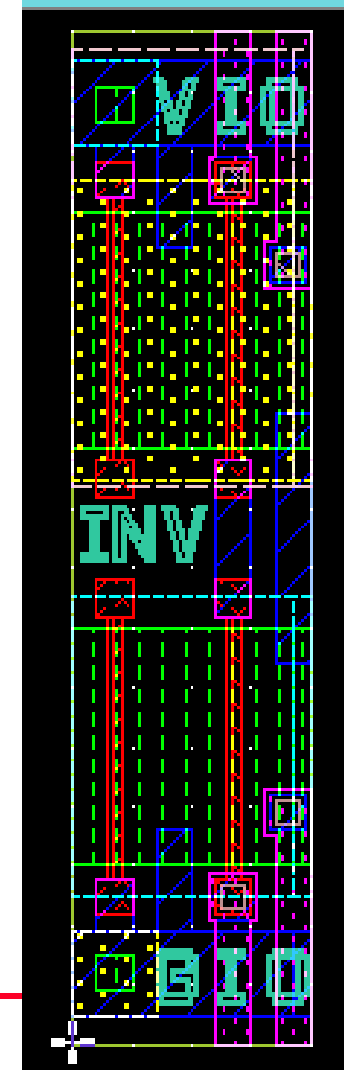
CMOS INVERTER

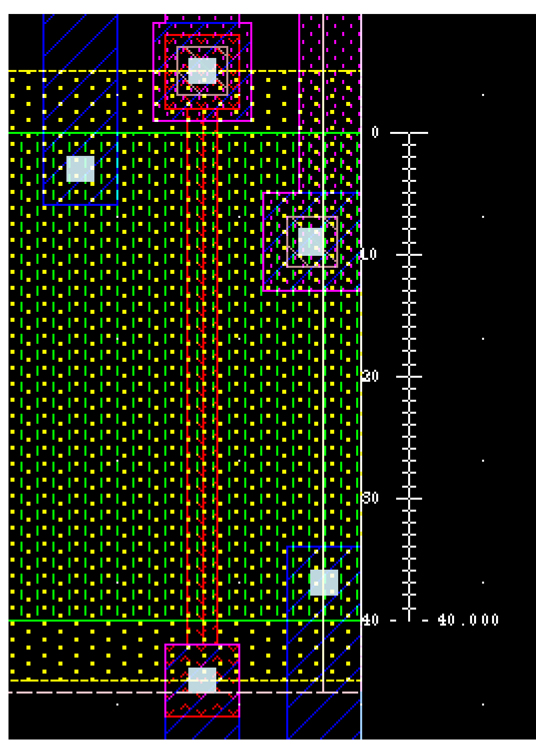


CMOS

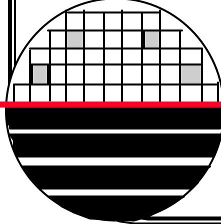
TRUTH TABLE

VIN	VOUT
0	1
1	0





W = 40 µm
Ldrawn = 2.5µm
Lpoly = 1.0µm
Leff = 0.35 µm



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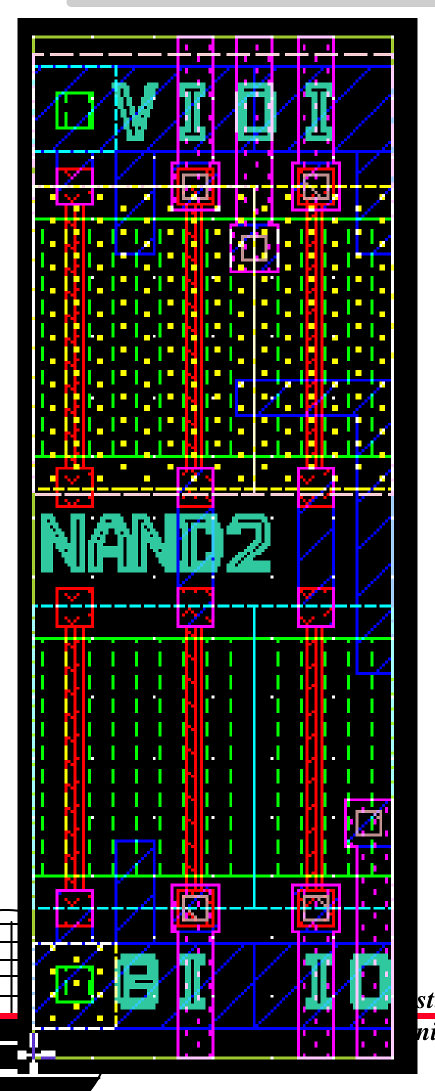
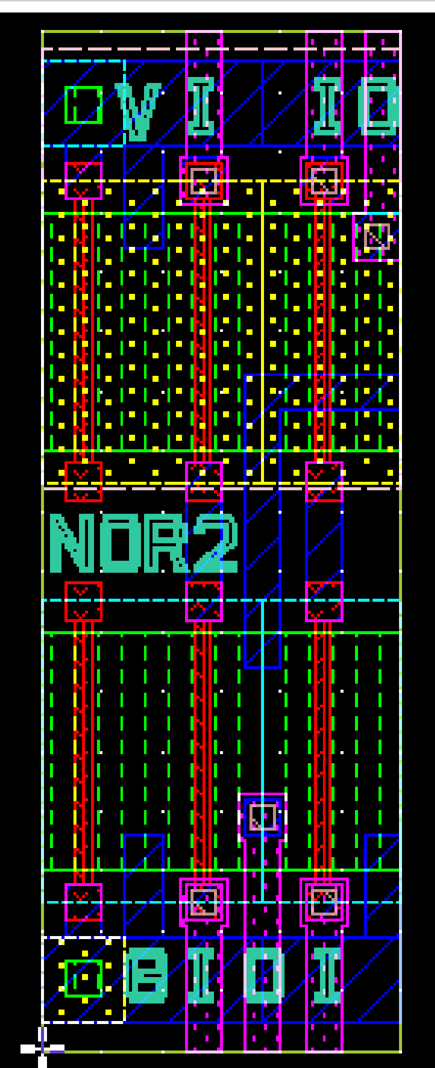
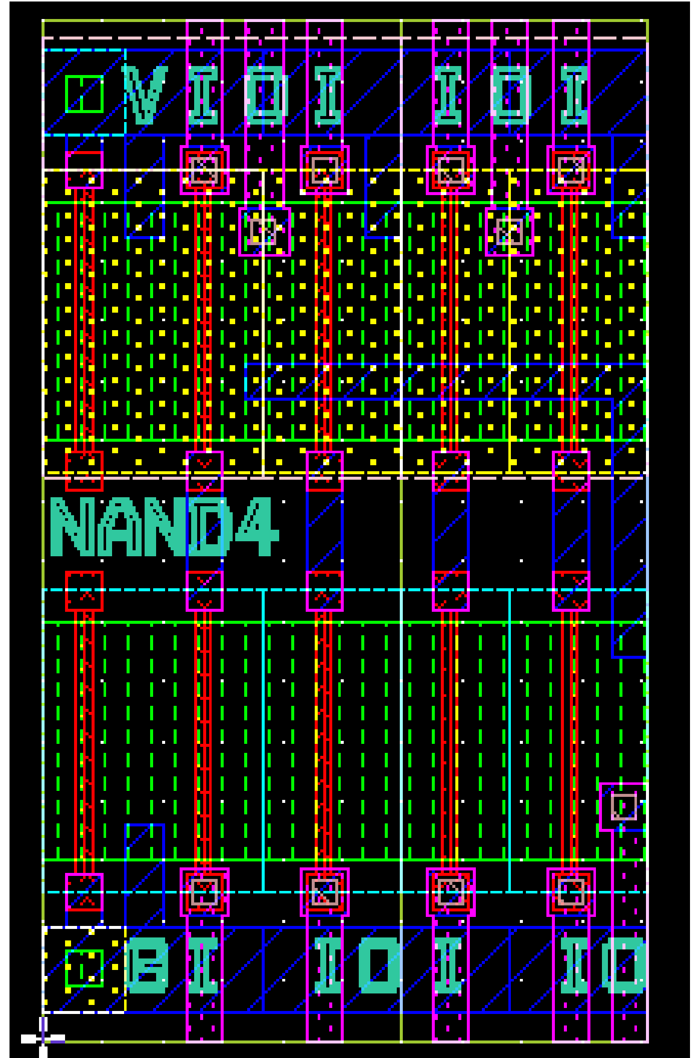
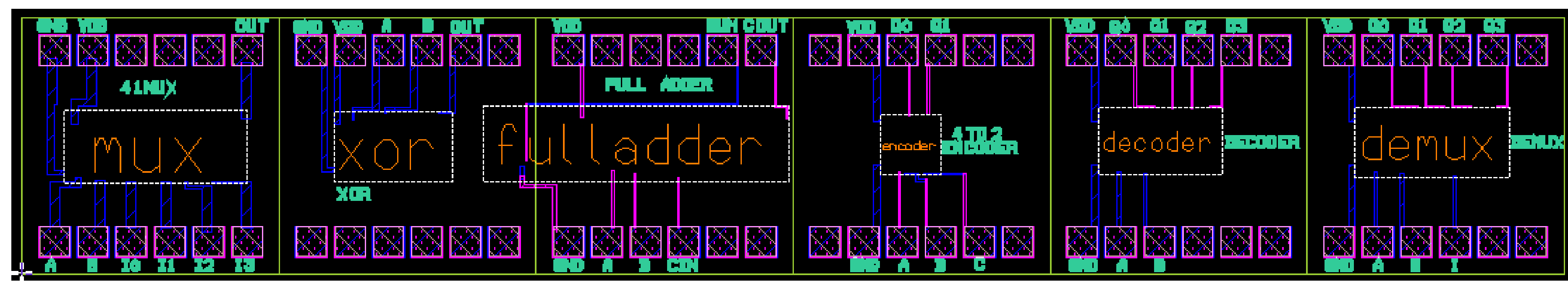
PRIMITIVE CELLS



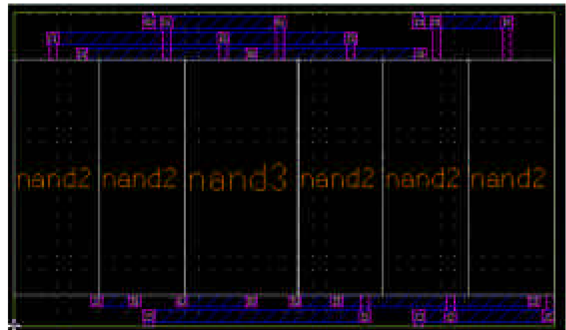




BASIC DIGITAL CELLS WITH PADS



Multiplexer XOR Full Adder Encoder Decoder Demux

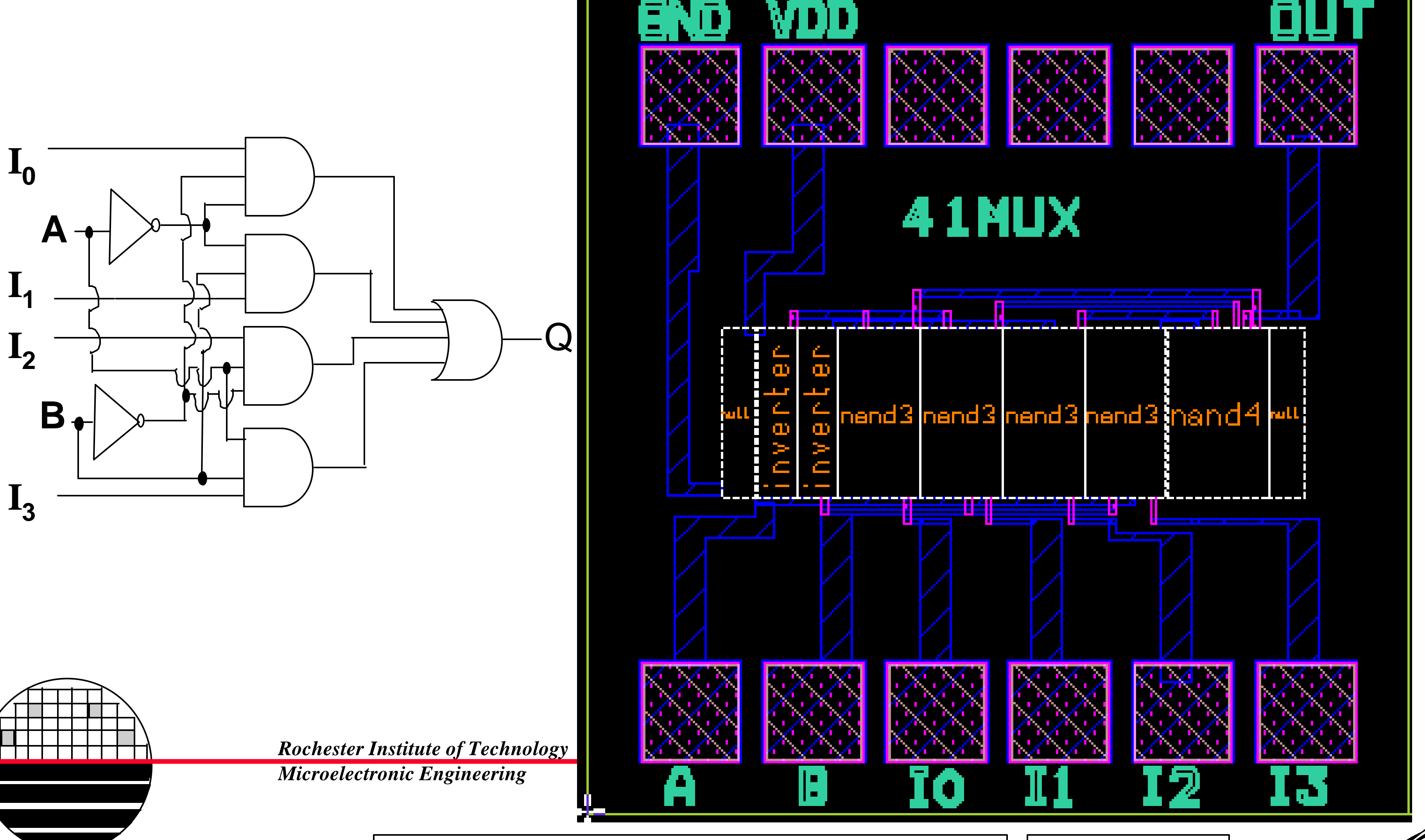


Edge Triggered D FF

nand3 nand3 inverter nand2 nand2 nand2 nand2 nand2 nand2

JK FF

4 TO 1 MULTIPLEXER



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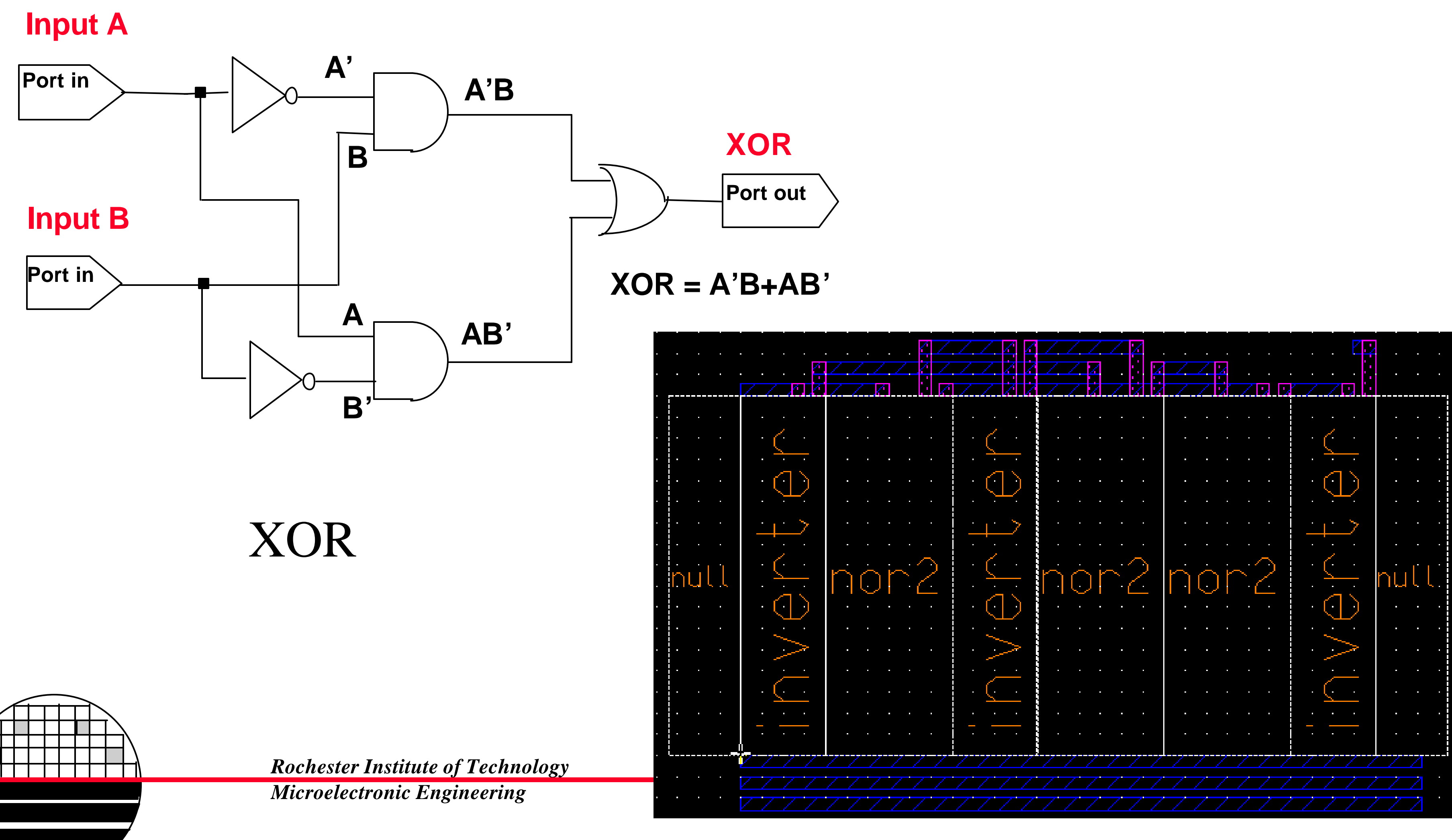
BASIC CELL XOR



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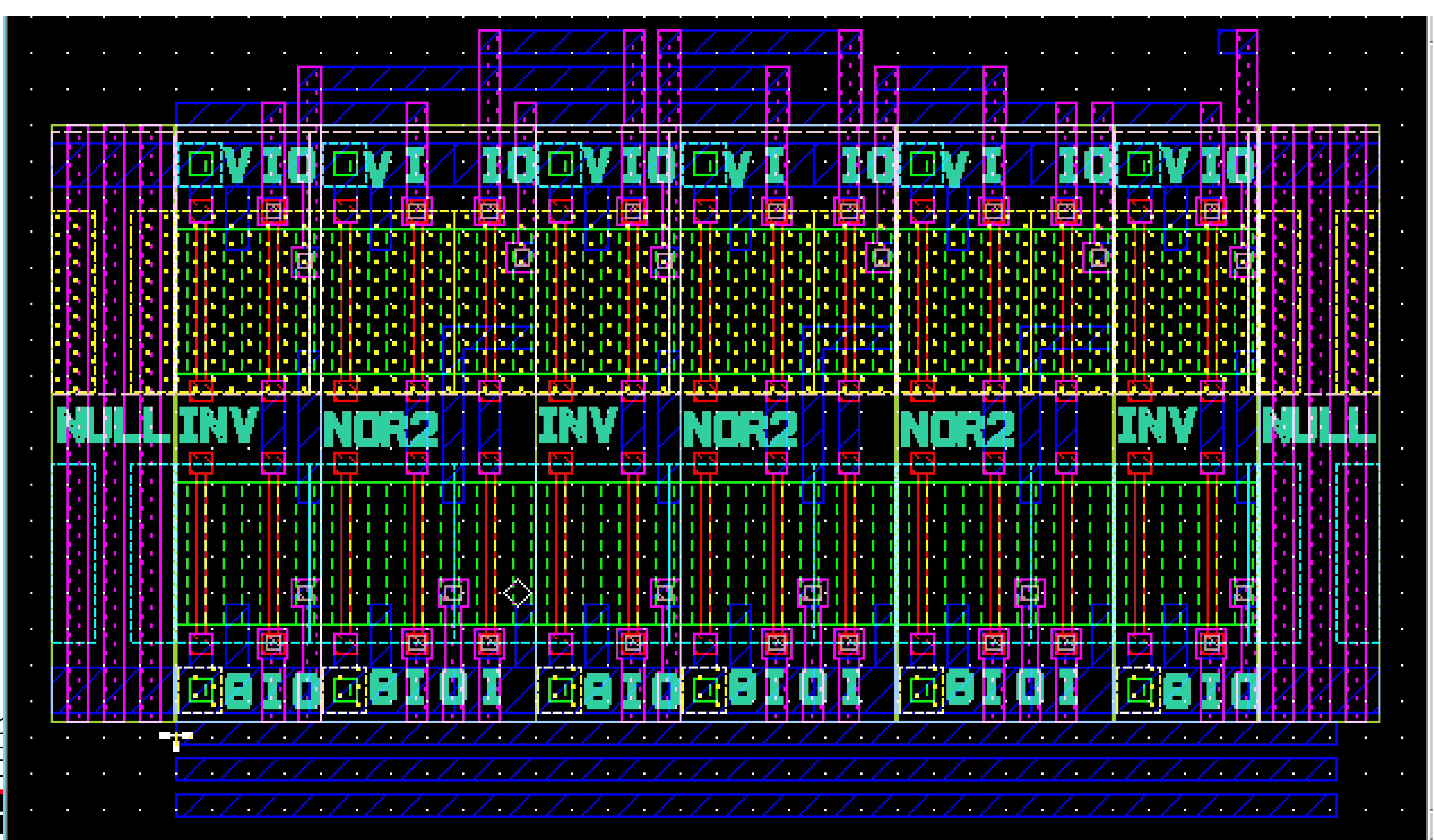
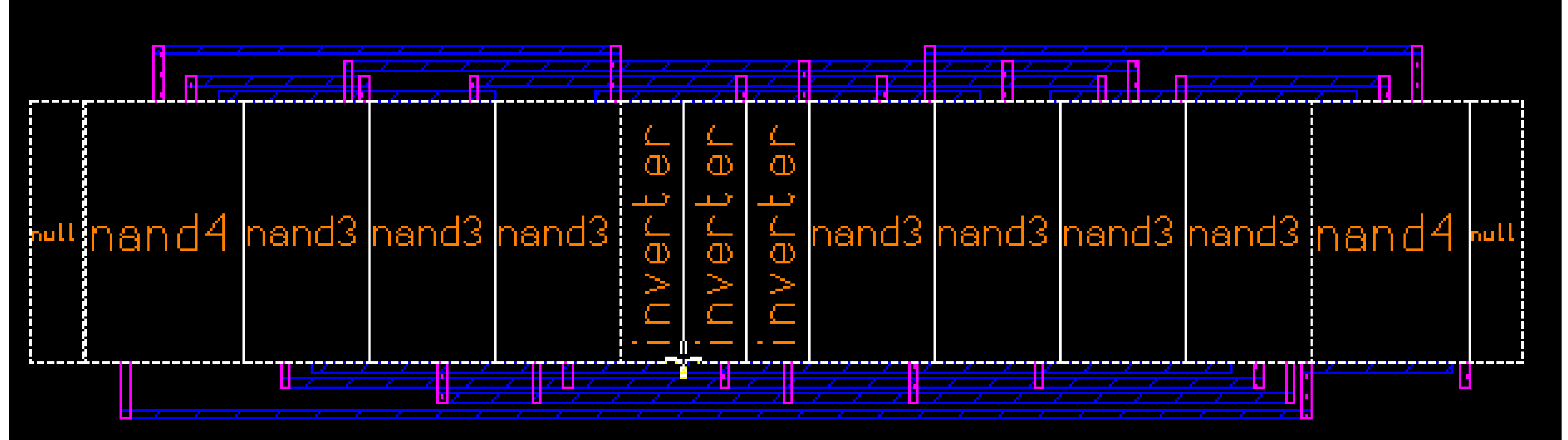
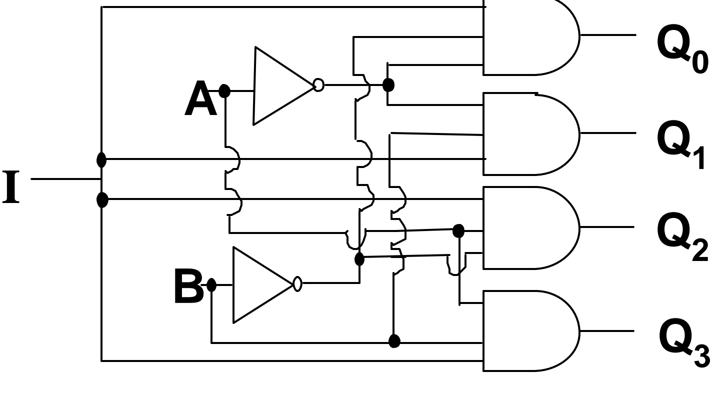
XOR



FULL ADDER



1 TO 4 DEMULTIPLEXER



VDD Q0 Q1 Q2 Q3

DEMUX

GND A B I

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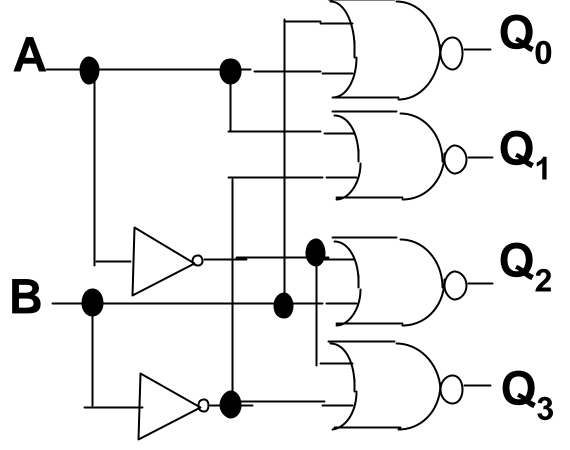
DECODER



VDD Q0 Q1 Q2 Q3

DECODER

GND A B

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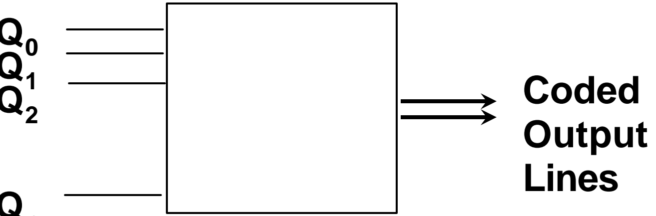
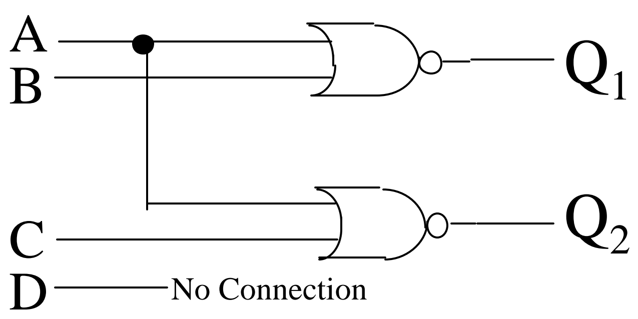
ENCODER

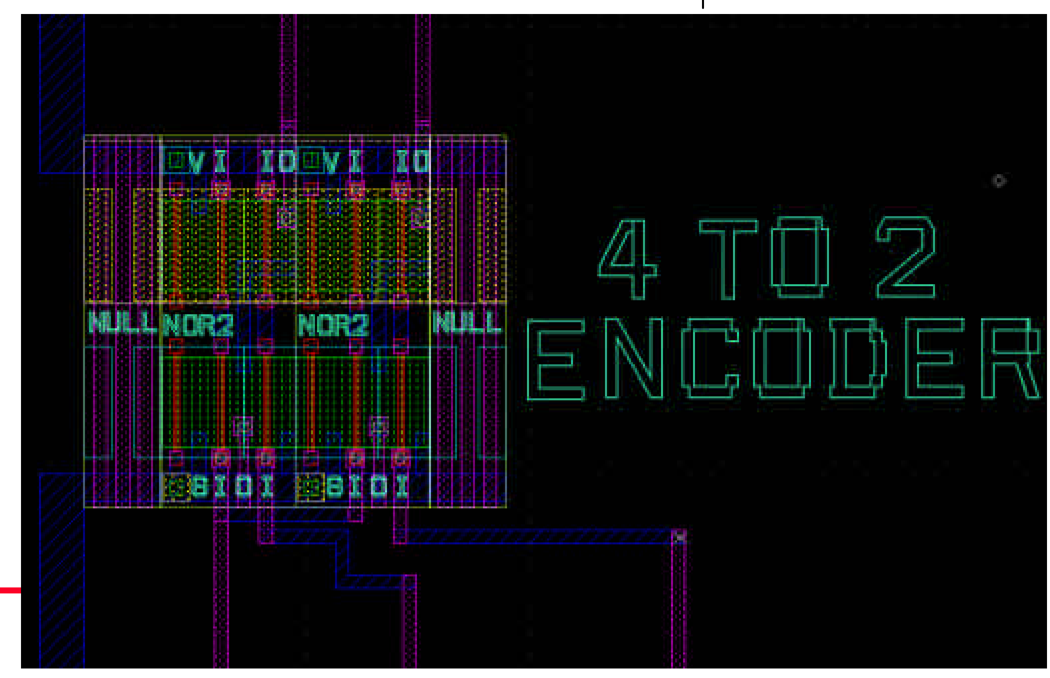


Digital Encoder

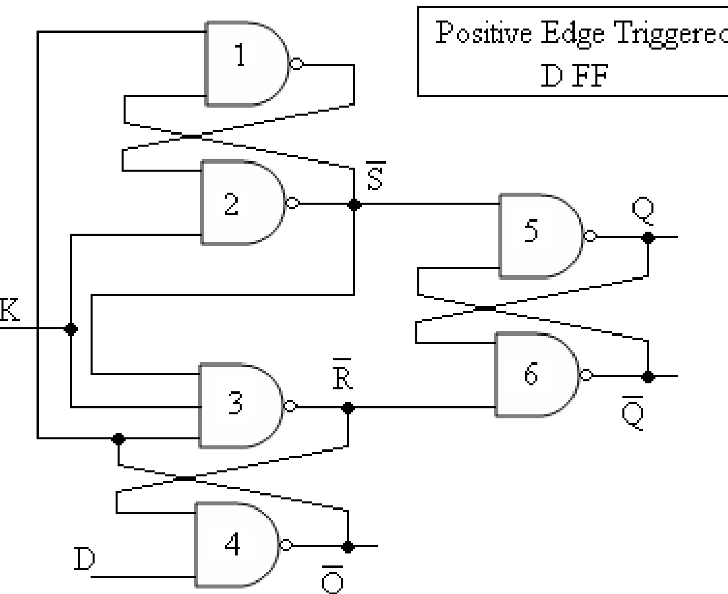
512 inputs can be coded into 9 lines which is a more dramatic benefit

A	B	C	D	Q0	Q1
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

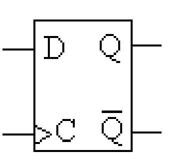




EDGE TRIGGERED D TYPE FLIP FLOP



Positive Edge Triggered
D FF



Inputs		Outputs	
D	C	Q^+	$\overline{Q^+}$
0	↑	0	1
1	↑	1	0
X	0	Q	$\overline{Q}$
X	1	Q	$\overline{Q}$

CLK D SET $\overline{Q}$ Q VDD

DFF SET RES
BURAK

RES GND

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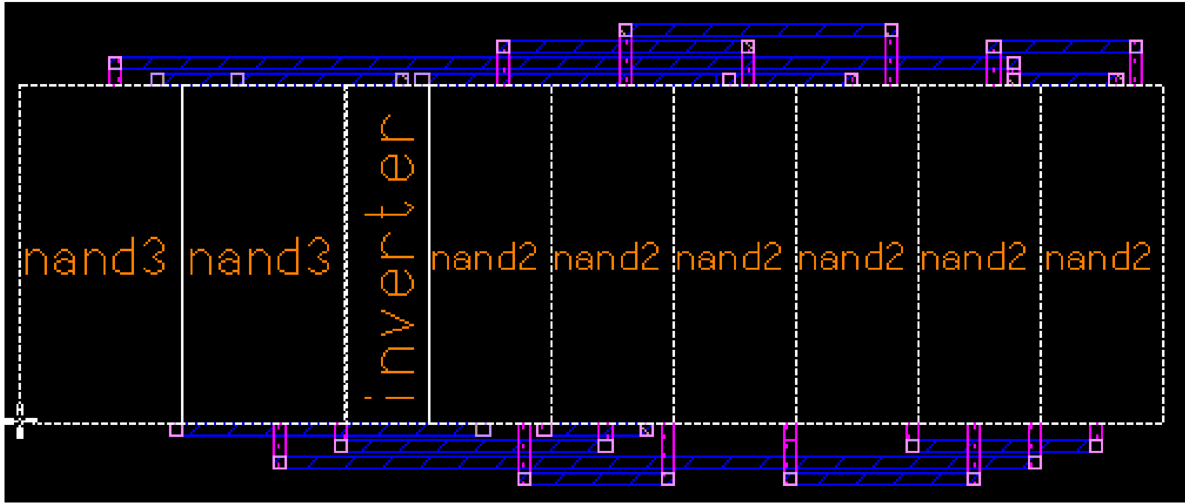
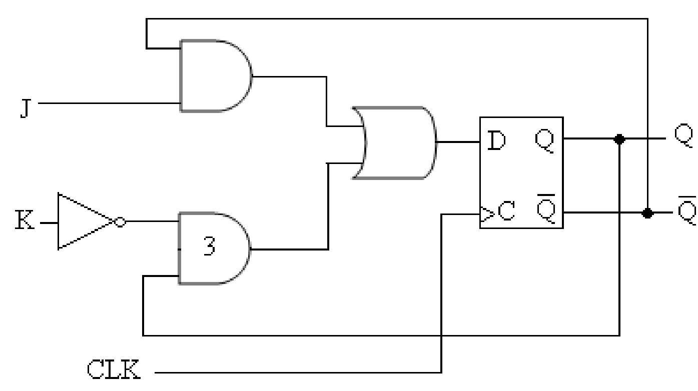
JK FLIP FLOP

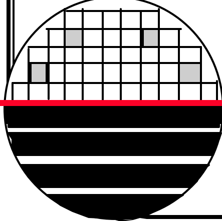




Positive Edge Triggered
JK FF

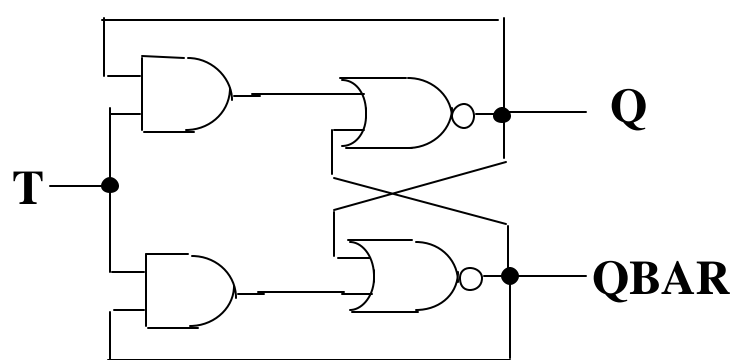
J Q
>C
K $\overline{Q}$

Inputs			Outputs	
J	K	C	Q^+	$\overline{Q}^+$
0	0	↑	Q	$\overline{Q}$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	Q	Q
X	X	0	Q	$\overline{Q}$
X	X	1	Q	$\overline{Q}$



T-TYPE FILP-FLOP

TOGGEL FLIP FLOP



Q: Toggles High and Low with Each Input

T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

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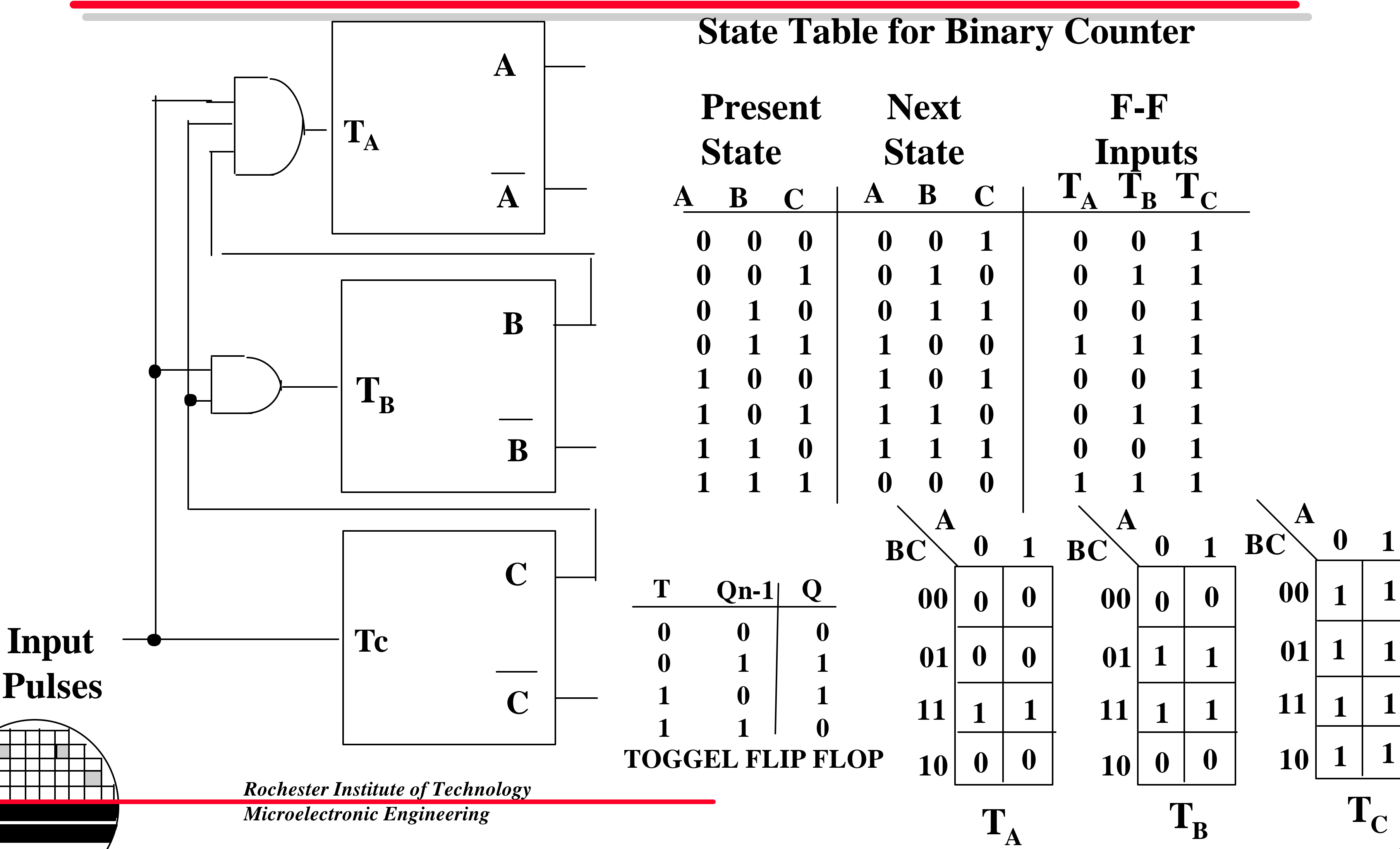
BINARY COUNTER USING T TYPE FLIP FLOPS



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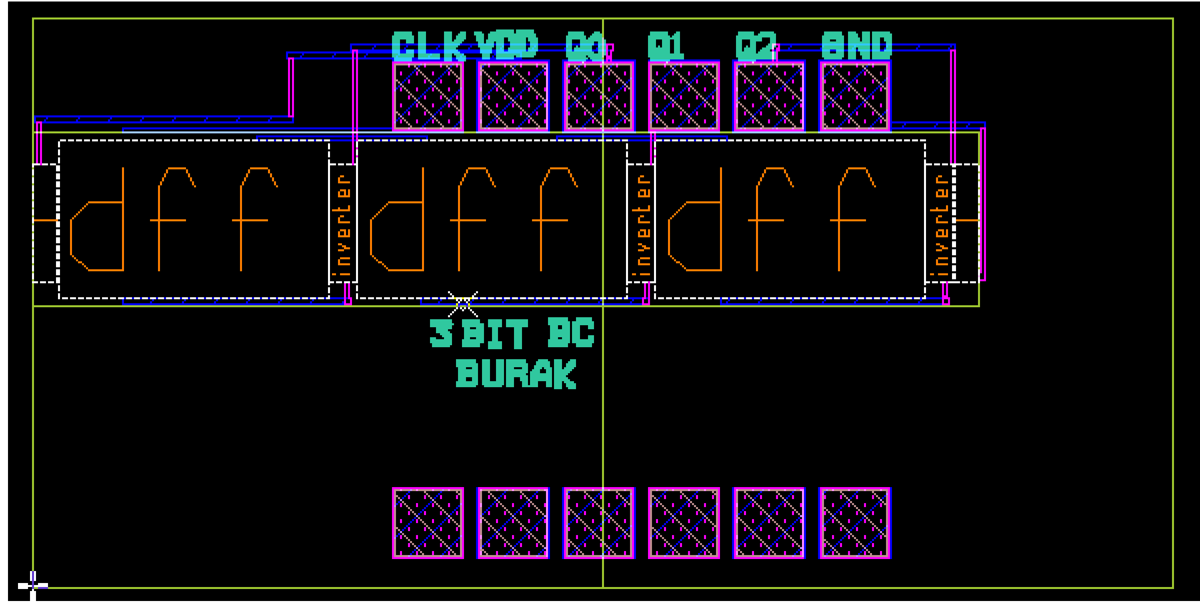
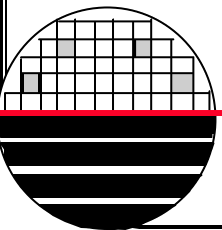
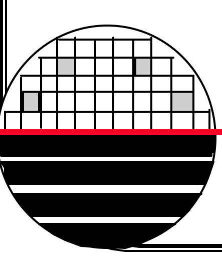
3-BIT BINARY COUNTER WITH D FLIP FLOPS





MACROCELLS

Binary Counter
SRAM



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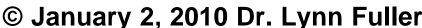
3-BIT BINARY COUNTER/SHIFT REGISTER

Binary Counter
Serial Output
Asynchronous Reset
Count Up Enable
Shift Out Clock Input
Count Up Clock Input
Start Bit and Stop Bit



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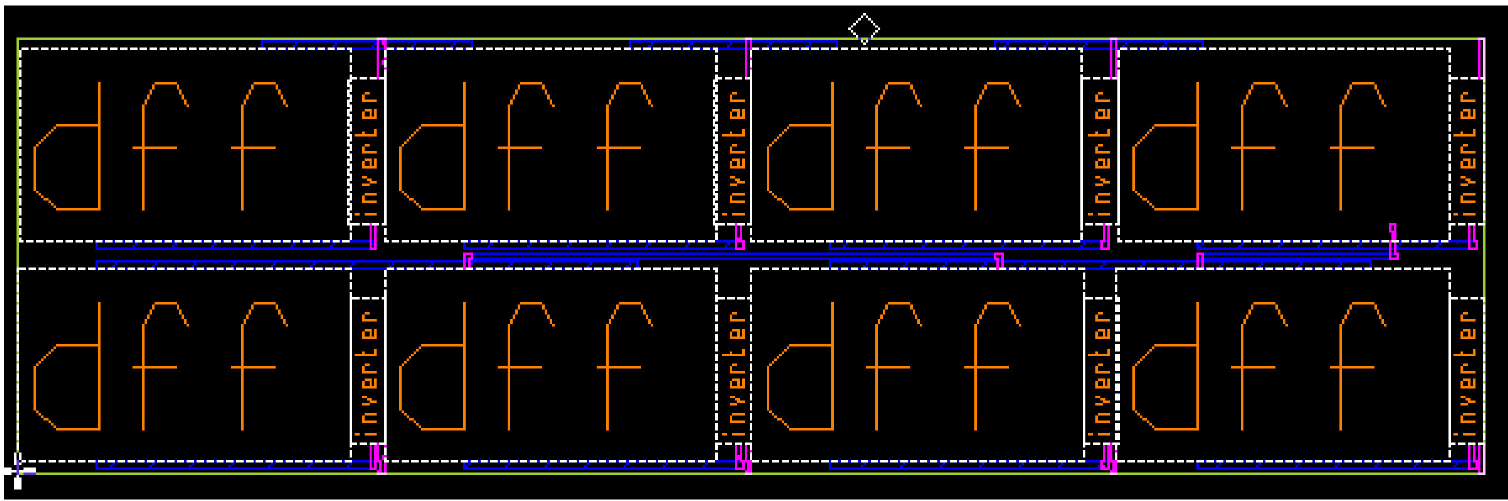
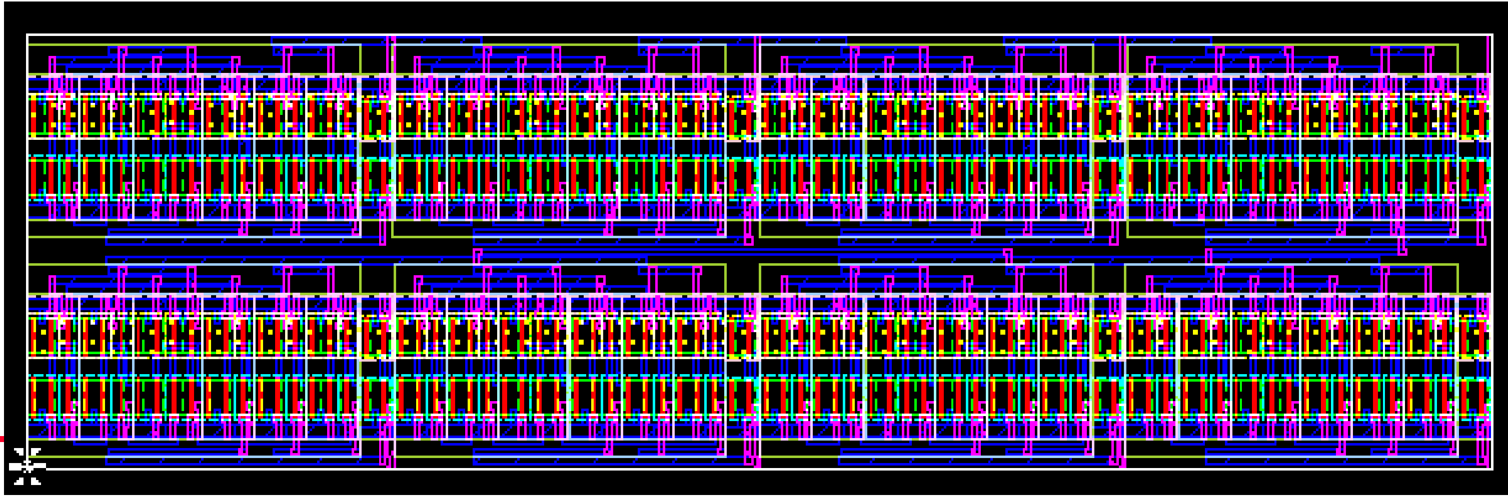
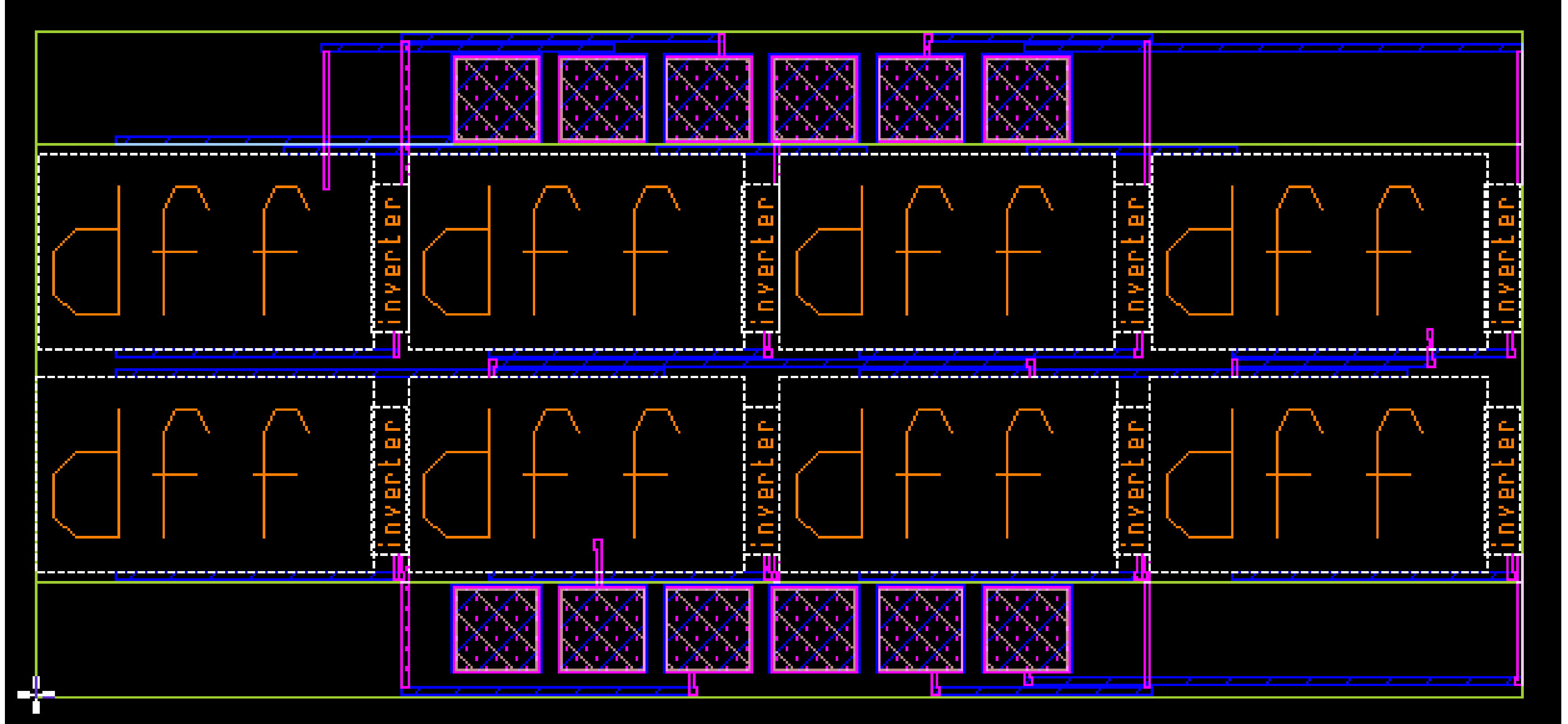
8-BIT BINARY COUNTER

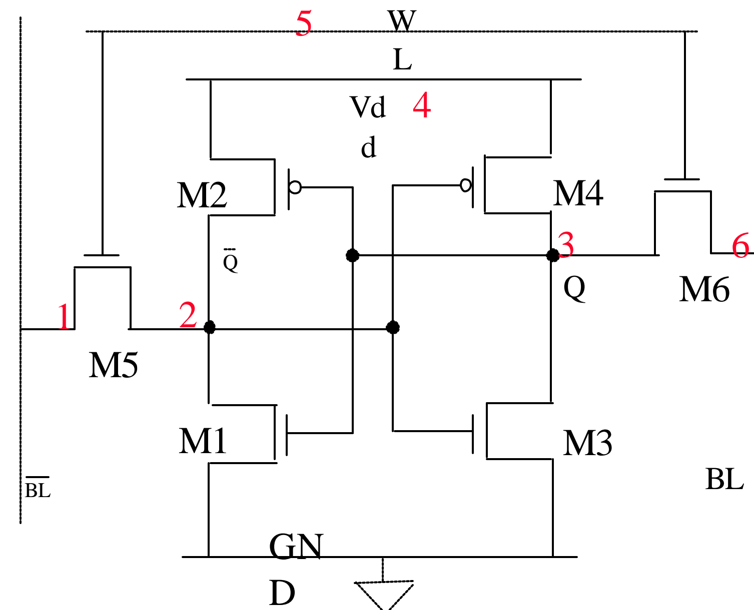




8-BIT BINARY COUNTER WITH PADS



SRAM



BH1 BL1 BH2 BL2 BH3 BL3

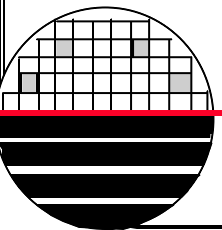
3x3
SRAM

DD GND W1 W2 W3

Rochester Institute of Technology
Microelectronic Engineering

ANALOG AND MIXED MODE CIRCUITS

Operational Amplifier
Inverter with Hysteresis
RC Oscillator
Two Phase Clock
Analog Switches
Voltage Doubler, Tripler
Analog Multiplexer
Comparator with Hysteresis
A-to-D
D-to-A
OTA, Biquad Filter, Elliptic Filter
Programmable Binary Weighted Resistors



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SPICE PARAMETERS FOR SUB-CMOS PROCESS

```
*This file is called: RIT_MICROE_MODELS.TXT
*
*1-15-2007 FROM DR. FULLER'S SPREADSHEET WITH VT0=0.75
.MODEL RITSUBN49 NMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8 NSS=3E11
+XWREF=2.0E-7 XLREF=2.95E-7 VTH0=0.75 U0= 950 WINT=2.0E-7 LINT=1.84E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGS0=3.4E-10 CGD0=3.4E-10 CGB0=5.75E-10)
*
*1-17-2007 FROM DR. FULLER'S SPREADSHEET WITH VT0=-0.75
.MODEL RITSUBP49 PMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8 NSS=3E11 PCLM=5
+XWREF= 2.0E-7 XLREF=3.61E-7 VTH0=-0.75 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 NGATE=5E20
+CGS0=4.5E-10 CGD0=4.5E-10 CGB0=5.75E-10)
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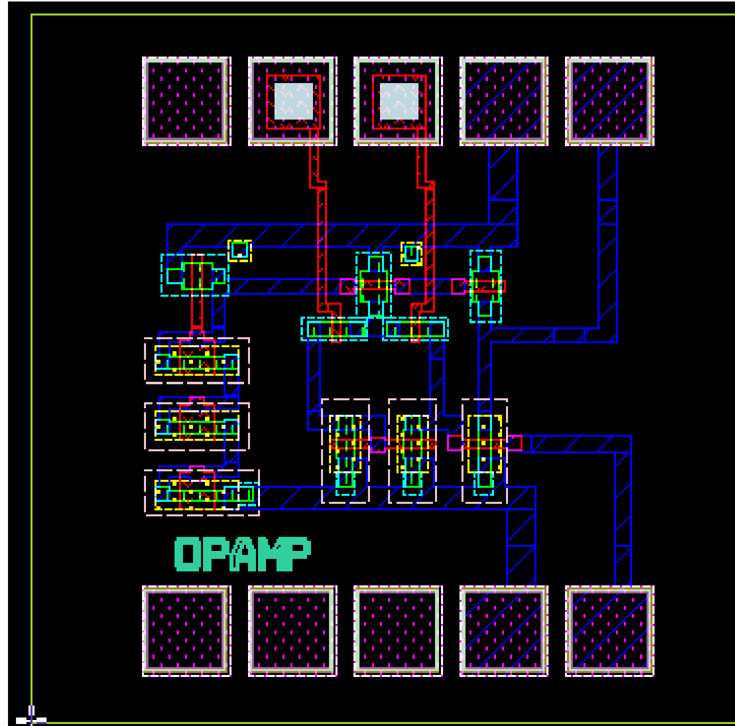
OPERATIONAL AMPLIFIER



Version 1

IN- VDD OUT IN+ VSS

OPAMP1
BURAK

OPAMP2
BURAK

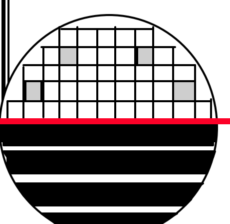
VDD IN- VSS IN+ OUT

VERSION 1 OPERATIONAL AMPLIFIER

+V
10
M11
8
L/W
80/20
M3
2
M4
20/40
20/40
M6
M10
3
80/20
7
5
20/30
M1
M2
20/30
4
20/30
Vin-
1
Vin+
9
M9
80/20
Vout
M7
6
M5
20/40
M8
20/40
20/40
-V
20

p-well CMOS

dimensions
L/W
(µm/µm)



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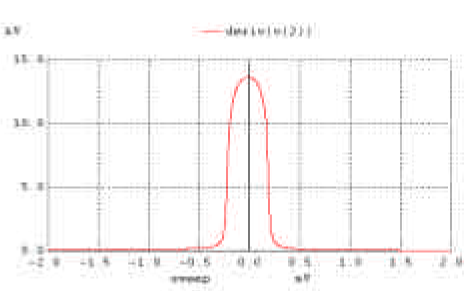
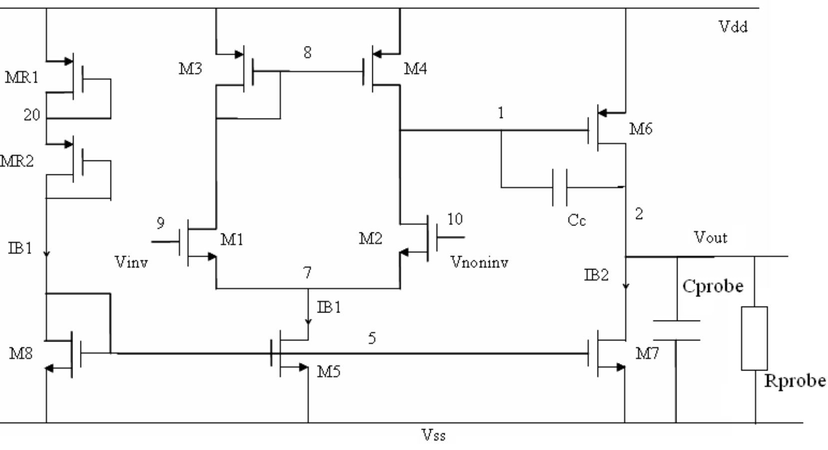
SPICE ANALYSIS OF OP AMP VERSION 2

```
.incl rit_sub_param.txt
m1 8 9 7 6 cmosn w=9u l=5u nrd=1 nrs=1 ad=45p pd=28u as=45p ps=28u
m2 1 10 7 6 cmosn w=9u l=5u nrd=1 nrs=1 ad=45p pd=28u as=45p ps=28u
m3 8 8 4 4 cmosp w=21u l=5u nrd=1 nrs=1 ad=102p pd=50u as=102p ps=50u
m4 1 8 4 4 cmosp w=21u l=5u nrd=1 nrs=1 ad=102p pd=50u as=102p ps=50u
m5 7 5 6 6 cmosn w=40u l=5u nrd=1 nrs=1 ad=205p pd=90u as=205p ps=90u
m6 2 1 4 4 cmosp w=190u l=5u nrd=1 nrs=1 ad=950p pd=400u as=950p ps=400u
m7 2 5 6 6 cmosn w=190u l=5u nrd=1 nrs=1 ad=950p pd=400u as=950p ps=400u
m8 5 5 6 6 cmosn w=40u l=5u nrd=1 nrs=1 ad=205p pd=90u as=205p ps=90u
vdd 4 0 3
vss 6 0 -3
cprobe 2 0 30p
Rprobe 2 0 1meg
cc 1 2 0.6p
mr1 20 20 4 4 cmosp w=6u l=10u nrd=1 nrs=1 ad=200p pd=60u as=200p ps=60u
mr2 5 5 20 4 cmosp w=6u l=10u nrd=1 nrs=1 ad=200p pd=60u as=200p ps=60u
***dc open loop gain*********
vi1 9 0 0
vi2 10 0 0
*.dc vi2 -0.002 0.002 1u
.dc vi2 -1 1 0.1m
*****open loop frequency
    characteristics*****
*vi1 9 0 0
*vi2 10 0 dc 0 ac 1u
*.ac dec 100 10 1g
.end
```



13.5kV/V gain



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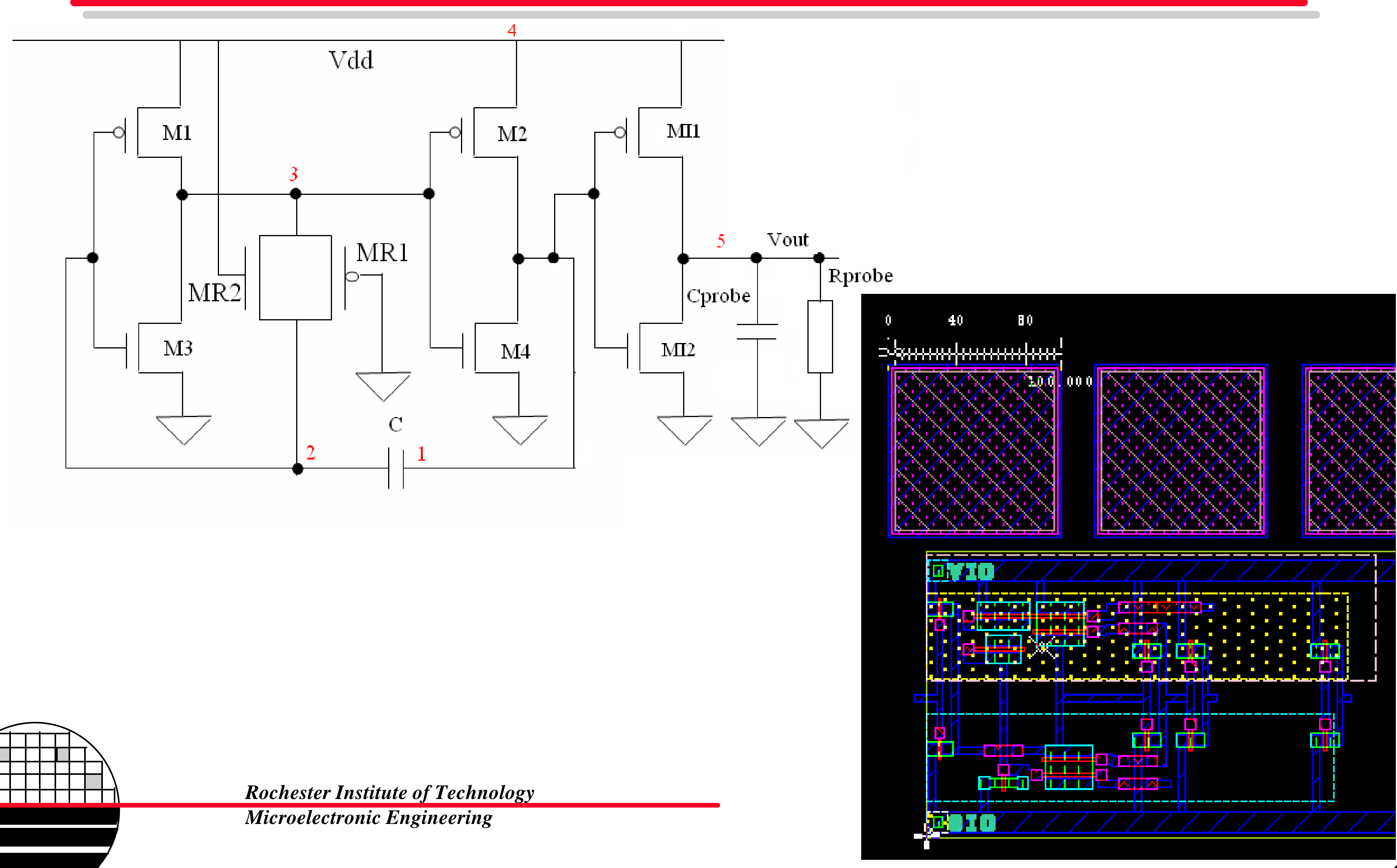
INVERTER WITH HYSTERESIS – RC OSCILLATOR



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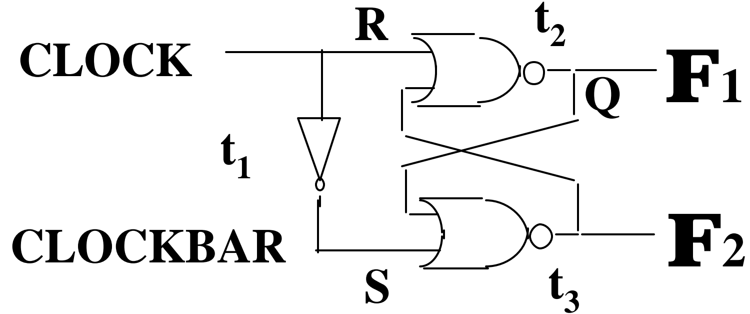
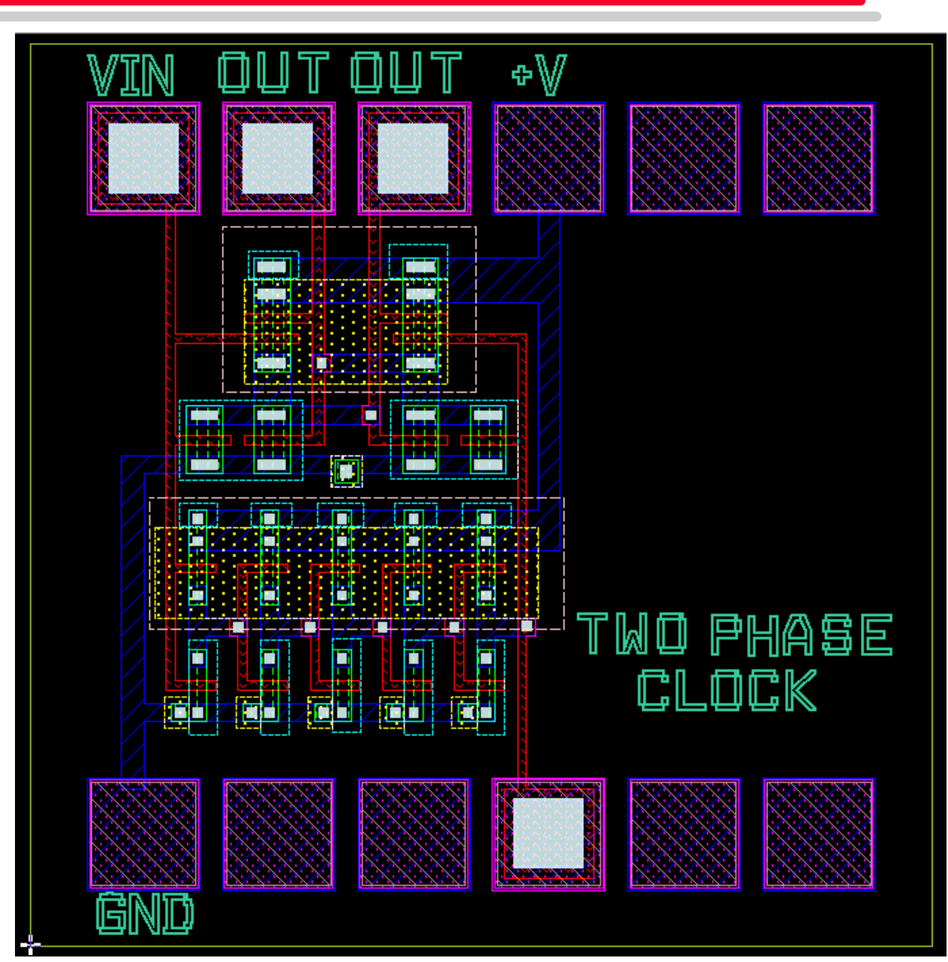
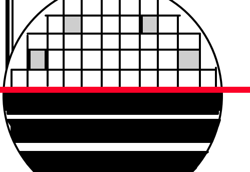
TWO PHASE CLOCK







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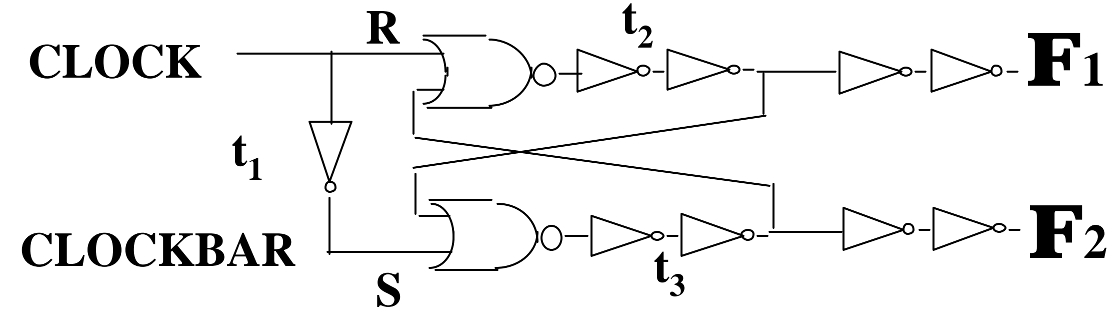
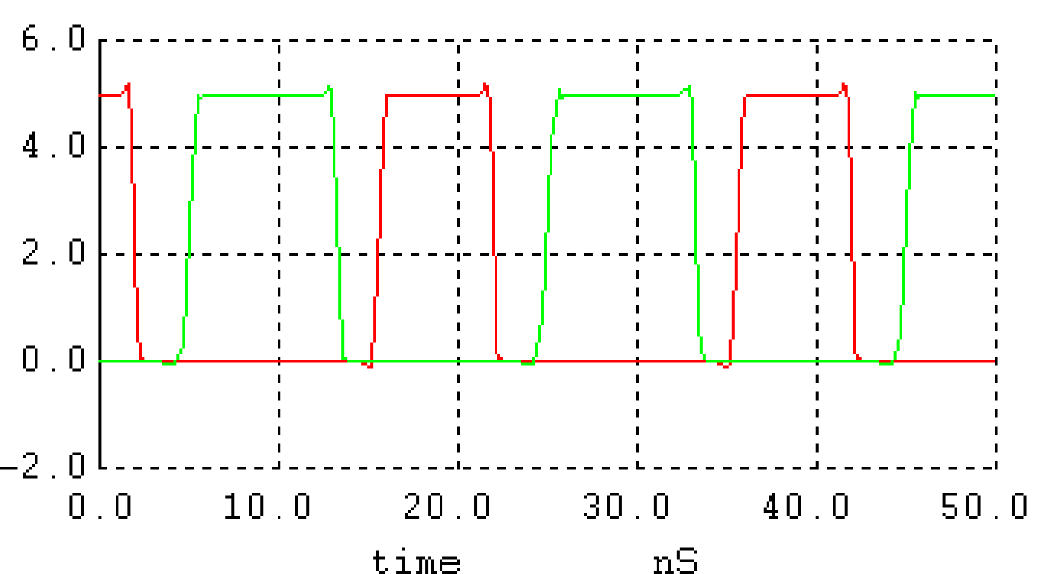
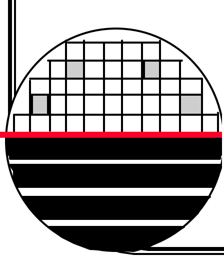
WINSPICE SIMULATION FOR VERSION TWO + BUFFERS



Next Design add buffers





TWO PHASE CLOCK WITH BUFFERS

+V IN OUT1 OUT2 GND

null inverter inverter inverter inverter inverter inverter inverter nor2 nor2 inverter inverter inverter inverter inverter inverter null

TWO PHASE CLK

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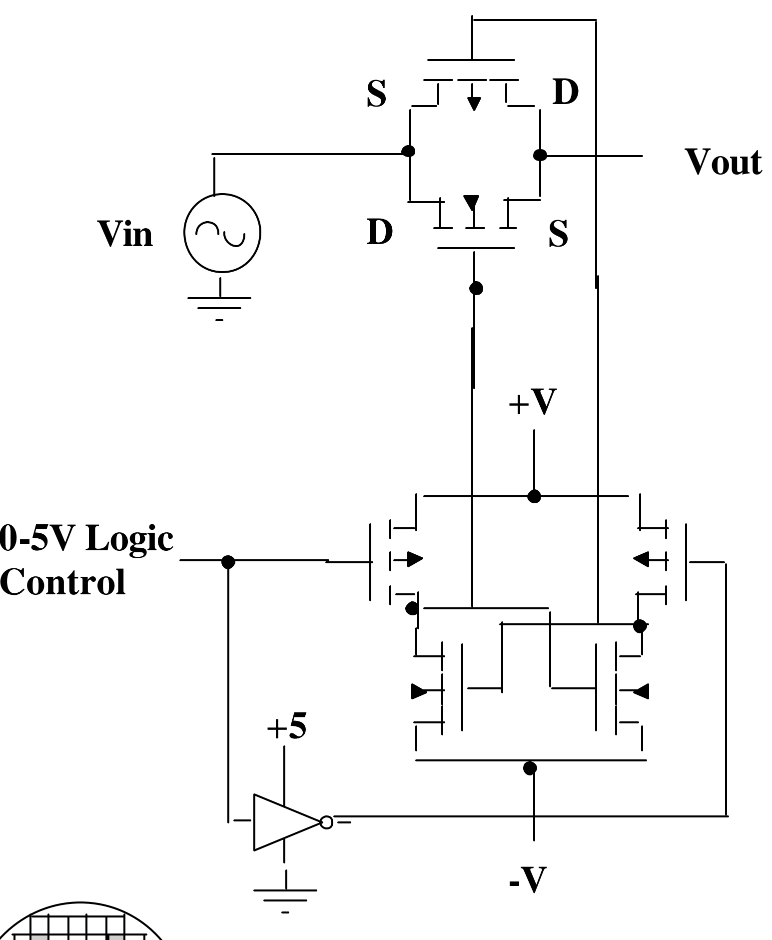
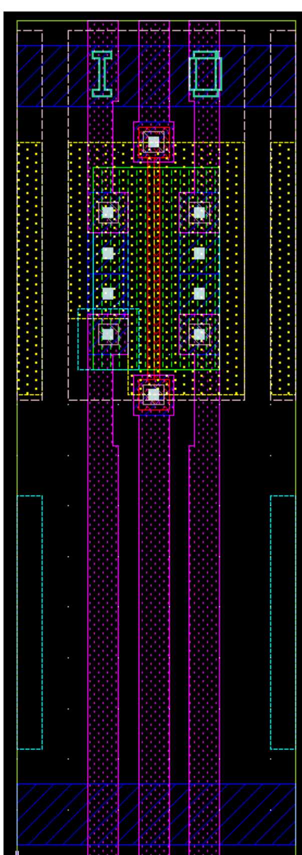
ANALOG SWITCH





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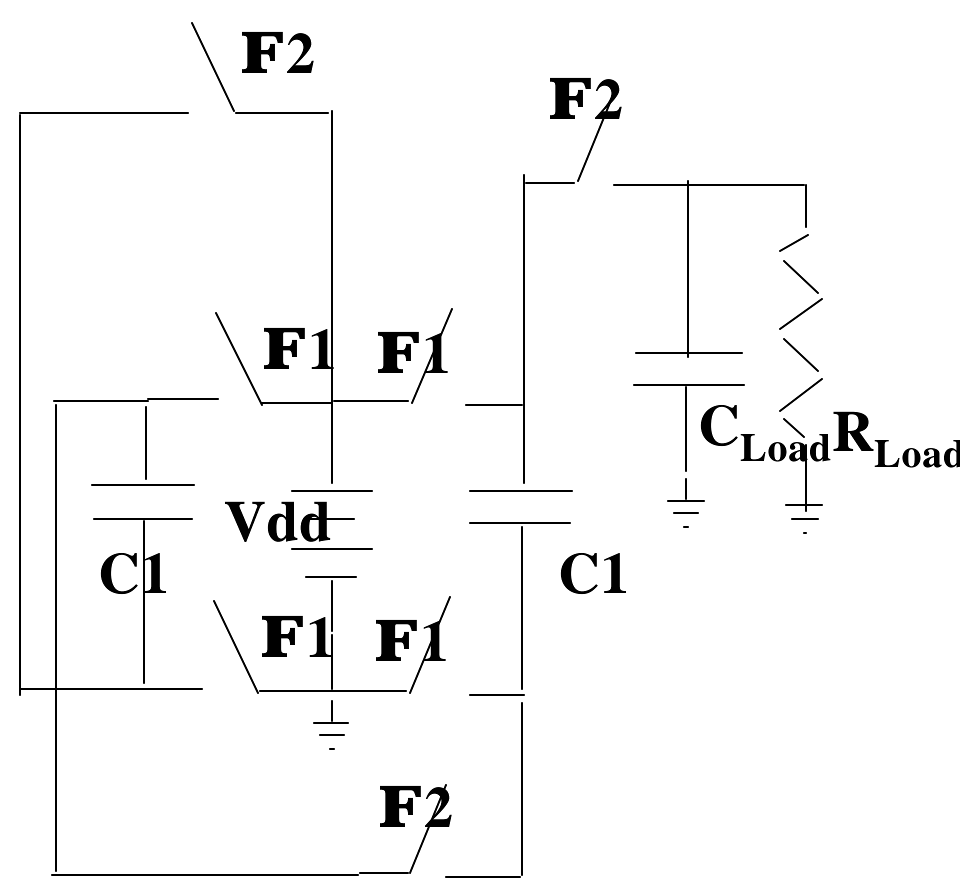
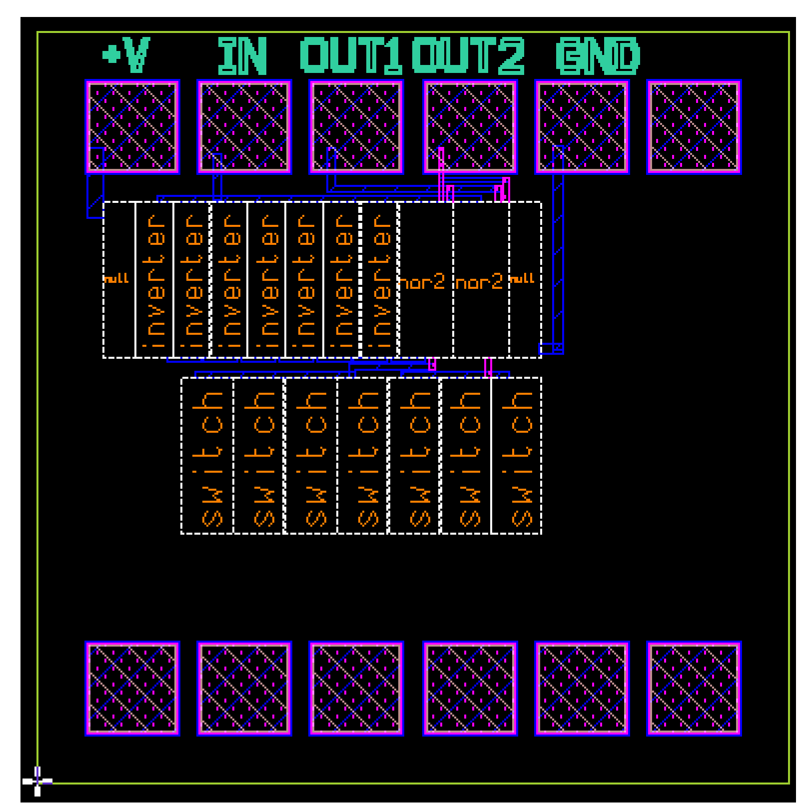
VOLTAGE DOUBLER





Voltage Tripler

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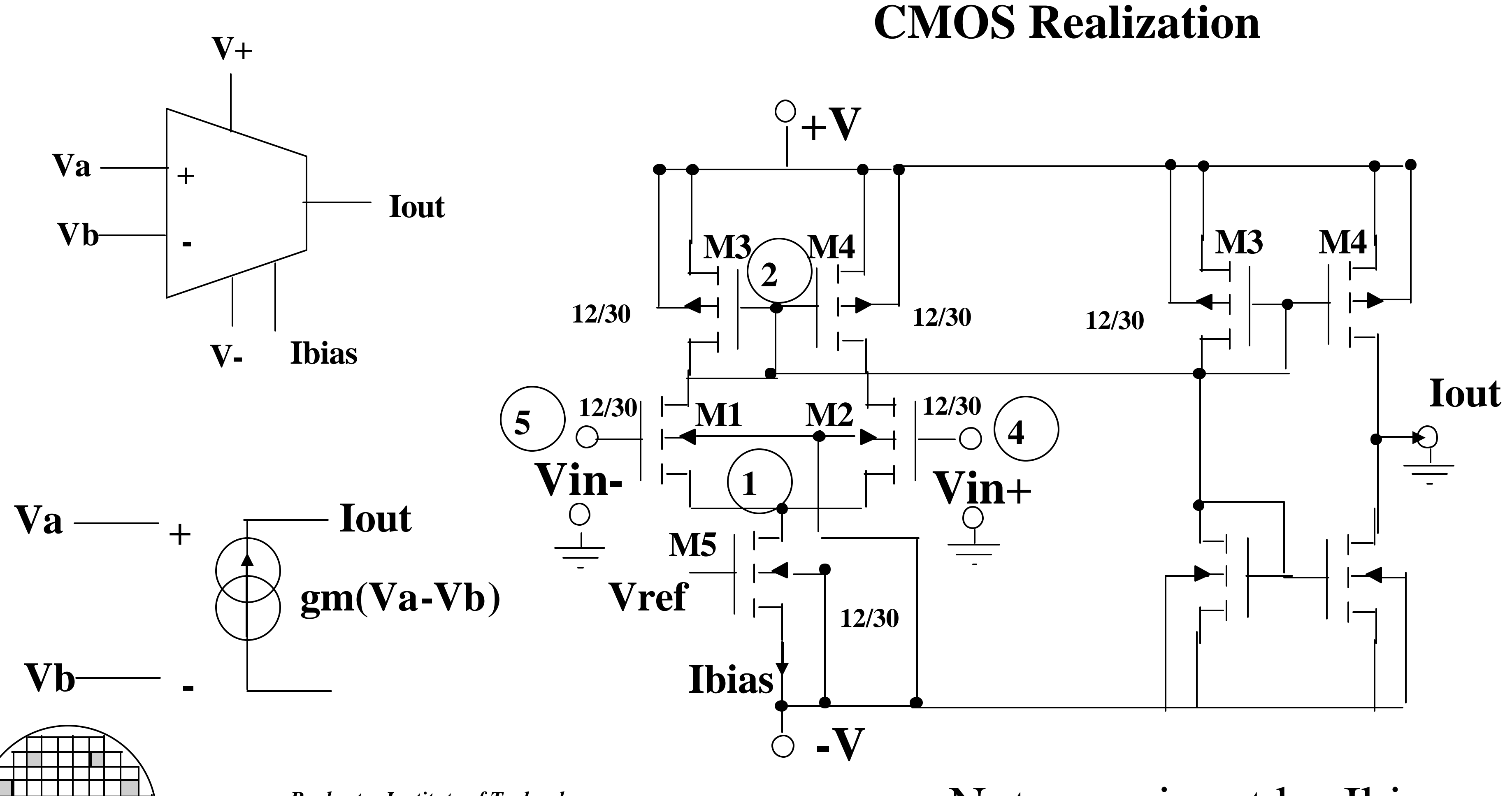
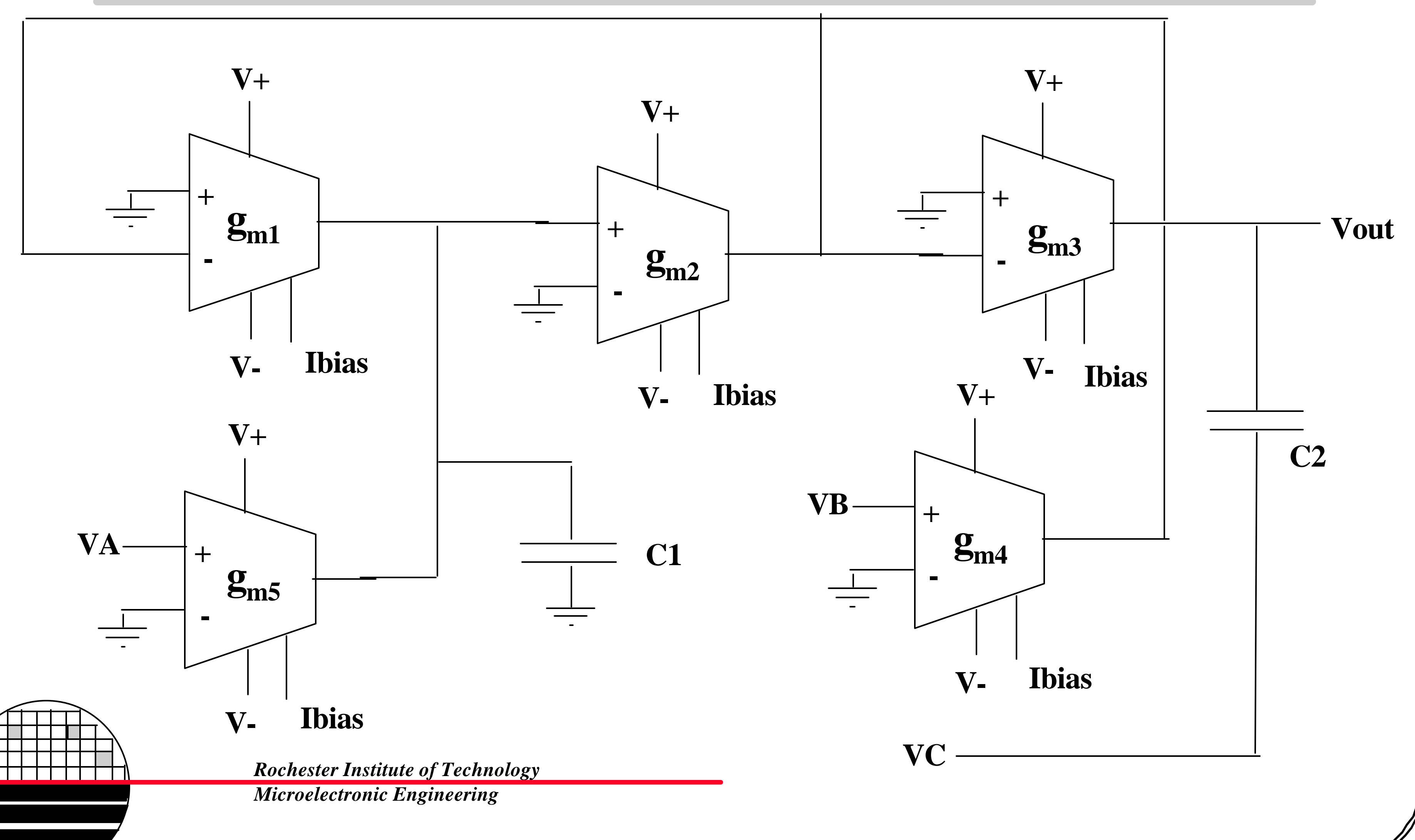
OPERATIONAL TRANSCONDUCTANCE AMPLIFIER



Note: gm is set by Ibias

BIQUAD FILTER



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BIQUAD FILTER

$$V_{out} = (s^2C_1C_2V_c + s\,C_1\,g_{m4}\,V_b + g_{m2}\,g_{m5}\,V_a)/(s^2C_1C_2 + sC_1g_{m3} + g_{m2}g_{m1})$$

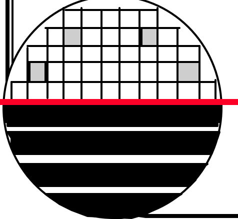
This filter can be used as a low-pass, high-pass, bandpass, bandrejection and all pass filter. Depending on the C and gm values a Butterworth, Chebyshev, Elliptic or any other configuration can be achieved

For example: let Vc=Vb=0 and Va=Vin, also let all g_m be equal, then

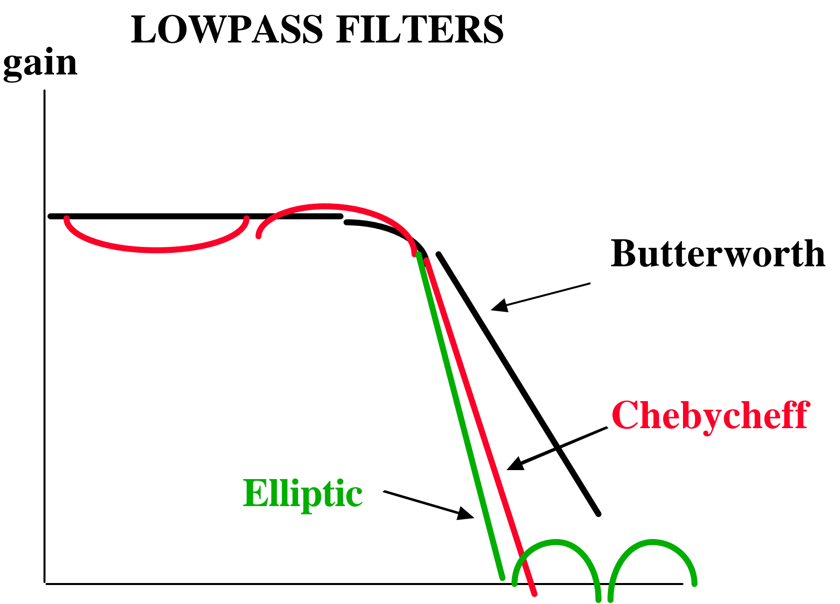
$$Vout = Vin\,/\,(s^2C_1C_2/\,g_mg_m + sC_1/g_m + 1)$$

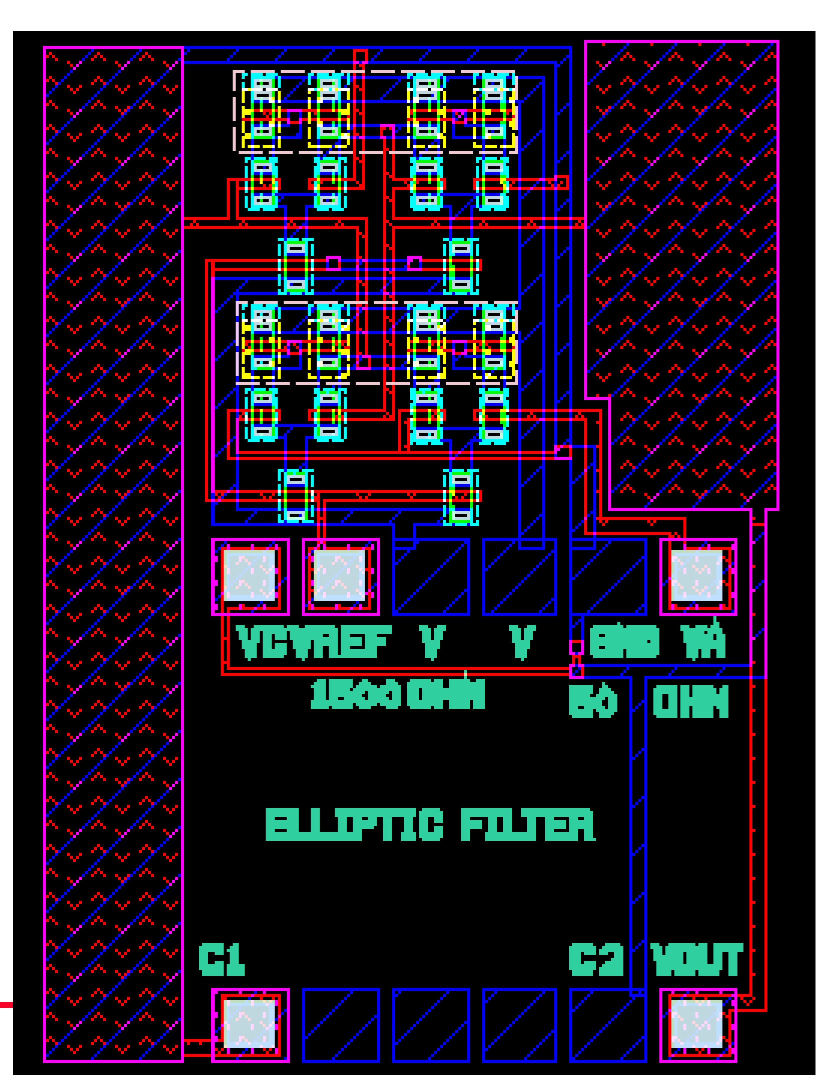
which is a second order low pass filter with corner frequency at

$$\omega_c = g_m/\sqrt{C_1C_2} \quad \text{and } Q = \sqrt{C_2/C_1}$$



OTA, BIQUAD ELLIPTIC FILTER





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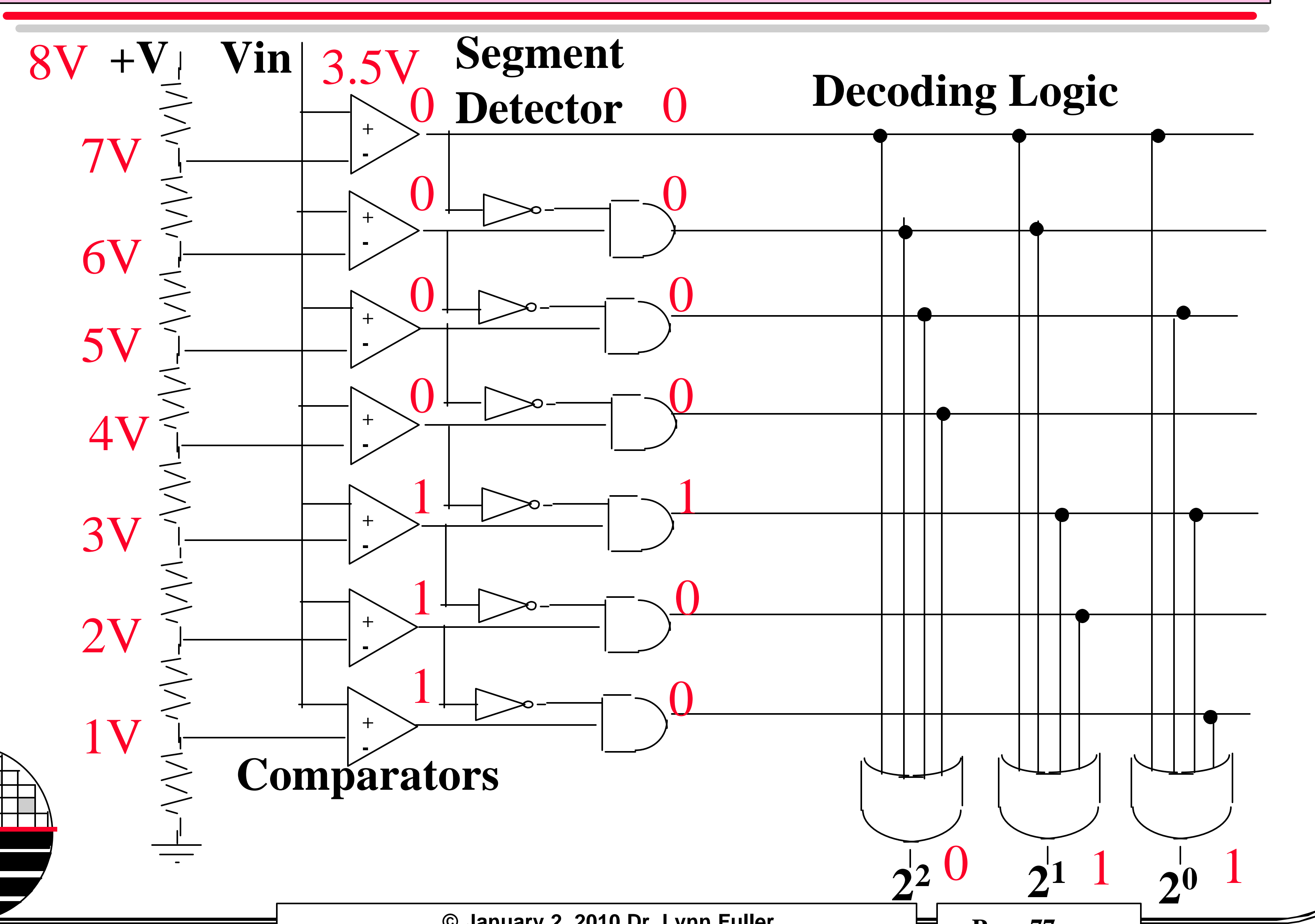
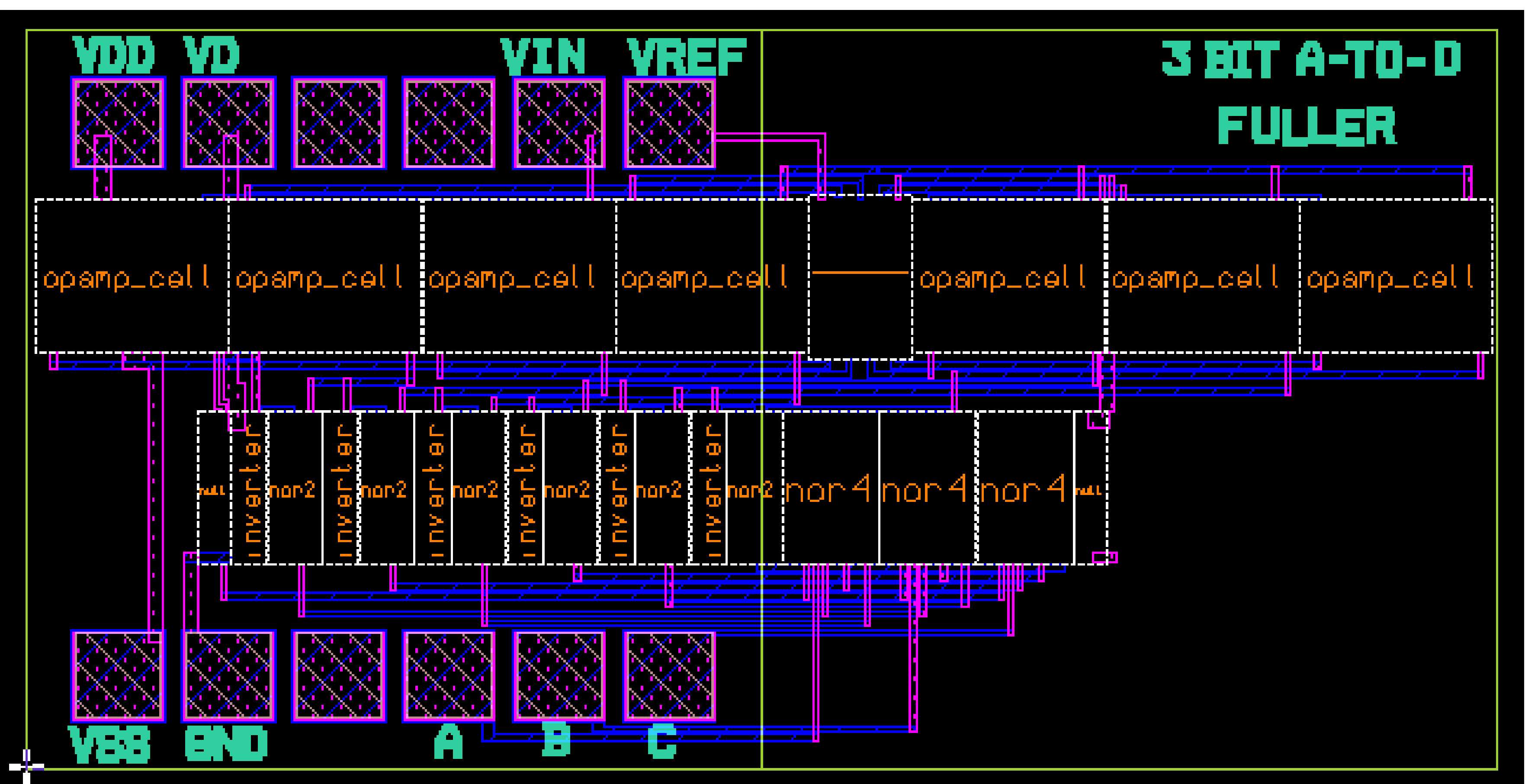
3 BIT ANALOG TO DIGITAL CONVERTER



3 BIT ANALOG TO DIGITAL CONVERTER



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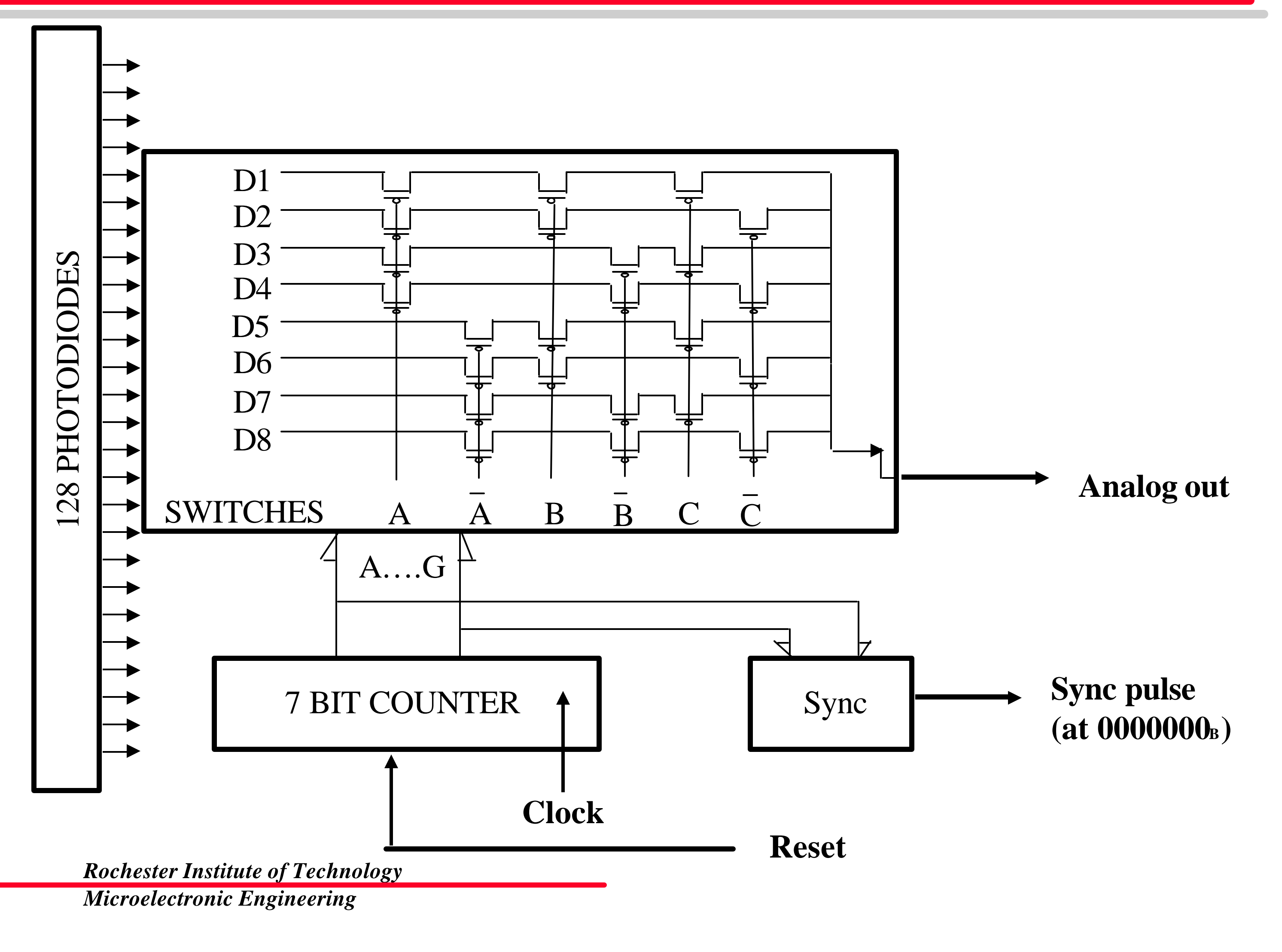
ANALOG MULTIPLEXER



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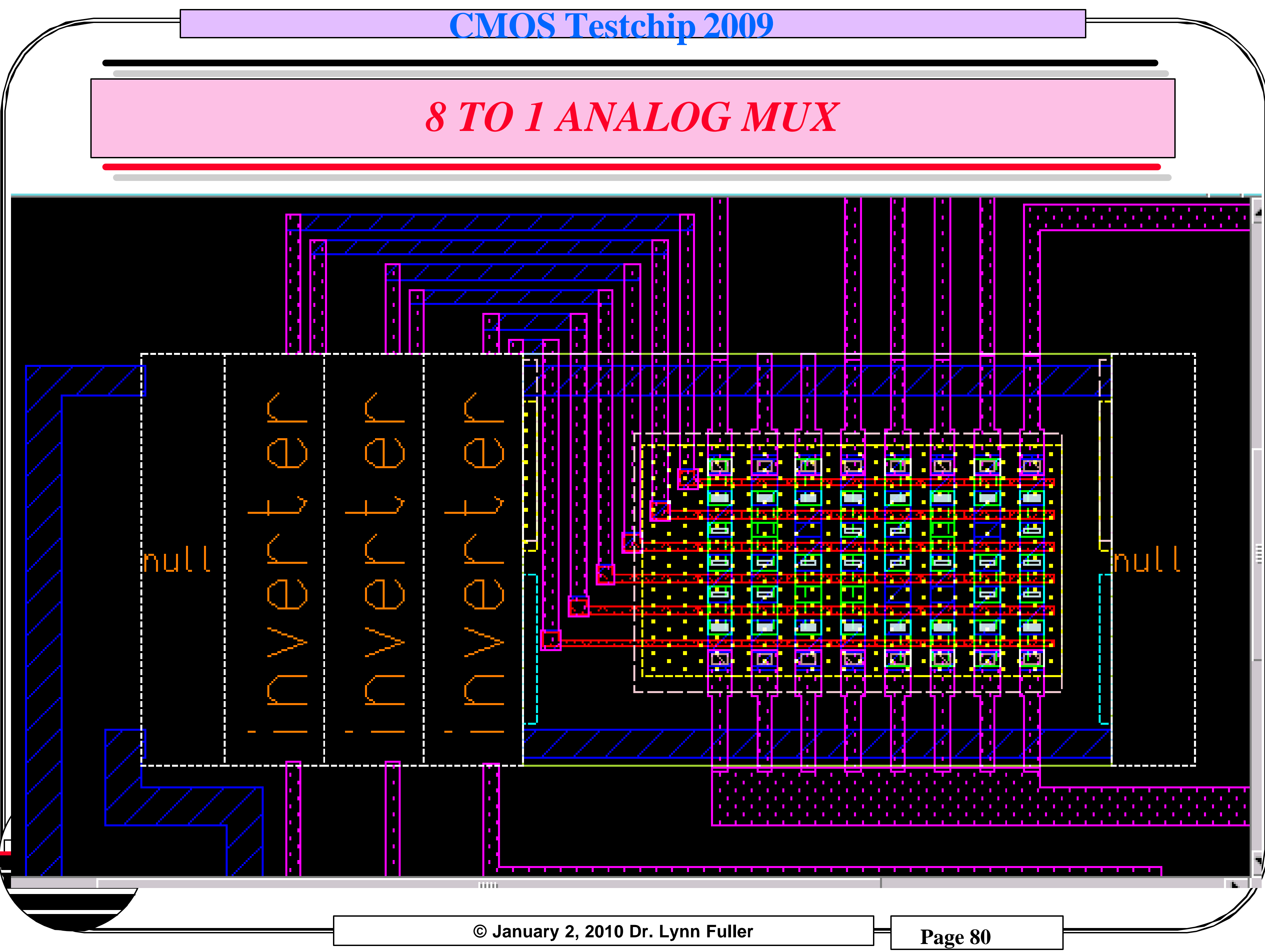
8 TO 1 ANALOG MUX



3 BIT D TO A

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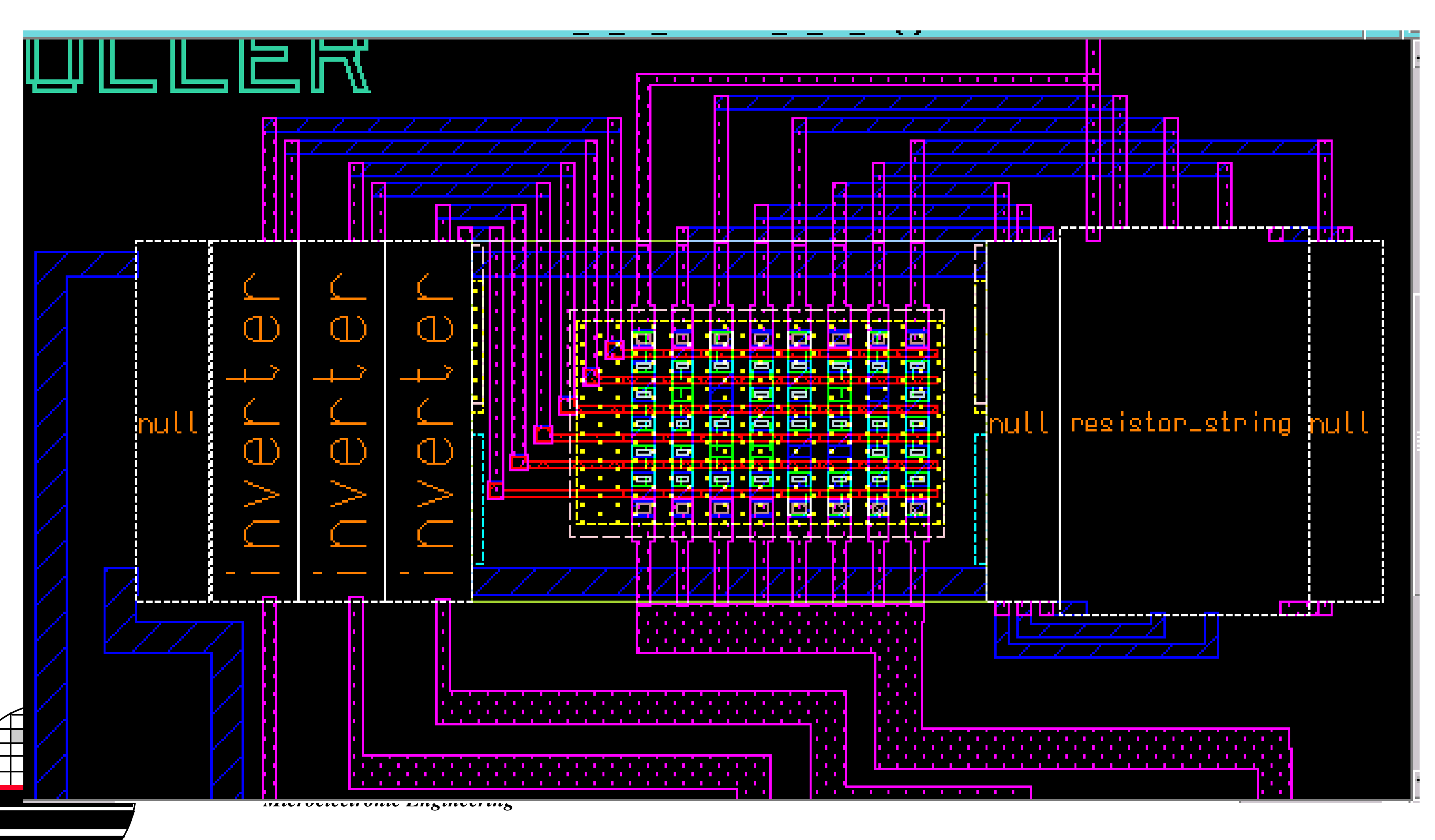
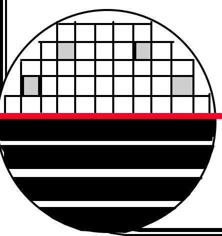
3 BIT D TO A



PROJECTS

Wireless Capacitive Sensor
MEMS Pressure Sensor
Spectro Photometer
Hearing Aid
CCD
CCD Imager



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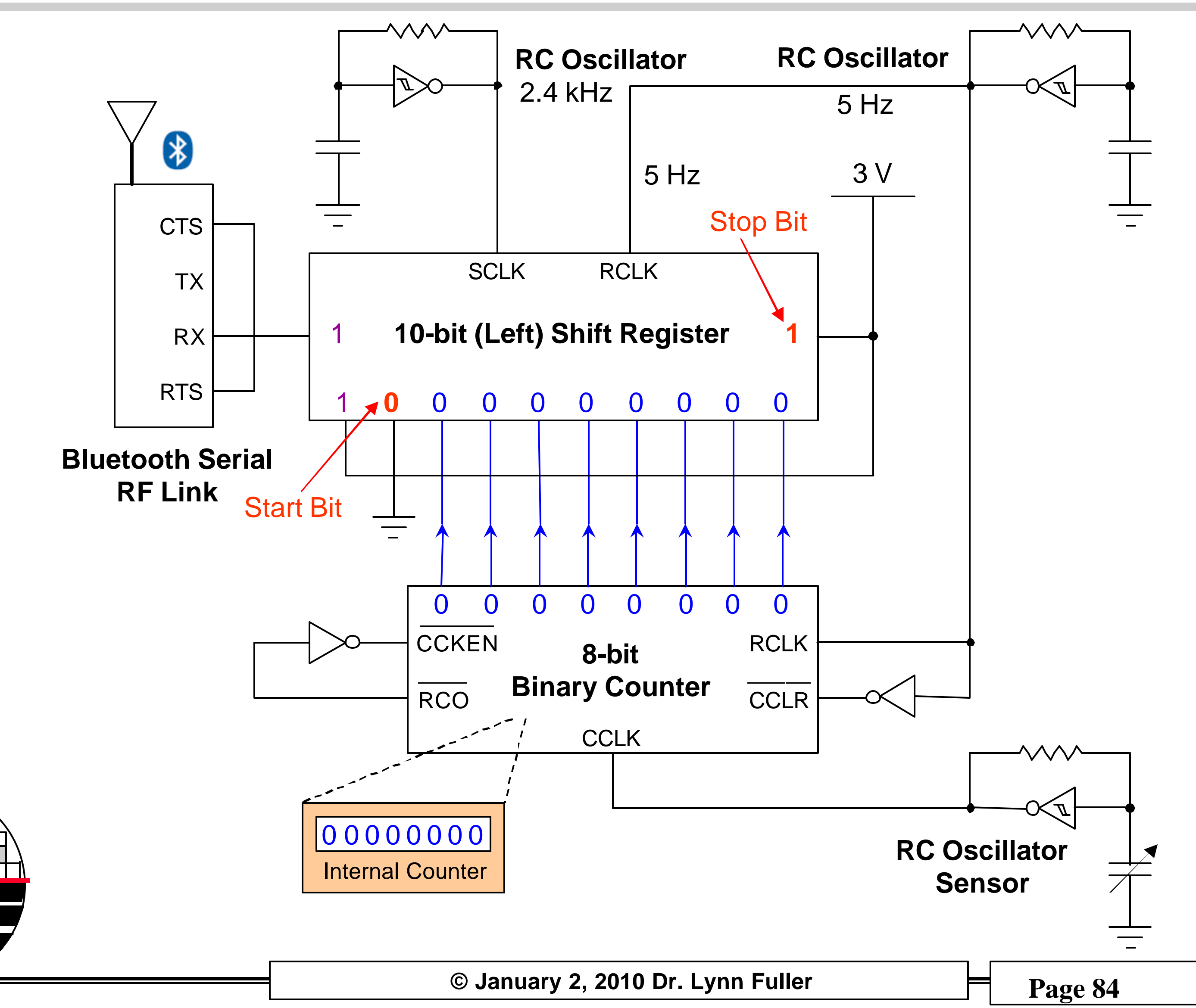
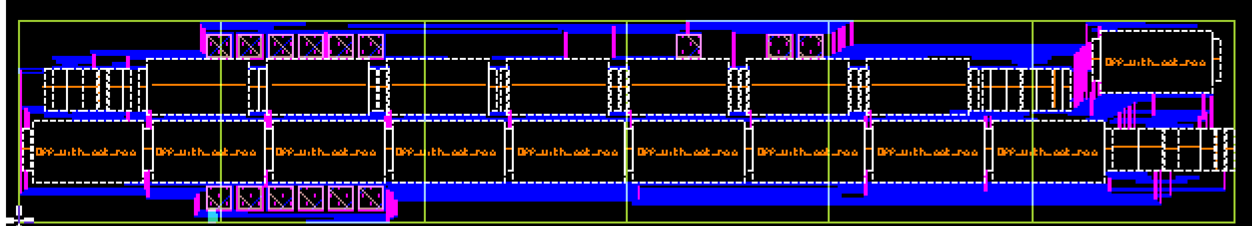
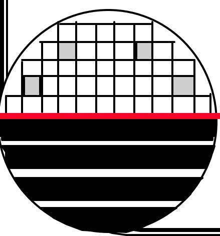
WIRELESS CAPACITIVE SENSOR PROJECT



WIRELESS CAPACITIVE SENSOR PROJECT





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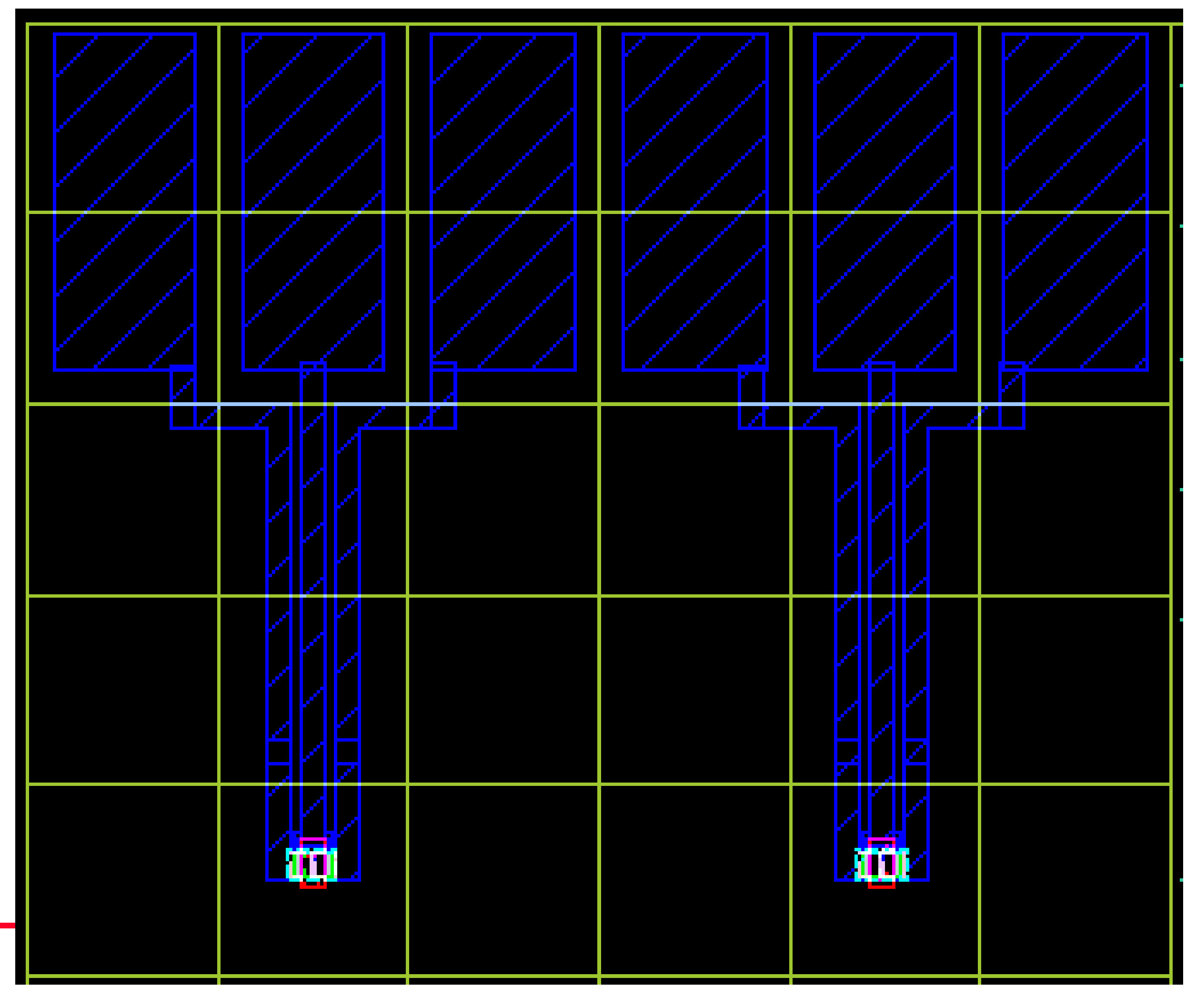
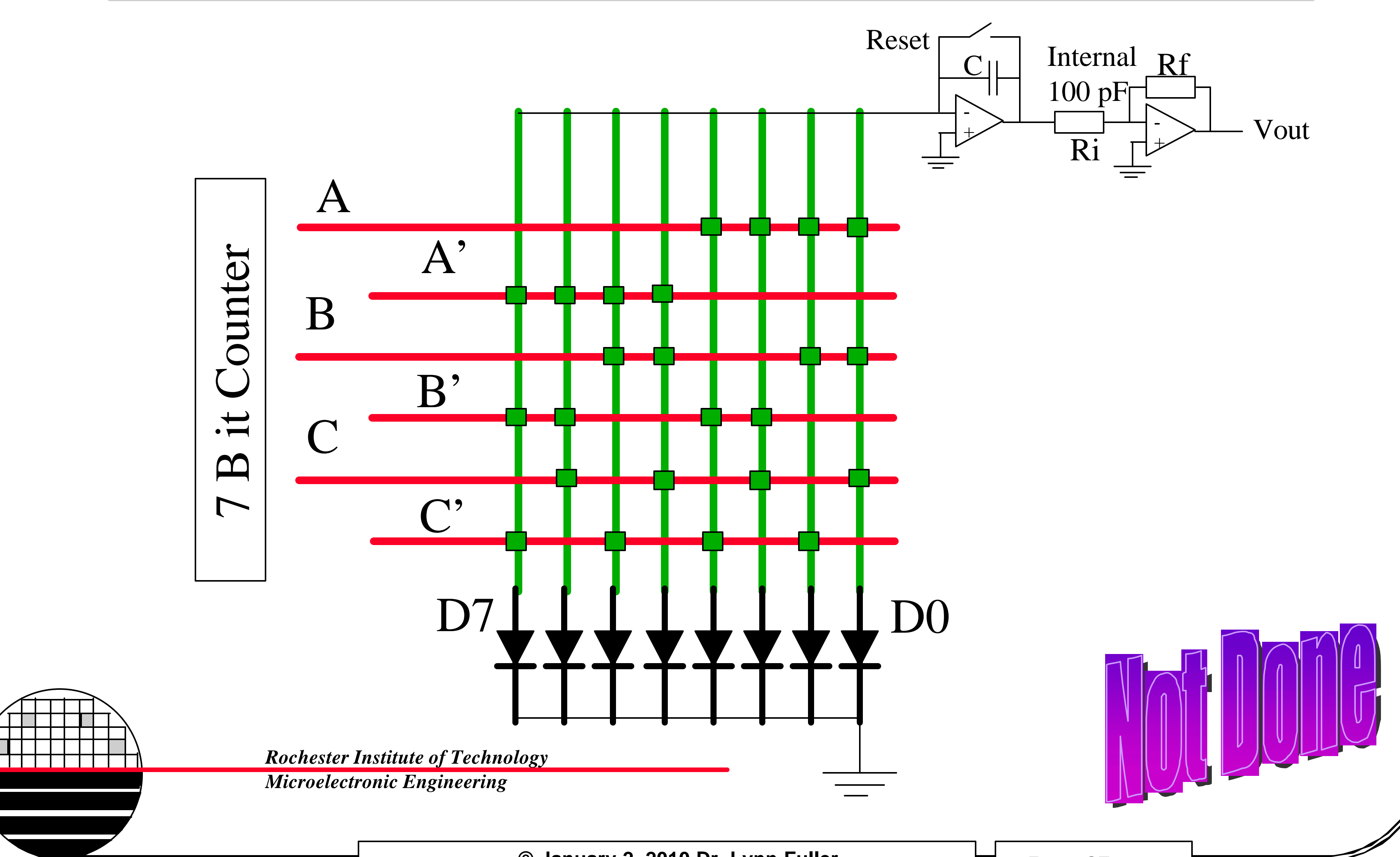
MEMS PRESSURE SENSOR



SPECTRO PHOTOMETER PROJECT



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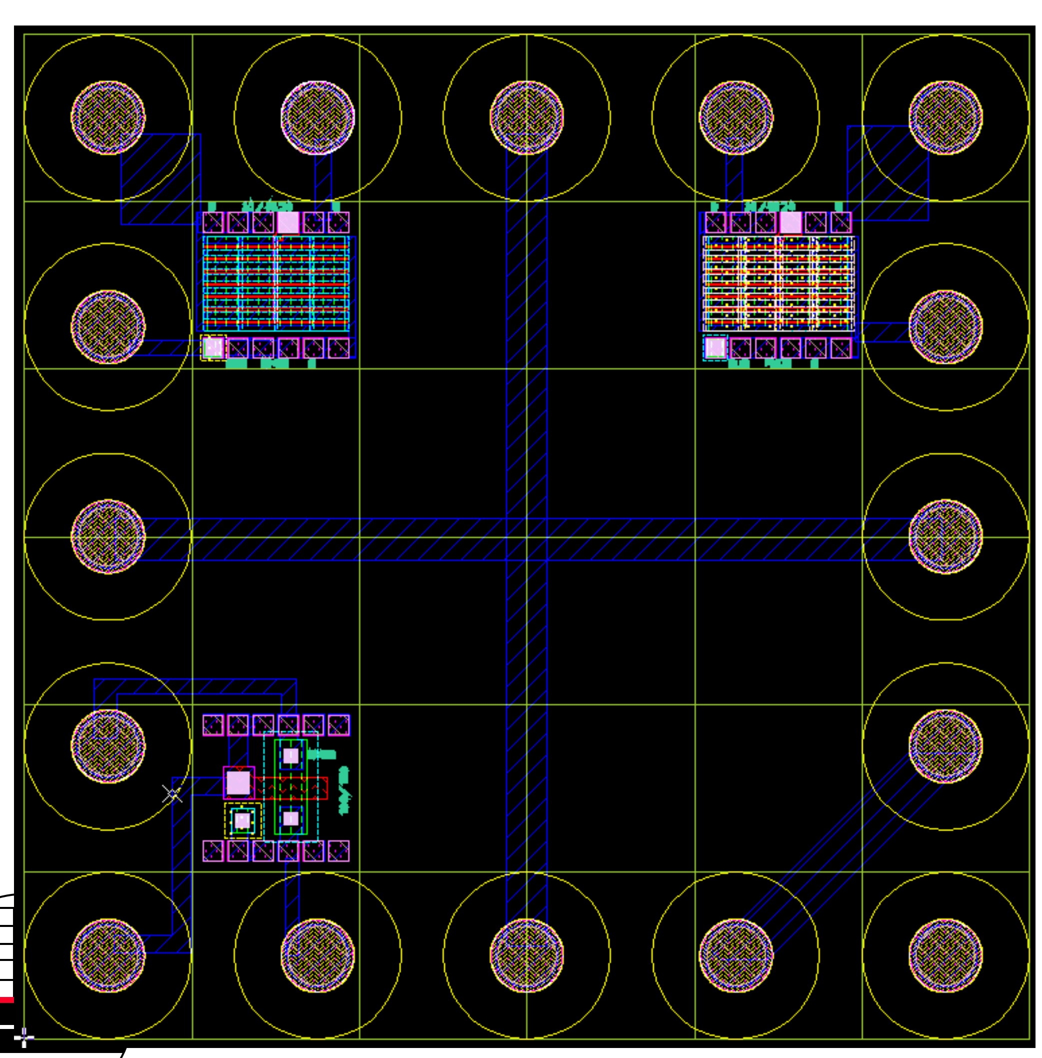
SOLDER BUMP TEST CHIP

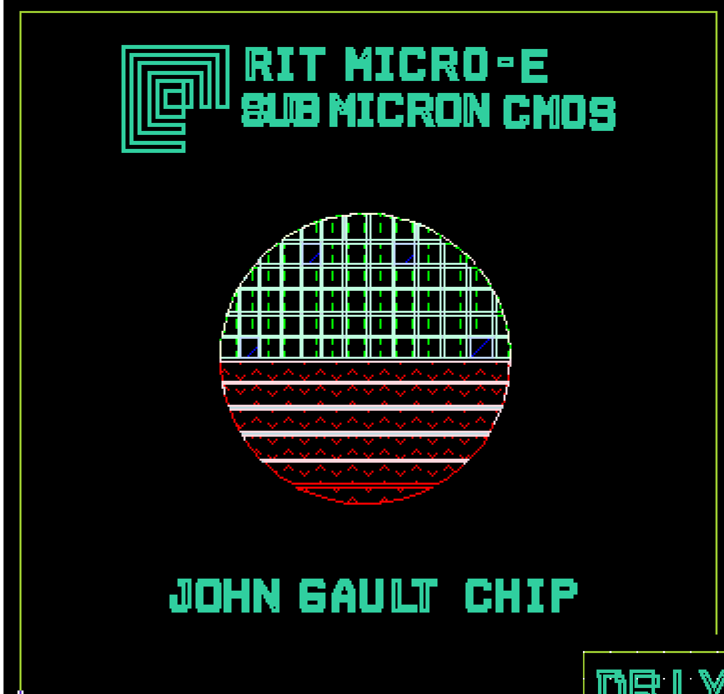


1000µm center-to-center
225µm diameter circle

Under bump metal is Cr/Ni and is defined by a lift-off lithography.

The solder is printed using a 150um photoresist and solder paste. (or 500um solder ball is placed over circle)

LOGO AND ACKNOWLEDGEMENTS



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IVAN PUCHADES
BURAK BAYLAV
TAL NAGOURNEY

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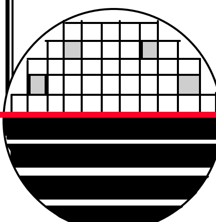
8. Digital Principles and Design, Donald Givone, 2003, pg 321
9. MOSIS SCMOS at http://www.mosis.com
10. Texas Instruments, Data Sheet for inverter with hysteresis.

HOMEWORK

1. Calculate the expected values of some of the resistor test structures.
2. Calculate the expected values of some of the capacitor test structures.



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