ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

CMOS Testing of First John Galt Chips

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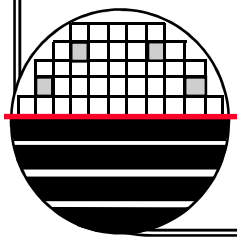
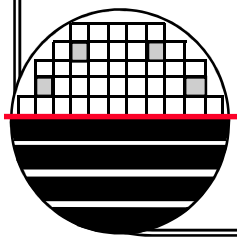


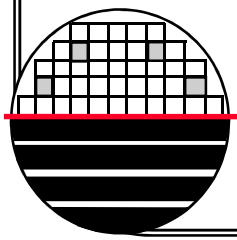
OUTLINE

Introduction
Process Technology
Design Rules
Chip Floor Plan
Structures for Fabrication Process and Evaluation
Sensors
Digital Circuits
Analog Circuits
Projects
References



INTRODUCTION

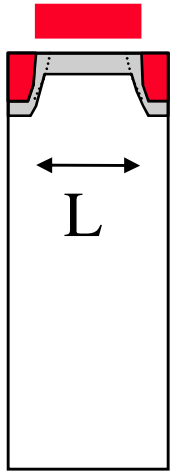
This document will describe a new CMOS test chip. The test chip will be used to develop CMOS process technology and to verify analog and digital circuit designs. In addition the test chip includes a variety of CMOS compatible sensors and signal processing electronics for those sensors. A section of the chip is for manufacturing process characterization and transistor parametric characterization. Other sections of the chip have basic digital and analog circuits, chip scale packaging designs and projects to evaluate various Microsystems architectures. For example a variable frequency oscillator, binary counter and shift register allows for capacitor sensor measurement and Blue-Tooth wireless transmission of data to a remote host. The test chip will be used with RIT's SUB-CMOS and ADV-CMOS processes.



RIT SUBμ CMOS

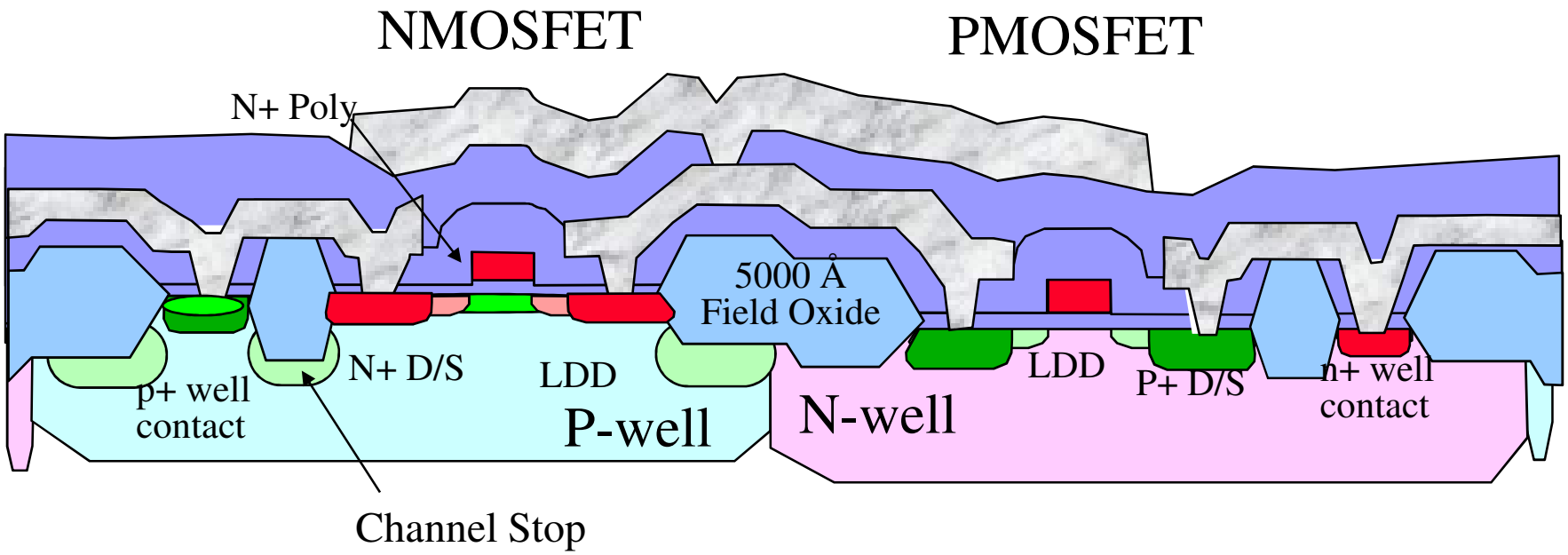
RIT Subμ CMOS

150 mm wafers
Nsub = 1E15 cm-3
Nn-well = 3E16 cm-3
Xj = 2.5 μm
Np-well = 1E16 cm-3
Xj = 3.0 μm
LOCOS
Field Ox = 6000 Å
Xox = 150 Å
Lmin= 1.0 μm
LDD/Side Wall Spacers
Vdd = 5 Volts, Vto= +/- 1 Volt
Two Layer Metal



Long Channel Behavior

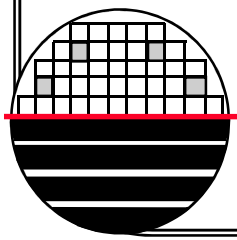
SUB-CMOS 150 CROSSECTION



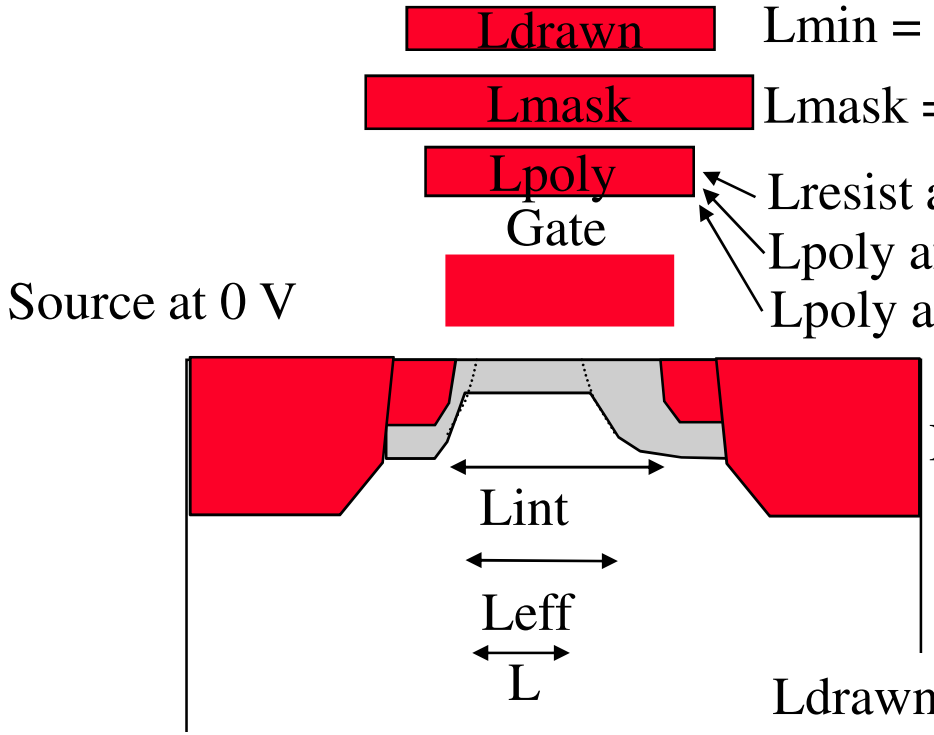
p-Type Substrate 10 ohm-cm

DESIGN RULES

We will use a modified version of the MOSIS TSMC 0.35 2P 4M design rules. Eventually we hope to be compatible with MOSIS but new process technology needs to be developed at RIT to do that (PECVD Tungsten, improved lithography overlay, 4 layer metal). We plan to use one layer of poly and two layers of metal. We will use the same design layer numbers with additional layers as defined on the following pages for manufacturing/maskmaking enhancements. Many of the designs will use minimum drawn poly gate lengths of 2µm where circuit architecture is the main purpose of the design. Minimum size devices (Drawn Poly = 0.5µm, etc.) are included to develop manufacturing process technology.



LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L



Lambda = design rule parameter, λ, ie	0.25µm
Lmin = min drawn poly length, 2λ	0.50µm
Lmask = ? Depends on +/-bias	1.00µm x 5
Lresist after photo (resist trimming??)	0.50µm
Lpoly after poly etch	0.40µm
Lpoly after poly reoxidation	0.35µm
	0.30µm
	0.20µm
	0.11µm

Ldrawn = what was drawn

Internal Channel Length, Lint =distance between junctions, including under diffusion
Effective Channel Length, Leff = distance between space charge layers,Vd = Vs= 0
Channel Length, L, = distance between space charge layers, when Vd= what it is
Extracted Channel Length Parameters = anything that makes the fit good (not real)

MOSIS TSMC 0.35 2POLY 4 METAL PROCESS

General Information
About MOSIS
Products
Processes
Prices
Support
User Group
Events
Job Openings
News

Work with MOSIS
Overview
Getting Started
Design and Test

Requests
Run Status
Project Status
Test Data

Docs and Forms
Documents
Forms/Agreements
Web Forms

Quick Reference
New Users
Experienced Users
Purchasing Agents
Design and Test
Academic Institutions
Export Program
Submit A Project

Search MOSIS
Search

http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html#tech-codes

MOSIS SCMOS Technology Codes and Layer Maps

SCN4M and SCN4M_SUBM

This is the layer map for the technology codes SCN4M and SCN4M_SUBM using the MOSIS Scalable CMOS layout rules (SCMOS), and only for SCN4M and SCN4M_SUBM. For designs that are laid out using other design rules (or technology codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

SCN4M: Scalable CMOS N-well, 4 metal, 1 poly, silicided. Silicide block and thick oxide option available only on the TSMC process.

SCN4M_SUBM: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

Fabricated on TSMC, AMIS, and Agilent/HP 0.35 micron process runs. See "Notes" section of layer map for foundry-specific options.

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	
ACTIVE	43	CAA		2	
THICK_ACTIVE	60	CTA		24	Optional for TSMC; not available for Agilent/HP nor AMIS
POLY	46	CPG		3	
SILICIDE_BLOCK	29	CSB		20	Optional for Agilent/HP; not available for AMI
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	
METAL3	62	CM3	CMT	15	
VIA3	30	CV3	CVT	21	
METAL4	31	CM4	CMQ	22	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME

MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

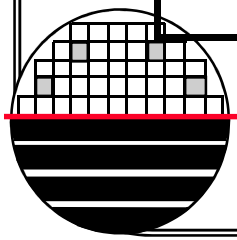
MASK LAYER NAME	MENTOR NAME	GDS #	COMMENT
N WELL	N_well.i	42	
ACTIVE	Active.i	43	
POLY	Poly.i	46	
N PLUS	N_plus_select.i	45	
P PLUS	P_plus_select.i	44	
CONTACT	Contact.i	25	Active_contact.i 48 poly_contact.i 47
METAL1	Metal1.i	49	
VIA	Via.i	50	
METAL2	Metal2.i	51	
VIA2	Via2.i	61	Under Bump Metal
METAL3	Metal3.i	62	Solder Bump

These are the main design layers up through metal two

MORE LAYERS USED IN MASK MAKING

LAYER	NAME	GDS	COMMENT
	cell_outline.i	70	Not used
	alignment	81	Placed on first level mask
	nw_res	82	Placed on nwell level mask
	active_lettering	83	Placed on active mask
	channel_stop	84	Overlay/Resolution for Stop Mask
	pmos_vt	85	Overlay/Resolution for Vt Mask
	LDD	86	Overlay/Resolution for LDD Masks
	p plus	87	Overlay/Resolution for P+ Mask
	n plus	88	Overlay/Resolution for N+ Mask
	tile_exclusion	89	Areas for no STI tiling

These are the additional layers used in layout and mask making



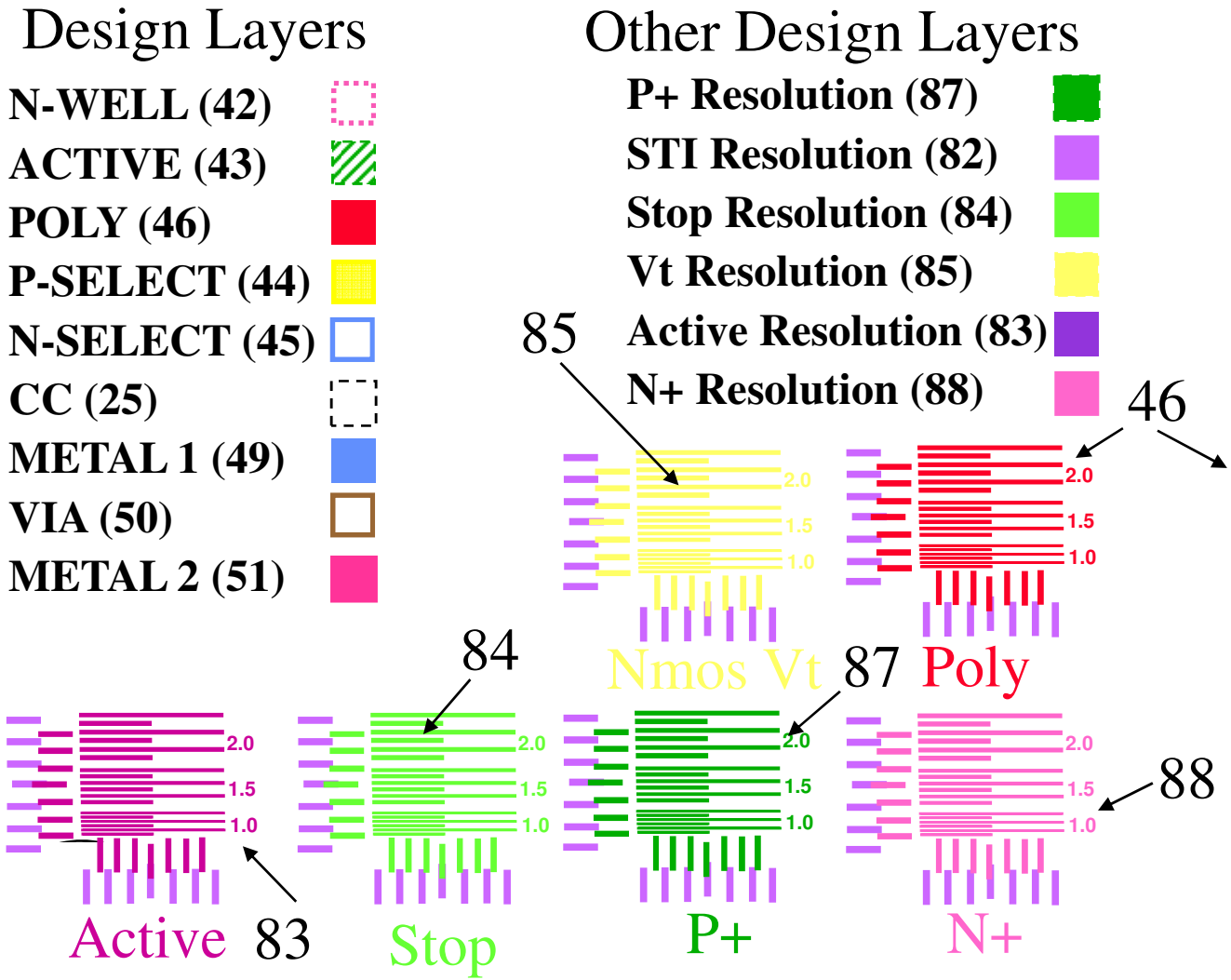
OTHER LAYERS

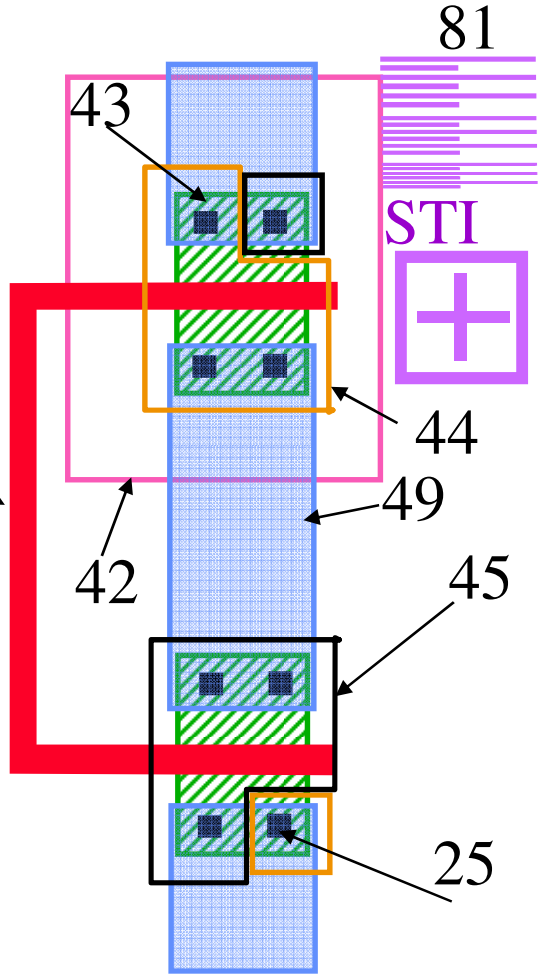
Design Layers

- N-WELL (42)
- ACTIVE (43)
- POLY (46)
- P-SELECT (44)
- N-SELECT (45)
- CC (25)
- METAL 1 (49)
- VIA (50)
- METAL 2 (51)

Other Design Layers

- P+ Resolution (87)
- STI Resolution (82)
- Stop Resolution (84)
- Vt Resolution (85)
- Active Resolution (83)
- N+ Resolution (88)





MASK ORDER FORM

Rochester Institute of Technology
Microelectronic Engineering

Date 6/25/2008
Requestor Dr. Lynn Fuller

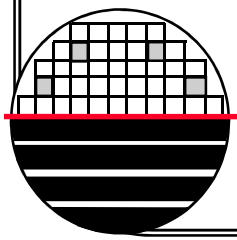
Attachment for Mask Order Form

Design Descripti CMOS_TESTCHIP_2008_final **gdr File:** /shared/smartertchip_2007/CMOS_TESTCHIP_2008_final.g

cture Resolution	0.5	**Mirror**	135
Scale Factor	5X	**Rotate**	none
Array	none		

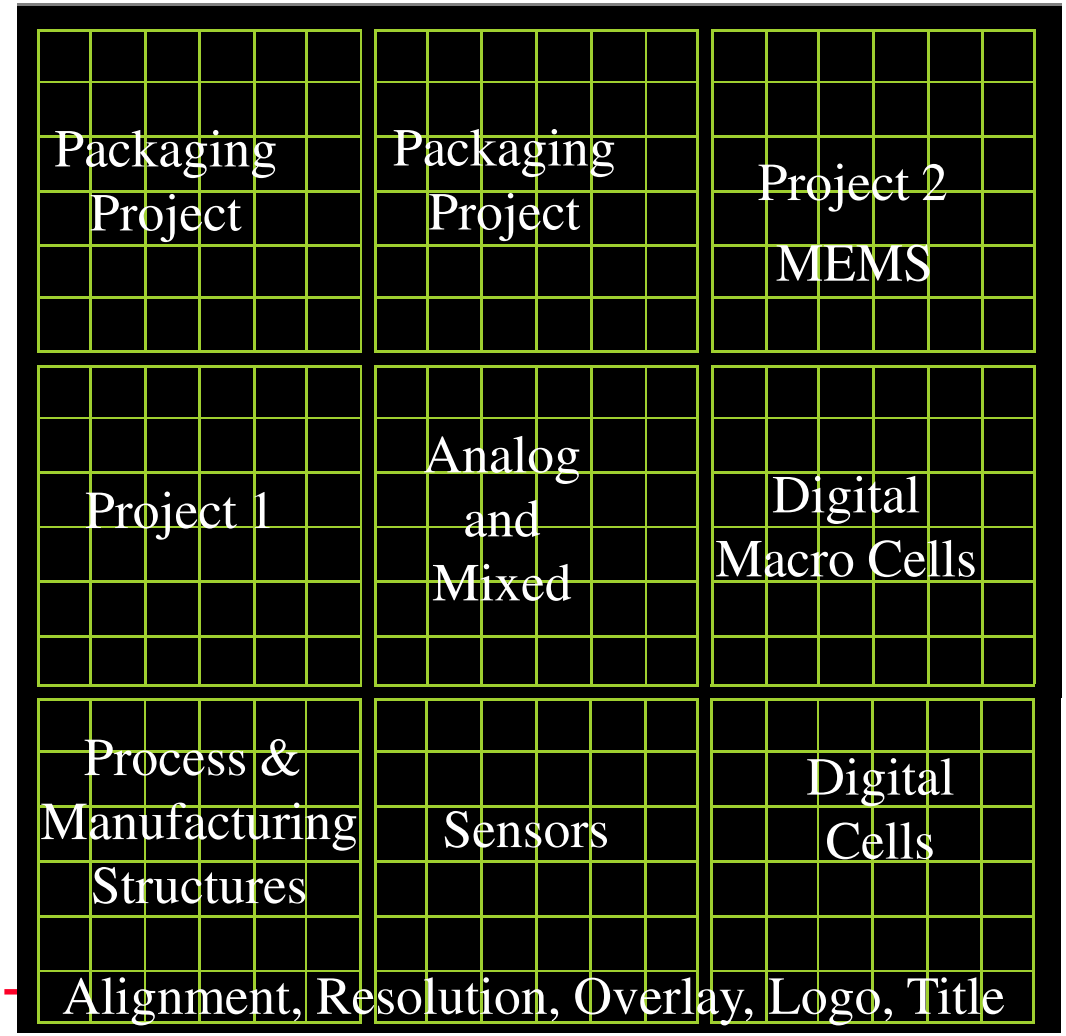
Plate Size	5"x5"x0.090"
# of levels/plat	1

Design Layer Name	Number	Mark Level Name	Number	Boolean Function	Comments
NWELL	1	n-well.i	42	(42 OR 81 OR 82) INVERT	Dark Field Mark
		alignment	81		
		nu_rer	82		
ACTIVE	2	active-area.i	43	(43 OR 83)	Clear Field Mark
		active-area.e	83		
STOP	3	n-well.i	42	(42 OR 84)	Clear Field Mark
		channel_stop	84		
PMOSVT	4	p_plus_select.i	44	(44 OR 85)	Dark Field Mark
		pmos_vt	85		
POLY	5	poly.i	46	none	Clear Field Mark, Biar layer 6 +0.5µm
LDD-N	6	n_plus_select.i	45	(45 OR 86) INVERT	Dark Field Mark
		LDD	86		
LDD-P	7	p_plus_select.i	44	(44 OR 86) INVERT	Dark Field Mark
		LDD	86		
N+DS	9	n_plus_select.i	45	(45 OR 88) INVERT	Dark Field Mark
		n plus	88		
P+DS	9	p_plus_select.i	44	(44 OR 87) INVERT	Dark Field Mark
		p plus	87		
CC	10	contact	25	(25 OR 87 OR 47) INVERT	Dark Field Mark
		Active_contact	48		
		Poly_contact.i	47		
METAL1	11	metal1.i	49	none	Clear Field Mark
VIA	12	Via.i	50	INVERT	Dark Field Mark
METAL2	13	metal2.i	51	none	Clear Field Mark
VIA2	14	Via2	61	none	Dark Field Mark
METAL3	15	metal3	62	none	Clear Field Mark



FLOORPLAN AND HIERARCHY

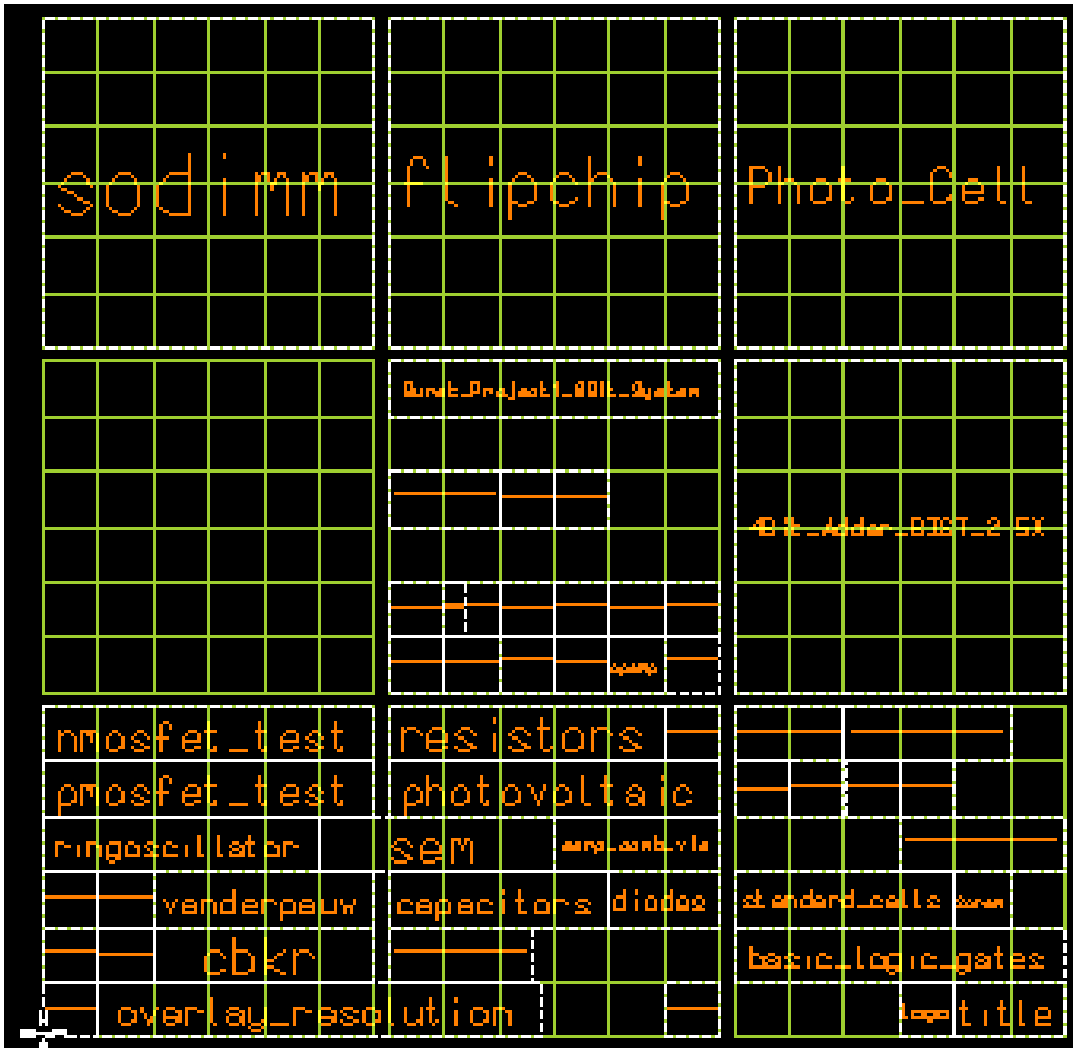
CMOSTestchip2007
- Process
- Digital
  - Primitive Cells
  - Basic Cells
  - Macro Cells
- Analog & Mixed Projects
  - Packaging
  - MEMS
  - Project 1
  - Project2



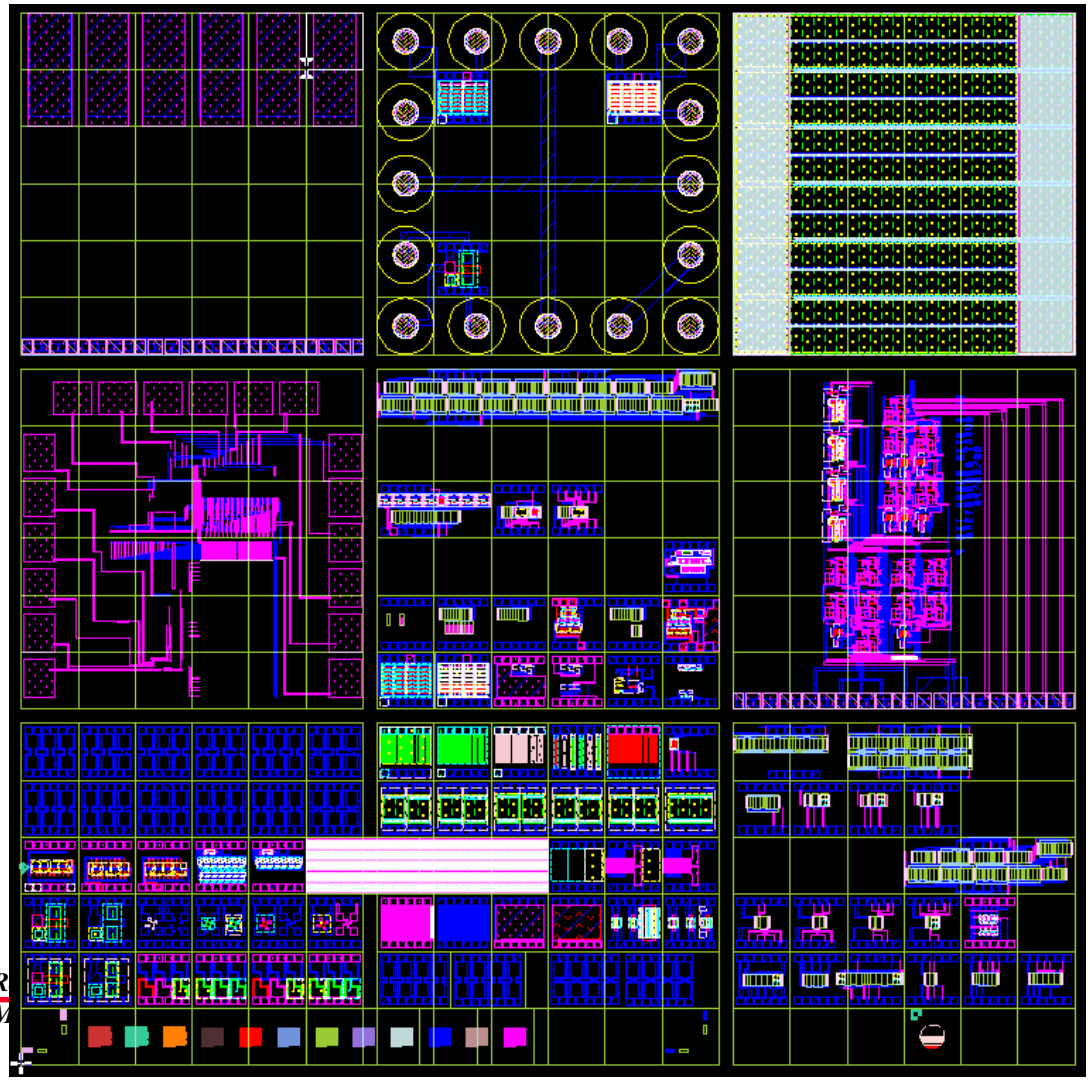
OVERALL CHIP LAYOUT

(14800,14800)

The test chip is divided into nine cells each 5 mm by 5 mm. The cells are divided into 36 individual tiny cells each 800 µm by 800 µm in size plus 200 µm sawing streets. Most structures fit into the tiny cells including a 12 probe pad layout for probe card testing. The overall chip size is 14800 µm by 14800µm plus 200 µm sawing street to give x and y step size of 15 mm by 15 mm.

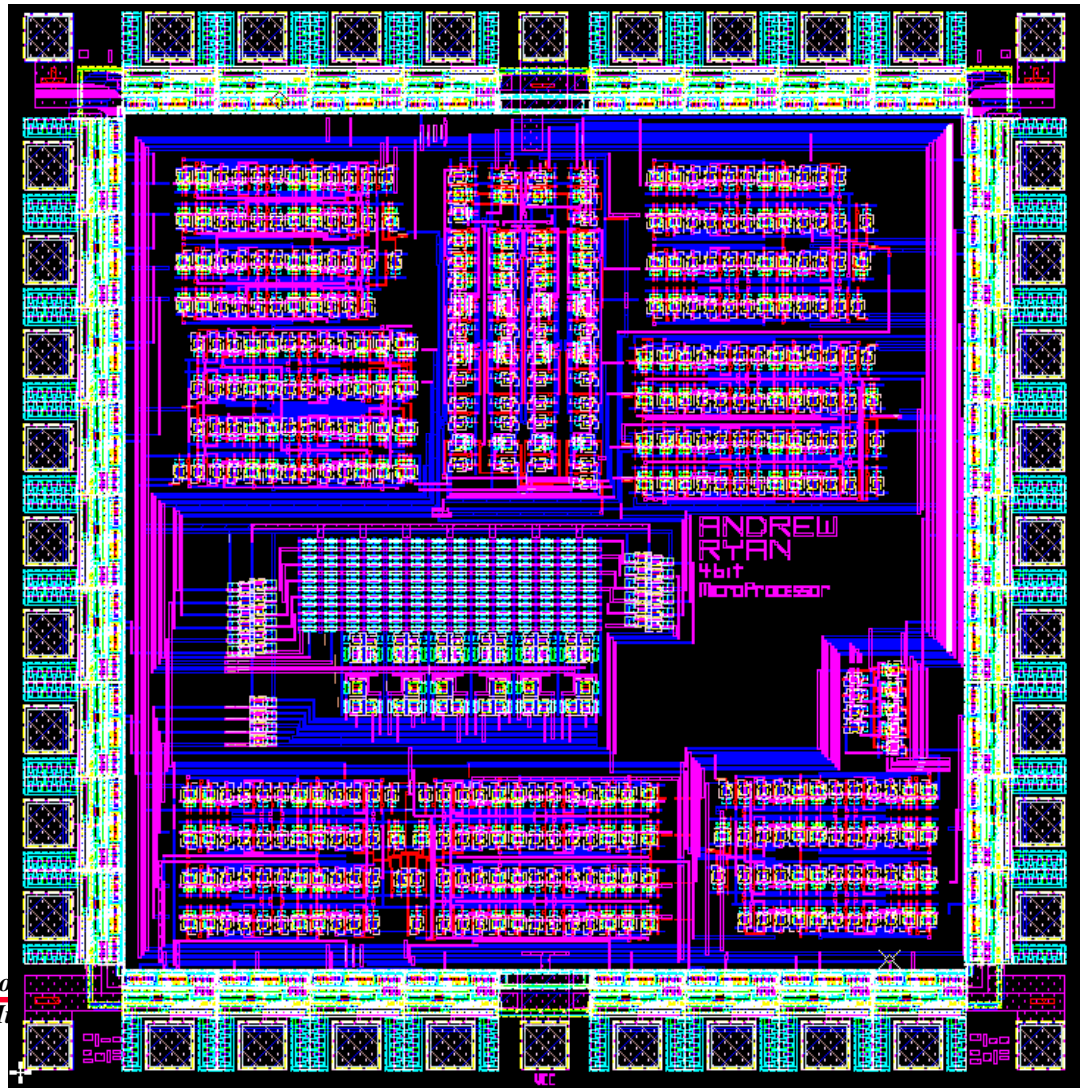


JOHN GALT CMOS TESTCHIP

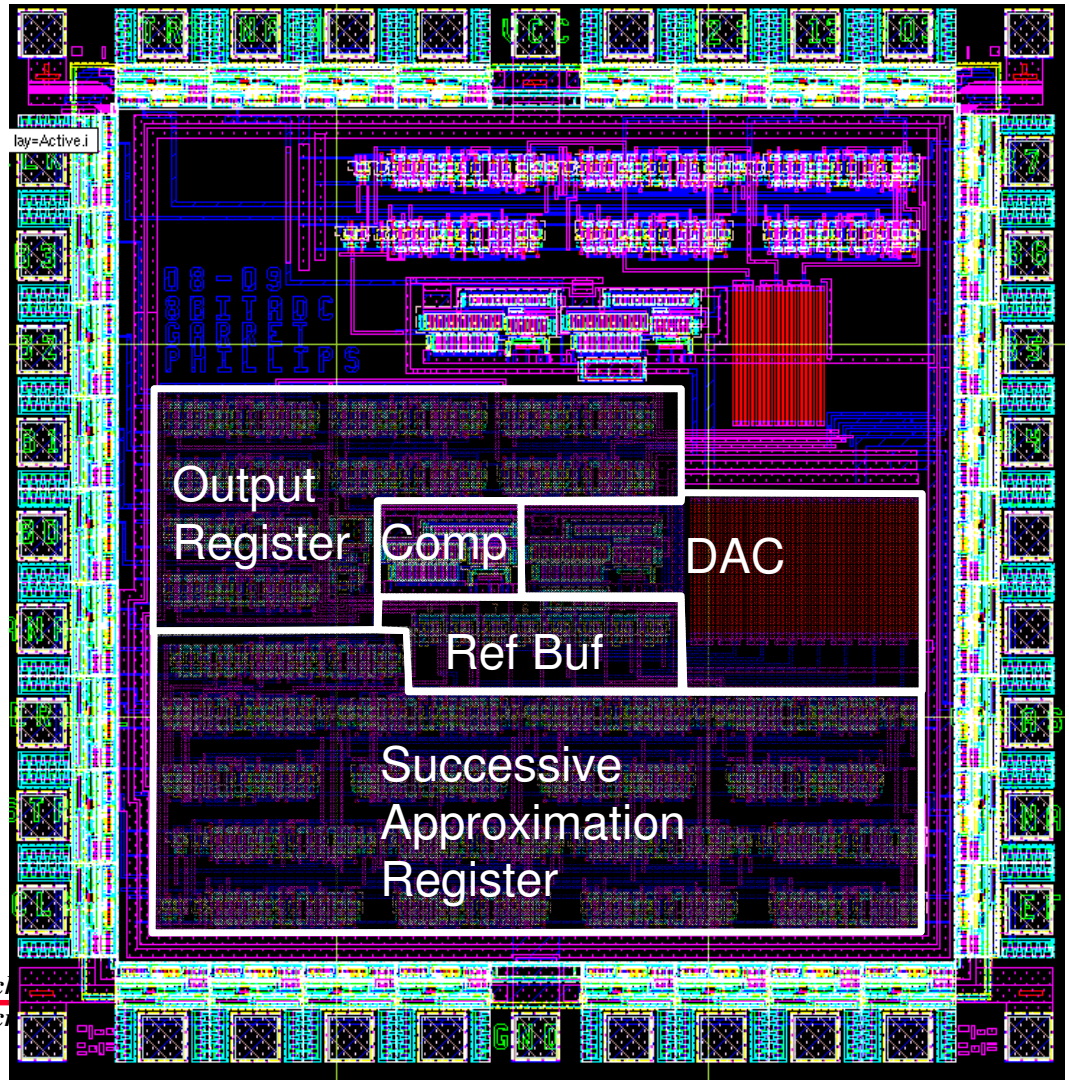


2008

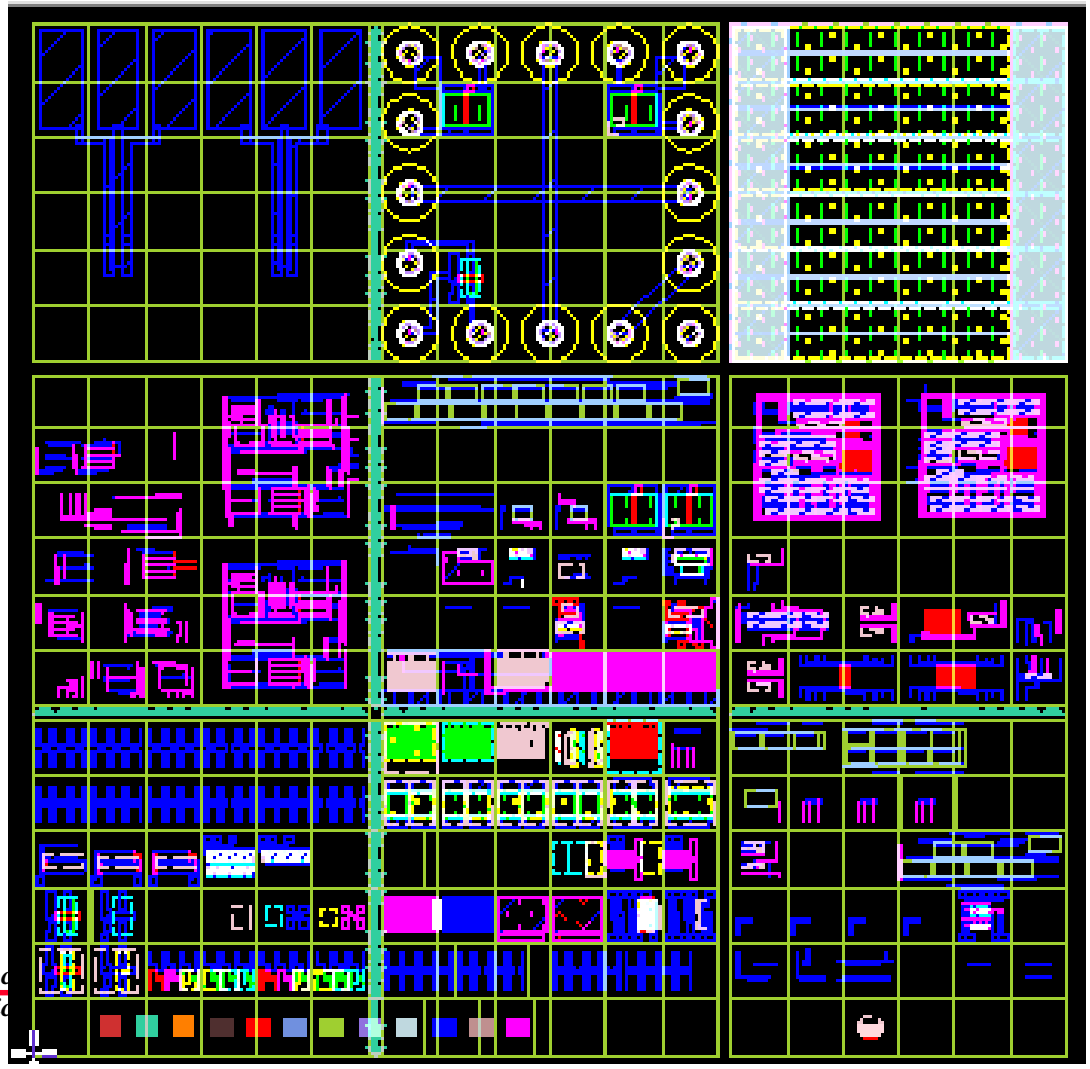
4-BIT MICROPROCESSOR



ANALOG TO DIGITAL CONVERTER

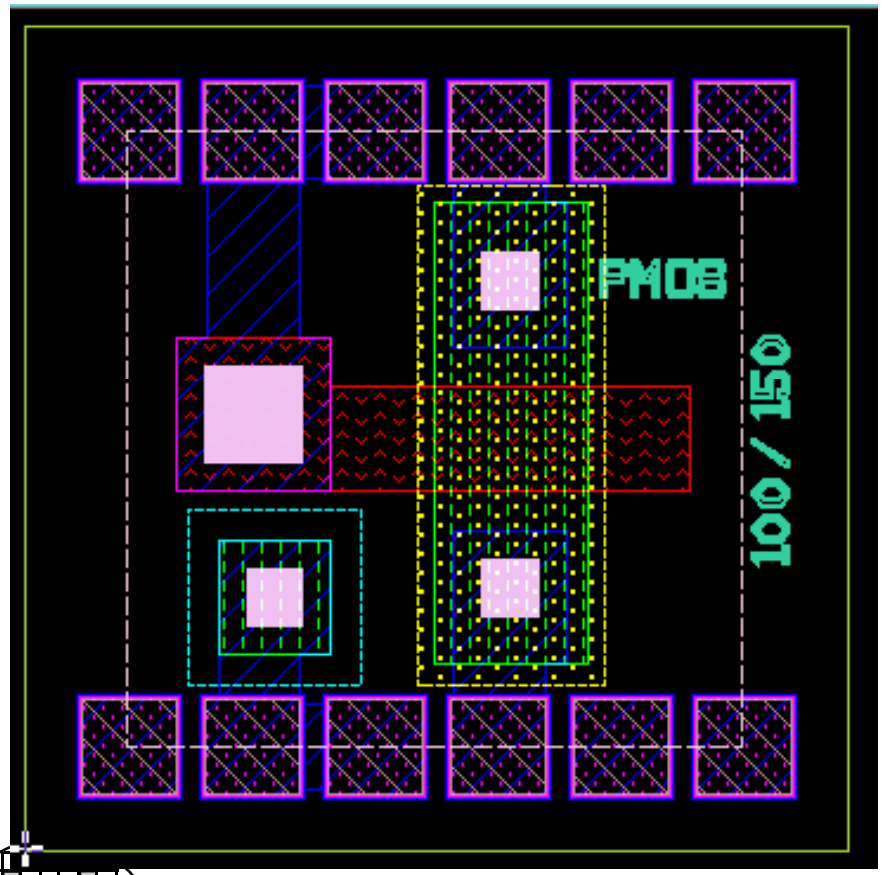


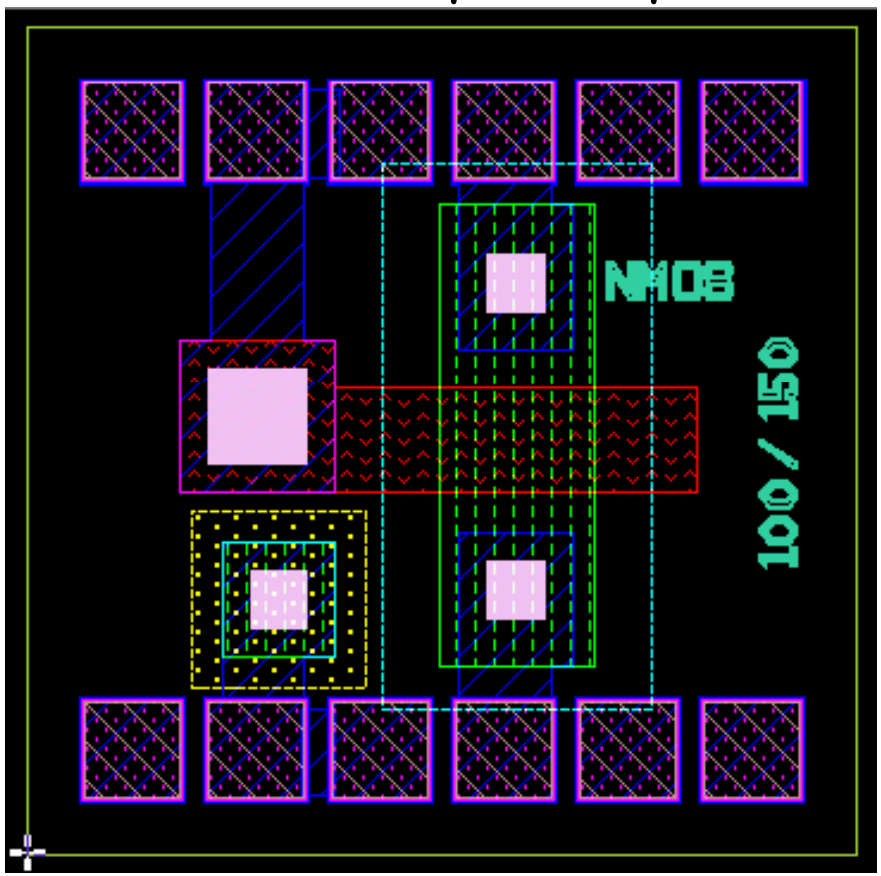
NEW JOHN GALT 2010



BIG NMOS AND PMOS FETS

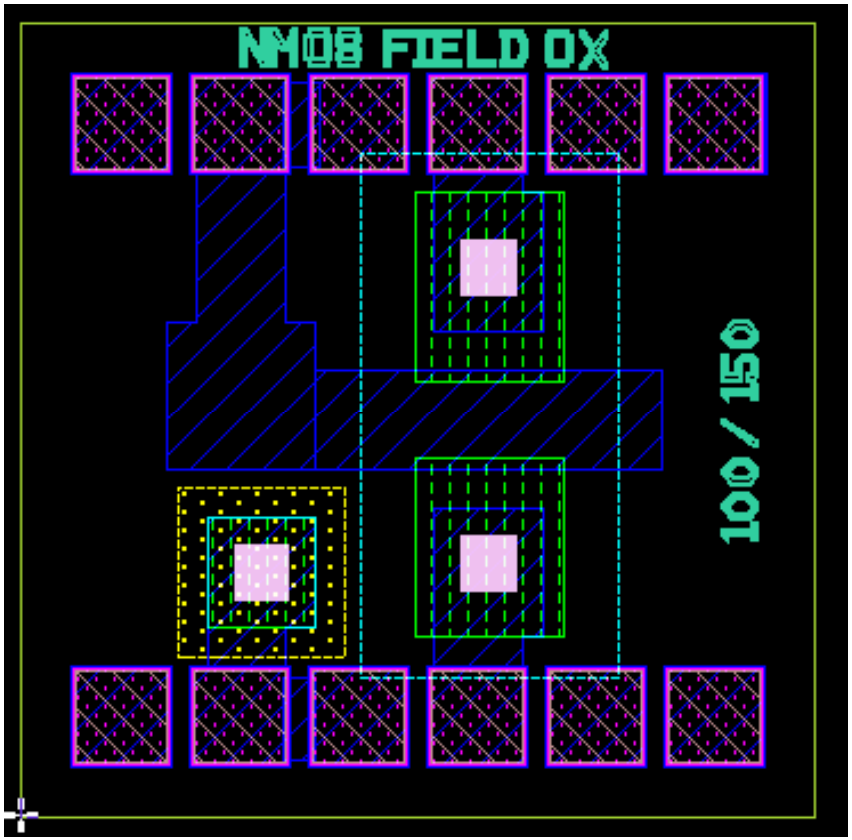
L/W = 100µm/150µm

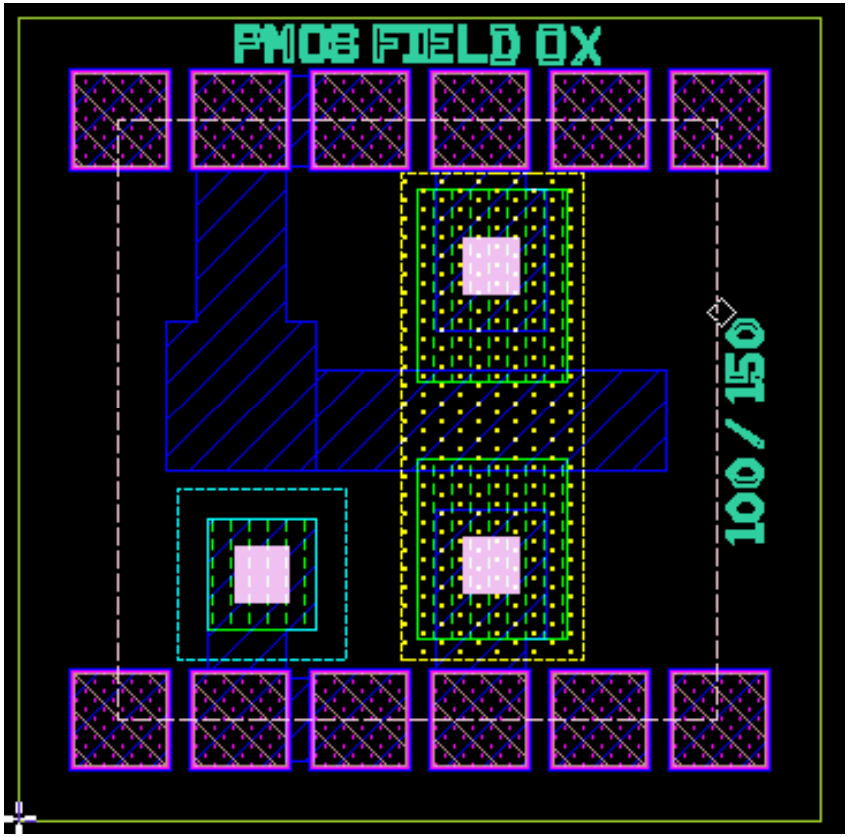


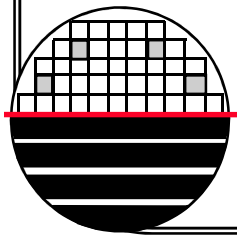


Big enough for easy Nanospec Measurements
Not for device testing

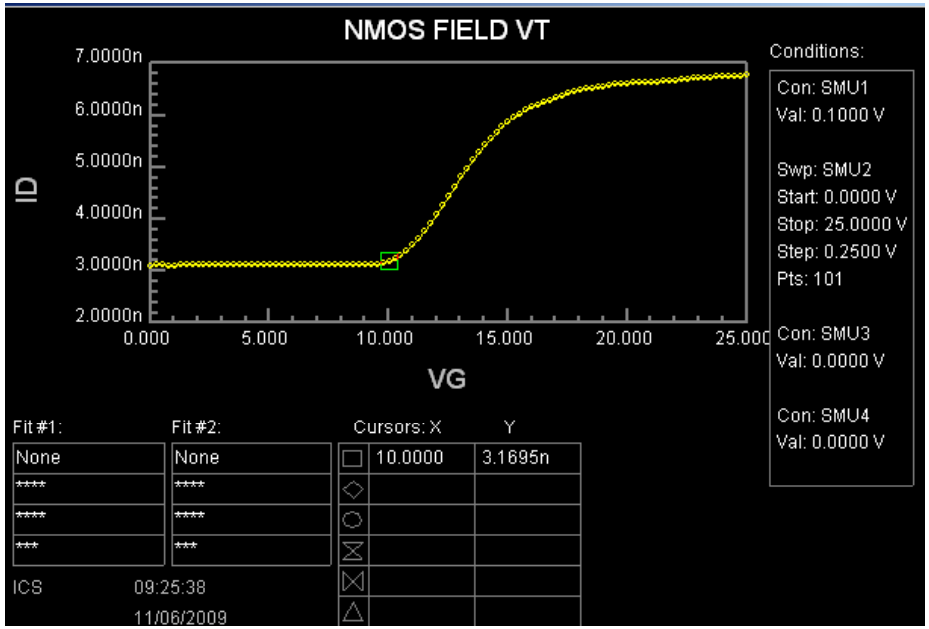
FIELD OXIDE NMOS AND PMOS FET'S

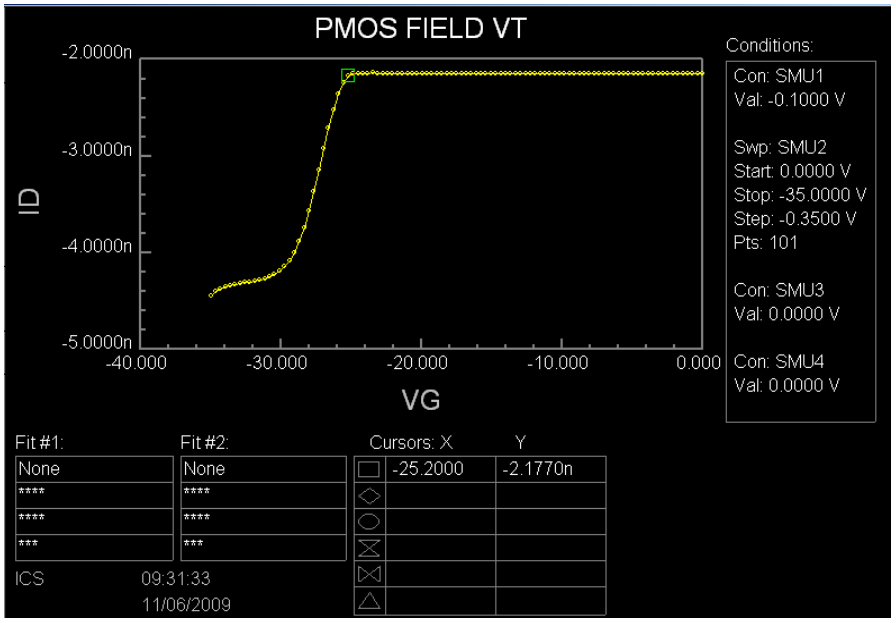






FIELD OXIDE ID-VGS, EXTRACT VT(FIELD)

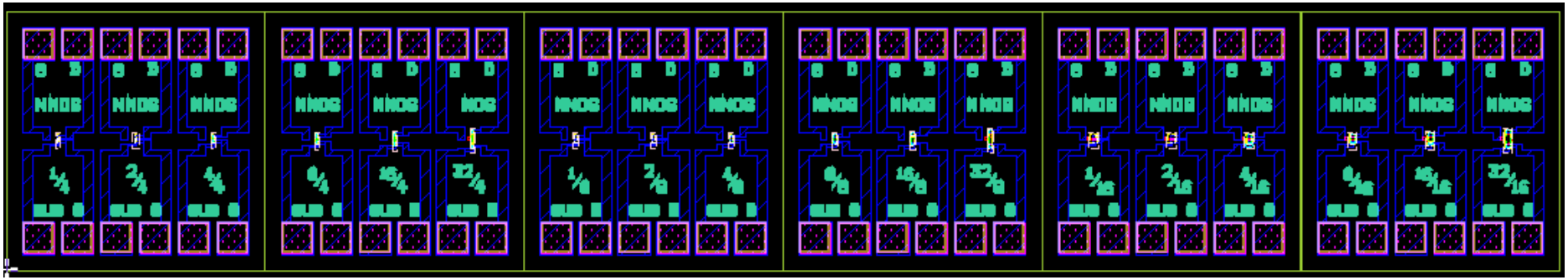




NMOS Field Vt > 10 volts

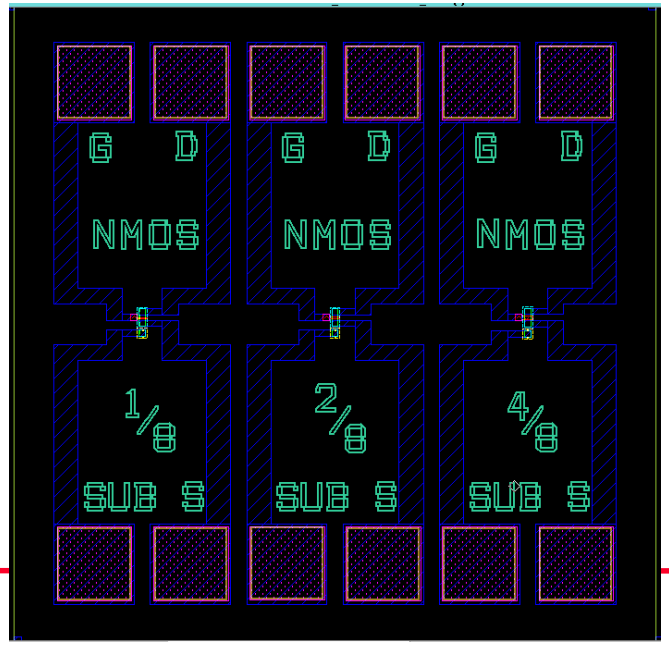
Pmos Field Vt < -25 volts

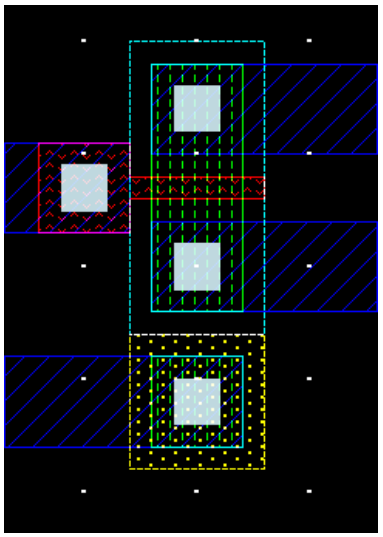
NMOS AND PMOS TRANSISTORS



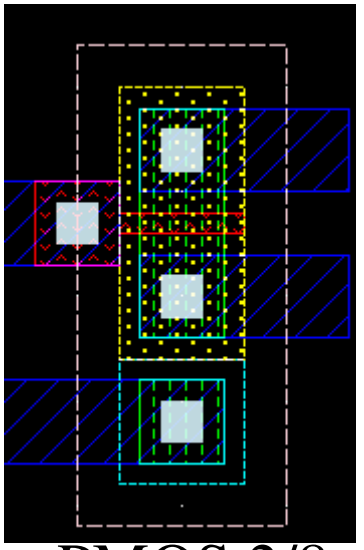
1/4 2/4 4/4 8/4 16/4 32/4 1/8 2/8 4/8 8/8 16/8 32/8 1/32 2/32 4/32 8/32 16/32 32/32

Various L/W Ratios



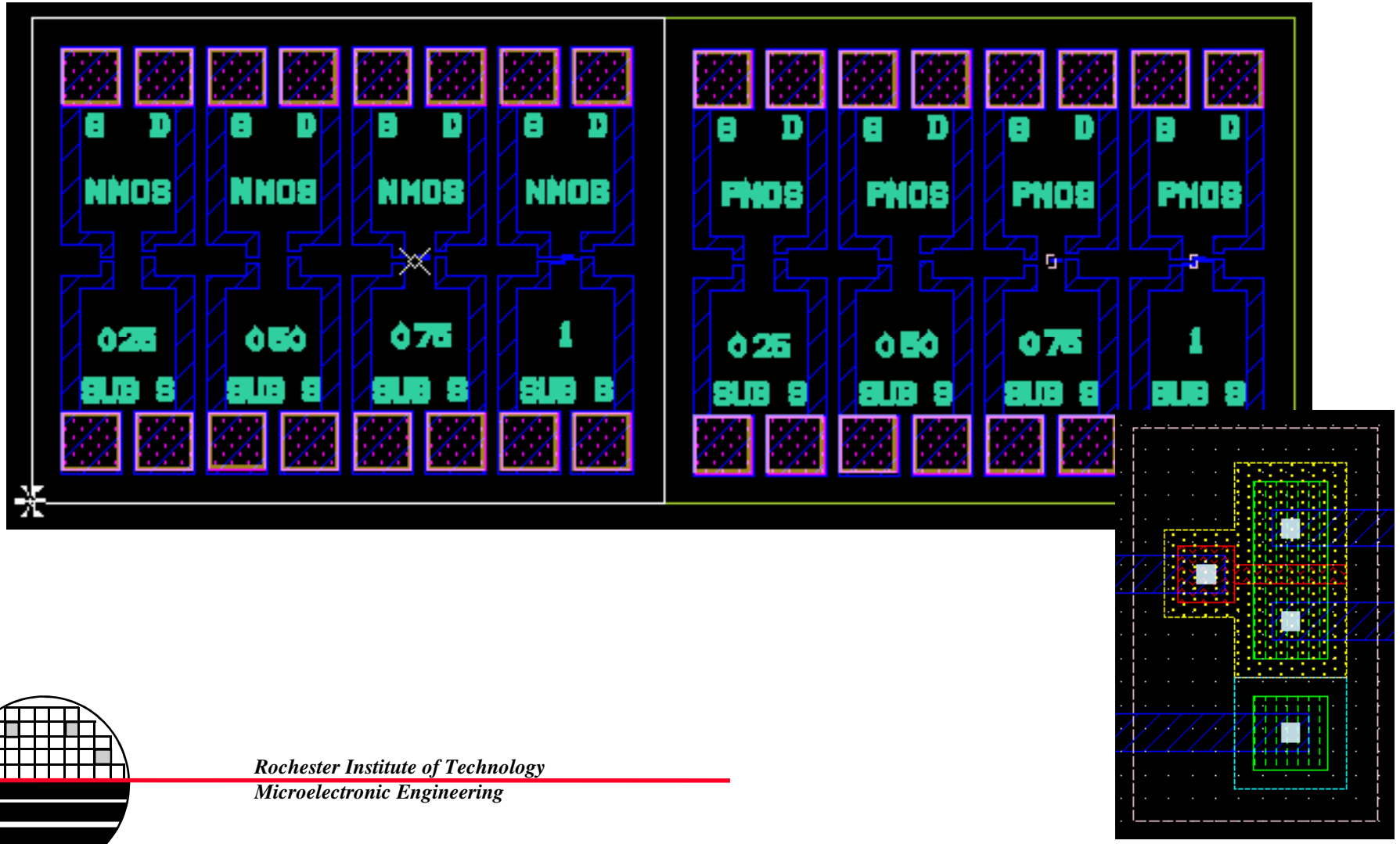


NMOS 2/8

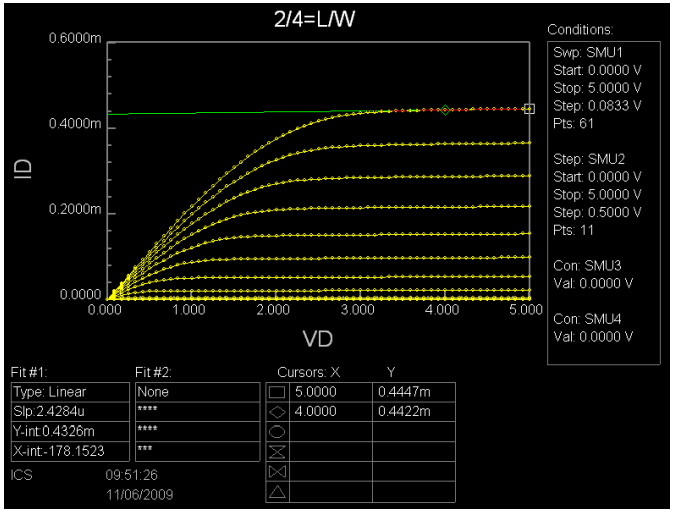


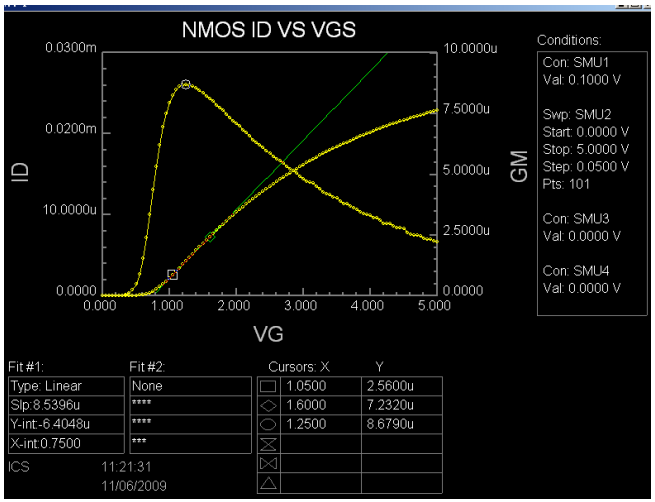
PMOS 2/8

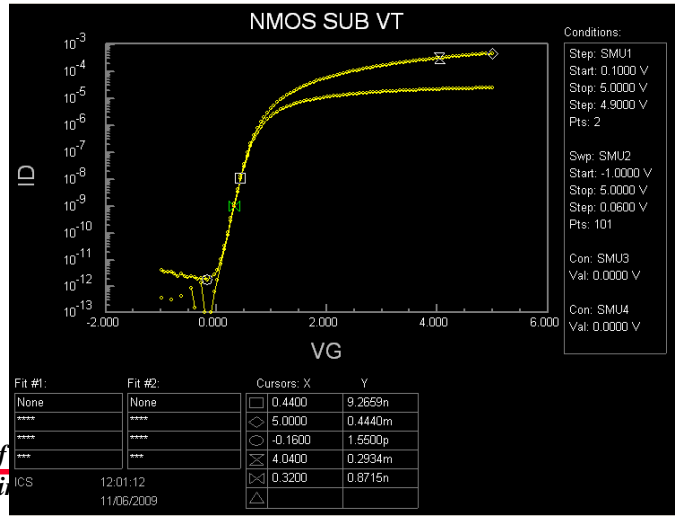
FULLY SCALED SUB MICRON TRANSISTORS

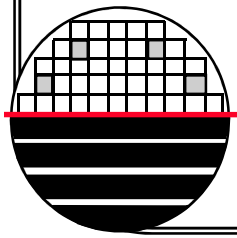


NMOS TEST RESULTS



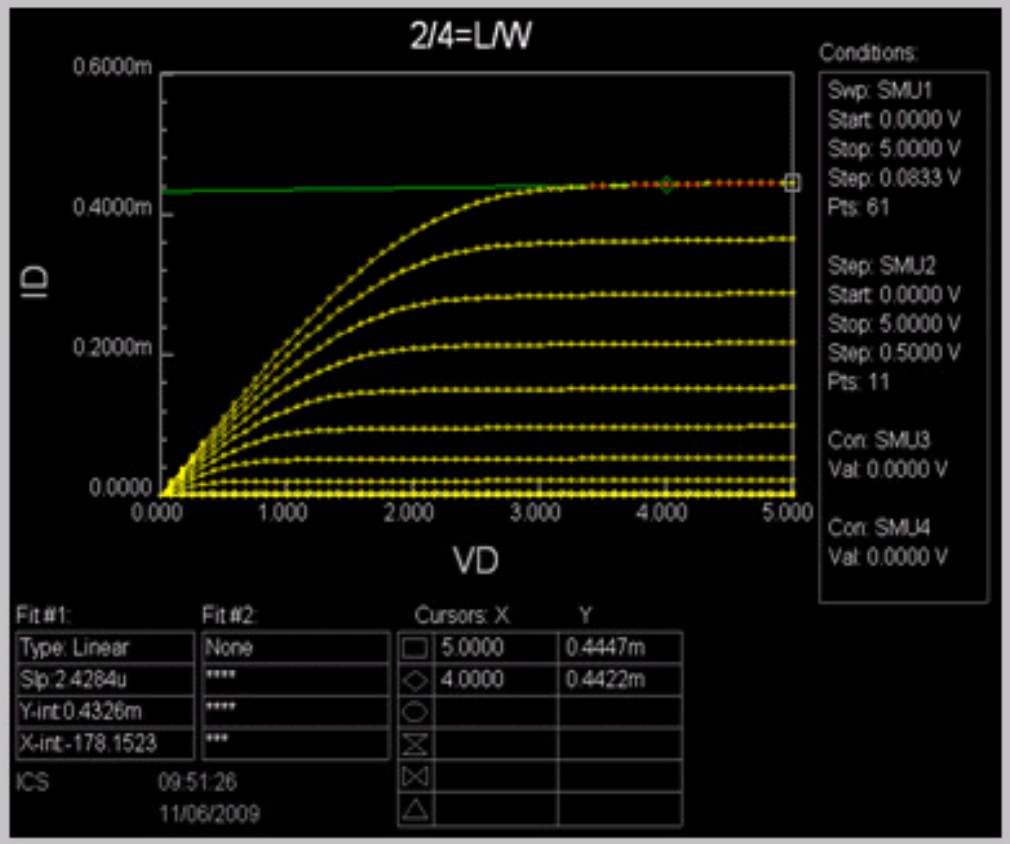






TRANSISTOR PARAMETER EXTRACTION

NMOS Transistor Family of Curves

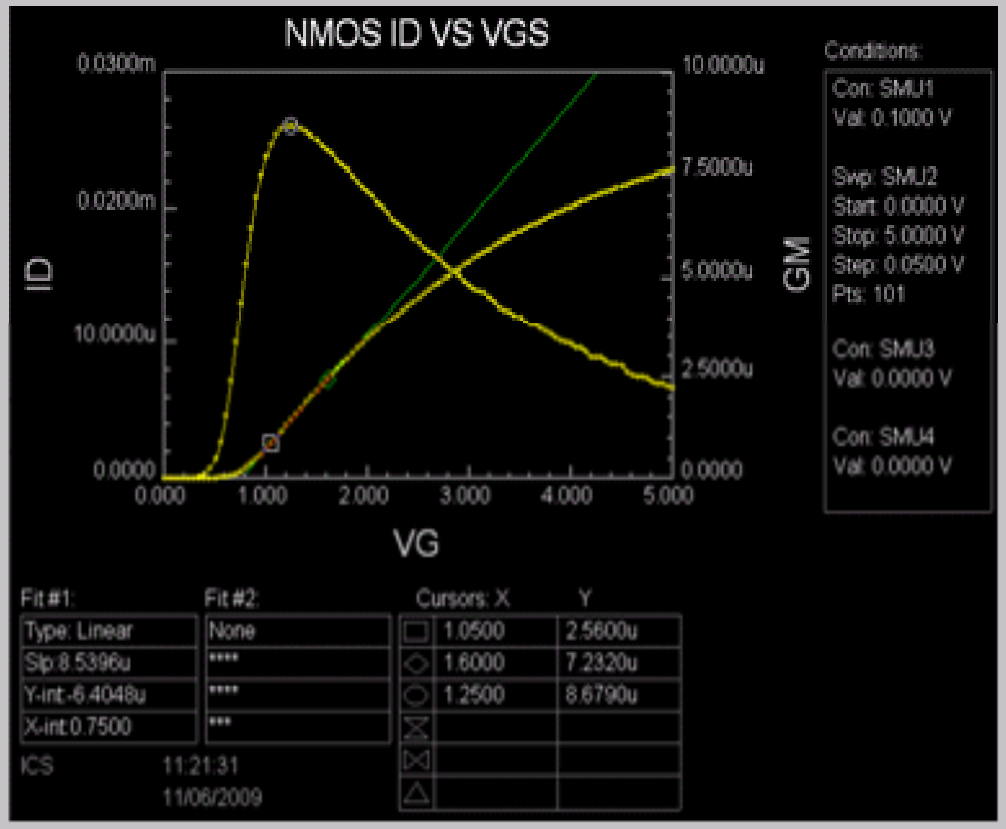


Idmax at Vgs = 5 and Vds = 5
Idsat at Vgs = 5 and Vds = 4

Length L=	2	um
Width W =	4	um
Idmax =	0.4447	mA
Idsat =	0.4422	mA
Lambda = slope/Idsat	0.006	1/V
I drive =	111	uA/um

TRANSISTOR PARAMETER EXTRACTION

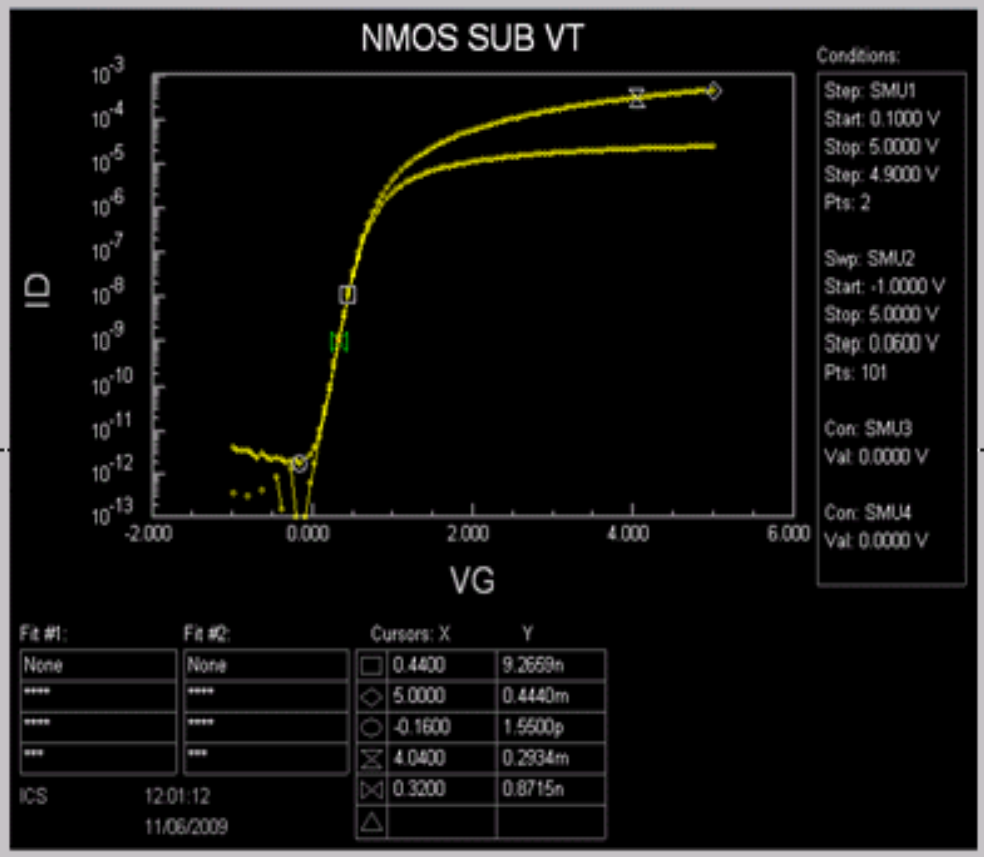
NMOS Transistor Ids vs Vgs with Vds = 0.1 volts



gm max =	0.008679	mS
X intercept = VT	0.75	V
gm =	2.17	mS/mm
VT =	0.75	V

TRANSISTOR PARAMETER EXTRACTION

NMOS Transistor Subthrehold Plot at Vd = 0.1 and Vd = 5

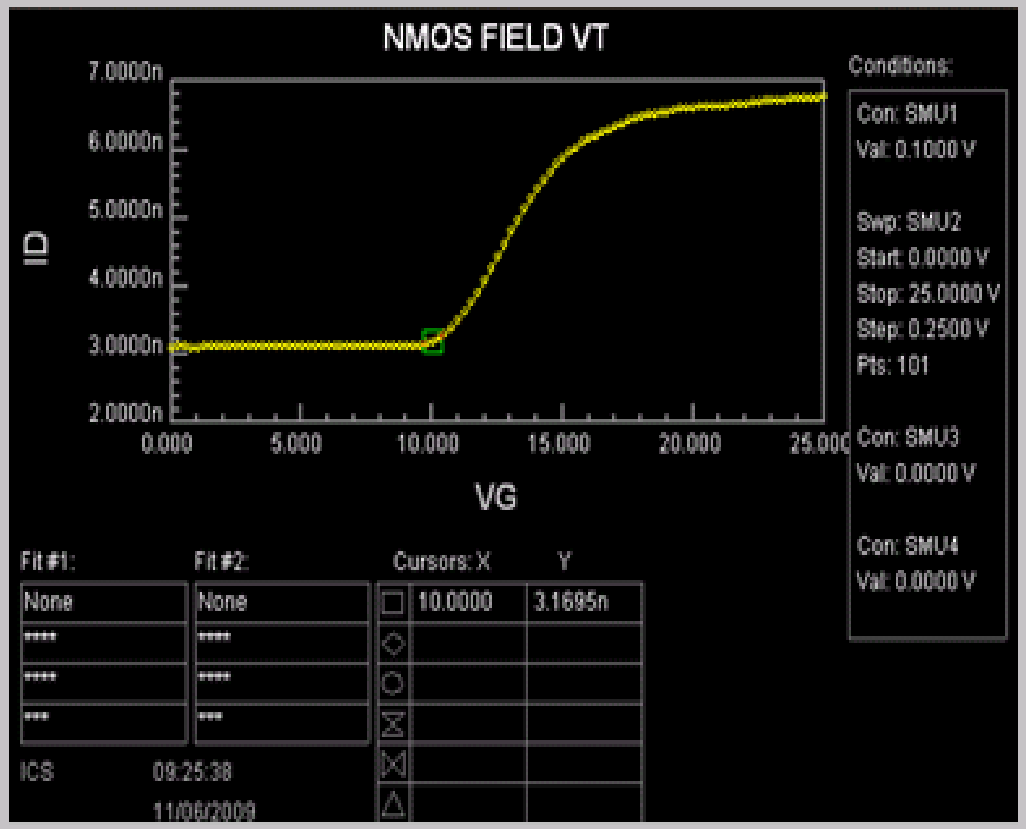


Measure in the Dark

Imax @ Vds=0.1	2.50E-05	A
Imax @ Vds=5	4.44E-04	A
Imin @ Vds=0.1	1.55E-12	A
Imin @ Vds=5	1.55E-12	A
Vgs at Id=10nA, Vd=0.1	0.440	V
Vgs at Id=1nA, Vd=0.1	0.320	V
Vgs at Id=1nA, Vd=5	0.320	V
Ion/Ioff @ Vds=0.1	7.21	DEC
Ion/Ioff @ Vds=5	8.46	DEC
sub-threshold swing =	120	mV/DEC
DIBL =	0.0	mV/V

TRANSISTOR PARAMETER EXTRACTION

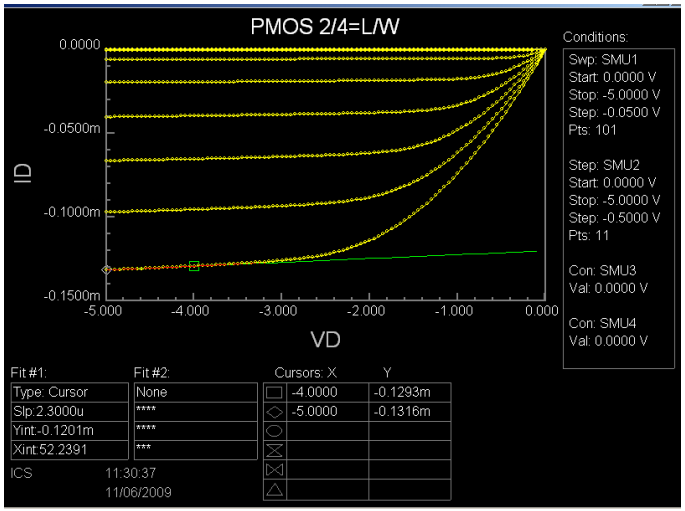
NMOS Field Oxide FET, Id versus Vgs

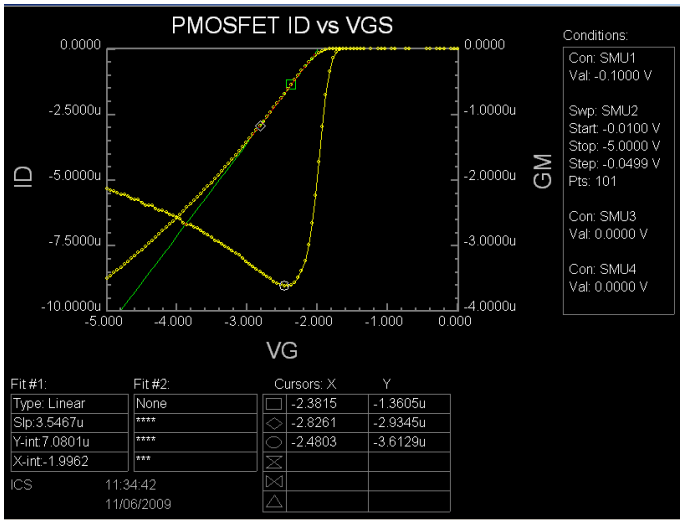


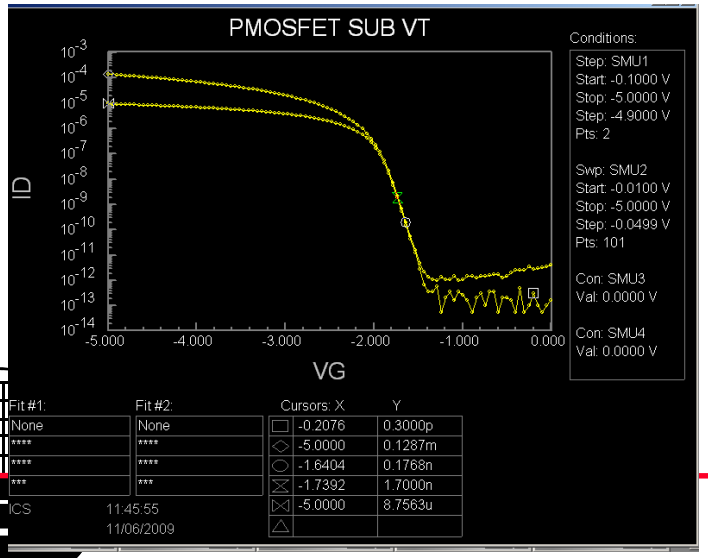
X intercept = 10.0 V

Field VT = 10.0 V

PMOS TEST RESULTS







Note: Vt adjust mask made incorrectly
Vt = ~ -2.0

MOSFET EXTRACTED PARAMETERS

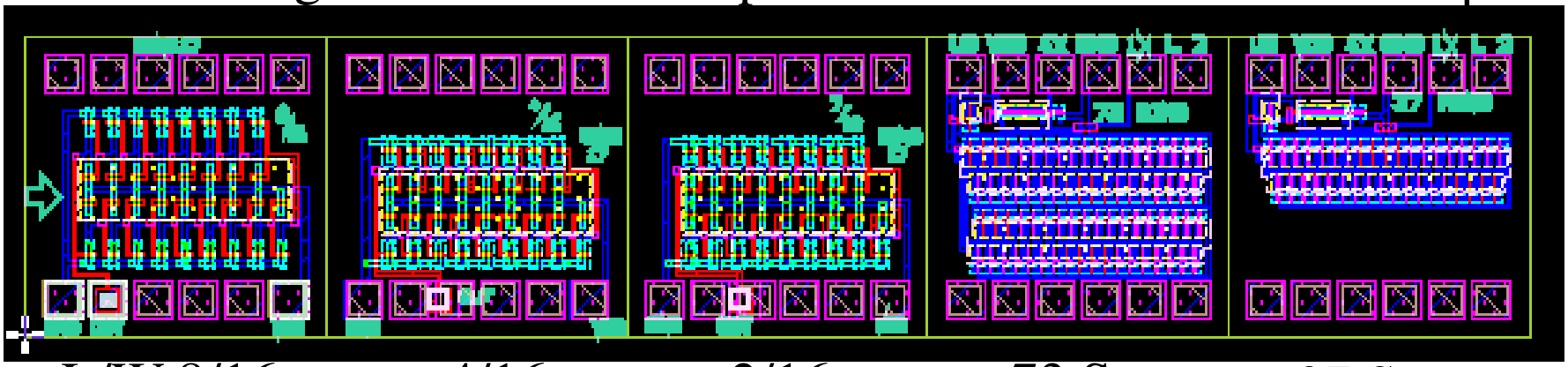
Lot Number = F080729 – Wafer Number = D2, Die Location R= , C=

	PMOS	NMOS	Units
Mask Length / Width	**2/4**	**2/4**	**µm**
VT	**-2.0**	**0.75**	**V**
Lambda (for Vgs = Vdd)	**0.018**	**0.006**	**V^{-1}**
Max gm / mm of channel width	**0.90**	**2.17**	**mS/mm**
Idrive	**33**	**111**	**µA/µm**
Ion/Ioff @ Vd = 0.1V	**7.47**	**7.21**	**Decades**
Ion/Ioff @ Vd = 5V	**8.52**	**8.46**	**Decades**
Ioff @ Vd = 0.1V	**3E-13**	**1.55E-12**	**A/µm**
Ioff @ Vd = 5V	**3E-13**	**1.55E-12**	**A/µm**
Sub-Vt Slope @ Vd = 0.1V	**99**	**120**	**mV/Dec**
Sub-Vt Slope @ Vd = 5 V	**99**	**120**	**mV/Dec**
DIBL@1nA/µm =$\Delta V_g/\Delta V_d$	**0**	**0**	**mV/V**
Field VT	**-25.2**	**10**	**V**

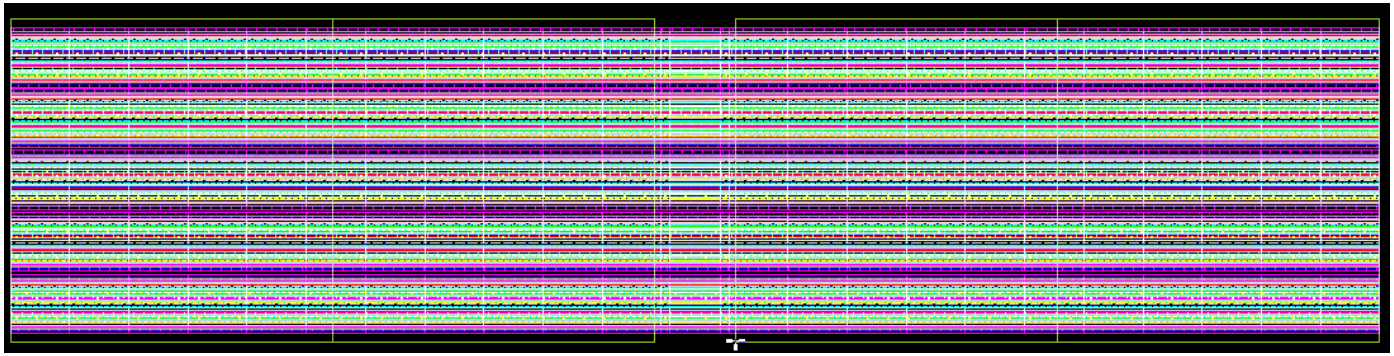
RING OSCILLATORS AND SEM STRUCTURES

17 Stage Un-buffered Output

L/W=2/30 Buffered Output



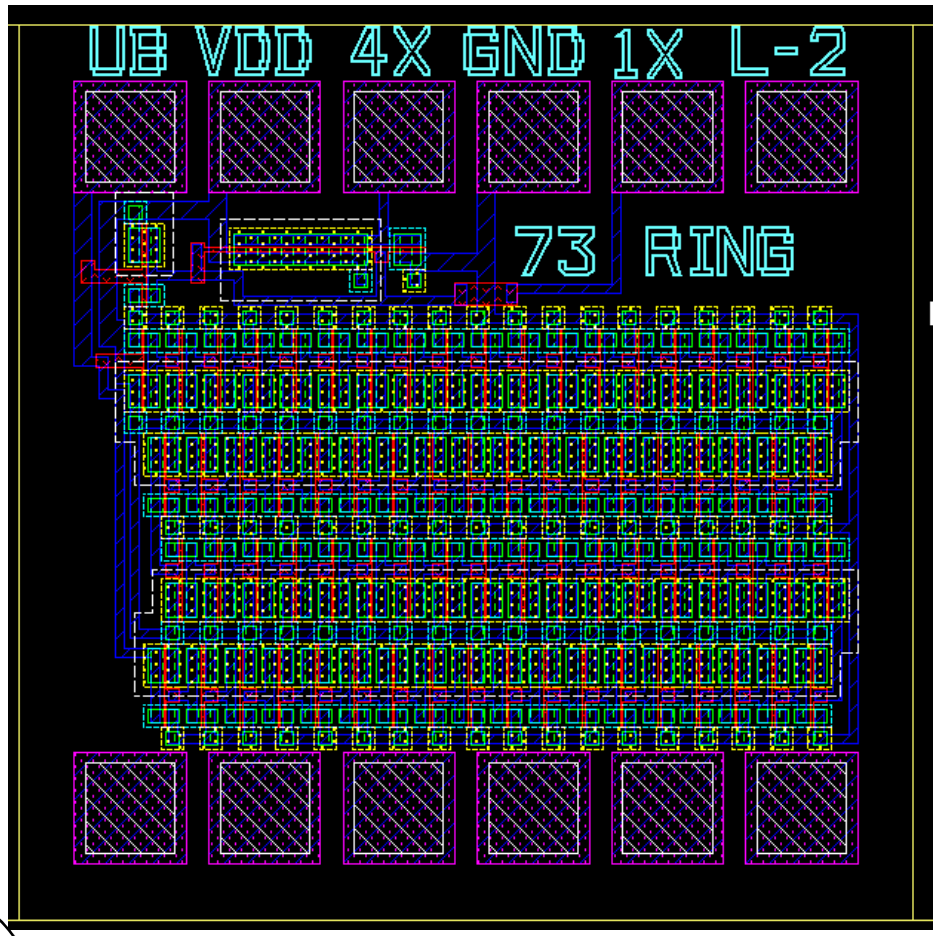
L/W 8/16 4/16 2/16 73 Stage 37 Stage



SEM Structures

CMOS Inverter Crossection

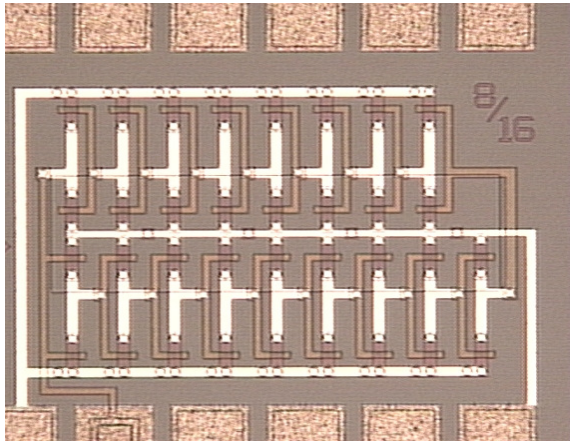
RING OSCILLATOR DESIGN

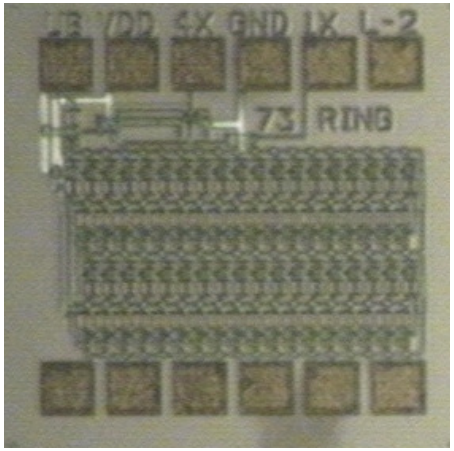


2µm gate length
5 Volt
73 stage
4x Buffer Output
1x Buffer Output
Unbuffered Output

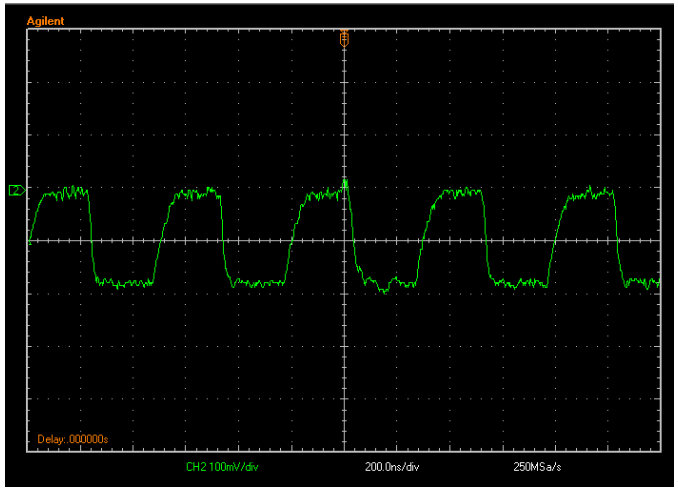
RING OSCILLATOR RESULTS

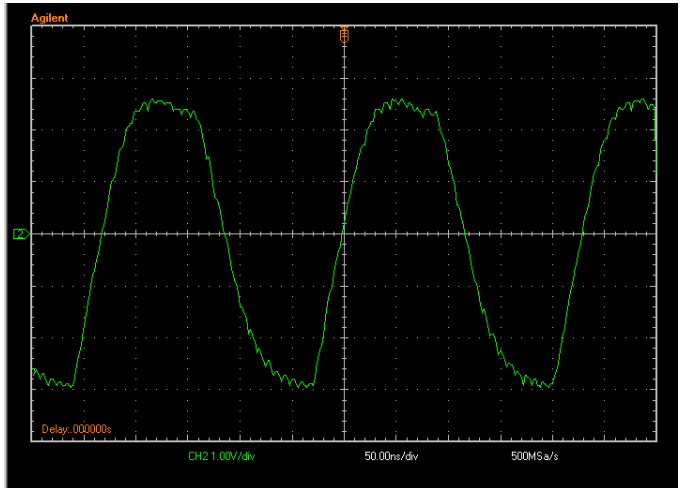
17 Stage
unBuffered
L=8µm
Frequency = 2MHz
Period = 500ns
td = 14ns





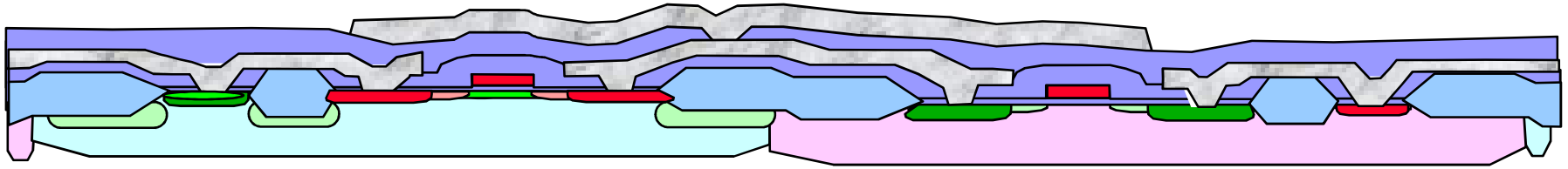
73 Stage
4X Buffer
L=2µm
Frequency = 4.37MHz
Period = 230ns
td = 1.58ns



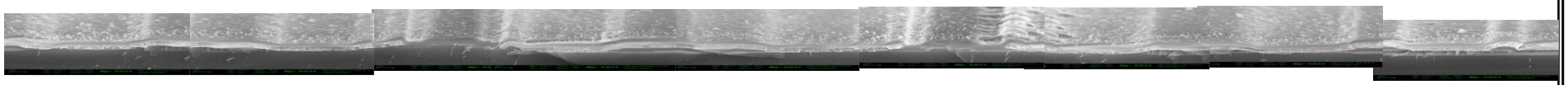


These worked the others did not.
Design errors in 2nd & 3rd wrong layer for CC, missing CC in 5th

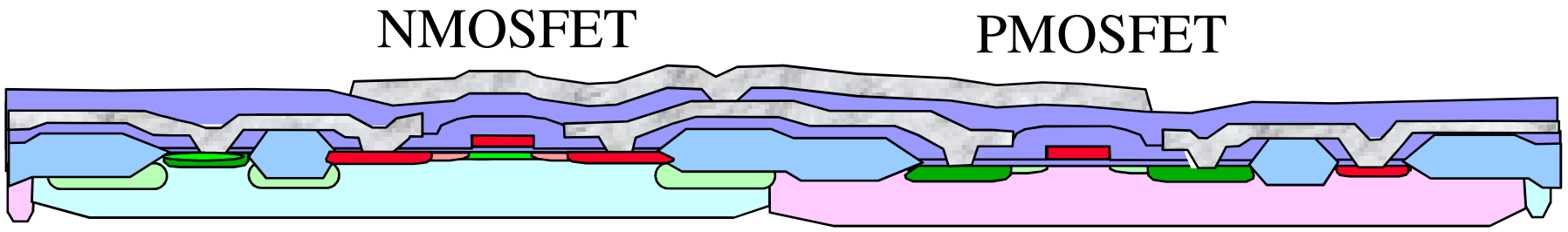
SEM PICTURE OF INVERTER CROSSECTION

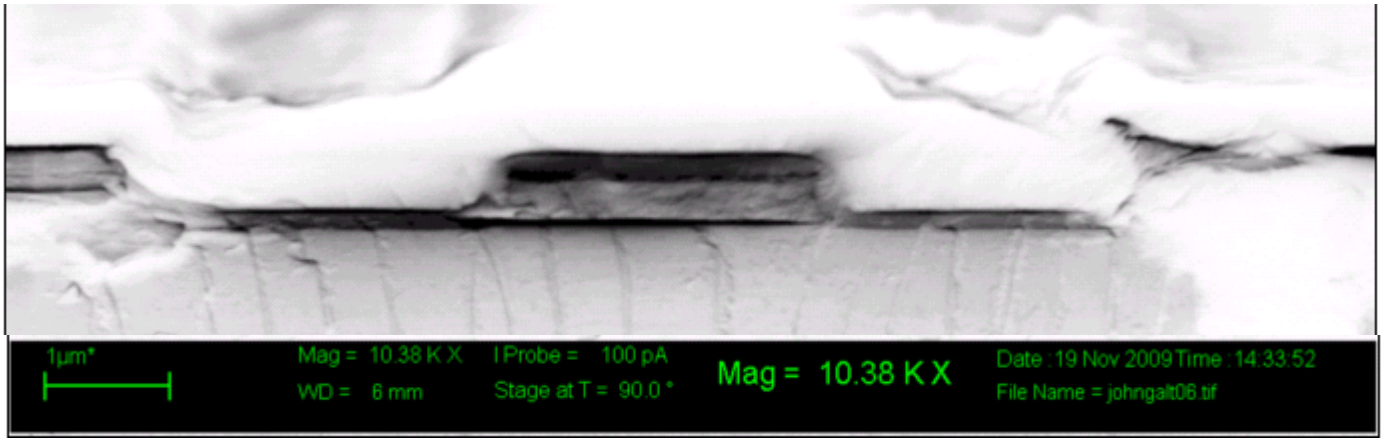


P-well N-well

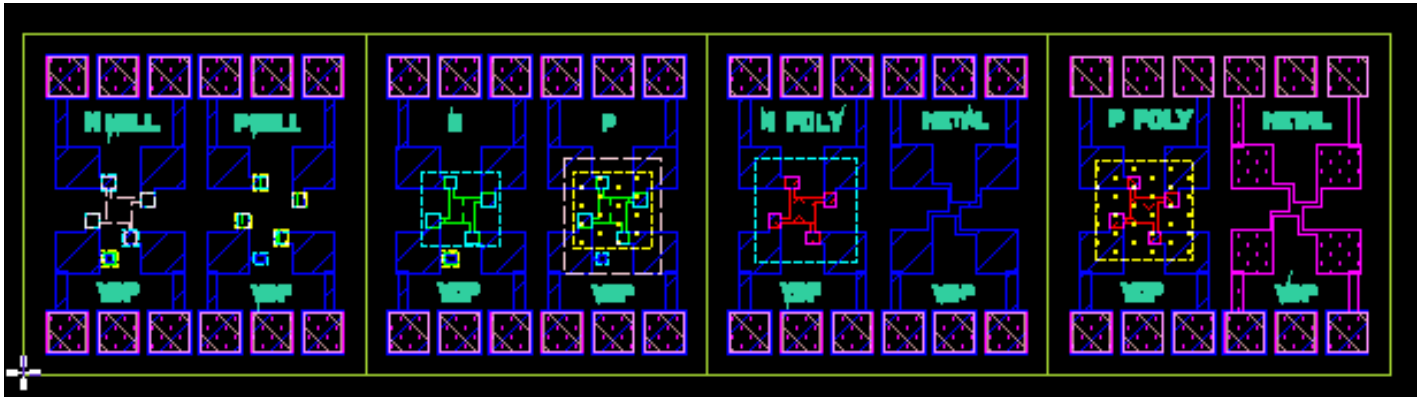


SEM CROSSECTION OF MOSFET

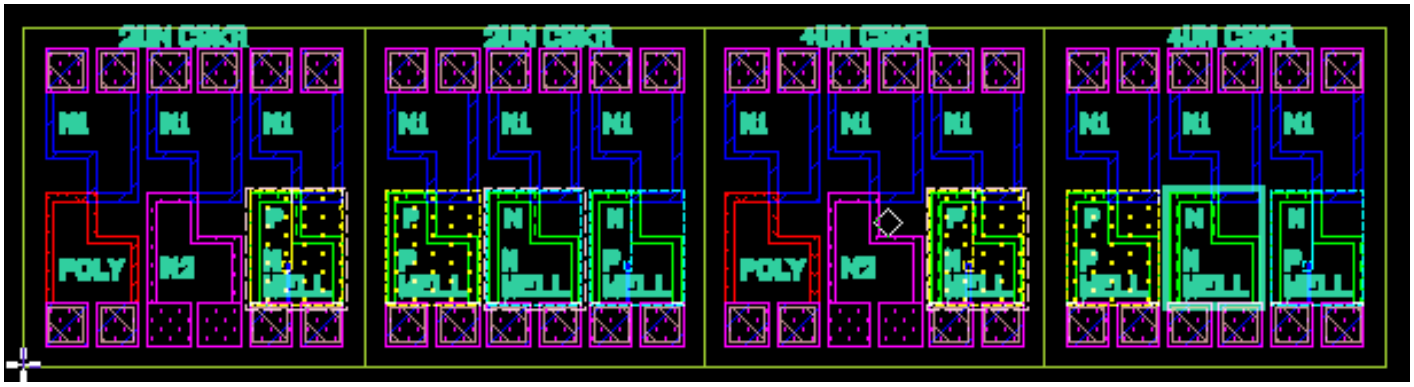




VAN DER PAUWS AND CBKR's

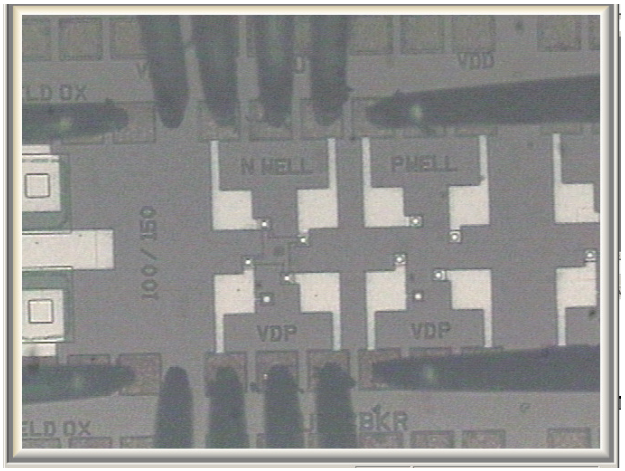


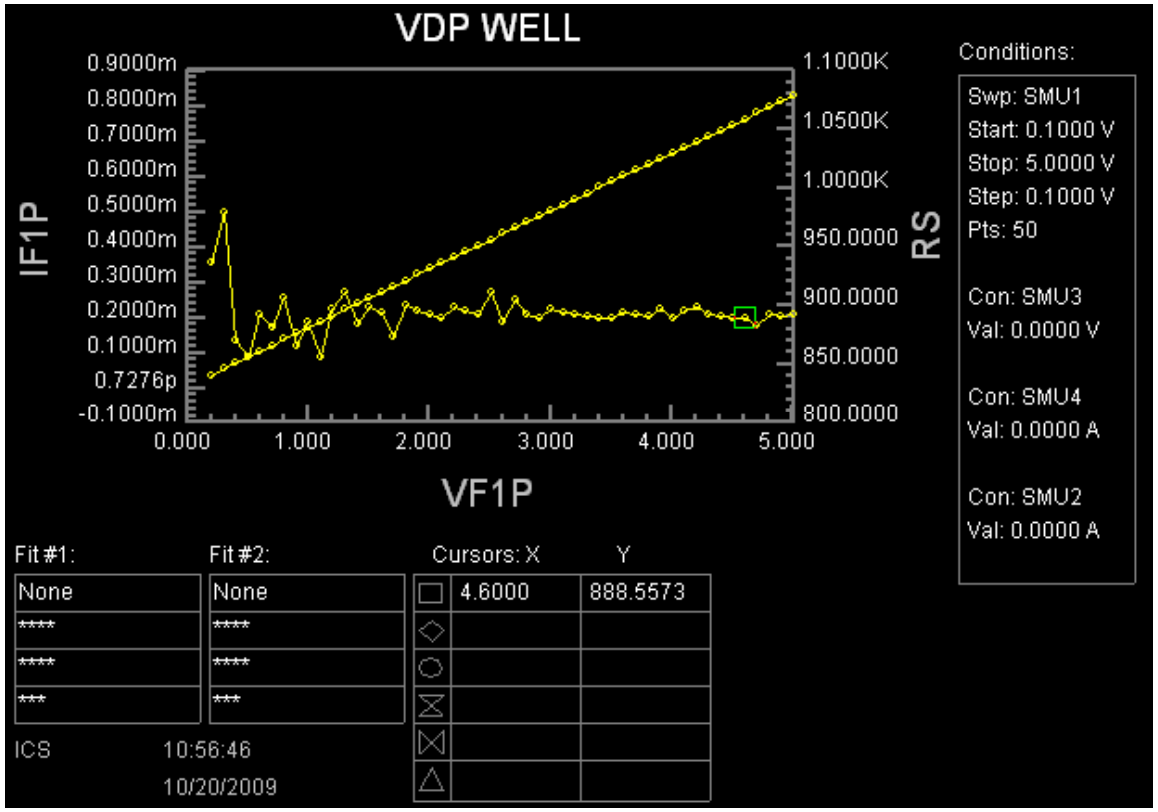
NWELL PWELL N+ P+ N-POLY M1 P-POLY M2



2µm M1toPoly	2µm M1toP+	4µm M1toPoly	4µm M1toP+
2µm M1toM2	2µm M1toN+	4µm M1toM2	4µm M1toN+
2µm M1toP+	2µm M1toN+	4µm M1toP+	4µm M1toN+

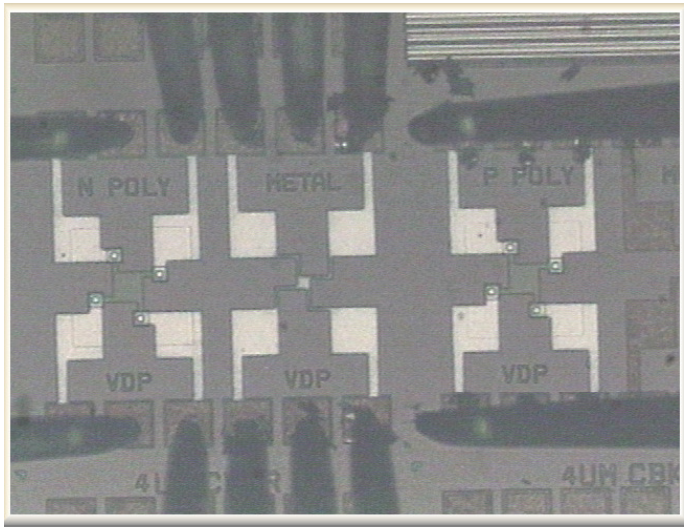
VAN DER PAUW TEST RESULTS

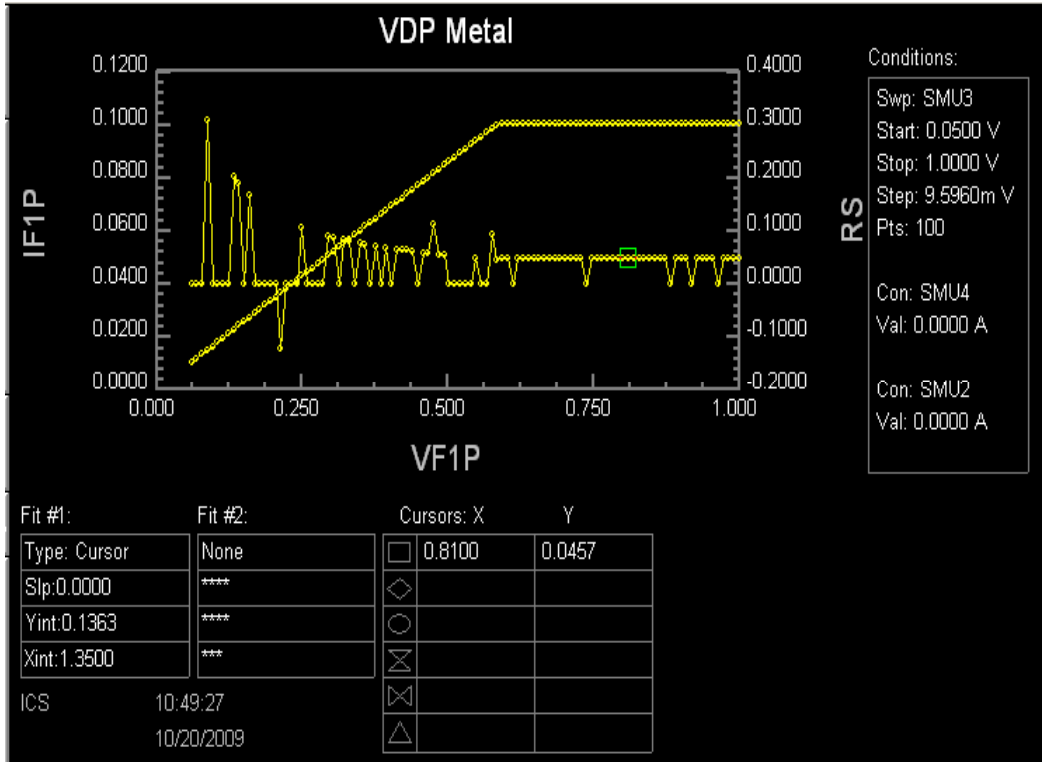




N-Well
Rhos=888 ohm/sq

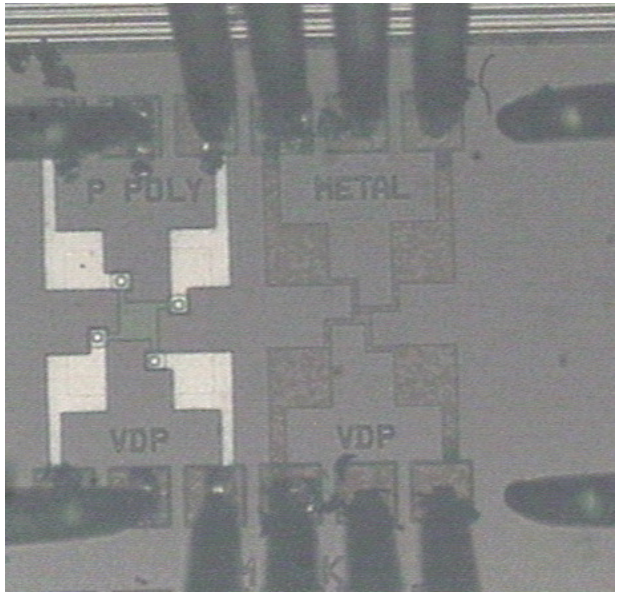
VAN DER PAUW TEST RESULTS



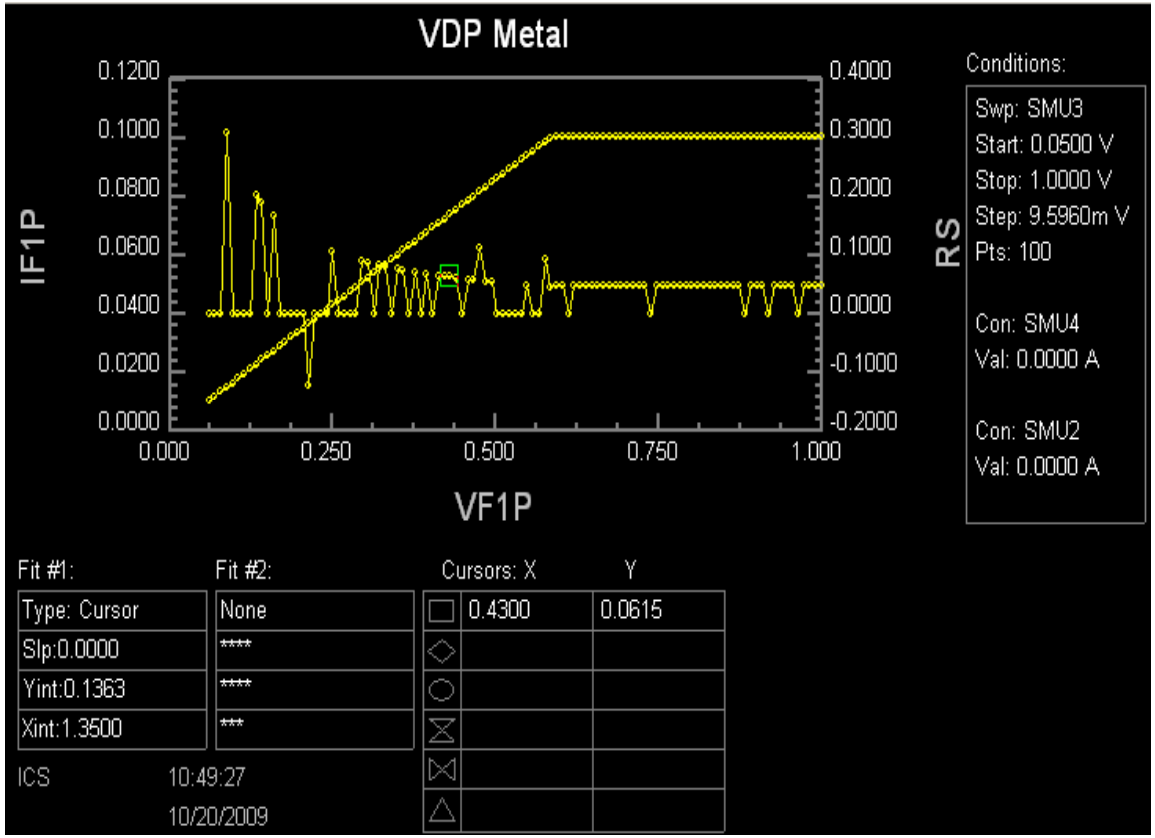


Metal 1
Rhos=0.0457 ohm/sq

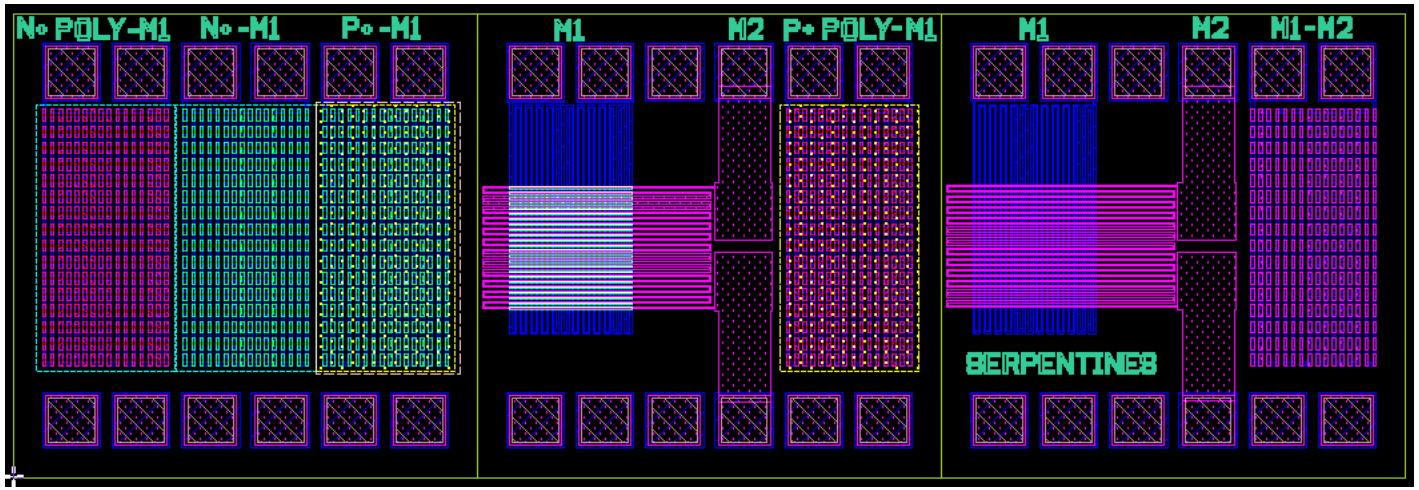
VAN DER PAUW TEST RESULTS



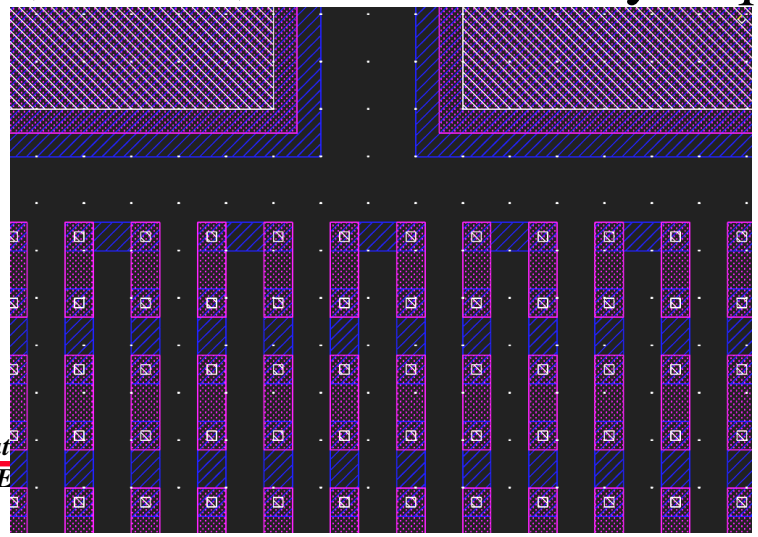
Metal 2
Rhos=0.0615 ohm/sq



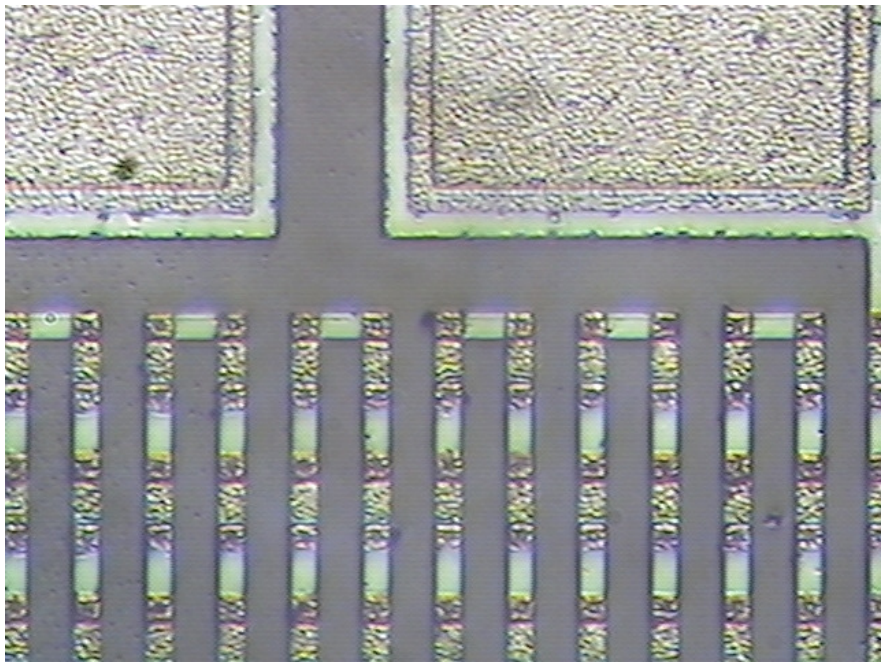
SERPENTINES, COMBS, AND VIA CHAINS

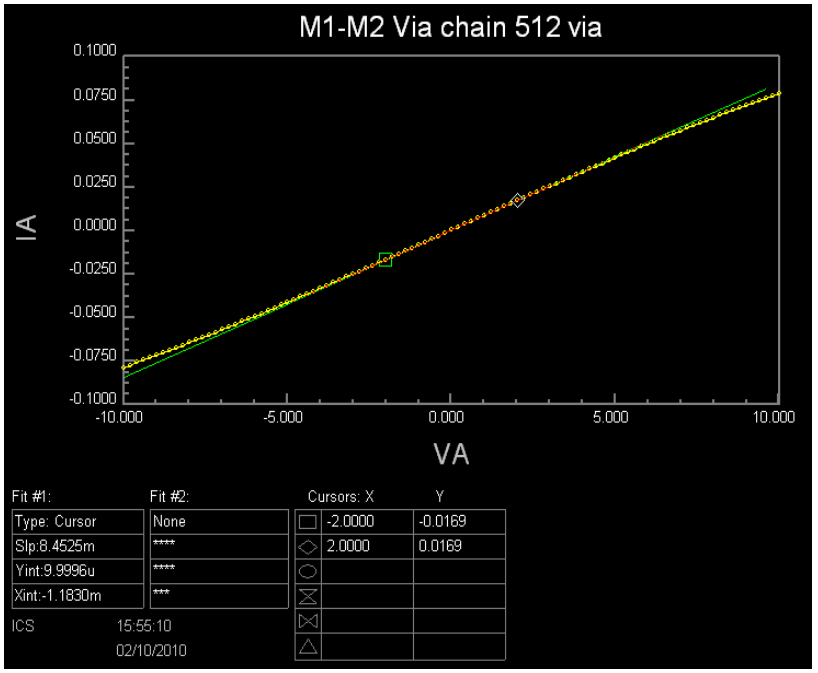


To evaluate metal1, metal2, CC and Via layer quality.



M1-M2 VIA CHAIN



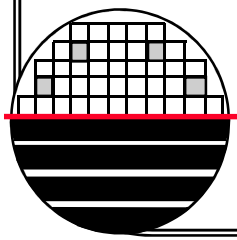


F081201

M1-M2 Via chain with 512 Vias and total resistance of 118 ohms or 0.231 ohms per contact

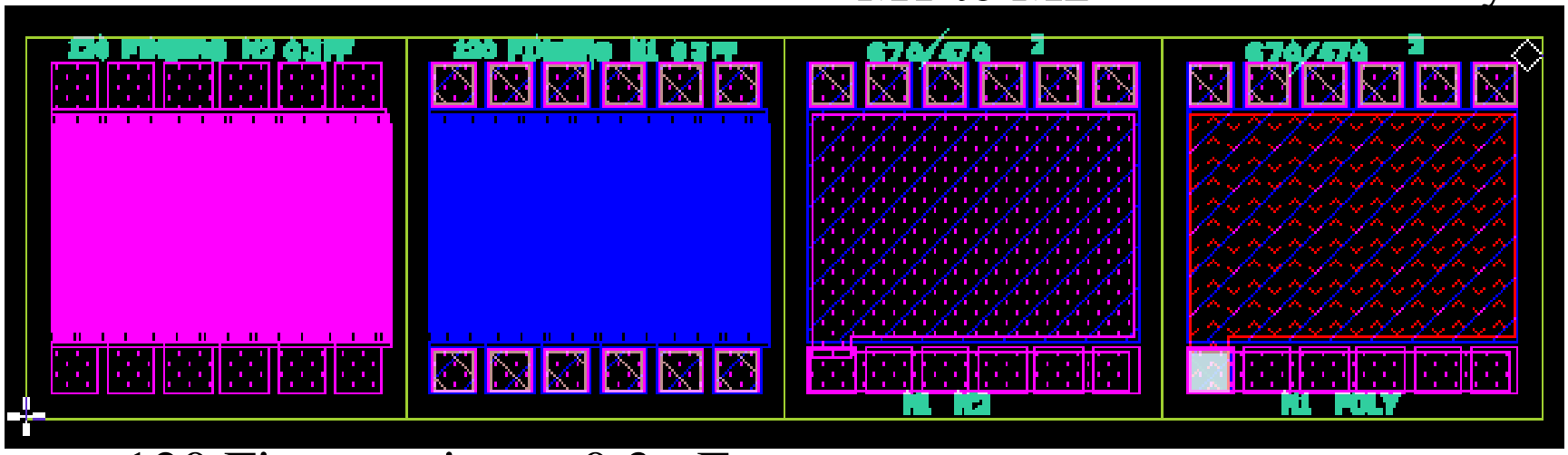
SENSORS

Interdigitated and Plate Capacitors
Diodes and Heaters
Resistors
Photovoltaic Cells, 1x, 2x, 4x
Two side by side pn diode sensors for differential readout



CAPACITORS

M2 M1 M1 to M2 M1 to Poly

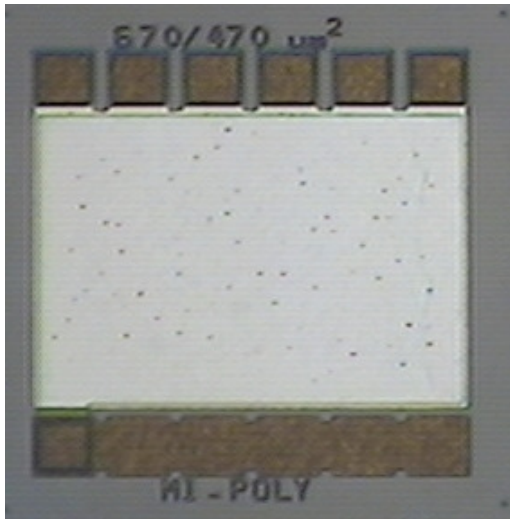


120 Fingers gives ~0.3 pF

670µm/470µm Plate
~3 pF

PARALLEL PLATE CAPACITORS

TEOS=4000Å



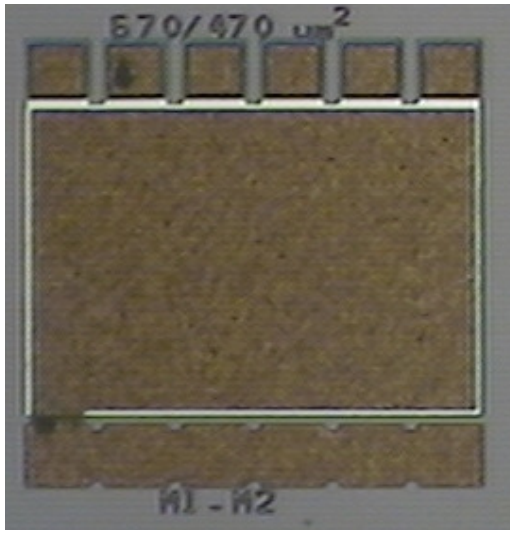
Measured = 22.5pF

Calculated= εo εr Area/d

=(8.85e-14)(3.9)(670x470)(1E-4)/(0.4)

=27.2 pF

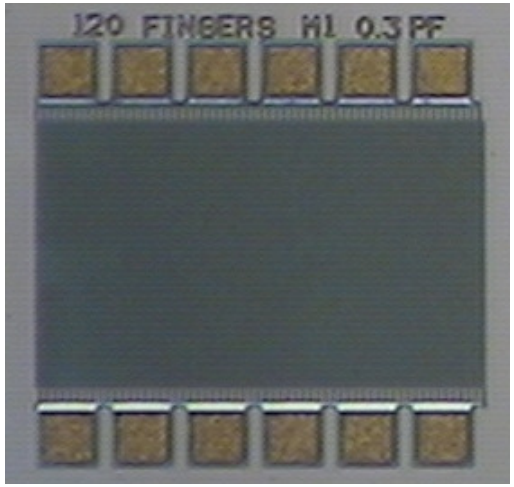
TEOS=5000Å



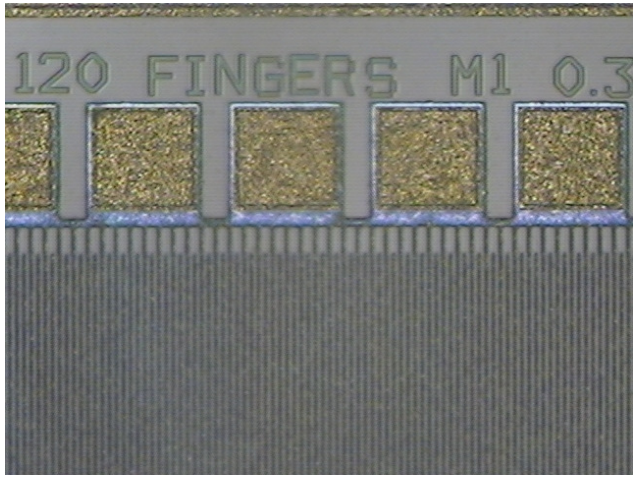
Measured = 29.4pF

Calculated = 22pF

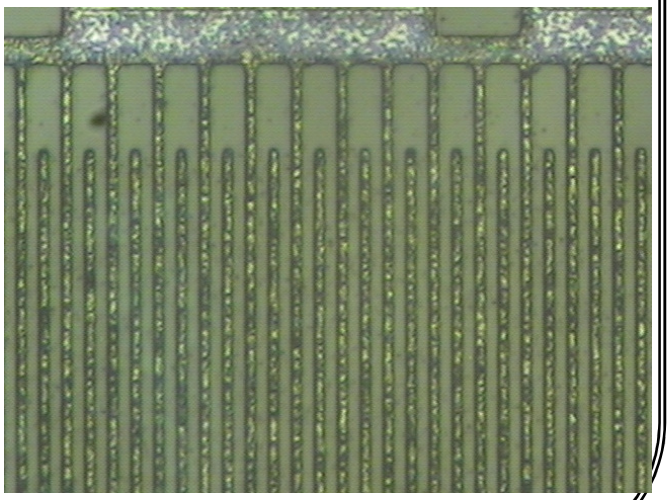
METAL ONE INTERDIGITATED FINGER CAPACITORS



Measured: 1.1pF
Calculated: 2.3pF



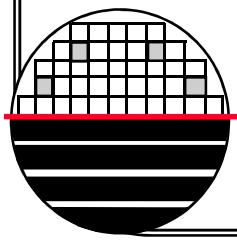
120 fingers
3um line
3um space
Er = 4.9
Overlap = 440um



$$C = LN\left(4\frac{\varepsilon_0\varepsilon_r}{\pi}\right)\sum_{n=1}^{\infty}\frac{1}{2n-1}\,Jo^2\left[\frac{(2n-1)\pi s}{2(s+w)}\right]$$

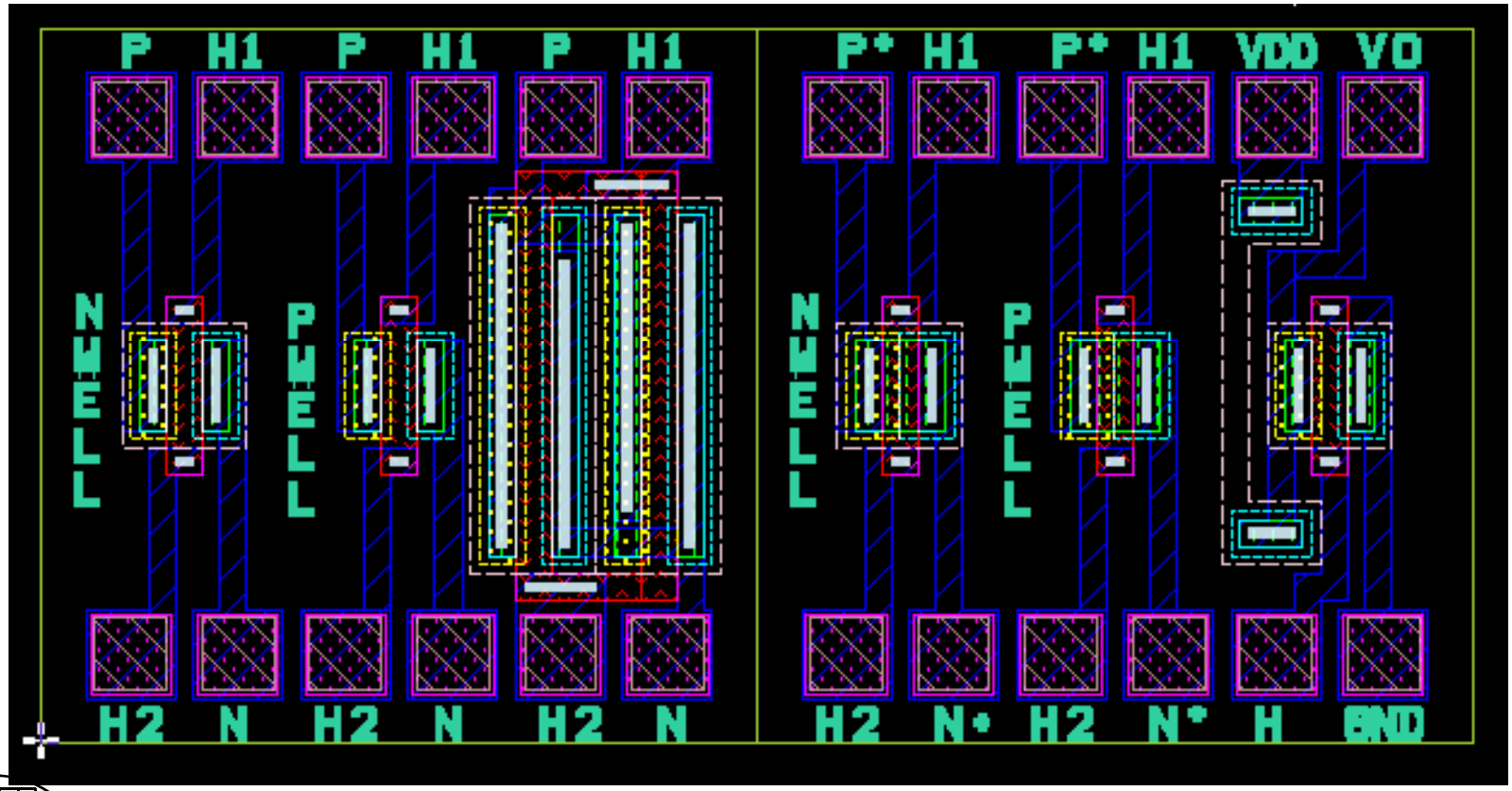
INTERDIGITATED FINGER CAPACITOR CALCULATIONS

28	**Capacitance for very Thin Interdigitated Fingers**				CMOS_TESTC
29	$C = LN\left(4\frac{\varepsilon_o\varepsilon_r}{\pi}\right)\sum_{n=1}^{00}\frac{1}{2n-1}Jo^2\left[\frac{(2n-1)\pi s}{2(s+w)}\right]$		Capacitance, C =	2.26E-12	F
30			Number of Fingers, N =	120	
31			relative dielectric constant, er =	4.9	
32			Length of finger overlap, L =	440	µm
33			width of fingers, w =	3	µm
34			space between fingers, s =	3	µm



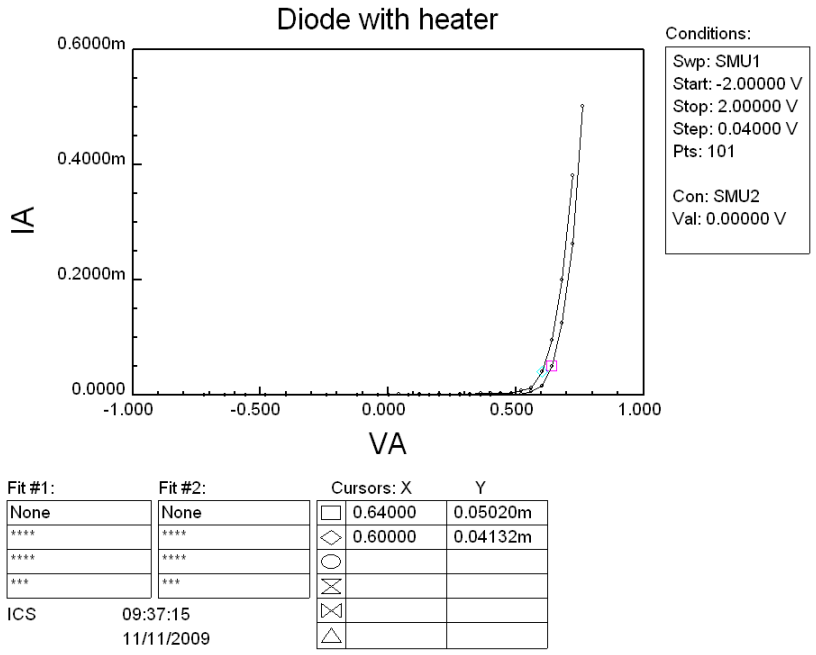
DIODES AND HEATERS

Poly Heater on top of Diodes



Integrated series well resistor.

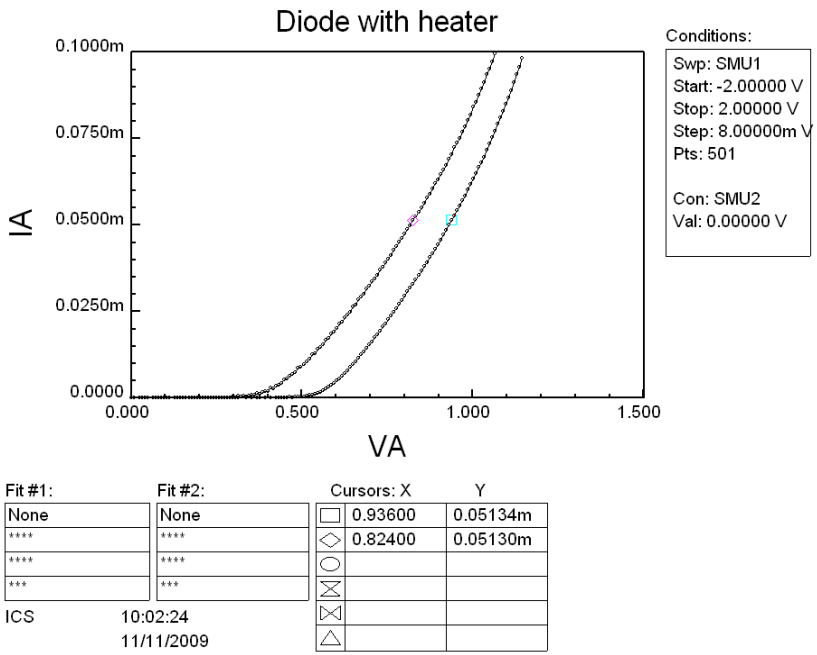
DIODES AND HEATER TEST RESULTS



Heater at 10 volts

$T = 25 + 0.04V/(2.2mV/°C)$

$= 43.2\ °C$

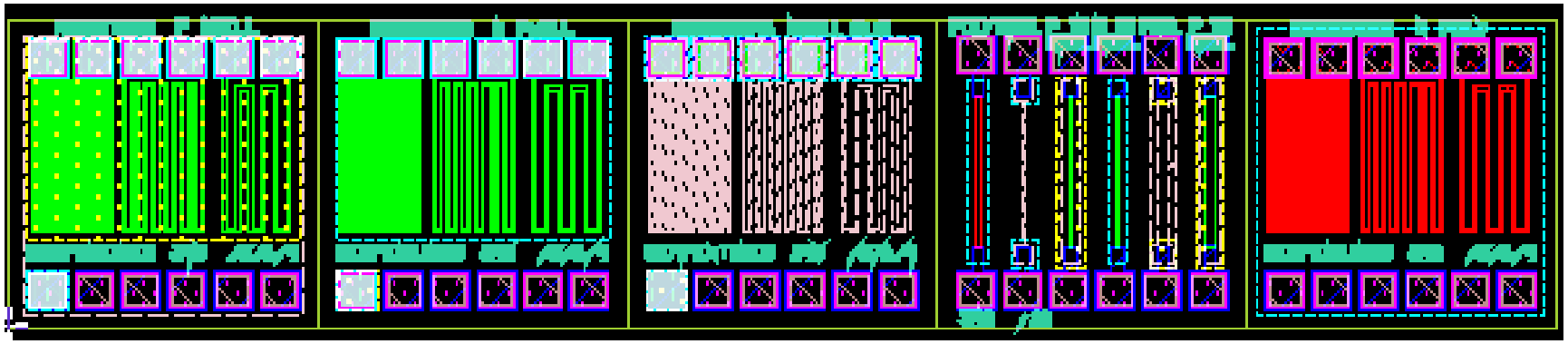


Heater at 20 volts

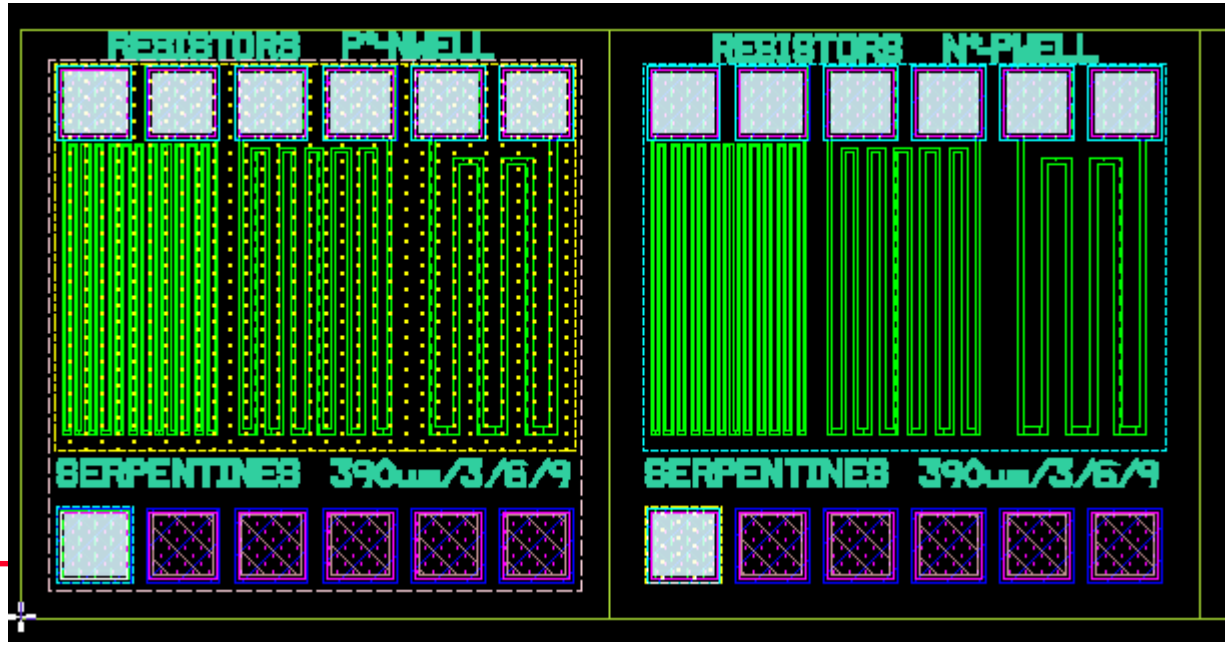
$T = 25 + 0.11V/(2.2mV/°C)$

$= 75\ °C$

RESISTORS

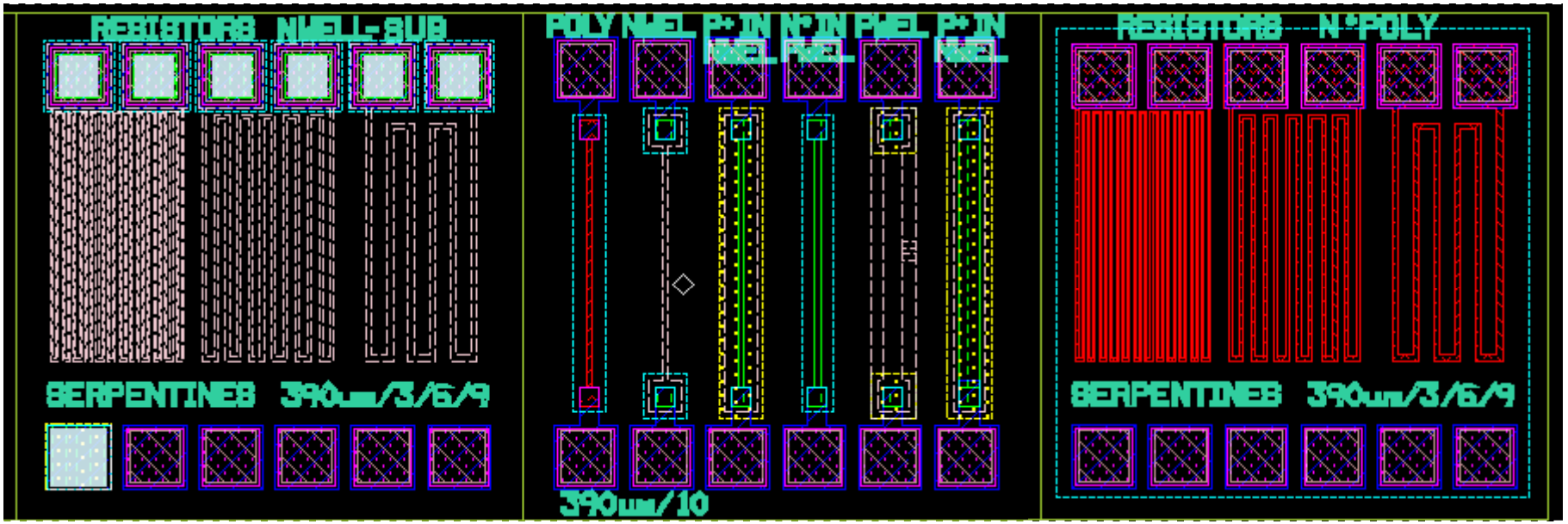


P+ in Nwell



N+ in Pwell

RESISTORS



Nwell in P substrate

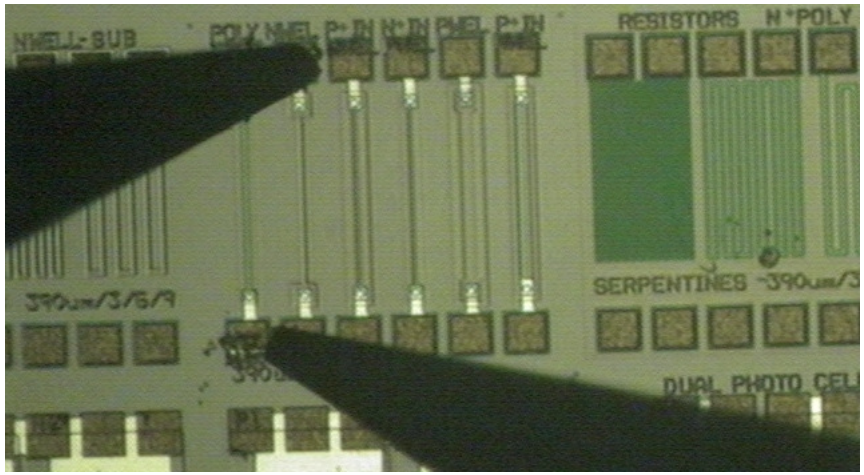
6 different Resistor Designs

N+ Poly

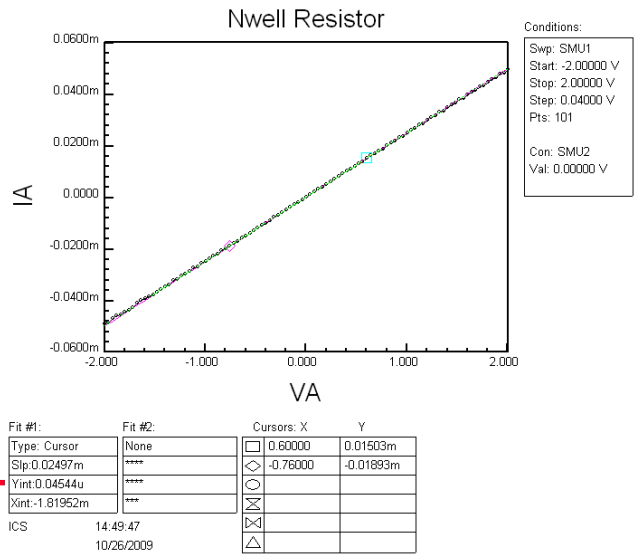
(missing contact cuts)

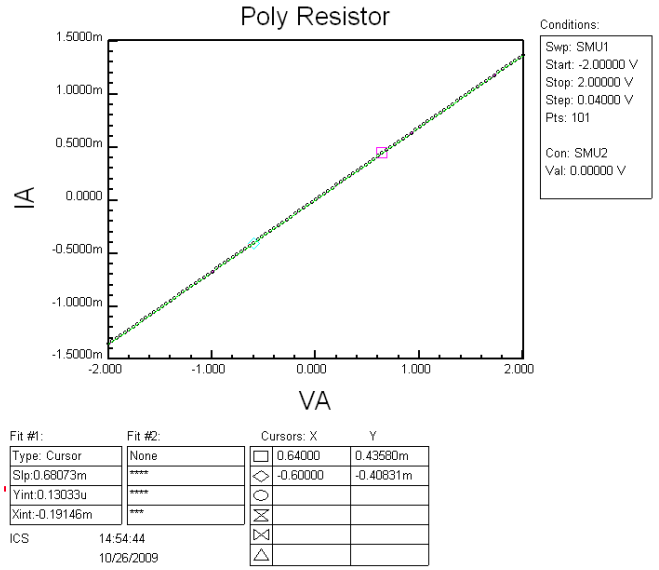
RESISTORS

NWell
R = 1/SLOPE
= 1/0.025m
= 40,000 ohm
Rhos = 40K/39
=1026 ohm/sq

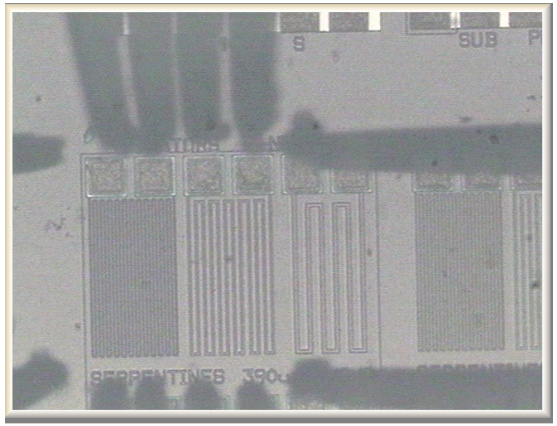


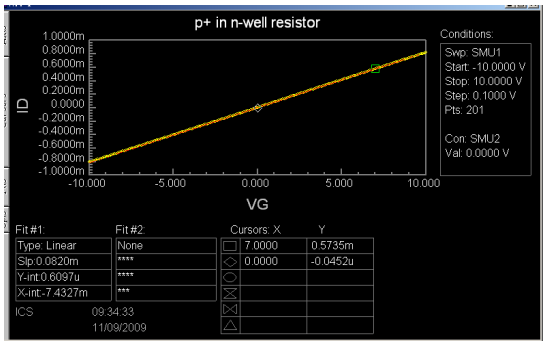
Poly
R = 1/SLOPE
= 1/0.681m
= 1468 ohm
Rhos = 1468/39
=37.6 ohm/sq



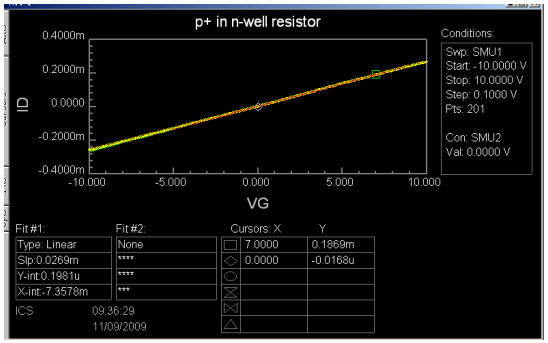


RESISTORS

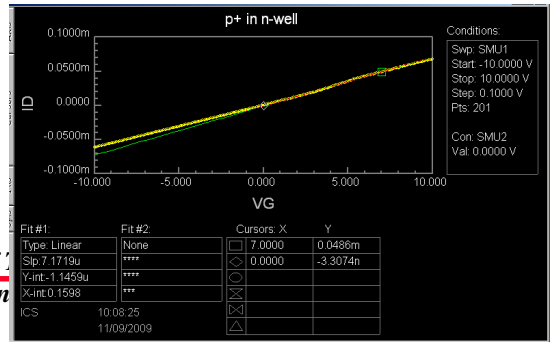




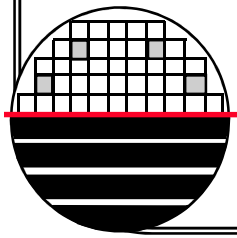
R=12K ohms
Theoretical R = Rhos L/W
= 45 (12*390)/9 = 23K



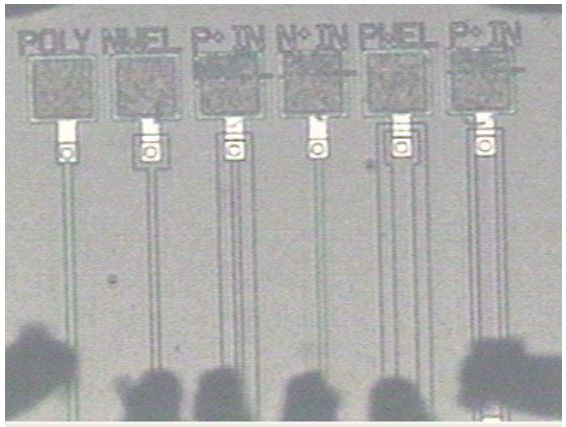
R=37.1K ohms
Theoretical R = Rhos L/W
= 45 (12*390)/6 = 35K



R= 139K ohms
Theoretical R = Rhos L/W
= 45 (12*390)/3 = 70K



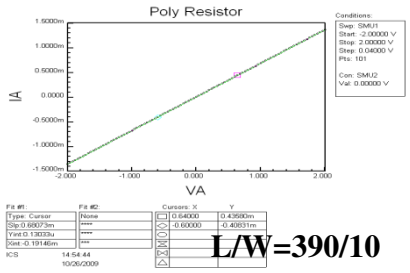
RESISTORS



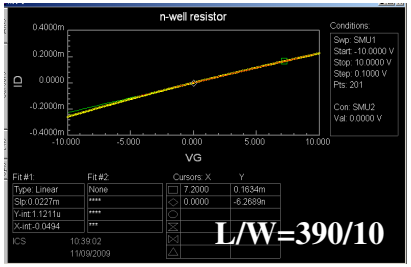
390/10um 390/30um
L/W

R= 1/slope

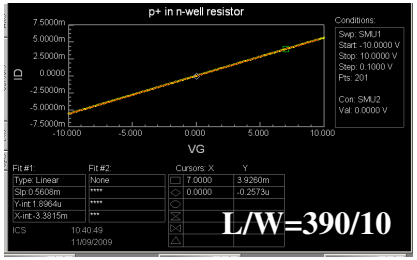
Rhos= R W/L



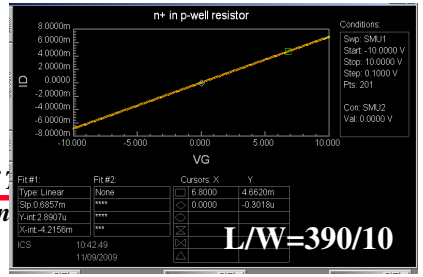
Poly
R=1468
Rhos=37.6



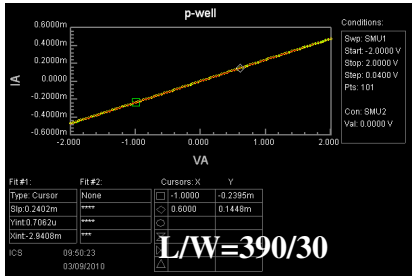
nWell
R=44K
Rhos=1.13K



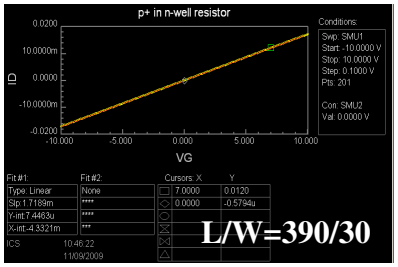
P+ in nWell
R=1.78K
Rhos=45.7



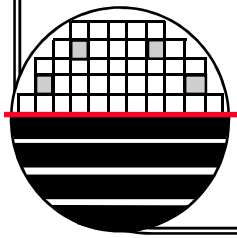
n+ in pWell
R=1.46K
Rhos=37.4



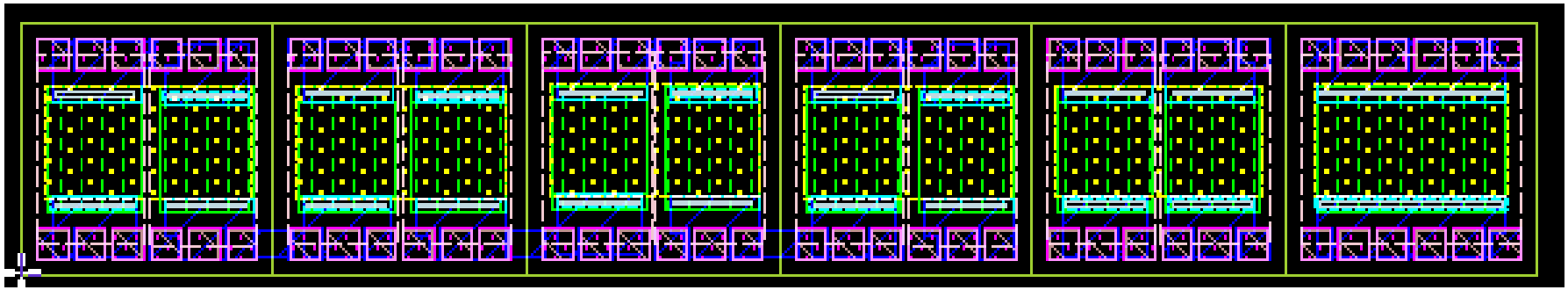
Pwell
R=4160
Rhos=320



P+ in nWell
R=582
Rhos=44.8

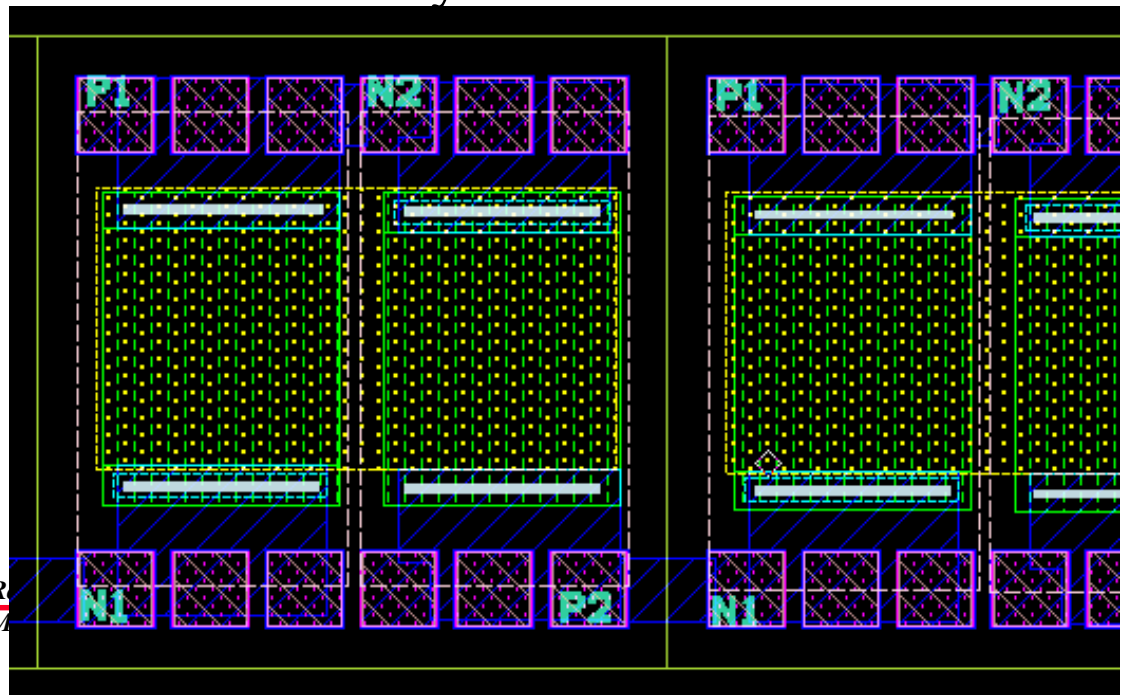


PHOTOVOLTAIC DEVICES



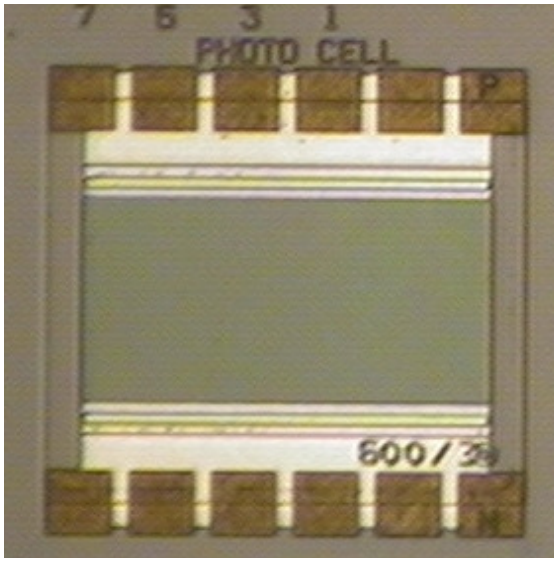
8 cell battery → dual cells single cell

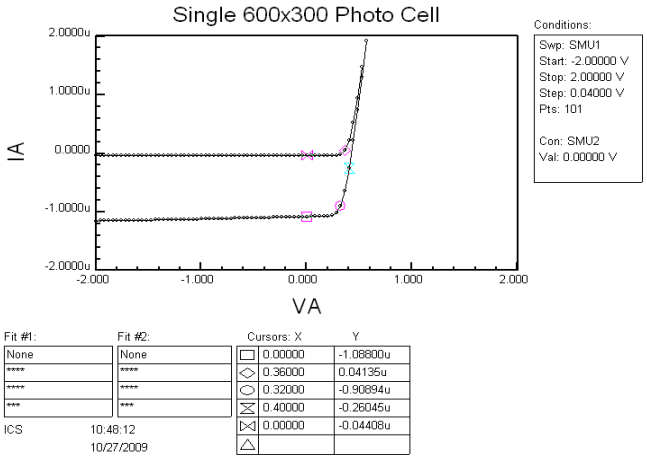
P+ in Nwell



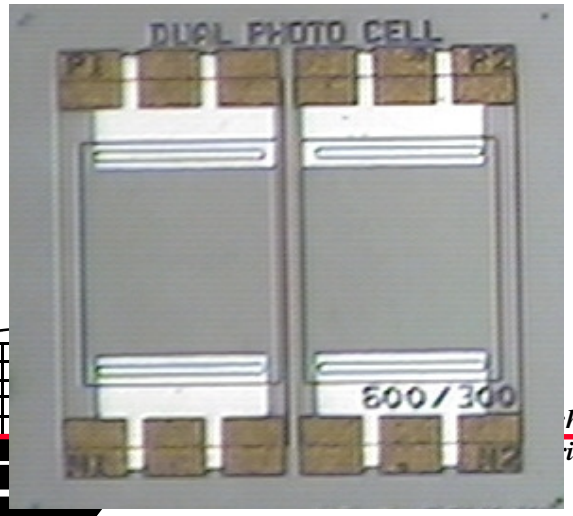
~350µm
by
~350µm

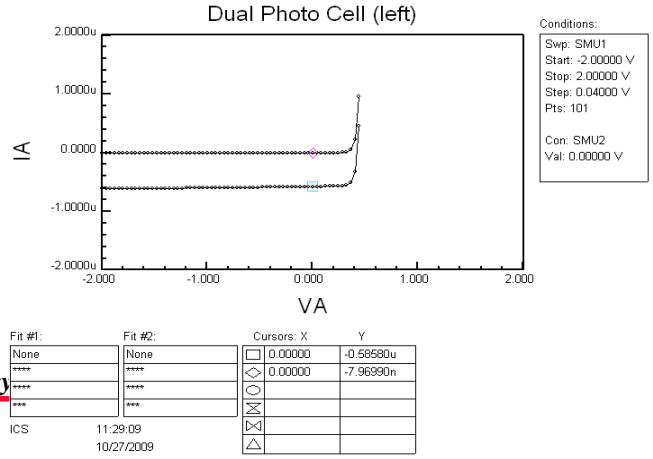
SINGLE AND DUAL PHOTO CELL





Isc = 1.088 uA
or 6 A/m2

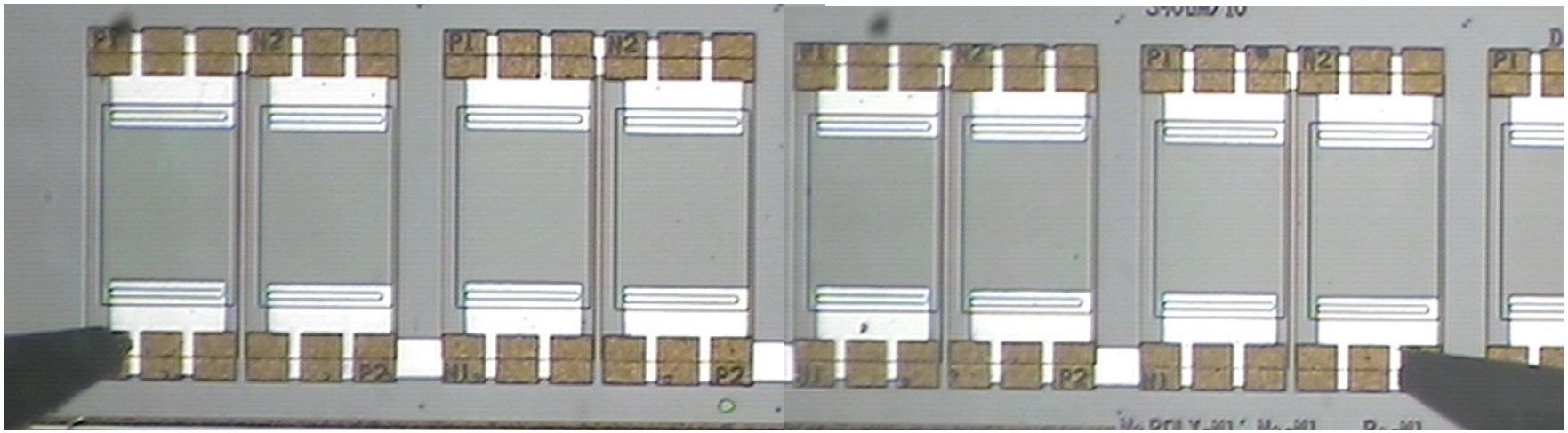


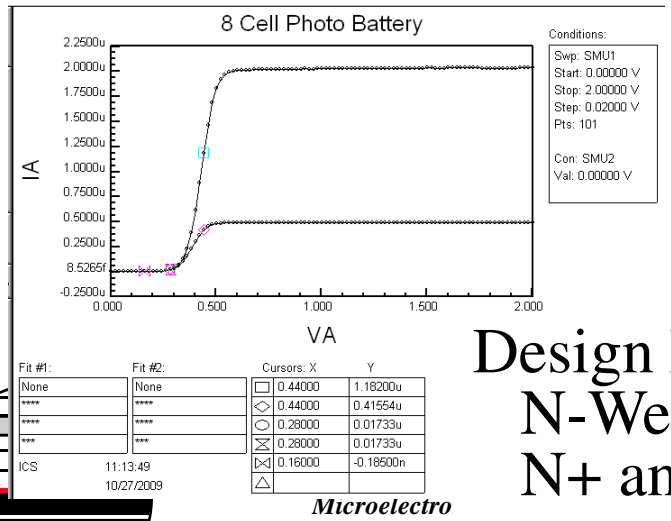


Isc = 0.585 uA
or 3.25 A/m2

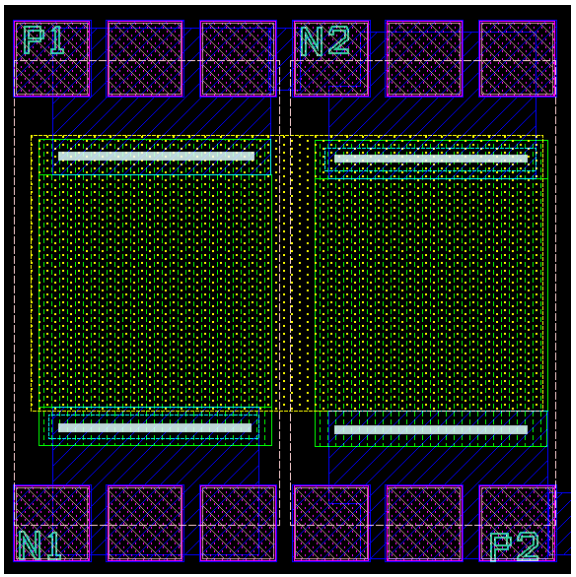
hnology
ing

8-CELL PHOTO BATTERY

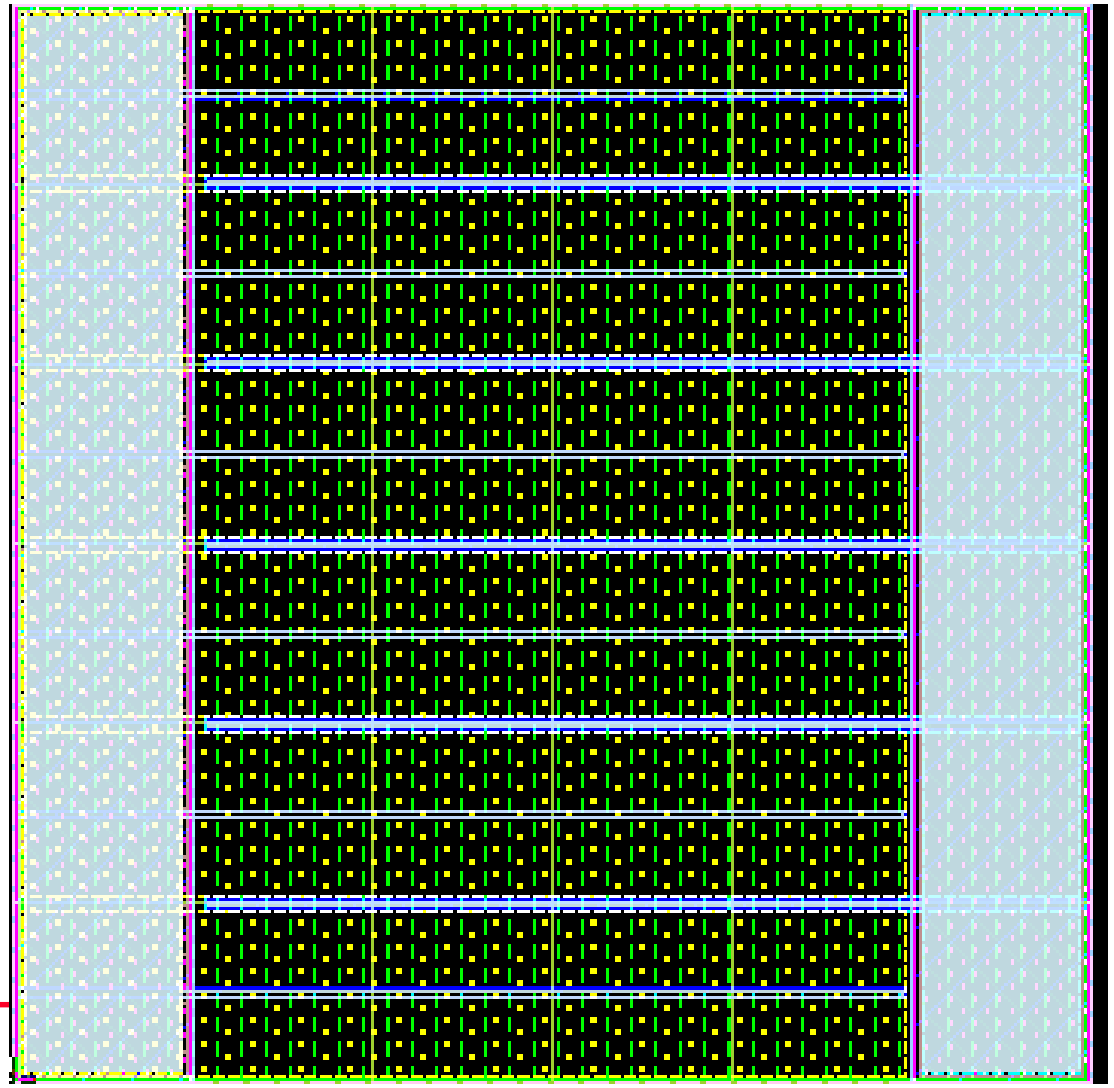




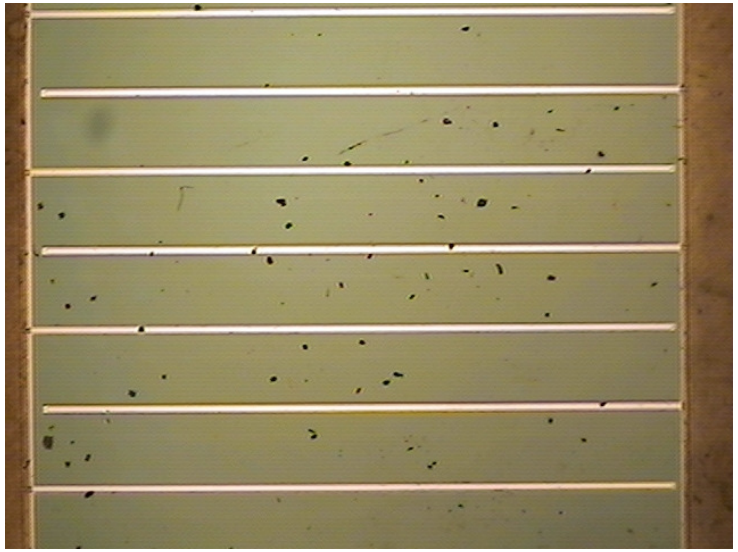
Design Errors
- N-Wells too close
- N+ and P+ not correct

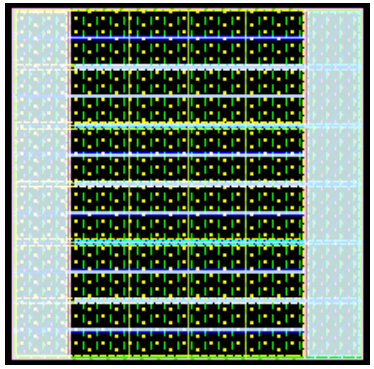


BIG PHOTO VOLTAIC CELL

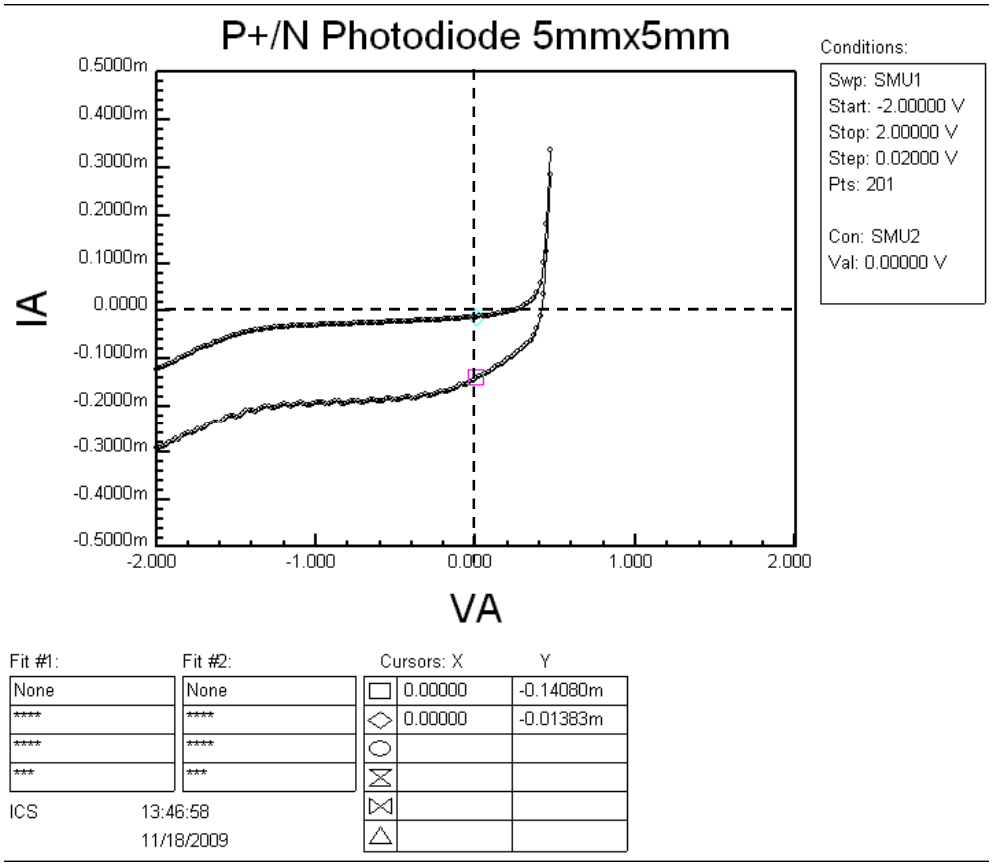


LARGE 5mm X 5mm PHOTODIODE





5mm
x
3.33mm



Isc = 0.15mA (short circuit current)
or 9.09 A/m2

DIGITAL CIRCUITS

Primitive Cells

INVERTER, NAND2,3,4, NOR2,3,4, NULL

Basic Cells

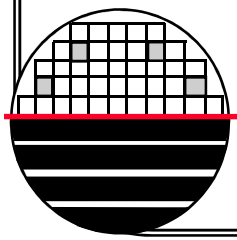
XOR, MUX, DEMUX, ENCODER, DECODER

FULL ADDER, FLIP FLOPS

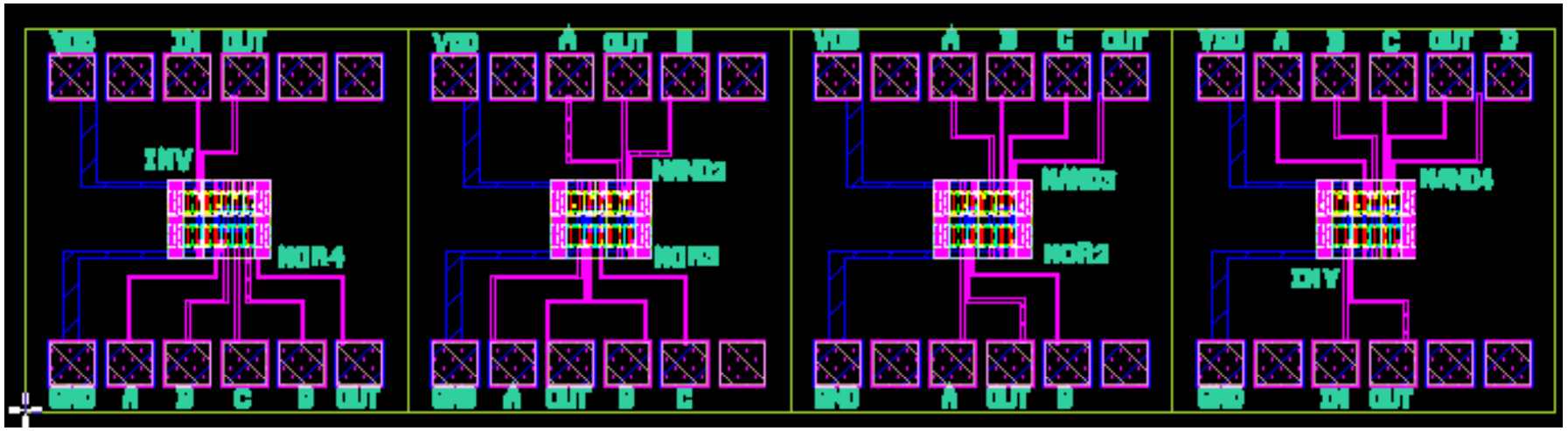
Macro Cells

BINARY COUNTER

SRAM

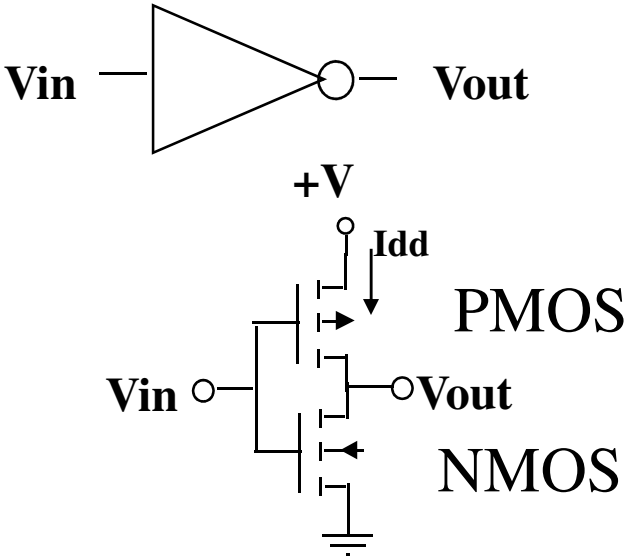


PRIMITIVE CELLS WITH PADS



INV/NOR4 NOR3/NAND2 NOR2/NAND3 INV/NAND4

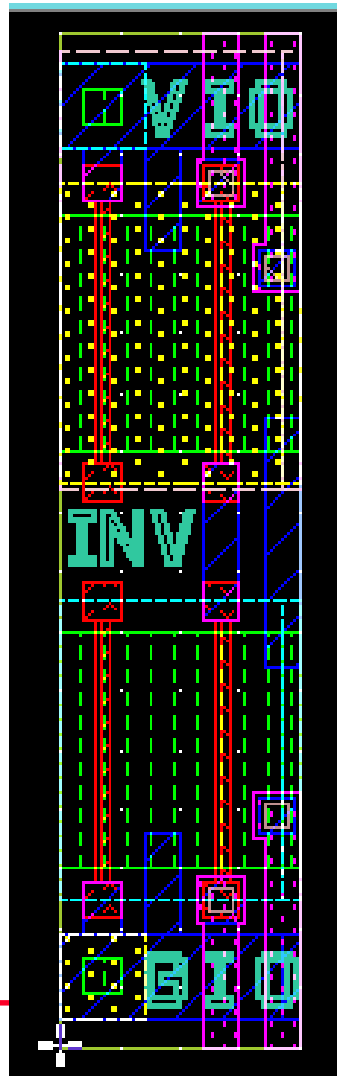
CMOS INVERTER

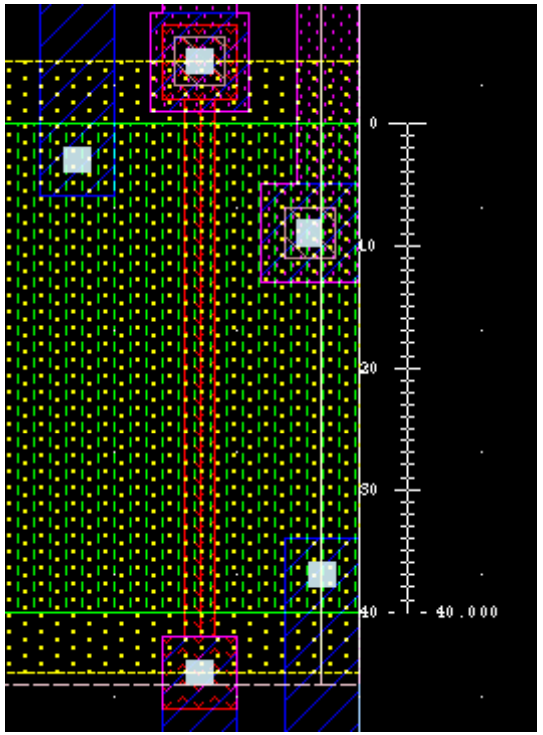


CMOS

TRUTH TABLE

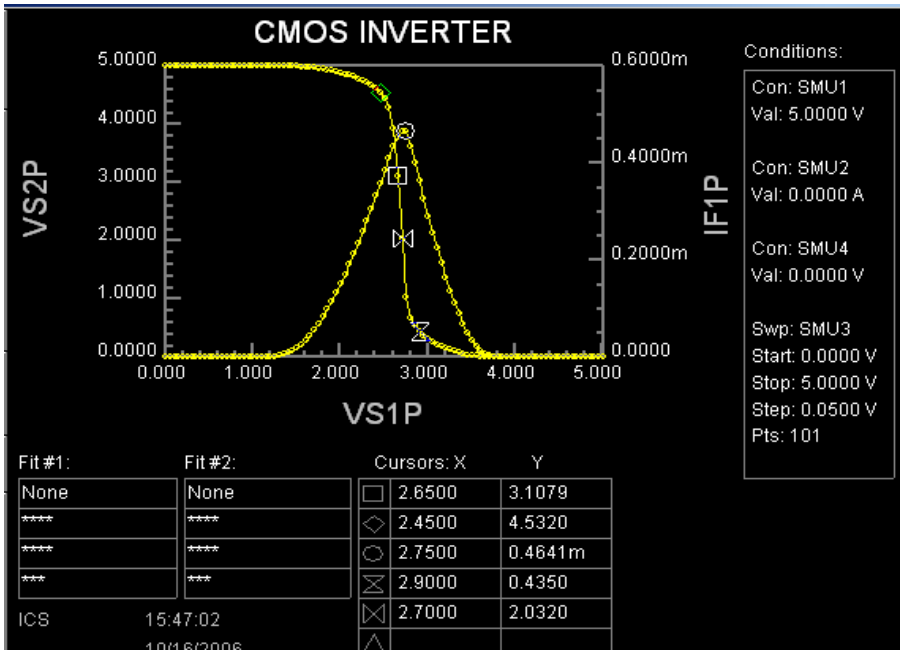
VIN	VOUT
0	1
1	0

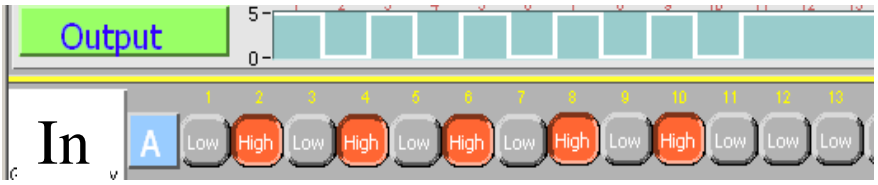


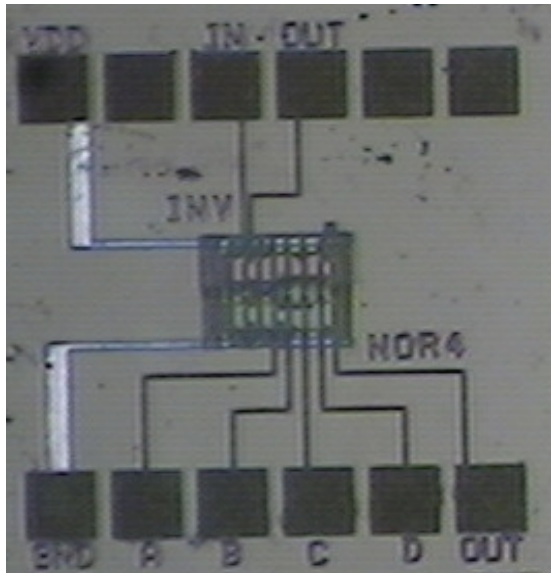


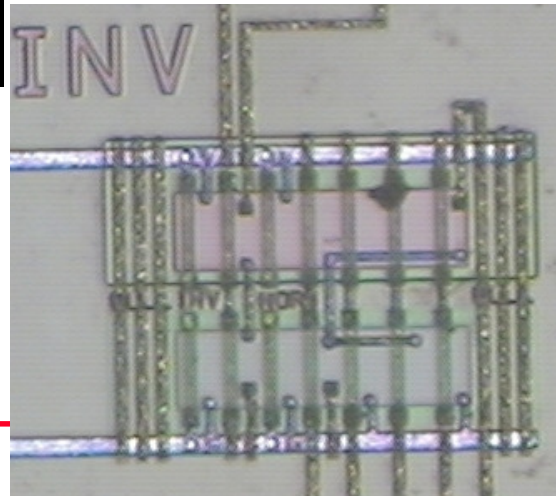
W = 40 µm
Ldrawn = 2.5µm
Lpoly = 1.0µm
Leff = 0.35 µm

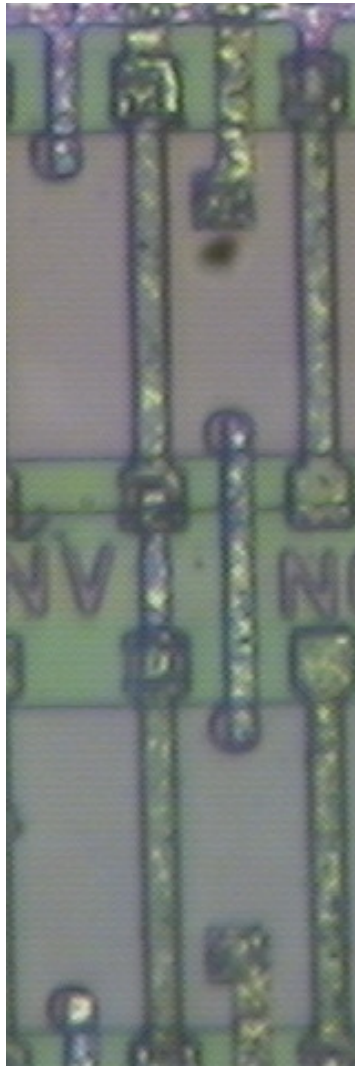
INVERTER TEST RESULTS



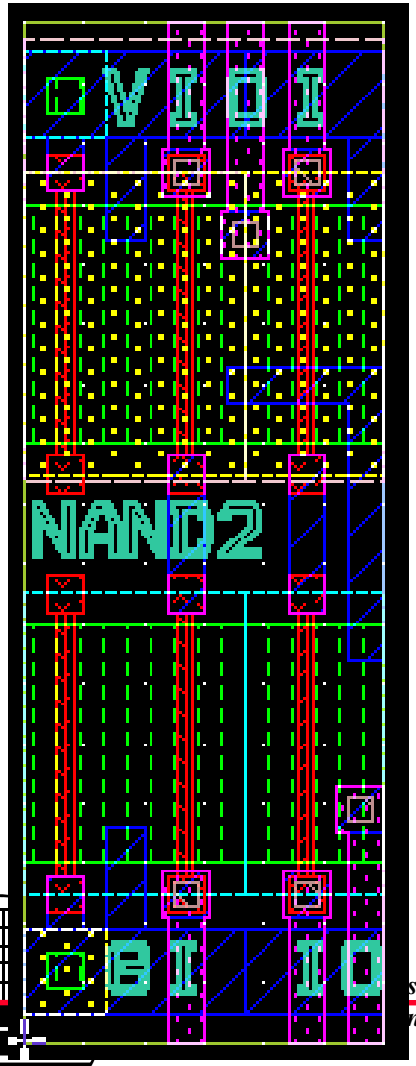


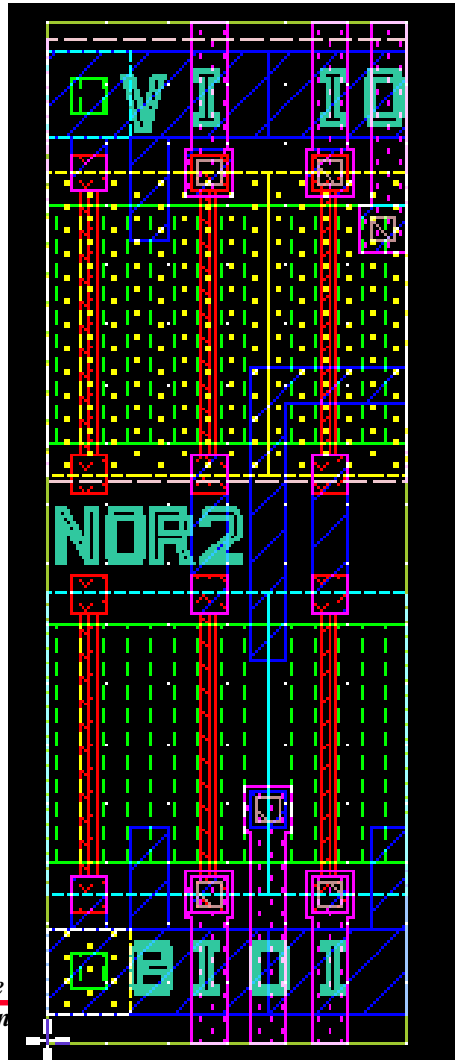


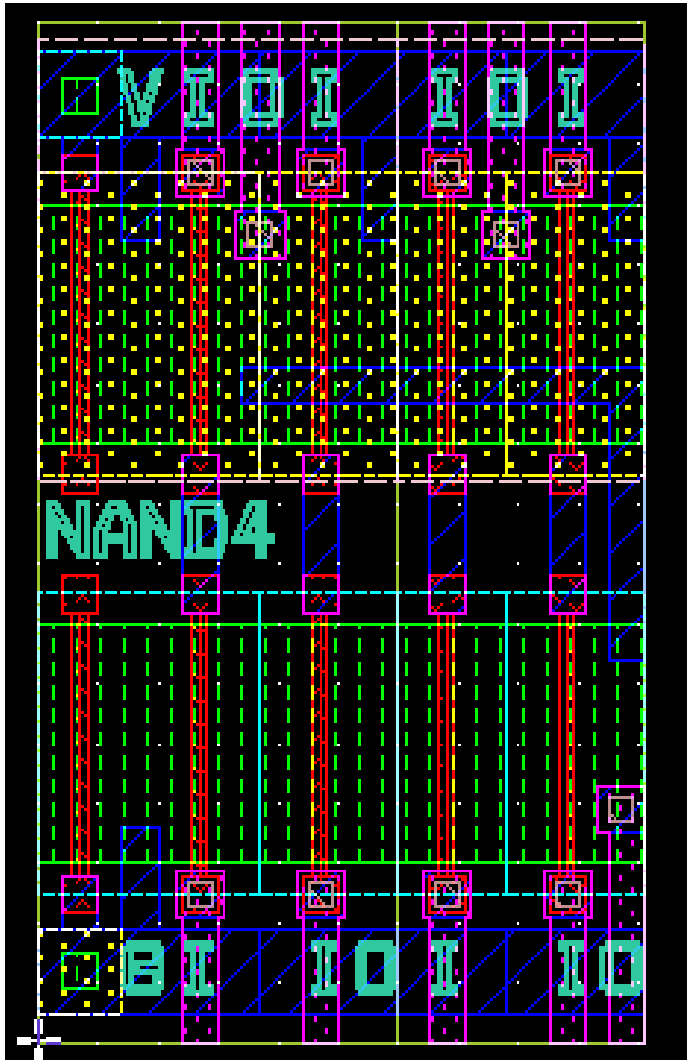




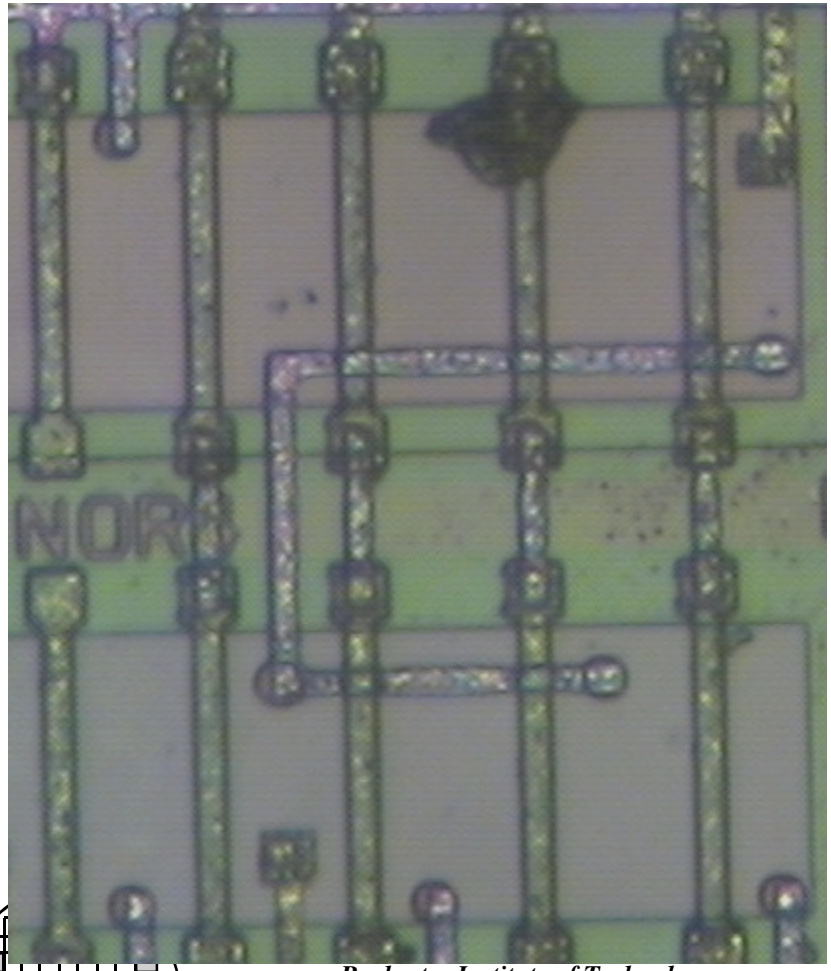
PRIMITIVE CELLS

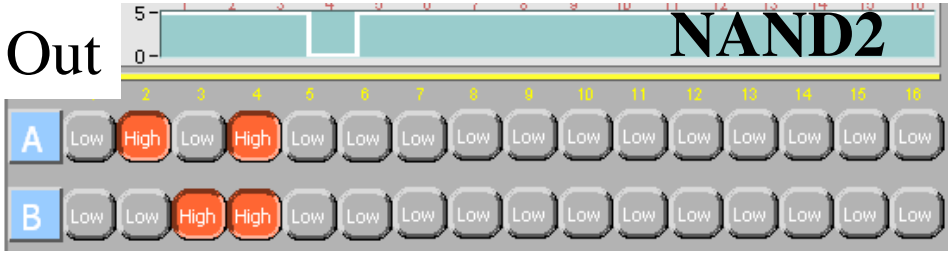


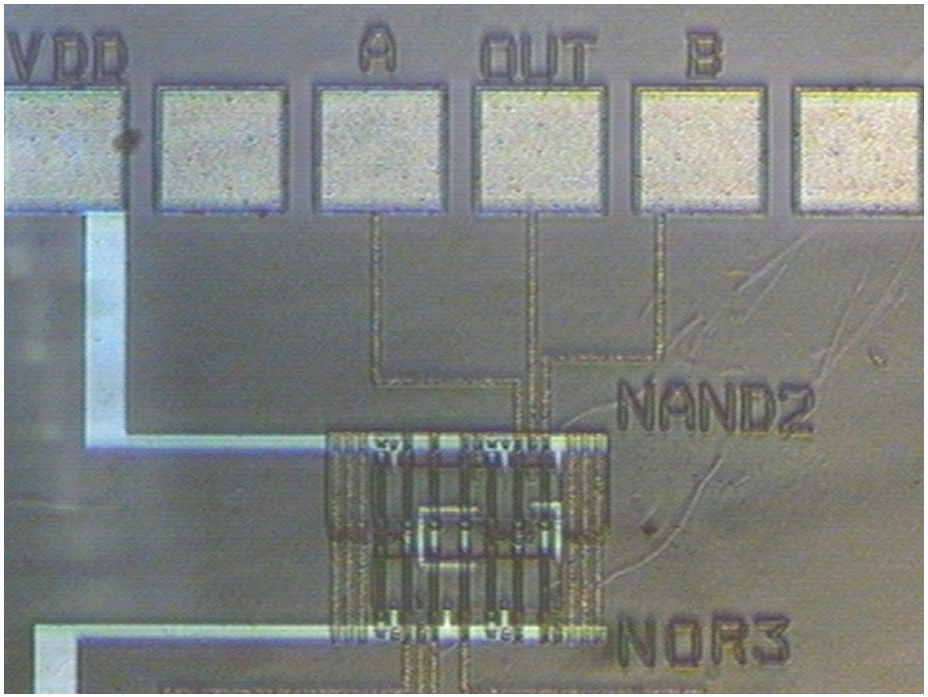




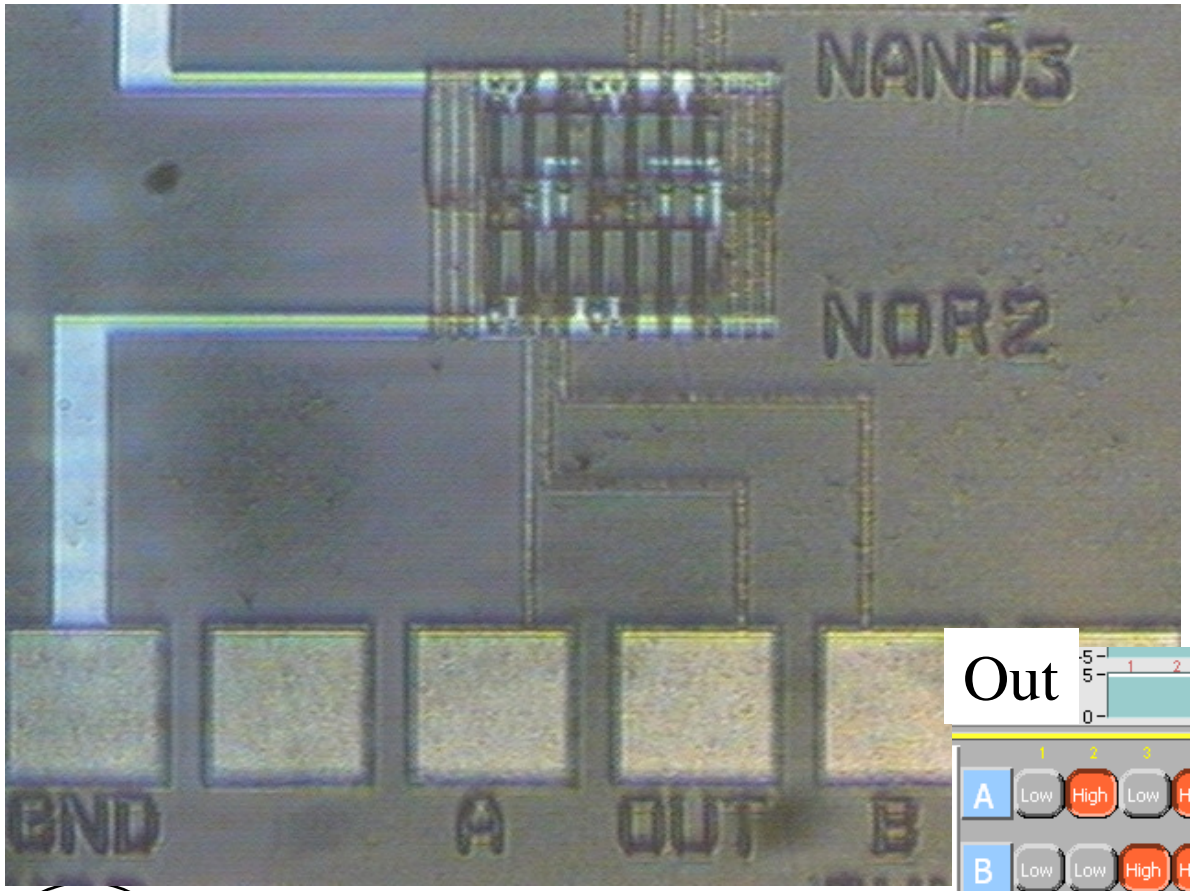
PRIMITIVE CELLS

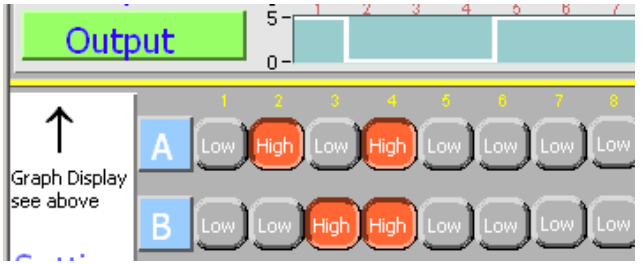




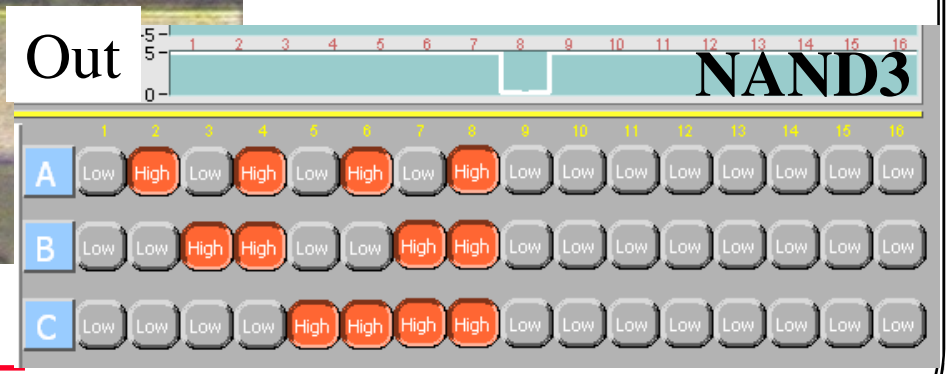


NOR2

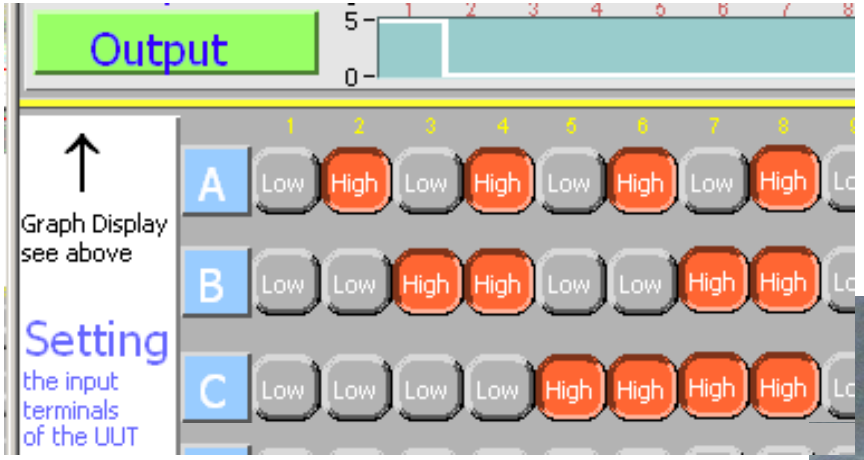




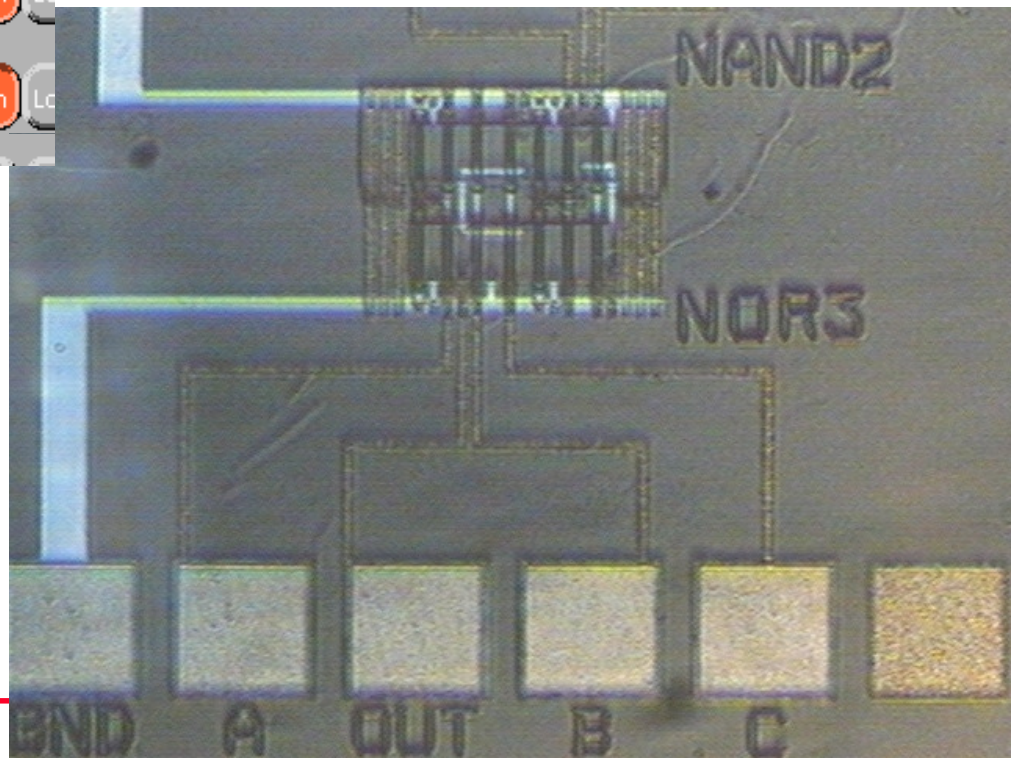
NOR2



NOR3

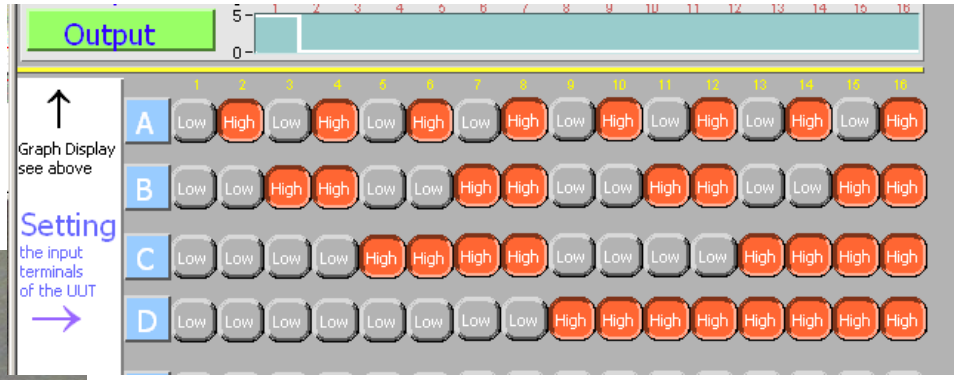


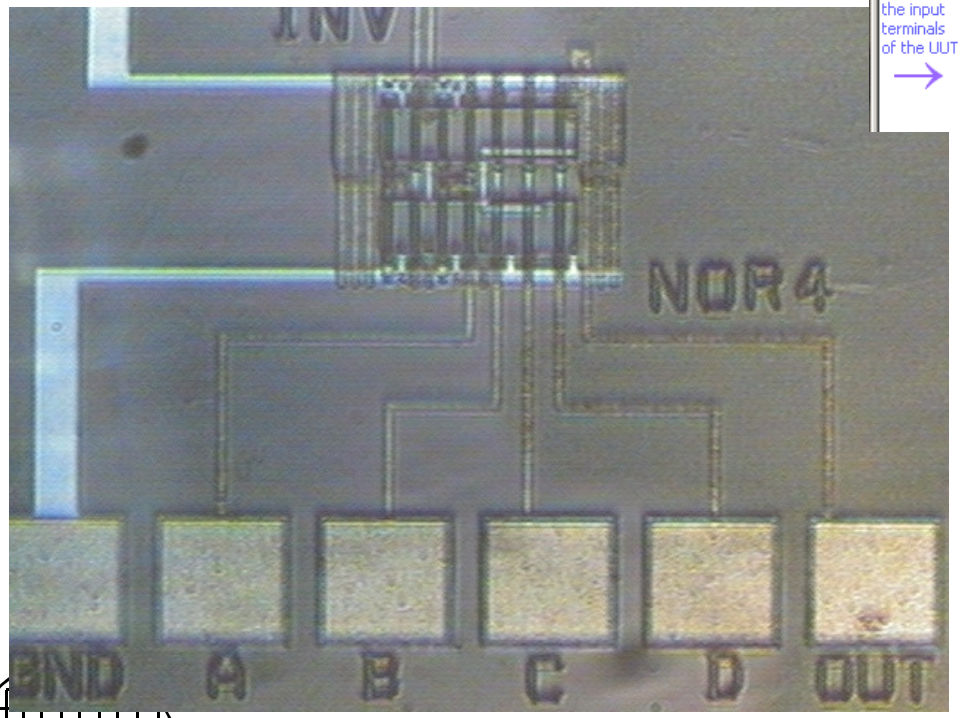
NOR3

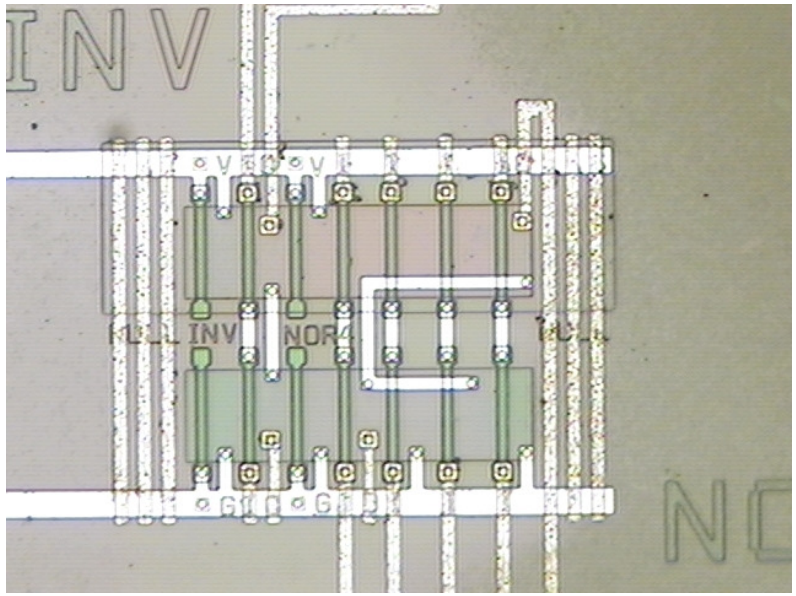


NOR4

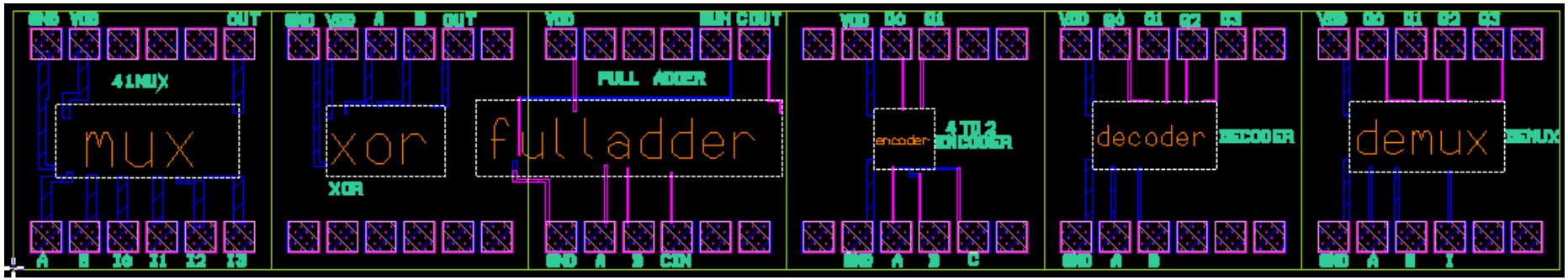
NOR4



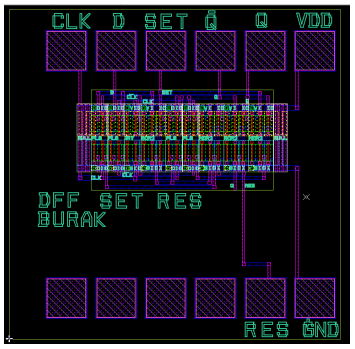




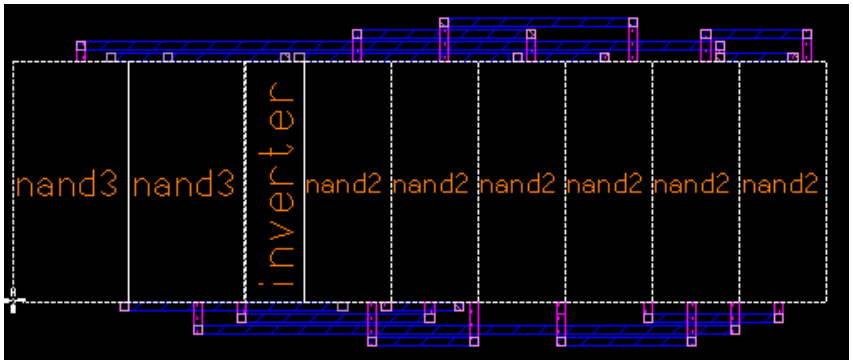
BASIC DIGITAL CELLS WITH PADS



Multiplexer XOR Full Adder Encoder Decoder Demux

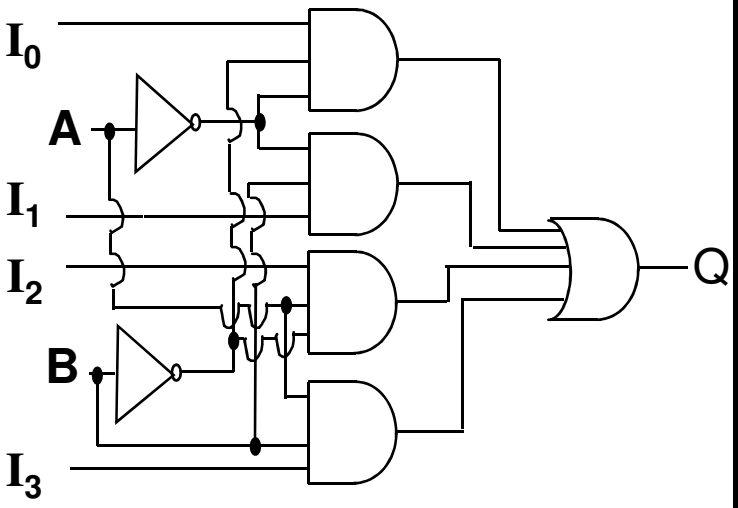


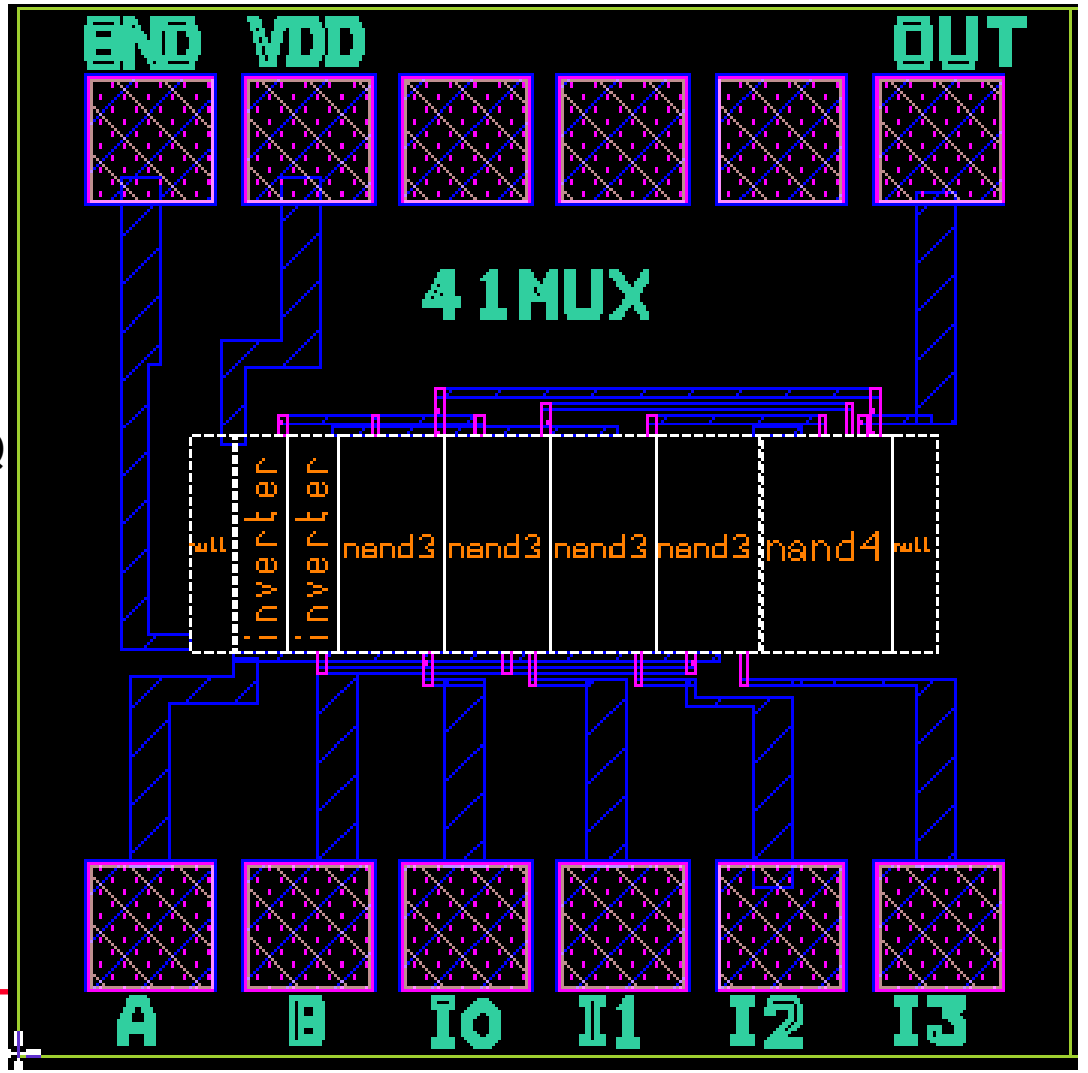
Edge Triggered DFF



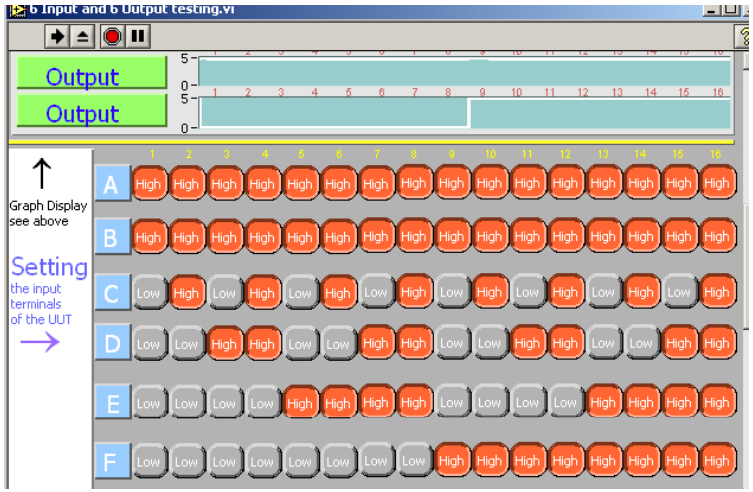
JK FF

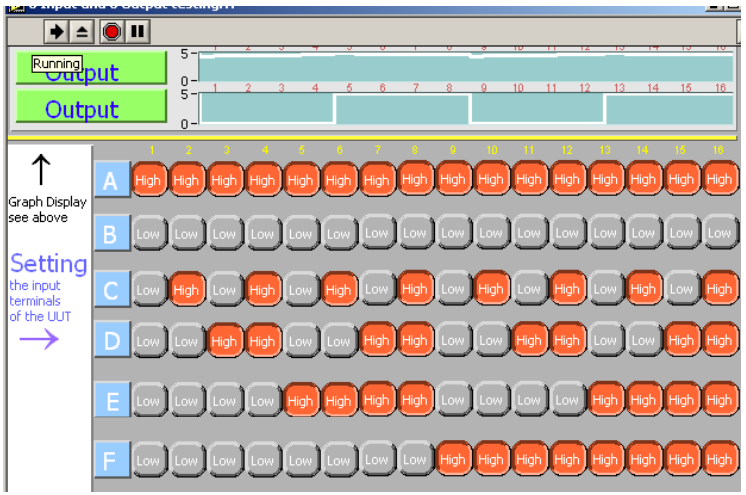
4 TO 1 MULTIPLEXER

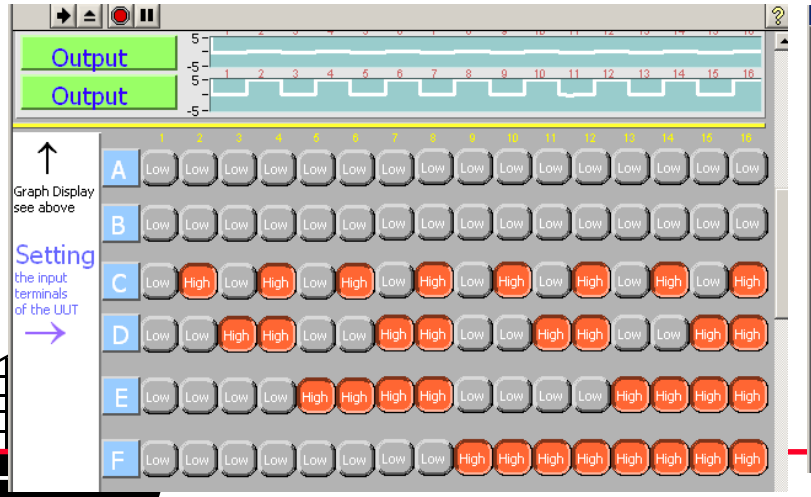


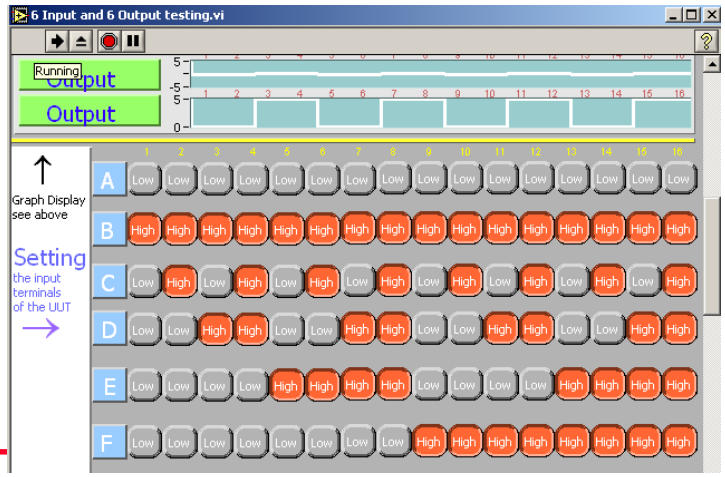


4 TO 1 MULTIPLEXER

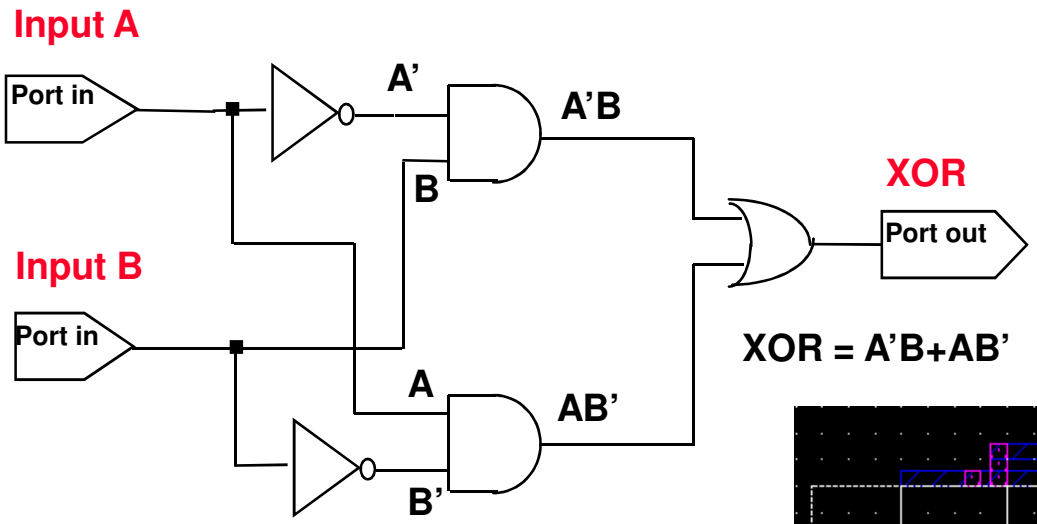






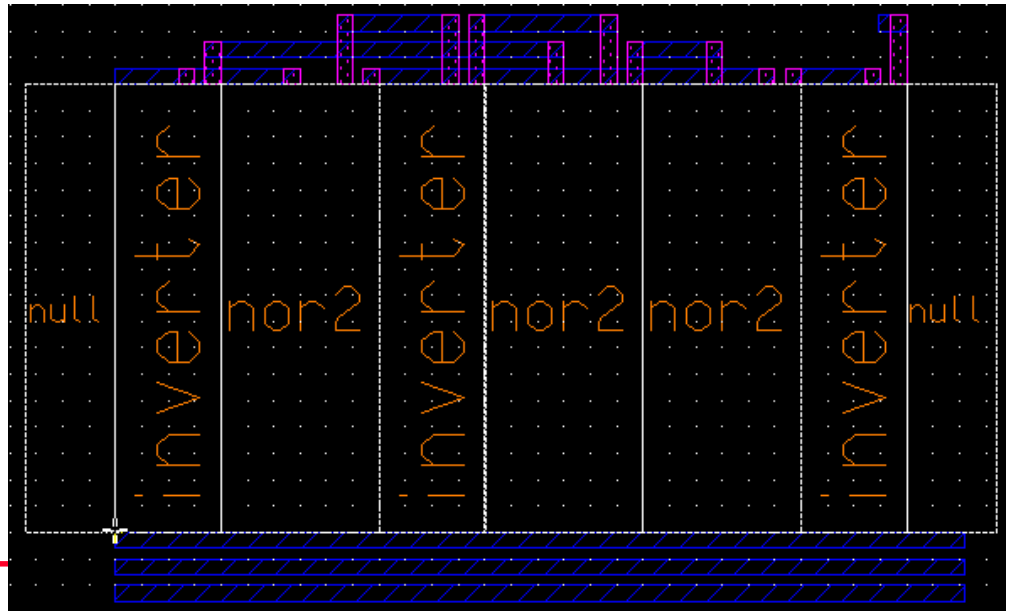


BASIC CELL XOR

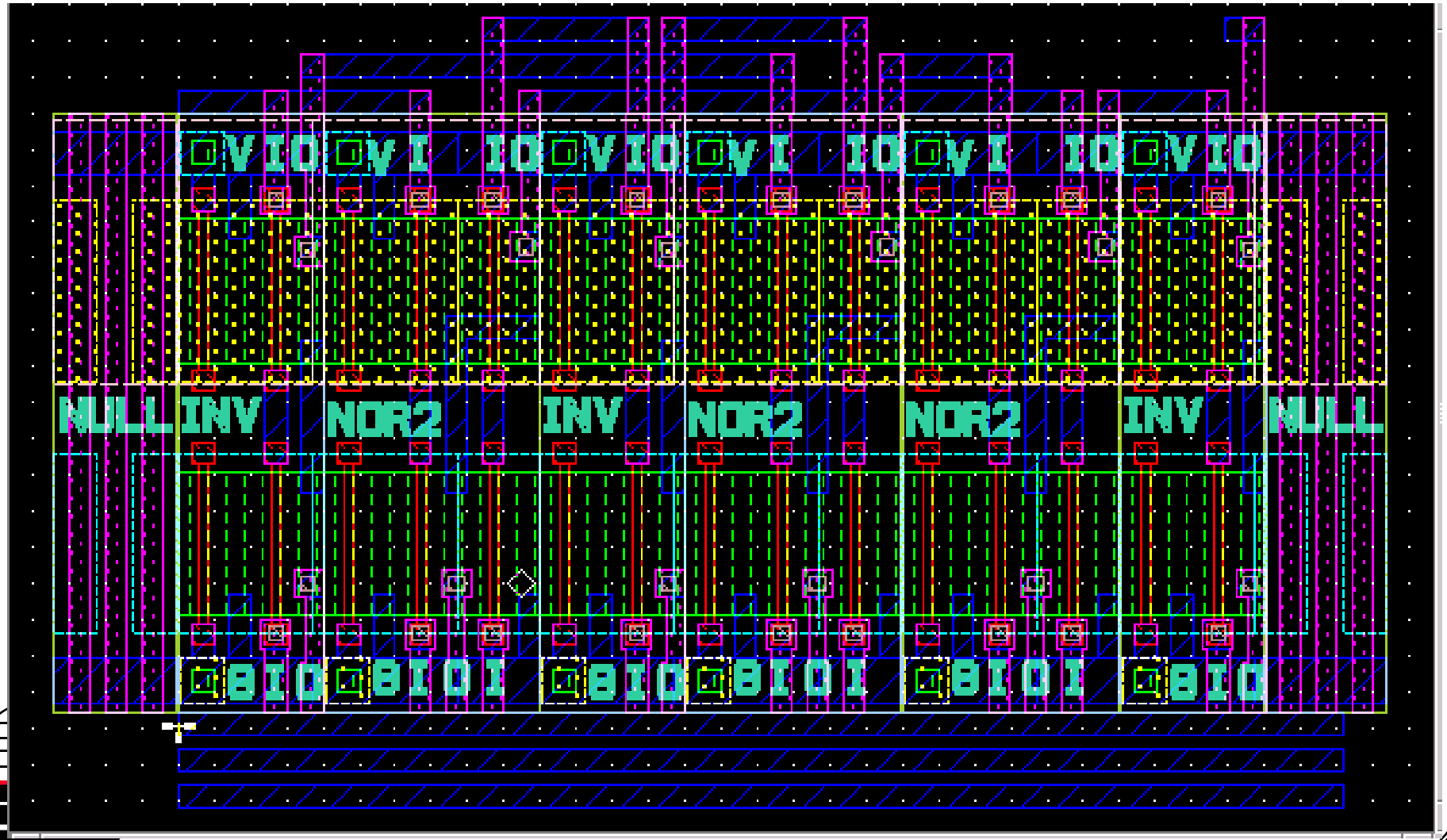


XOR = A'B+AB'

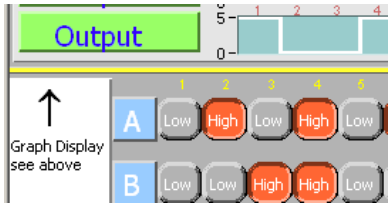
XOR



XOR

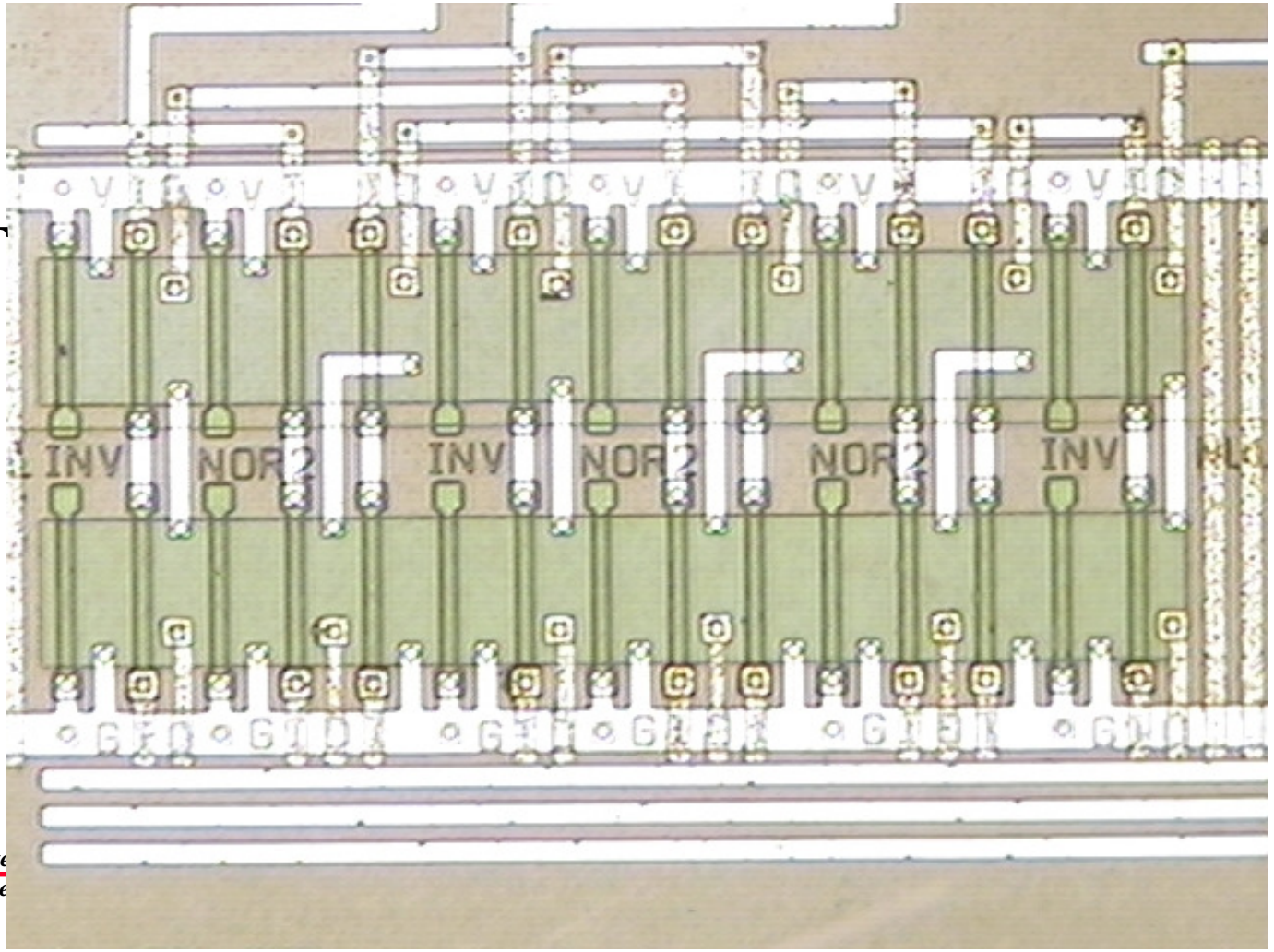

VDD
VDD
VDD
VDD
VDD
VDD
VDD
NULL
INV
NOR2
INV
NOR2
NOR2
INV
NULL
GND
GND
GND
GND
GND
GND
GND

XOR

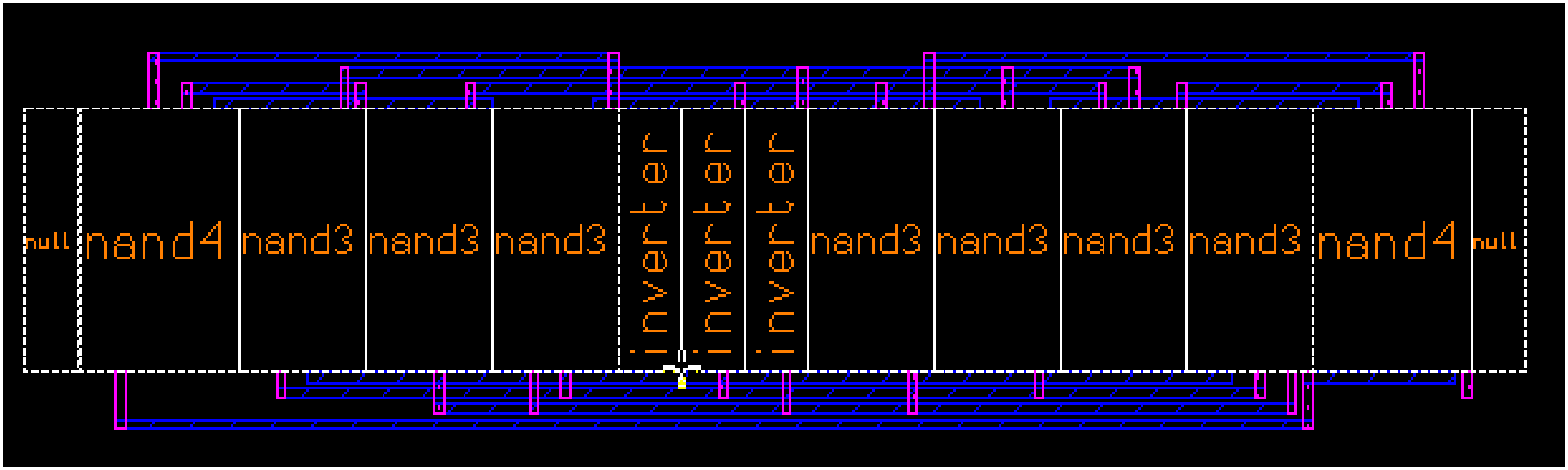


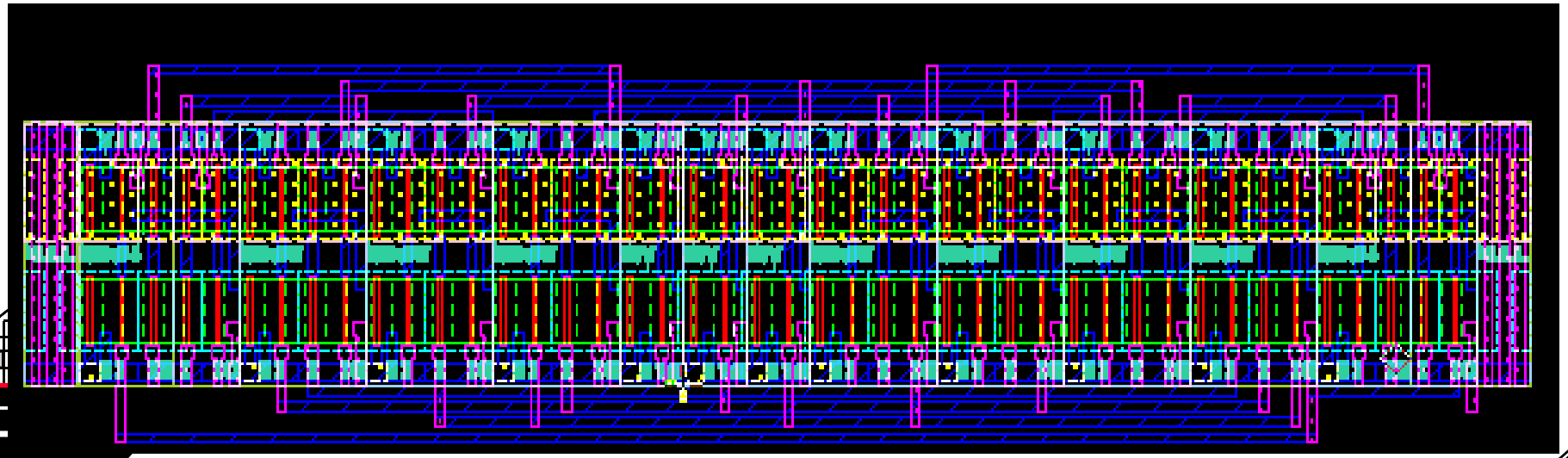
NOT CORRECT

Output Inverted

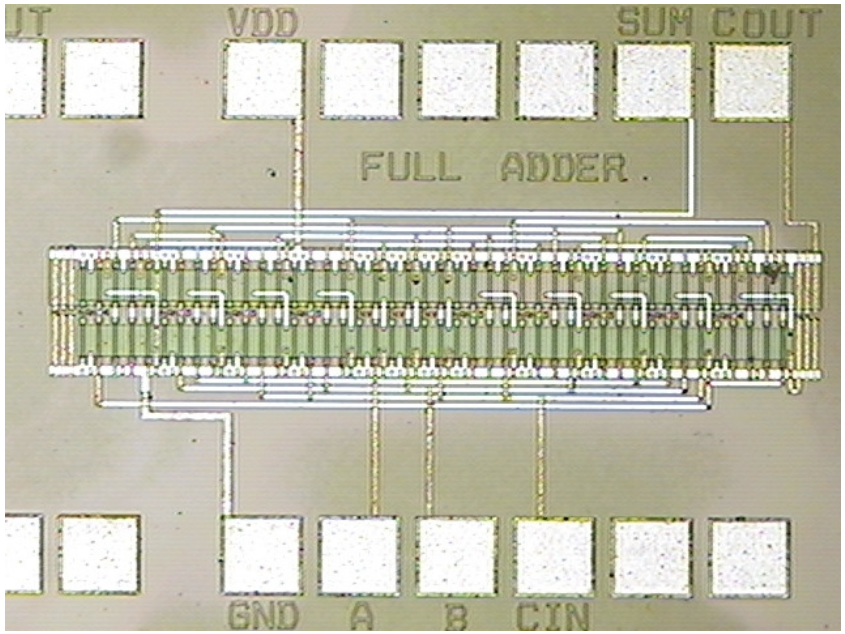


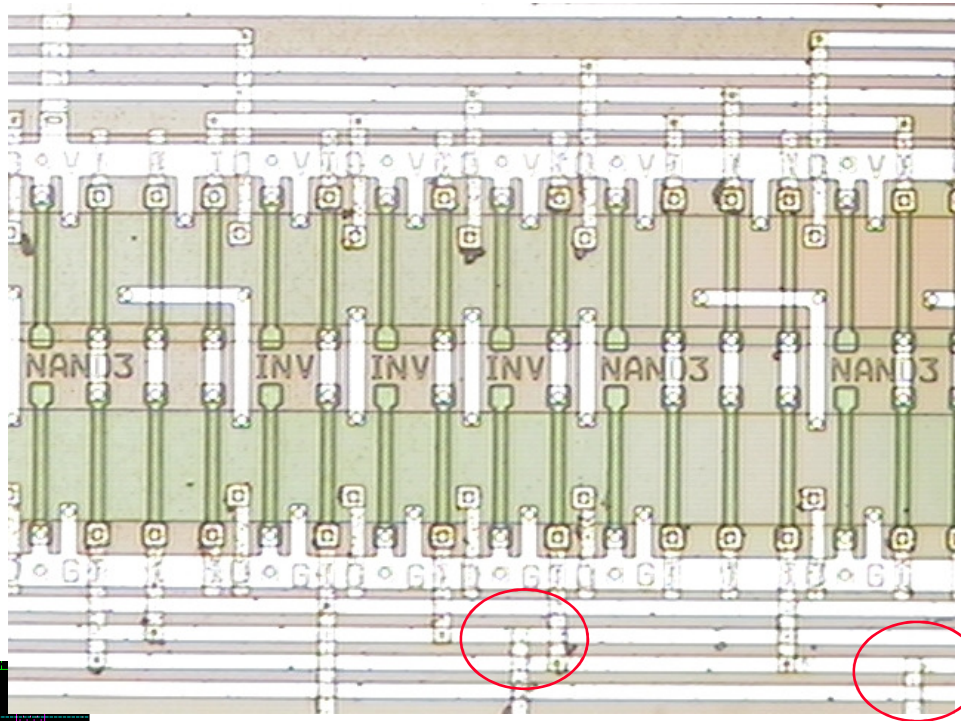
FULL ADDER

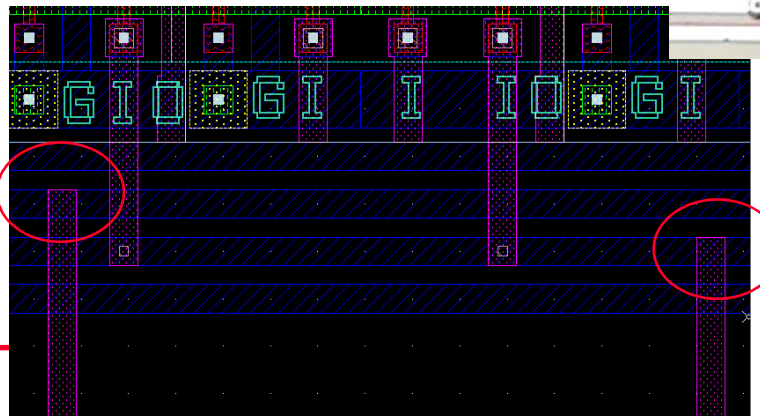




FULL ADDER

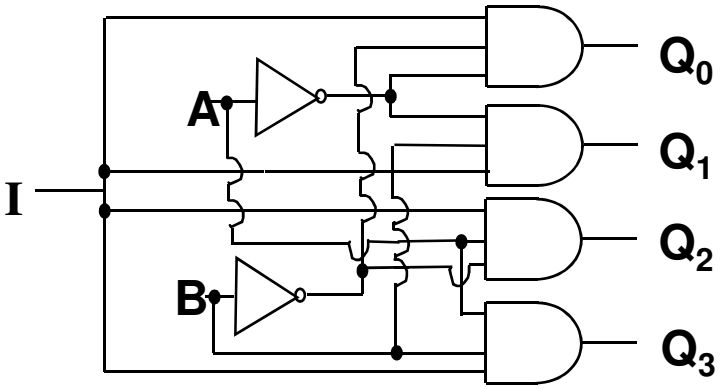


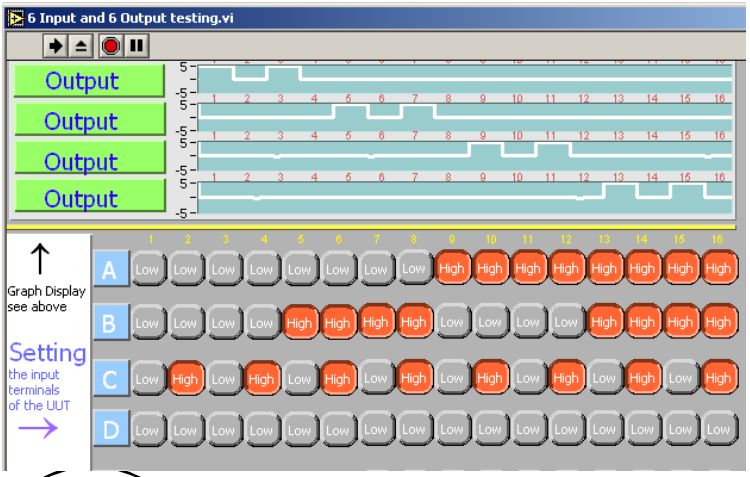


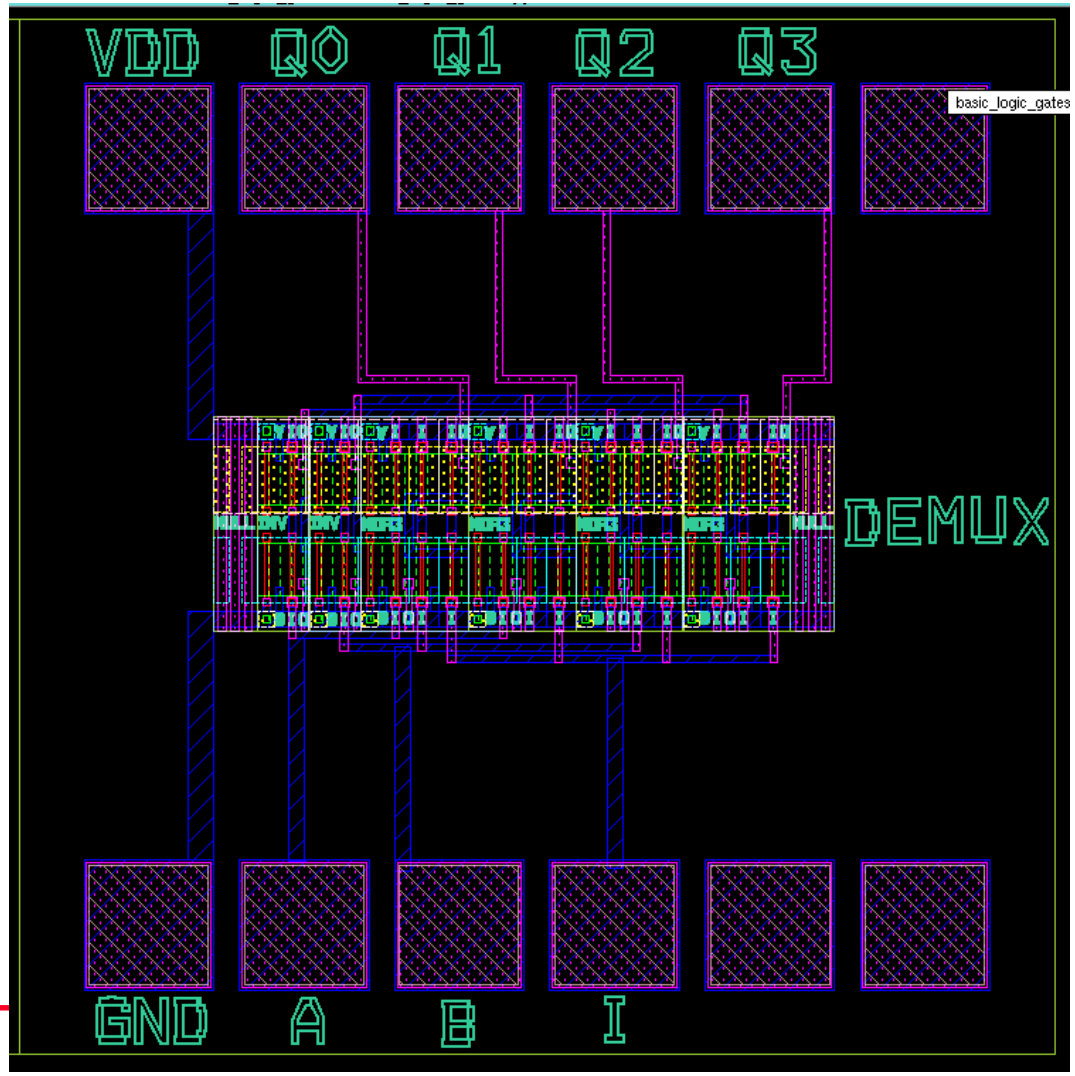


MISSING VIA

1 TO 4 DEMULTIPLEXER



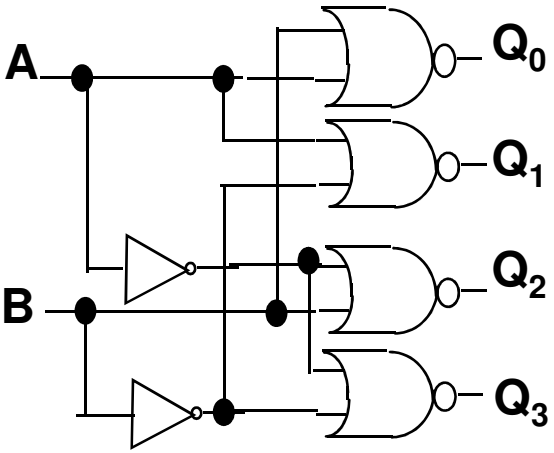


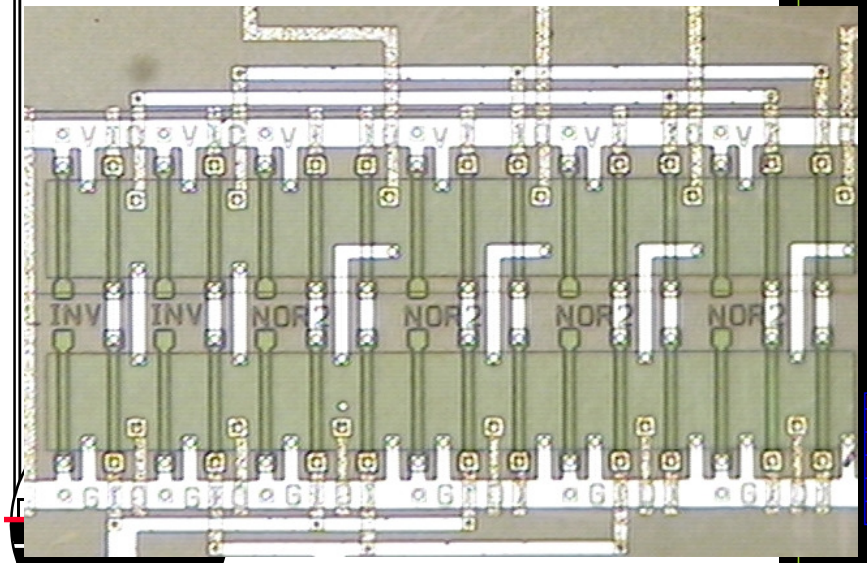


Correct

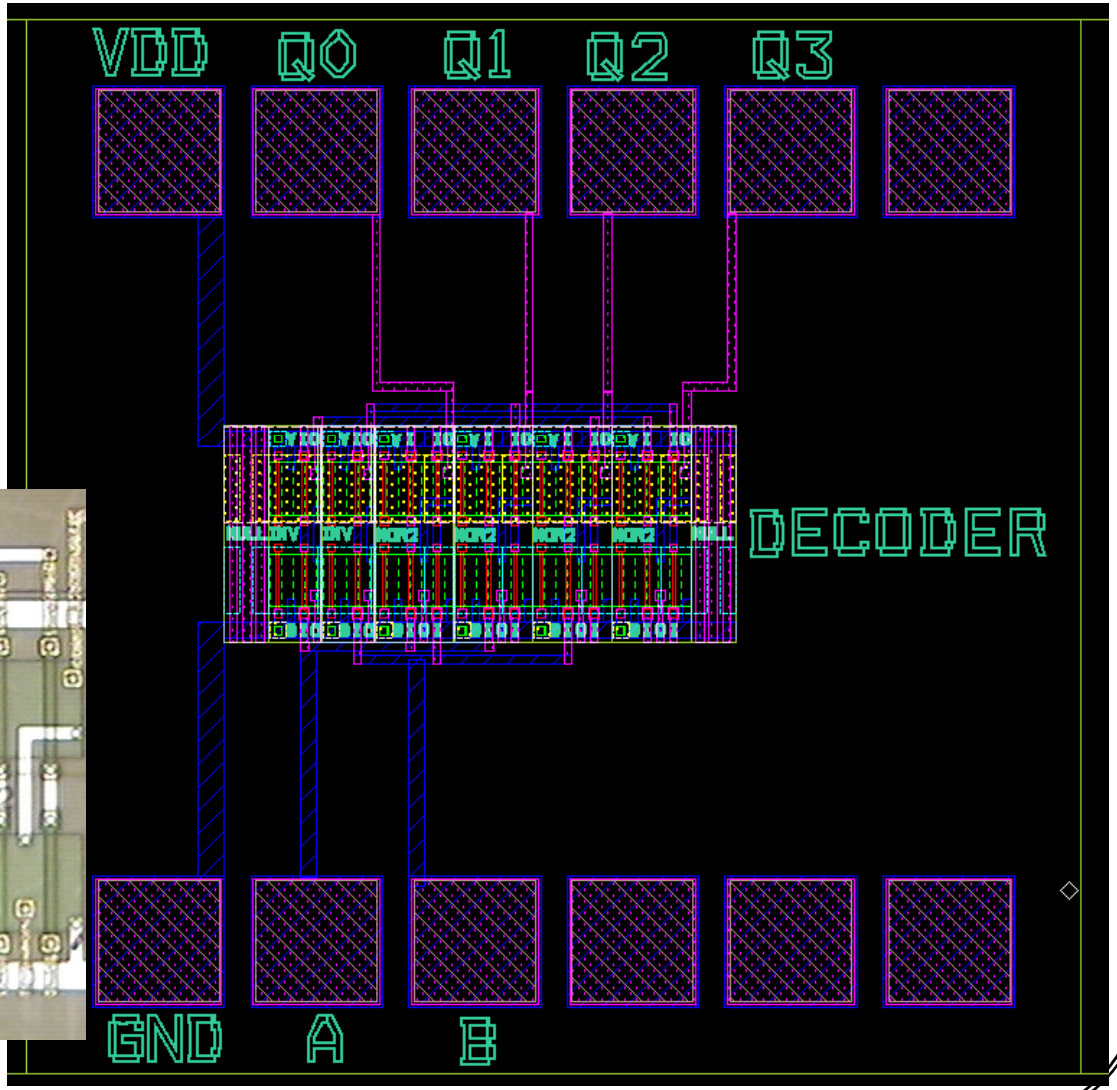
Rochester Institute of Technology
Microelectronic Engineering

DECODER

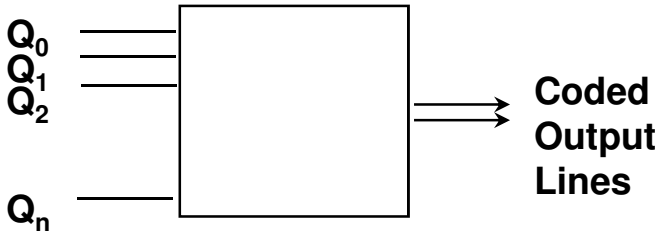




Correct

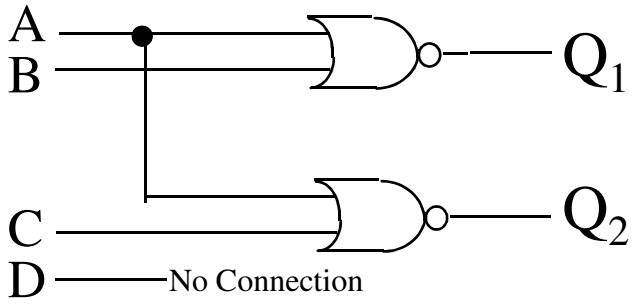


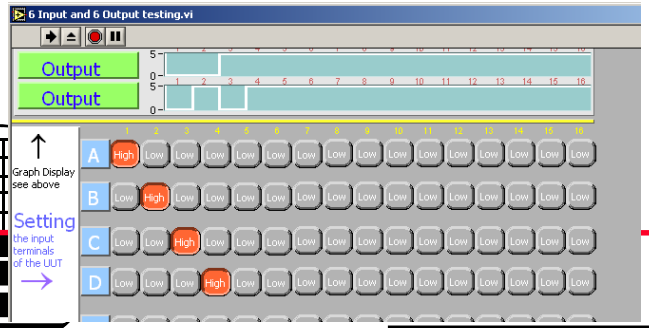
ENCODER

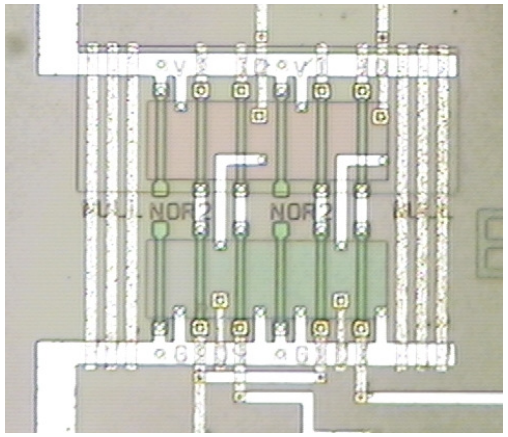


Digital Encoder

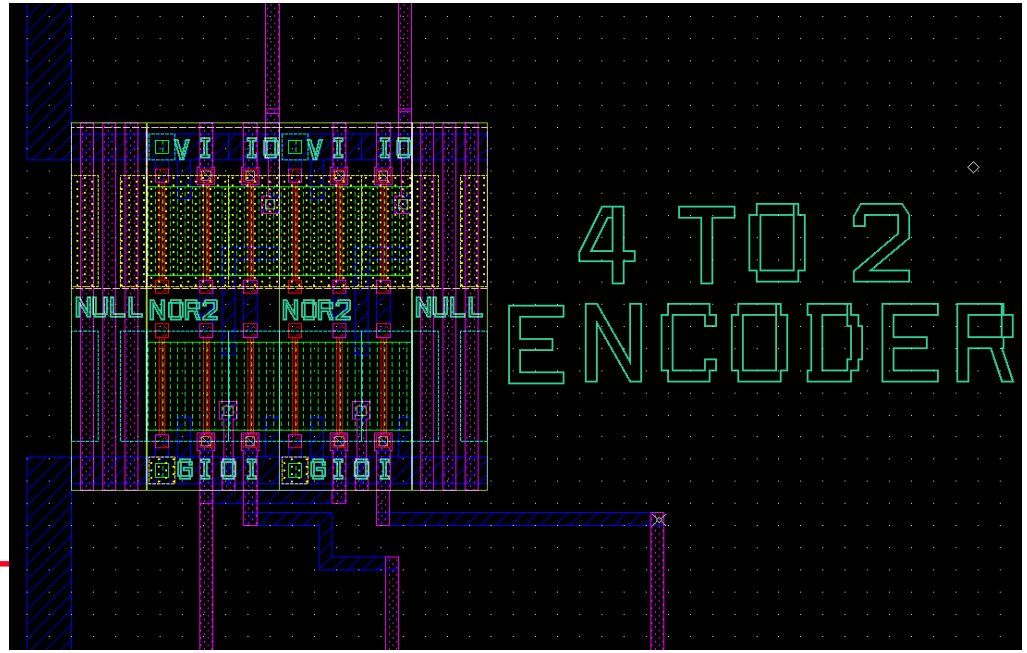
512 inputs can be coded into 9 lines which is a more dramatic benefit



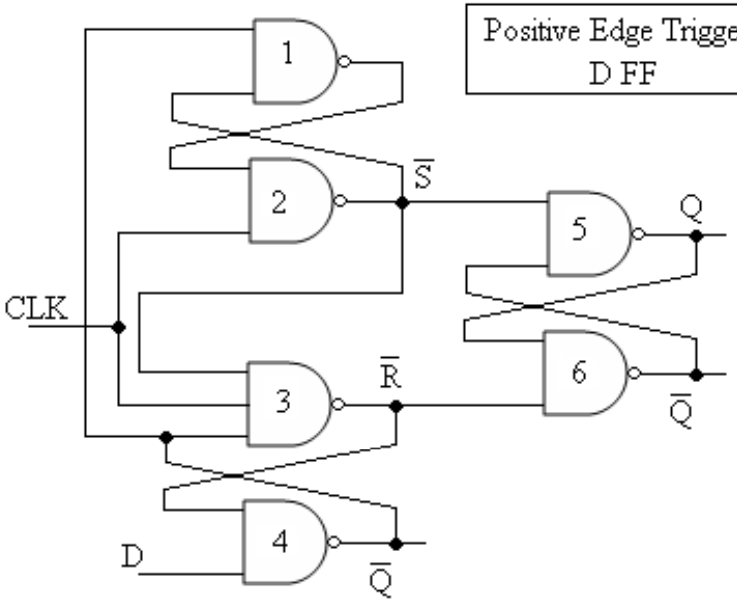


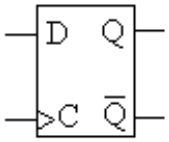


A	B	C	D	Q0	Q1
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

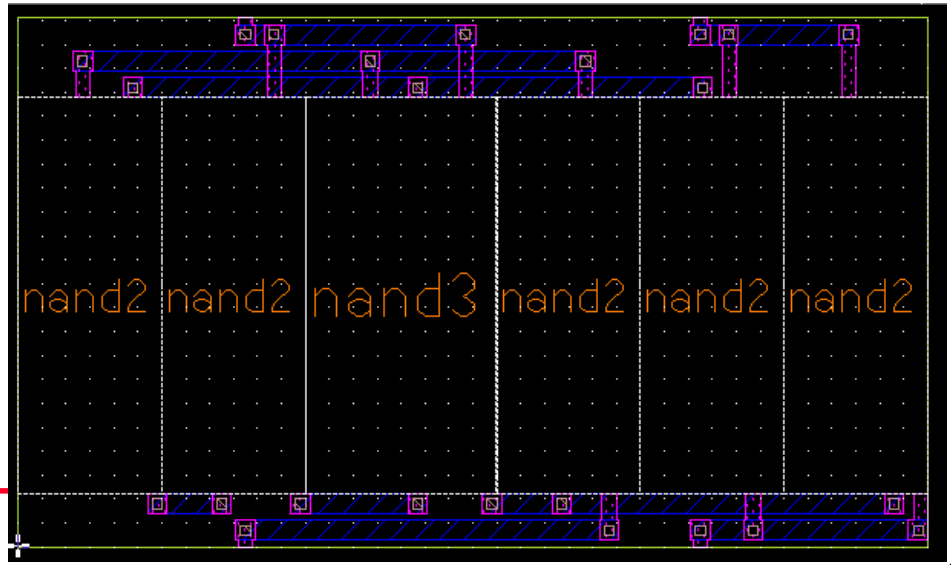


EDGE TRIGGERED D TYPE FLIP FLOP

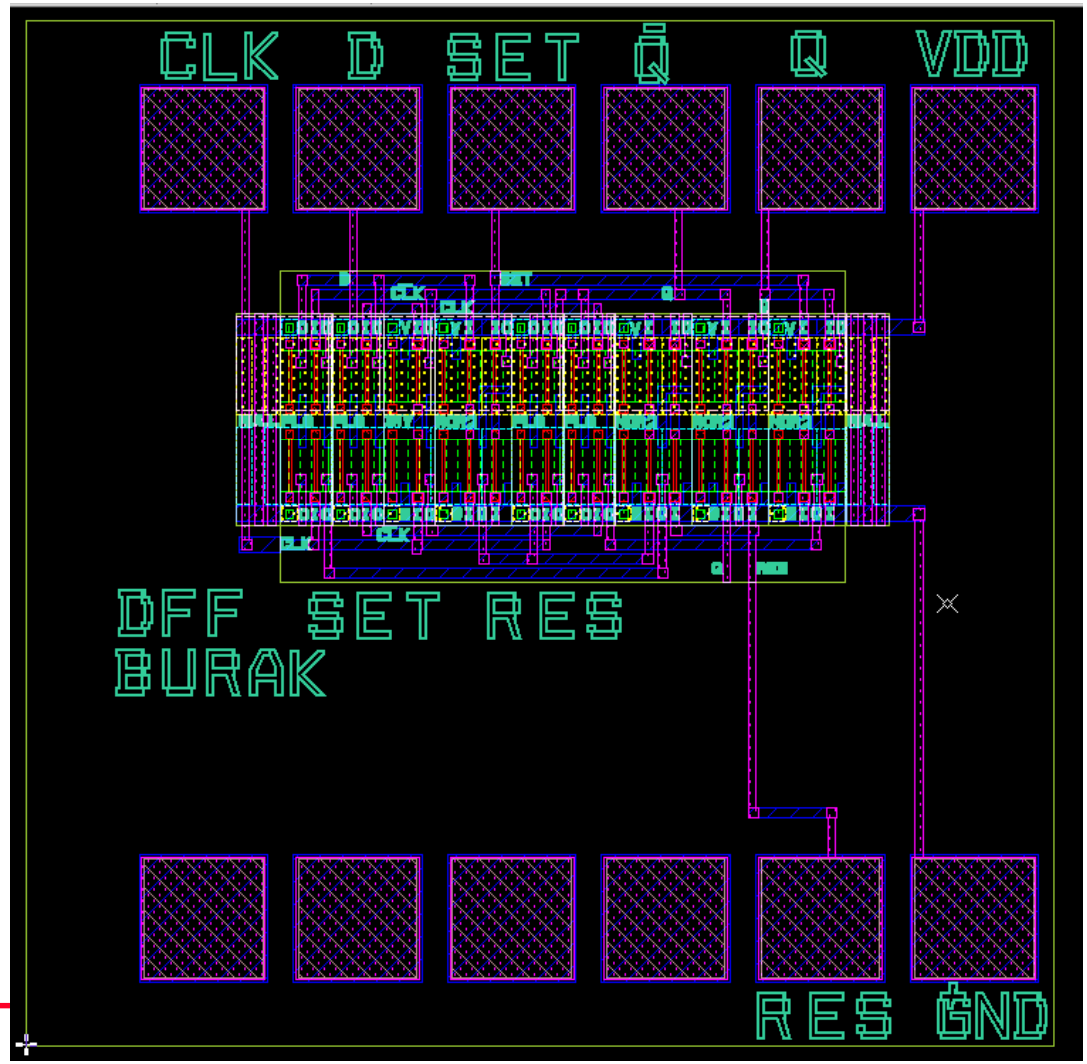




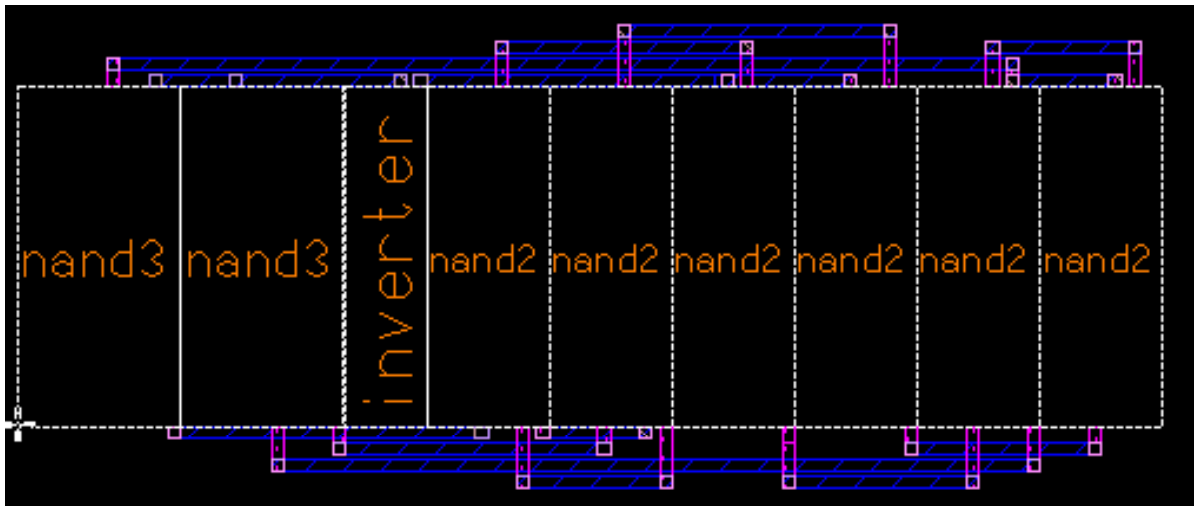
Inputs		Outputs	
D	C	Q^+	$\overline{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\overline{Q}$
X	1	Q	$\overline{Q}$

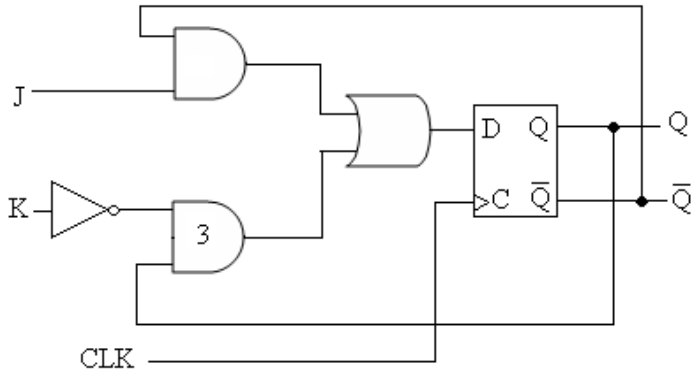


D FLIP FLOP WITH SET AND RESET

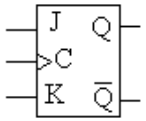


JK FLIP FLOP





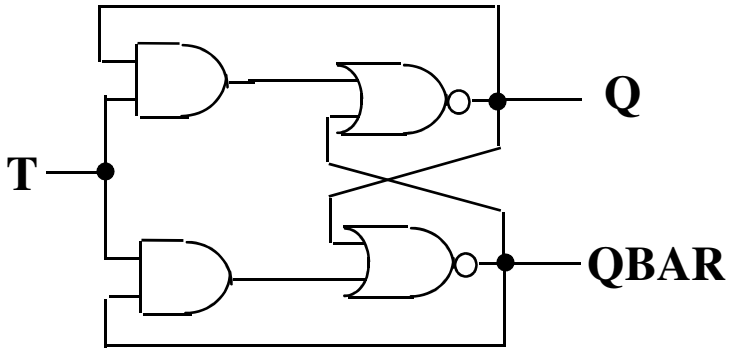
Positive Edge Triggered JK FF



Inputs			Outputs	
J	K	C	Q^+	$\overline{Q^+}$
0	0	↑	Q	$\overline{Q}$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\overline{Q}$	Q
X	X	0	Q	$\overline{Q}$
X	X	1	Q	Q

T-TYPE FILP-FLOP

TOGGEL FLIP FLOP

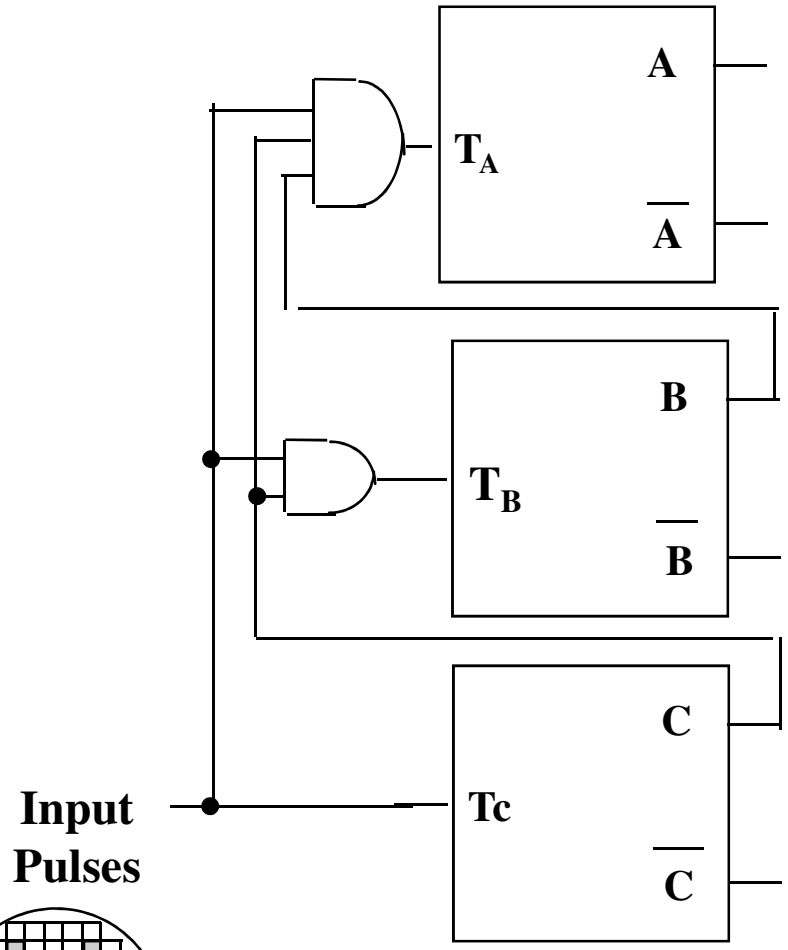


Q: Toggles High and Low with Each Input

T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

T Flip Flop is a JK FF
With J and K connected
together and labeled T

BINARY COUNTER USING T TYPE FLIP FLOPS



State Table for Binary Counter

Present State			Next State			F-F Inputs		
A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

TOGGEL FLIP FLOP

BC \ A	0	1
00	0	0
01	0	0
11	1	1
10	0	0

T_A

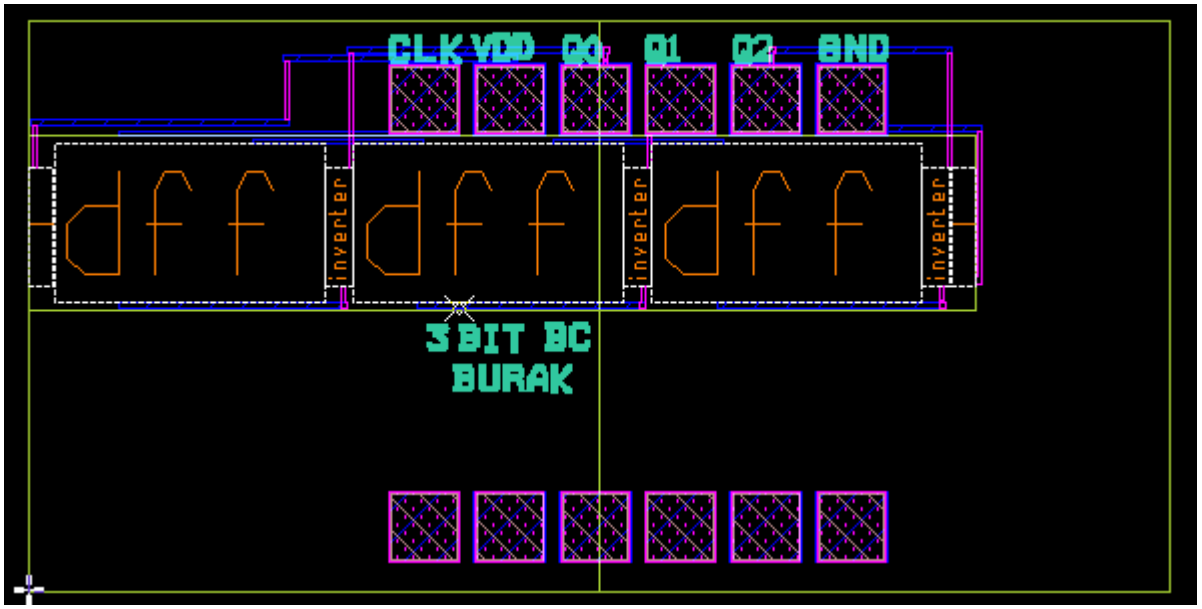
BC \ A	0	1
00	0	0
01	1	1
11	1	1
10	0	0

T_B

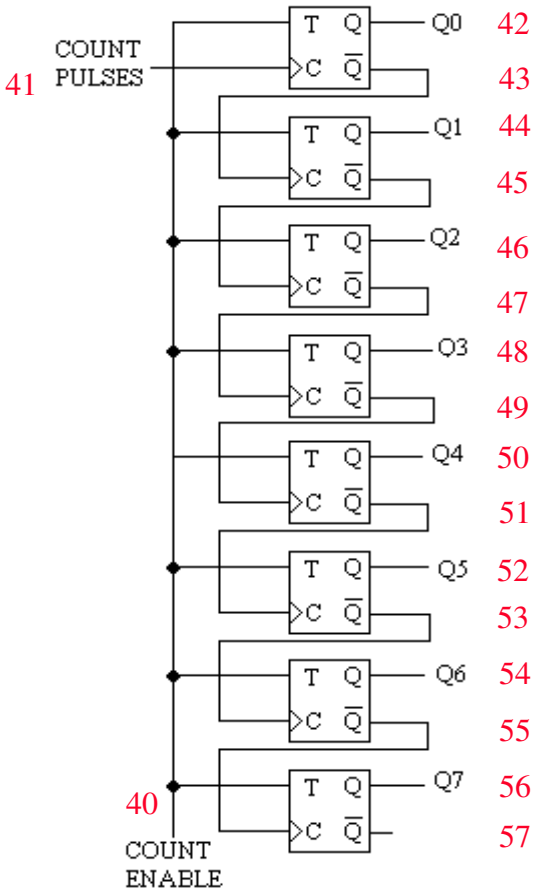
BC \ A	0	1
00	1	1
01	1	1
11	1	1
10	1	1

T_C

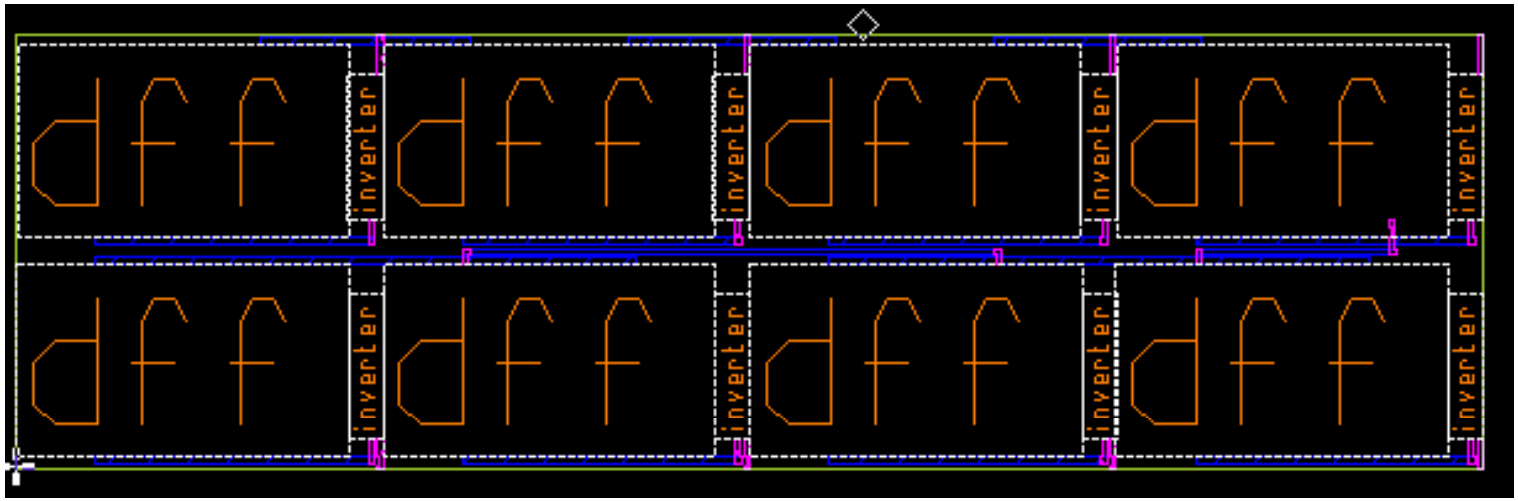
3-BIT BINARY COUNTER WITH D FLIP FLOPS

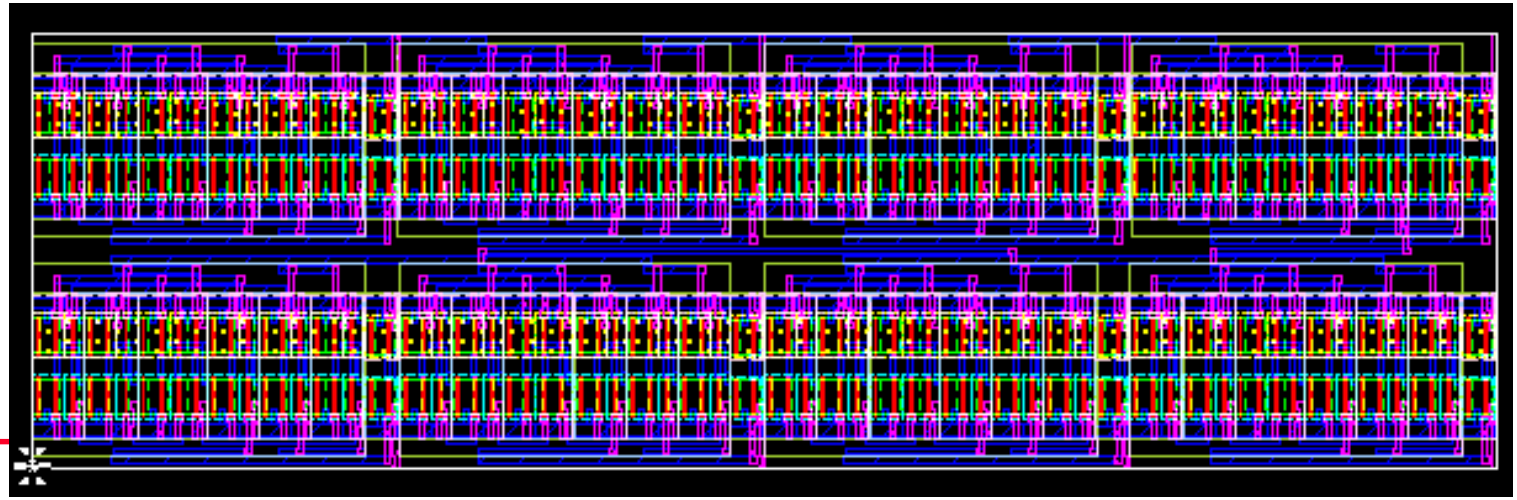


8-BIT BINARY COUNTER

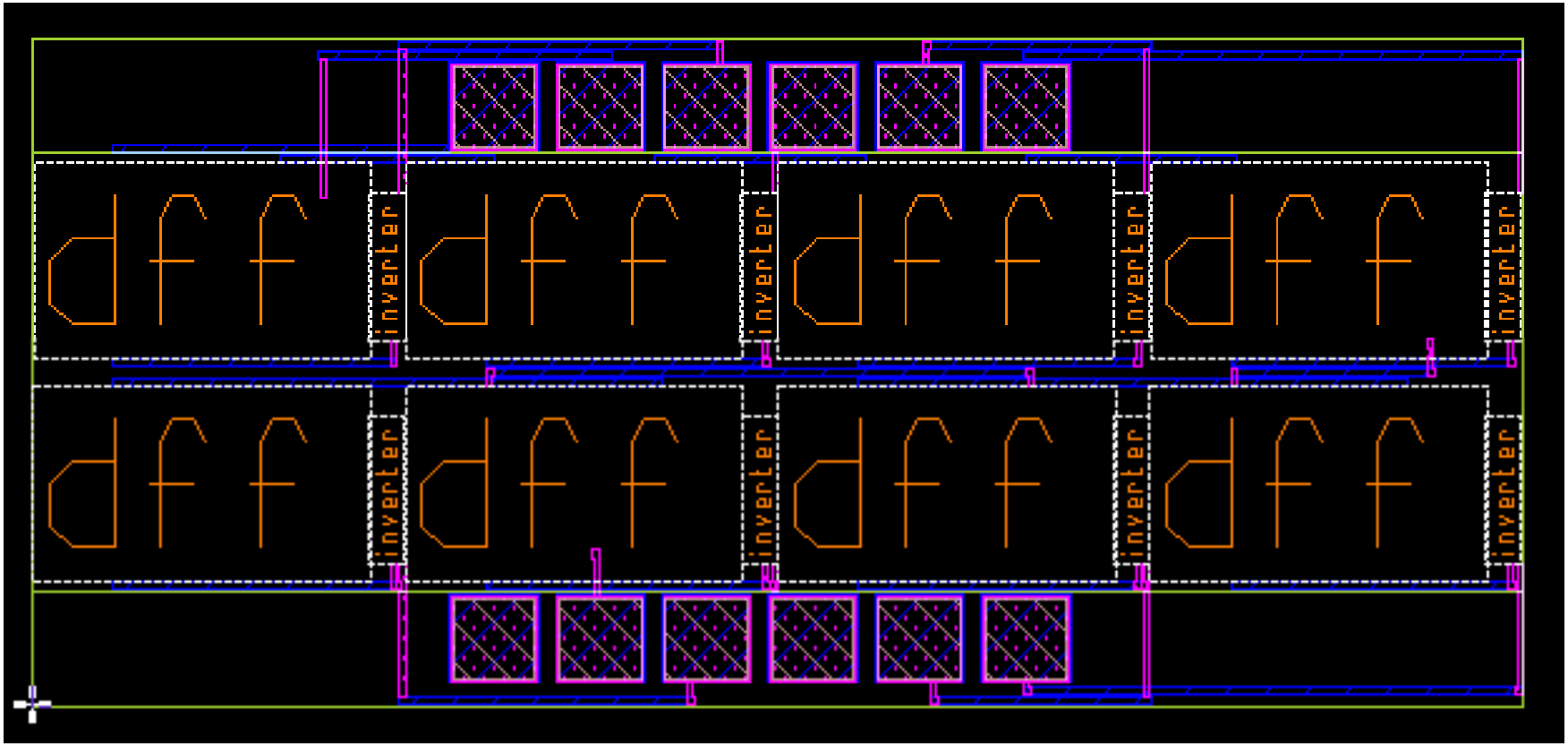


8-BIT BINARY COUNTER



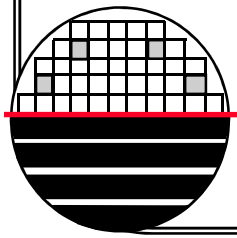


8-BIT BINARY COUNTER WITH PADS

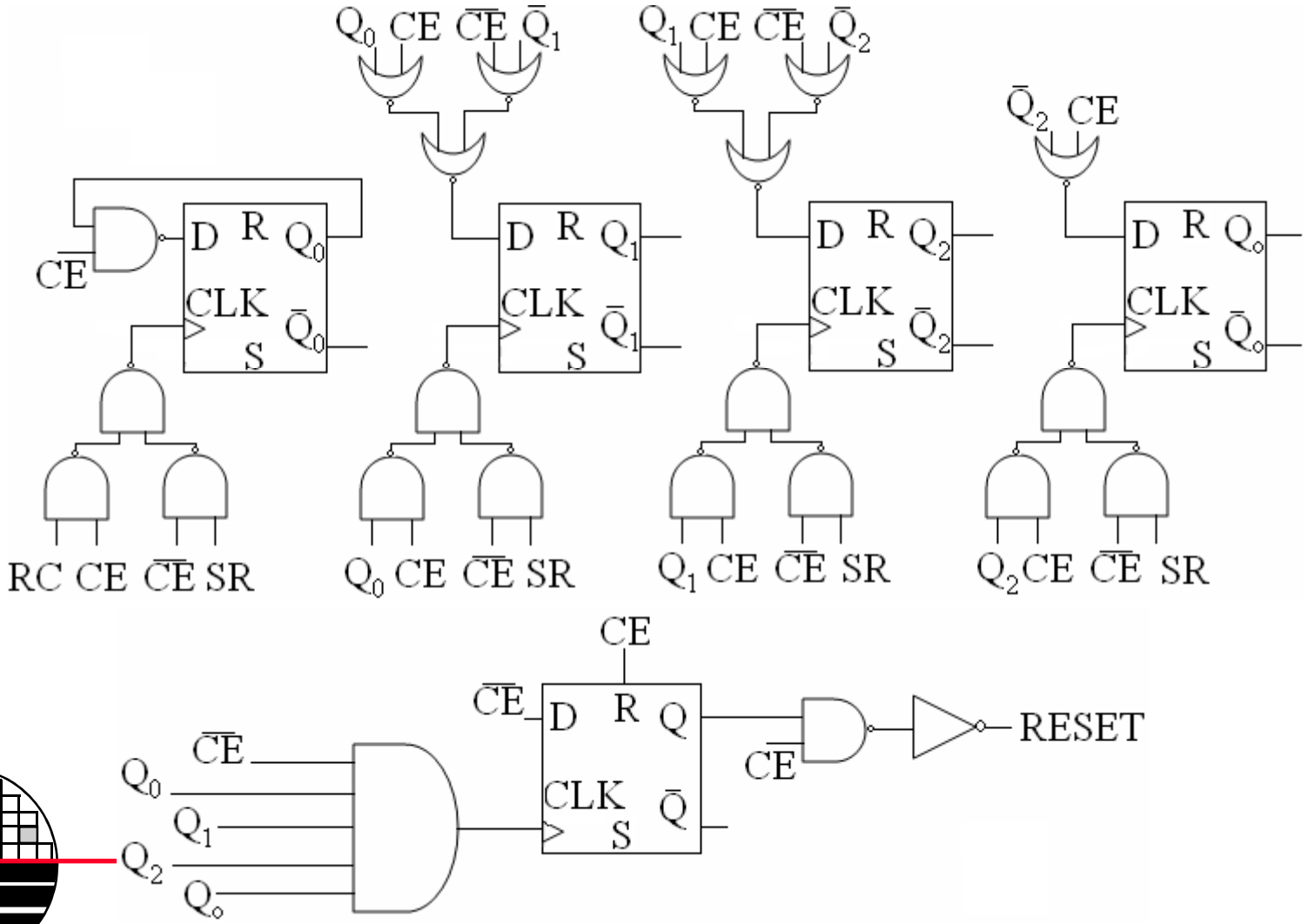


MACROCELLS

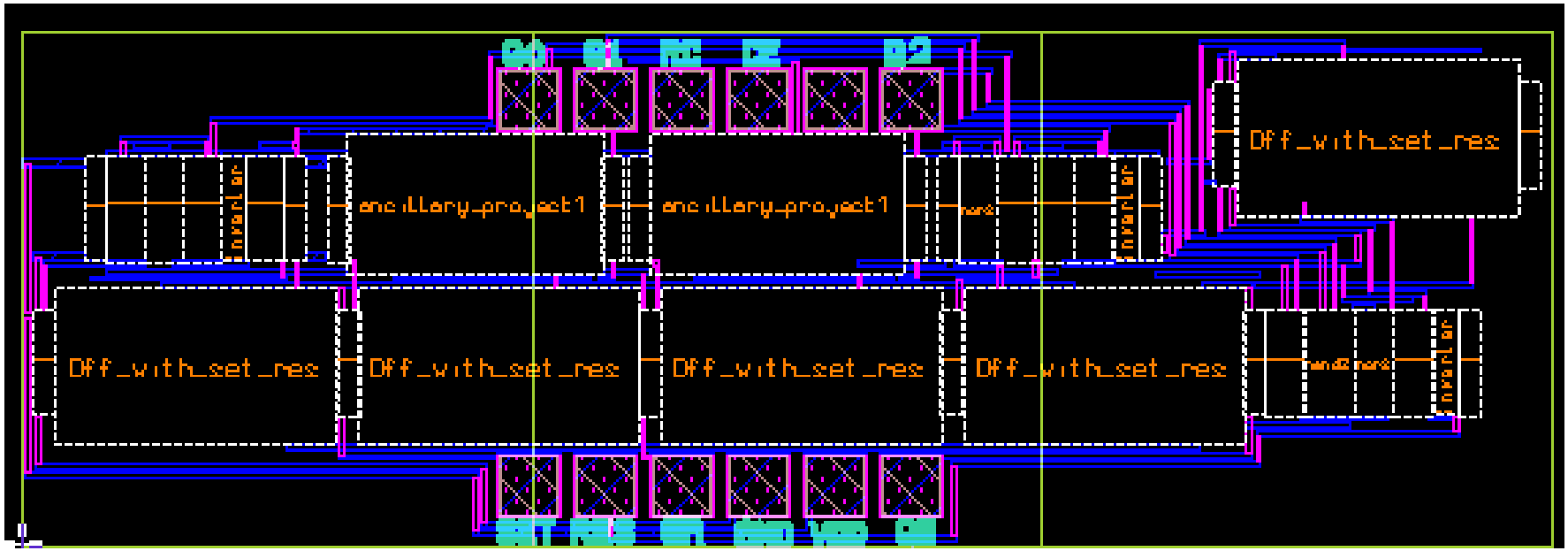
3-Bit Binary Counter / Shifter
8-Bit Binary Counter / Shifter
SRAM
Microcontroller
Etc.



ADDITIONAL CIRCUITRY TO RESET, SHIFT, COUNT

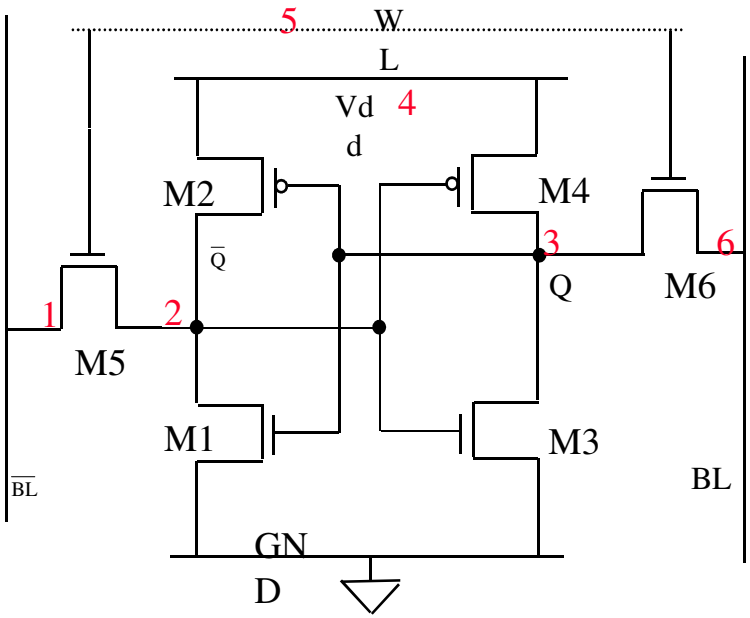


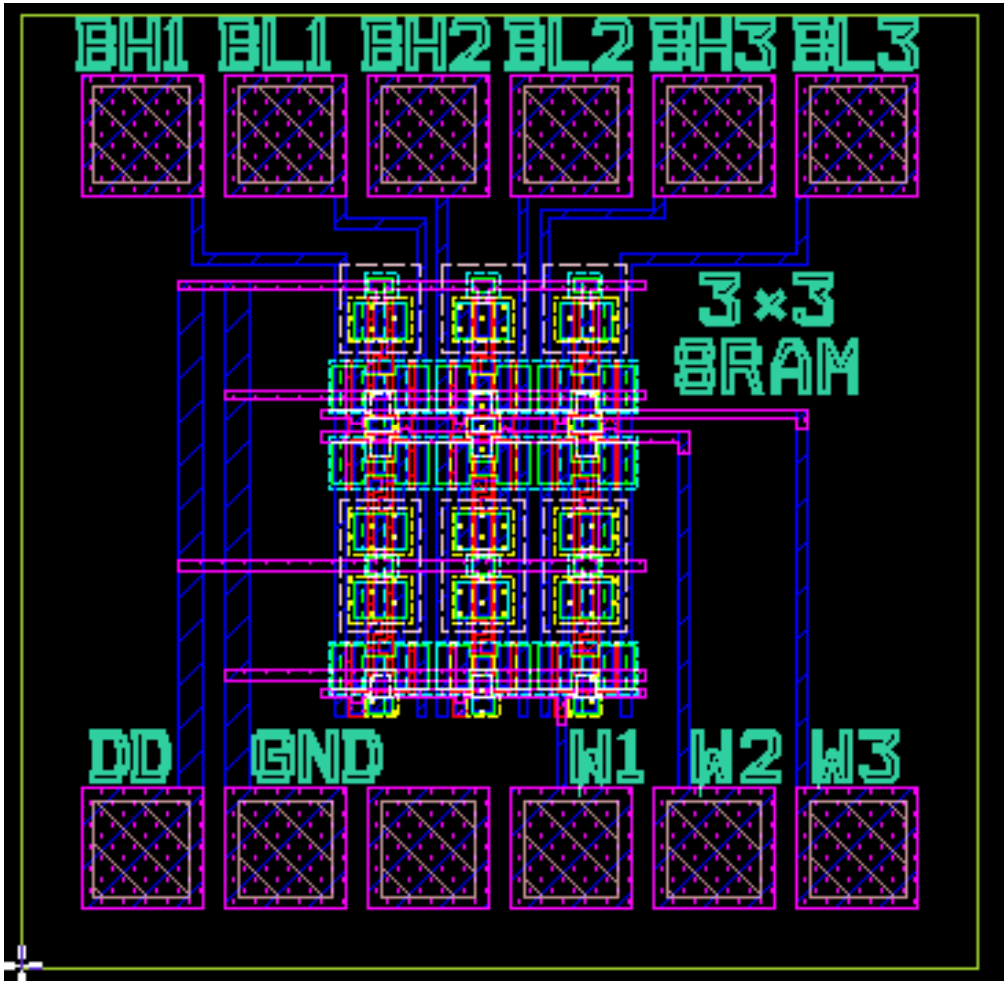
3-BIT BINARY COUNTER/SHIFT REGISTER



Binary Counter
Serial Output
Asynchronous Reset
Count Up Enable
Shift Out Clock Input
Count Up Clock Input
Start Bit and Stop Bit

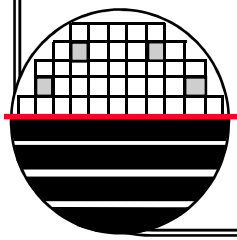
SRAM


5
W
L
Vd
d
4
M2
M4
3
6
Q
M6
1
2
M5
M1
M3
BL
GN
D


BH1
BL1
BH2
BL2
BH3
BL3
3×3
SRAM
DD
GND
W1
W2
W3

ANALOG AND MIXED MODE CIRCUITS

Operational Amplifier
Inverter with Hysteresis
RC Oscillator
Two Phase Clock
Analog Switches
Voltage Doubler, Tripler
Analog Multiplexer
Comparator with Hysteresis
A-to-D
D-to-A
OTA, Biquad Filter, Elliptic Filter
Programmable Binary Weighted Resistors



SPICE PARAMETERS FOR SUB-CMOS PROCESS

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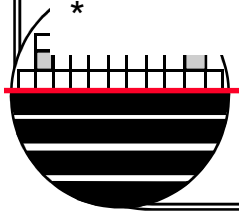
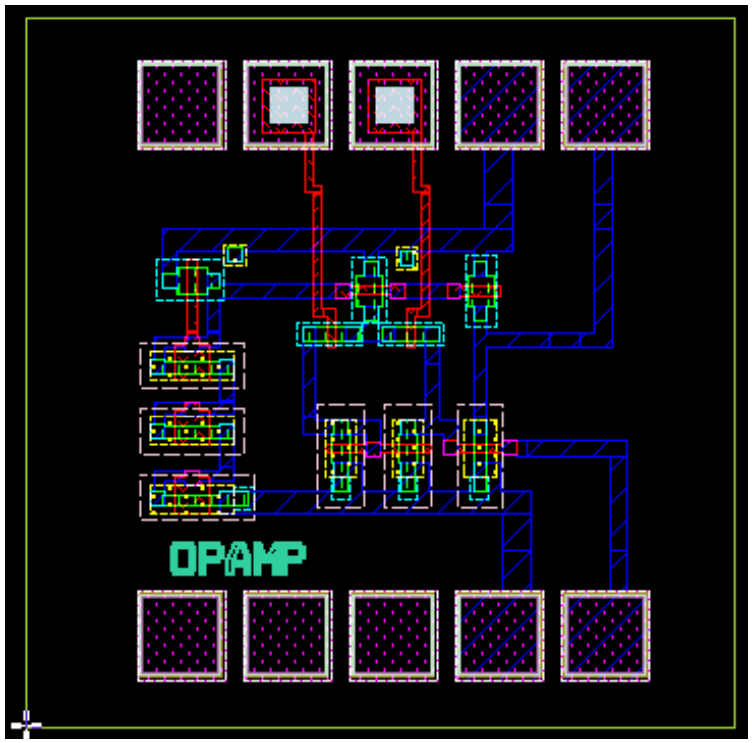
*This file is called: RIT_MICROE_MODELS.TXT
*
*1-15-2007 FROM DR. FULLER'S SPREADSHEET WITH VT0=0.75
.MODEL RITSUBN49 NMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8 NSS=3E11
+XWREF=2.0E-7 XLREF=2.95E-7 VTH0=0.75 U0= 950 WINT=2.0E-7 LINT=1.84E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGS0=3.4E-10 CGD0=3.4E-10 CGB0=5.75E-10)
*
*1-17-2007 FROM DR. FULLER'S SPREADSHEET WITH VT0=-0.75
.MODEL RITSUBP49 PMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8 NSS=3E11 PCLM=5
+XWREF= 2.0E-7 XLREF=3.61E-7 VTH0=-0.75 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 NGATE=5E20
+CGS0=4.5E-10 CGD0=4.5E-10 CGB0=5.75E-10)
*
```

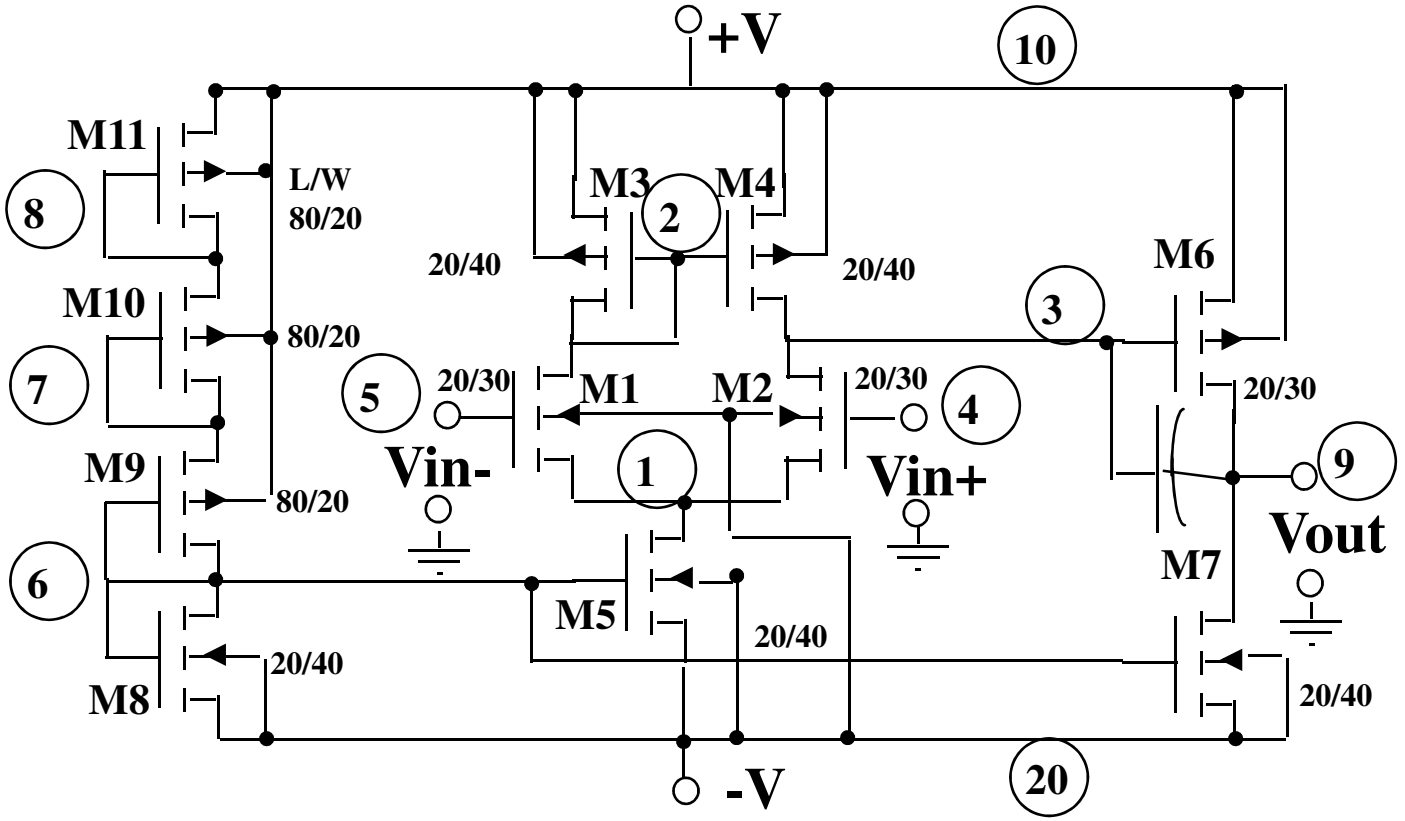


OPERATIONAL AMPLIFIER



Version 1

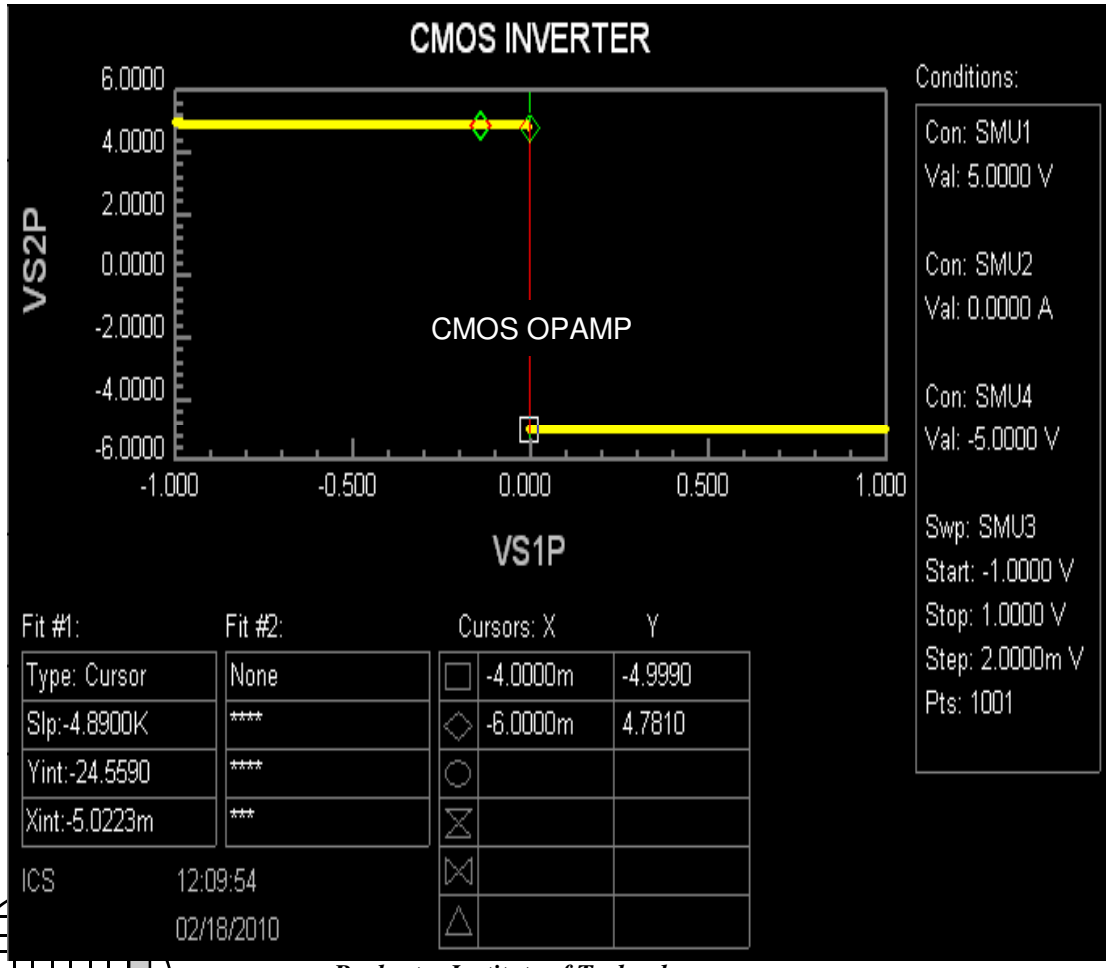
VERSION 1 OPERATIONAL AMPLIFIER

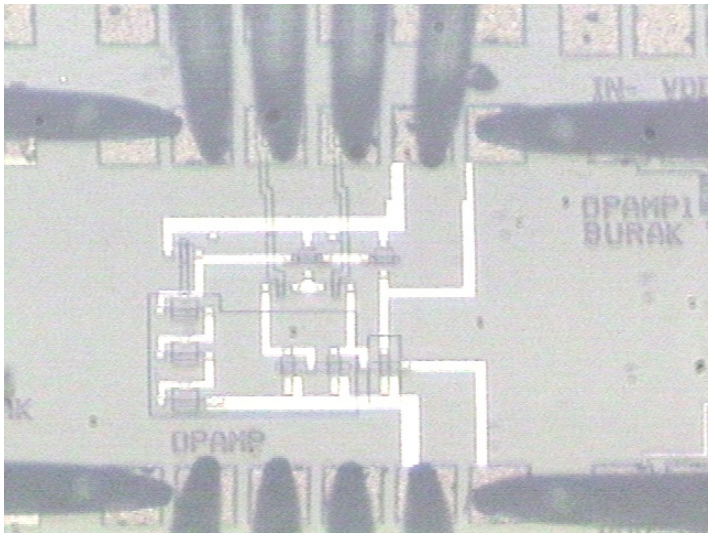


p-well CMOS

dimensions
L/W
(µm/µm)

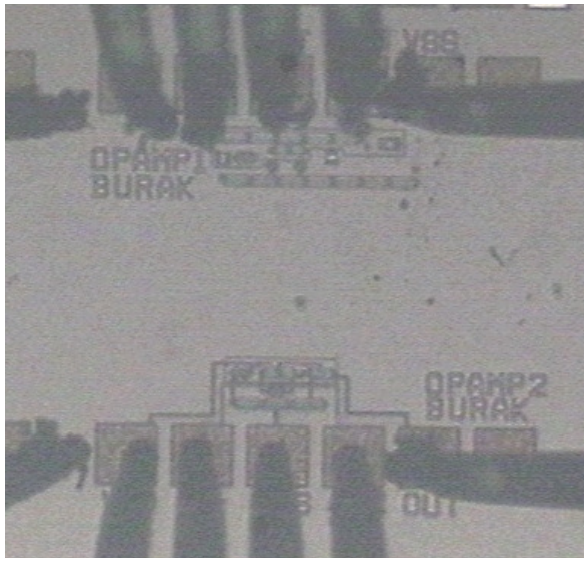
R/C 2/2 OpAmp





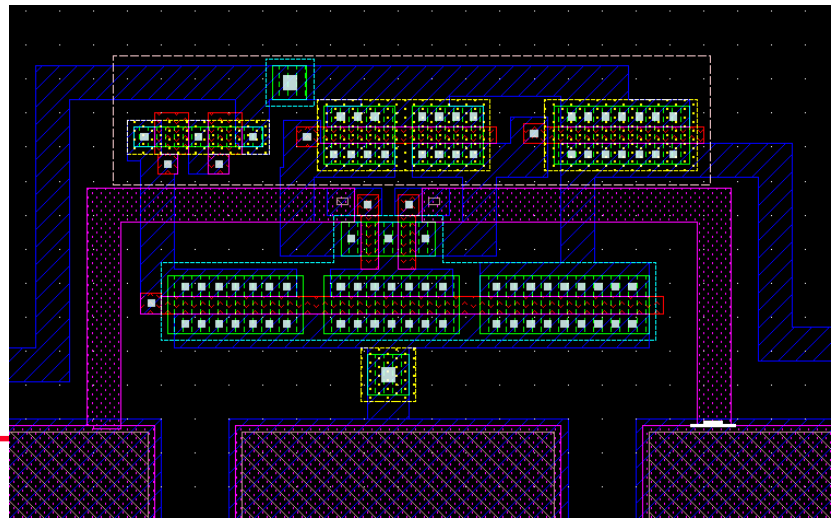
	Op Amp	
Gain	**-4.89k**	
Offset	**0**	**m Volts**
GBW		**Hz**

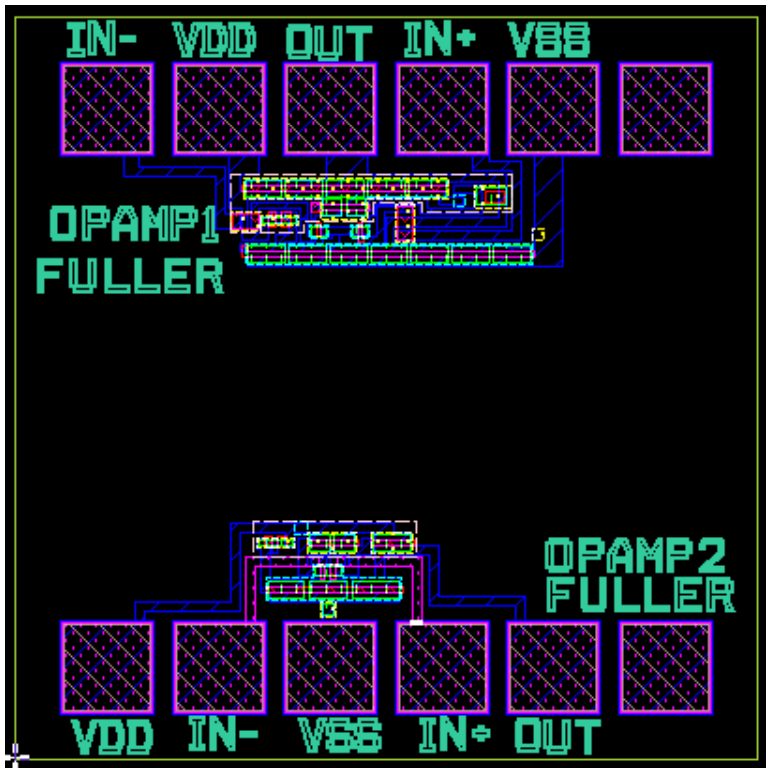
OPAMP 1



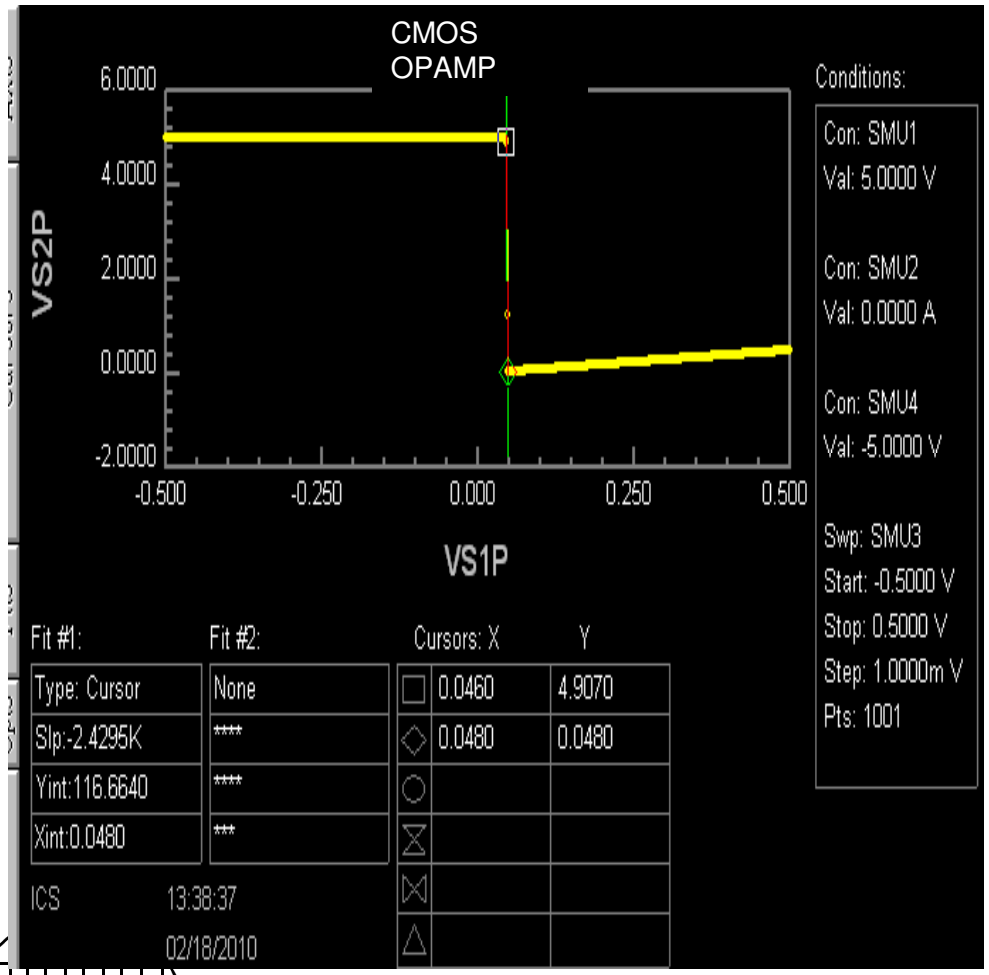
All had missing metal one due to over etch. Metal lines at 3µm.

Redesign with bigger metal lines.



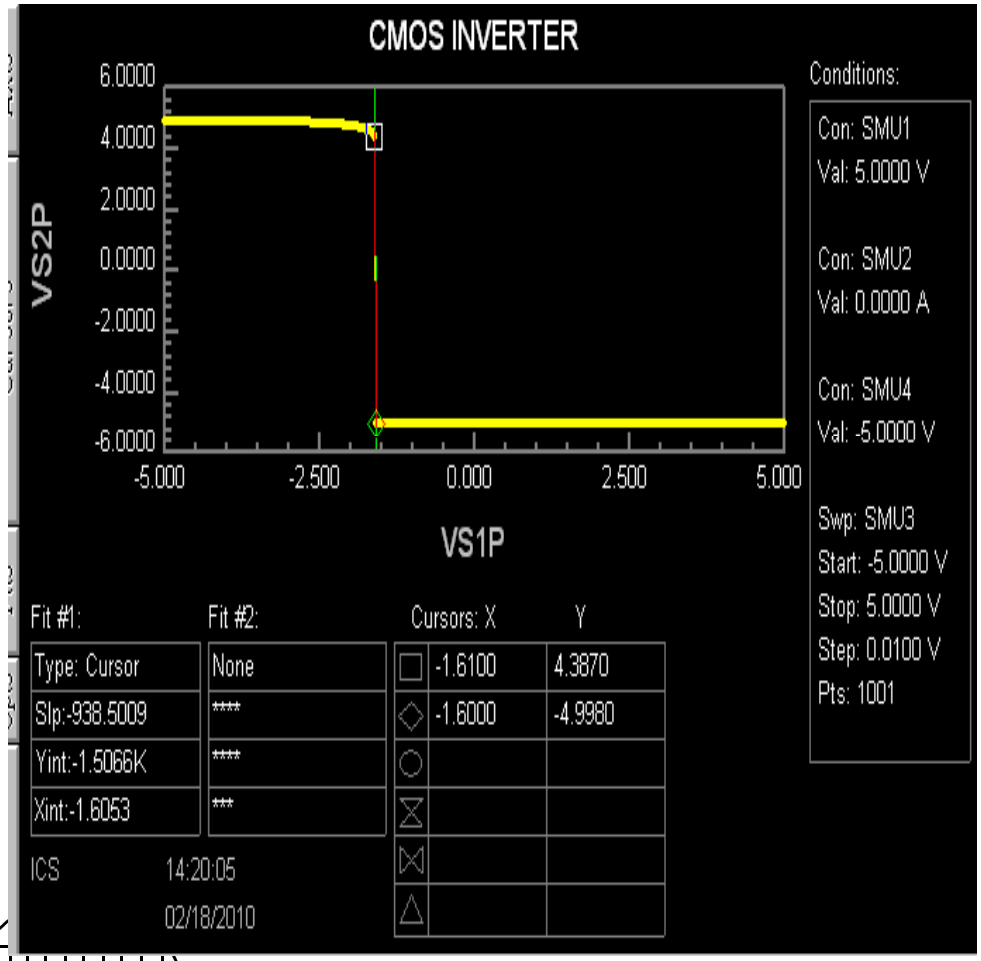


OpAmp: 1 R/C 2/2



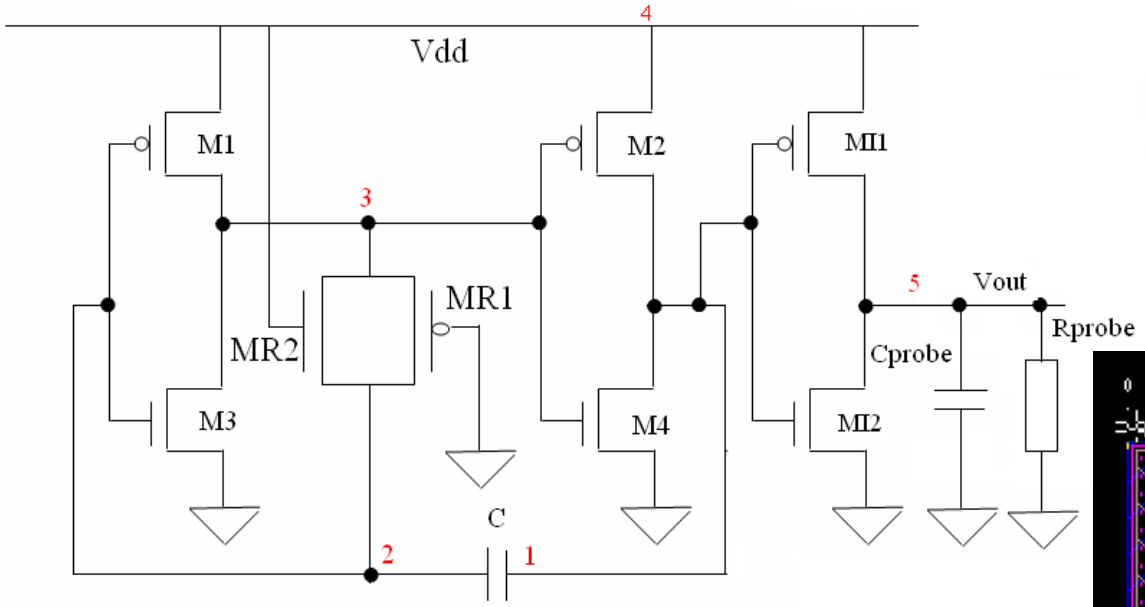
	Op Amp	
Gain	**-2.4k**	
Offset	**47**	**m Volts**
GBW		**Hz**

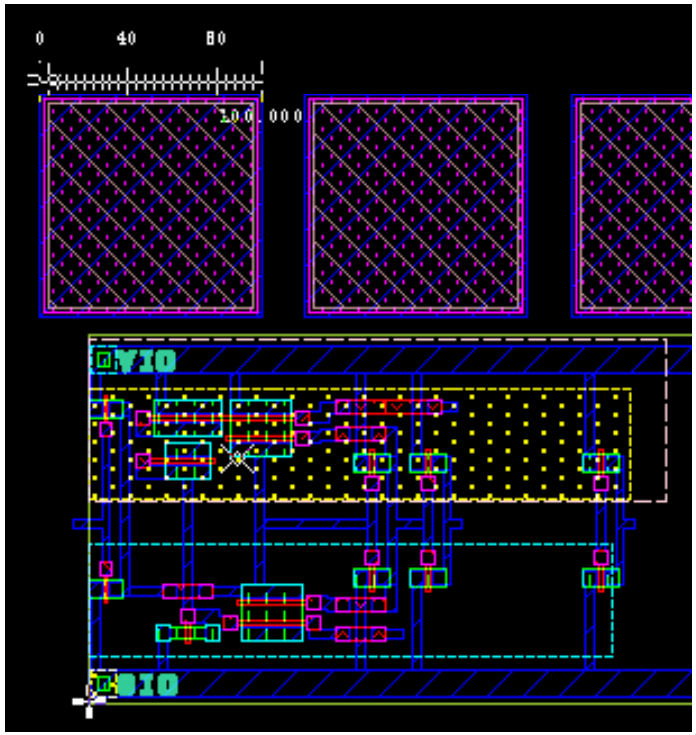
OPAMP 2

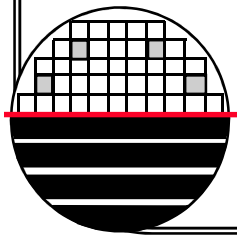


	Op Amp	
Gain	**-939**	
Offset	**-1.6**	**Volts**
GBW		**Hz**

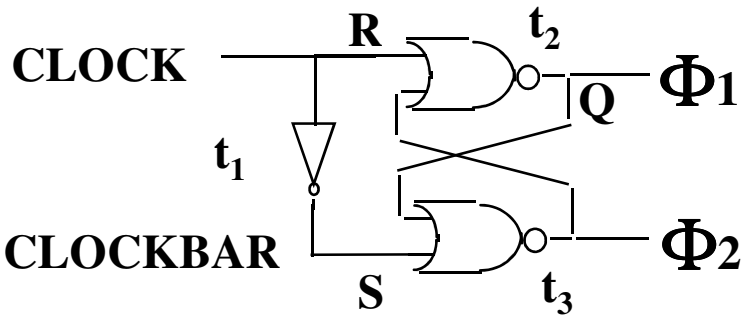
INVERTER WITH HYSTERESIS – RC OSCILLATOR

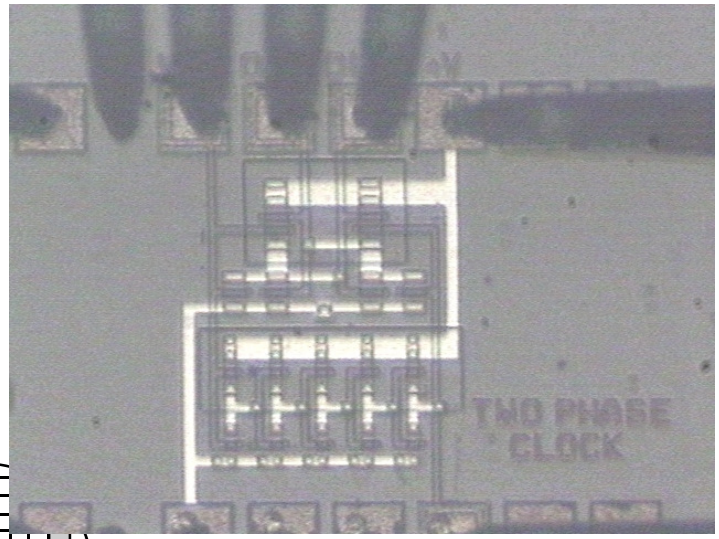


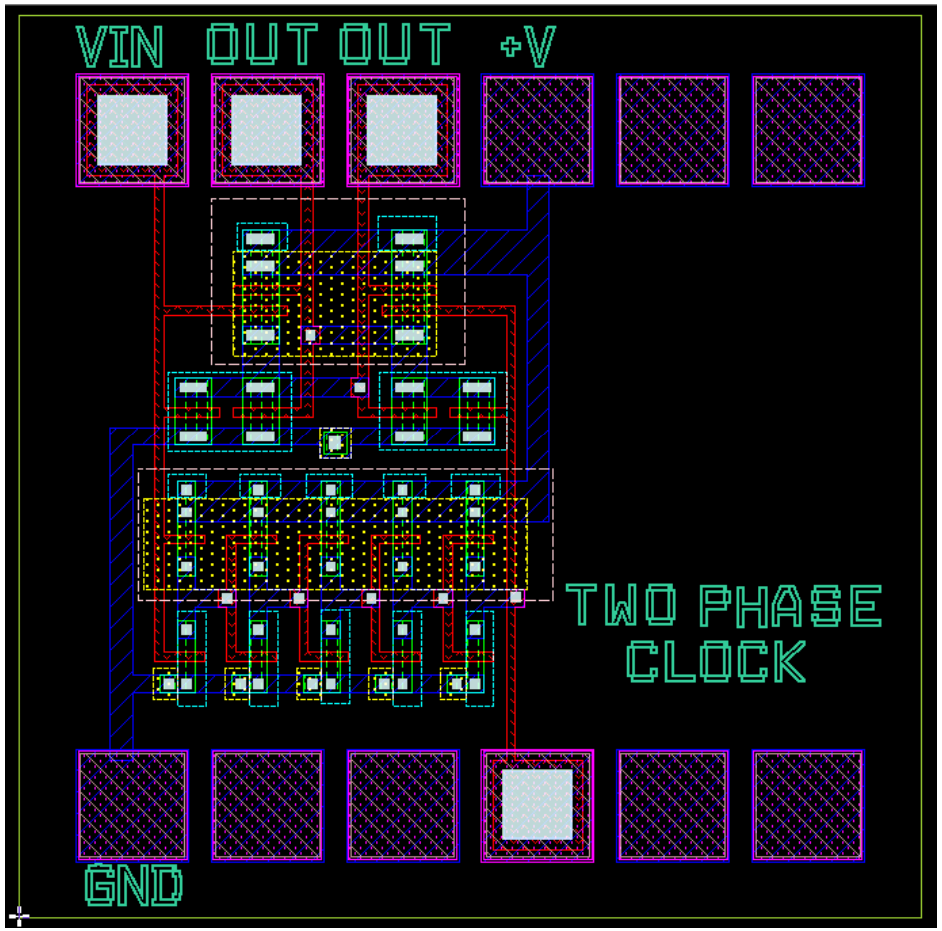




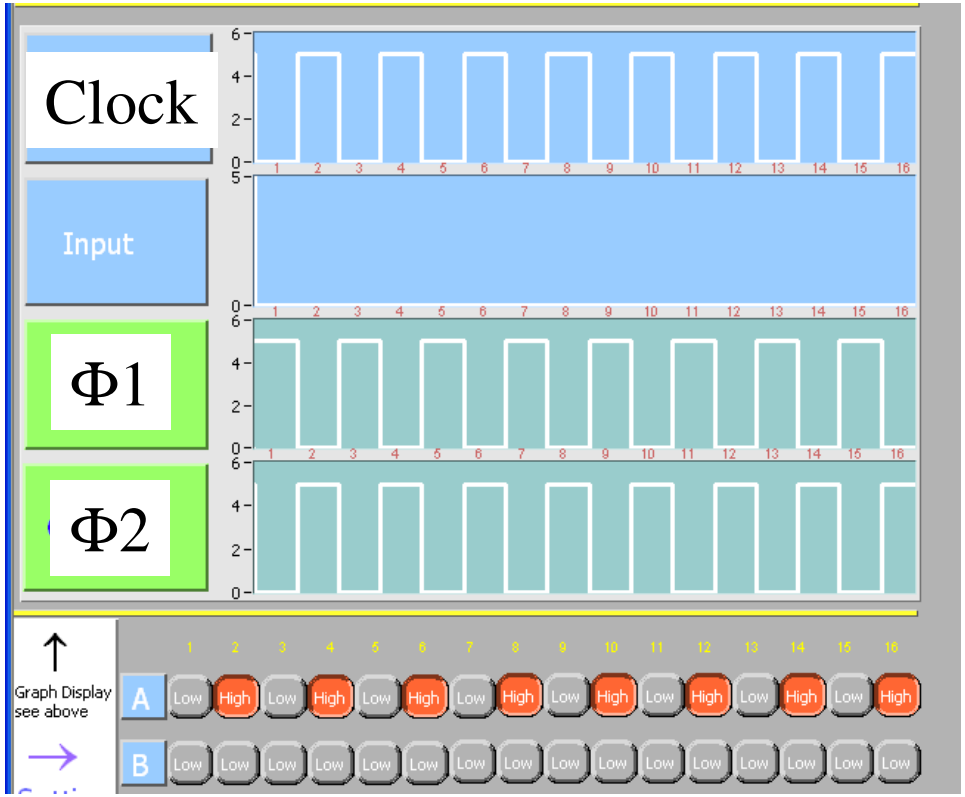
TWO PHASE CLOCK

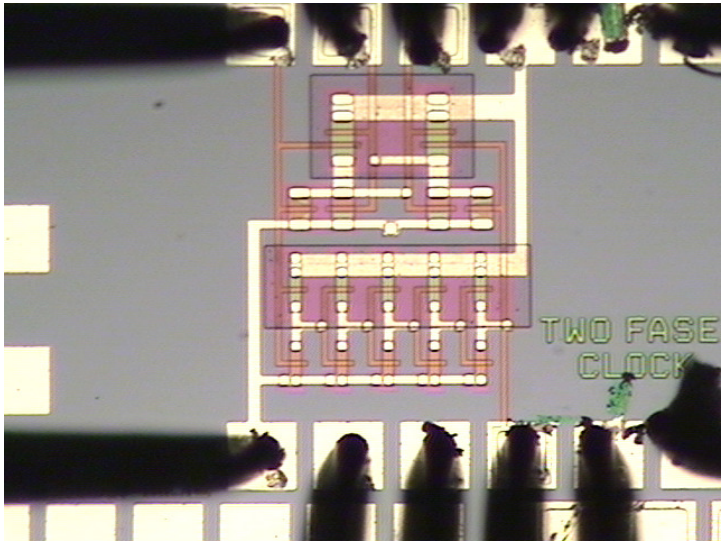


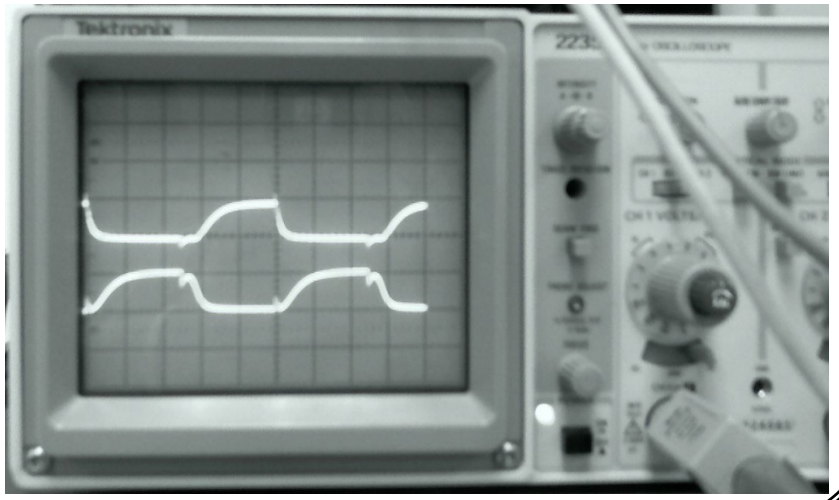




TWO PHASE NON OVERLAPPING CLOCK

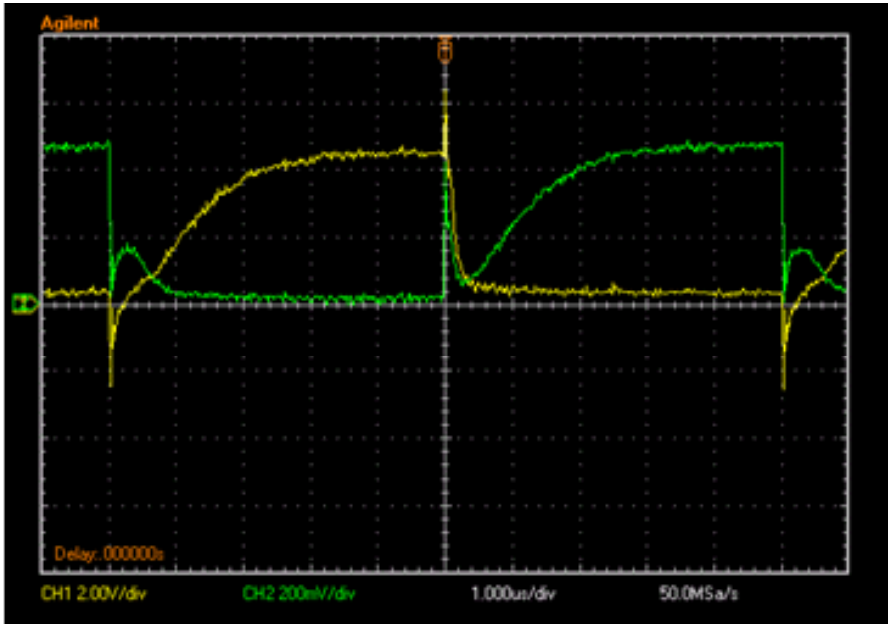


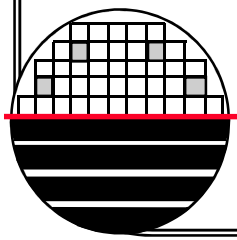




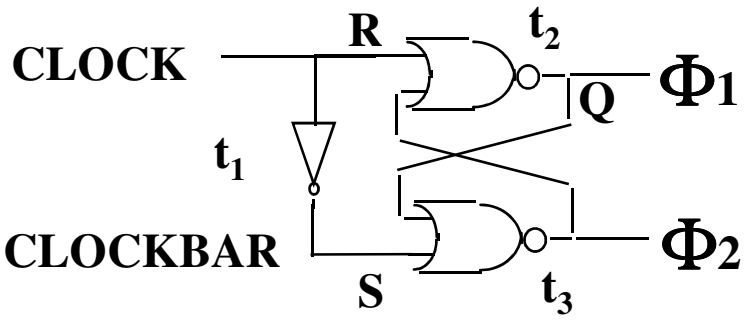
TWO PHASE CLOCK

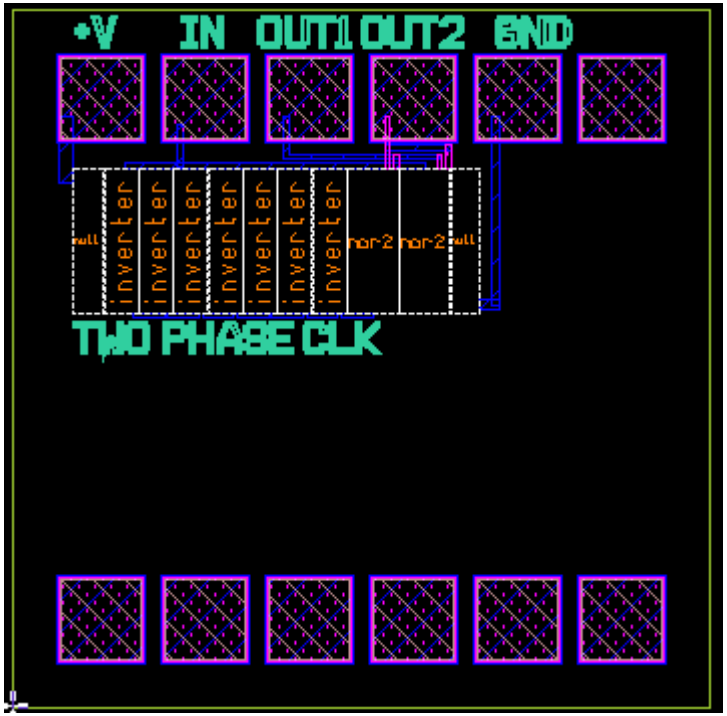
Circuit of previous page at 100Khz

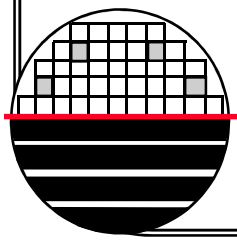




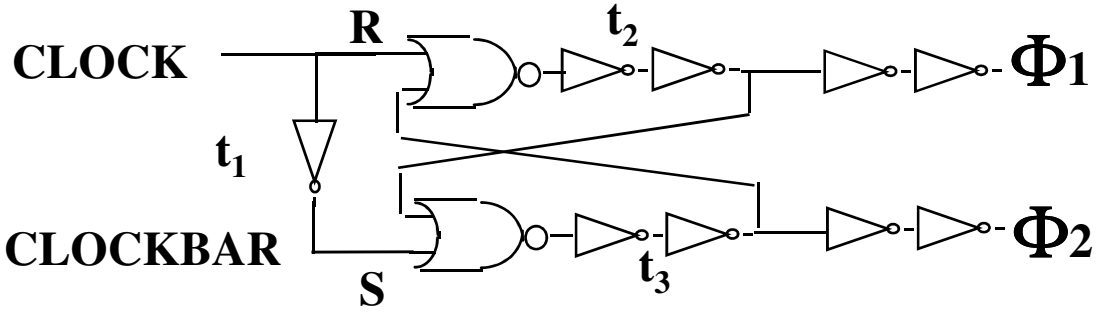
NEW TWO PHASE CLOCK

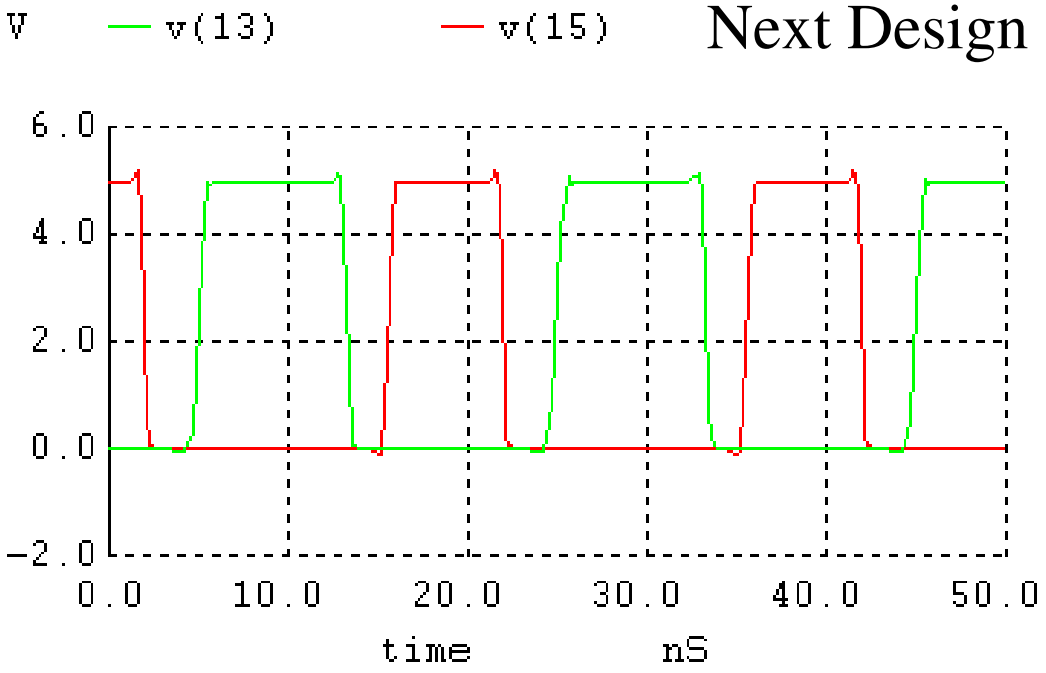






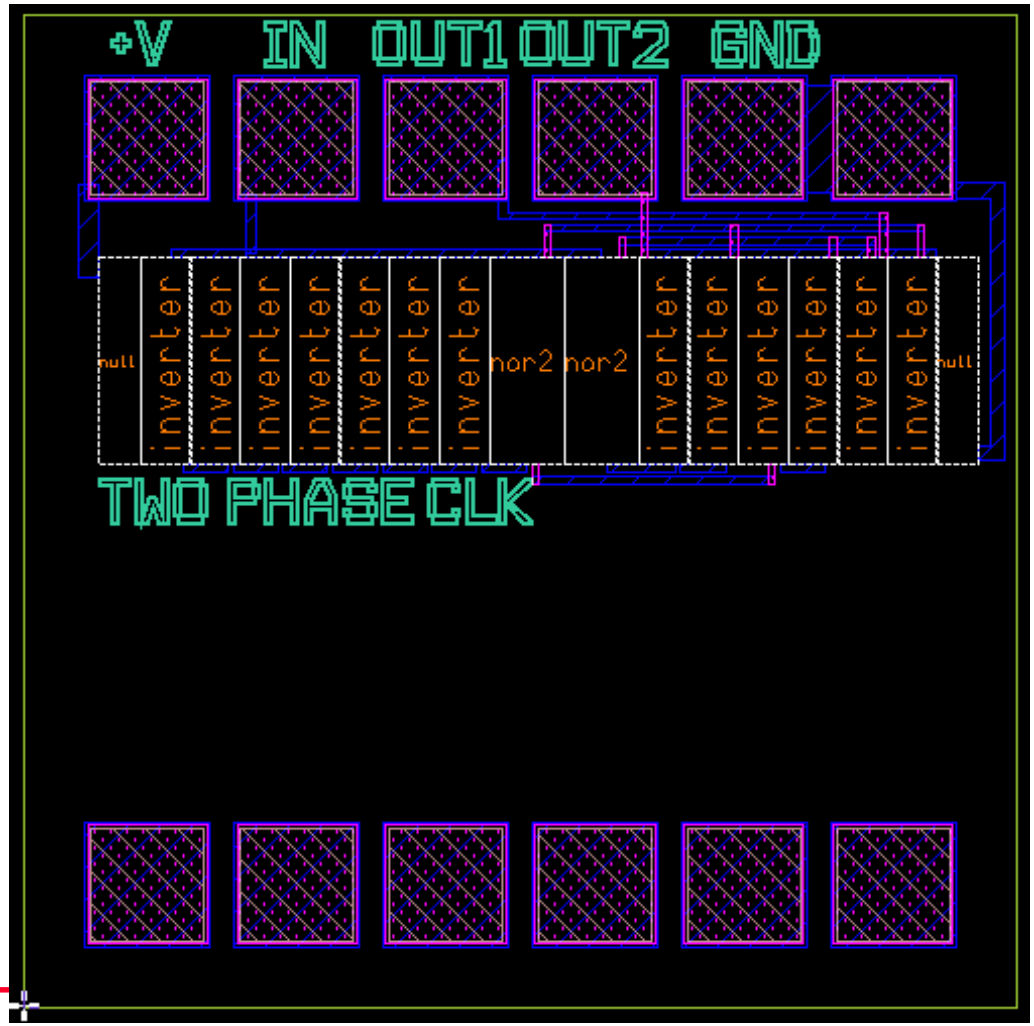
WINSPICE SIMULATION FOR VERSION TWO + BUFFERS



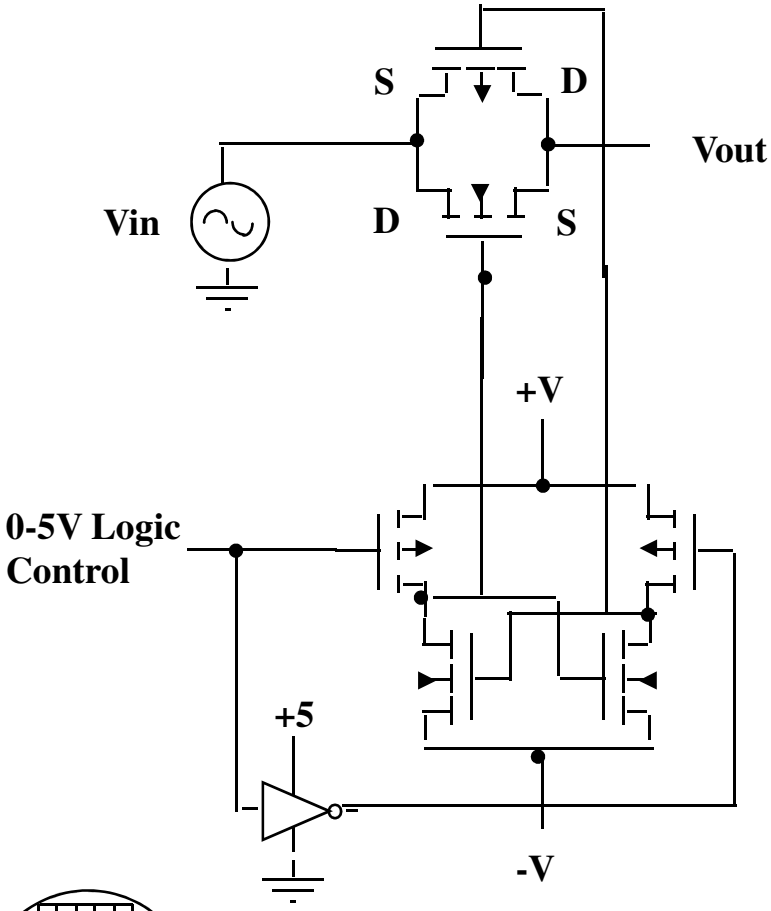


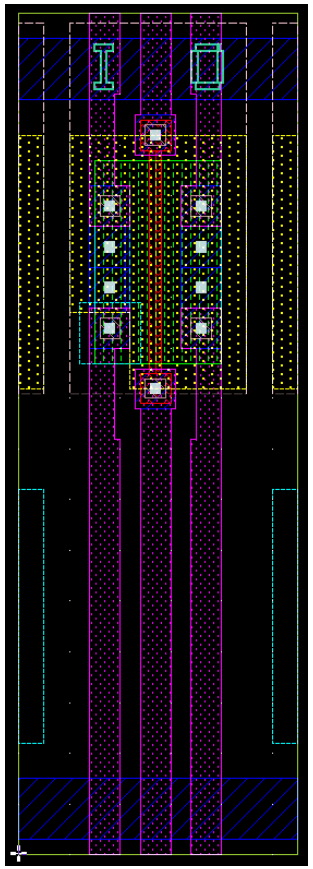
Next Design add buffers

TWO PHASE CLOCK WITH BUFFERS

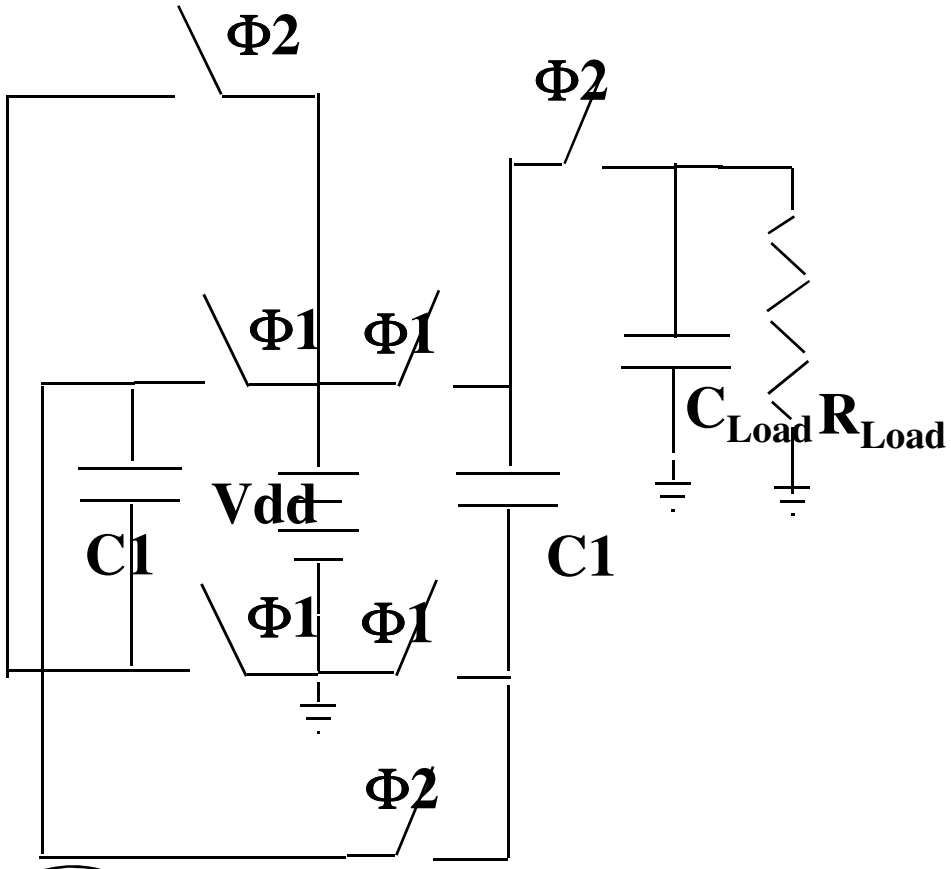


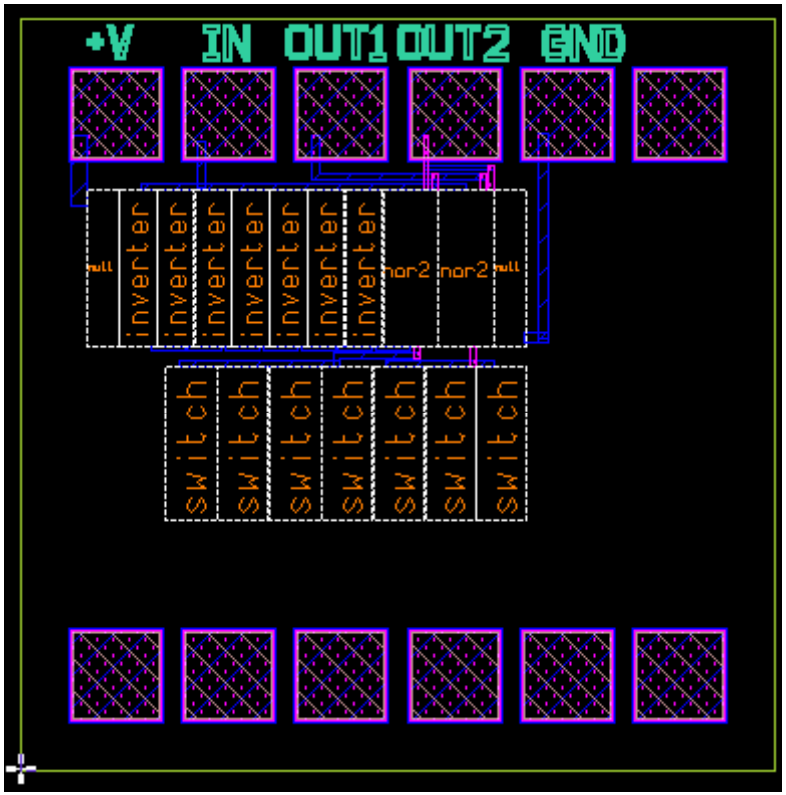
ANALOG SWITCH





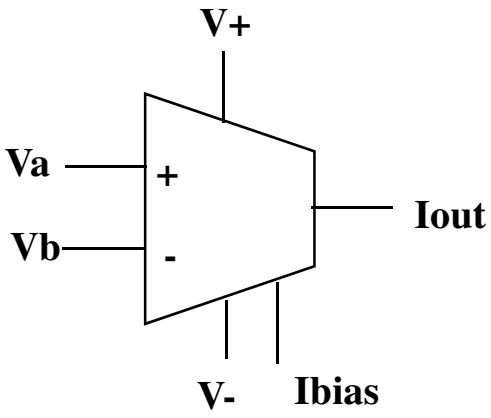
VOLTAGE DOUBLER / TRIPLER

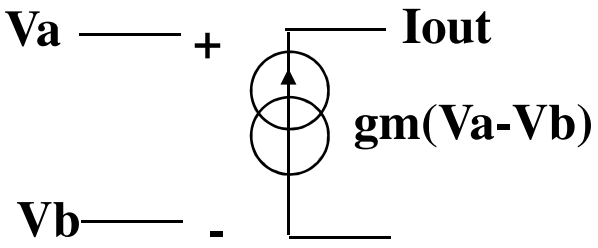




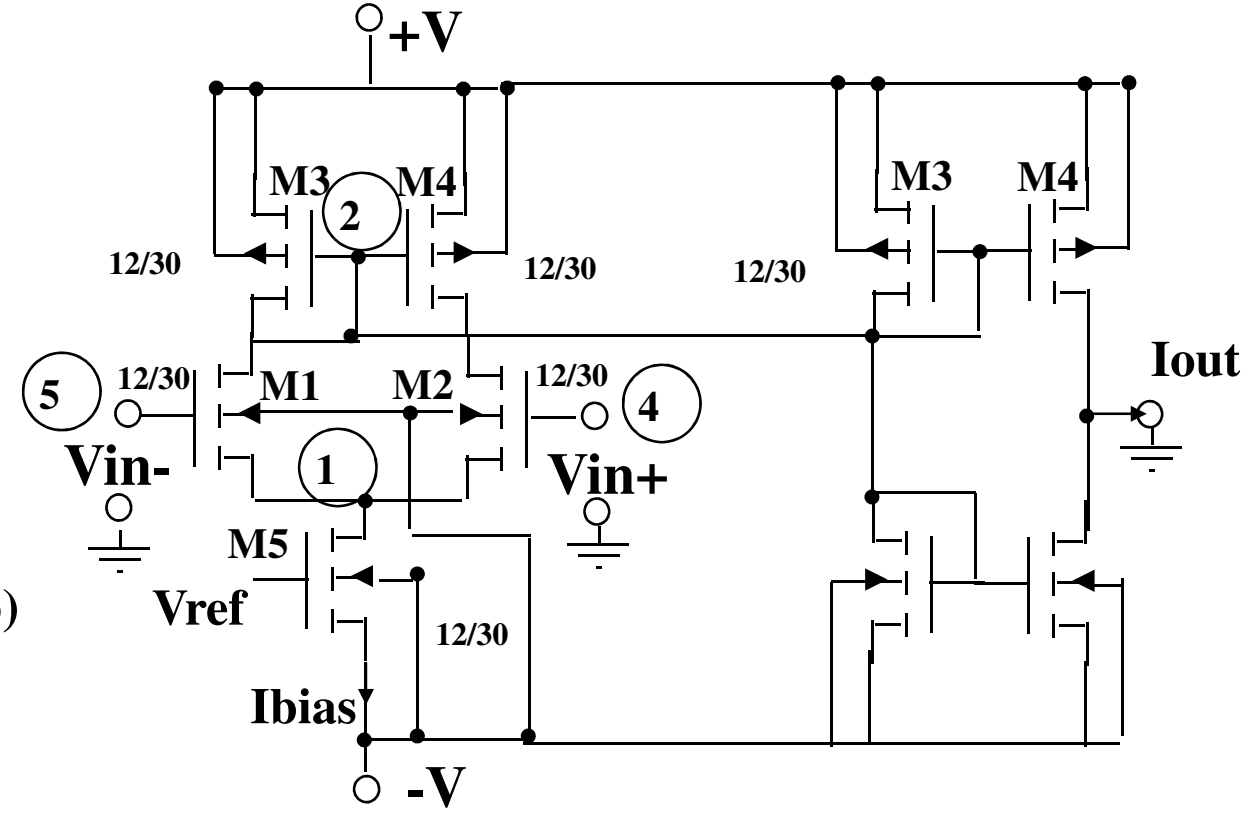
Voltage Tripler

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER





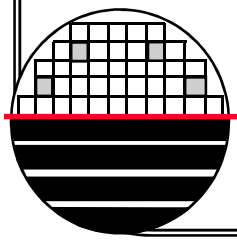
CMOS Realization



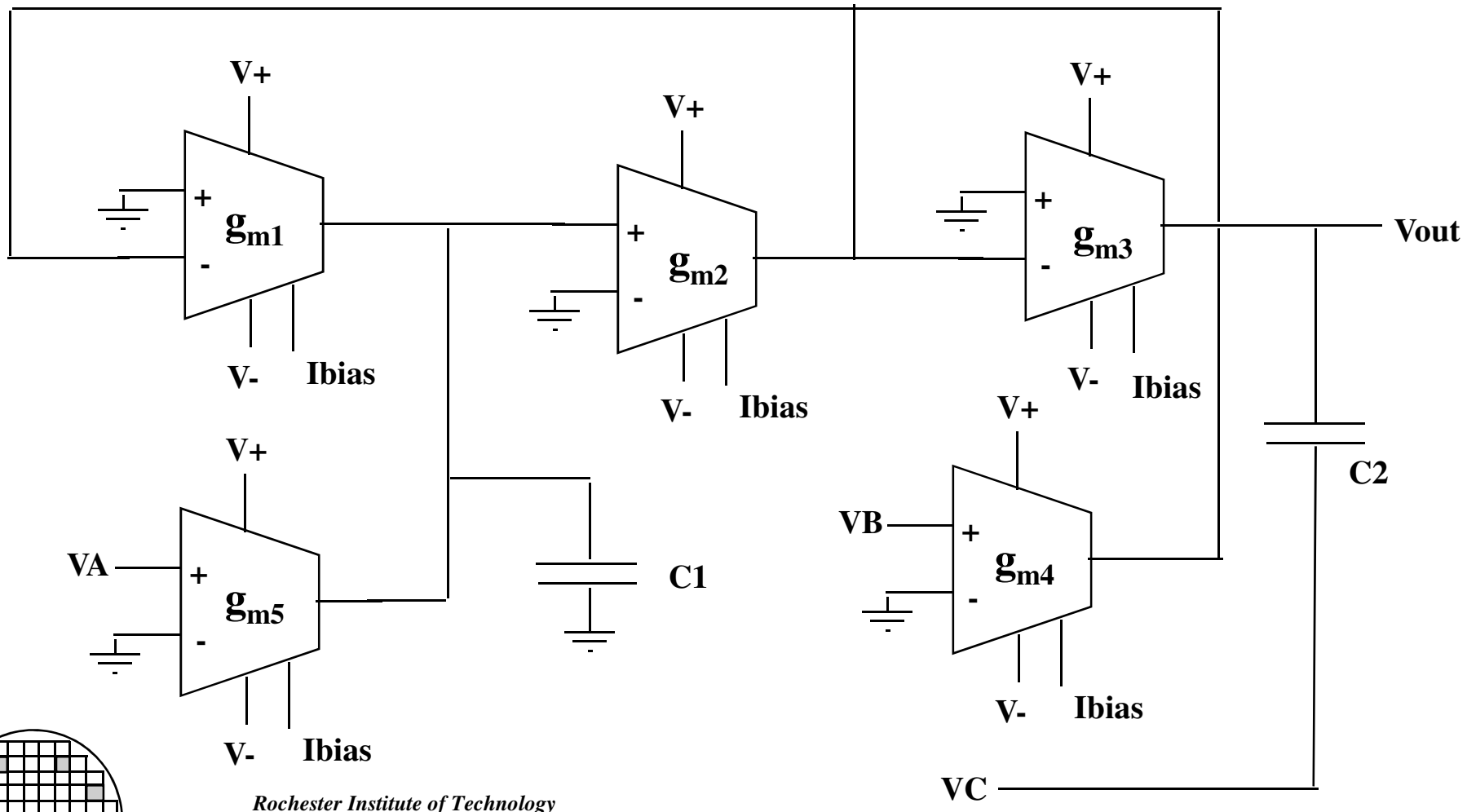
Note: gm is set by Ibias

SPICE ANALYSIS OF CIRCUIT ON PREVIOUS PAGE

Homework Assignment



BIQUAD FILTER



BIQUAD FILTER

$$V_{out} = (s^2C_1C_2V_c + s\,C_1\,g_{m4}\,V_b + g_{m2}\,g_{m5}\,V_a)/(s^2C_1C_2 + sC_1g_{m3} + g_{m2}g_{m1})$$

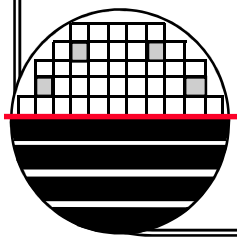
This filter can be used as a low-pass, high-pass, bandpass, bandrejection and all pass filter. Depending on the C and gm values a Butterworth, Chebyshev, Elliptic or any other configuration can be achieved

For example: let Vc=Vb=0 and Va=Vin, also let all g_m be equal, then

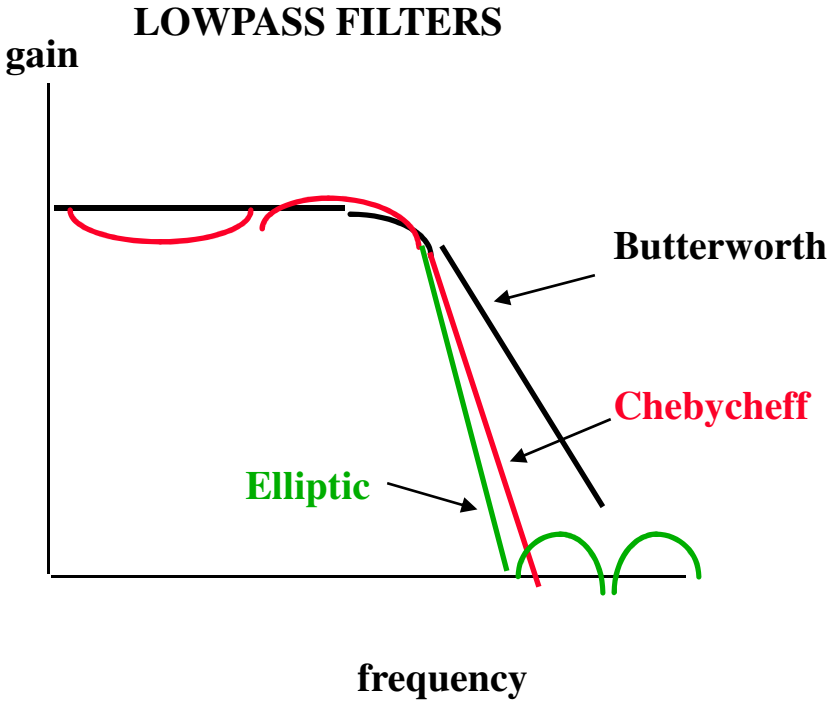
$$Vout = Vin / (s^2C_1C_2/ g_mg_m + sC_1/g_m + 1)$$

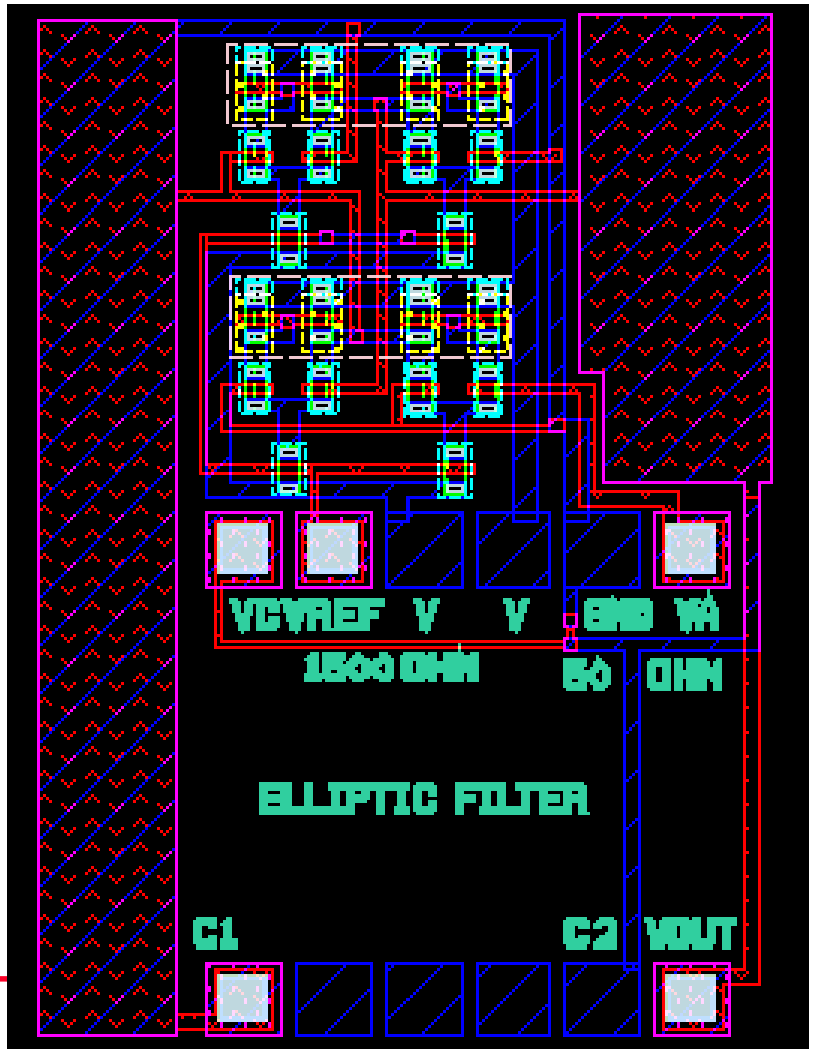
which is a second order low pass filter with corner frequency at

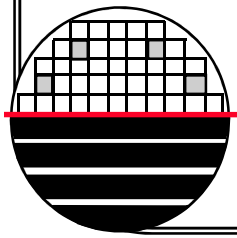
$$\omega_c = g_m / \sqrt{C_1C_2} \quad \text{and } Q = \sqrt{C_2/C_1}$$



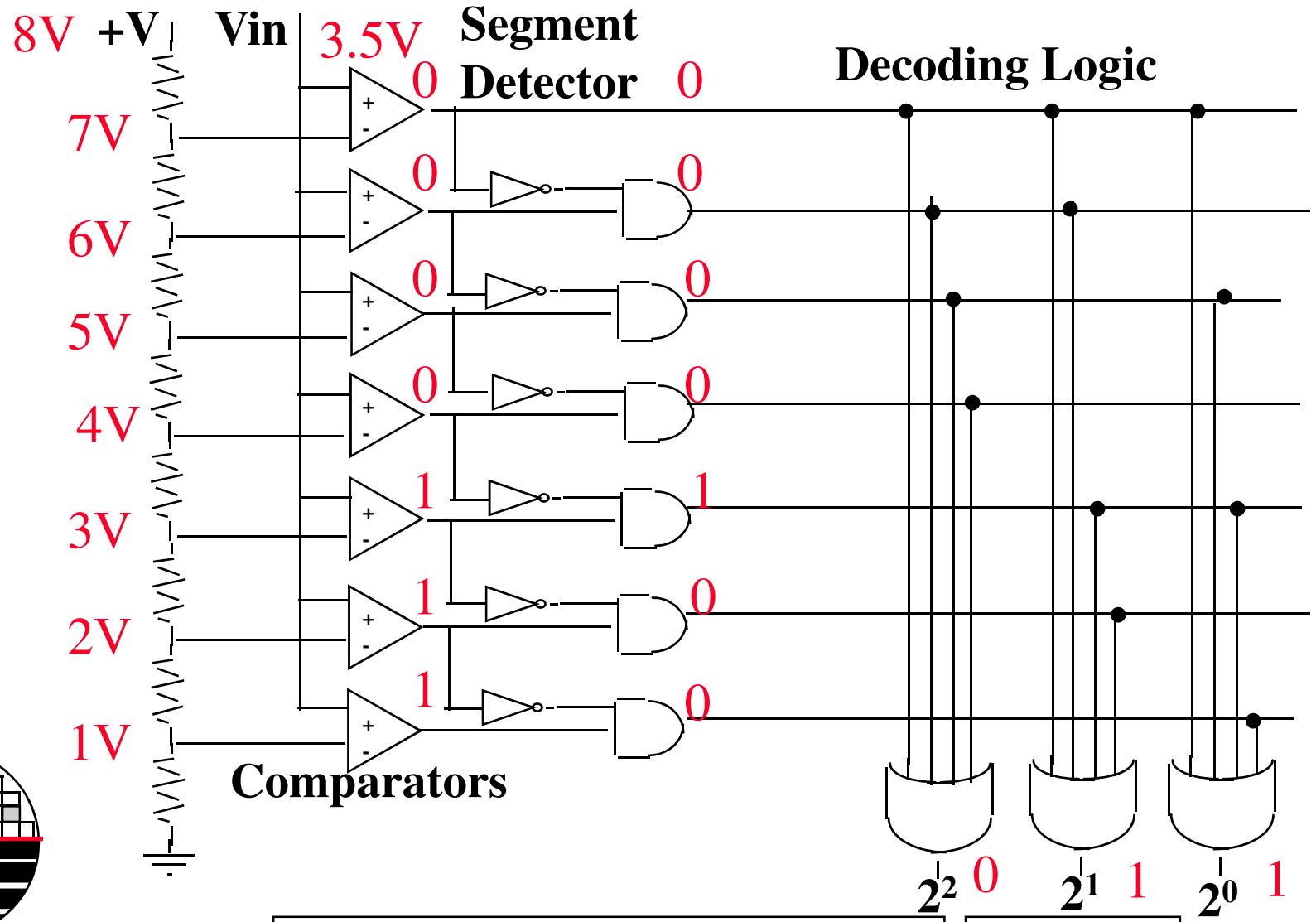
OTA, BIQUAD ELLIPTIC FILTER



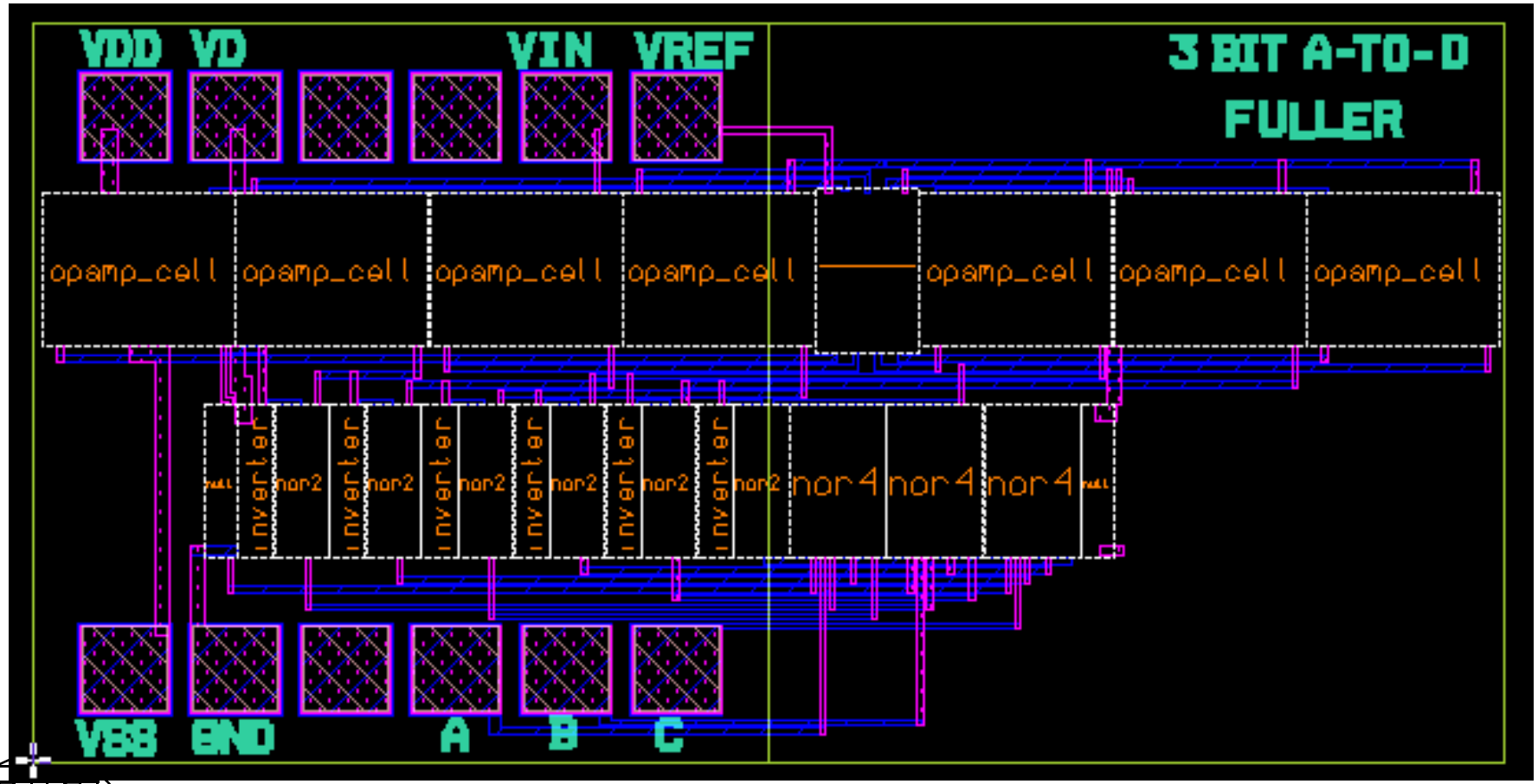




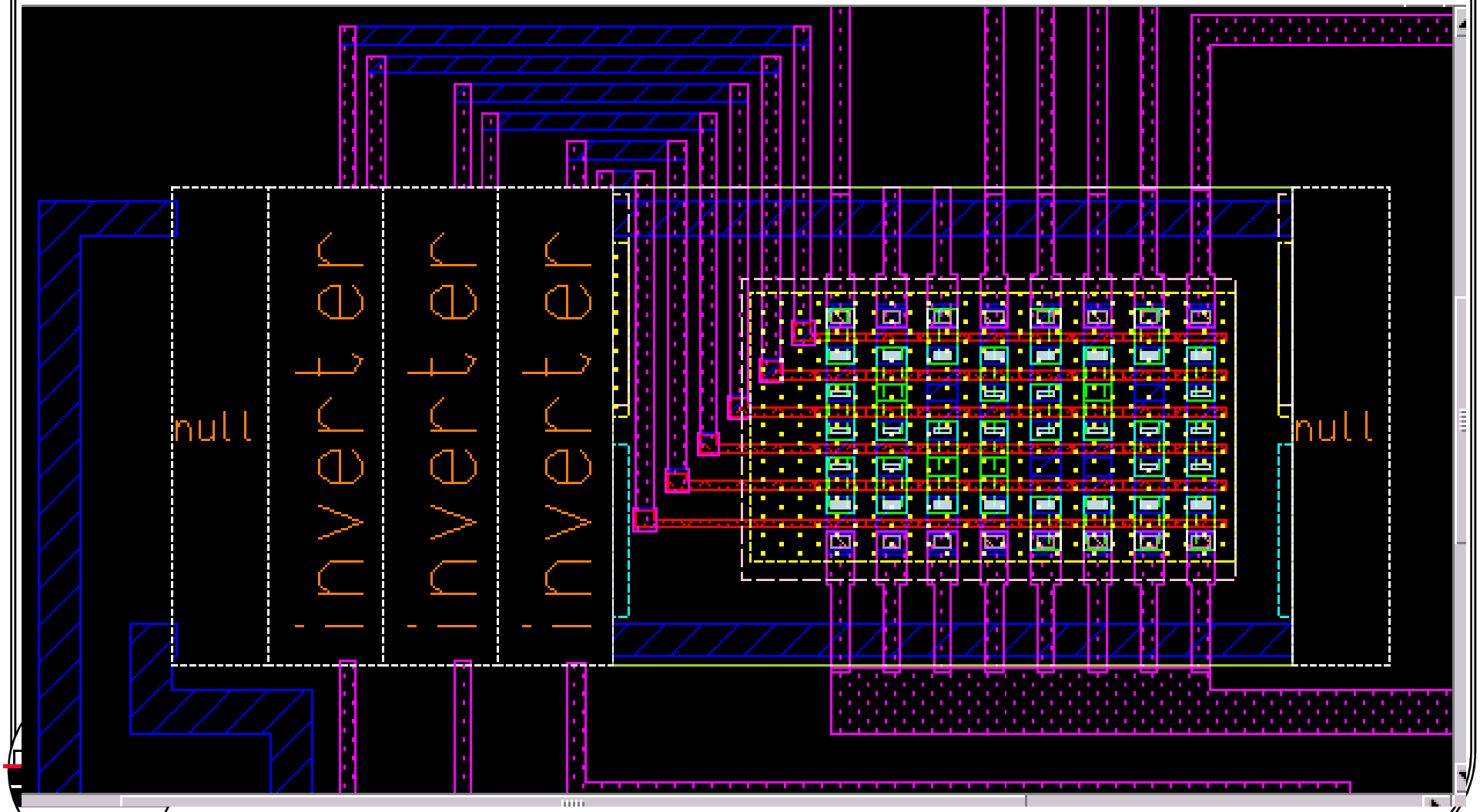
3 BIT ANALOG TO DIGITAL CONVERTER



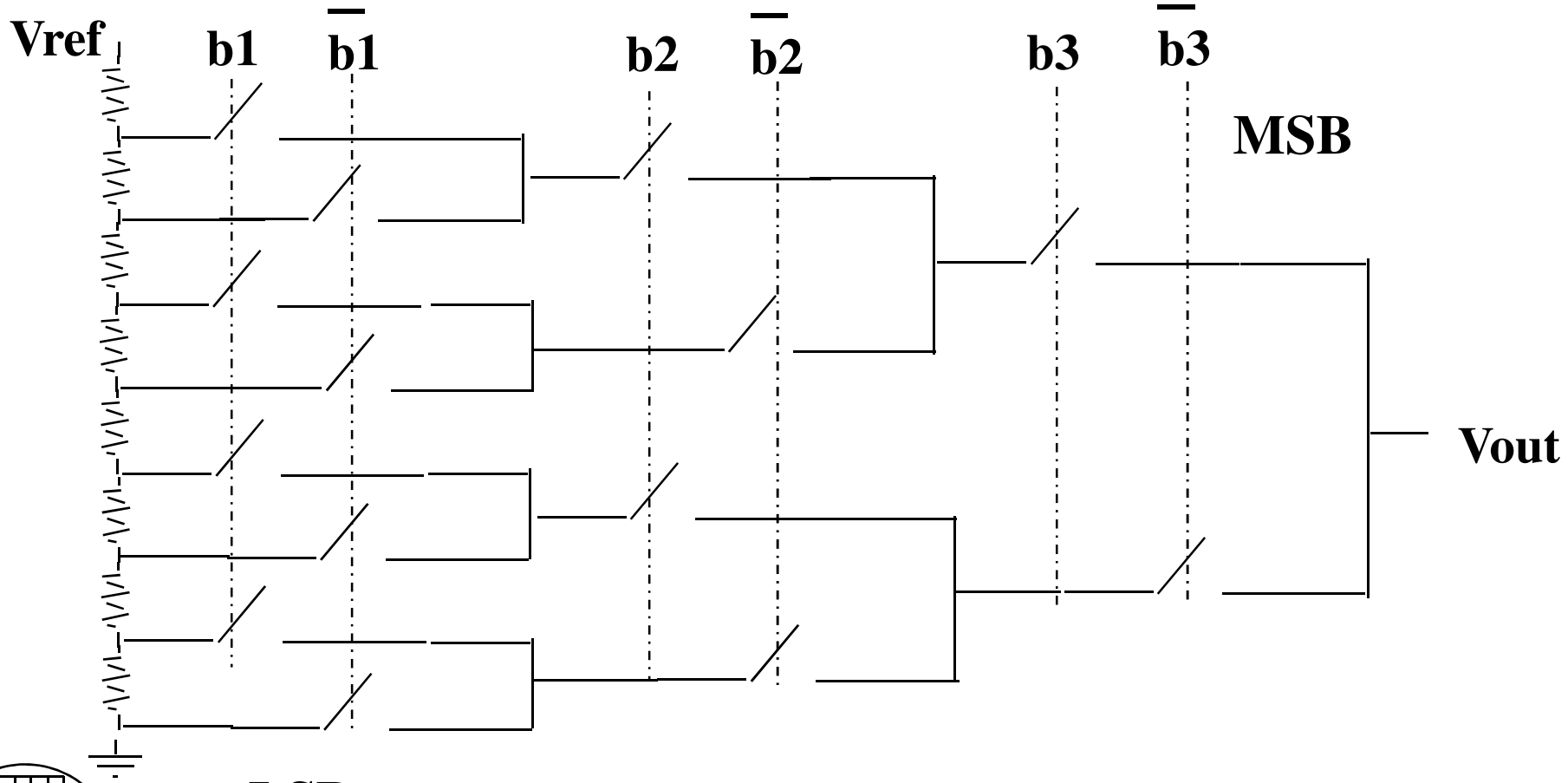
3 BIT ANALOG TO DIGITAL CONVERTER



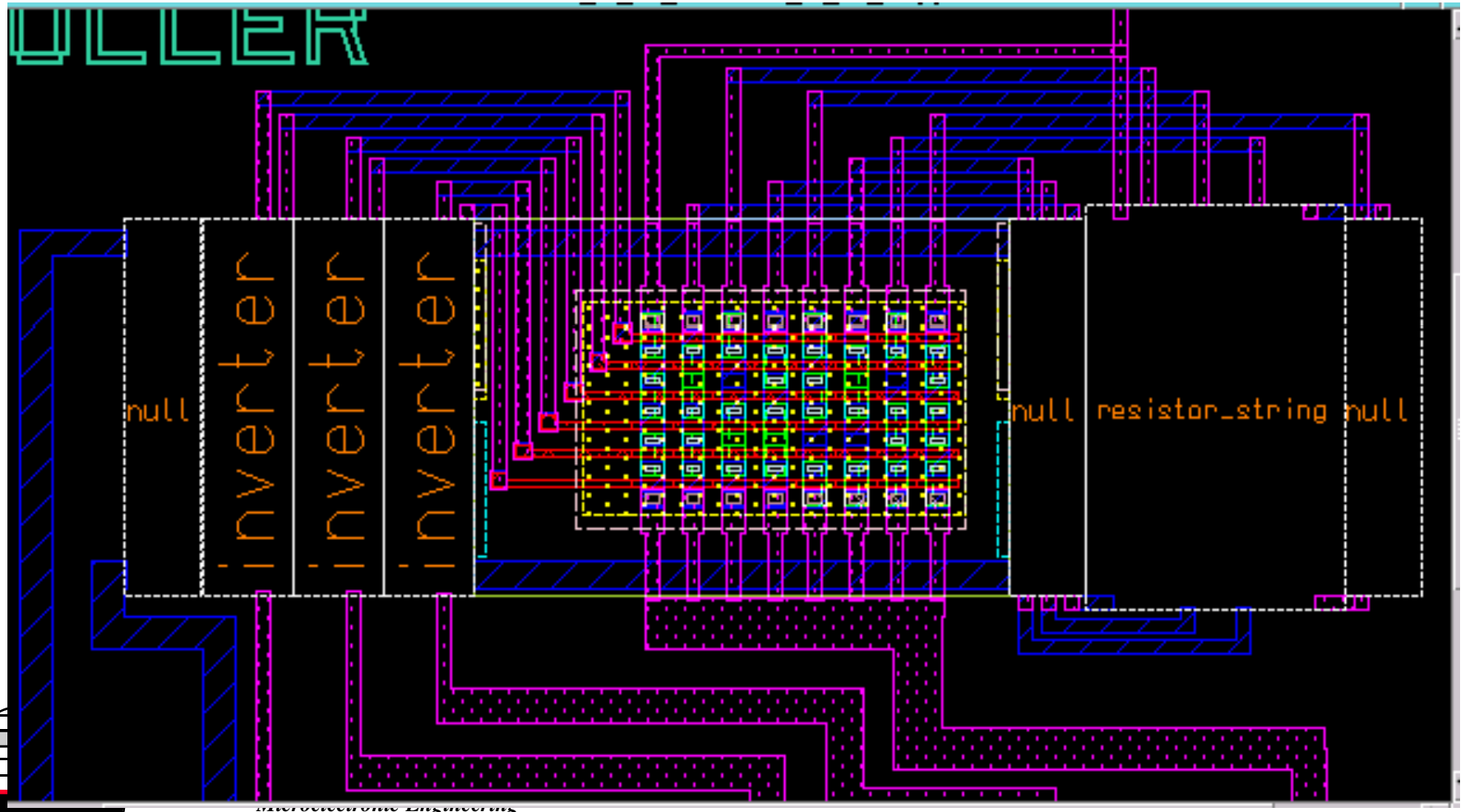
8 TO 1 ANALOG MUX



3 BIT D TO A


Vref
b1
$\overline{b1}$
b2
$\overline{b2}$
b3
$\overline{b3}$
MSB
Vout
LSB

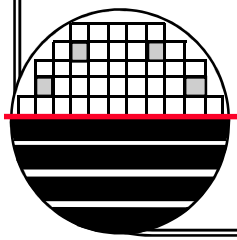
3 BIT D TO A



OTHER ANALOG BUILDING BLOCKS

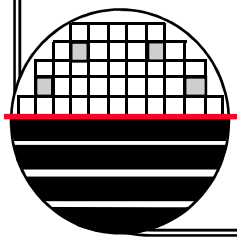
Comparator With Hysteresis
Voltage Controlled Oscillator
Binary Weighted R-2R Current Source
EEPROM
Binary Weighted EEPROM Selected Current Source
CCD
CCD Shift Register
More…

Not Done

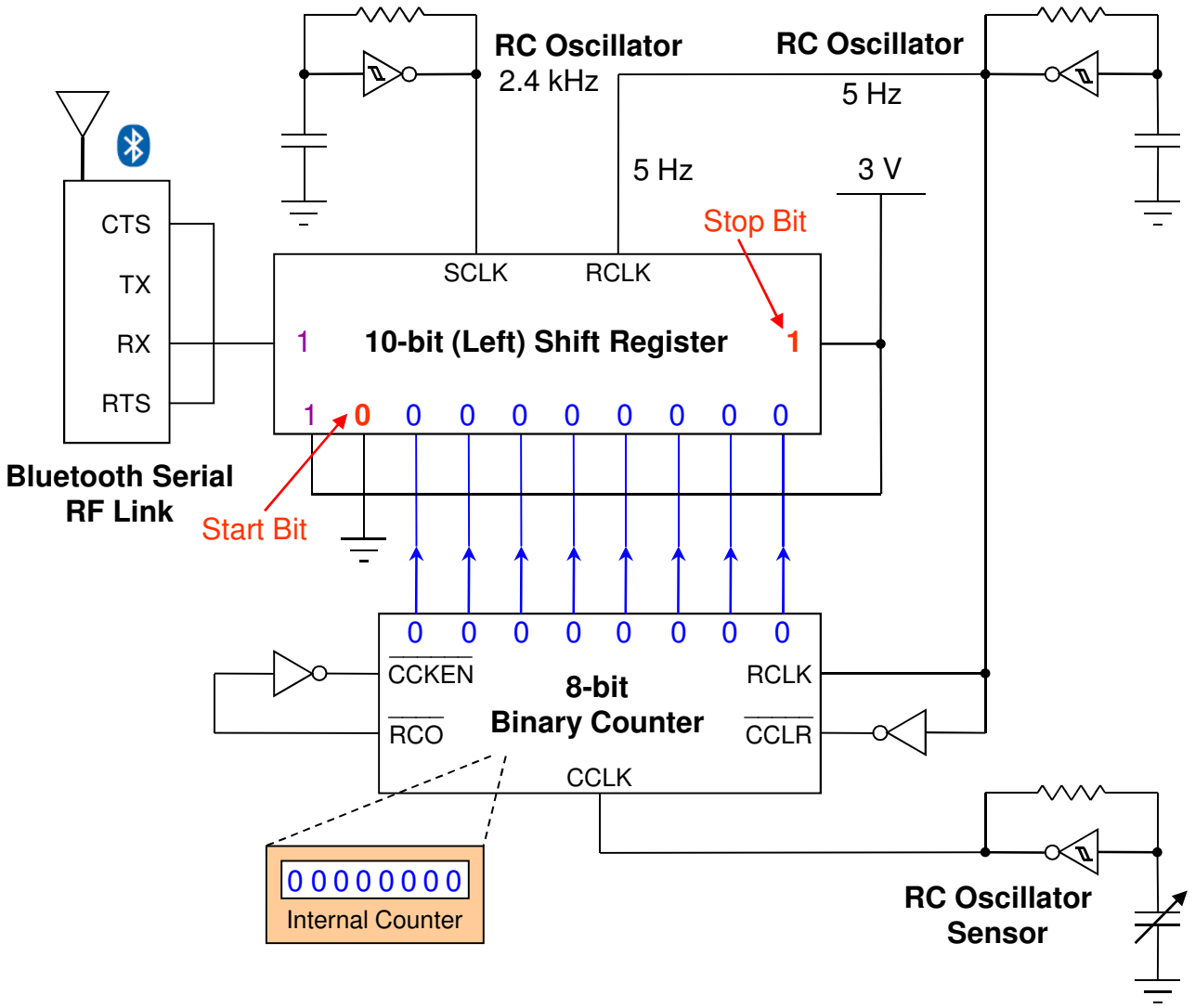


PROJECTS

Wireless Capacitive Sensor
Spectro Photometer
Hearing Aid
CCD Imager

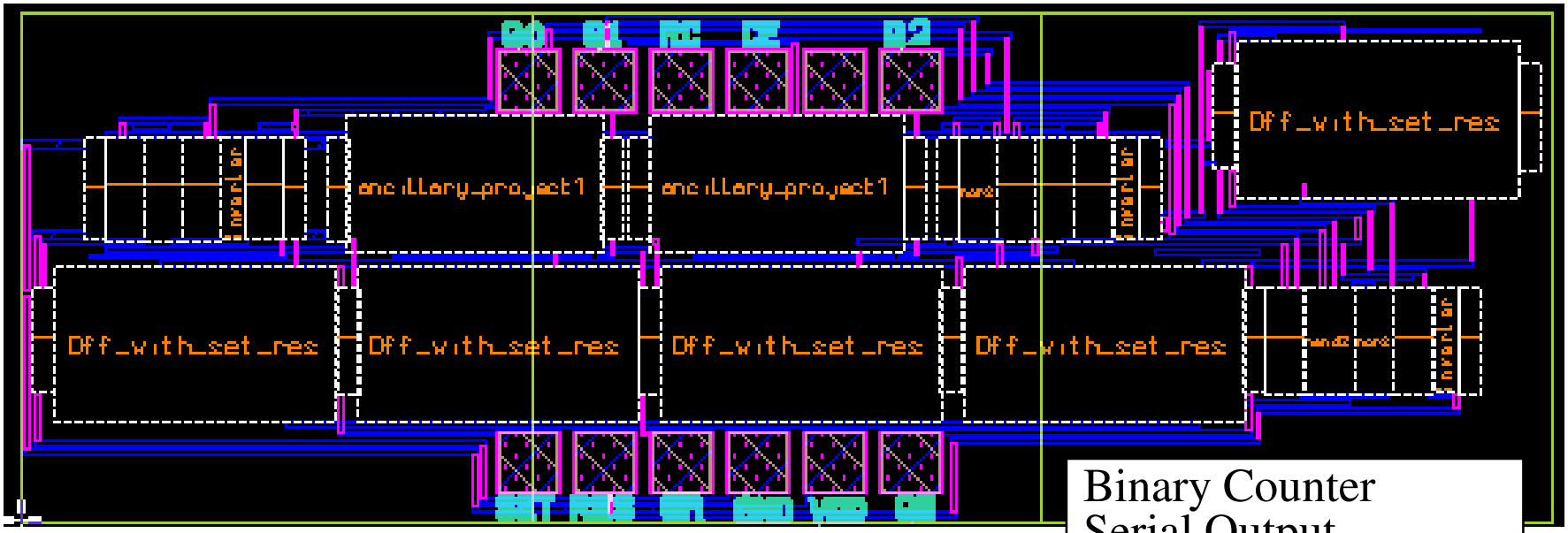


WIRELESS CAPACITIVE SENSOR PROJECT



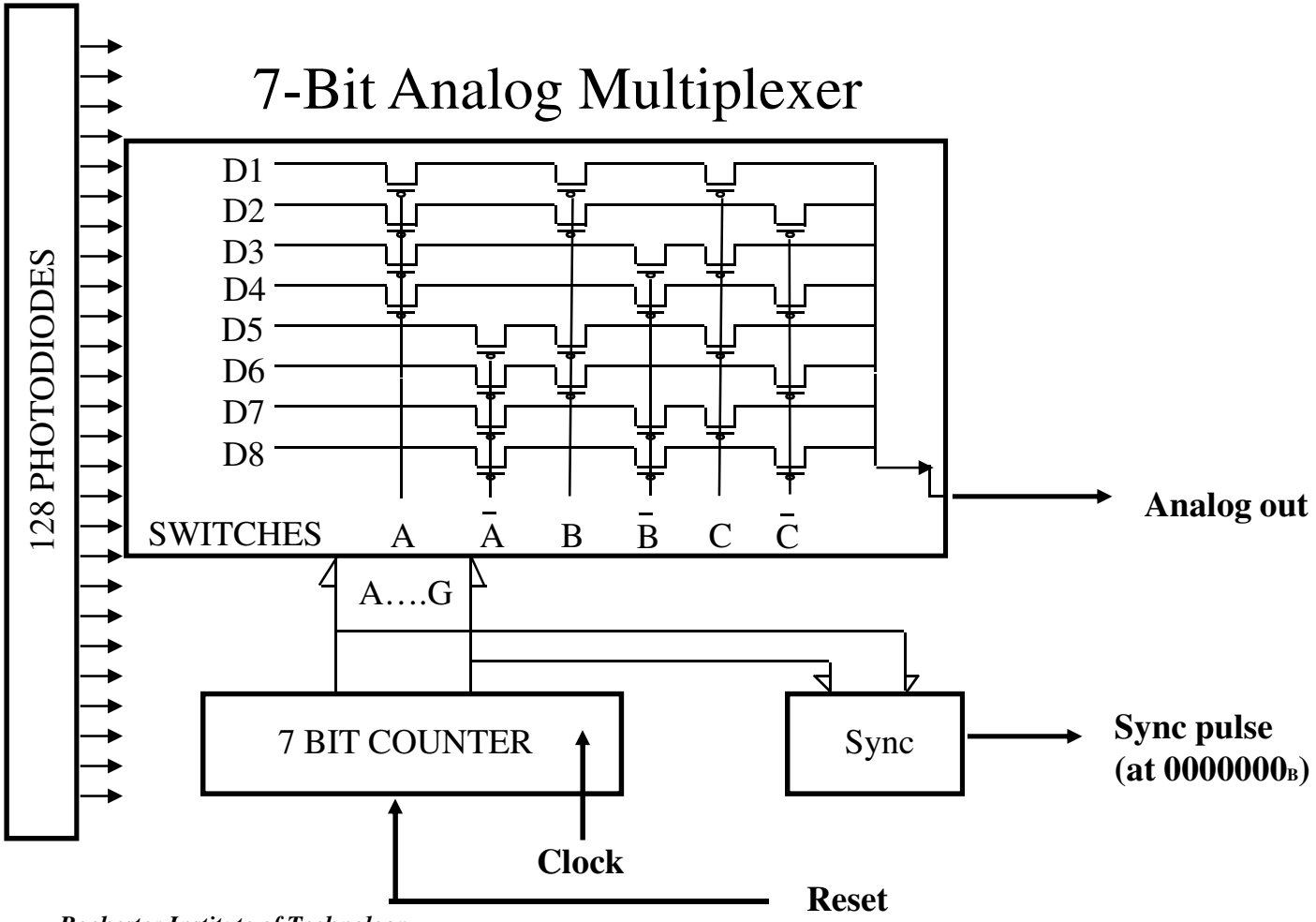
UP/DOWN COUNTER AND SHIFT REGISTERS

Many of these circuits need Up/Down counters and shift registers. In the next few pages we will look at one type of counter and see how to modify it to also function as a shift register.

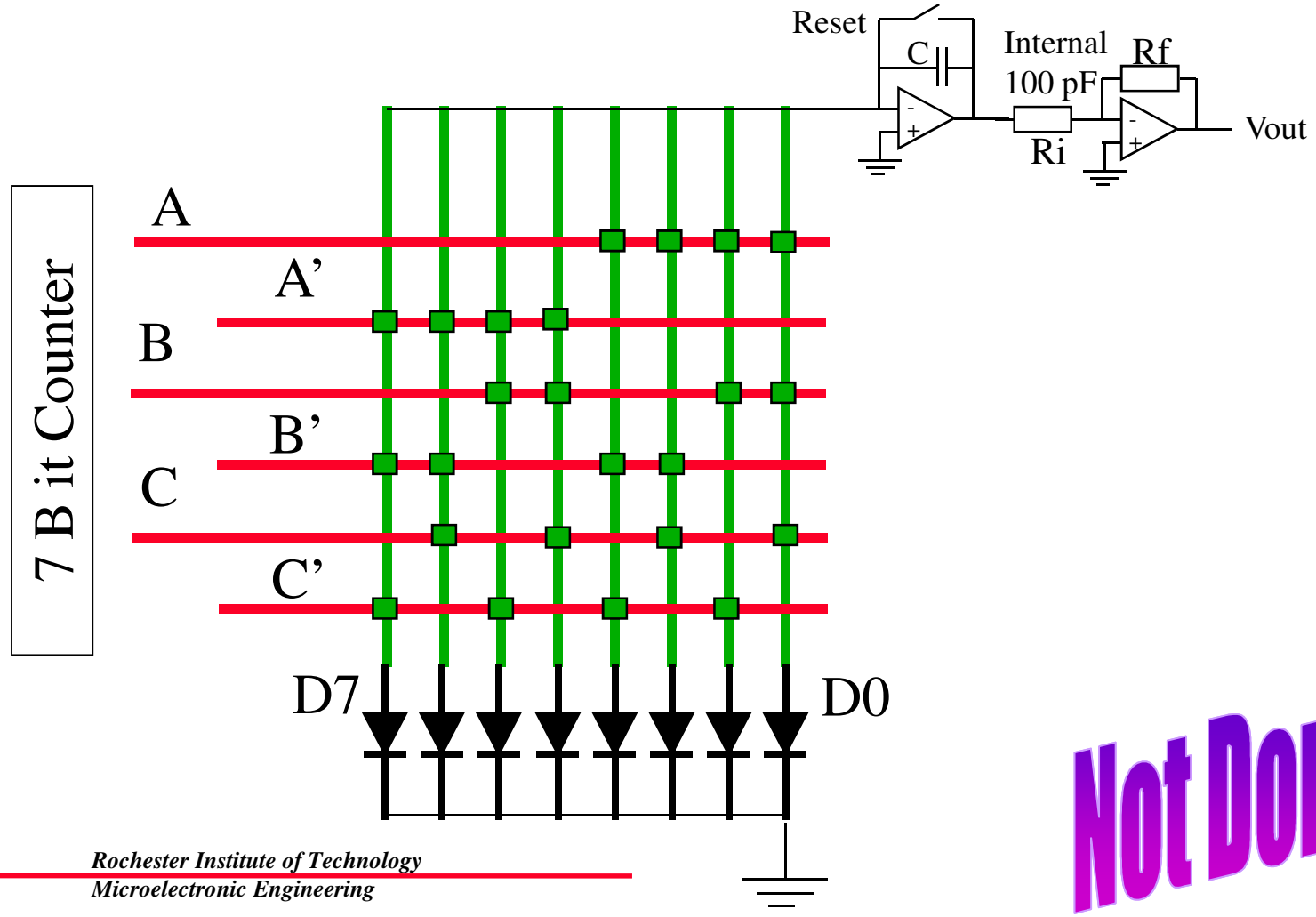


Binary Counter
Serial Output
Asynchronous Reset
Count Up Enable
Shift Out Clock Input
Count Up Clock Input
Start Bit and Stop Bit

SPECTROPHOTOMETER



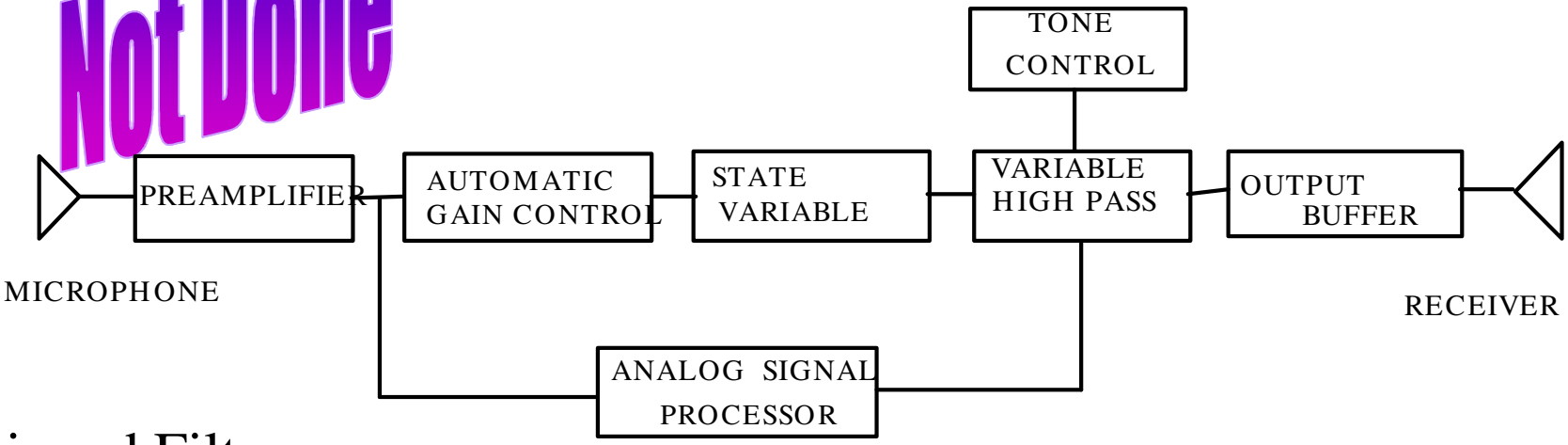
SPECTRO PHOTOMETER PROJECT



Not Done

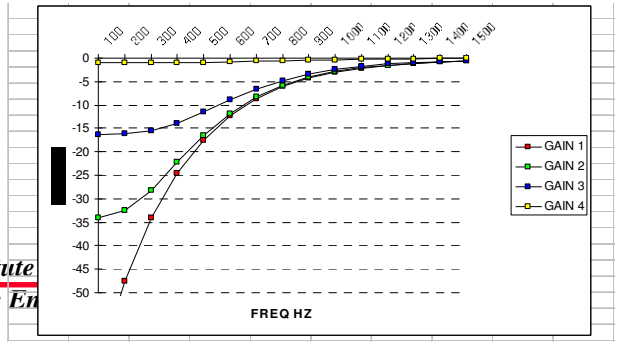
HEARING AID PROJECT

Not Done

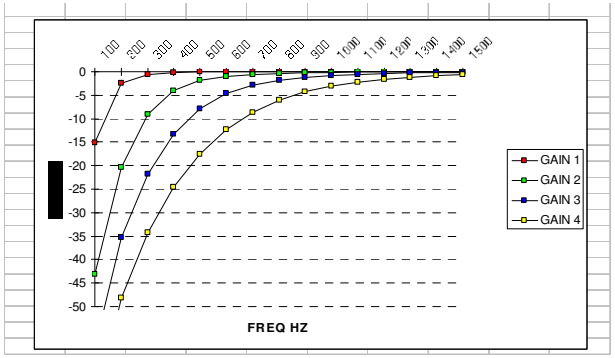


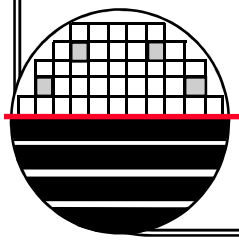
Biquad Filters
EEPROM
MEMS Microphone
MEMS Speaker
Energy Harvesting

4th Order High Pass
Pole Constant, Zero Varied



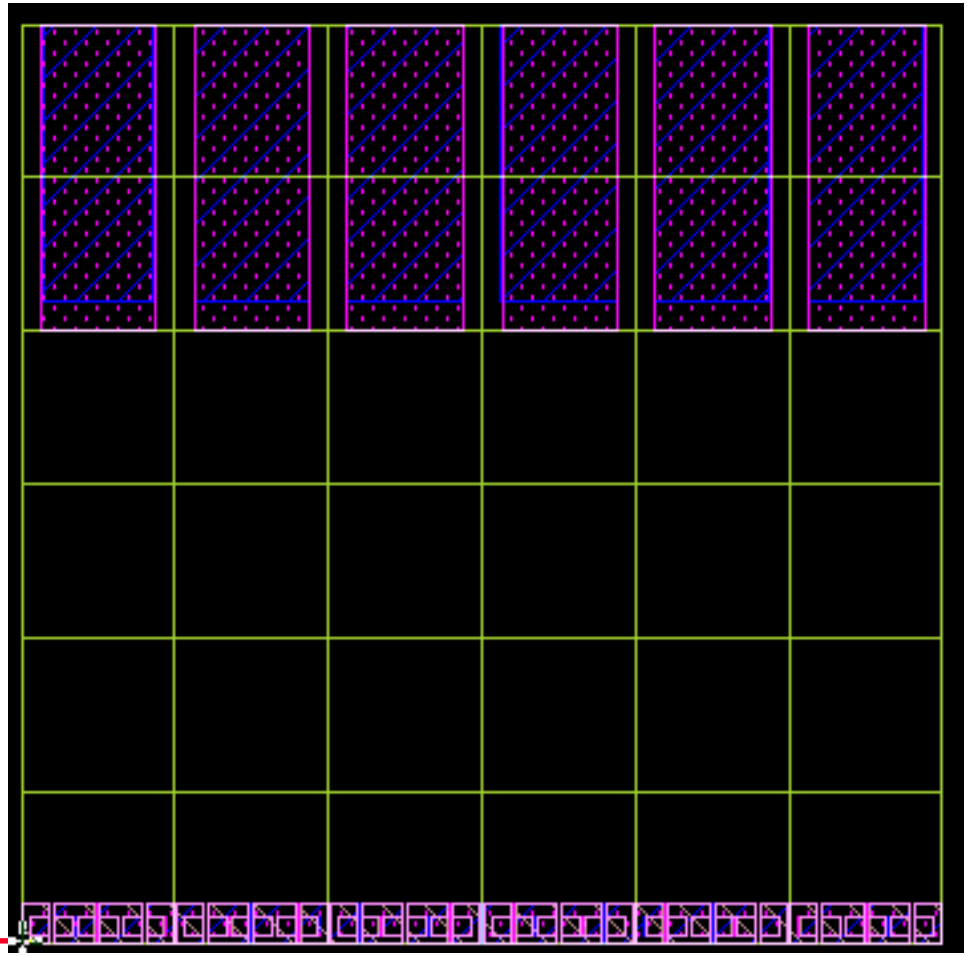
4th Order High Pass
Zero Constant, Pole Varied

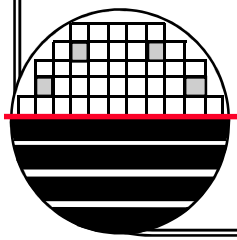




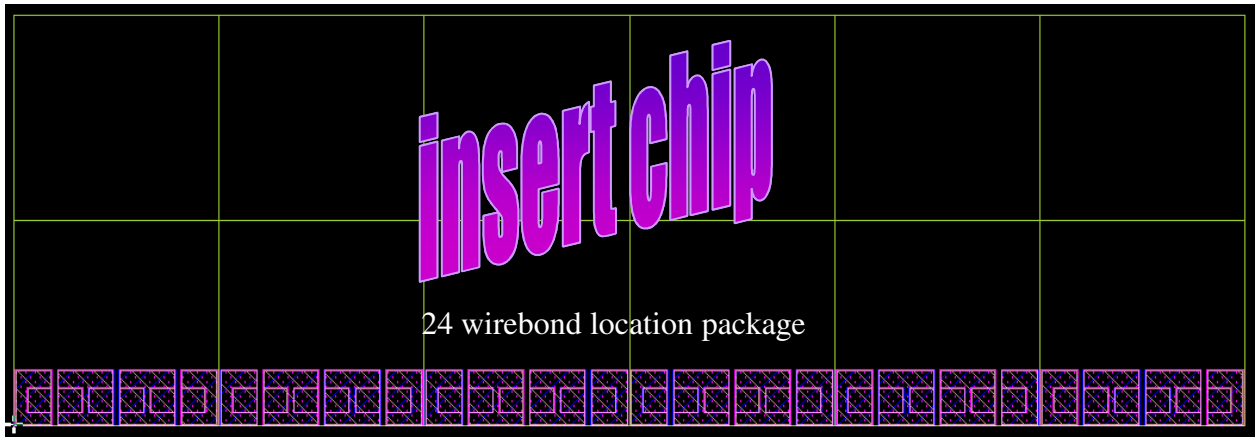
PACKAGING

Wire Bond Pads
SODIMM Connectors
(Zero Insertion Force)
Solder Bump

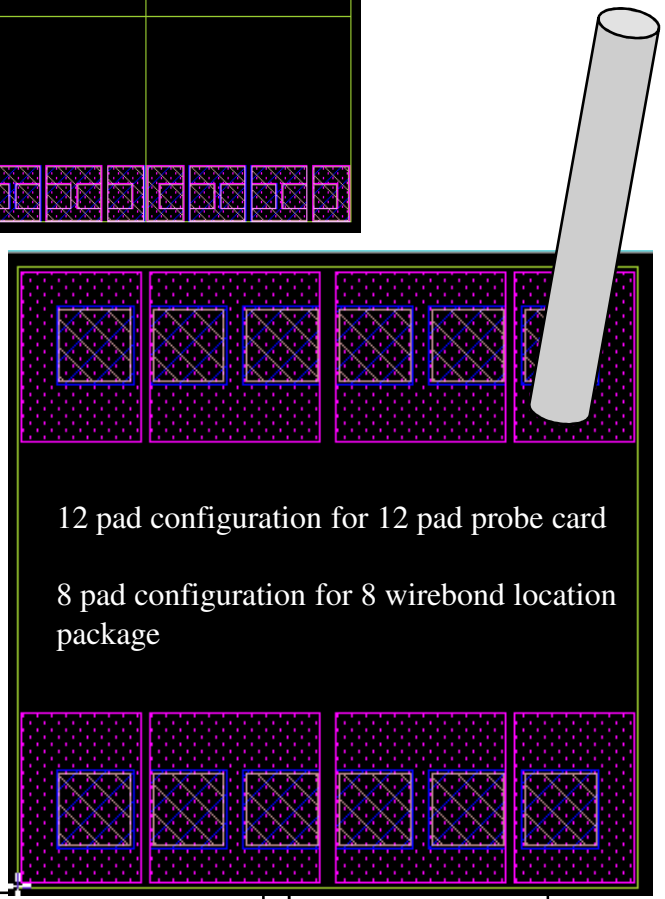




WIREBOND PADS FOR PACKAGING



Pads ~0.22mm x 0.22mm
With ~ 0.030mm space
Wire is ~75µm diameter
Bond is ~150 µm diameter



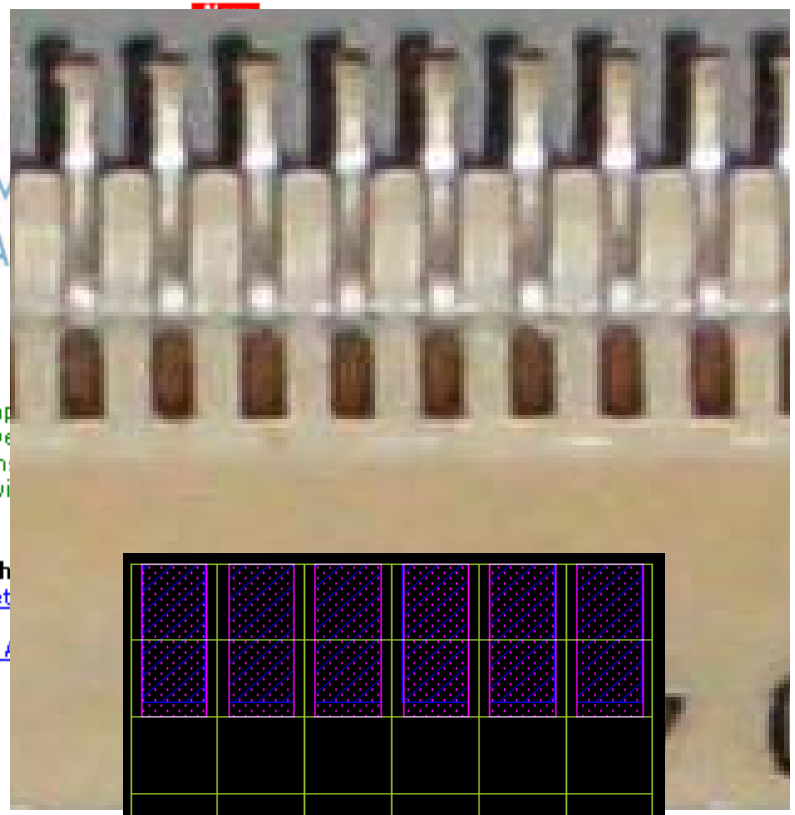
S.O.DIMM CONNECTOR

144 CONTACT(S), FEMALE, RIGHT ANGLE SINGLE PART CARD EDGE CONN, SURFACE MOUNT, SOCKET

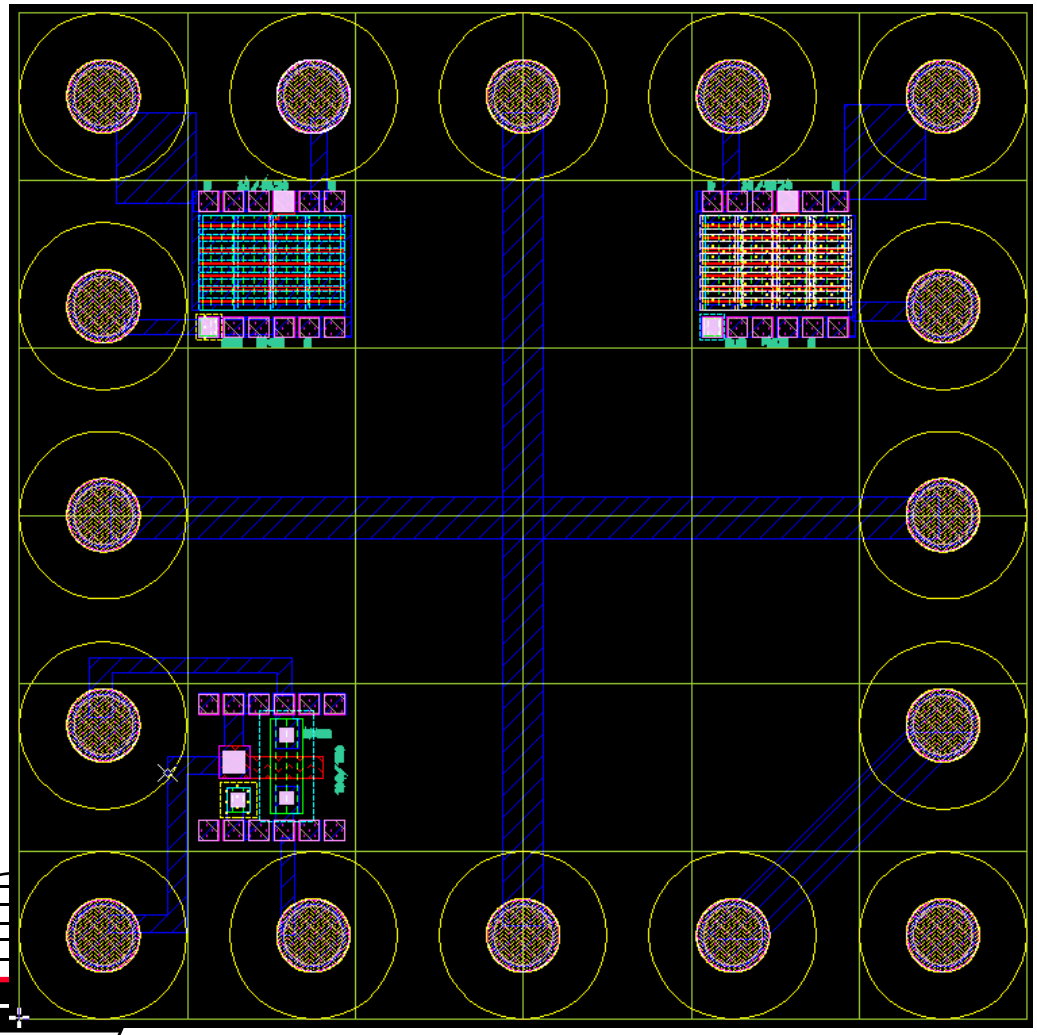
This product ships from a Jameco satellite warehouse, usually within 2 to 3 the next business day when received by 5:00PM EST. Please choose *expedited processing* at checkout if you prefer to have the other products on your order ship immediately. Separate shipping charges would then apply.

Jameco P/N	801588PS
Mfg	MOLEX INC.
Mfg #	54697-1440
RoHS?	Yes
In Stock	Y
Contact Gender	FEMALE
Filter Feature	NO
Mixed Contacts	NO
Mounting Style	RIGHT ANGLE
Mounting Type	BOARD
Number of Rows Loaded	2
Single Part Card Edge Connector Type	SINGLE PART CARD EDGE CONN
Terminal Pitch (mm)	0.8

0.8 S.O.DIMM HSG ASSY 144CKT



SOLDER BUMP TEST CHIP

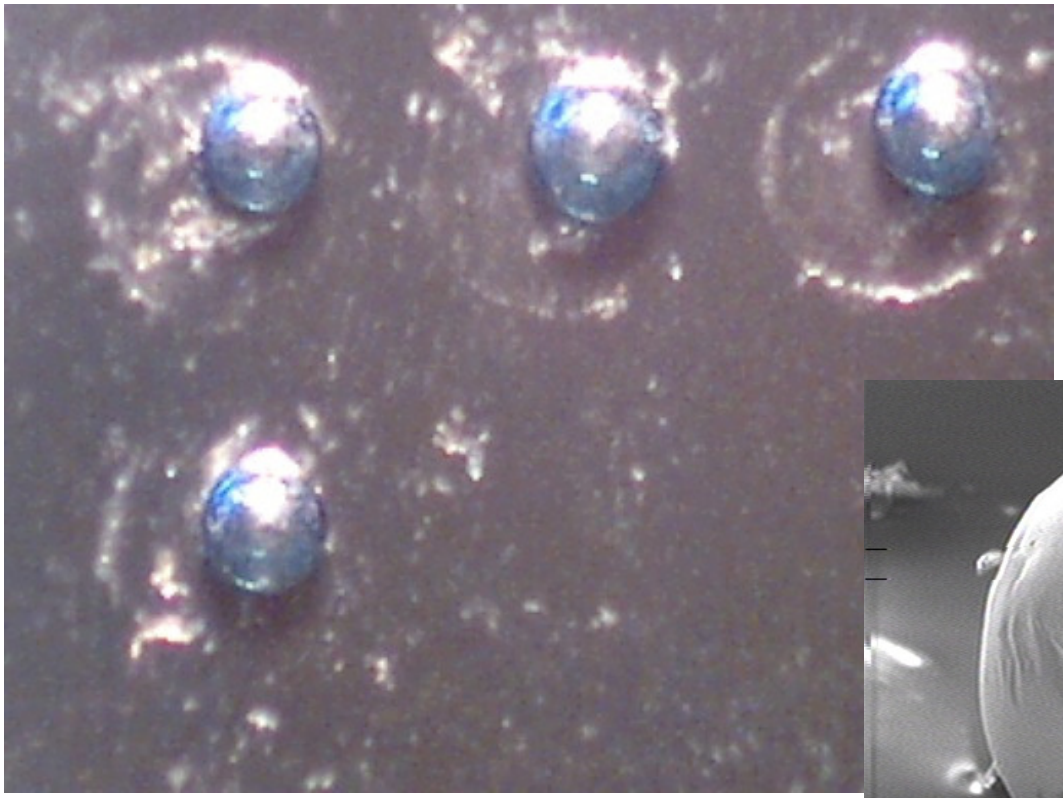


1000µm center-to-center
225µm diameter circle

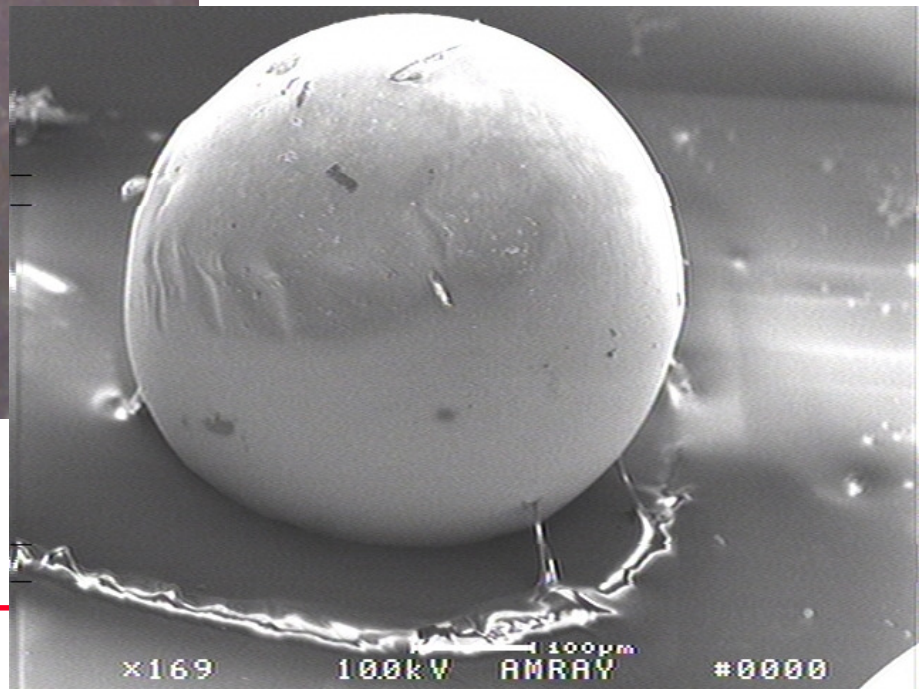
Under bump metal is Cr/Ni and is defined by a lift-off lithography.

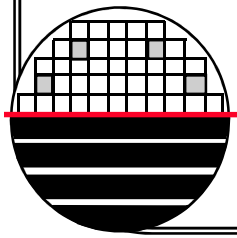
The solder is printed using a 150um photoresist and solder paste. (or 500um solder ball is placed over circle)

RIT SOLDER BUMPS

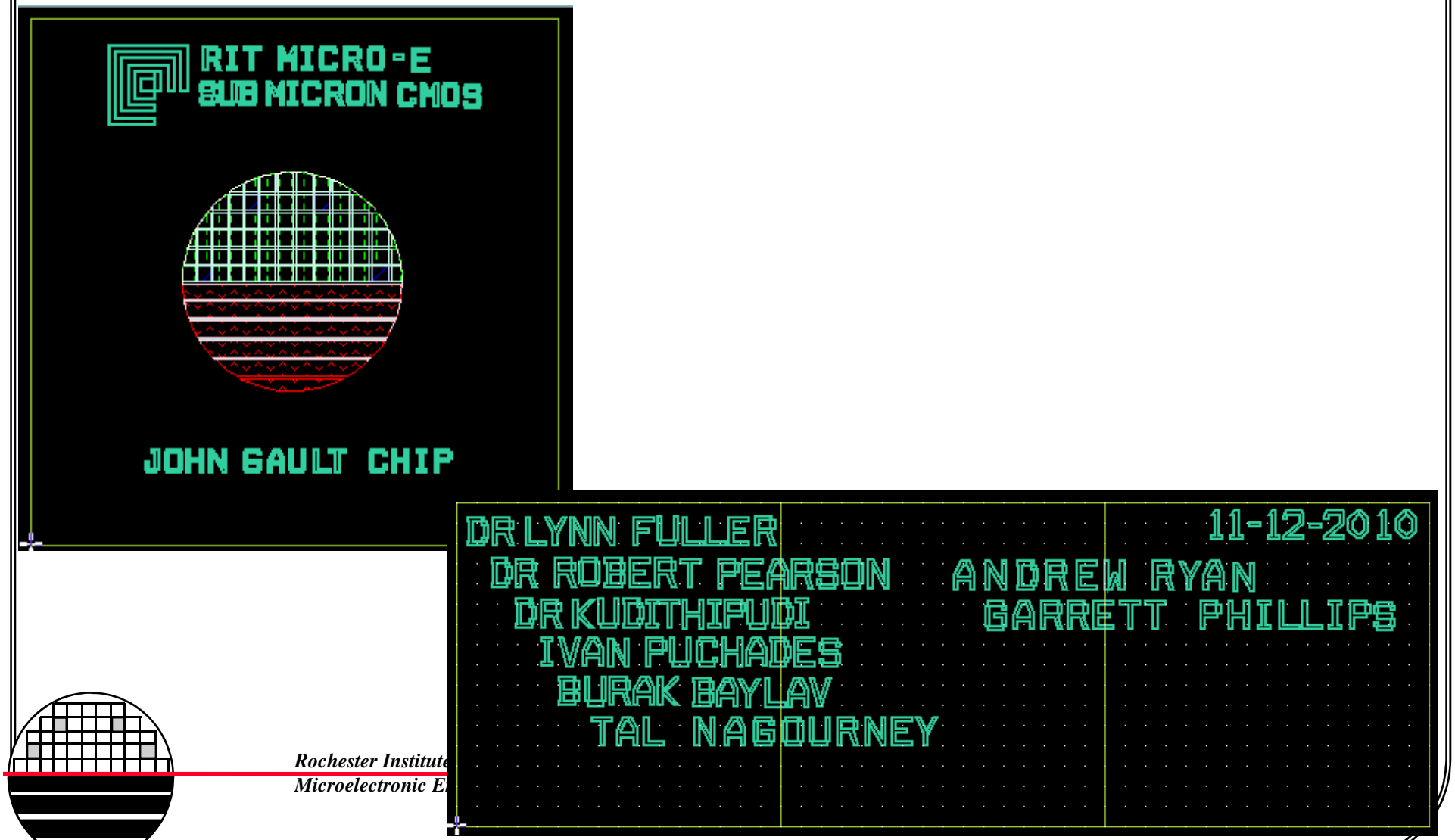


~500µm





LOGO AND ACKNOWLEDGEMENTS



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10. Texas Instruments, Data Sheet for inverter with hysteresis.

HOMEWORK

1. Calculate the expected values of the poly heaters over the diode temperature sensors on page 47.
2. For the PMOS transistor shown on page29 determine Lambda, Idrive, gm max, and Vt. Use correct units as shown on page 25-27.
3. Why is the gate delay different for the two ring oscillators shown on page 33.
4. List the digital circuits that were shown to be working correctly in this document.
5. Write a 150 word abstract for the John Galt Chip and the test results shown in this document.