ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

CMOS VLSI DESIGN

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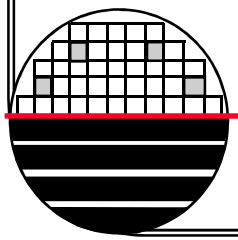
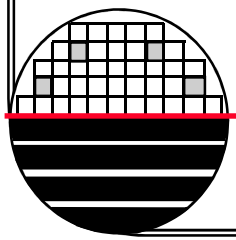


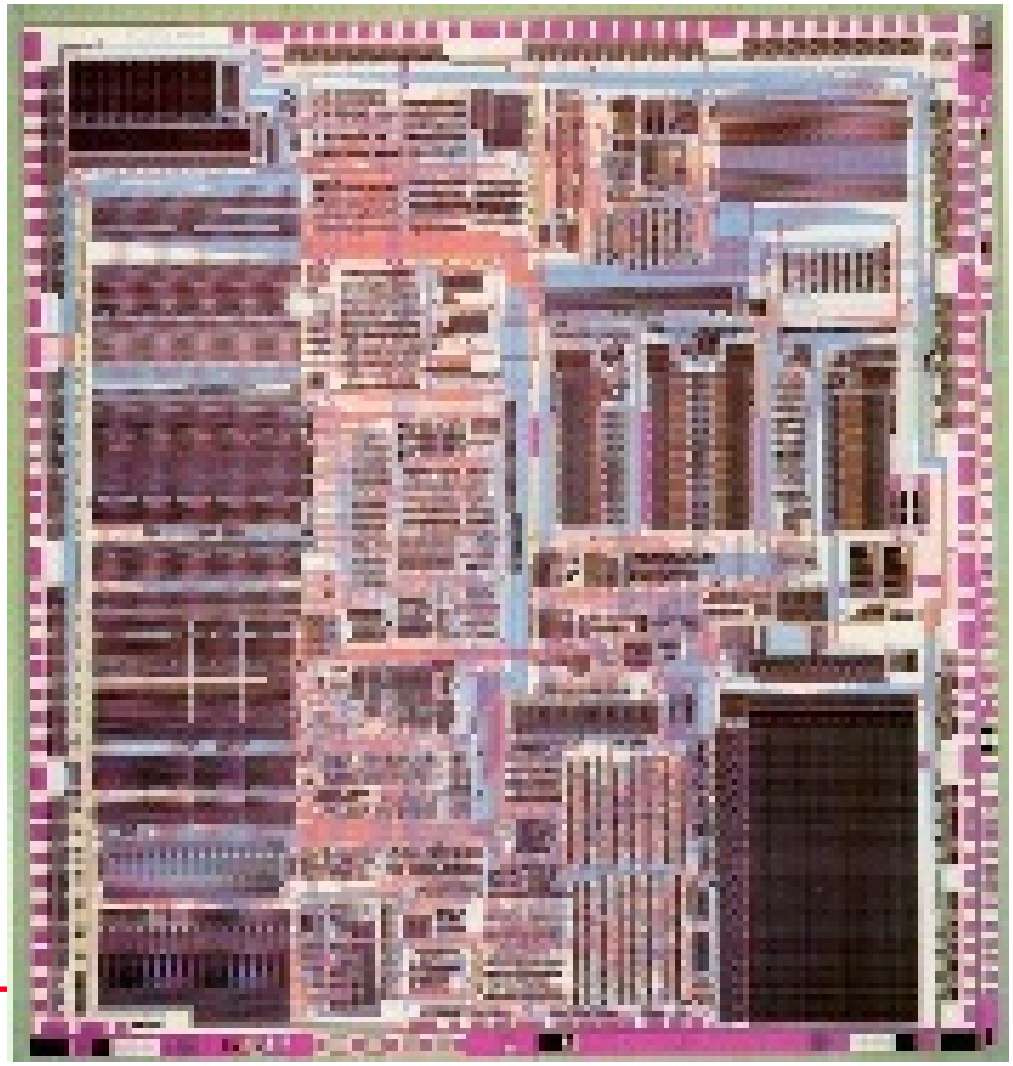
OUTLINE

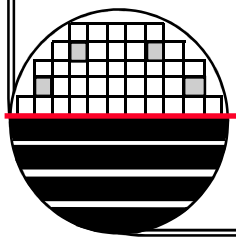
Design Approach
Process Technology
MOSIS Design Rules
Primitive Cells, Basic Cells, Macro Cells
Projects
Maskmaking
References
Homework



THE NEED FOR CAD

With millions of transistors per chip it is impossible to design with no errors without computers to check layout, circuit performance, process design, etc.





COMPARISON OF DESIGN METHODOLOGIES

Full Custom Design

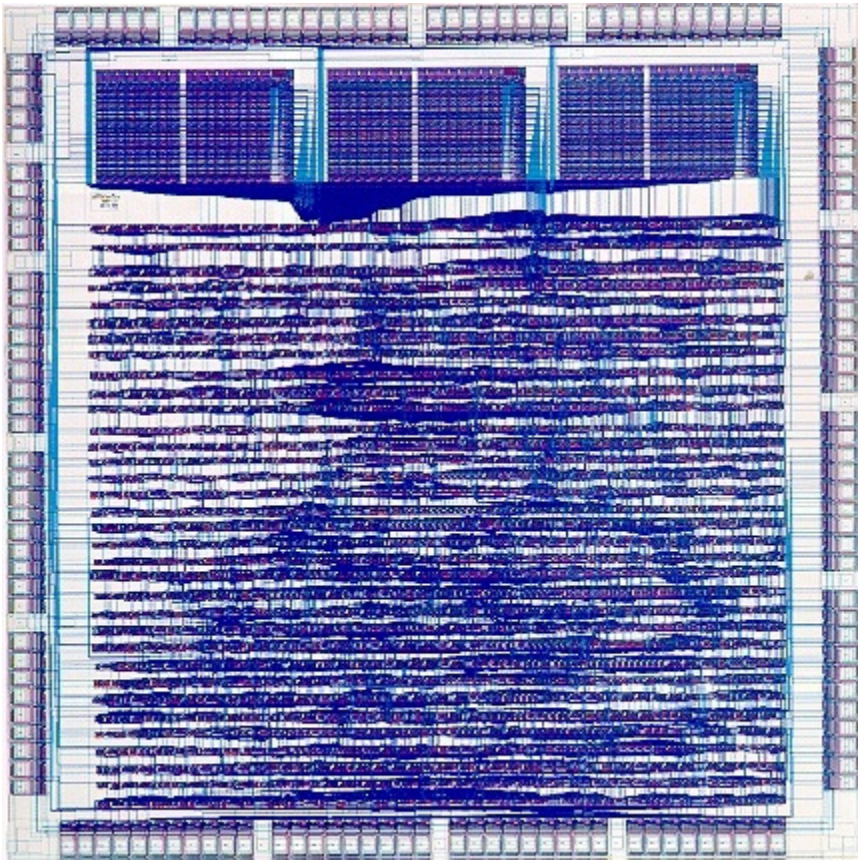
Direct control of layout and device parameters
Longer design time
but faster operation
more dense

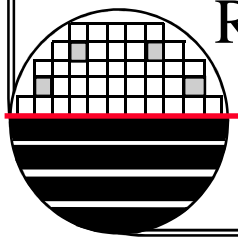
Standard Cell Design

Easier to implement
Limited cell library selections

Gate Array or
Programmable Logic Array Design

Fastest design turn around
Reduced Performance





STAGES IN THE CAD PROCESS

Problem Specification

Behavioral Design

Functional and Logic Design

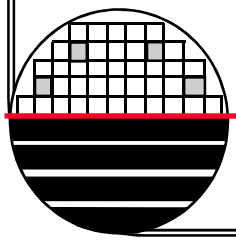
Circuit Design

Physical Design (Layout)

Fabrication Technology CAD (TCAD)

Packaging

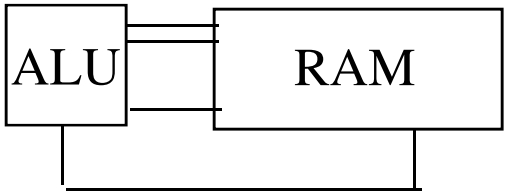
Testing



DESIGN HEIRARCHY - LEVELS OF ABSTRACTION

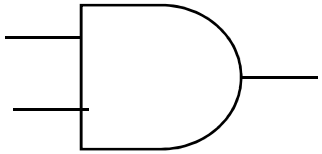
A = B + C
if (A) then X: = Y

Behavioral Model

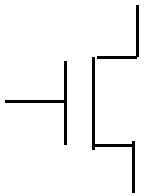


Block-Functional Model

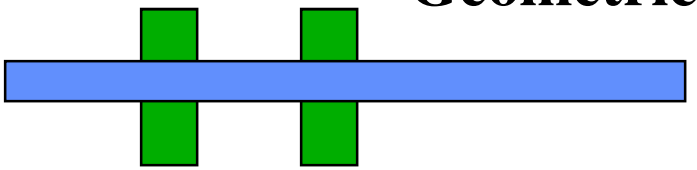
Gate-Level Model

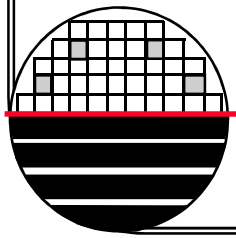


Transistor level Model



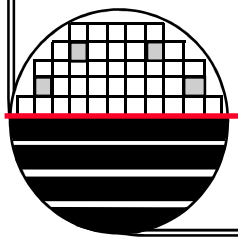
Geometric Model





PROCESS SELECTION

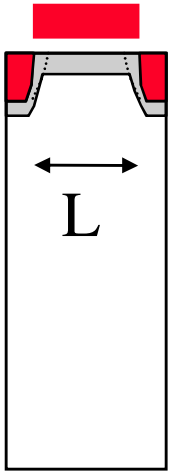
It is not necessary to know all process details to do CMOS integrated circuit design. However the process determines important circuit parameters such as supply voltage and maximum frequency of operation. It also determines if devices other than PMOS and NMOS transistors can be realized such as poly-to-poly capacitors and EEPROM transistors. The number of metal interconnect layers is also part of the process definition.



RIT SUBμ CMOS

RIT Subμ CMOS

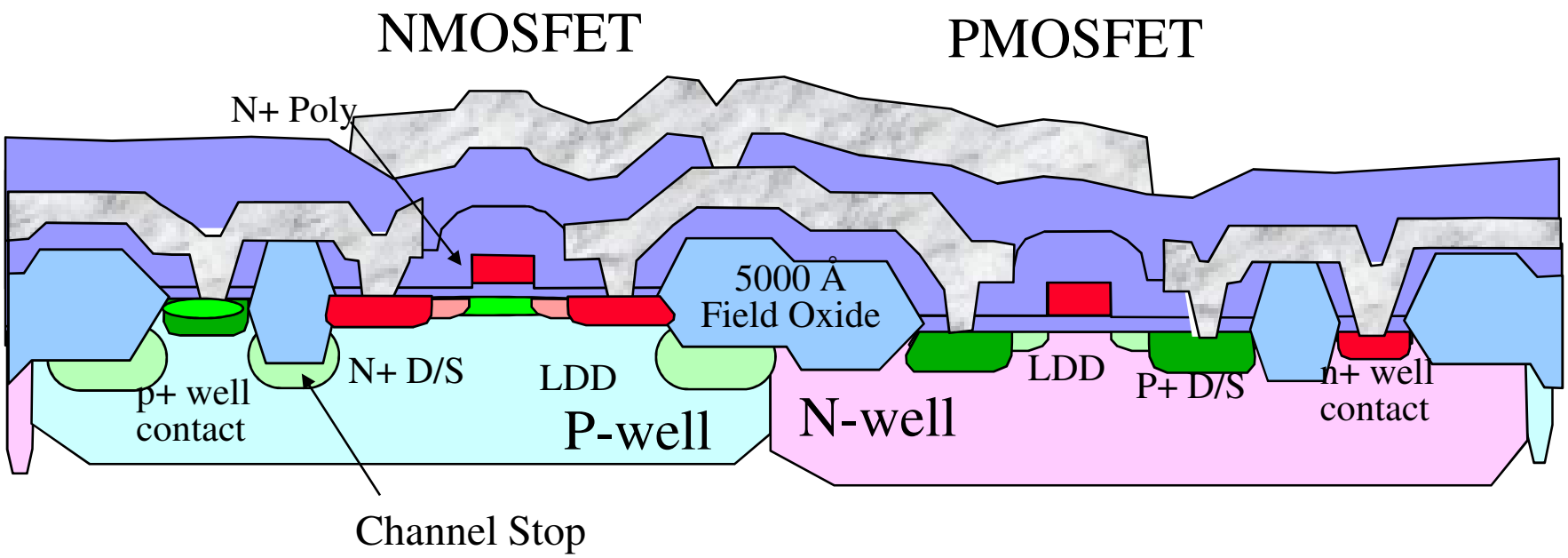
150 mm wafers
Nsub = 1E15 cm-3
Nn-well = 3E16 cm-3
Xj = 2.5 μm
Np-well = 1E16 cm-3
Xj = 3.0 μm
LOCOS
Field Ox = 6000 Å
Xox = 150 Å
Lmin= 1.0 μm
LDD/Side Wall Spacers
2 Layers Aluminum



Long Channel Behavior

3.3 Volt Technology
VT's = +/- 0.75 Volt
Robust Process (always works)
Fully Characterized (SPICE)

RIT SUBμ CMOS

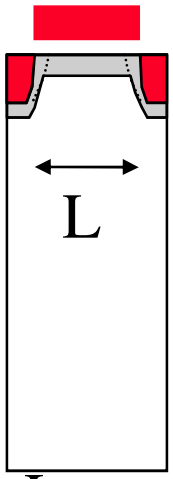


Substrate 10 ohm-cm

RIT ADVANCED CMOS VER 150

RIT Advanced CMOS

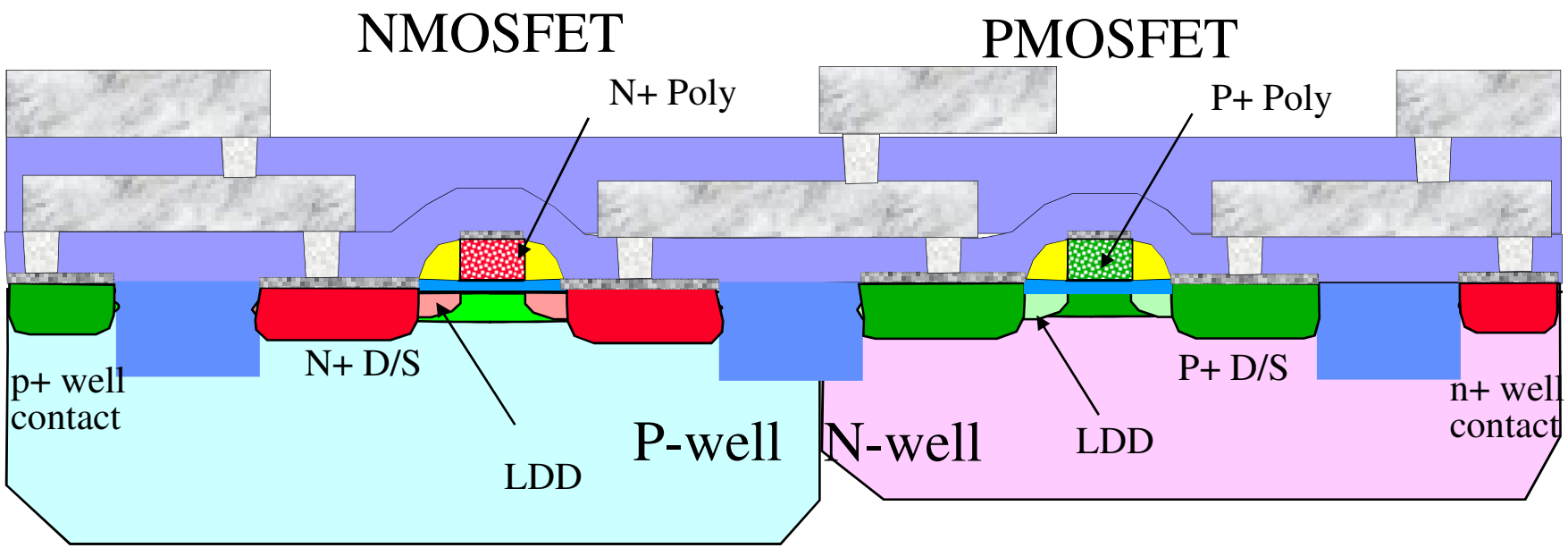
150 mm Wafers
Nsub = 1E15 cm-3 or 10 ohm-cm, p
Nn-well = 1E17 cm-3
Xj = 2.5 µm
Np-well = 1E17 cm-3
Xj = 2.5 µm
Shallow Trench Isolation
Field Ox (Trench Fill) = 4000 Å
Dual Doped Gate n+ and p+
Xox = 100 Å
Lmin = 0.5 µm , Lpoly = 0.35 µm, Leff = 0.11 µm
LDD/Nitride Side Wall Spacers
TiSi2 Salicide
Tungsten Plugs, CMP, 2 Layers Aluminum



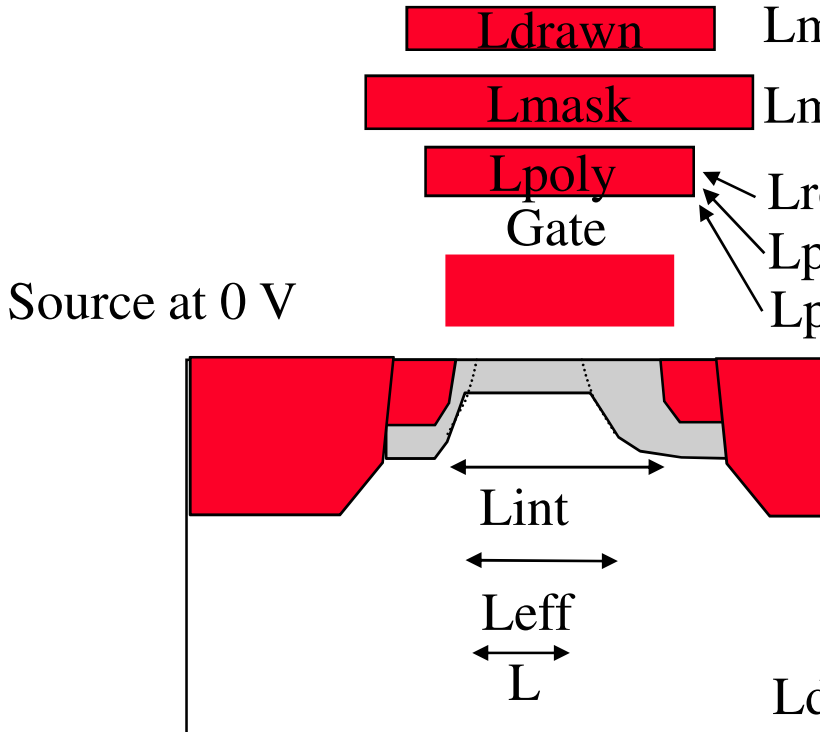
Long Channel Behavior

Vdd = 3.3 volts
Vto=+- 0.75 volts

RIT ADVANCED CMOS



LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L



Lambda = design rule parameter, λ, ie	0.25µm
Lmin = min drawn poly length, 2λ	0.50µm
Lmask = ? Depends on +/-bias	1.00µm x 5
Lresist after photo (resist trimming??)	0.50µm
Lpoly after poly etch	0.40µm
Lpoly after poly reoxidation	0.35µm
	0.30µm
	0.20µm
	0.11µm

Ldrawn = what was drawn

Internal Channel Length, Lint =distance between junctions, including under diffusion

Effective Channel Length, Leff = distance between space charge layers,Vd = Vs= 0

Channel Length, L, = distance between space charge layers, when Vd= what it is

Extracted Channel Length Parameters = anything that makes the fit good (not real)

MOSIS TSMC 0.35 2POLY 4 METAL PROCESS

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http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html#tech-codes

MOSIS SCMOS Technology Codes and Layer Maps

SCN4M and SCN4M_SUBM

This is the layer map for the technology codes SCN4M and SCN4M_SUBM using the MOSIS Scalable CMOS layout rules (SCMOS), and only for SCN4M and SCN4M_SUBM. For designs that are laid out using other design rules (or technology codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

SCN4M: Scalable CMOS N-well, 4 metal, 1 poly, silicided. Silicide block and thick oxide option available only on the TSMC process.

SCN4M_SUBM: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

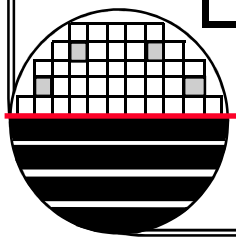
Fabricated on TSMC, AMIS, and Agilent/HP 0.35 micron process runs. See "Notes" section of layer map for foundry-specific options.

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	
ACTIVE	43	CAA		2	
THICK_ACTIVE	60	CTA		24	Optional for TSMC; not available for Agilent/HP nor AMIS
POLY	46	CPG		3	
SILICIDE_BLOCK	29	CSB		20	Optional for Agilent/HP; not available for AMI
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	
METAL3	62	CM3	CMT	15	
VIA3	30	CV3	CVT	21	
METAL4	31	CM4	CMQ	22	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME

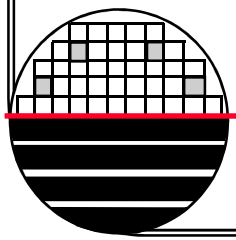
MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

MASK LAYER NAME	MENTOR NAME	GDS #	COMMENT
N WELL	N_well.i	42	
ACTIVE	Active.i	43	
POLY	Poly.i	46	
N PLUS	N_plus_select.i	45	
P PLUS	P_plus_select.i	44	
CONTACT	Contact.i	25	Active_contact.i 48 poly_contact.i 47
METAL1	Metal1.i	49	
VIA	Via.i	50	
METAL2	Metal2.i	51	



MORE LAYERS USED IN MASK MAKING

LAYER	NAME	GDS	COMMENT
	cell_outline.i	70	Not used
	alignment	81	Placed on first level mask
	nw_res	82	Placed on nwell level mask
	active_lettering	83	Placed on active mask
	channel_stop	84	Overlay/Resolution for Stop Mask
	pmos_vt	85	Overlay/Resolution for Vt Mask
	LDD	86	Overlay/Resolution for LDD Masks
	p plus	87	Overlay/Resolution for P+ Mask
	n plus	88	Overlay/Resolution for N+ Mask



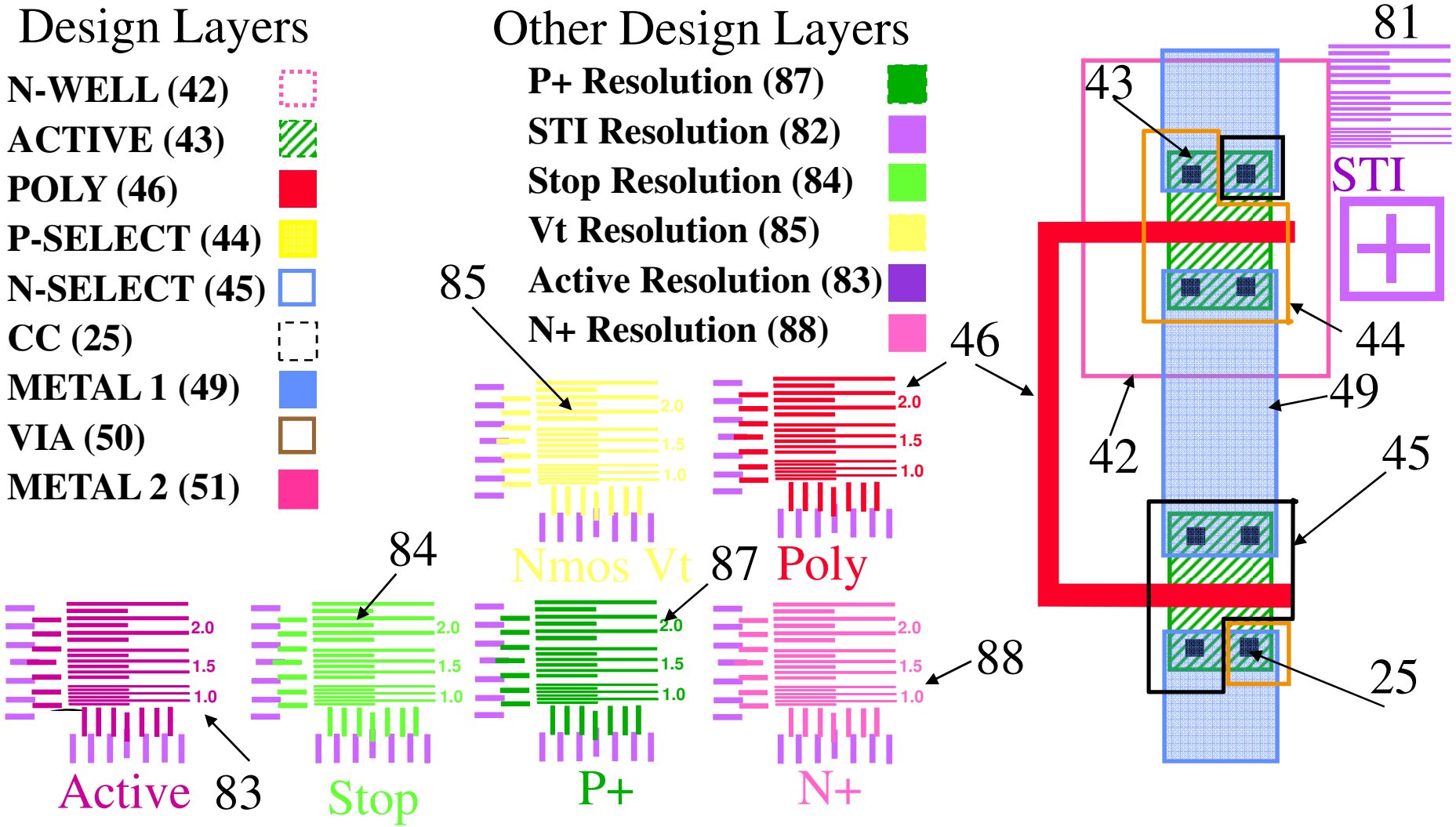
OTHER LAYERS

Design Layers

- N-WELL (42)
- ACTIVE (43)
- POLY (46)
- P-SELECT (44)
- N-SELECT (45)
- CC (25)
- METAL 1 (49)
- VIA (50)
- METAL 2 (51)

Other Design Layers

- P+ Resolution (87)
- STI Resolution (82)
- Stop Resolution (84)
- Vt Resolution (85)
- Active Resolution (83)
- N+ Resolution (88)

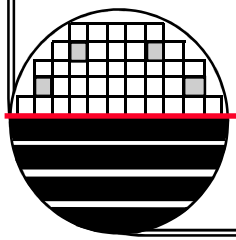


LAMBDA BASED DESIGN RULES

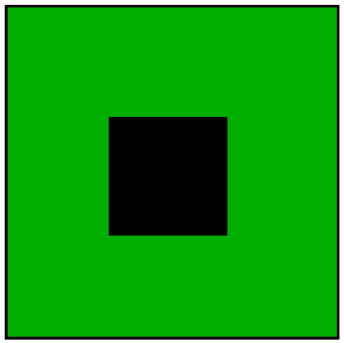
The design rules may change from foundry to foundry or for different technologies. So to make the design rules generic the sizes, separations and overlap are given in terms of numbers of lambda (λ). The actual size is found by multiplying the number by the value for lambda for that specific foundry.

For example:

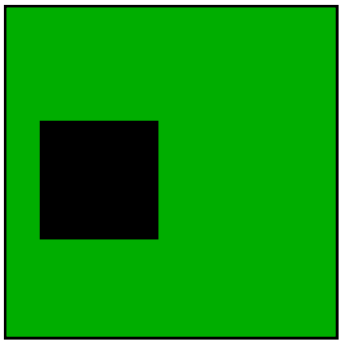
RIT PMOS process λ = 10 μm and minimum metal width is 3 λ so that gives a minimum metal width of 30 μm. The RIT SUB-CMOS process has λ = 0.5 μm and the minimum metal width is also 3 λ so minimum metal is 1.5 μm but if we send our CMOS designs out to industry λ might be 0.25 μm so the minimum metal of 3 λ corresponds to 0.75 μm. In all cases the design rule is the minimum metal width = 3 λ



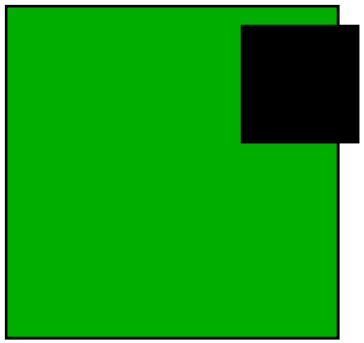
LAYOUT RULES



Perfect Overlay



Slight Overlay
Not Fatal

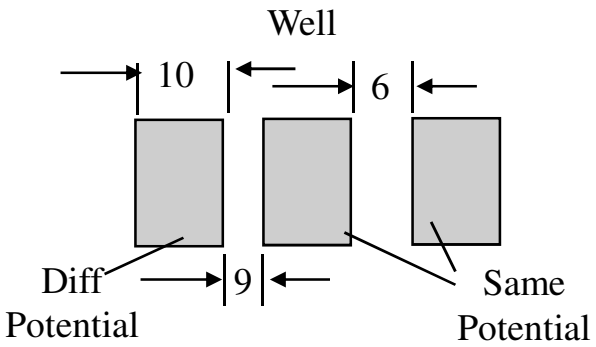


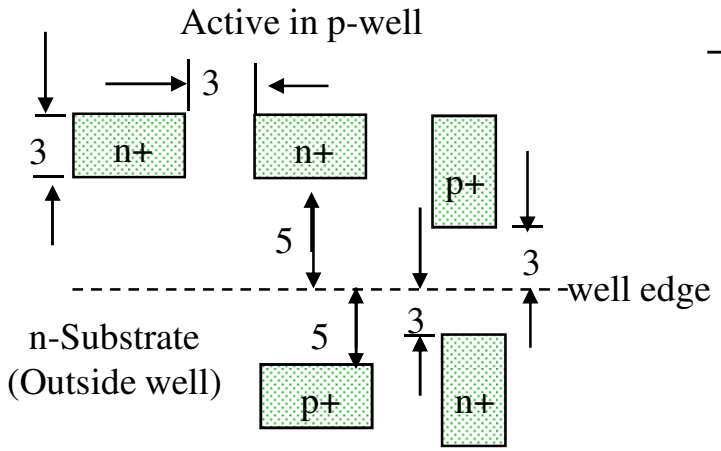
Misalignment
Fatal

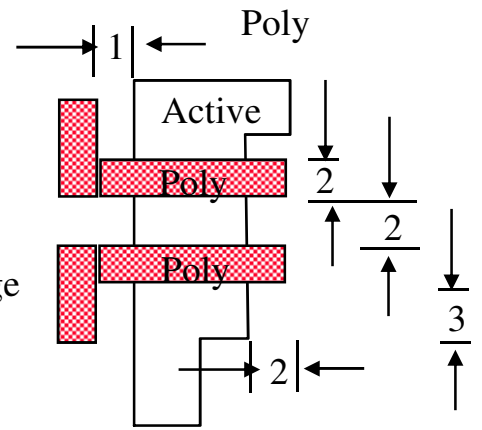
Layout rules prevent slight misalignment from being fatal.

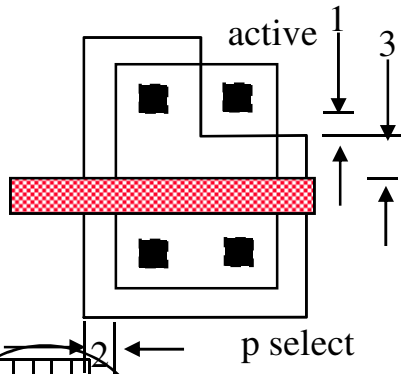
MOSIS LAMBDA BASED DESIGN RULES

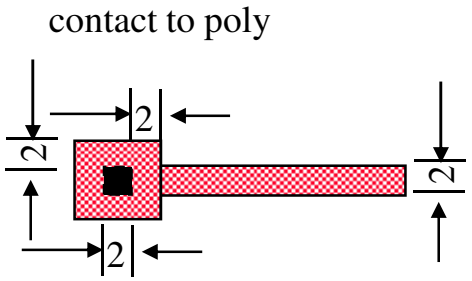
http://www.mosis.com/design/rules/

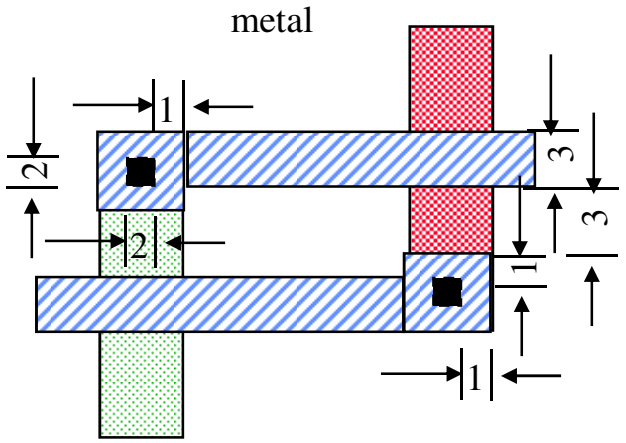








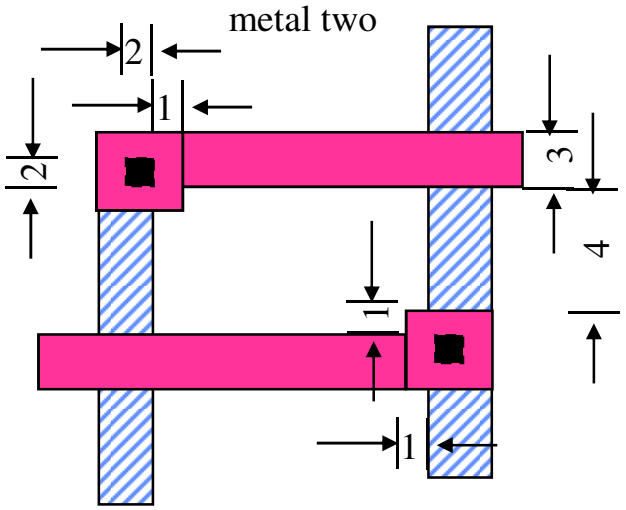




If λ = 1 µm then contact is 2 µm x 2 µm

MOSIS LAMBDA BASED DESIGN RULES

http://www.mosis.com/design/rules/



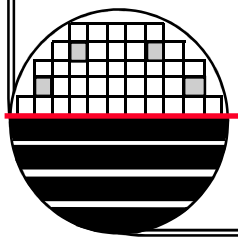
MOSIS Educational Program

Instructional Processes Include:
AMI $\lambda = 0.8\ \mu m$ SCMOS Rules
AMI $\lambda = 0.35\ \mu m$ SCMOS Rules

Research Processes:
go down to poly length of 65nm

MOSIS REQUIREMENTS

MOSIS requires that projects have successfully passed LVS (Layout Versus Schematic) and DRC (Design Rule Checking). Our MENTOR tools for LVS and DRC (as they are set up) require separate N-select and P-select levels in order to know an NMOS transistor from a PMOS transistor. Although either an N-well, P-well or both will work for a twin well process, we have set up our DRC to look for N-well.



RIT PROCESSES

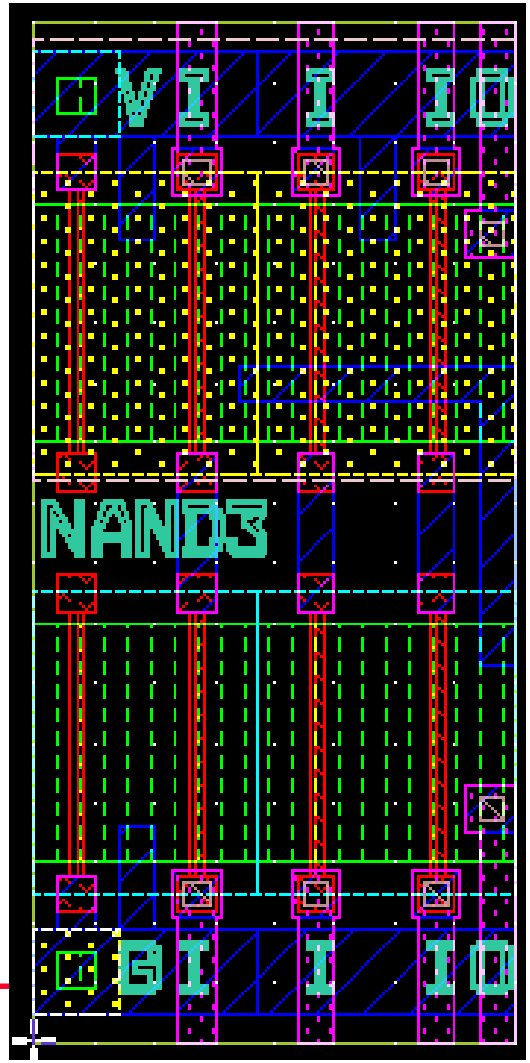
At RIT we use the Sub-CMOS and ADV-CMOS processes for most designs. In these processes the minimum poly length is 1µm and 0.5µm respectively. We use scalable MOSIS design rules with lambda equal to 0.5µm and 0.25µm. These processes use one layer of poly and two layers of metal.

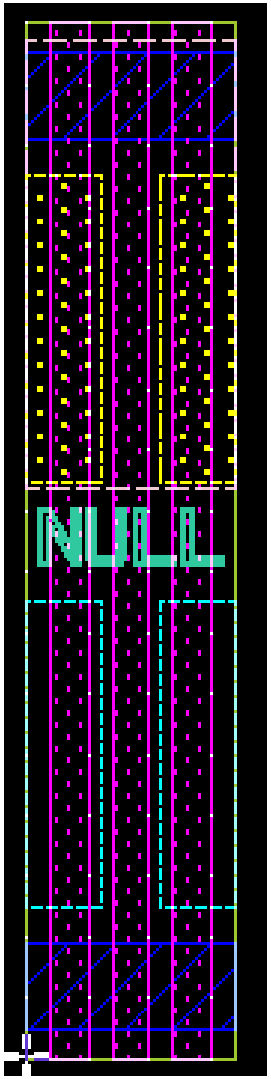
The examples on the following pages are designs that could be made with either of the above processes. As a result the designs are generous, meaning that larger than minimum dimensions are used. For example $\lambda = 0.5\mu m$ and minimum poly is 2λ but designed at 2.5µm because our poly etch is isotropic.

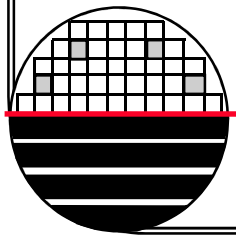
The design approach for digital circuits is to design primitive cells and then use the primitive cells to design basic cells which are then used in the project designs. A layout approach is also used that allows for easy assembly of these cells into more complex cells.

PRIMITIVE CELLS

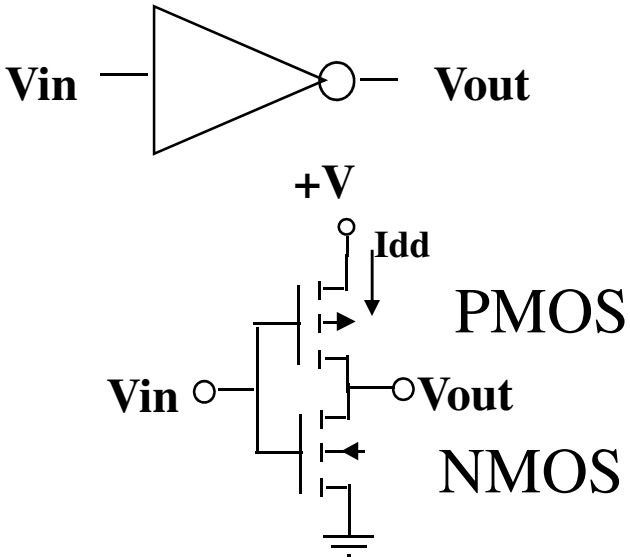
Primitive Cells
- Inverter
- NOR2
- NOR3
- NOR4
- NAND2
- NAND3
- NAND4
- Etc.







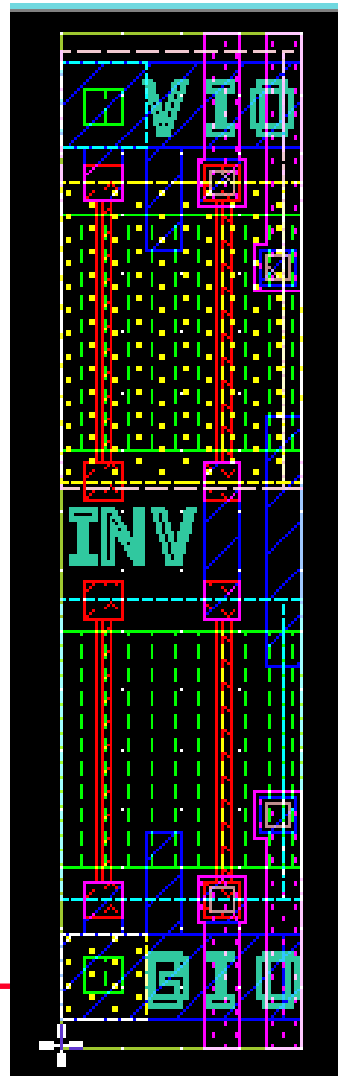
CMOS INVERTER

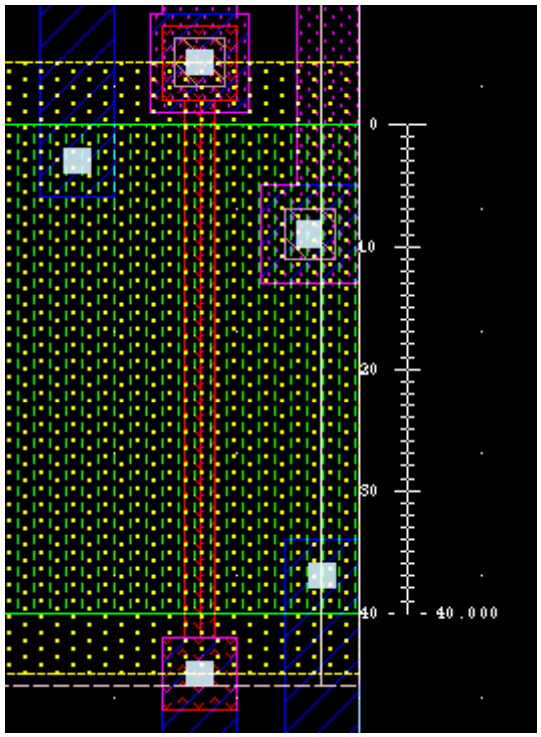


CMOS

TRUTH TABLE

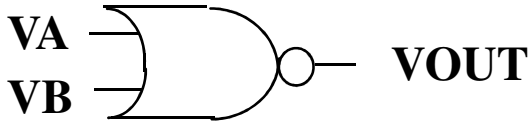
VIN	VOUT
0	1
1	0

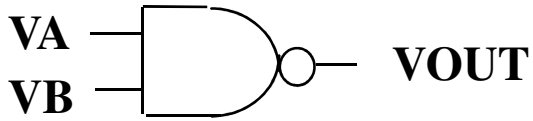




W = 40 µm
Ldrawn = 2.5µm
Lpoly = 1.5µm
Leff = 0.75 µm

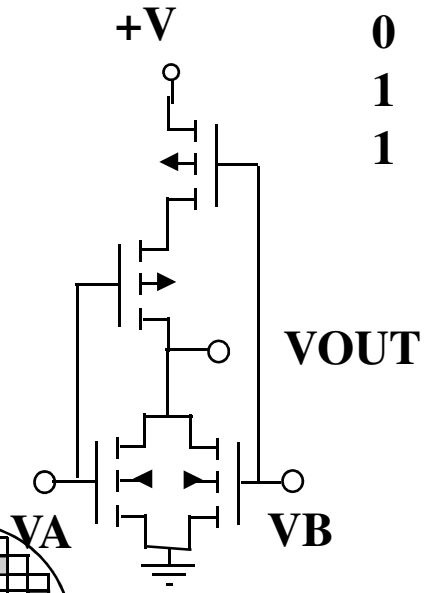
NOR and NAND

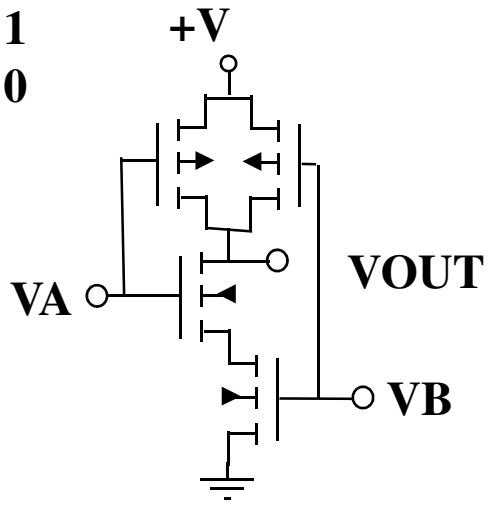




VA	VB	VOUT
0	0	1
0	1	0
1	0	0
1	1	0

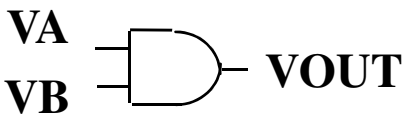
VA	VB	VOUT
0	0	1
0	1	1
1	0	1
1	1	0



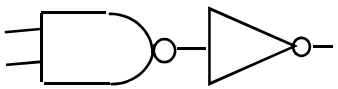


OTHER LOGIC GATES

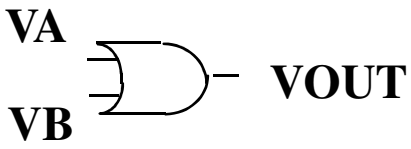
AND



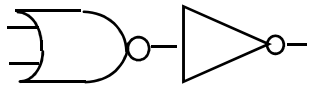
VA	VB	VOUT
0	0	0
0	1	0
1	0	0
1	1	1



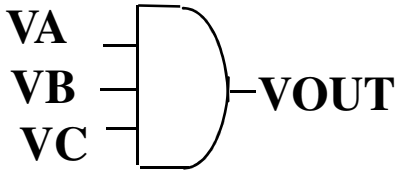
OR



VA	VB	VOUT
0	0	0
0	1	1
1	0	1
1	1	1

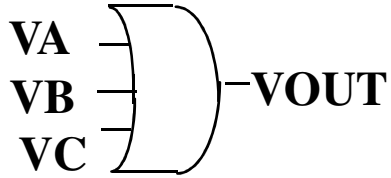


3 INPUT AND



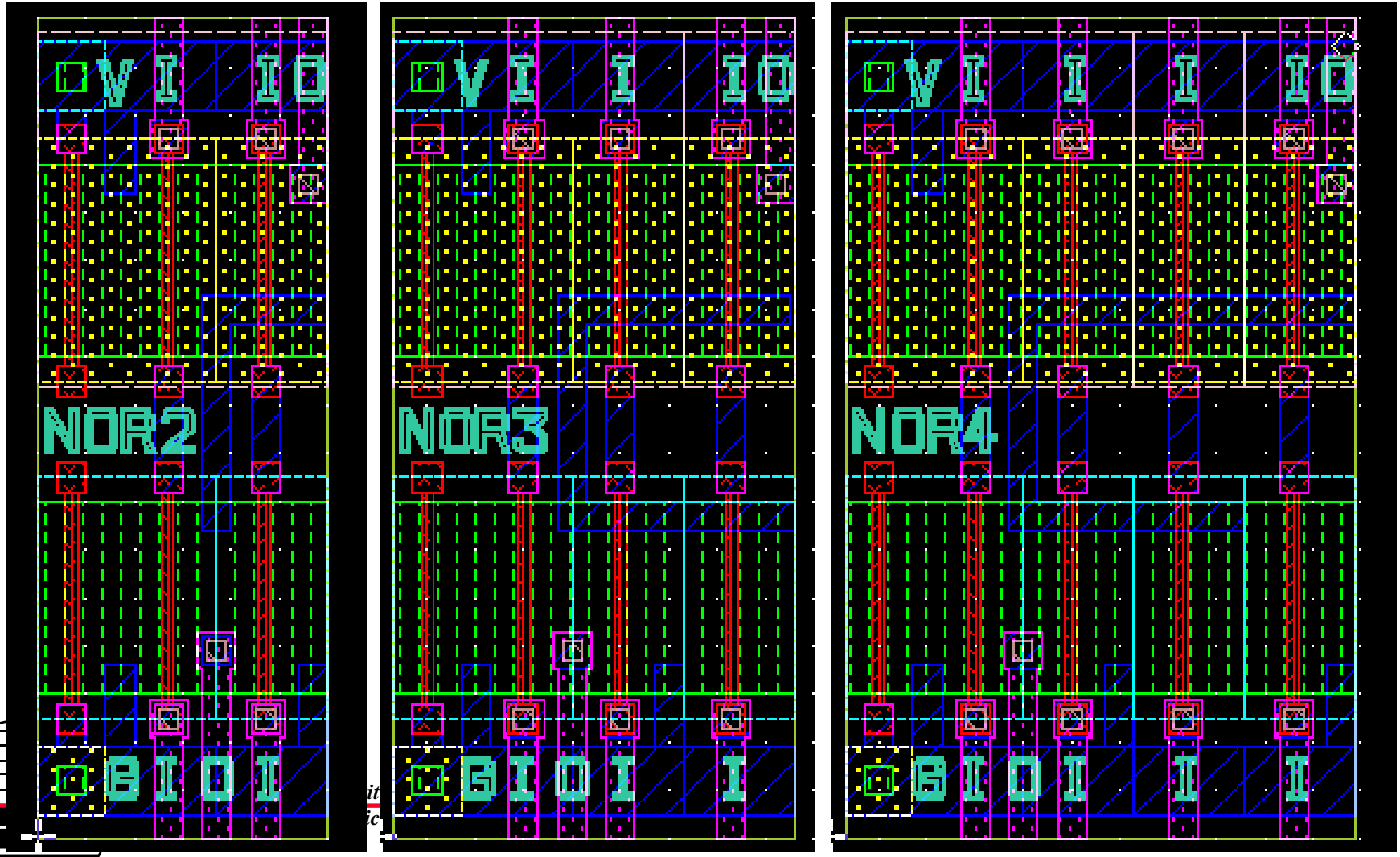
VA	VB	VC	VOUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3 INPUT OR

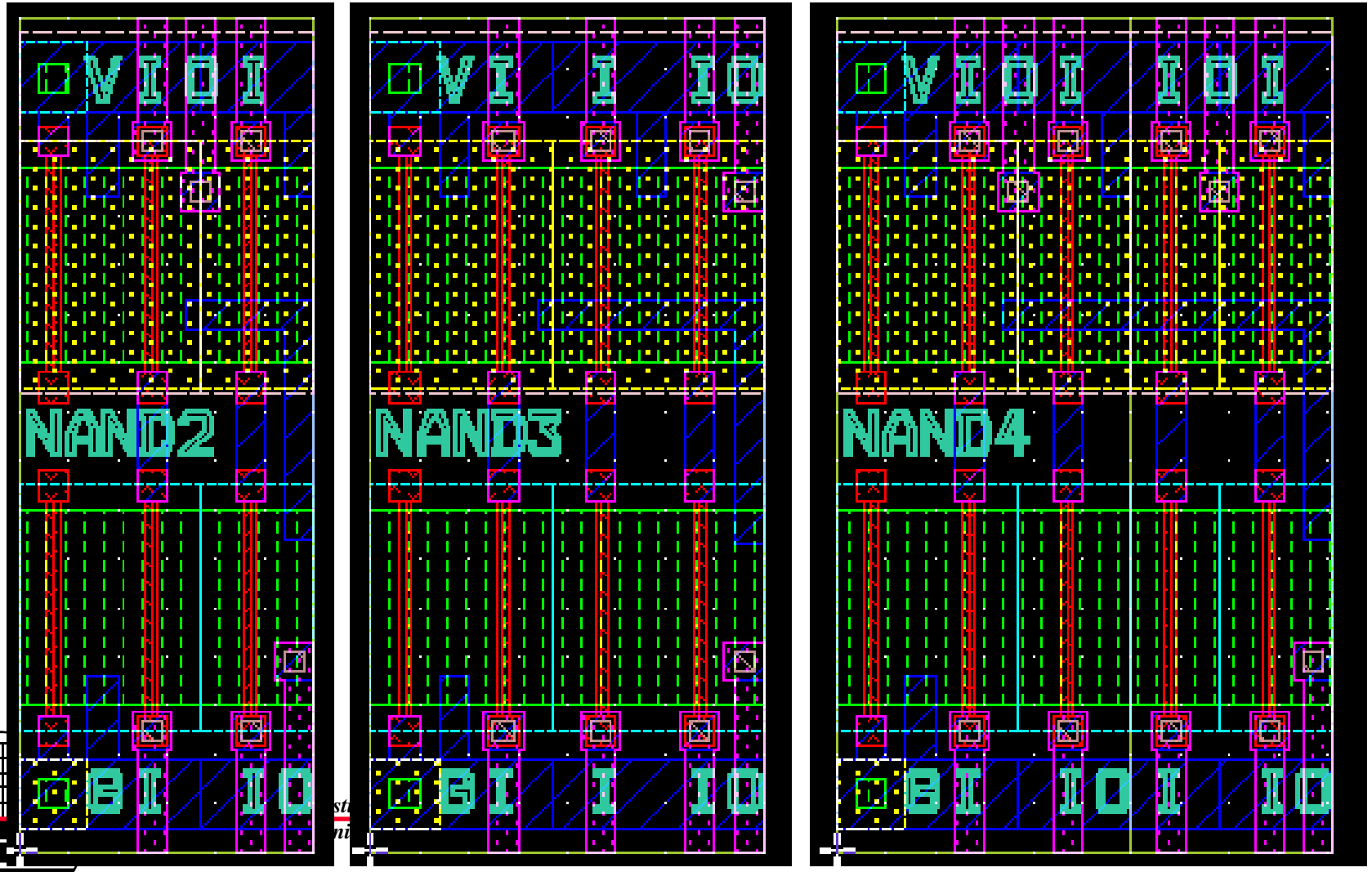


VA	VB	VC	VOUT
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

MORE PRIMITIVE CELLS

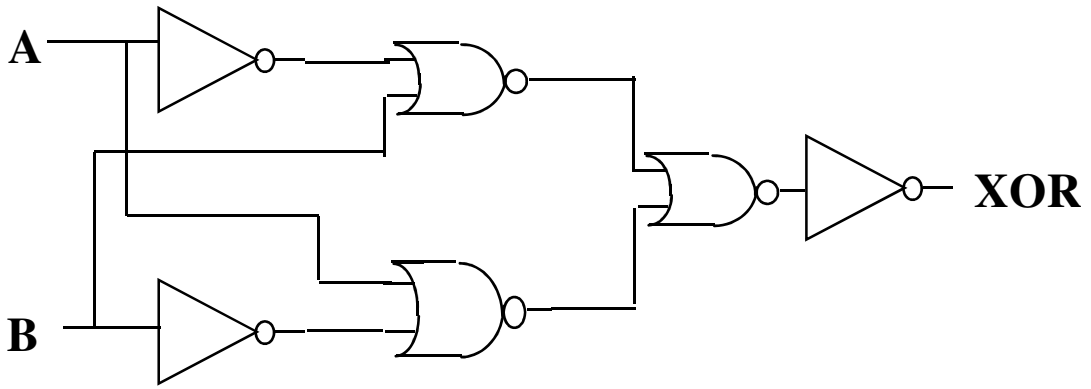


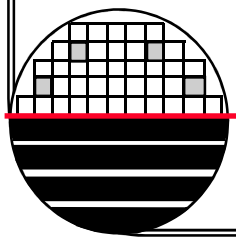
MORE PRIMITIVE CELLS



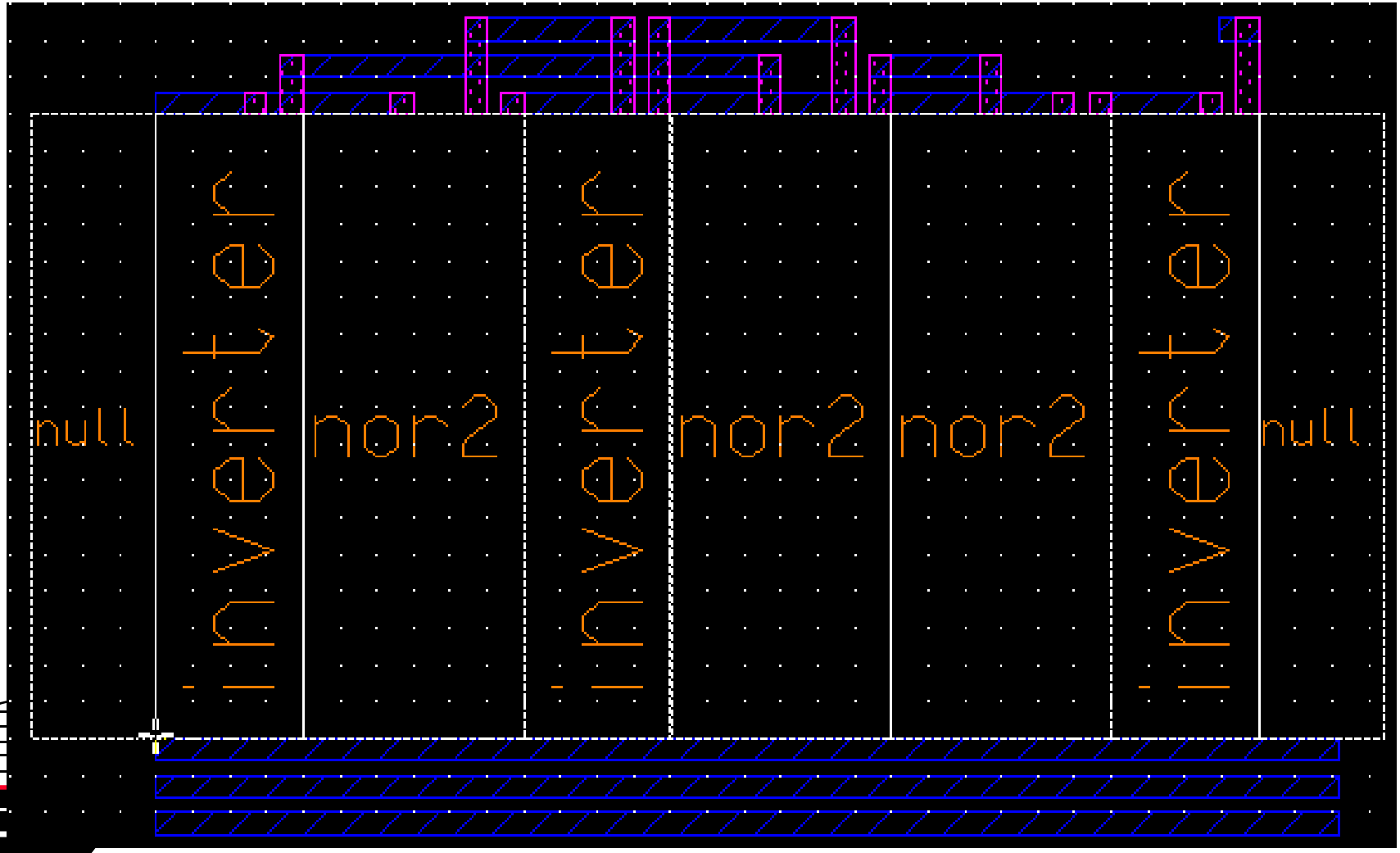
BASIC CELLS

Basic Cells
- XOR
- D FF
- JK FF
- Data Latch

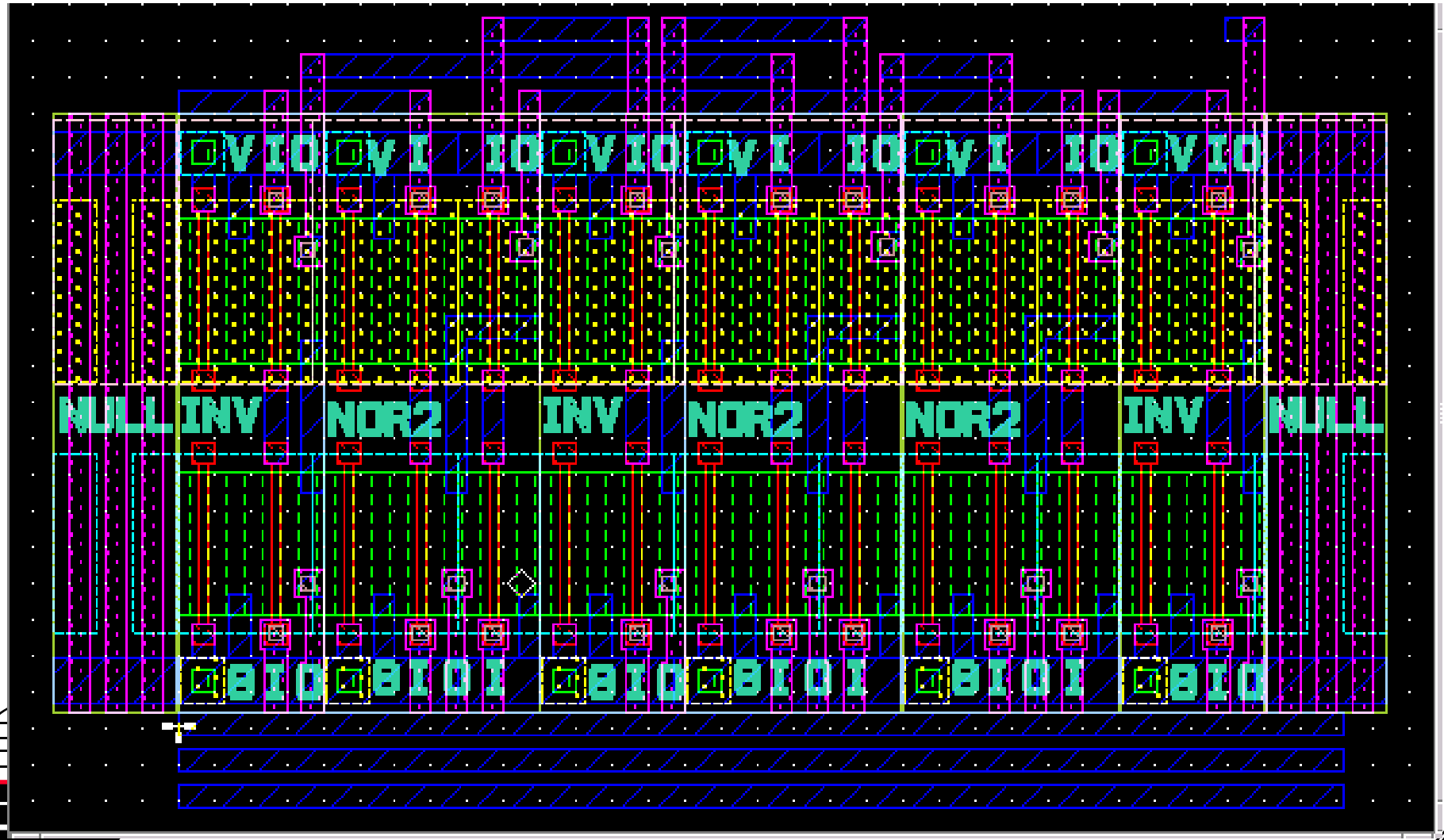




XOR

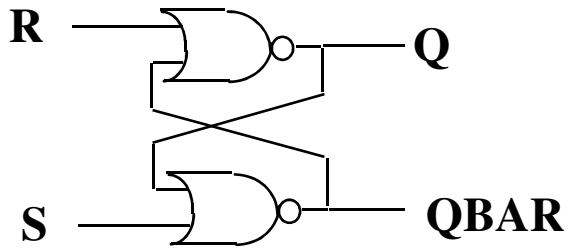


XOR


VIO
VIO
VIO
VIO
VIO
NULL
INV
NOR2
INV
NOR2
NOR2
INV
NULL
BIO
BIO
BIO
BIO
BIO

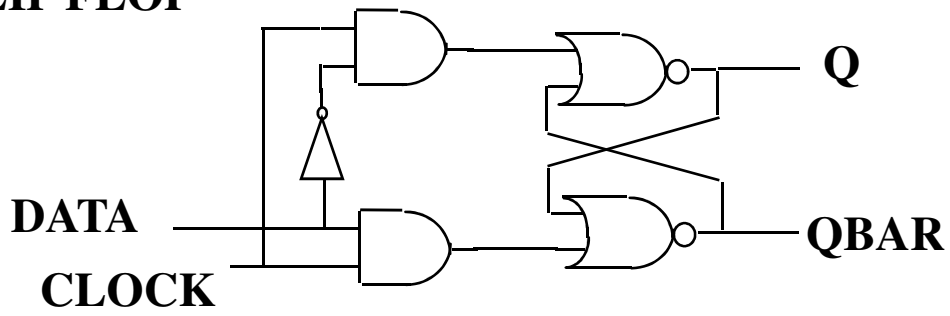
FILP-FLOPS

RS FLIP FLOP



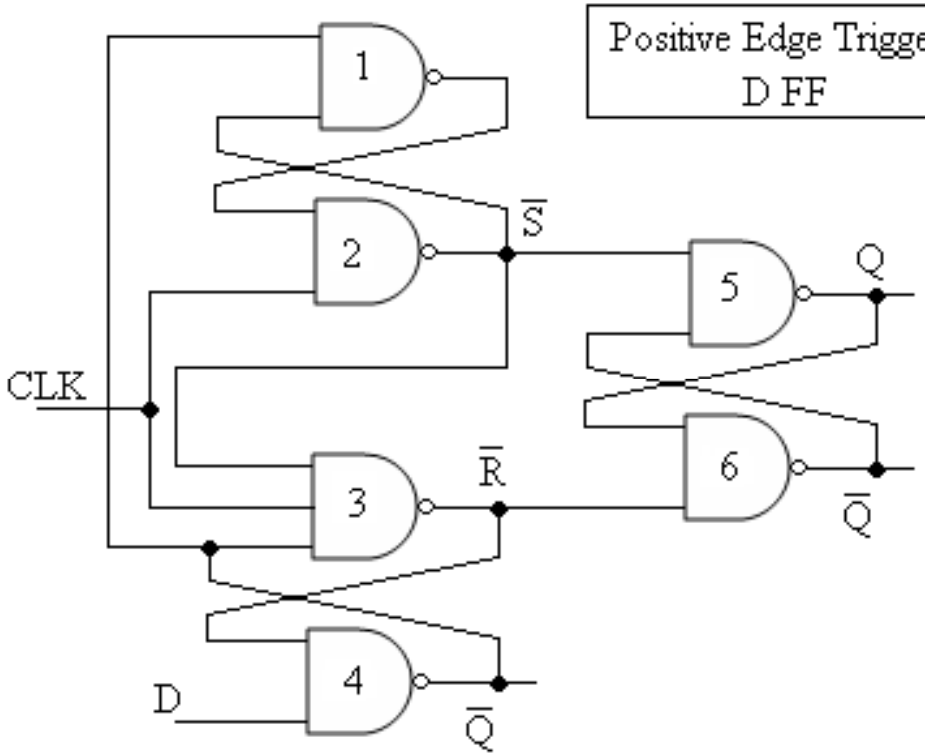
R	S	Q
0	0	Qn-1
0	1	1
1	0	0
1	1	INDETERMINATE

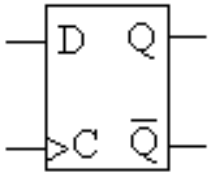
D FLIP FLOP



Q=DATA IF CLOCK IS HIGH
IF CLOCK IS LOW Q=PREVIOUS DATA VALUE

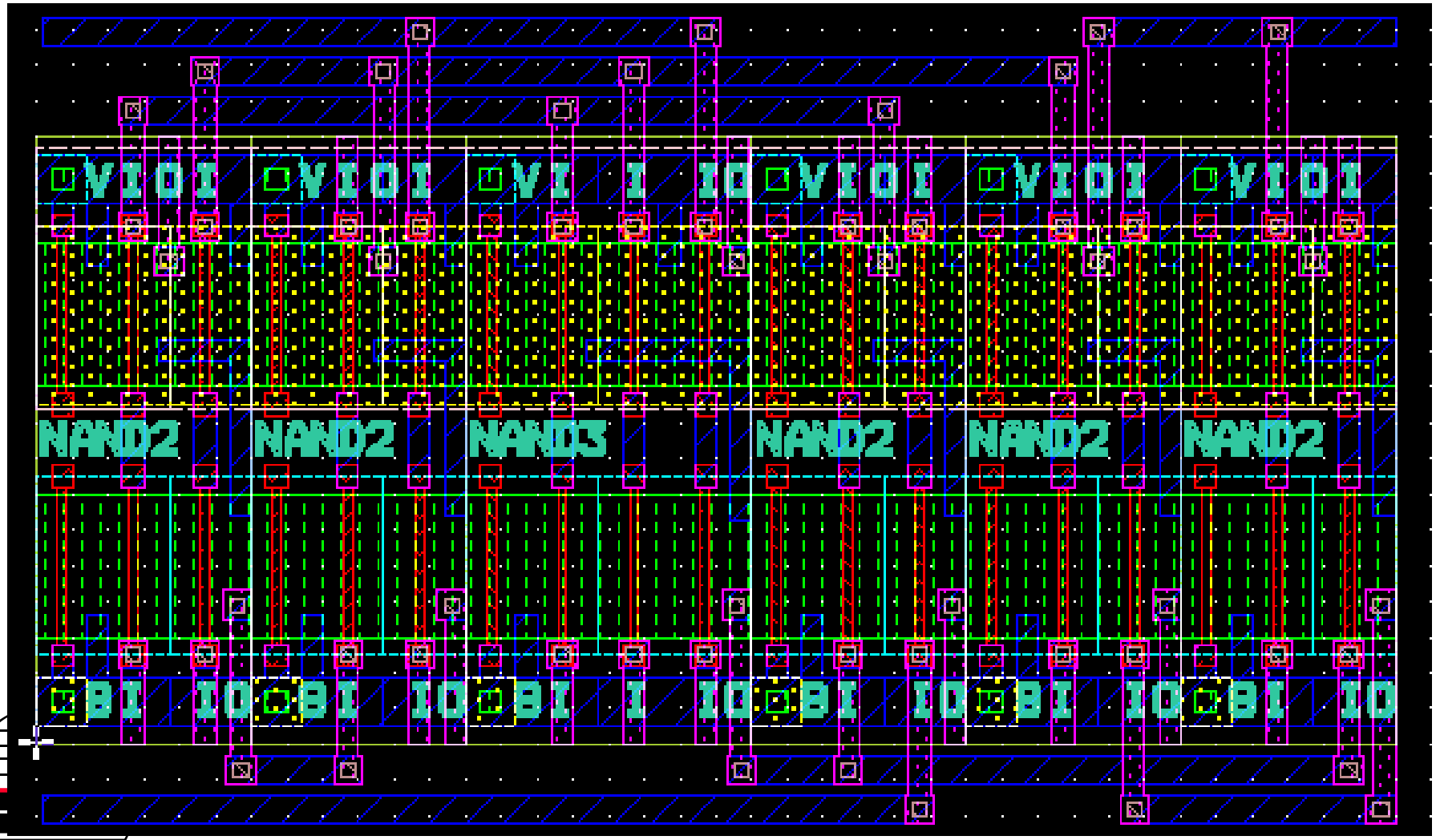
EDGE TRIGGERED D FLIP FLOP





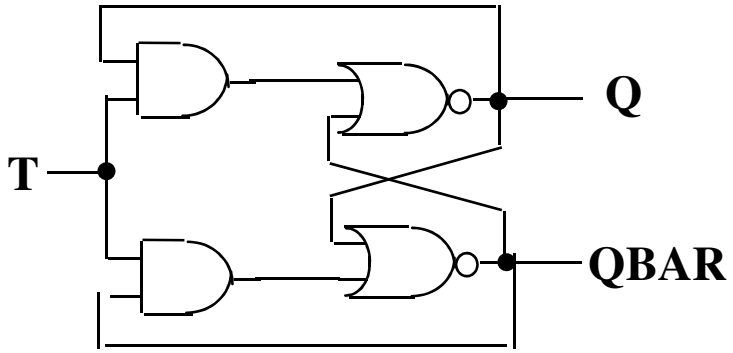
Inputs		Outputs	
D	C	Q^+	$\overline{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\overline{Q}$
X	1	Q	$\overline{Q}$

EDGE TRIGGERED D FLIP FLOP



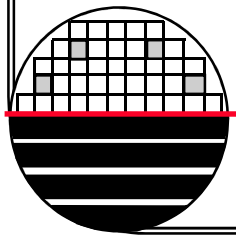
T FLIP FLOP

TOGGEL FLIP FLOP

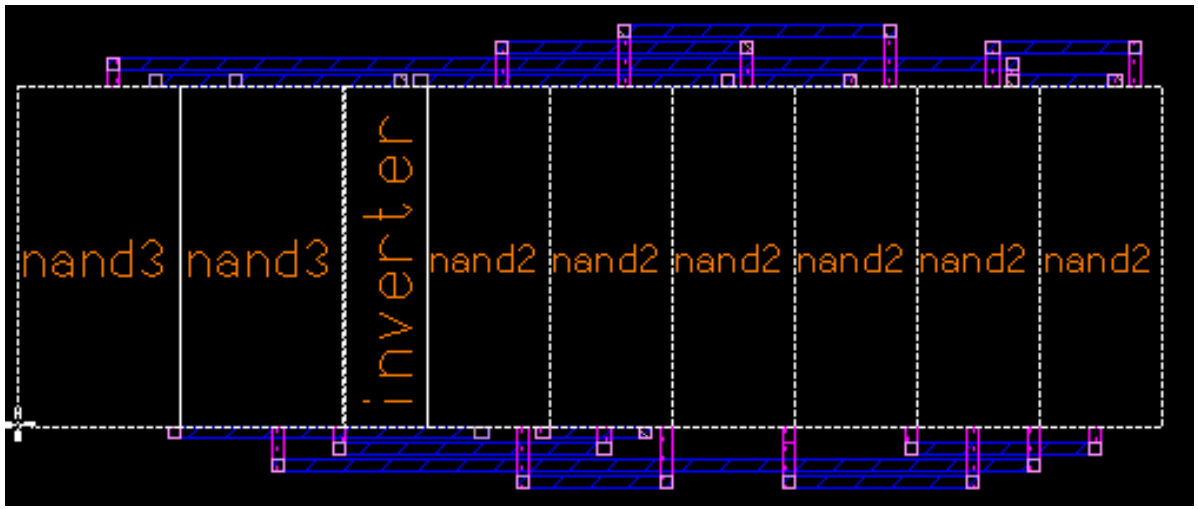


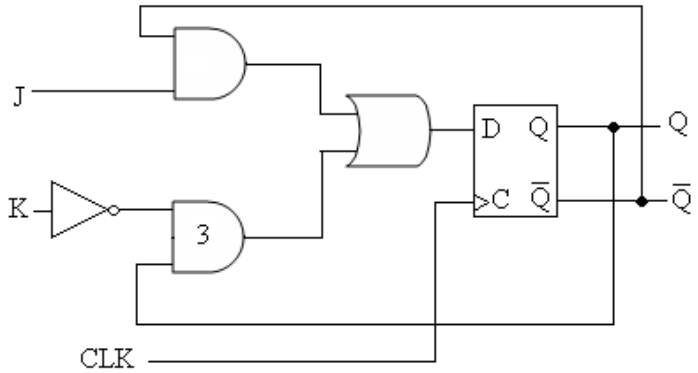
T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

Q: TOGGELS HIGH AND LOW WITH EACH INPUT

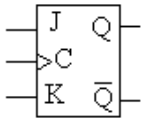


JK FLIP FLOP





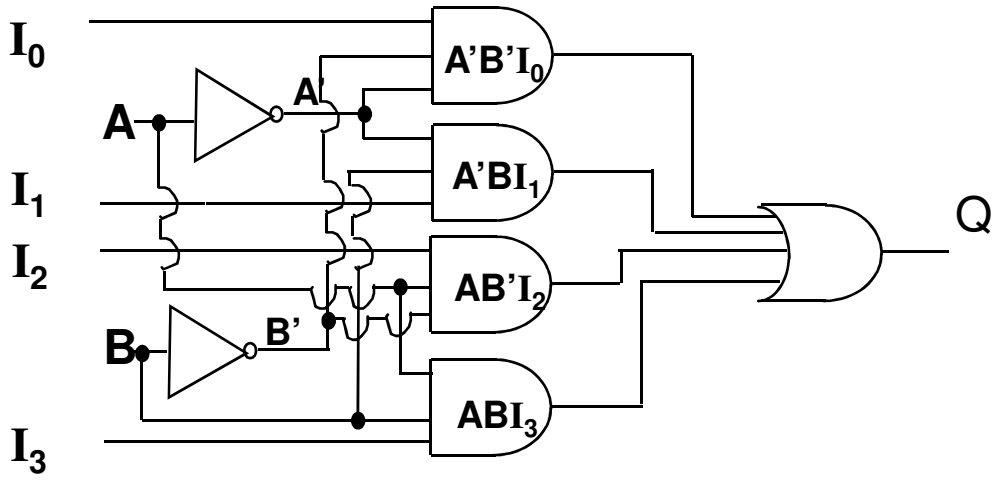
Positive Edge Triggered JK FF



Inputs			Outputs	
J	K	C	Q^+	$\overline{Q^+}$
0	0	↑	Q	$\overline{Q}$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\overline{Q}$	Q
X	X	0	Q	$\overline{Q}$
X	X	1	Q	Q

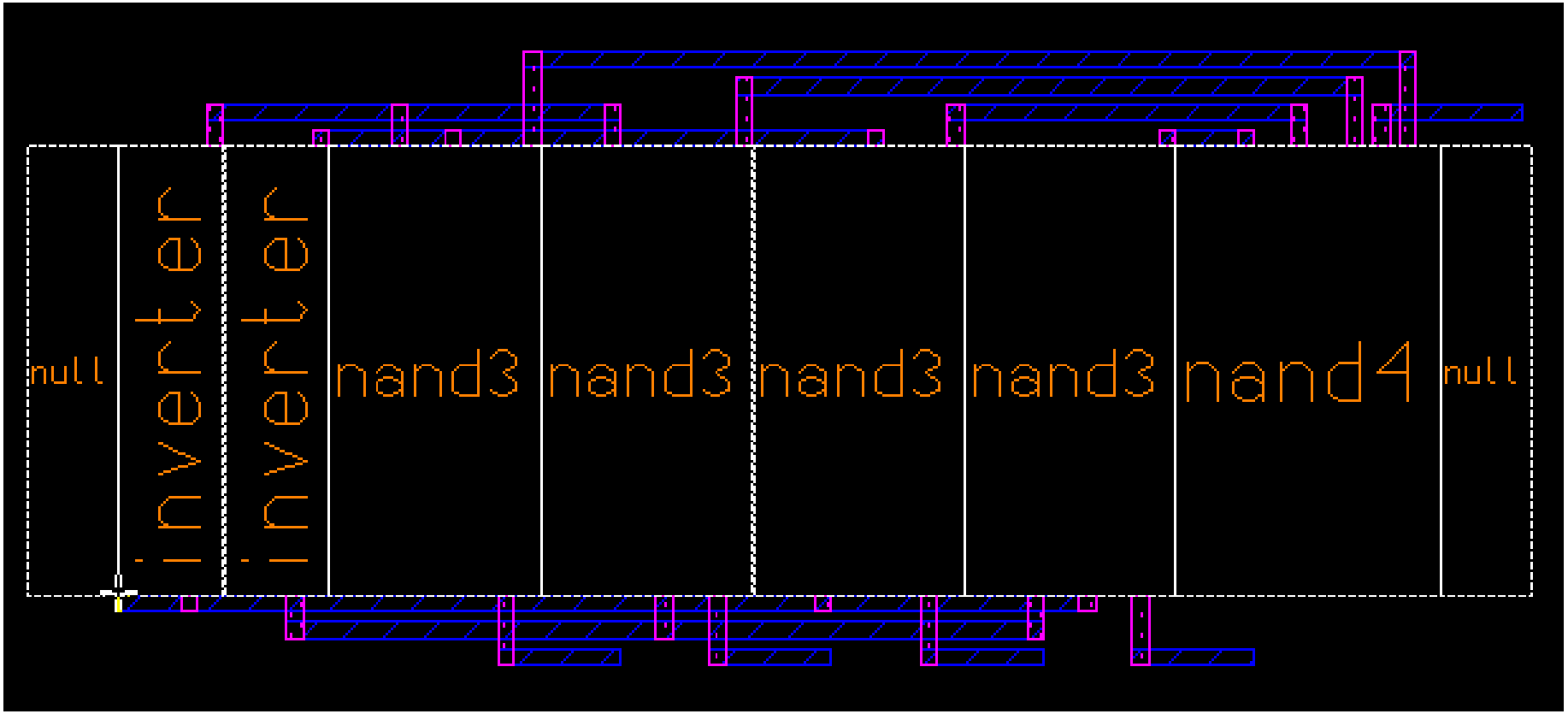
PROJECTS

Multiplexer
Full Adder
Binary Counter



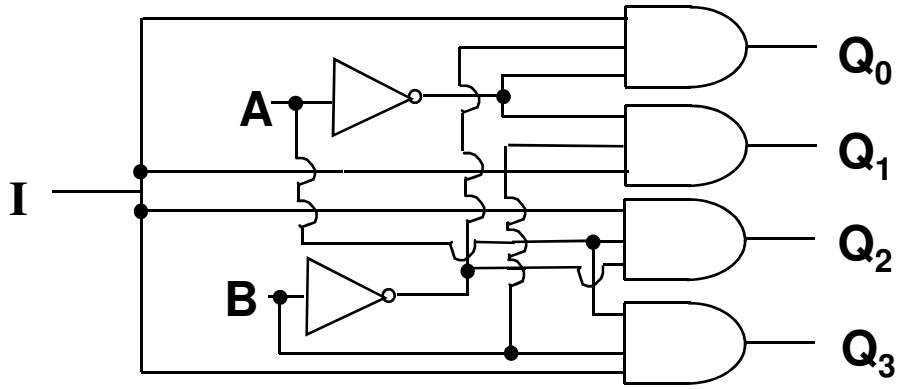
4:1 Multiplexer

MULTIPLEXER



DE MULTIPLEXER

De-multiplexer



$Q_0 = A'B'I$

so that when I=0 Q_0 =0

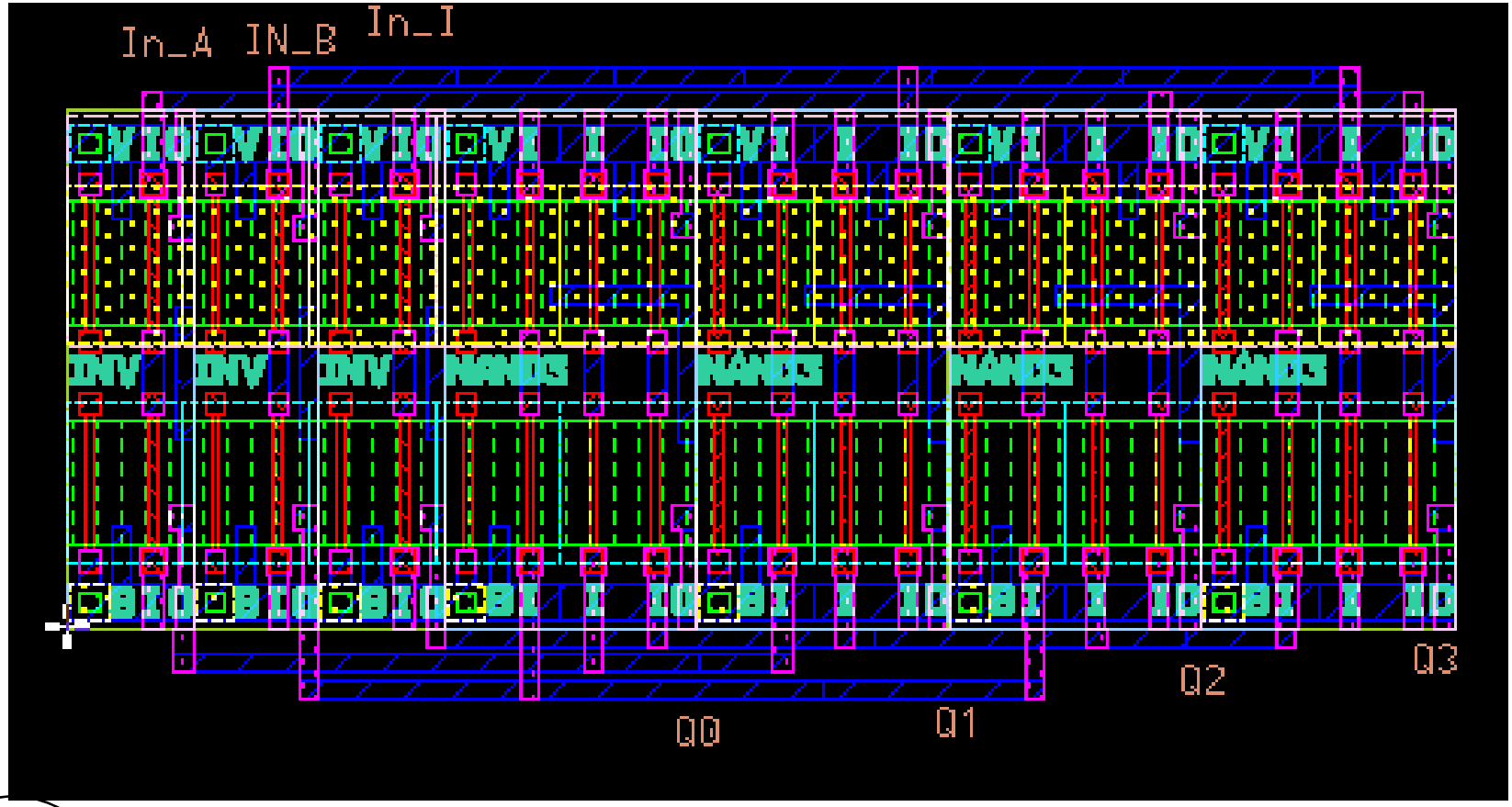
or when I=1 Q_0 = 1

similarly for Q_1, Q_2 and Q_3

$Q_1 = A'BI$

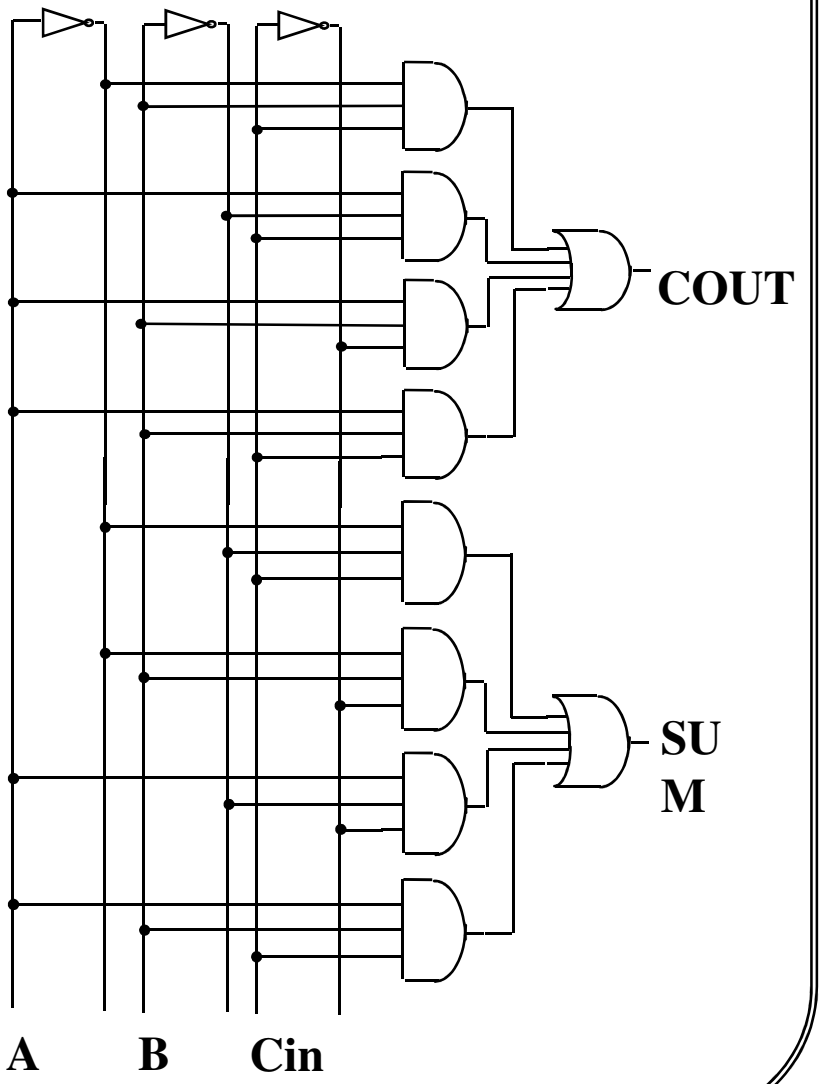
INPUTS		OUTPUTS			
A	B	Q_0	Q_1	Q_2	Q_3
0	0	I	0	0	0
0	1	0	I	0	0
1	0	0	0	I	0
1	1	0	0	0	I

DE MULTIPLEXER

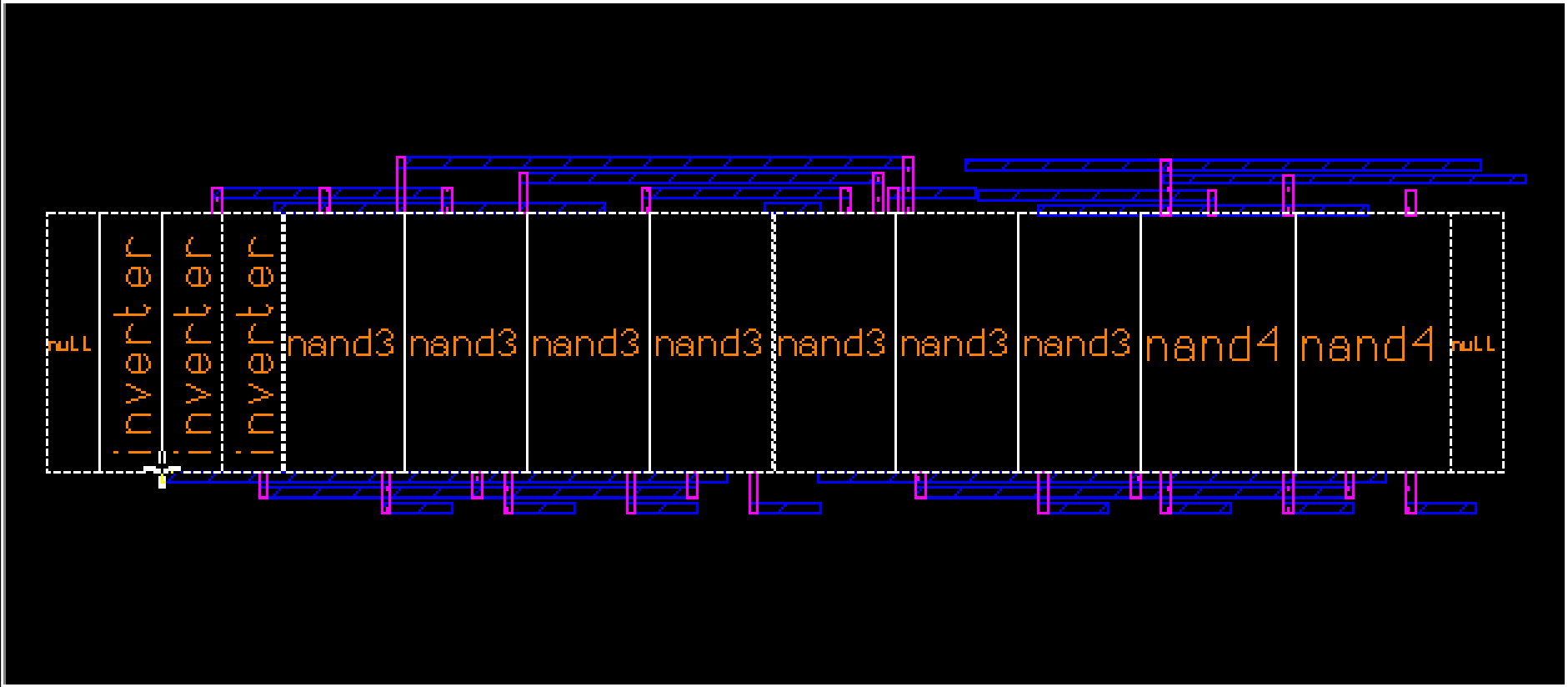


FULL ADDER

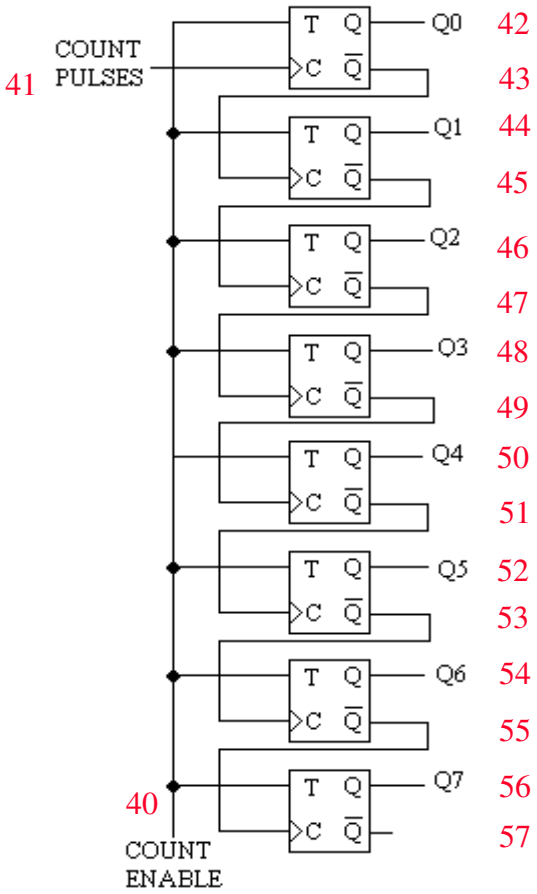
A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



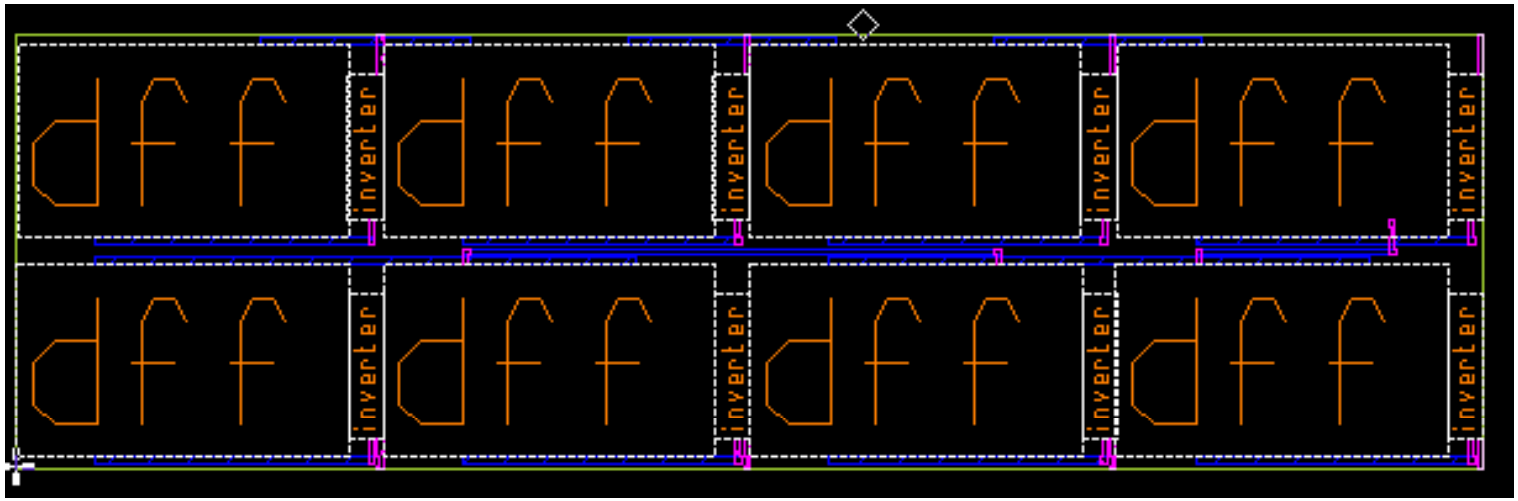
FULL ADDER

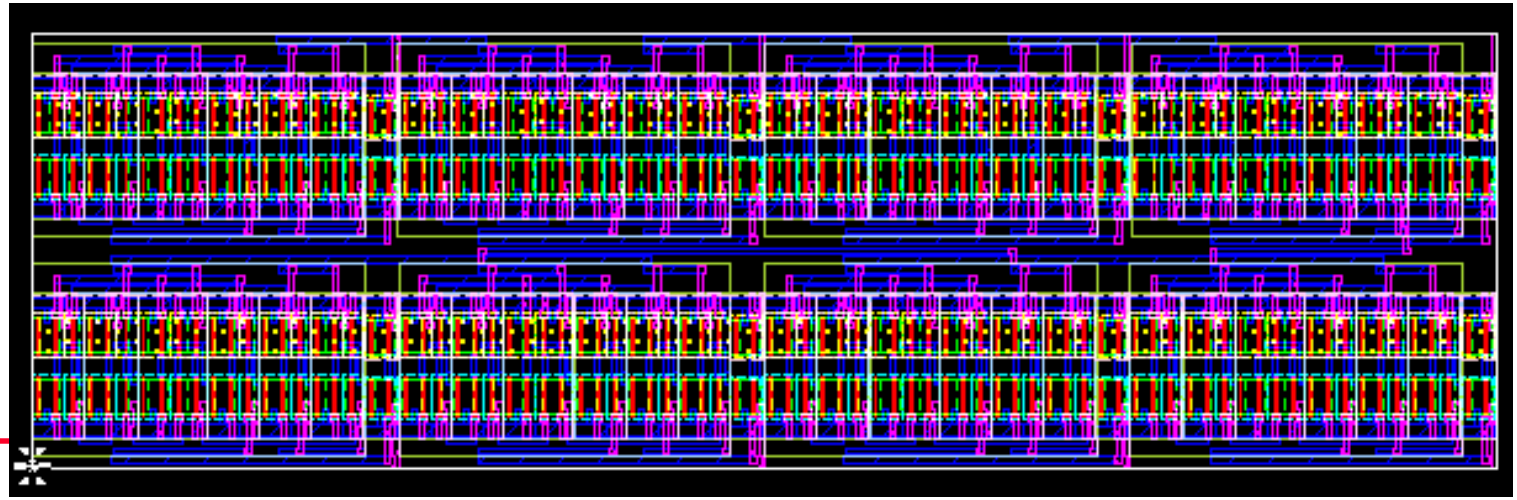

FULL
inverter
inverter
inverter
nand3
nand3
nand3
nand3
nand3
nand3
nand3
nand4
nand4
FULL

8-BIT BINARY COUNTER



8-BIT BINARY COUNTER



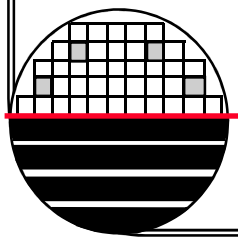


FILE FORMATS

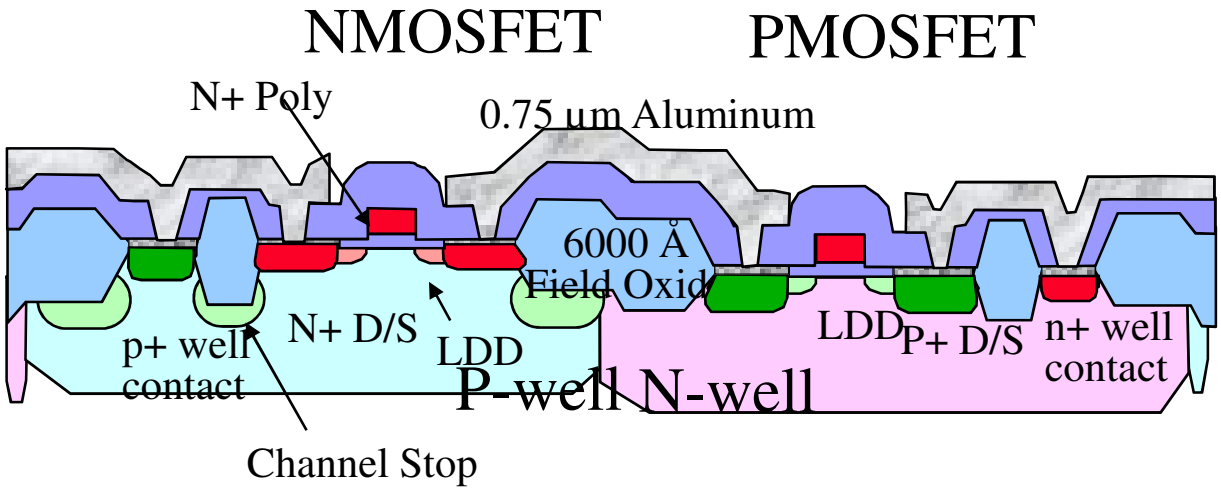
Mentor- ICGraph files (filename.iccel), all layers, polygons with up to 200 vertices

GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

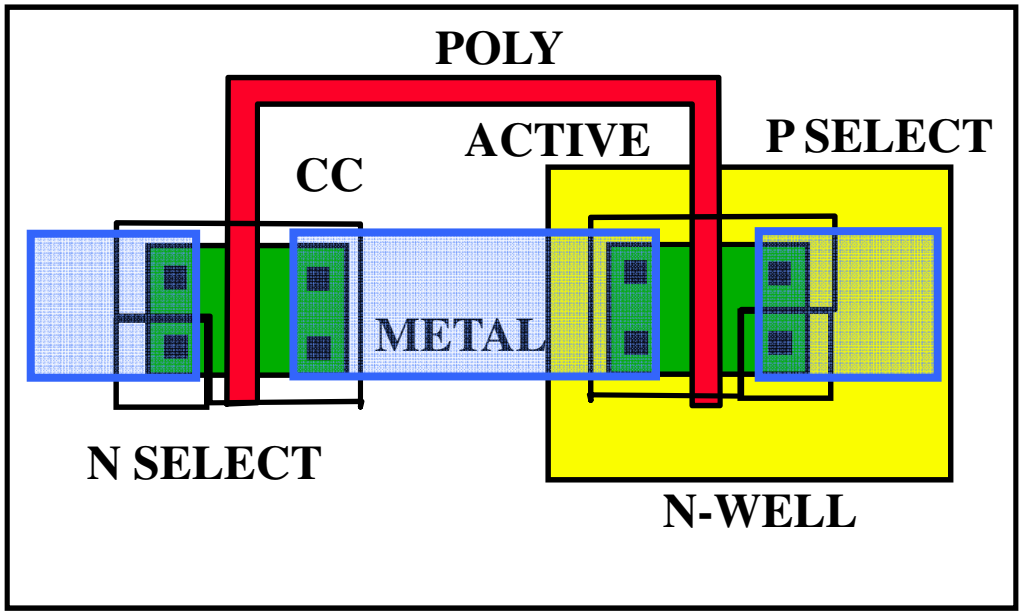
MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only

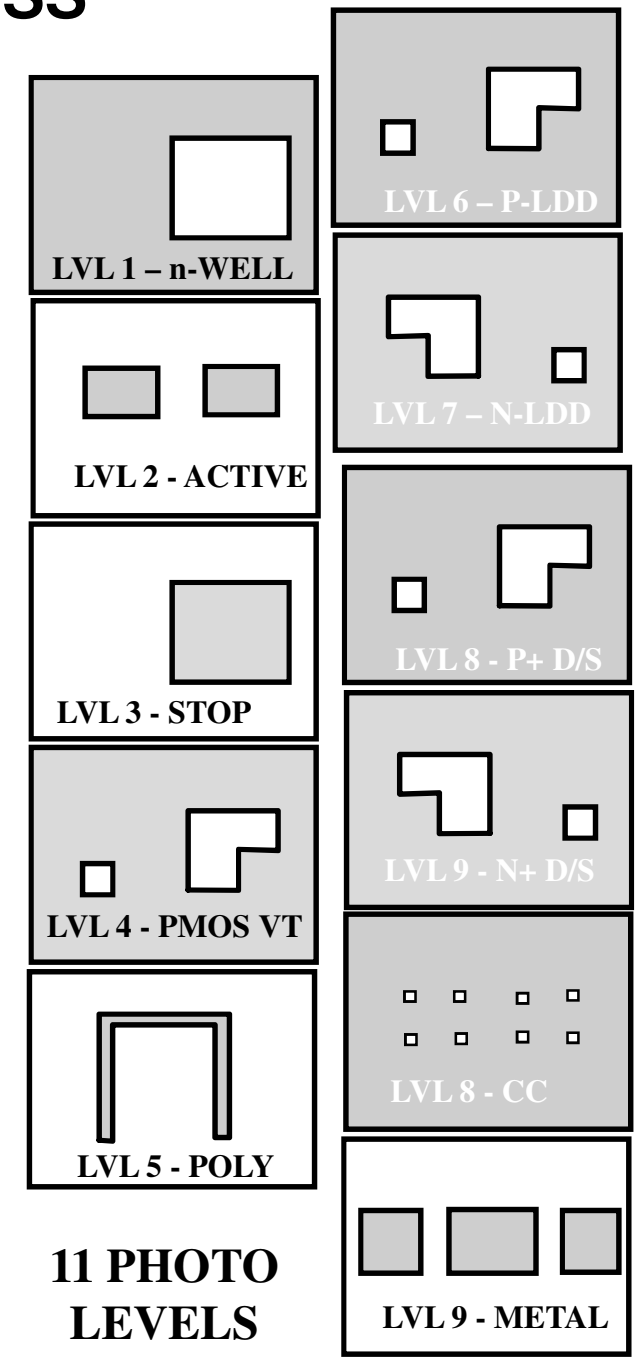


RIT SUB-CMOS PROCESS



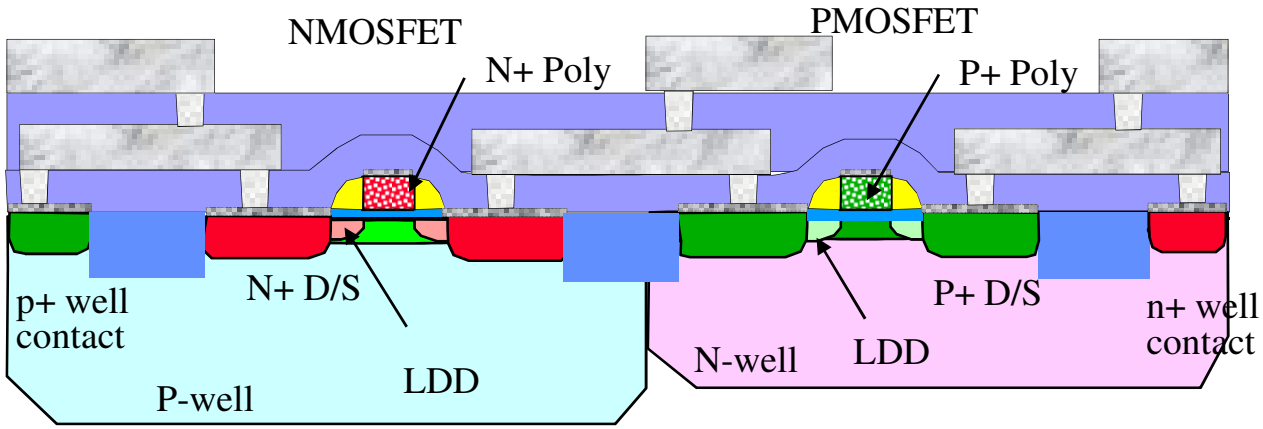
N-type Substrate 10 ohm-cm



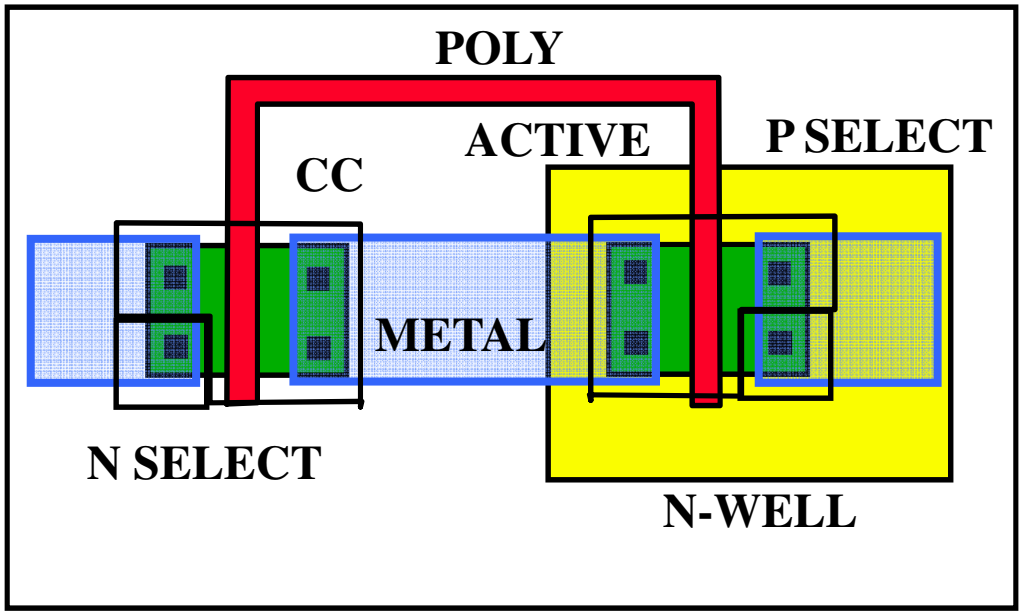


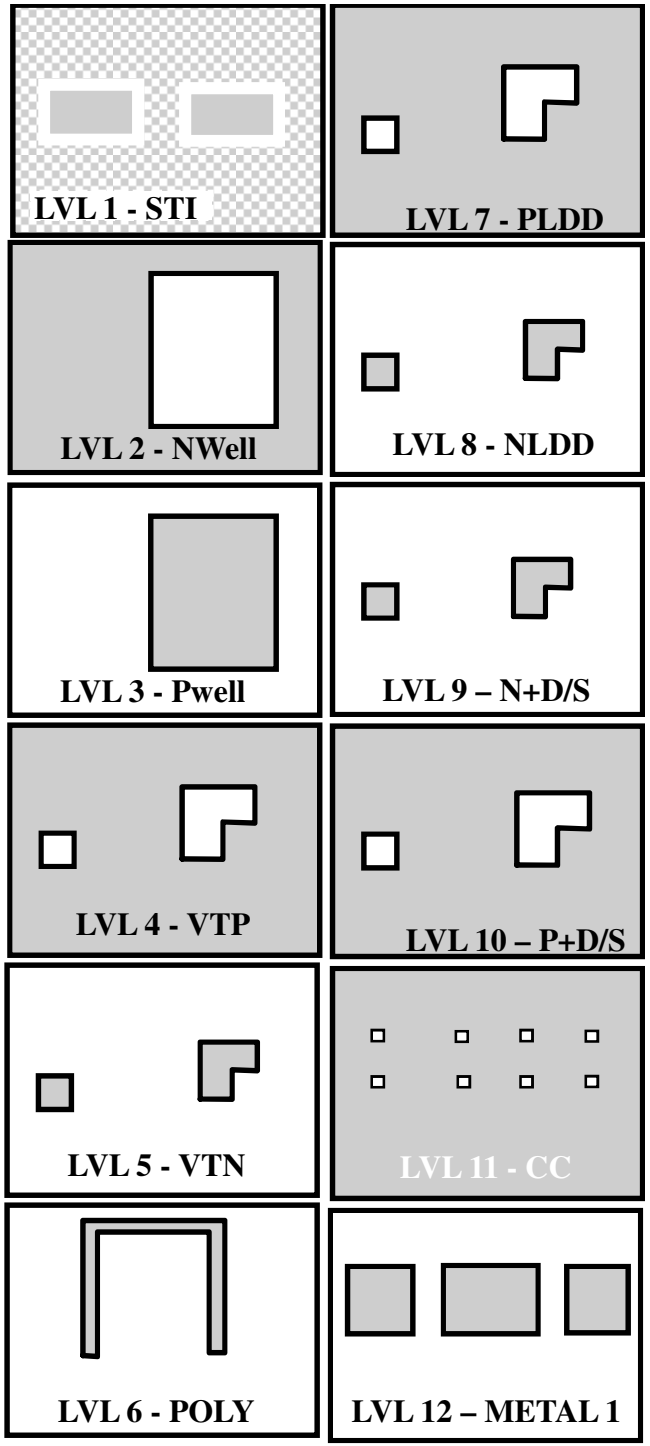
11 PHOTO LEVELS

RIT ADVANCED CMOS



12 PHOTO LEVELS + 2 FOR EACH ADDITIONAL METAL LAYER





OTHER MASKMAKING FEATURES

Fiducial Marks-marks on the edge of the mask used to align the mask to the stepper

Barcodes

Titles

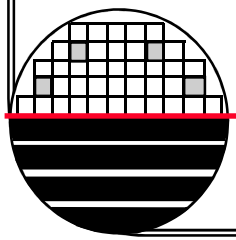
Alignment Keys- marks on the die from a previous level used to align the wafer to the stepper

CD Resolution Targets- lines and spaces

Overlay Verniers- structures that allow measurement of x and y overlay accuracy

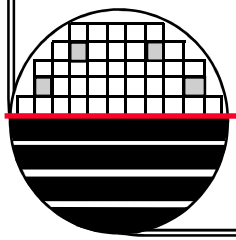
Tiling

Optical Proximity Correction (OPC)



REFERENCES

1. Silicon Processing for the VLSI Era, Volume 1 – Process Technology, 2nd, S. Wolf and R.N. Tauber, Lattice Press.
2. The Science and Engineering of Microelectronic Fabrication, Stephen A. Campbell, Oxford University Press, 1996.
3. MOSIS Scalable CMOS Design Rules for Generic CMOS Processes, www.mosis.org, and http://www.mosis.com/design/rules/



HOMEWORK - CMOS VLSI DESIGN

1. Sketch and label the seven layout layers of a CMOS 2-input OR gate that uses the MOSIS lambda based design rules and uses minimum area. Calculate the area of the smallest rectangle to enclose the design in μm^2 .
2. What lithographic layers are not drawn by the designer in the Adv-CMOS process? How are they created?
3. For the SUB-CMOS layout shown below sketch the crossection A-A' just after level 5 lithography.
4. Does the designer put the alignment marks, fiducial marks, barcode, resolution and overlay features on the design?