ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

CMOS Integrated Circuit Test Results

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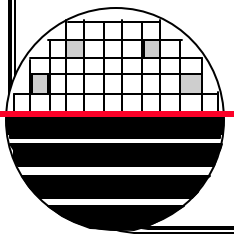
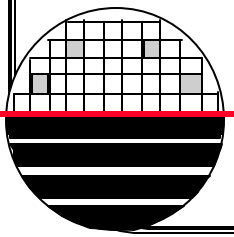
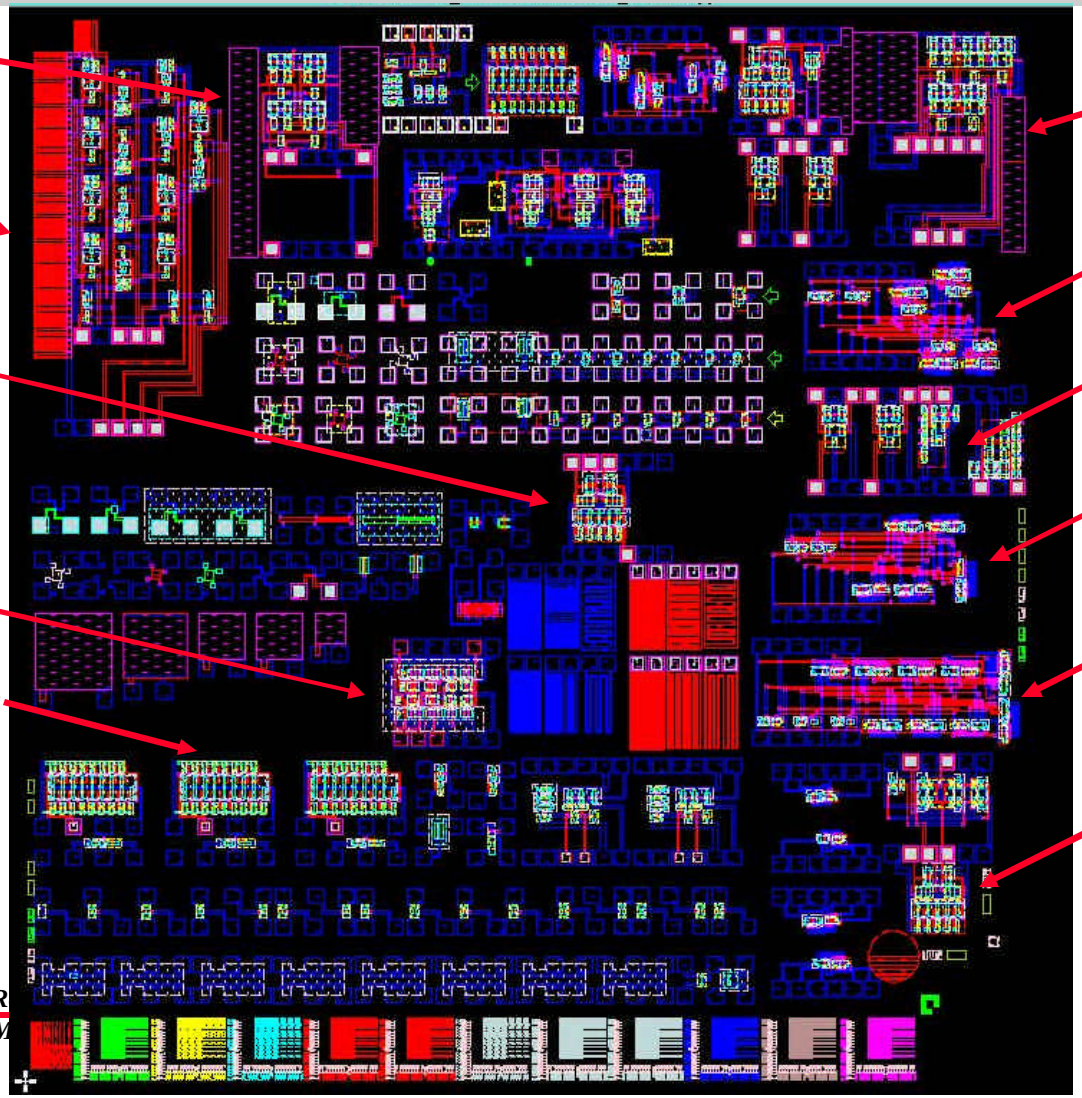


OUTLINE

Layout
Summary of Completed Factory Wafers
Ring Oscillator
Operational Amplifier
Two Phase Non-Overlapping Clock
2-Input NAND
2-Input NOR
3-Input NAND
3-Input NOR
Full Adder
1 to 4 DeMUX
4 to 1 MUX
Voltage Doubler



MIXED ANALOG DIGITAL CMOS TESTCHIP



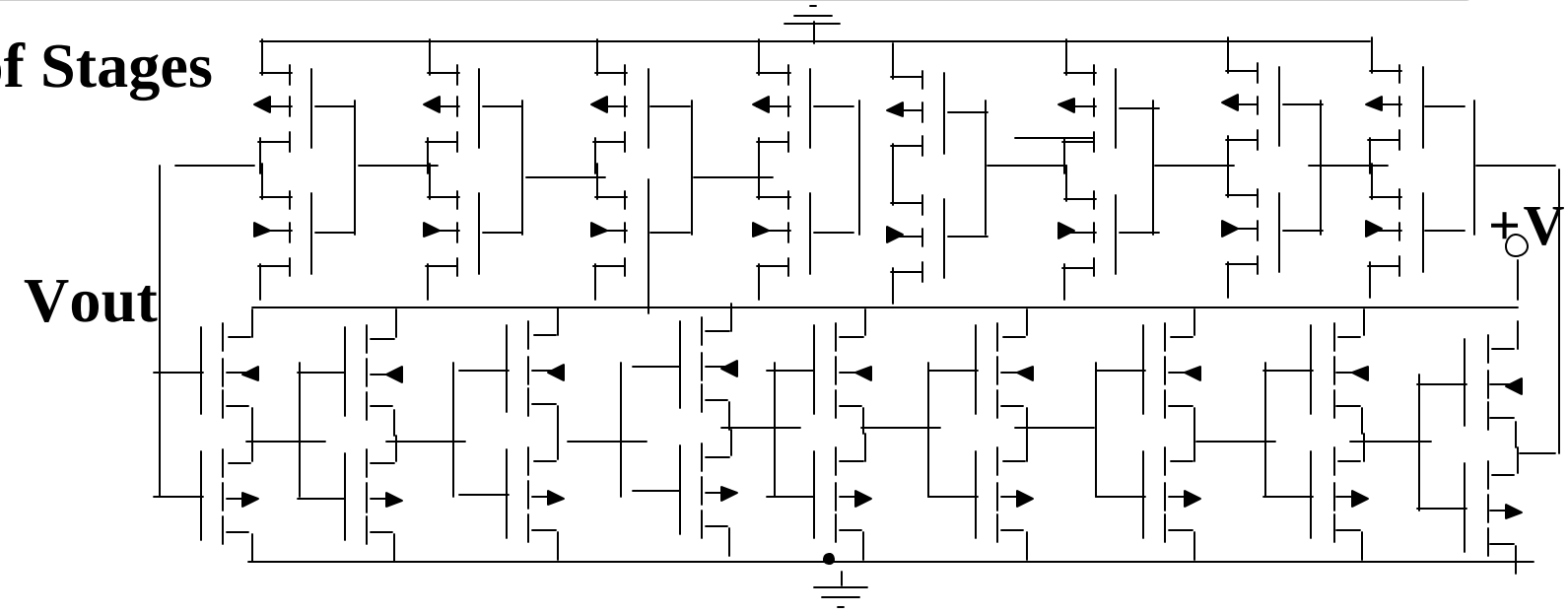
SUMMARY OF COMPLETED FACTORY WAFERS

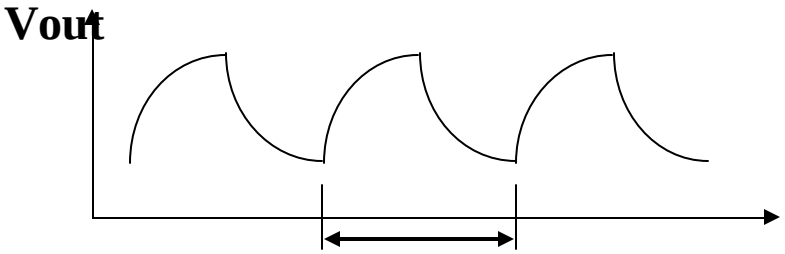
Lot No.	Product	Process	Wafer IDs	Vtn	Vtp	Comments
S030123	TESTCHIP	SUBCMOS				
S030922	MIXED	SUBCMOS	D2	2.6	None	suspect mask error for pmos
S030922	MIXED	SUBCMOS	D3	2	None	suspect mask error for pmos
S031013	MIXED	SUBCMOS	D2	1.26	None	suspect mask error for pmos
S040518	TESTCHIP	ADV				
S040318	TESTCHIP	ADV				
S040322	TESTCHIP	SMFL				
S040615	TESTCHIP	SMFL				
S040906	TESTCHIP	ADV				
S041004	MIXED	SUBCMOS	D1	0.7	-0.67	Metal Adhesion Poor
S050401	DAC	SMFL				
S050408	MIXED	SUBCMOS	D2	1.05	-0.89	
S050907	DAC	SMFL				
S051201	TESTCHIP	SMFL				
S051205	TESTCHIP	SMFL				
S070125	DAC	SMFL				
S070201	MIXED	SUBCMOS	D2	0.86	-0.88	
S070201	MIXED	SUBCMOS	D1	0.984	None	
S070208	TESTCHIP	SMFL				
S070910	MIXED	SUBCMOS	D1	0.4	-1.4	
S070910	MIXED	SUBCMOS	D3	0.6	-1.4	
S071001	MIXED	SUBCMOS	D1	0.94	-0.98	lot number not visible
S071001	MIXED	SUBCMOS	D2	0.76	-0.97	lot number not visible
S071001	MIXED	SUBCMOS	D3	1.82	None	lot number not visible

We tested all of the MIXED SUBCMOS lots that were completed in the last several years and found the NMOS and PMOS threshold voltages for the 2um transistors. Seven of the nine wafers completed had

RING OSCILLATOR

Odd # of Stages





T = period of oscillation

td = T/2N

T = period of oscillation

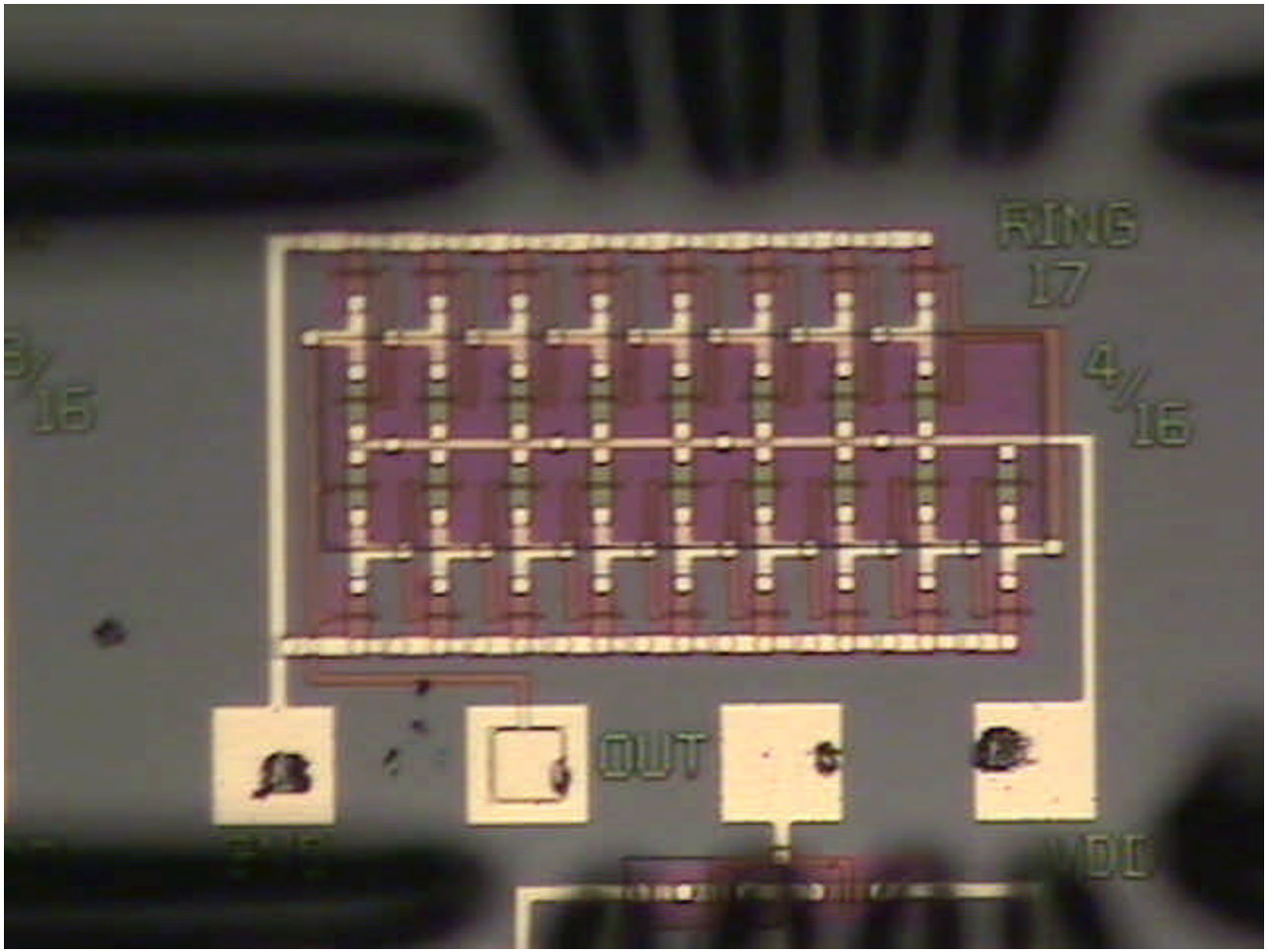
N = number of stages

td = gate delay

RING OSCILLATOR

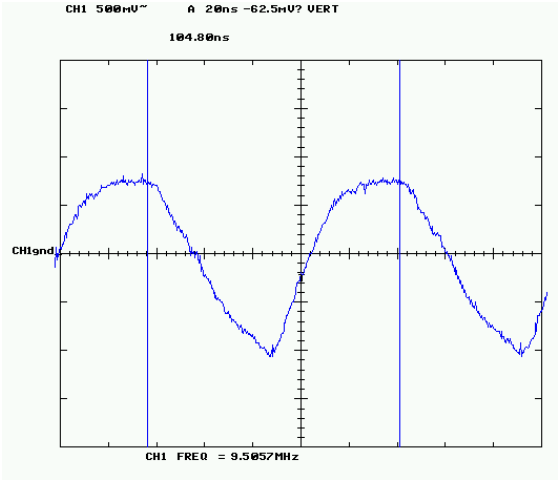
No buffer
17 Stage
L/W = 4/16
Vdd = 5V

td = gate delay
= 90ns/2/17
= 2.6ns



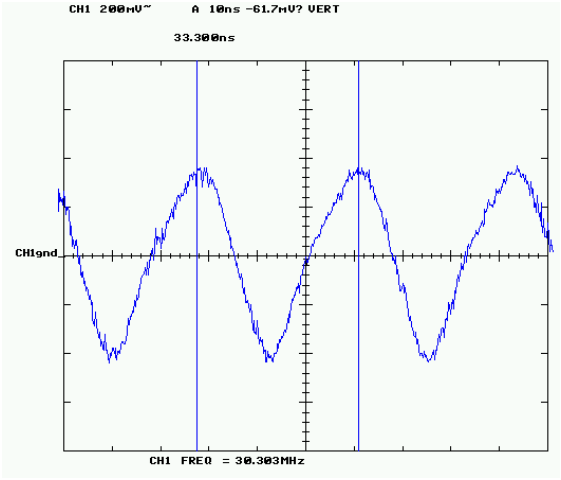
RING OSCILLATOR

SMFL CMOS Process

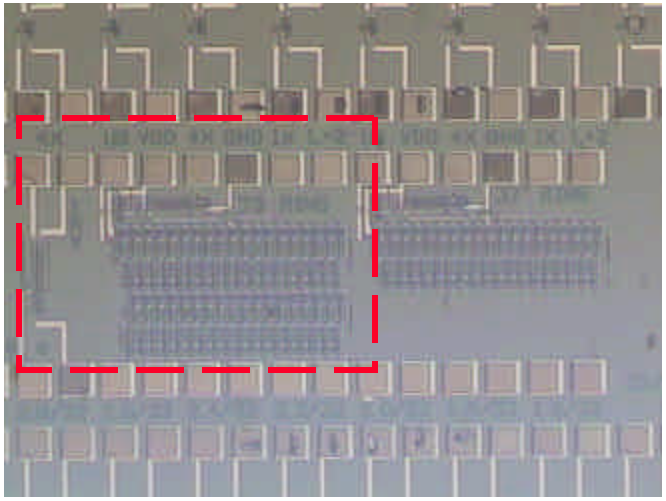


4x buffer

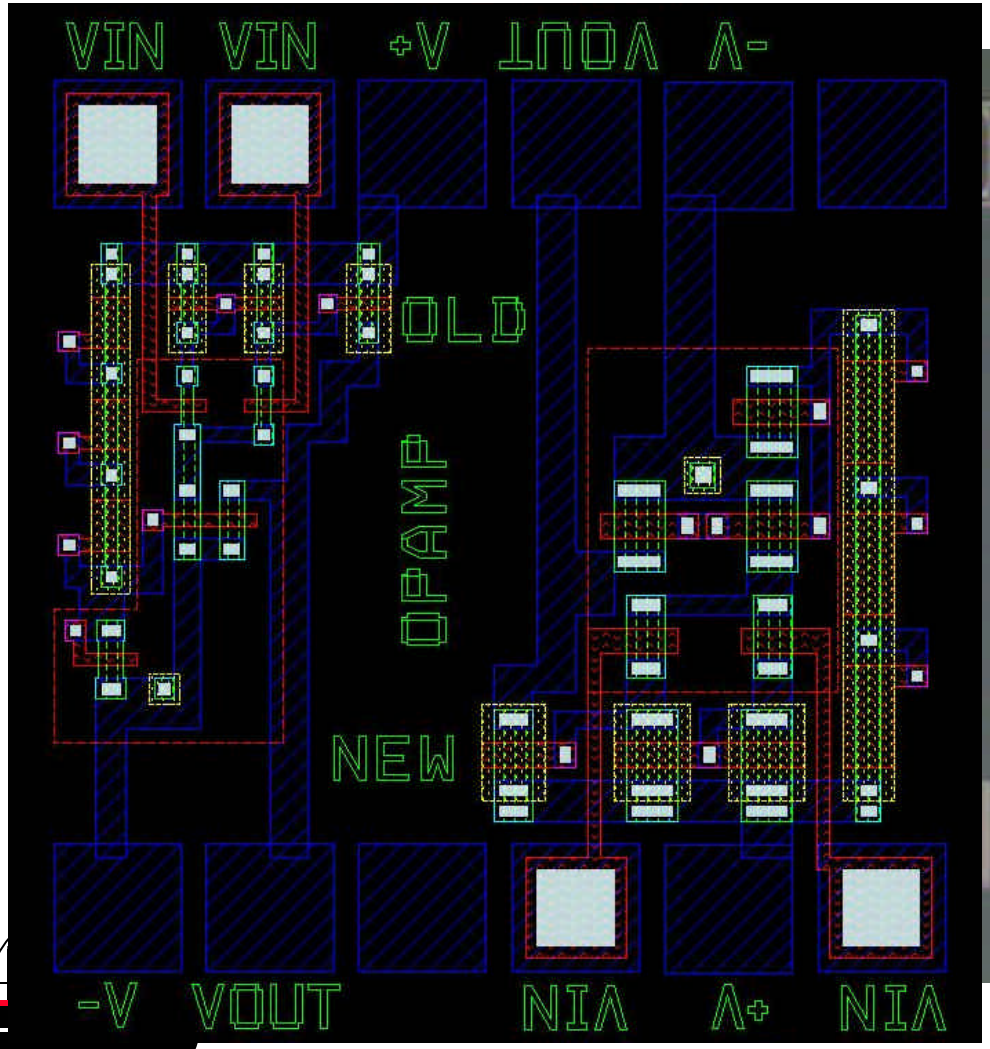
73 Stage Ring at 5V, td = 0.712ns

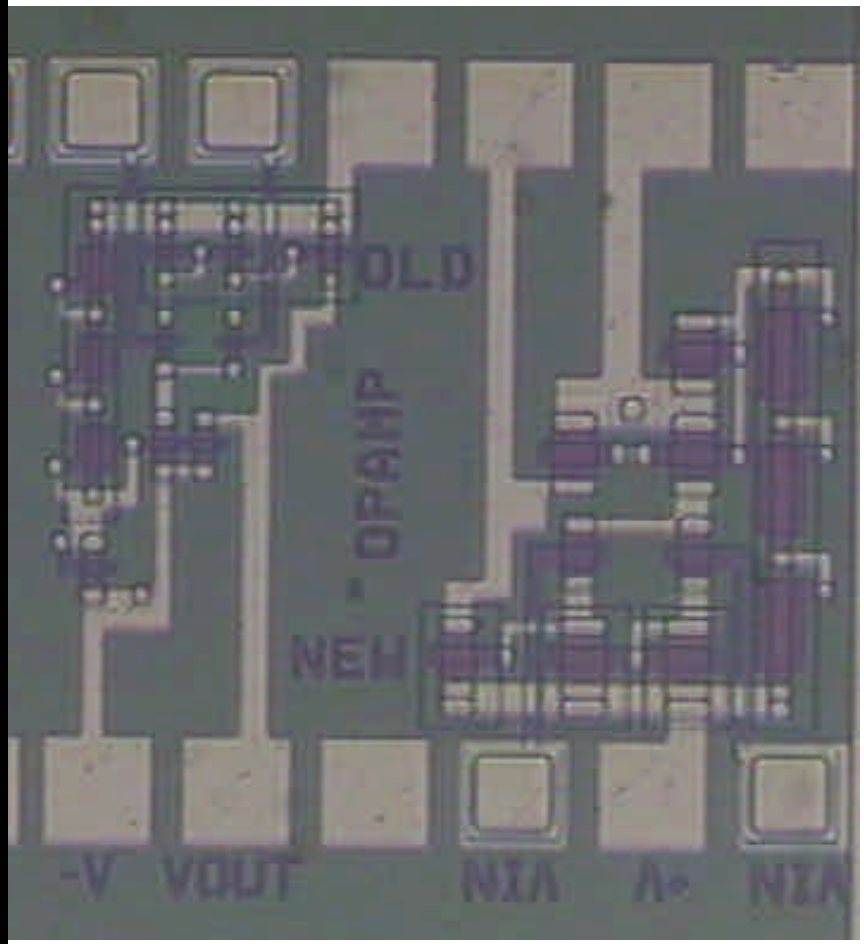


73 Stage Ring at 6V, td = 0.228ns

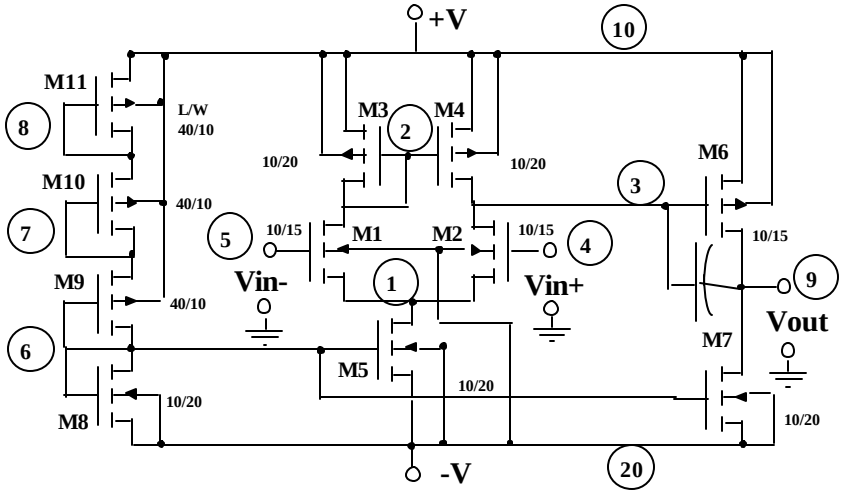


OPERATIONAL AMPLIFIER





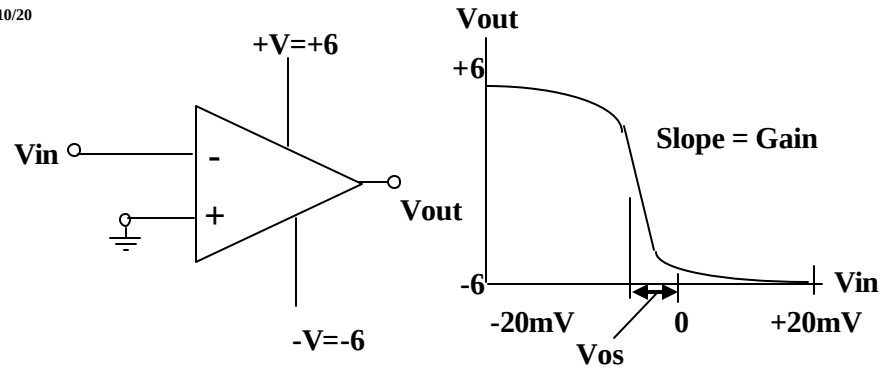
OPERATIONAL AMPLIFIER



p-well CMOS

dimensions
L/W
(μm/μm)

Old Version Schematic
New Version has L and W twice as large



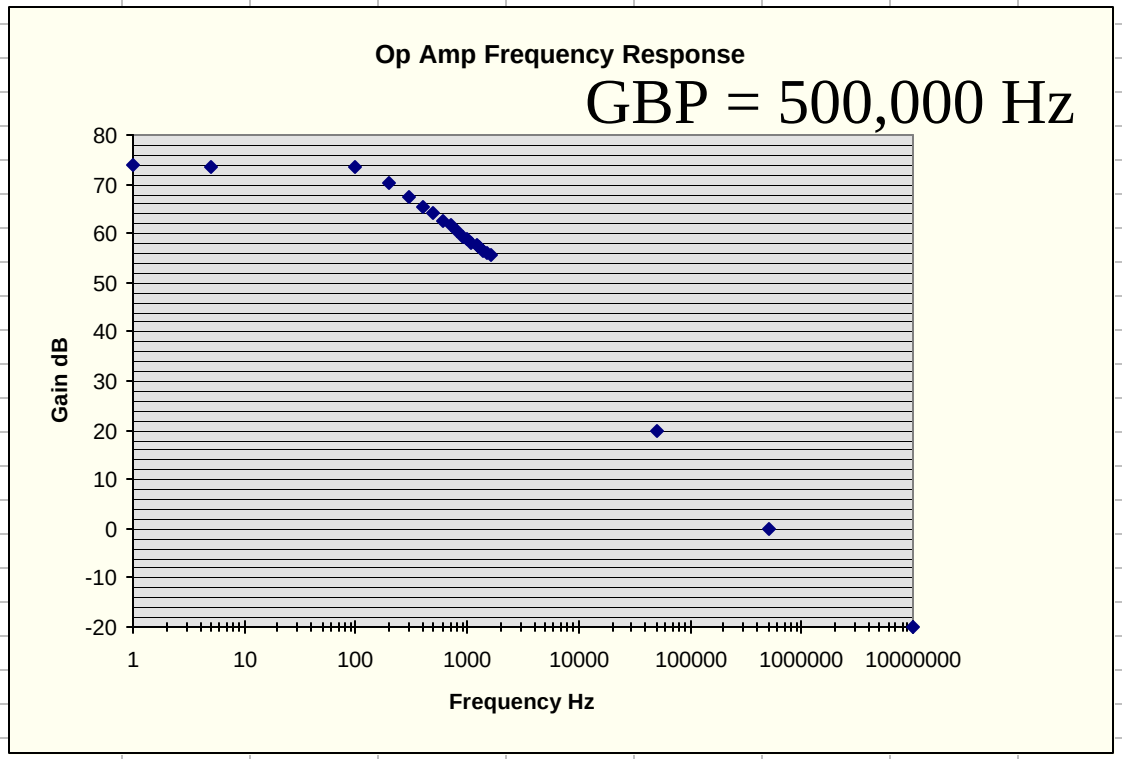
Set up the HP 4145 to sweep the Vin from -20 mV to +20 mV in 0.001V steps. Measure Gain and Input offset voltage.

AC TEST RESULTS

ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING — LFF OPAMP.XLS FILE3B

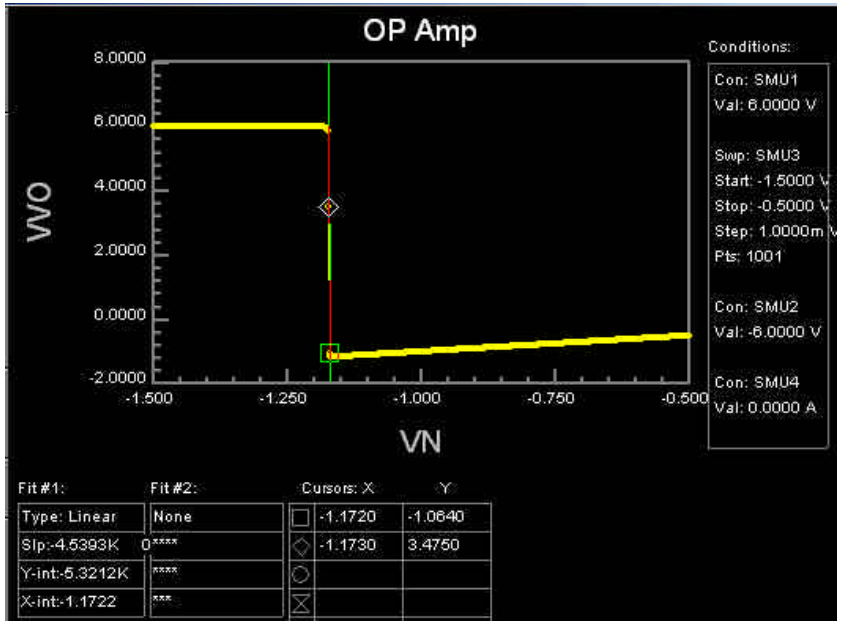
LOT F960319 OPAMP TEST RESULTS - 1-29-97

Frequency	Gain	Vout	Vin
hZ	dB	V	mV
1	73.9794	10	2
5	73.53387	9.5	2
100	73.33036	9.28	2
200	70.31748	6.56	2
300	67.53154	4.76	2
400	65.48316	3.76	2
500	63.97314	3.16	2
600	62.41148	2.64	2
700	61.51094	2.38	2
800	60.34067	2.08	2
900	59.46256	1.88	2
1000	58.68997	1.72	2
1100	58.0618	1.6	2
1200	57.50123	1.5	2
1300	57.14665	1.44	2
1400	56.5215	1.34	2
1500	56.1236	1.28	2
1600	55.56303	1.2	2
50000	20	0.02	2
500000	0	0.002	2
10000000	-20	0.0002	2



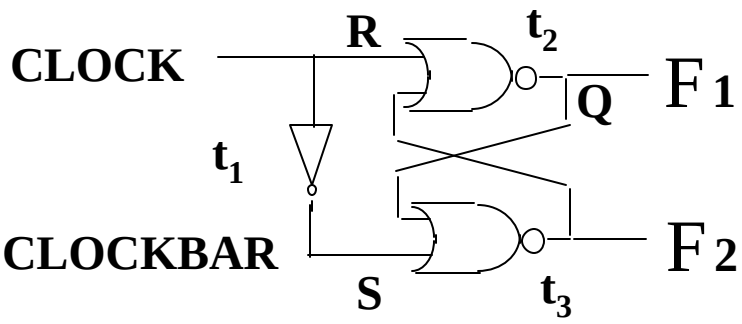
CMOS OPERATIONAL AMPLIFIER

SUB-CMOS Process

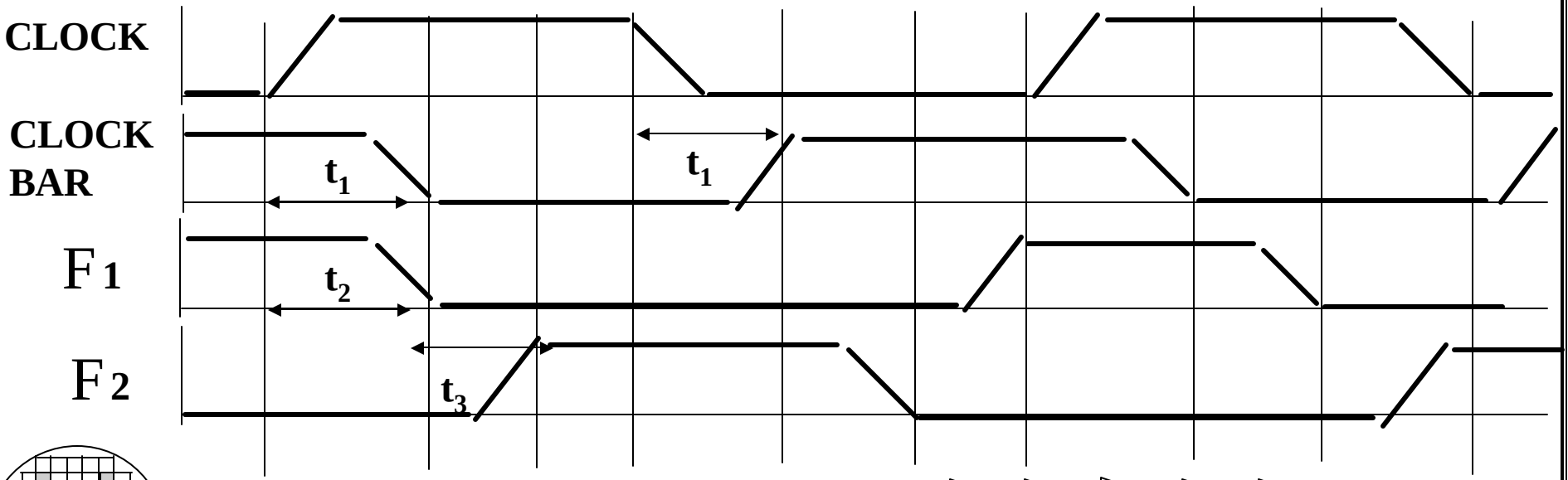


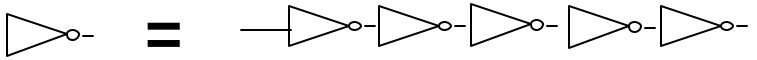
TWO-PHASE CLOCK GENERATORS

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

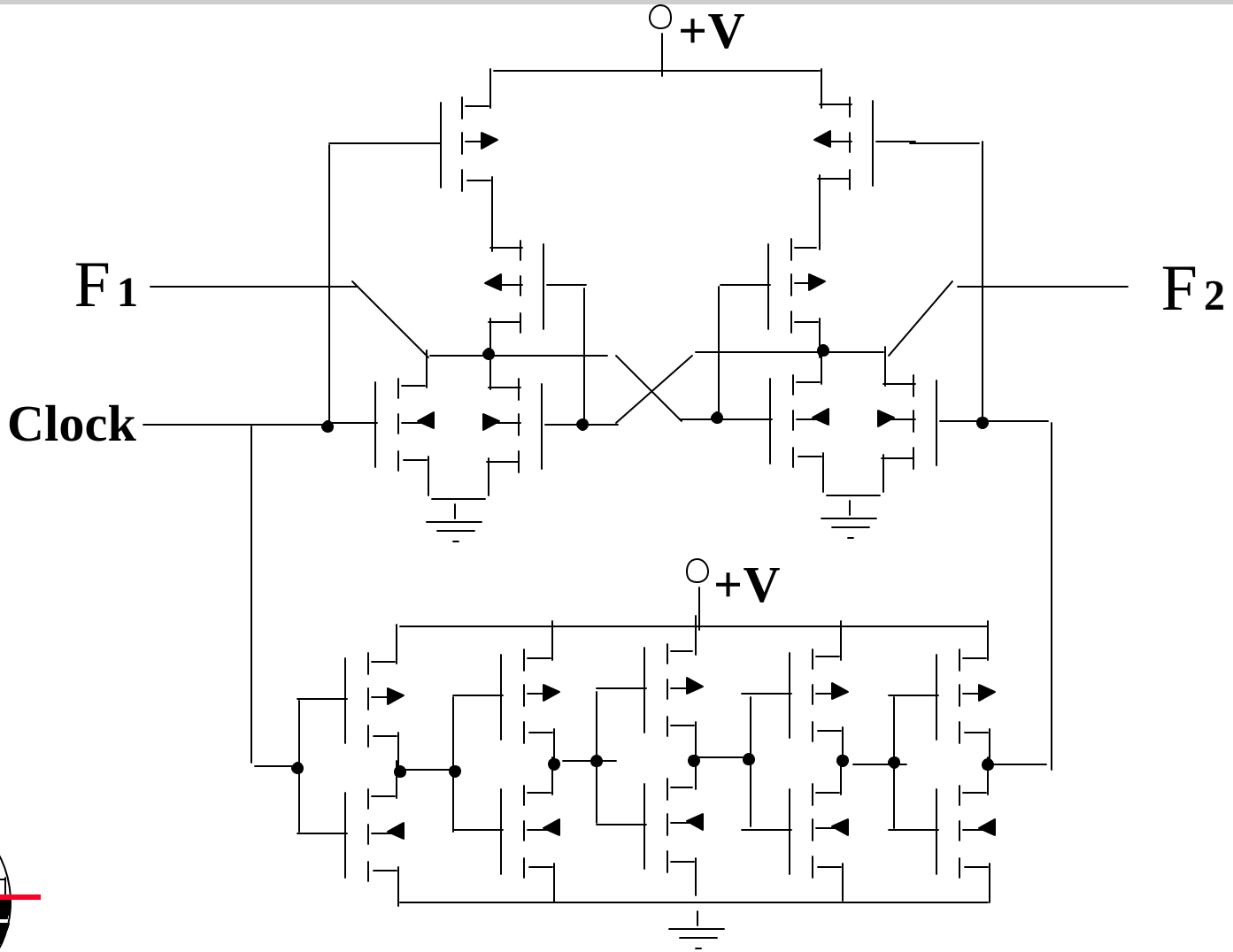


R	S	Q
0	0	Qn-1
0	1	1
1	0	0
1	1	INDETERMINATE

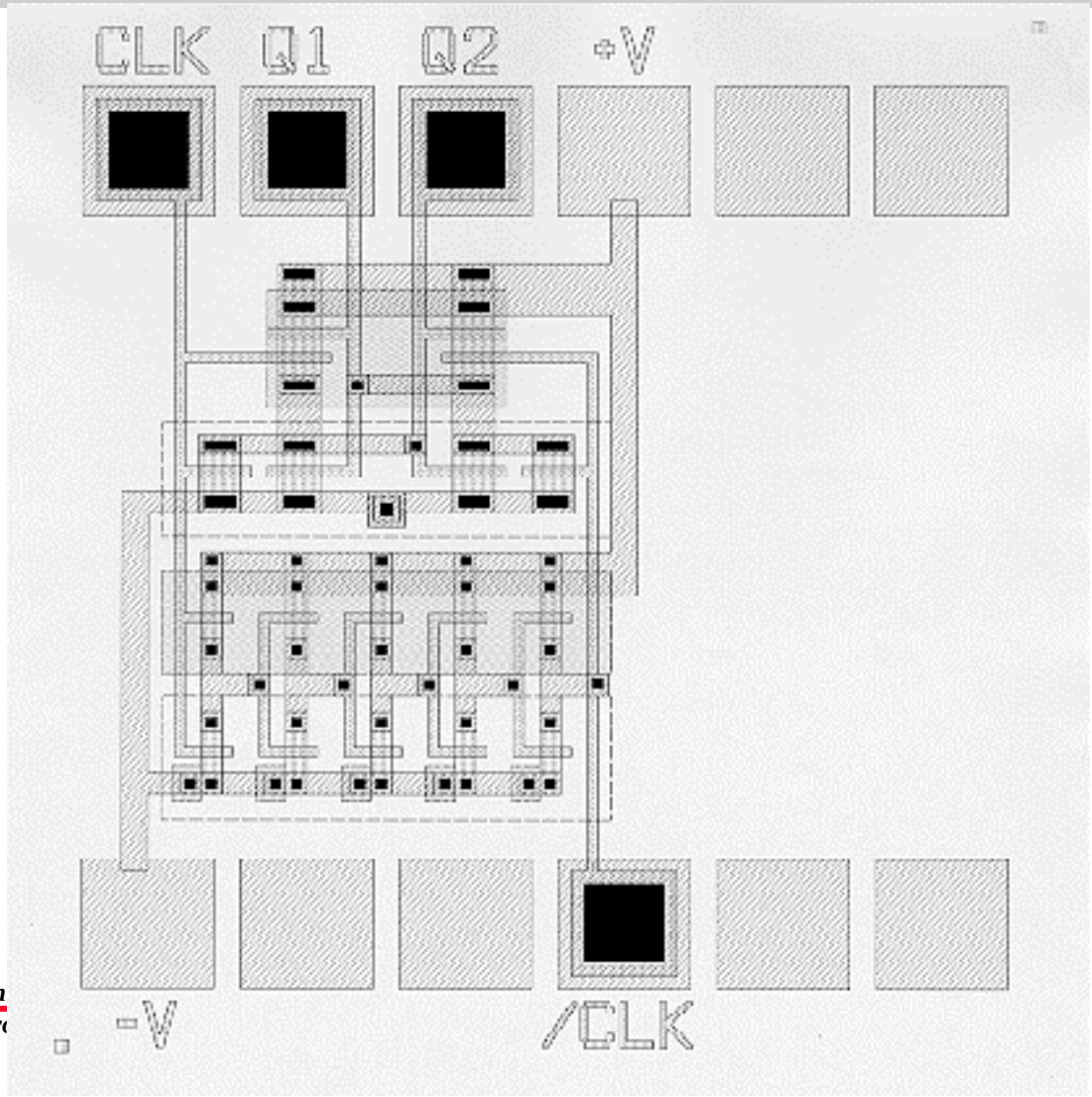




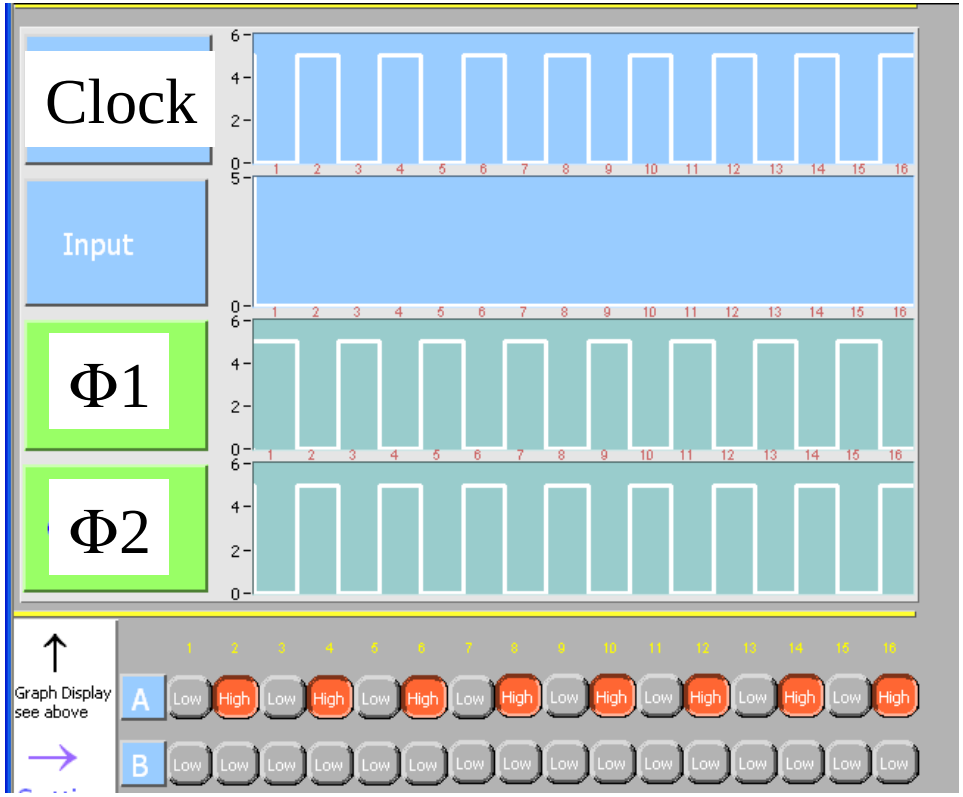
TRANSISTOR LEVEL SCHEMATIC OF 2 PHASE CLOCK

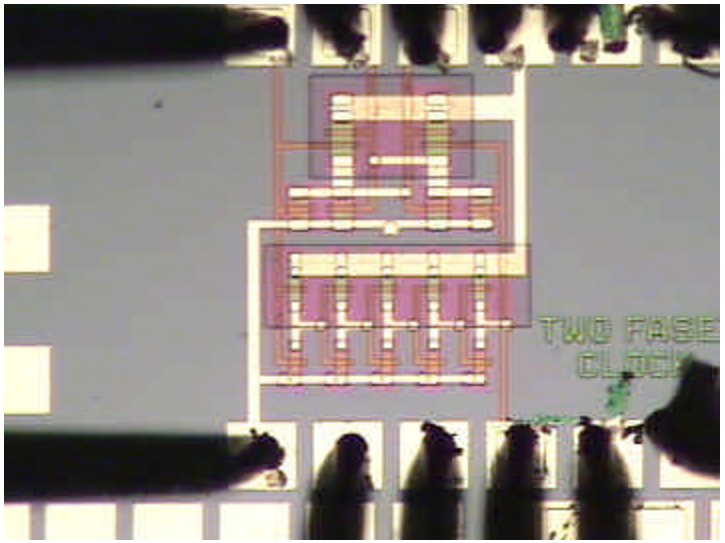


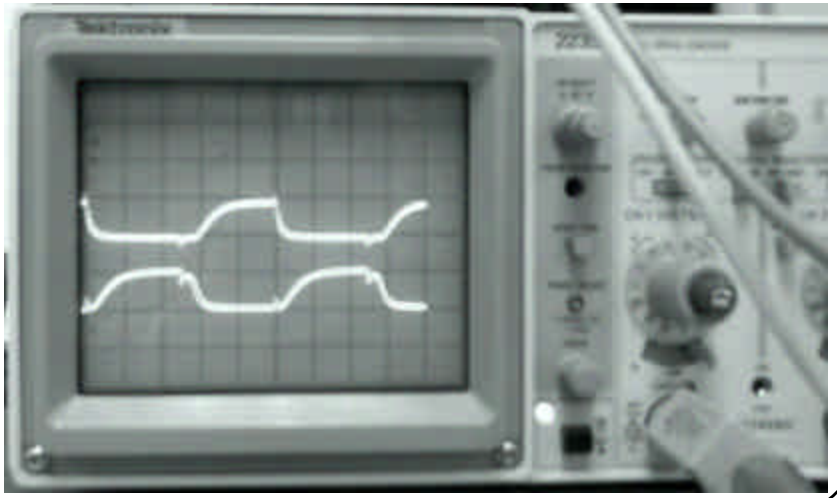
LAYOUT OF TWO PHASE CLOCK



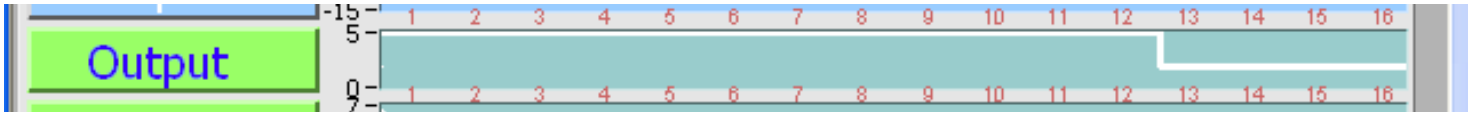
TWO PHASE NON OVERLAPPING CLOCK

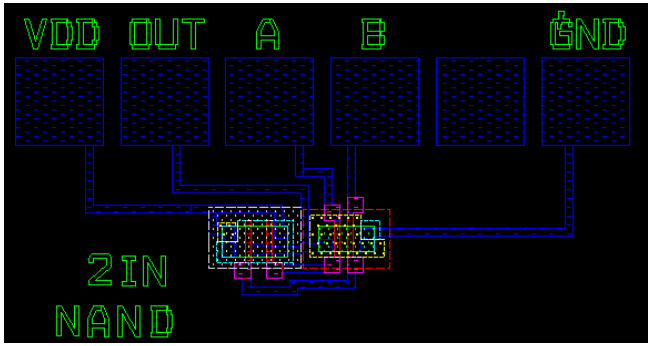


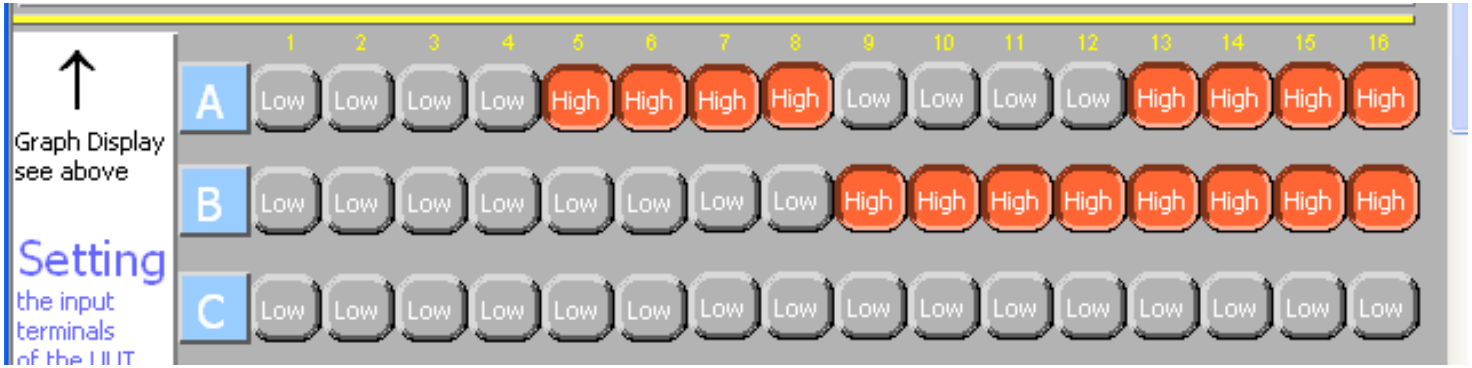




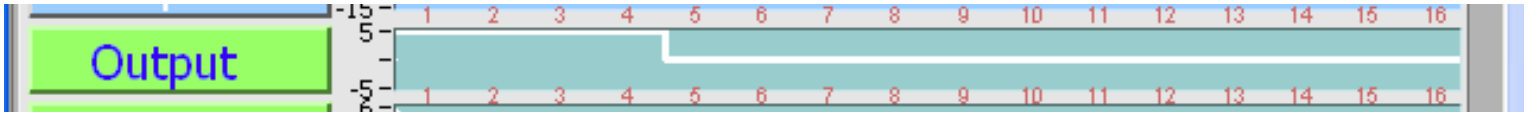
CMOS 2 INPUT NAND

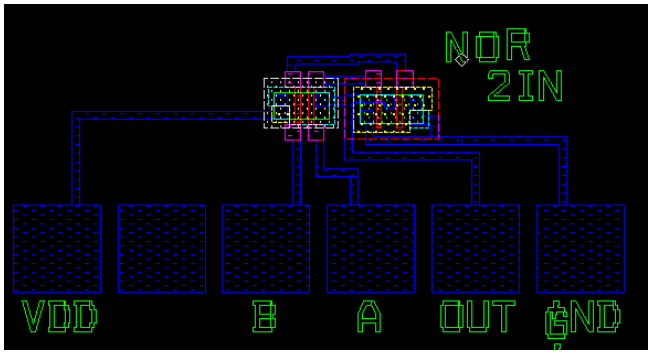


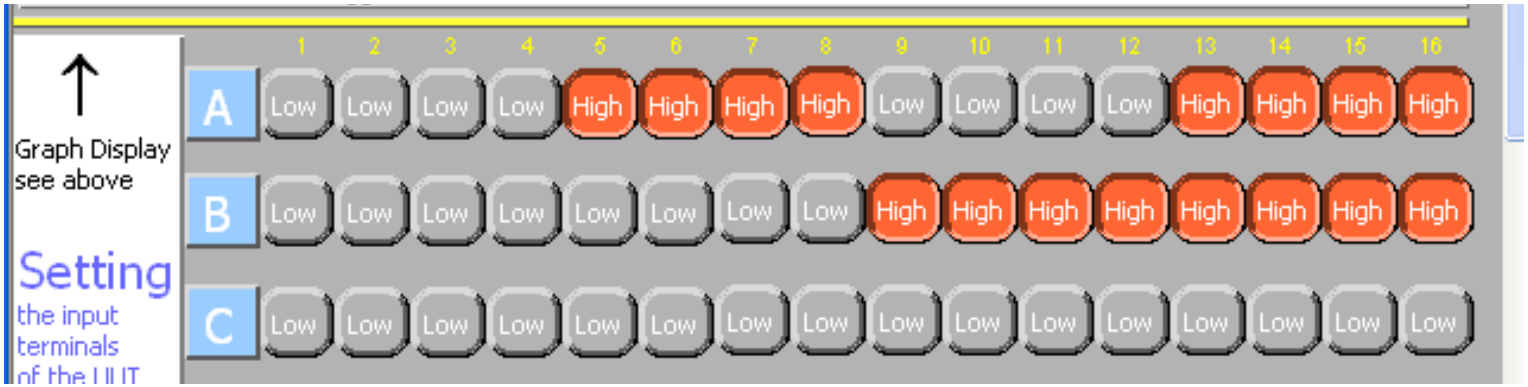




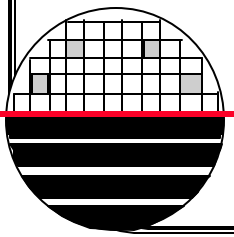
CMOS 2-INPUT NOR



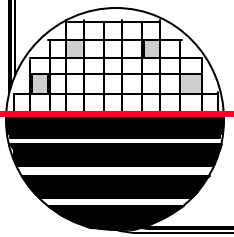




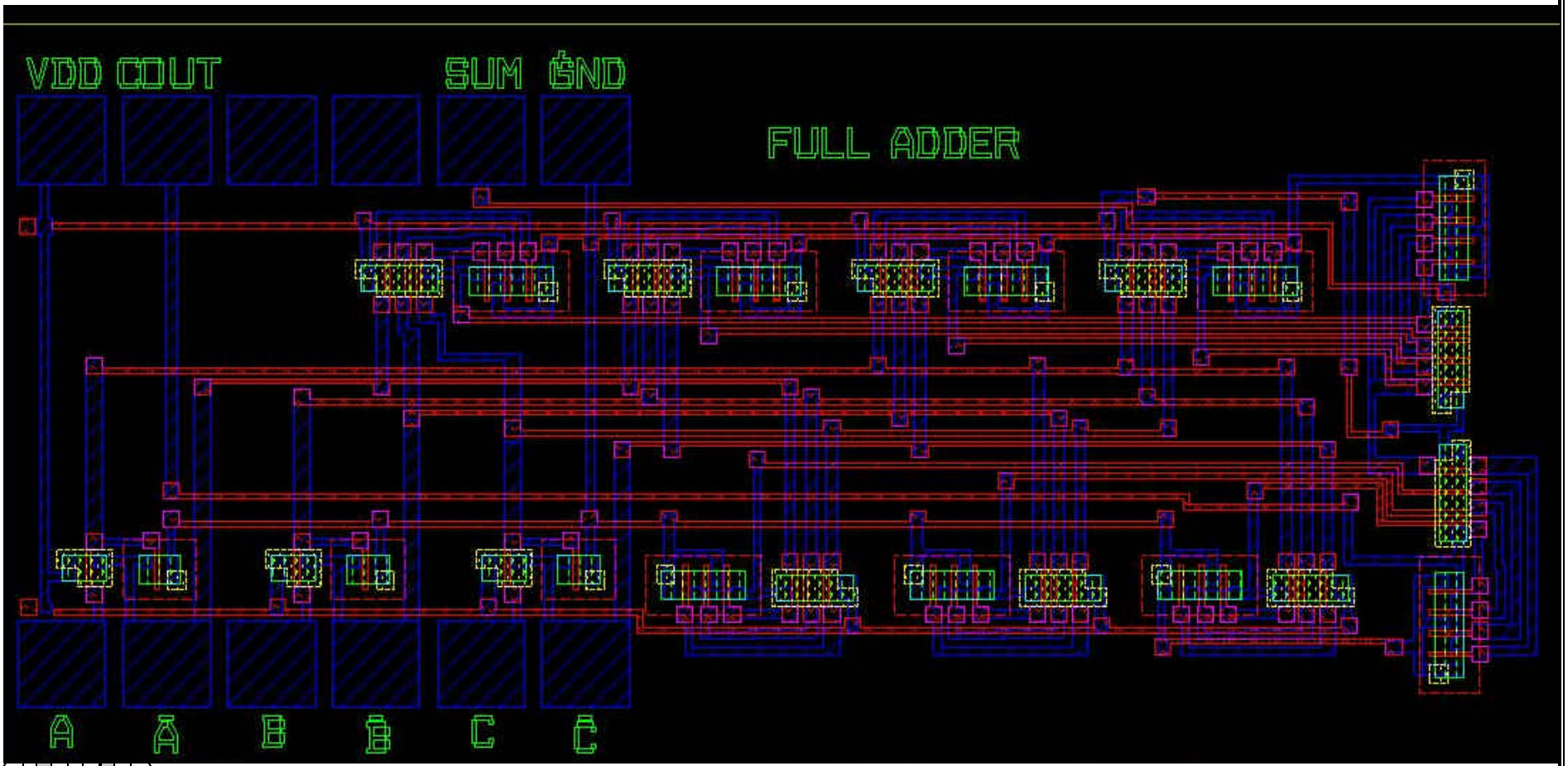
CMOS 3-INPUT NAND



CMOS 3-INPUT NOR

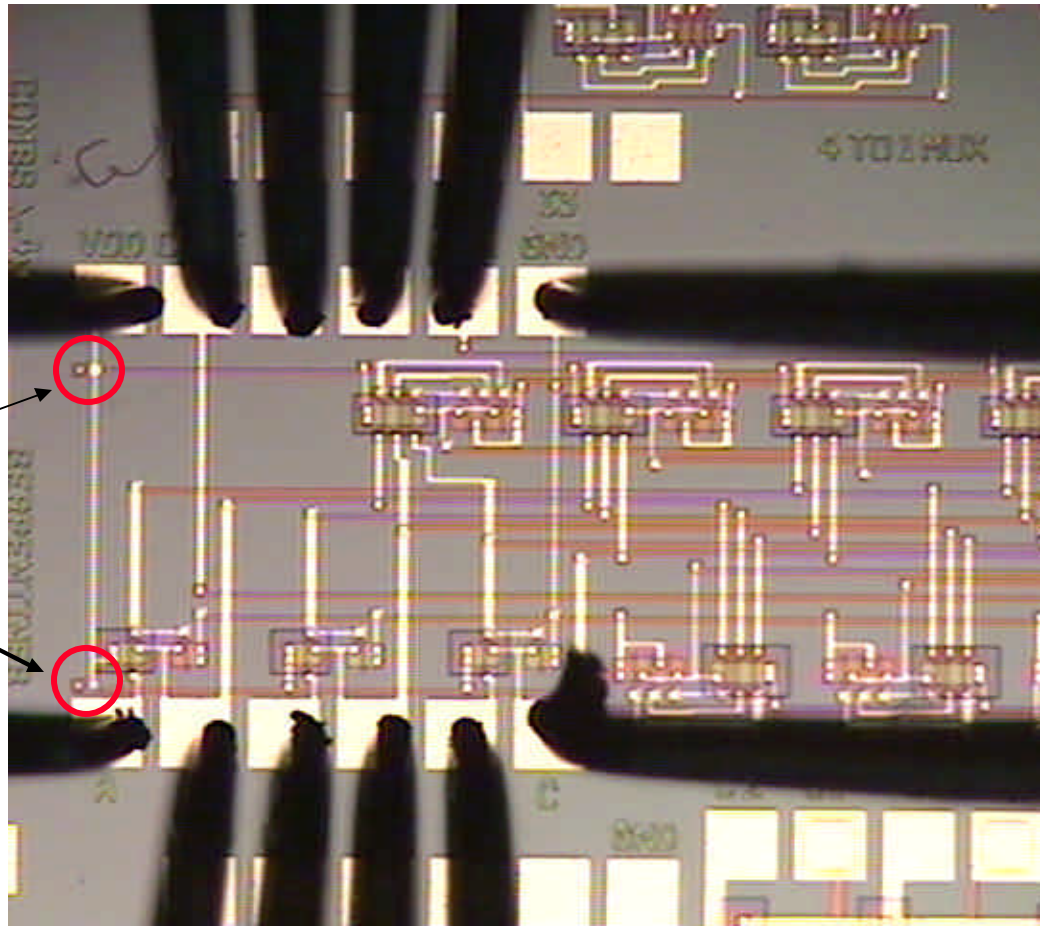


FULL ADDER DESIGN

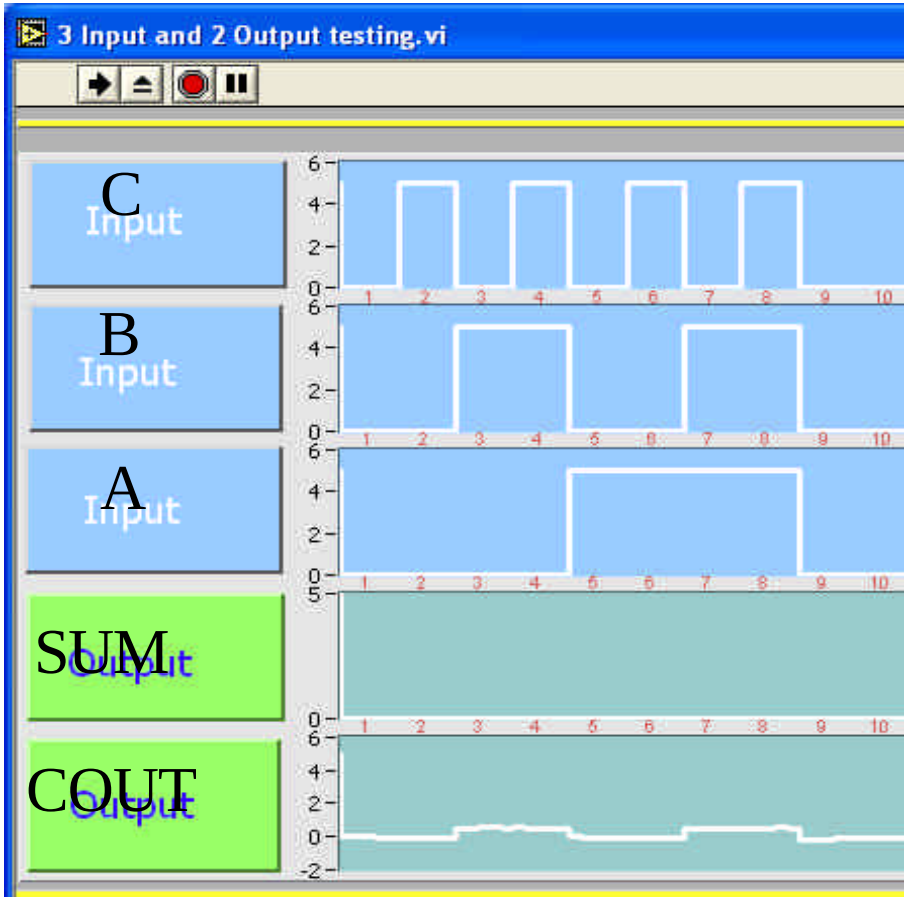


FULL ADDER BROKEN VDD CONNECTION

Broken Vdd Connections

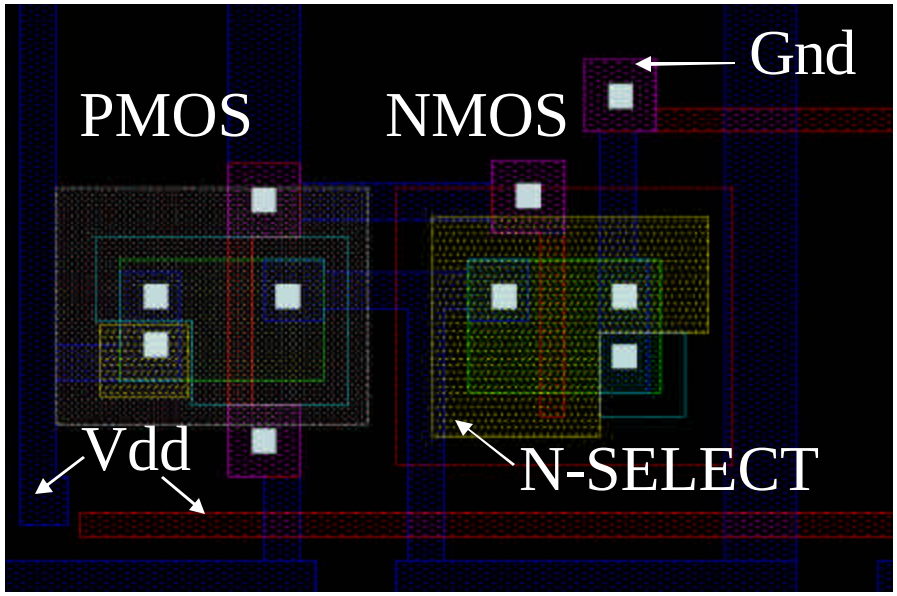


FULL ADDER TEST RESULTS

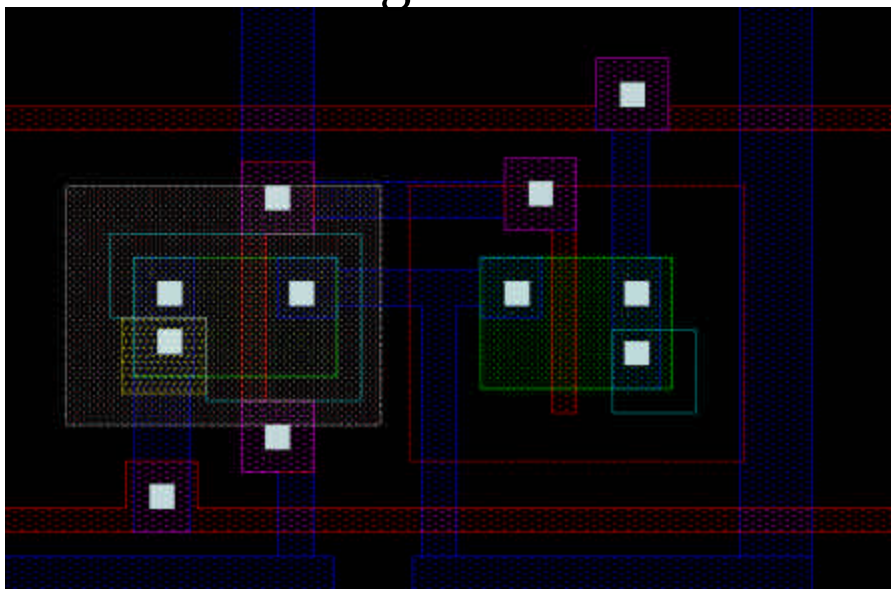


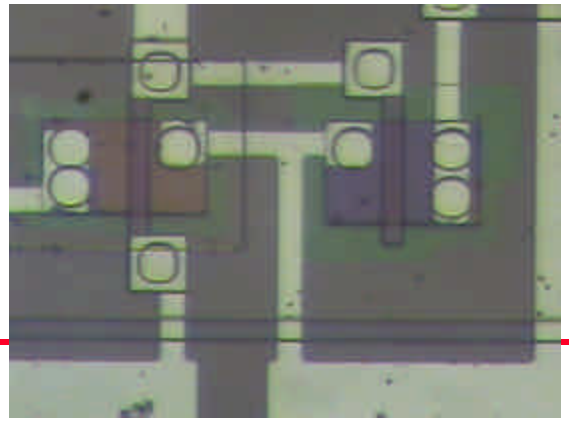
FULL ADDER MISSING N-SELECT ON SOME INVERTERS

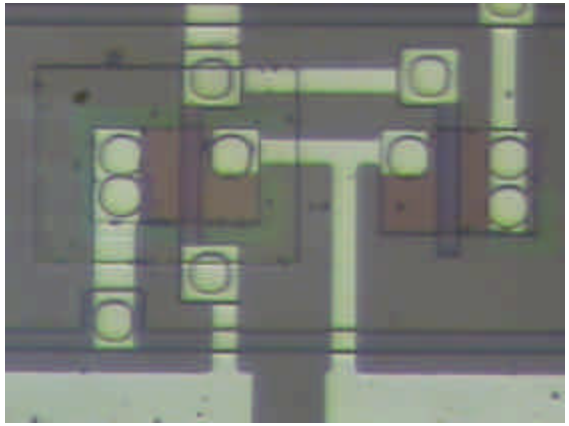
Vdd Connection Broken



Missing N-Select

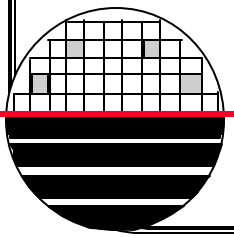




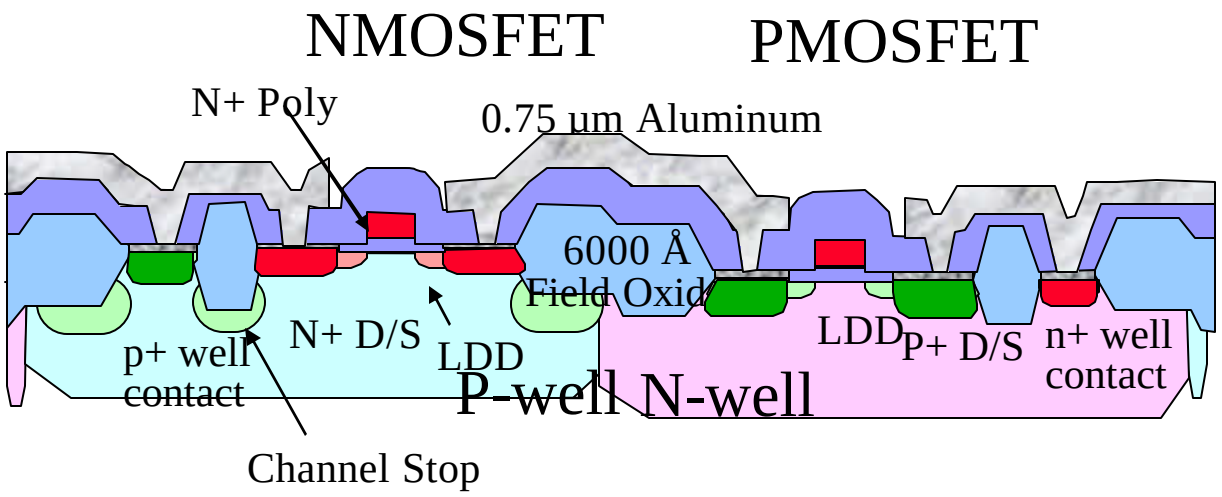


DISCUSSION ON N-SELECT AND P-SELECT

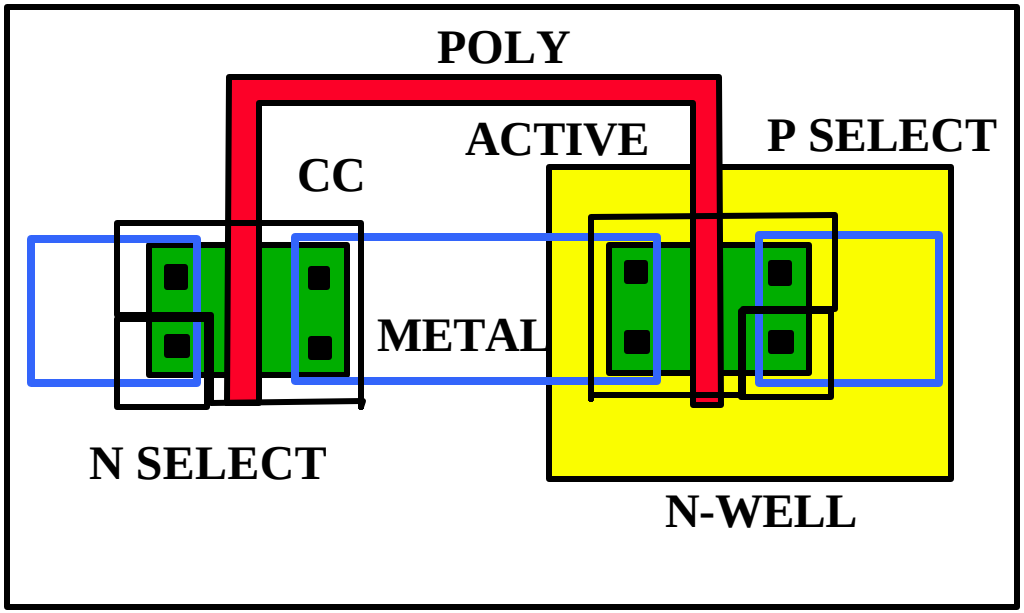
The designer needs only one of n-select or p-select to make the masks needed for CMOS. The design rule checkers can also be made to work with only one of the two select layers. At RIT we use both n-select and p-select in the design to make the design rule checks easier to implement. Thus at RIT both should be available for making the masks. On the next page you find that both n-select and p-select are used in making the masks for the sub-micron CMOS process. On the following page you see that only p-select is used to make the masks. It does not matter how it is done but it has to be done correctly.

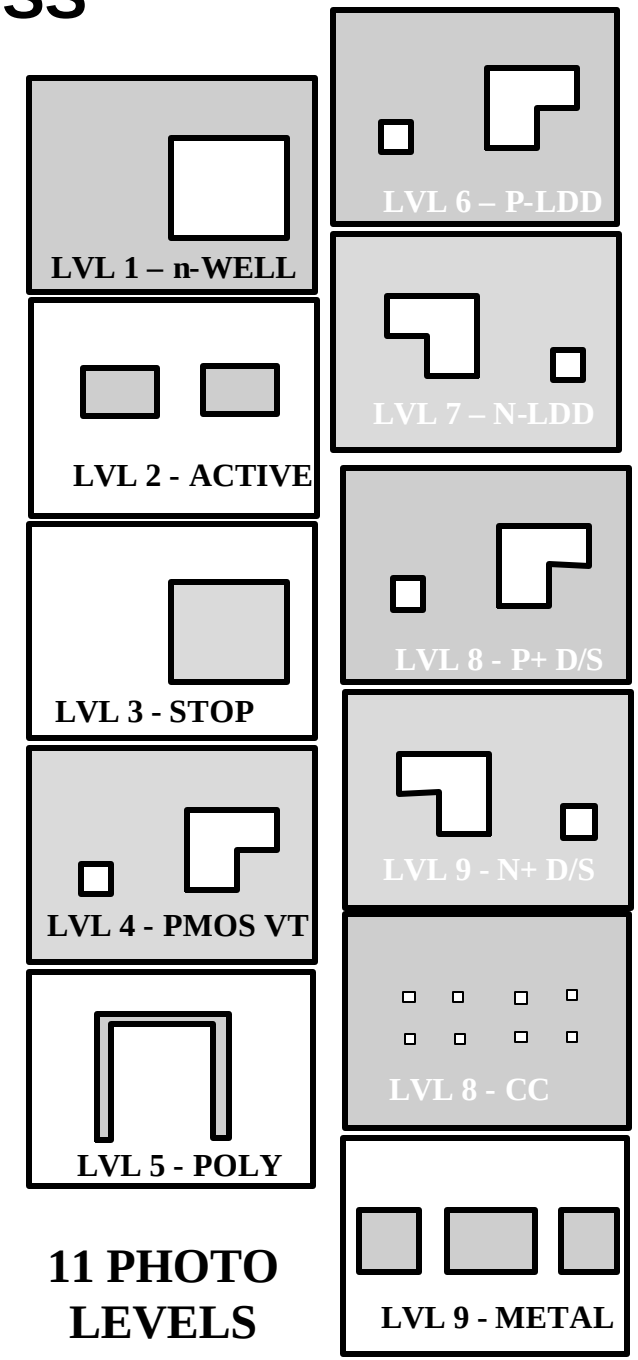


RIT SUB-CMOS PROCESS



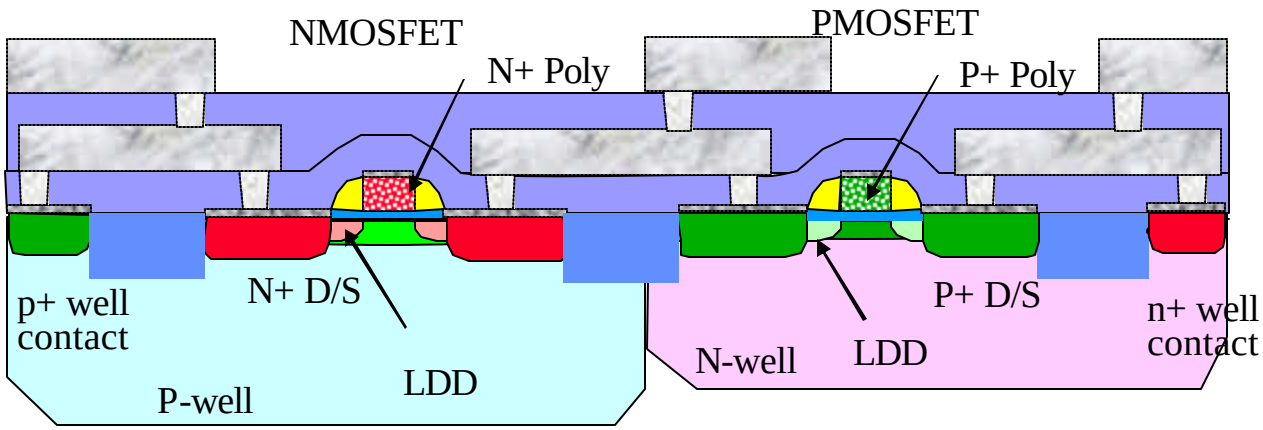
N-type Substrate 10 ohm-cm



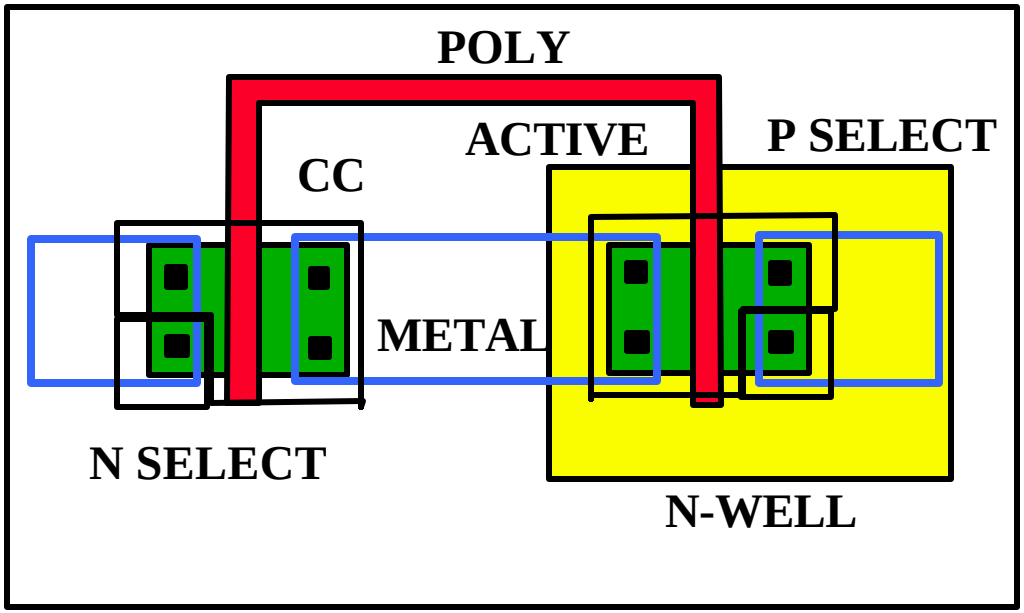


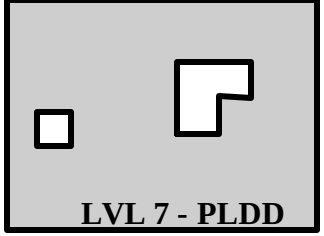
11 PHOTO LEVELS

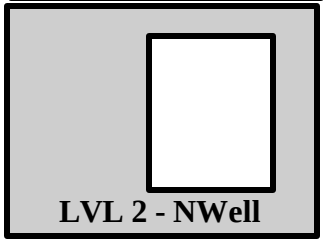
RIT ADVANCED CMOS PROCESS

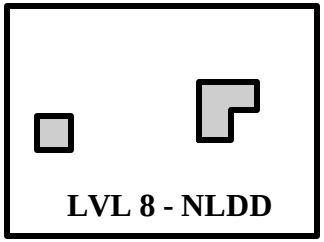


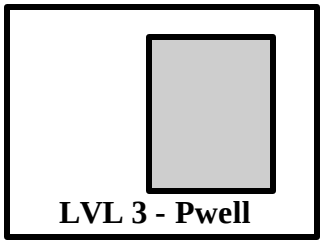
12 PHOTO LEVELS

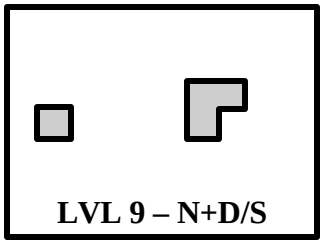


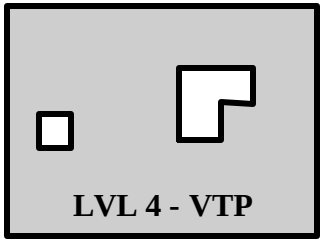


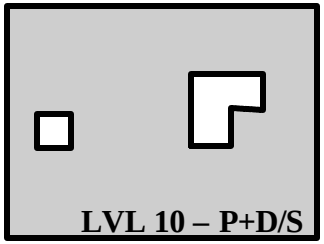


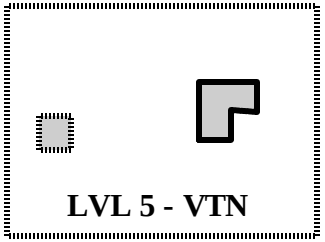


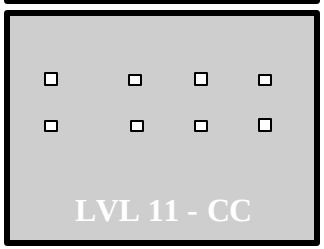


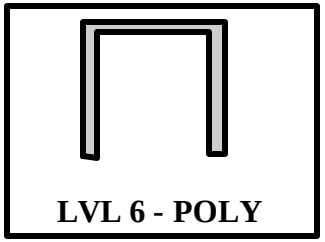


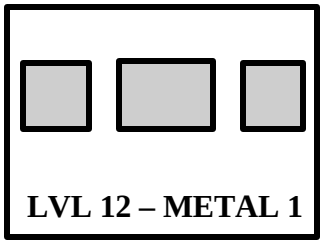




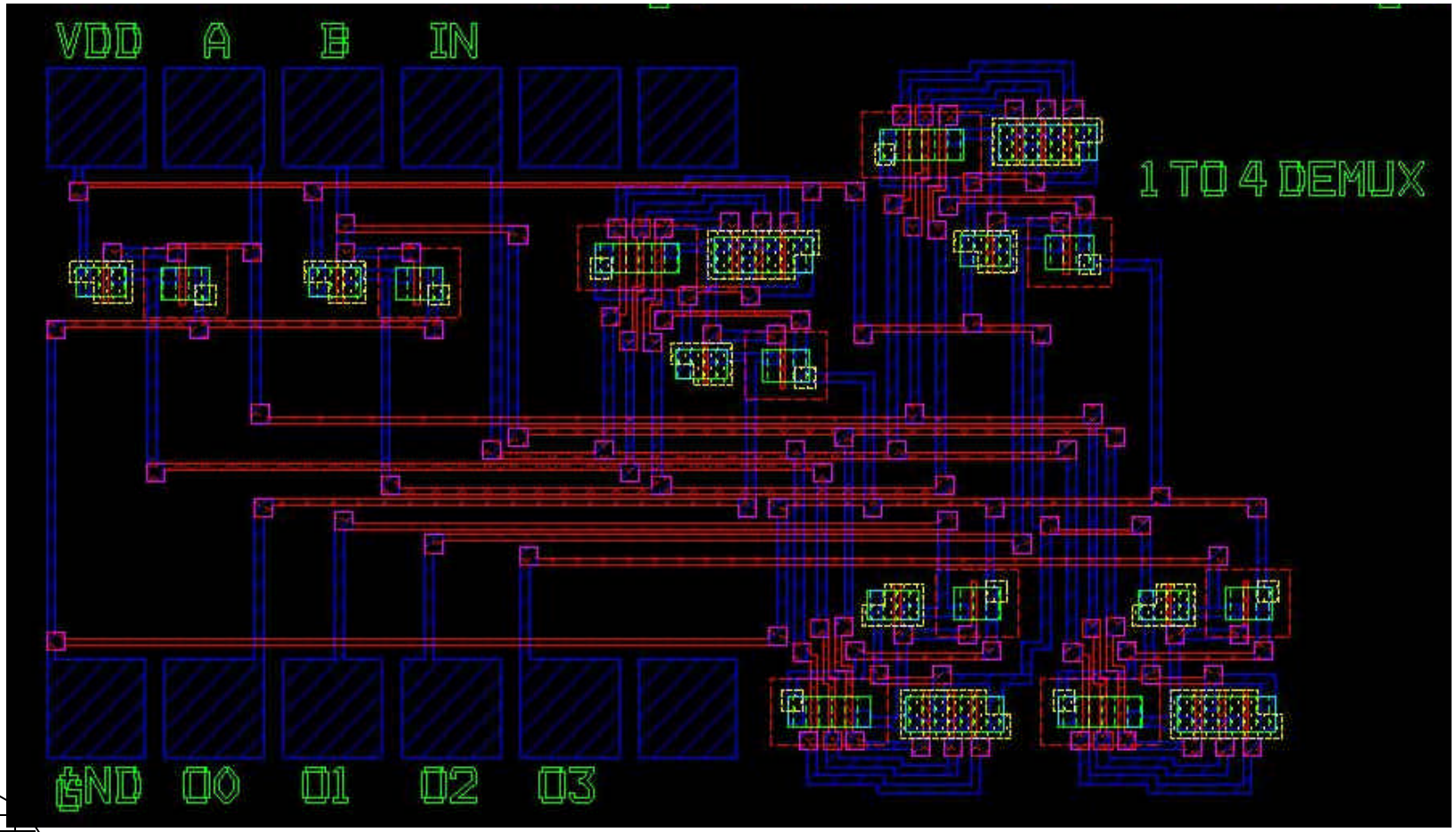




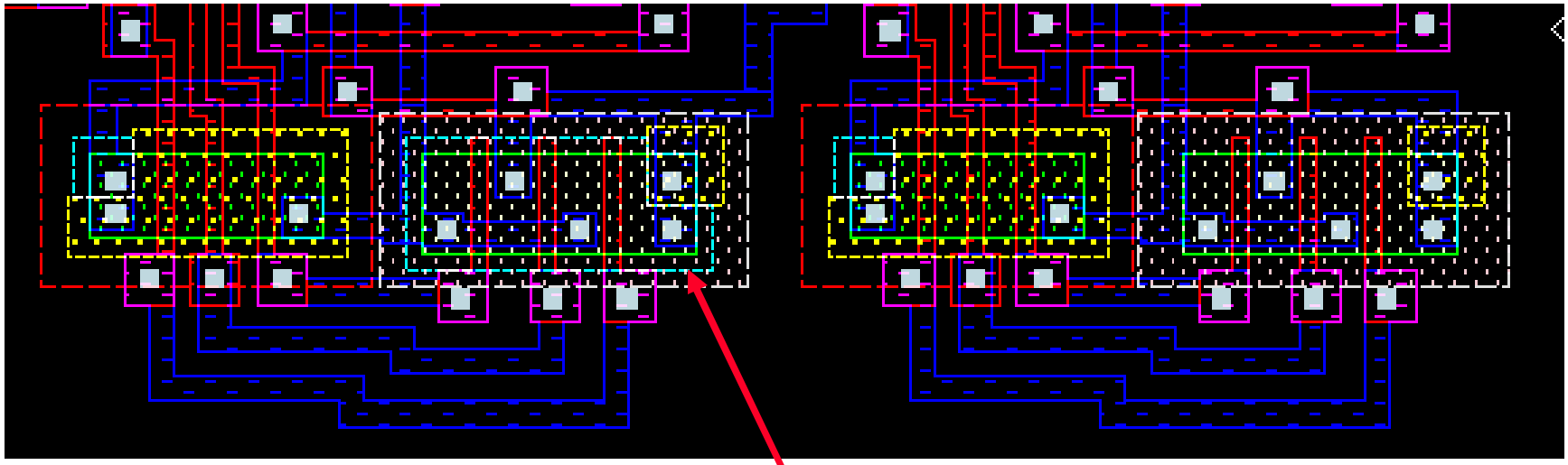




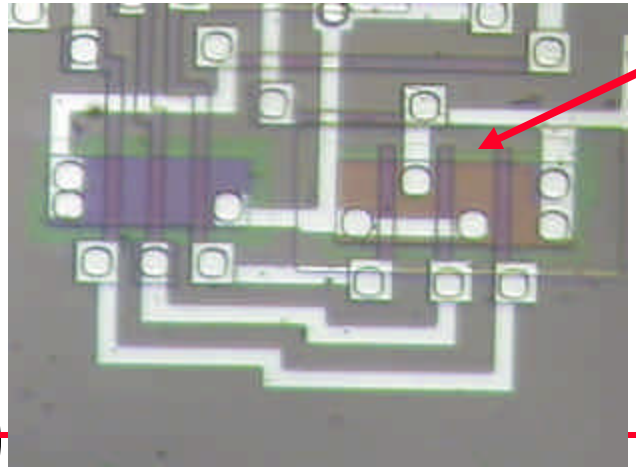
1 TO 4 DEMUX DESIGN

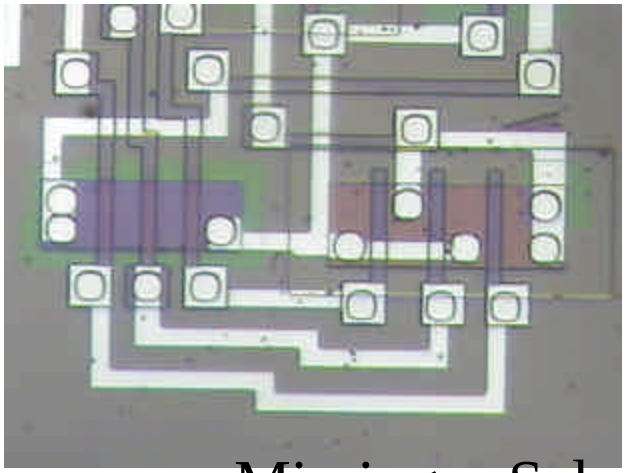


MISSING P-SELECT ON SOME NOR GATES



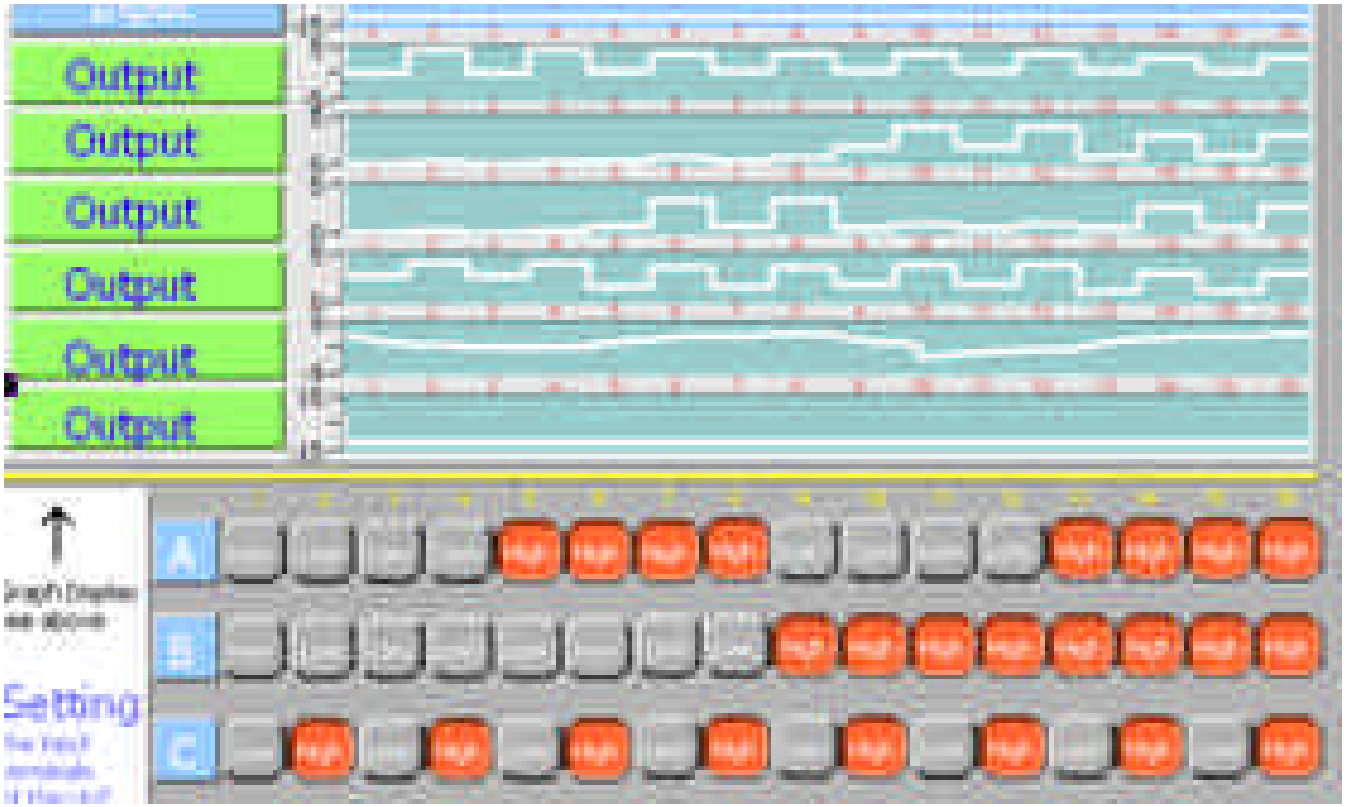
P-Select





Missing p-Select

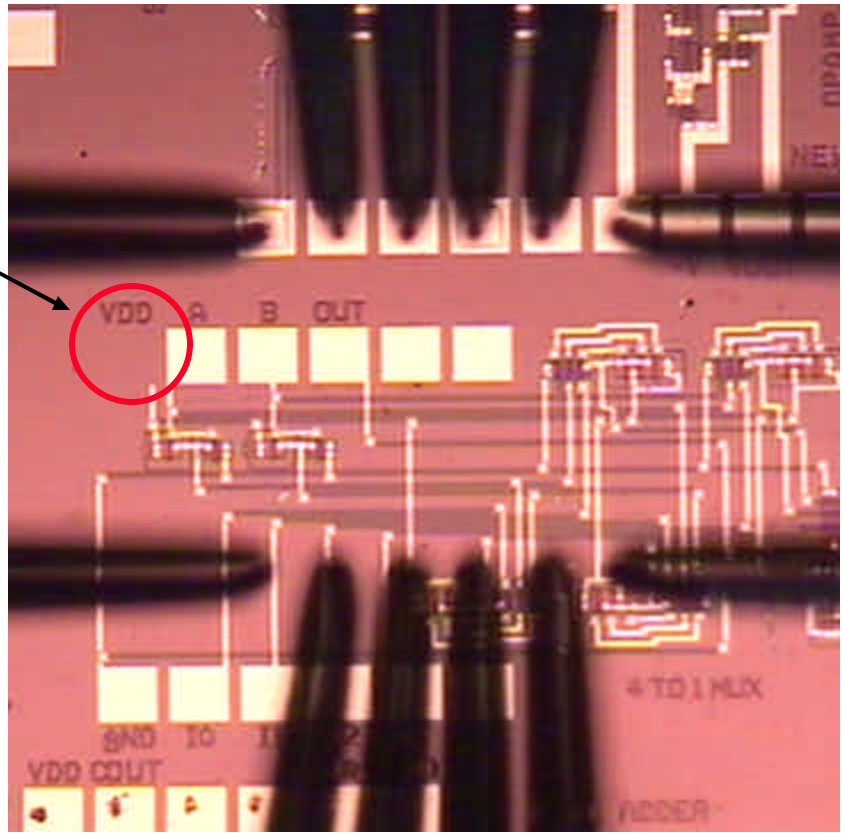
1 TO 4 DEMUX TEST RESULTS



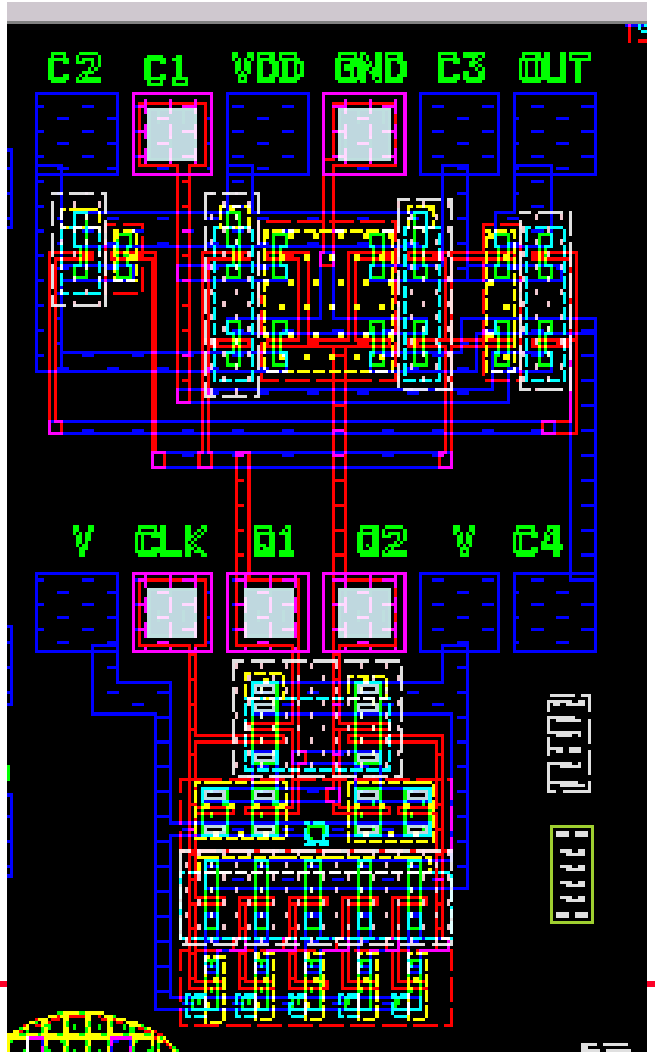
Missing p-Select on some 3-NORs

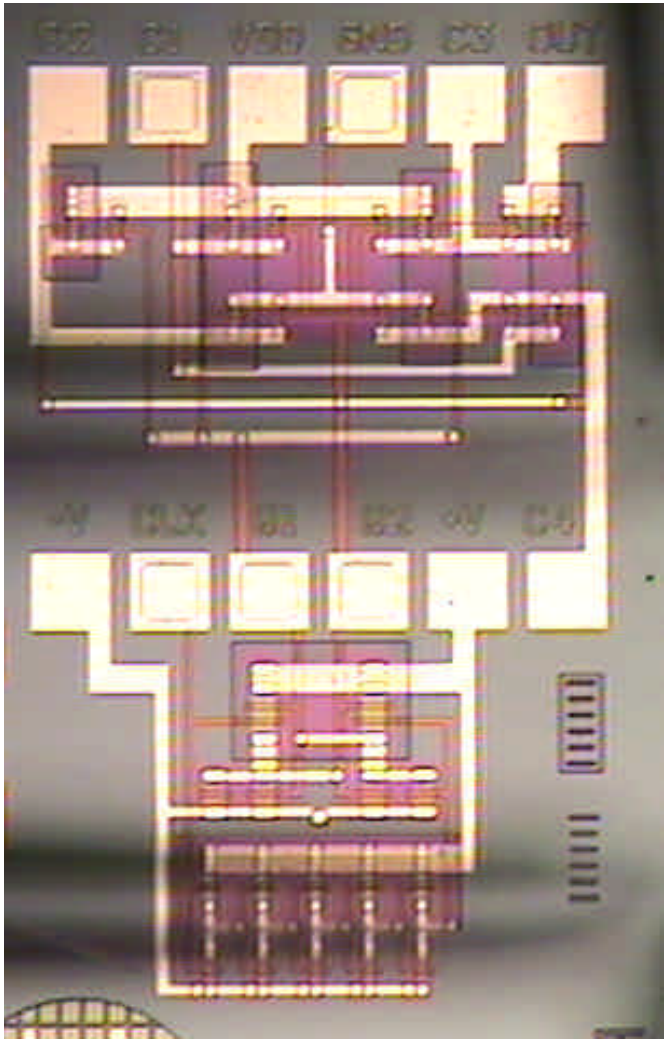
4 to 1 MUX

Missing Vdd Pad

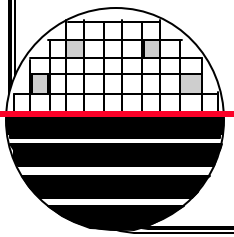


VOLTAGE DOUBLER





VOLTAGE DOUBLER TEST RESULTS



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