ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Combinatorial and Sequential CMOS Circuits

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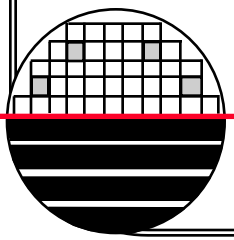

ADOBE PRESENTER

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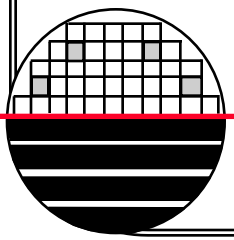
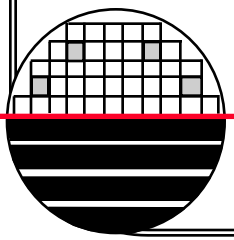
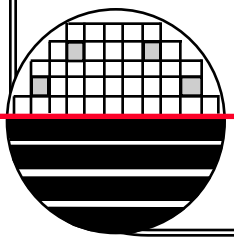


OUTLINE



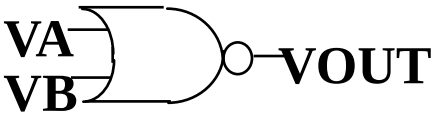
INTRODUCTION

In this module we want to look at combining transistors to make CMOS logic gates. In general we want the logic gate to function correctly for static operation, we want the noise margin to be similar to that of the CMOS inverter and the speed at which the gate operates to be similar to that of the CMOS inverter.

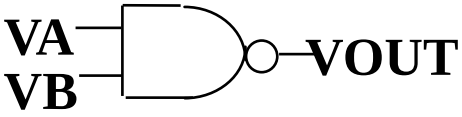


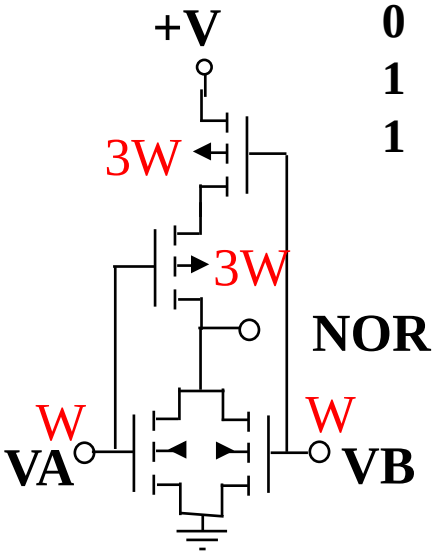
CMOS NOR AND NAND

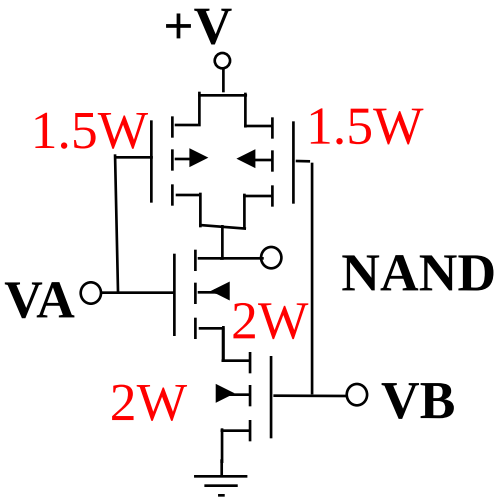
The design guideline is that the logic gate under consideration should have the same rise time and fall time as the inverter (after we adjusted the inverter for equal rise time and fall time. Assume L's are the same. $(W/L)_{pullup}$ = ~ 1.5 $(W/L)_{pulldown}$ based on mobility only



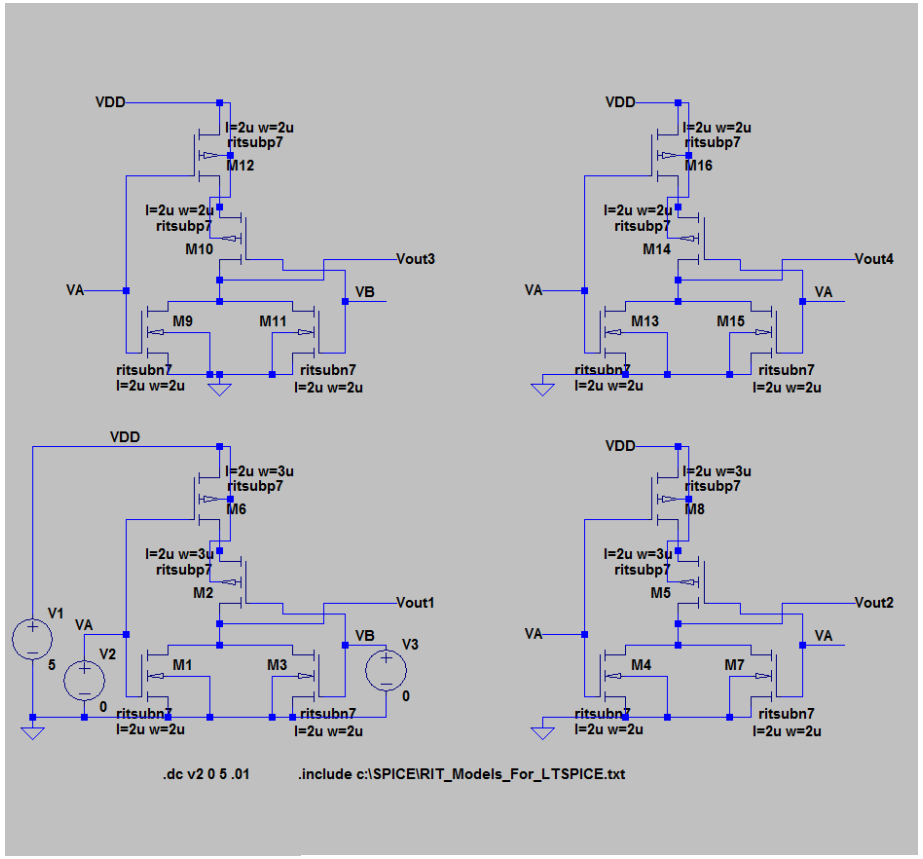
VA	VB	NOR	NAND
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

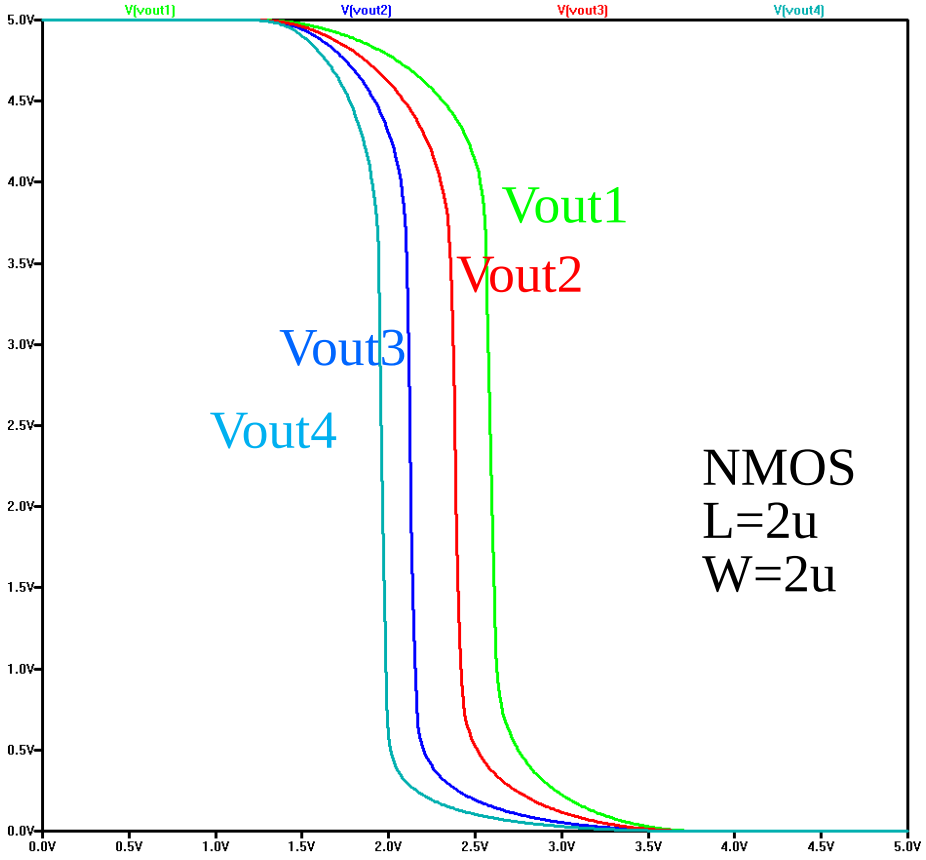






VTC FOR CMOS NOR AND NAND





Vout1 PMOS L=2u, W=3u, VA Sweep 0 to 5, VB=zero

Vout1 PMOS L=2u, W=3u, VA Sweep 0 to 5, VB=VA

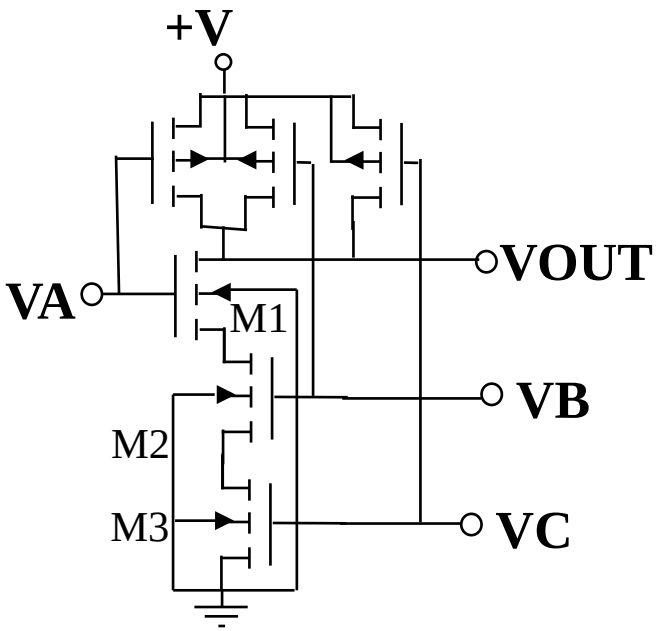
Vout1 PMOS L=2u, W=2u, VA Sweep 0 to 5, VB=zero

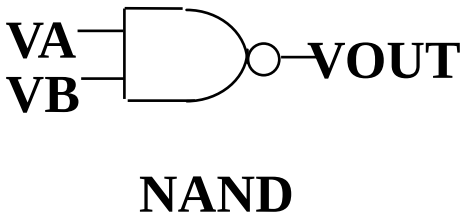
Vout1 PMOS L=2u, W=2u, VA Sweep 0 to 5, VB=VA

VTC FOR 3-INPUT NAND

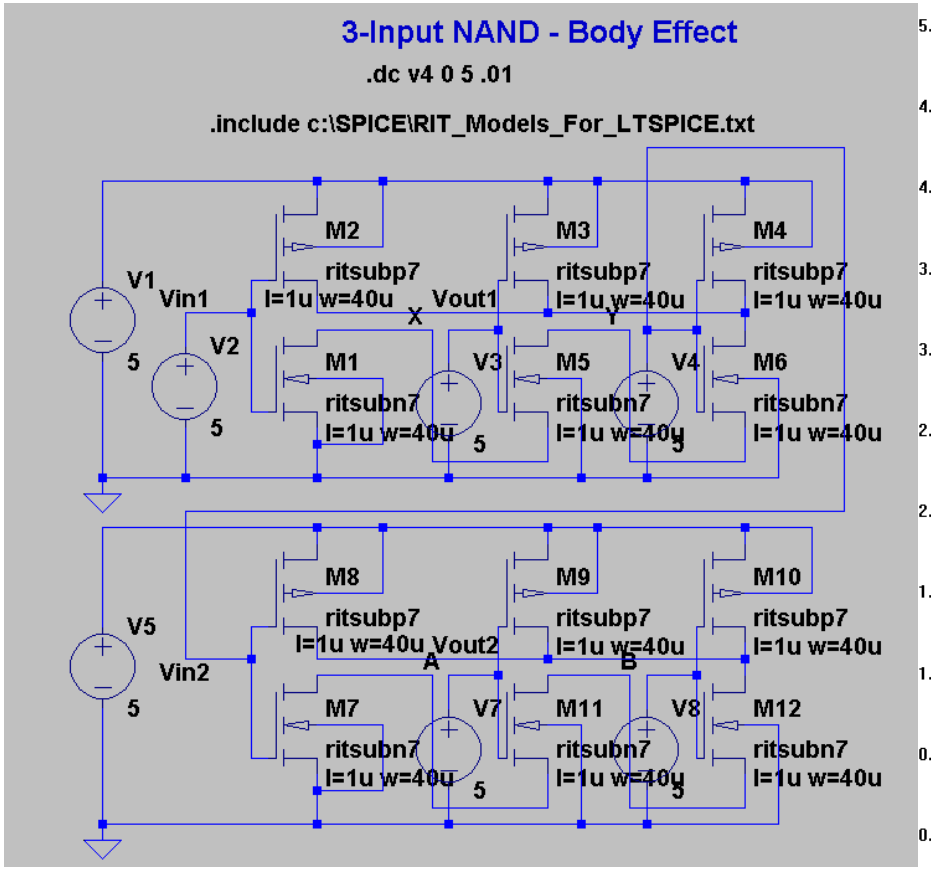
The three NMOS transistors each have different source to substrate voltages which will change the threshold voltage of those transistors and as a result will change the VTC depending on which transistors are switching. This causes a horizontal shift in the VTC.

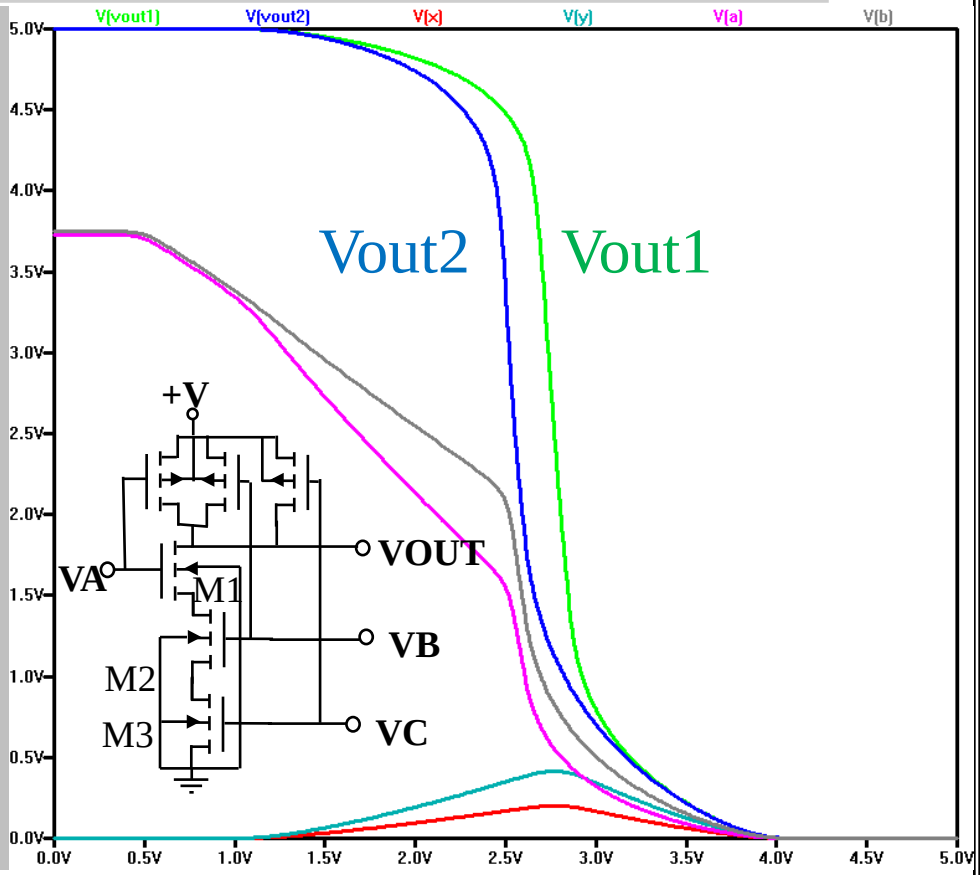
VA	VB	VC	NAND
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0





3-INPUT NAND



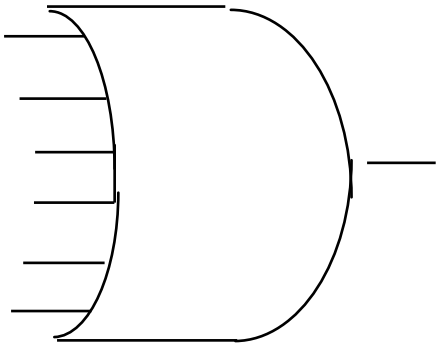


Vout1 has M2 and M3 NMOS on and M1 NMOS switching
Vout2 has M1 and M2 NMOS on and M3 NMOS switching
Other combinations are also possible.

FAN IN AND FAN OUT CONSIDERATIONS

Fan in refers to the number of inputs to a gate. It is common to have up to 8 inputs. In CMOS this implies that there are 8 transistors in parallel and 8 transistors in series. The 8 in parallel is not necessarily a problem but the 8 in series is because of the body effect on the threshold voltage of some of the transistors if they are all in the same well (at Vss or Vdd for p-well or n-well respectively)

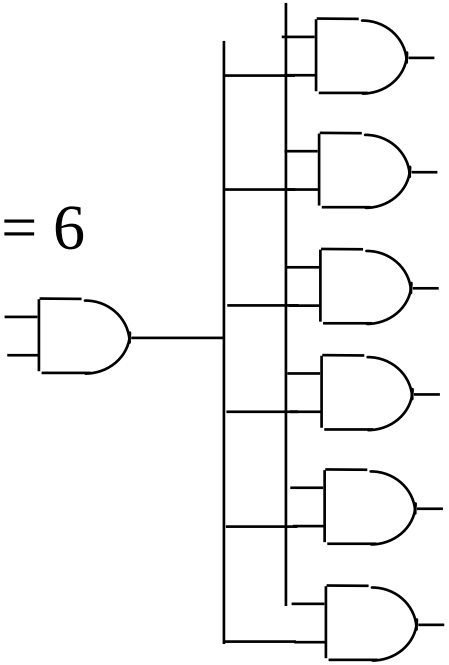
Fan-In = 6



FAN OUT CONSIDERATIONS

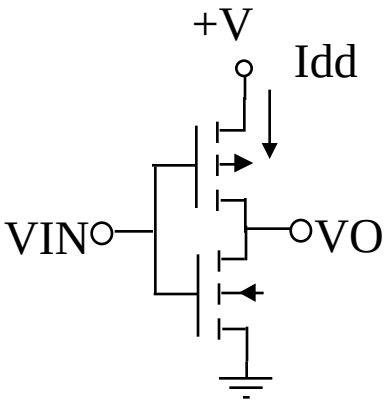
Fan out refers to the number of gates connected to the output of a gate. Each gate adds more capacitance to be charged or discharged during switching which has implications on rise time, fall time and gate delay. The size (W and L) of the MOSFETS can be made to keep the gate delay small.

Fan-Out = 6

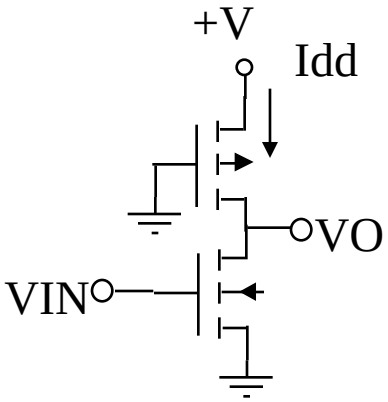


PSEUDO – CMOS

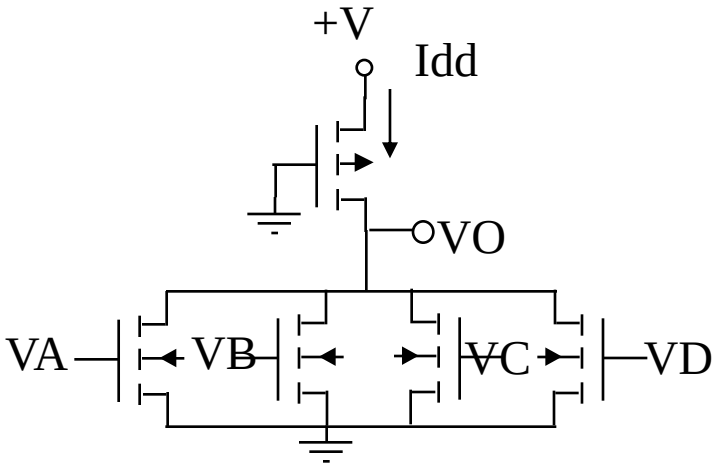
There are situations where we want a large number of inputs. Rather than have CMOS where there will be many transistors in series (which will not work) we can use a single PMOS/NMOS transistor that is always on.



CMOS



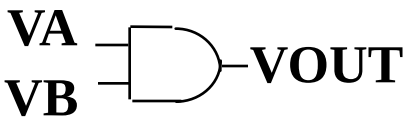
Pseudo NMOS Inverter



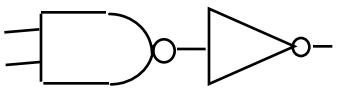
4 Input NOR

OTHER BASIC LOGIC GATES

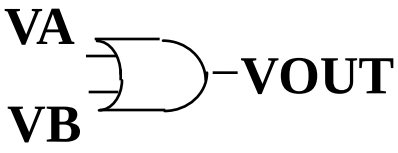
AND



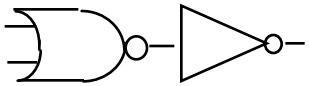
VA	VB	VOUT
0	0	0
0	1	0
1	0	0
1	1	1



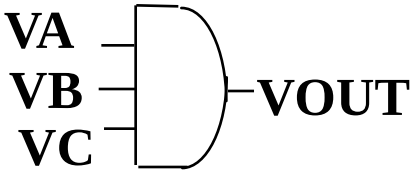
OR



VA	VB	VOUT
0	0	0
0	1	1
1	0	1
1	1	1

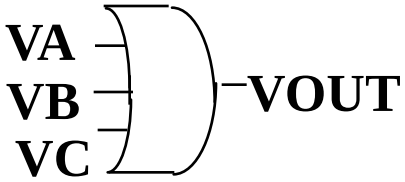


3 INPUT AND



VA	VB	VC	VOUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

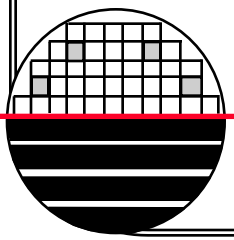
3 INPUT OR



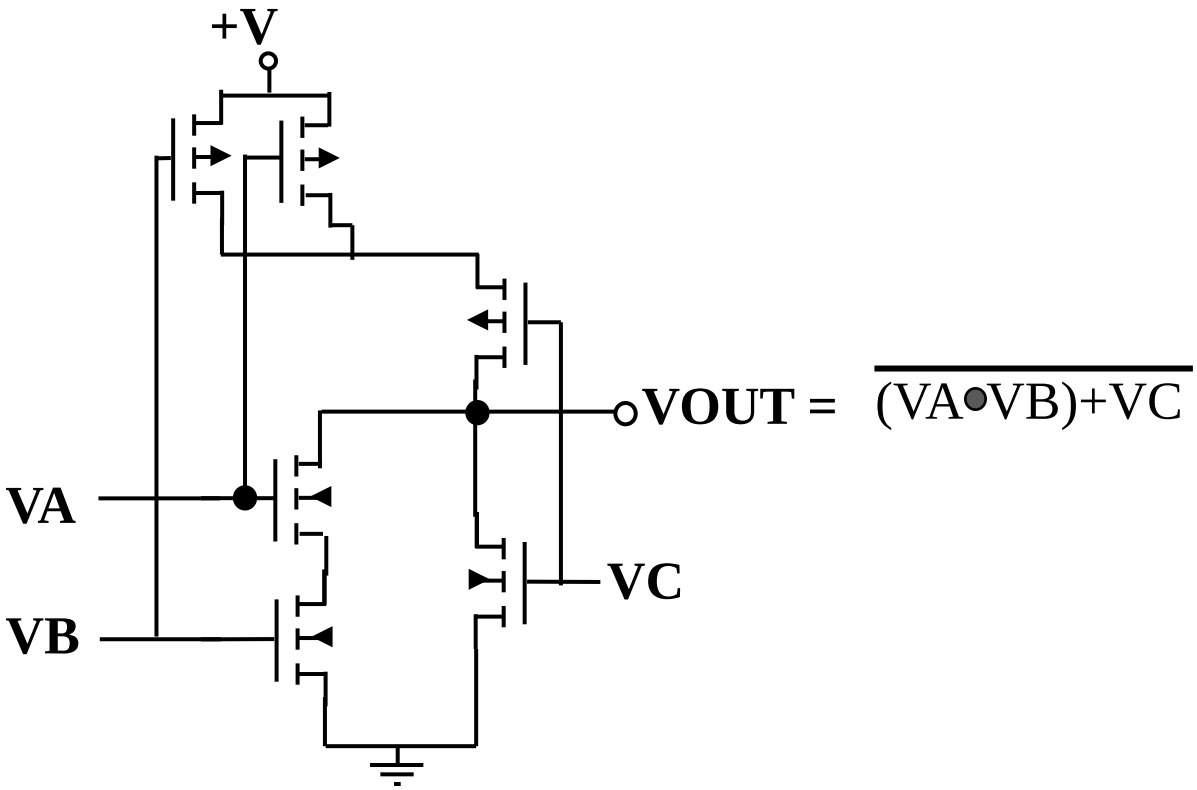
VA	VB	VC	VOUT
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

OTHER BASIC LOGIC GATE REALIZATIONS

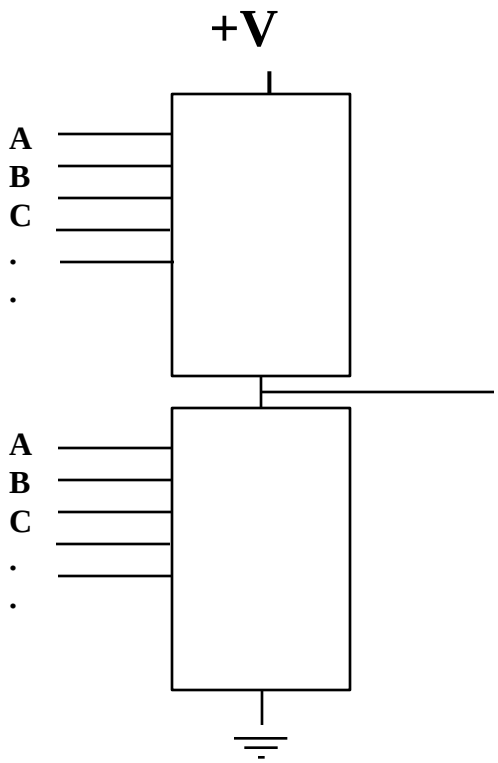
Enhancement Load
V++ Gate Enhancement Load
Depletion Load
Pseudo CMOS NAND, NOR
CMOS AND-OR-INVERT Gate
Generalized Complex CMOS Gate
More Complex Gates, XOR, MUX,
Encoder, Decoder, etc.



CMOS AND-OR-INVERT GATE



GENERALIZED COMPLEX GATE



$$F = \overline{(VA+VB) \bullet VC}$$

Design a gate that provides this output

EXCLUSIVE OR (XOR) DESIGN EXAMPLE

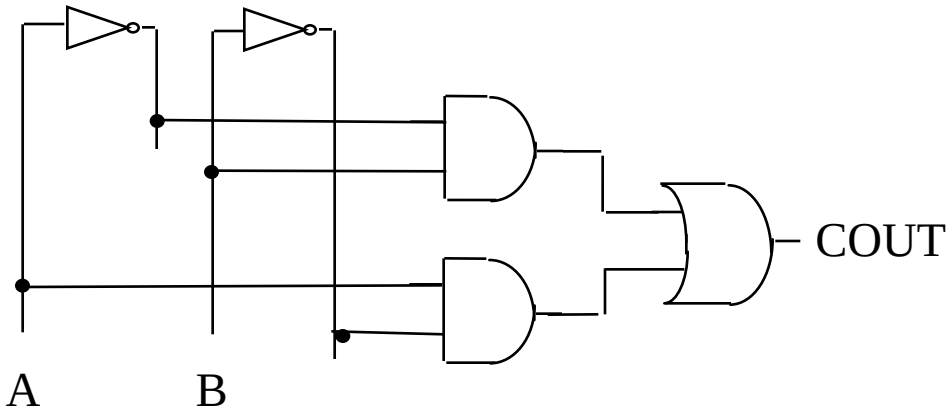
Functional Description – This digital logic circuit returns a true (high) value when one of two inputs is high and returns a false (zero) otherwise.

Truth Table

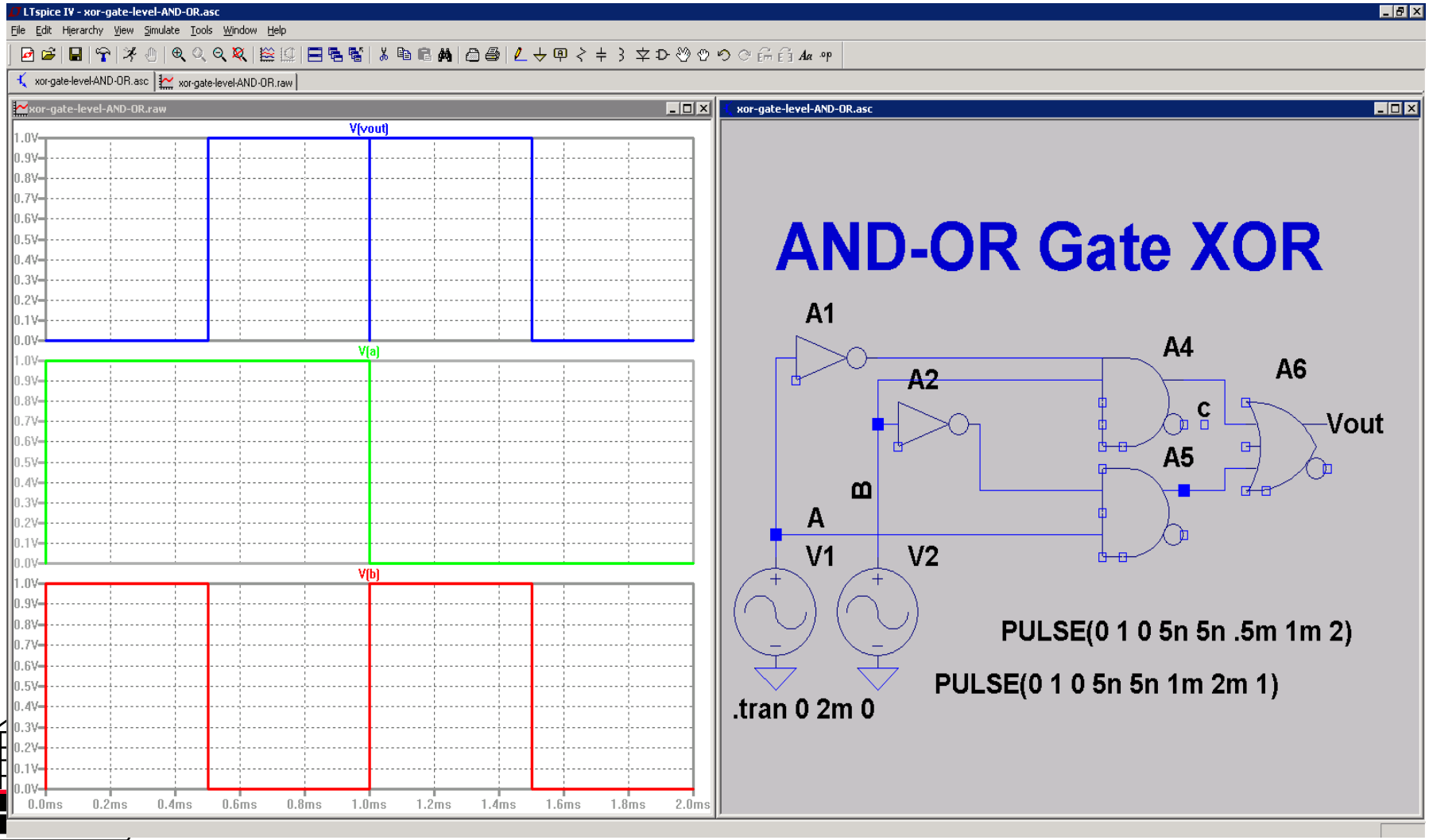
Exclusive OR
XOR

VA	VB	VOUT
0	0	0
0	1	1
1	0	1
1	1	0

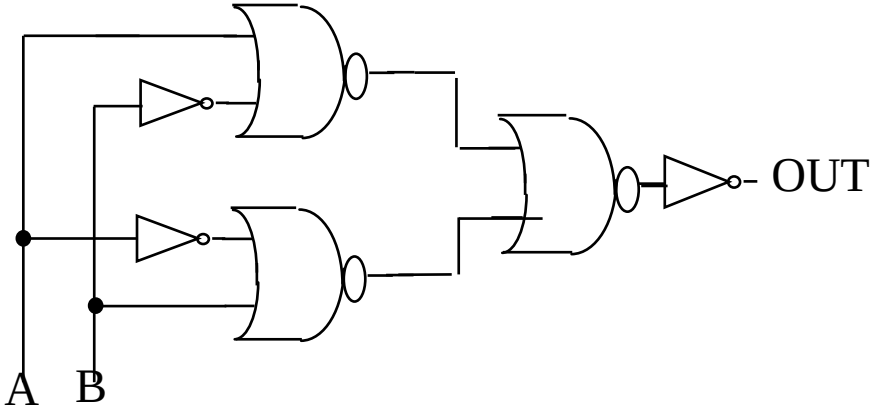
Gate Level Design



GATE LEVEL SIMULATION OF XOR – AND/OR



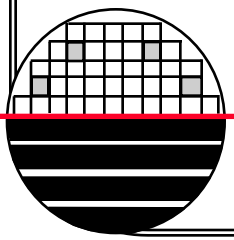
NOR CIRCUIT REALIZATION FOR XOR



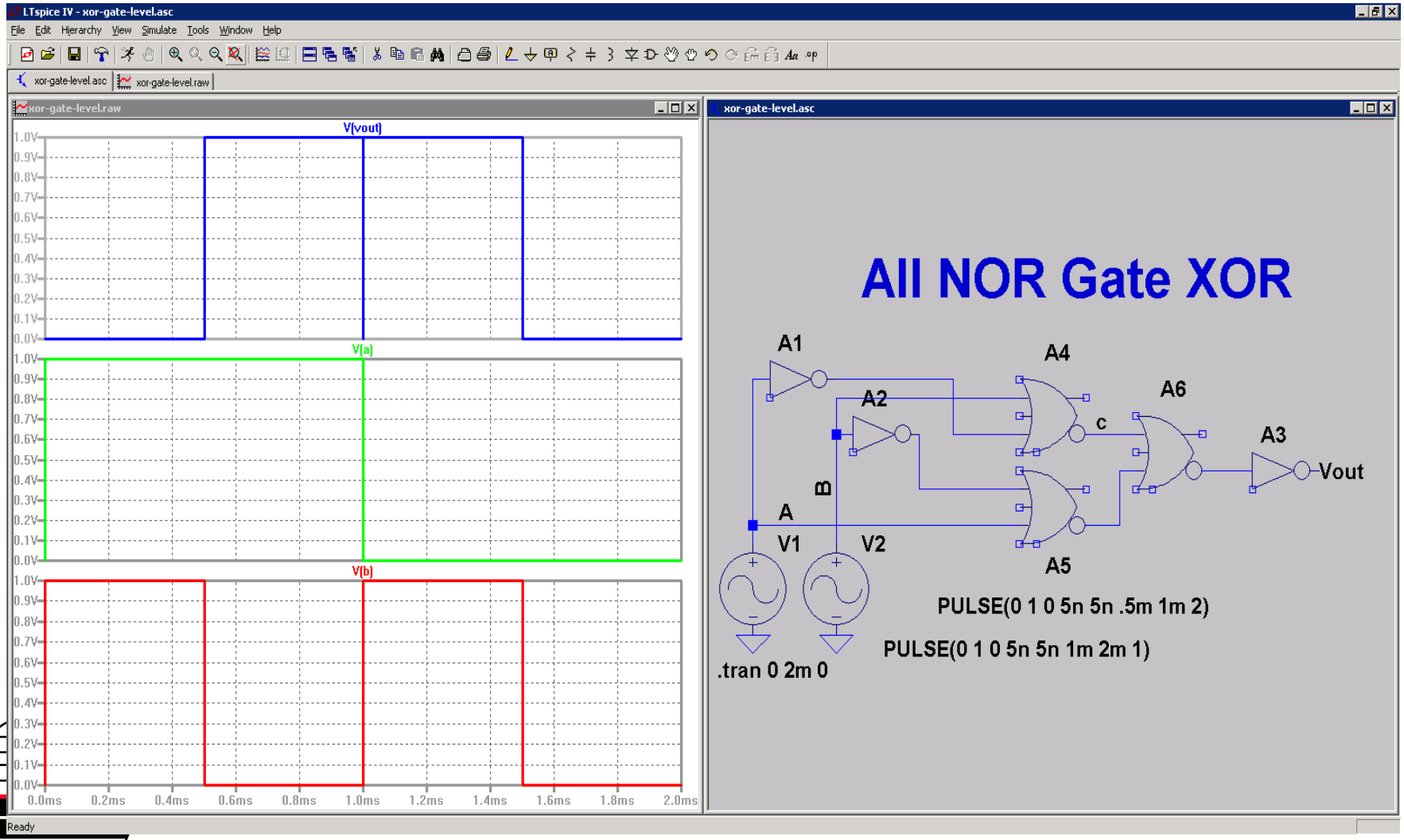
Exclusive OR

XOR

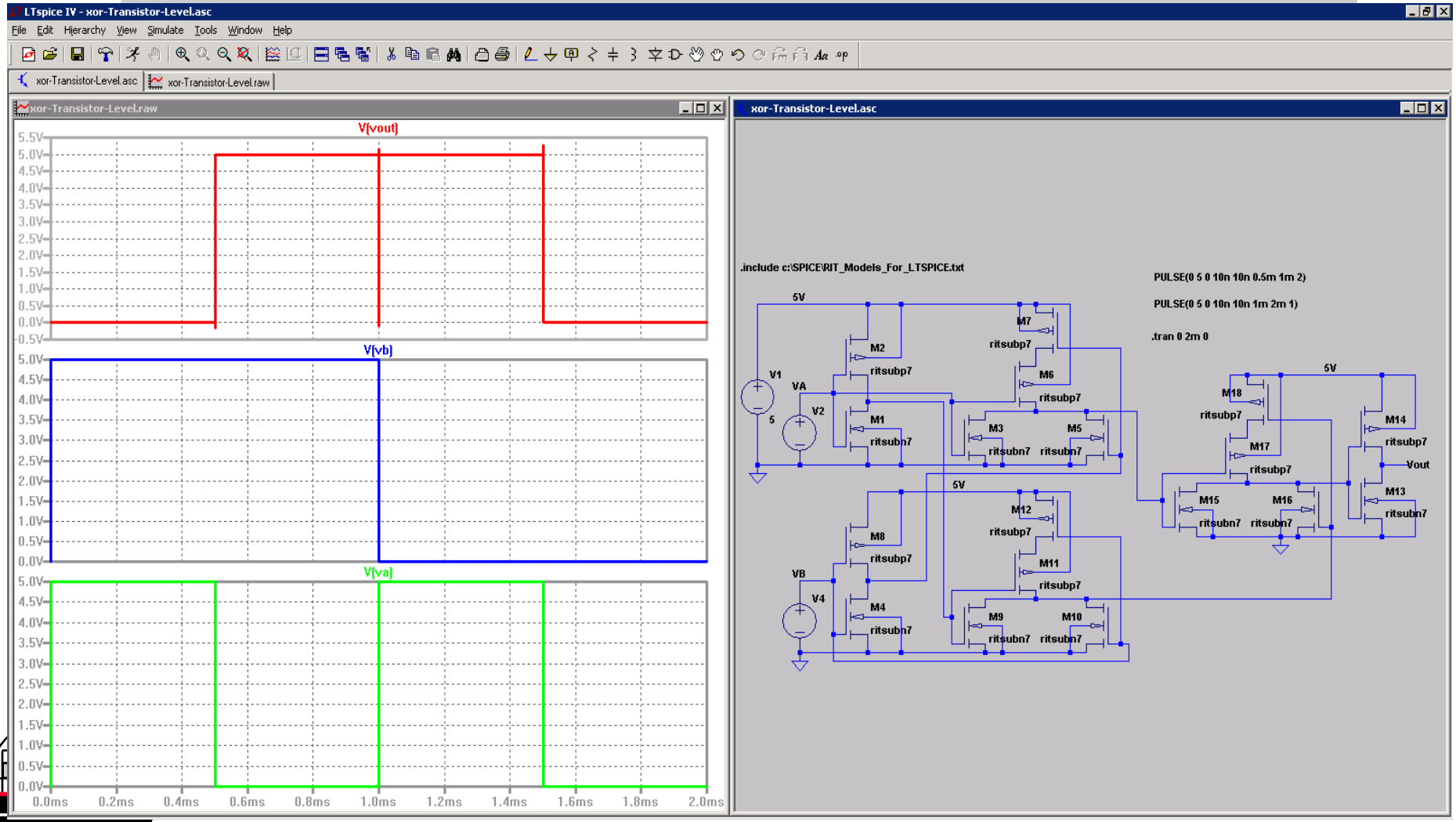
VA	VB	VOUT
0	0	0
0	1	1
1	0	1
1	1	0



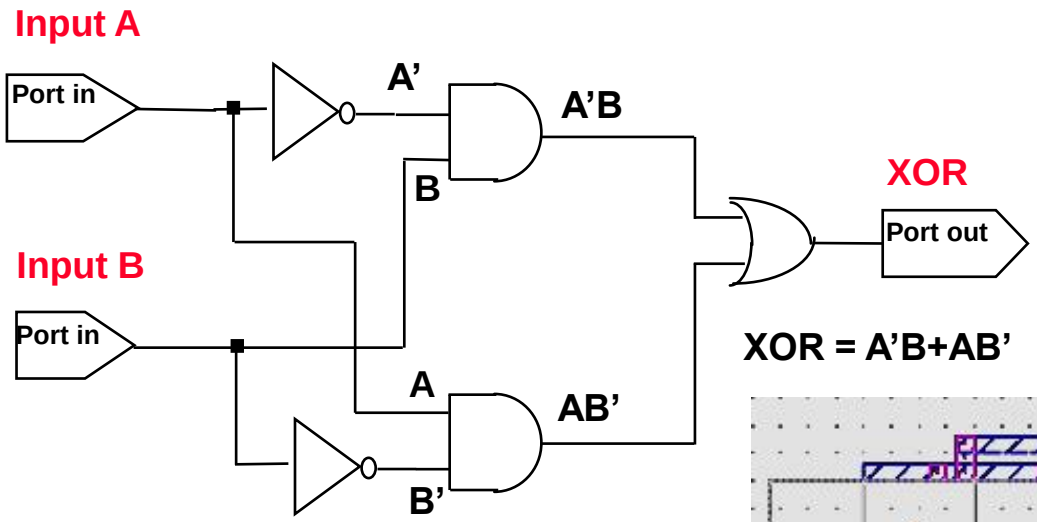
GATE LEVEL SIMULATION OF XOR – ALL/NOR



TRANSISTOR LEVEL SIMULATION OF XOR – ALL/NOR

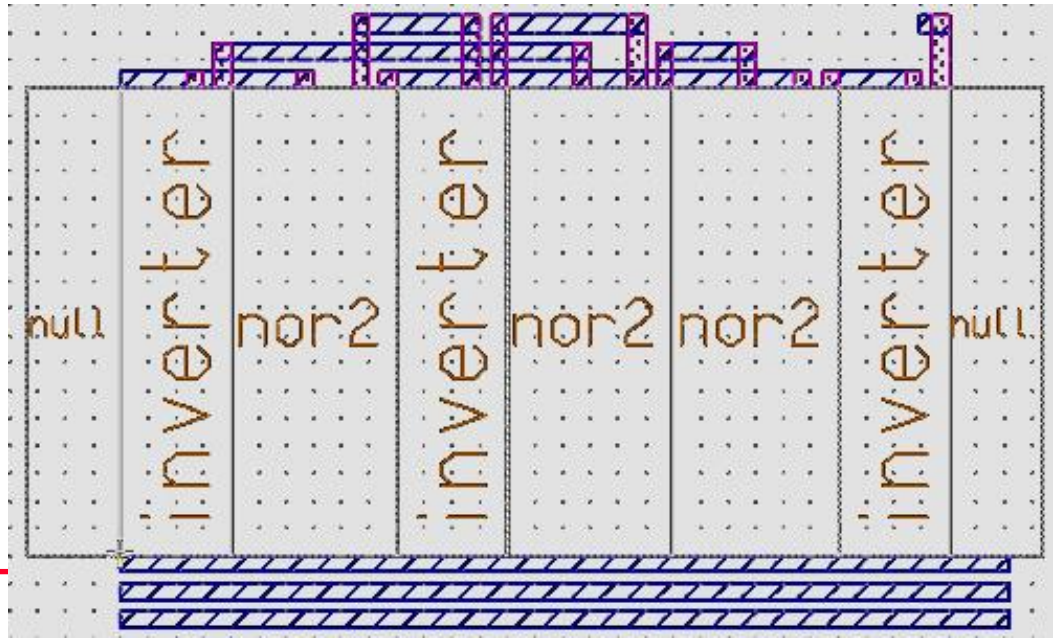


BASIC CELL XOR

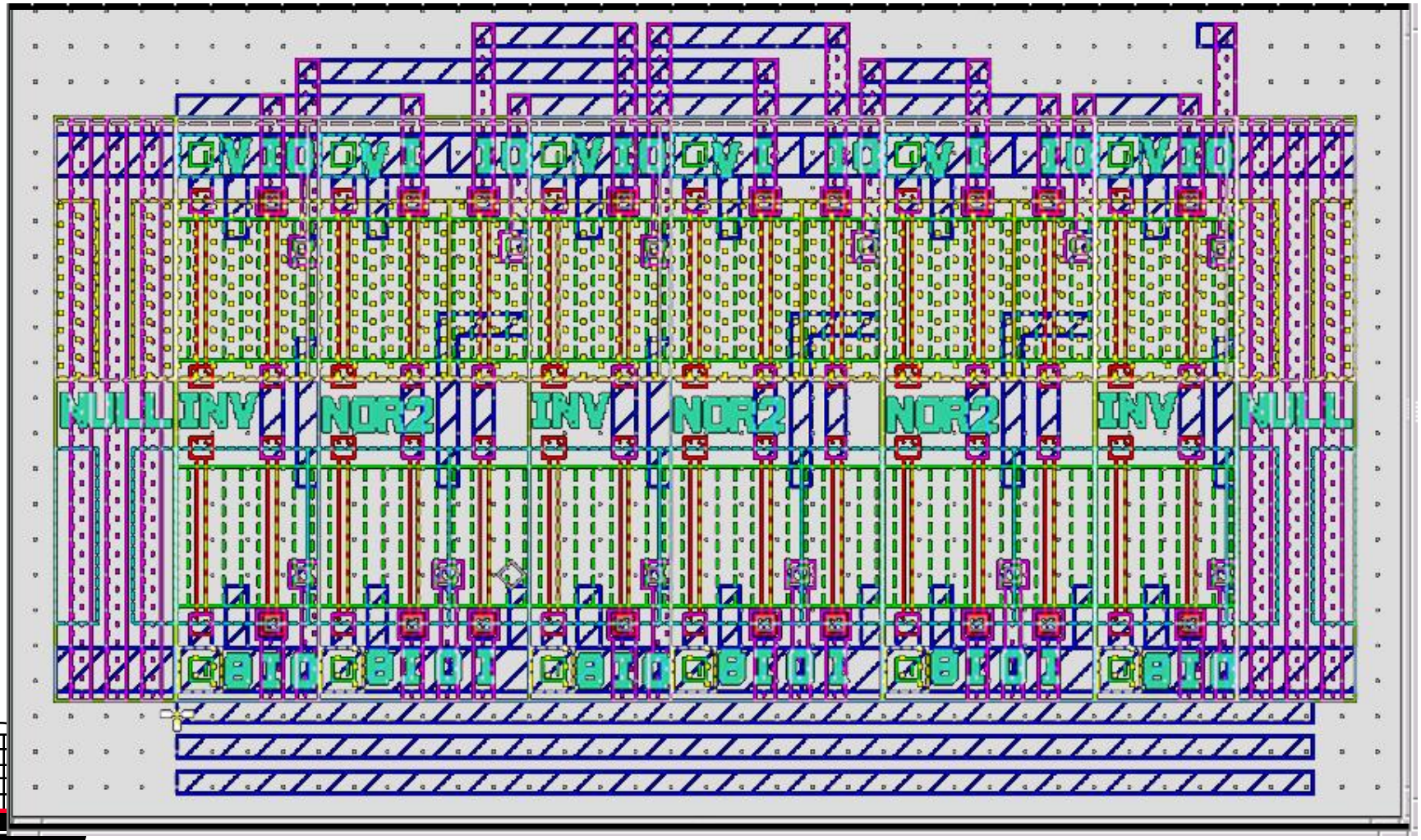


XOR = A'B+AB'

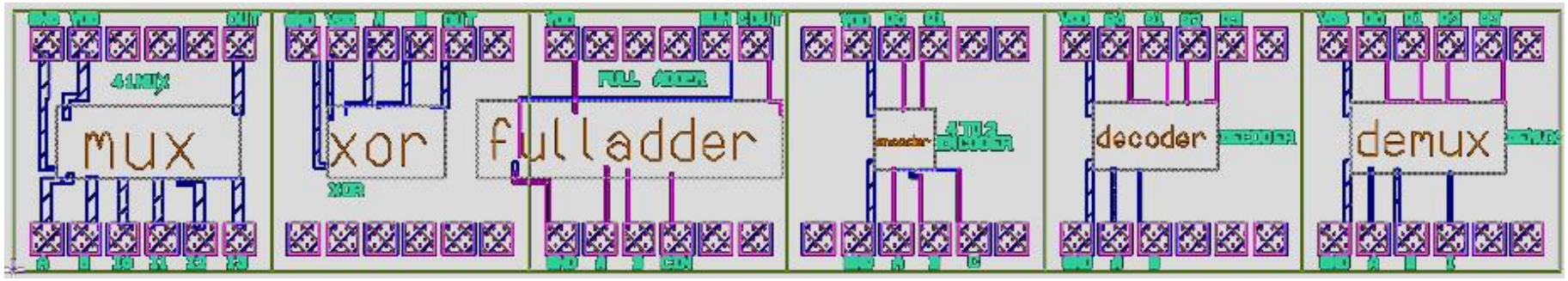
XOR



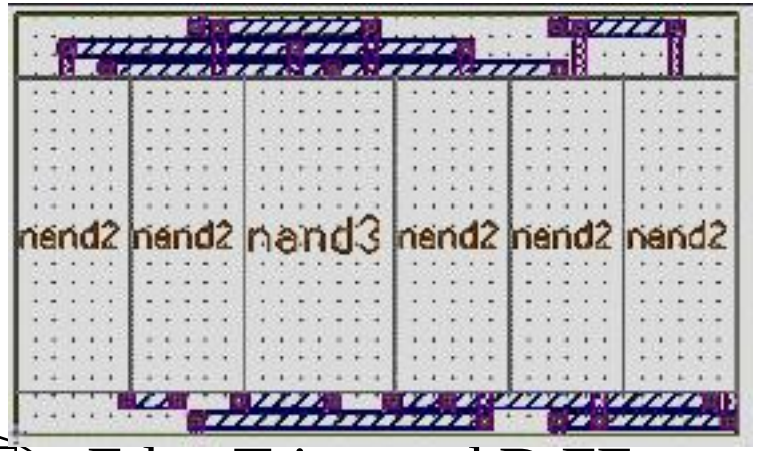
LAYOUT FOR XOR



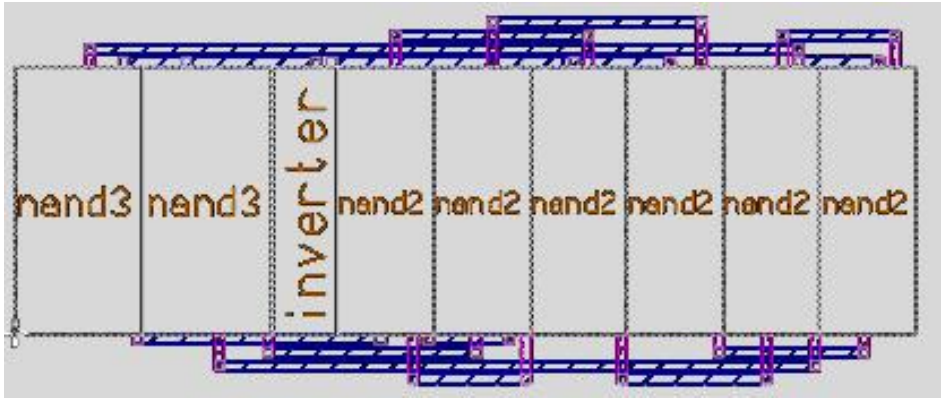
BASIC DIGITAL CELLS WITH PADS



Multiplexer XOR Full Adder Encoder Decoder Demux

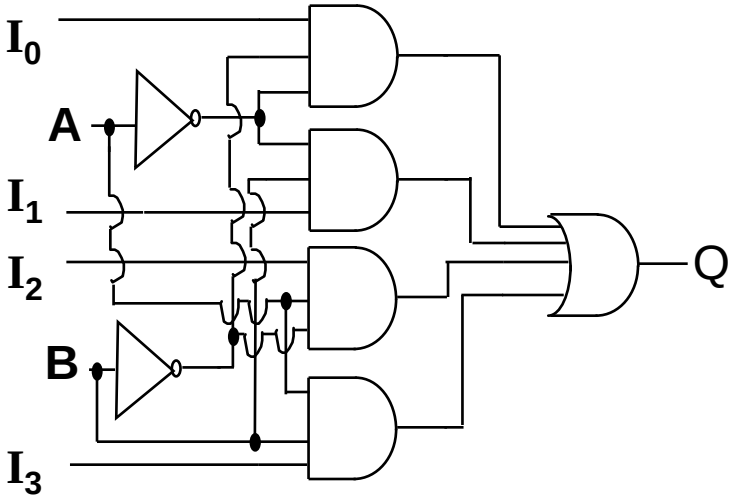


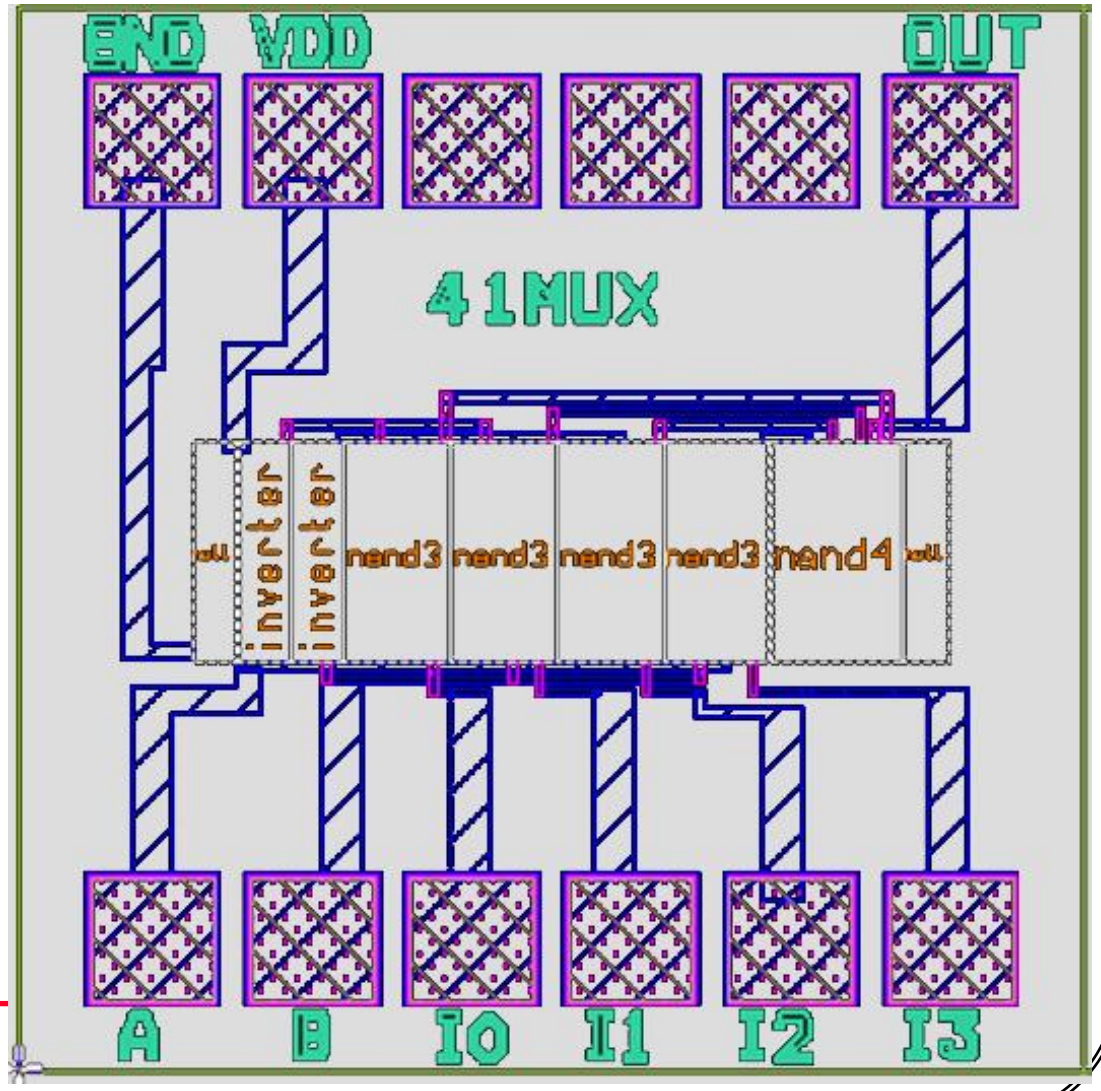
Edge Triggered D FF



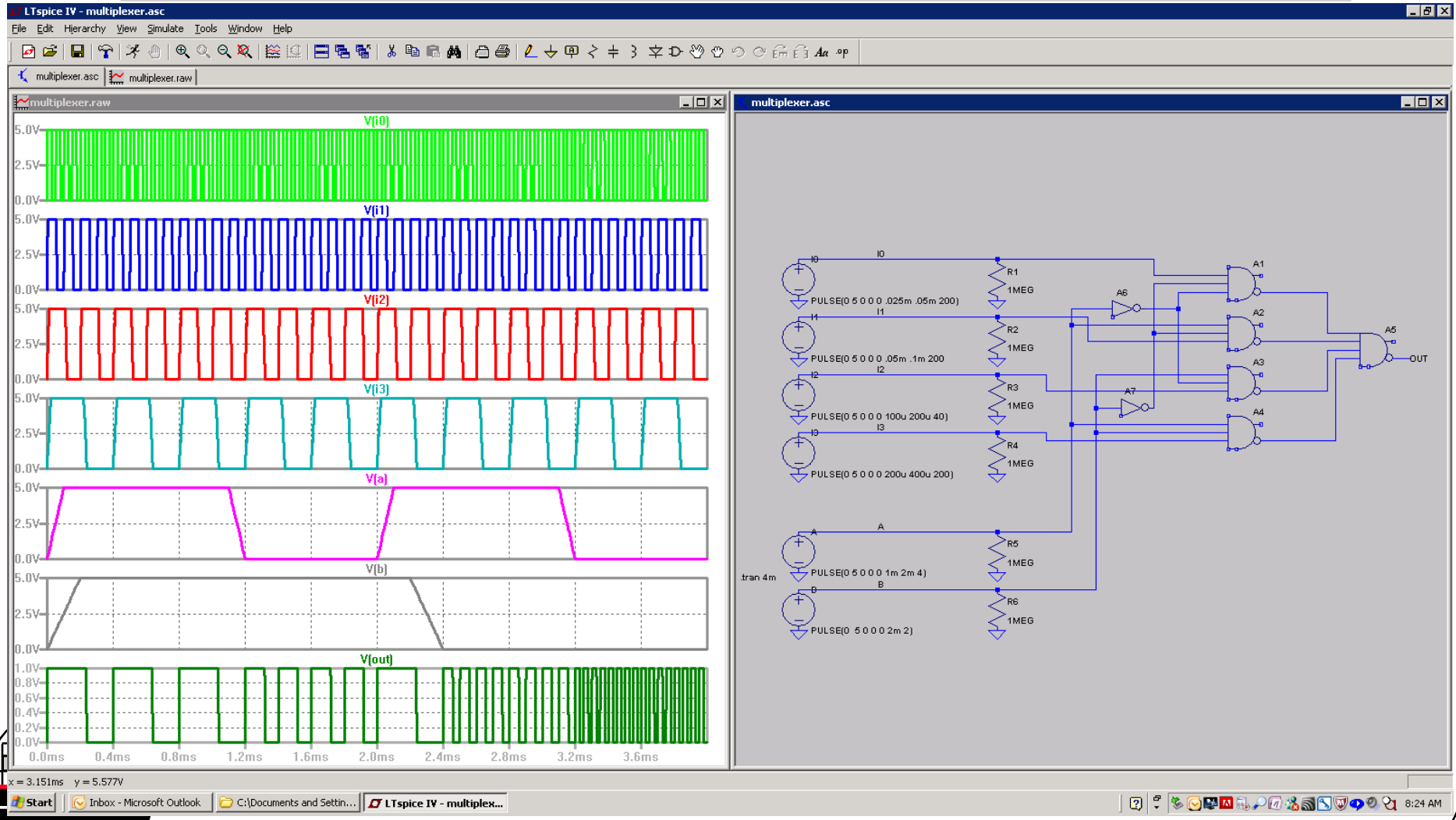
JK FF

4 TO 1 MULTIPLEXER





4 TO 1 MUX - GATE LEVEL SIMULATION



ADDITION IN BINARY

IN BASE 10

```
  7
 +2
 ___
  9
```

IN BINARY

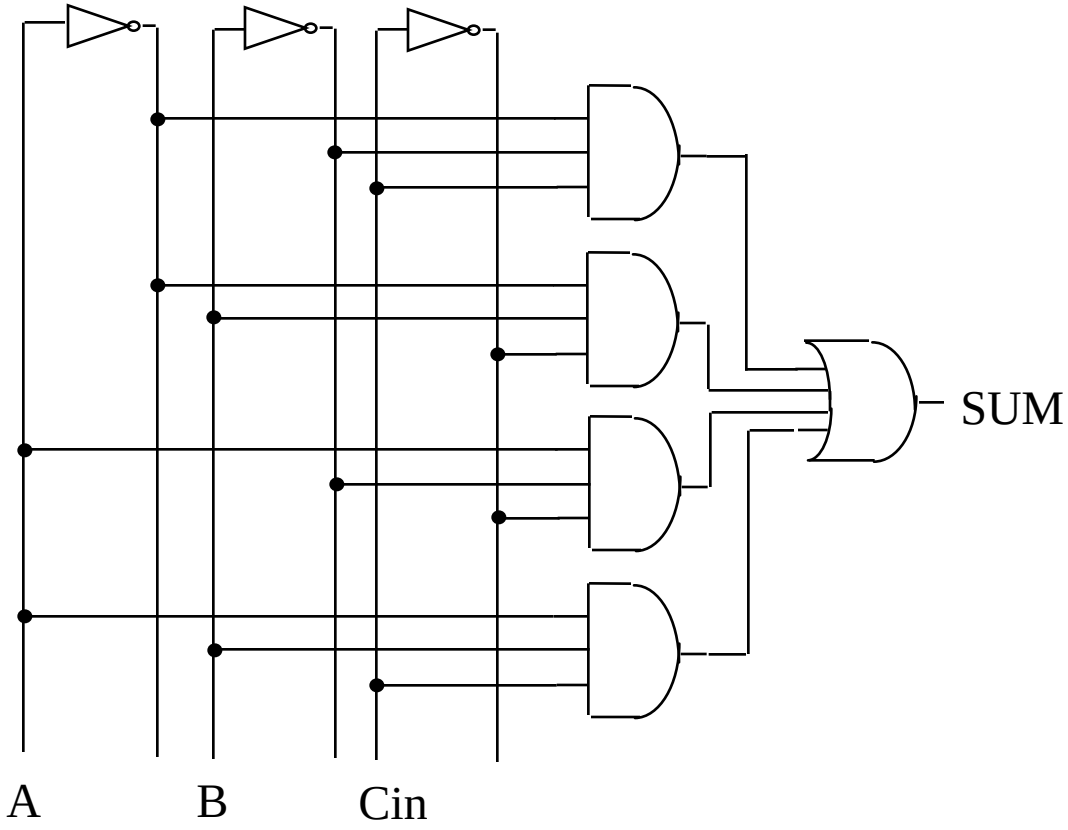
```
11          CARRY
0111
0010
____
1001        SUM
```

0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

TRUTH TABLE FOR ADDITION RULES

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

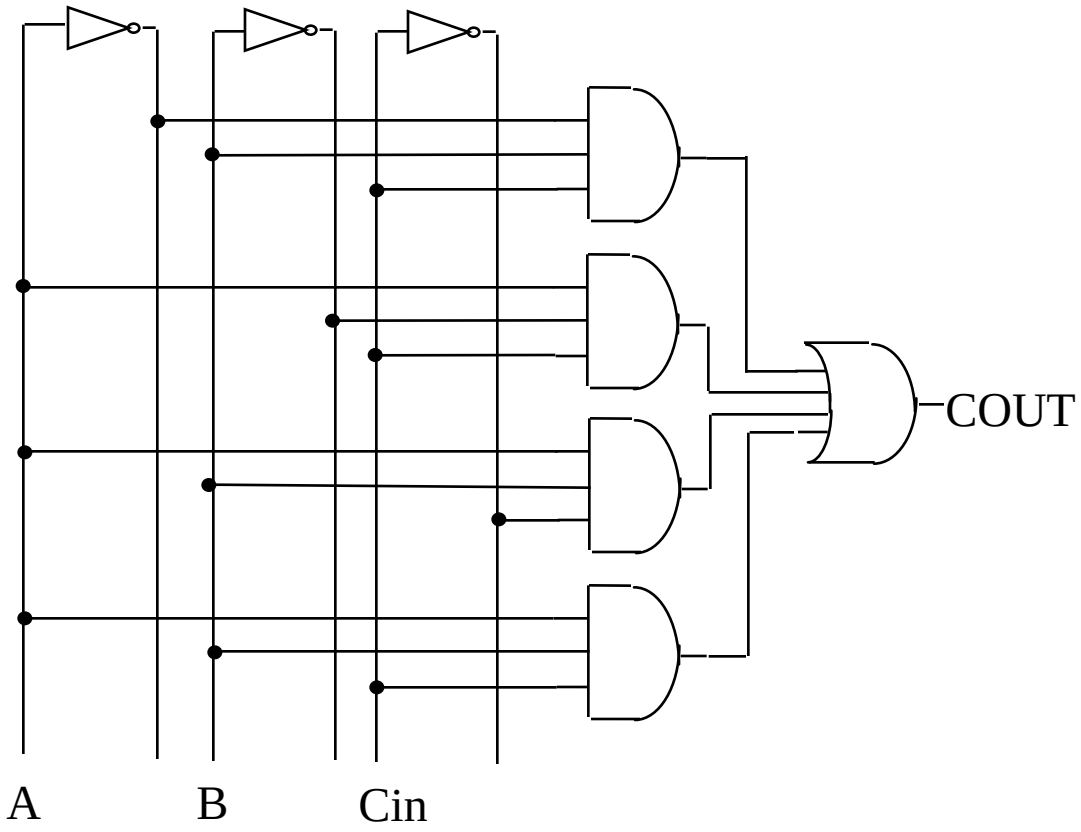
AND-OR CIRCUIT REALIZATION OF SUM



TRUTH TABLE
FOR ADDITION
RULES

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

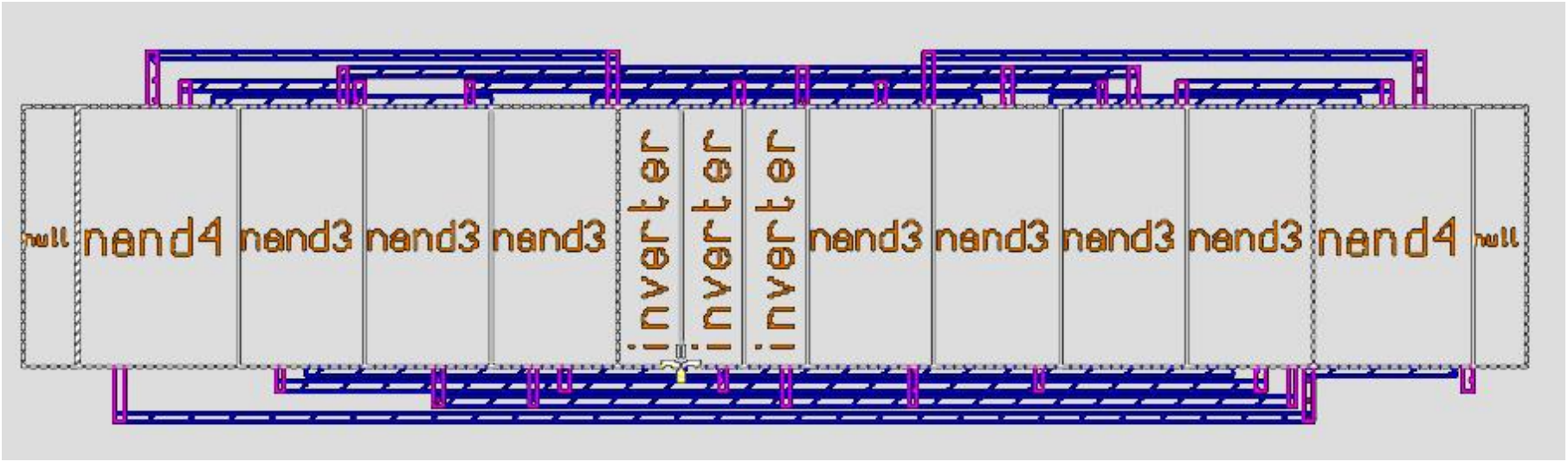
CIRCUIT REALIZATION OF CARRY OUT (COUT)



TRUTH TABLE
FOR ADDITION
RULES

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL ADDER


well
nand4
nand3
nand3
nand3
inverter
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nand3
nand3
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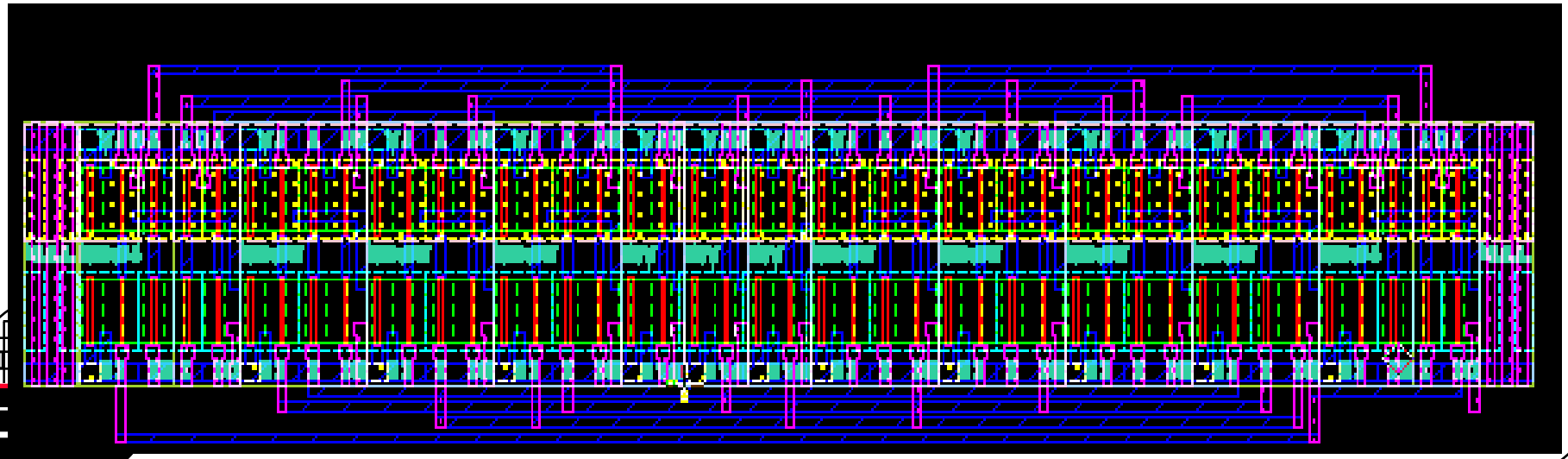
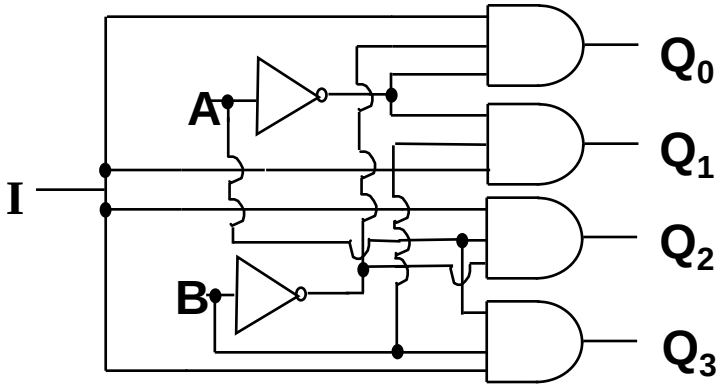
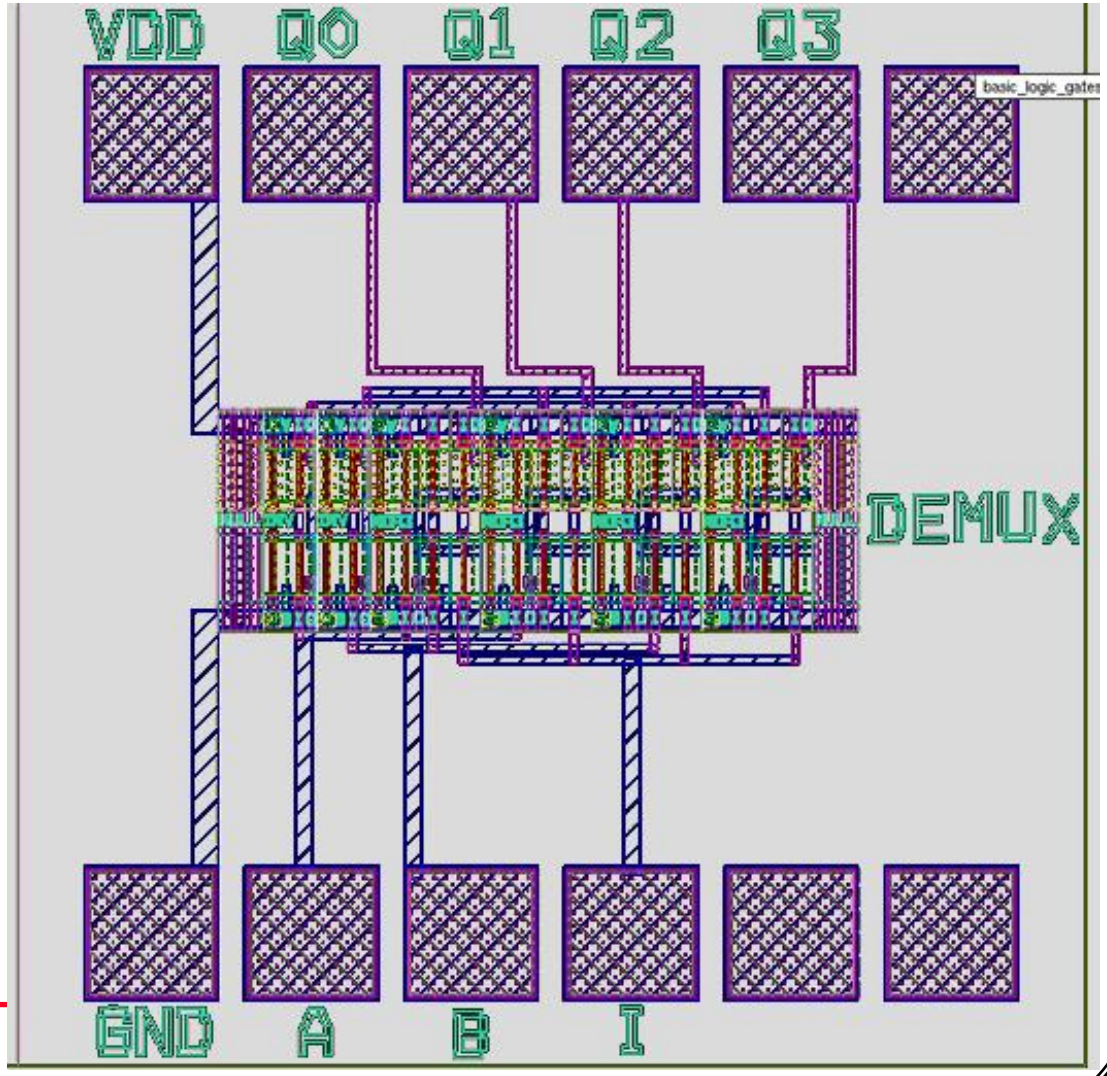
nand3
nand4
well

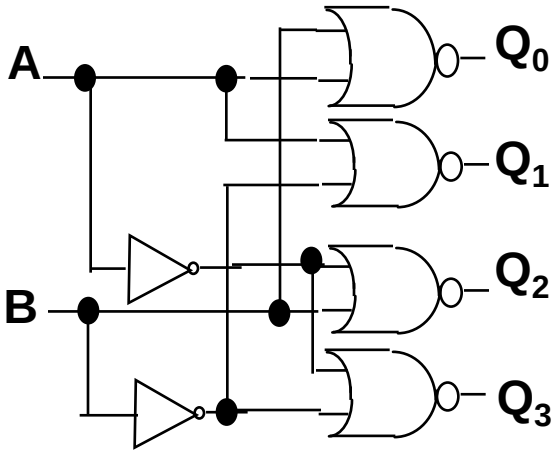


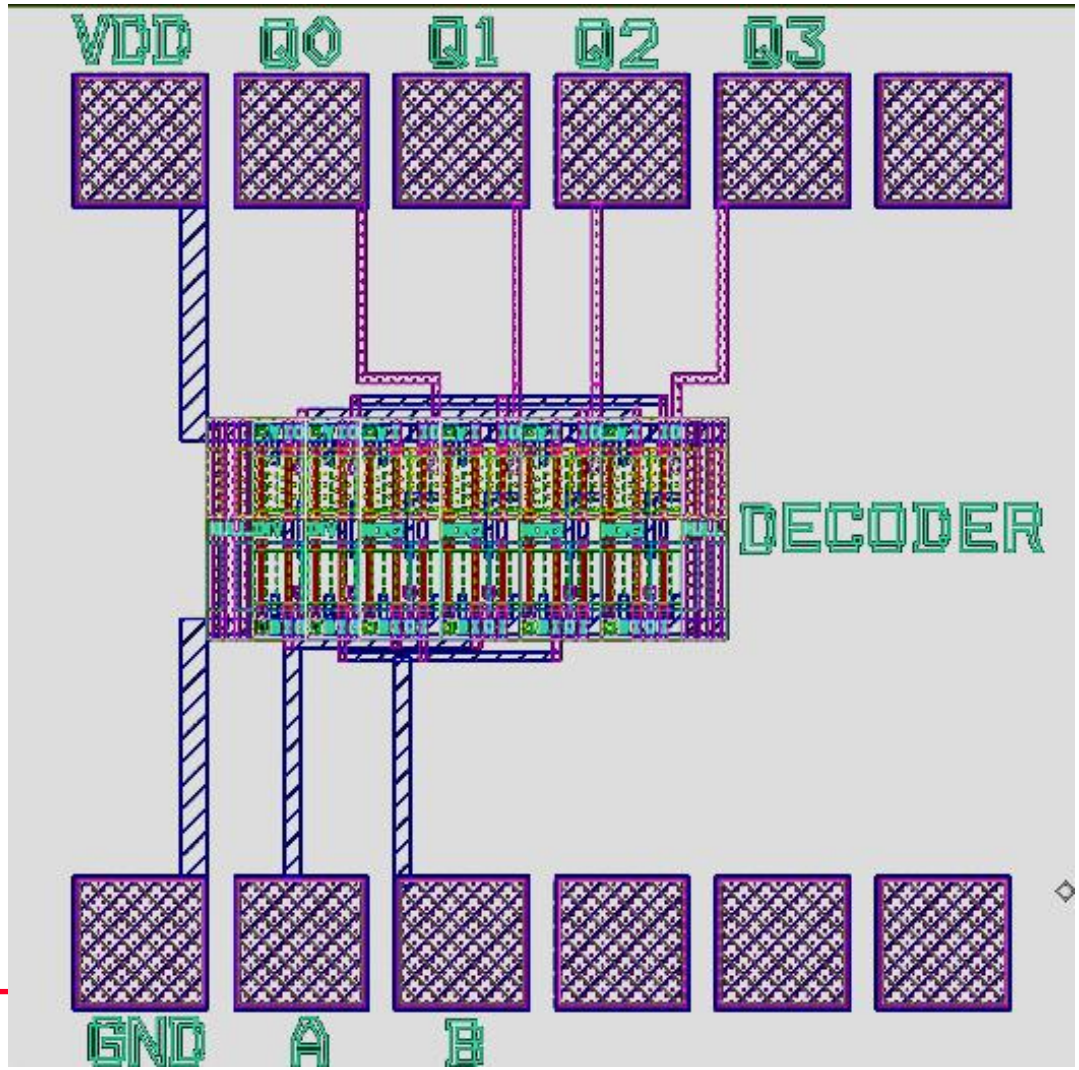
1 TO 4 DEMULTIPLEXER



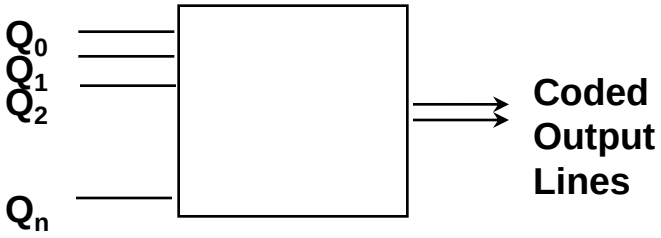


DECODER





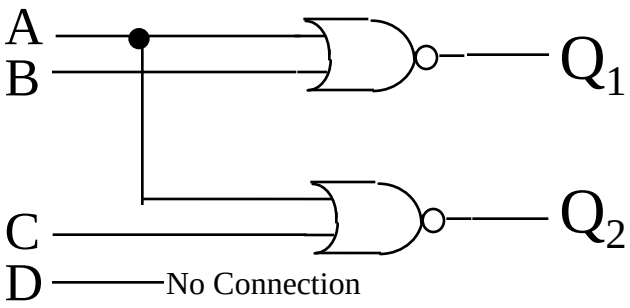
ENCODER

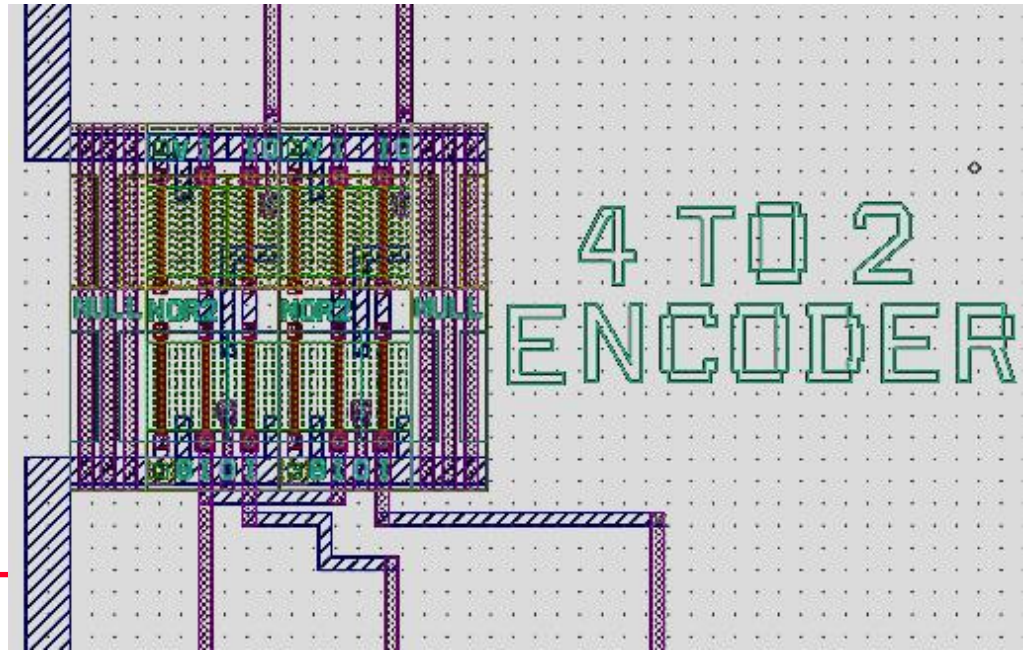


Digital Encoder

512 inputs can be coded into 9 lines which is a more dramatic benefit

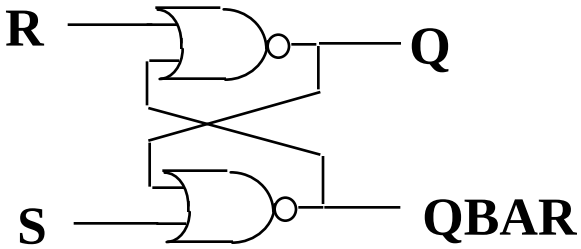
A	B	C	D	Q0	Q1
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1





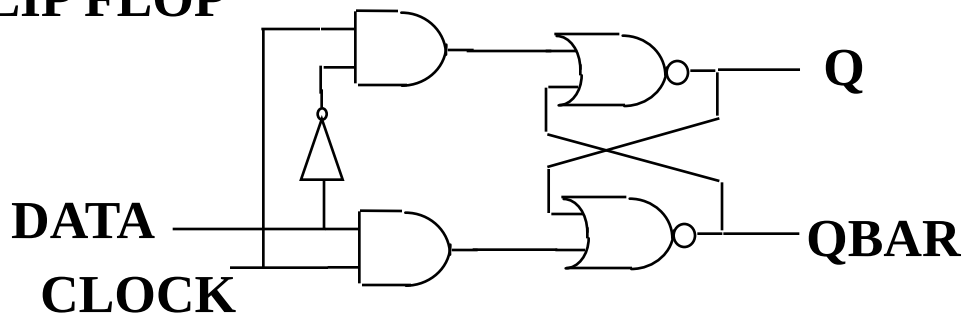
FILP-FLOPS

RS FLIP FLOP



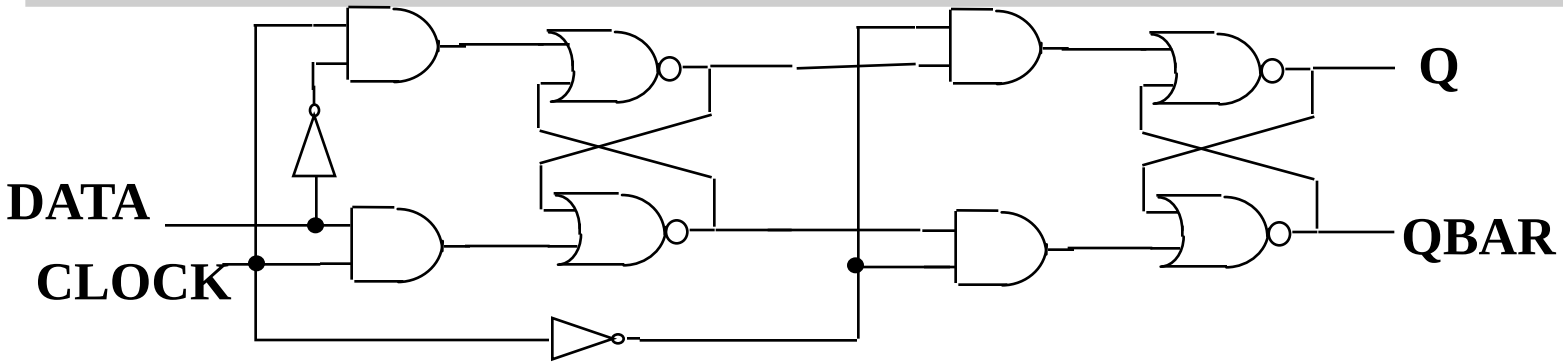
R	S	Q
0	0	Qn-1
0	1	1
1	0	0
1	1	INDETERMINATE

D FLIP FLOP

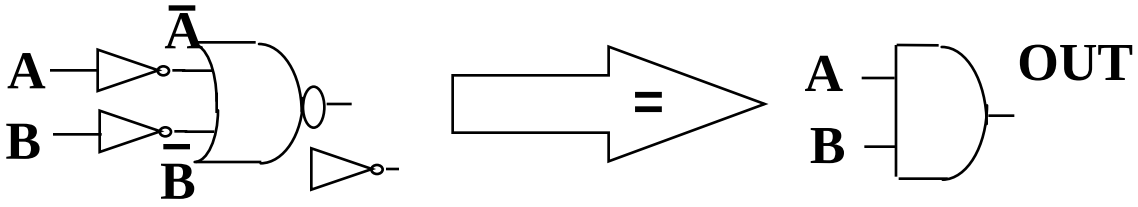


Q=DATA IF CLOCK IS HIGH
IF CLOCK IS LOW Q=PREVIOUS DATA VALUE

MASTER-SLAVE D FLIP FLOP

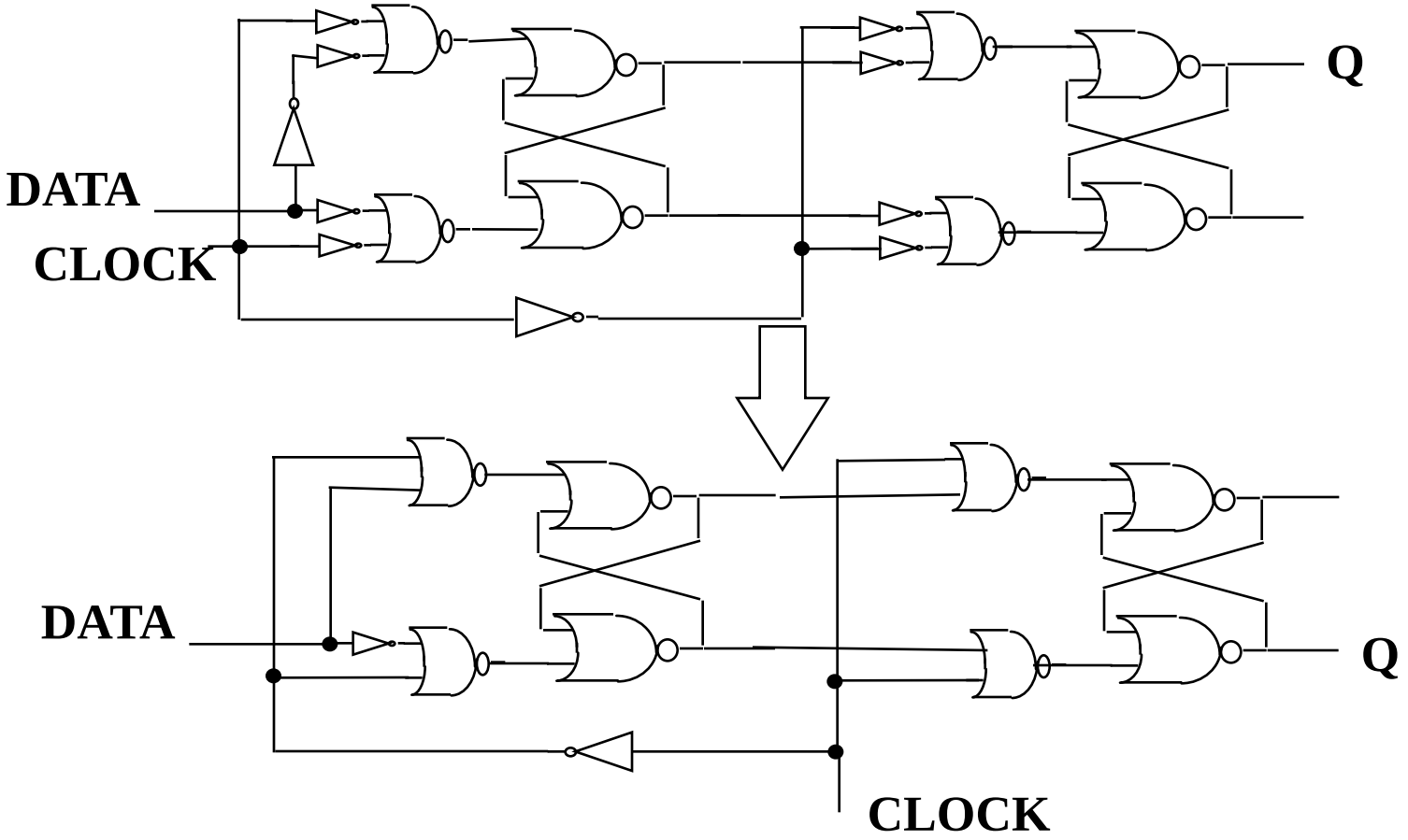


NEGATED INPUT NOR IS EQUAL TO AND



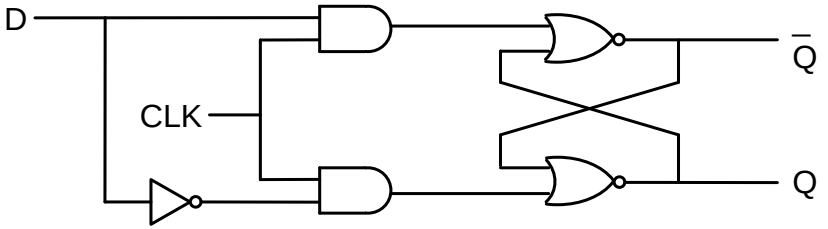
A	B	$\bar{A}$	$\bar{B}$	$\overline{OUT}$	OUT
0	0	1	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1

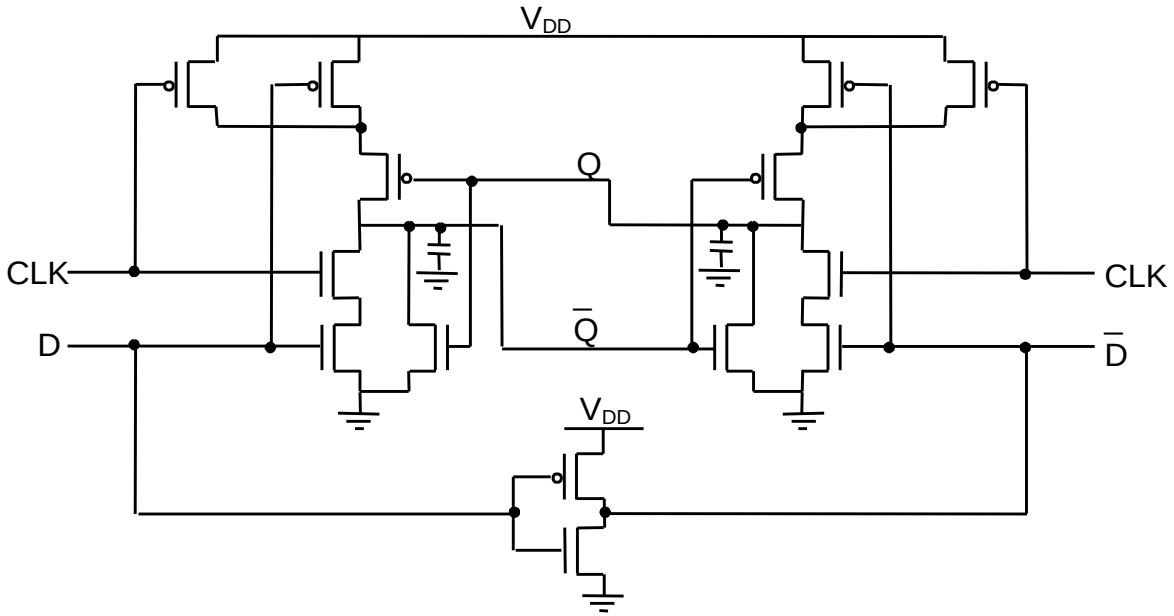
ALL NOR MASTER SLAVE D FLIP FLOP



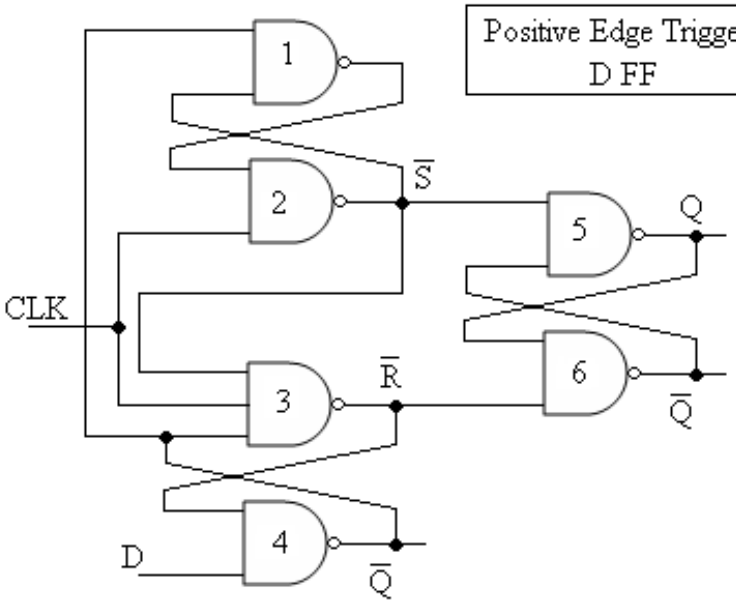
ALL NOR NMOS REALIZATION
ALLOWS FOR LOWER SUPPLY VOLTAGE

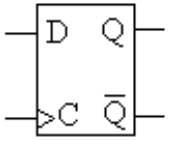
CMOS CLOCKED DATA LATCH USING AND-OR-INV



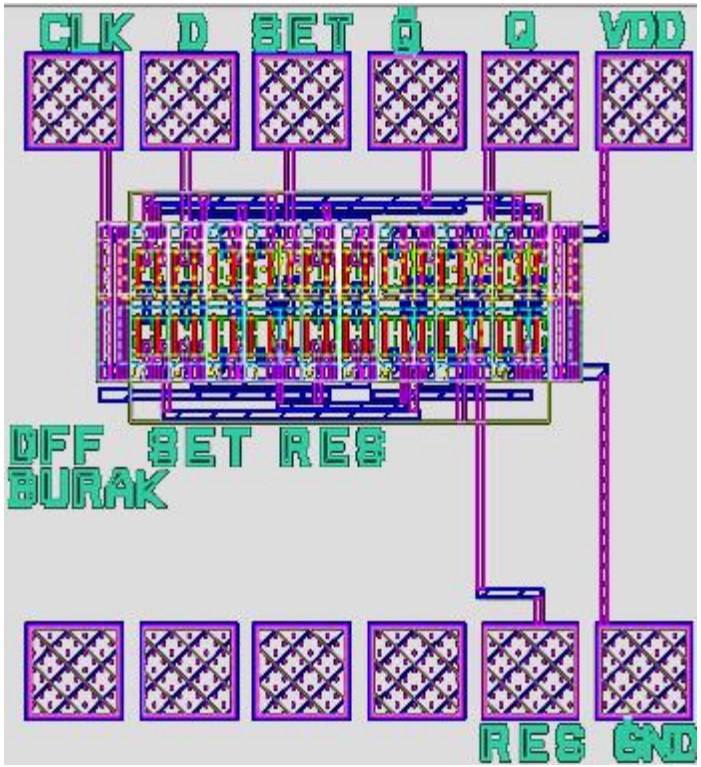


EDGE TRIGGERED D TYPE FLIP FLOP

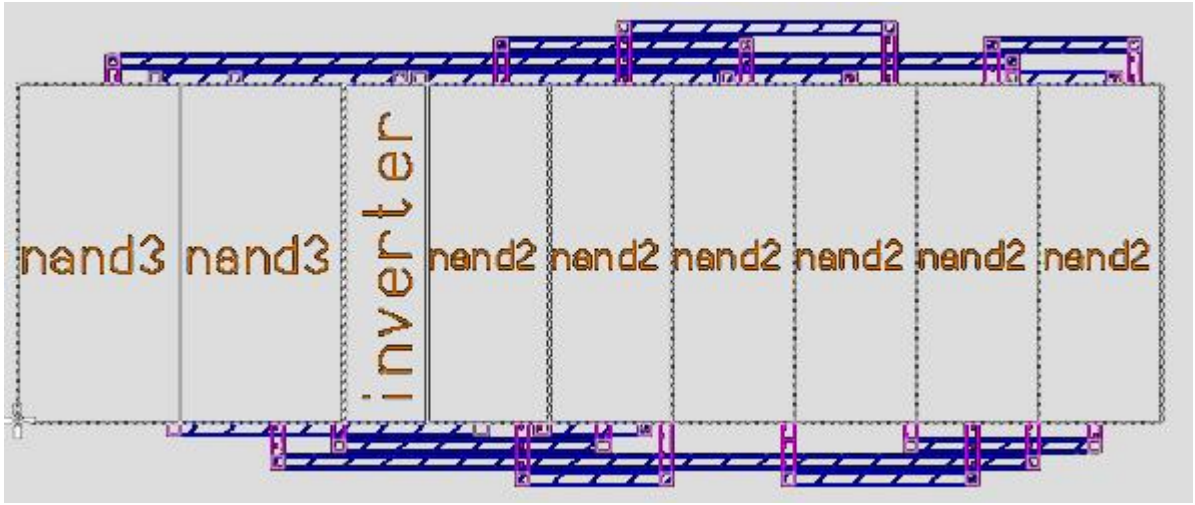


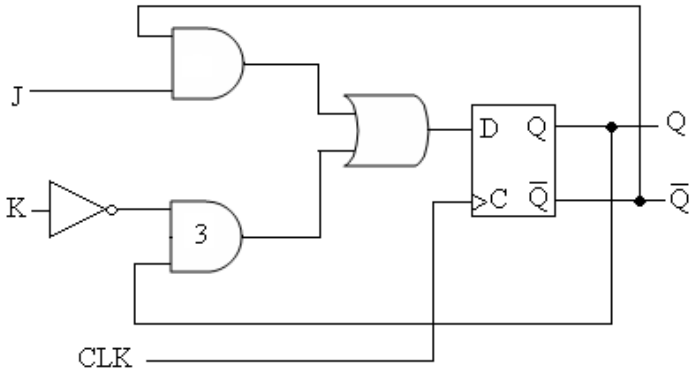


Inputs		Outputs	
D	C	Q^+	$\overline{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\overline{Q}$
X	1	Q	$\overline{Q}$

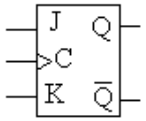


JK FLIP FLOP





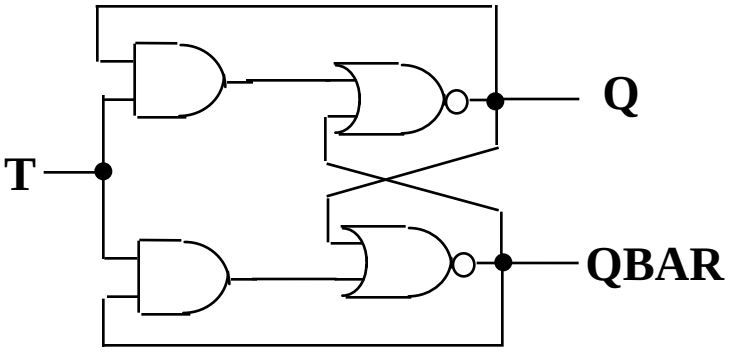
Positive Edge Triggered JK FF

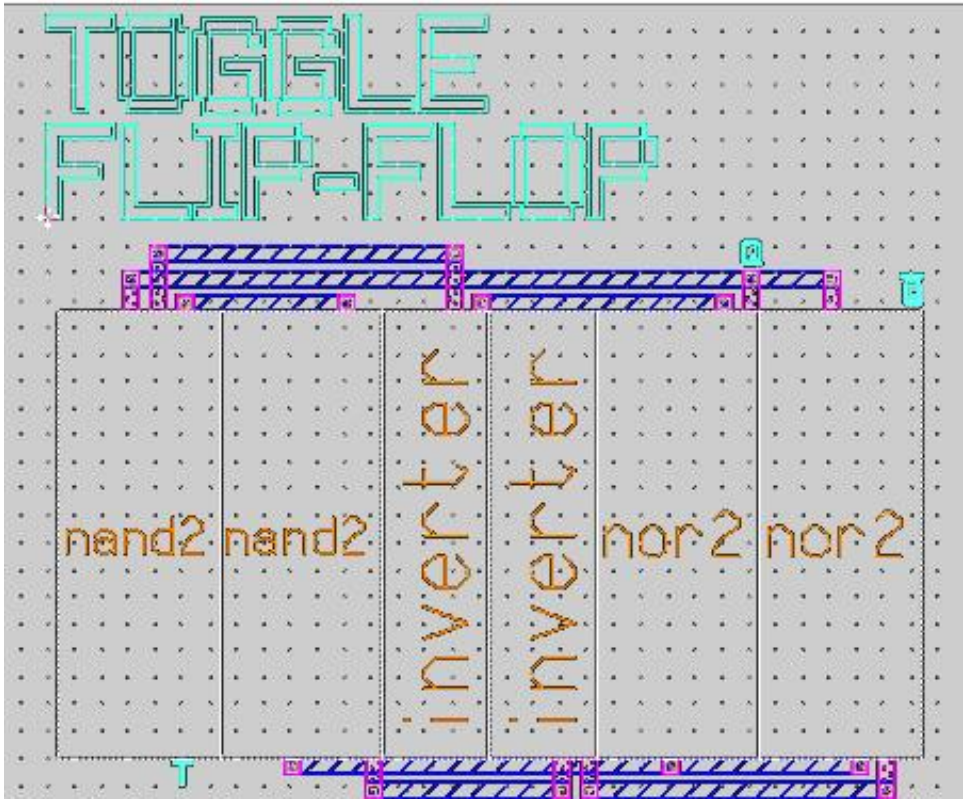


Inputs			Outputs	
J	K	C	Q^+	$\overline{Q^+}$
0	0	↑	Q	$\overline{Q}$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\overline{Q}$	Q
X	X	0	Q	$\overline{Q}$
X	X	1	Q	Q

T-TYPE FILP-FLOP

TOGGEL FLIP FLOP

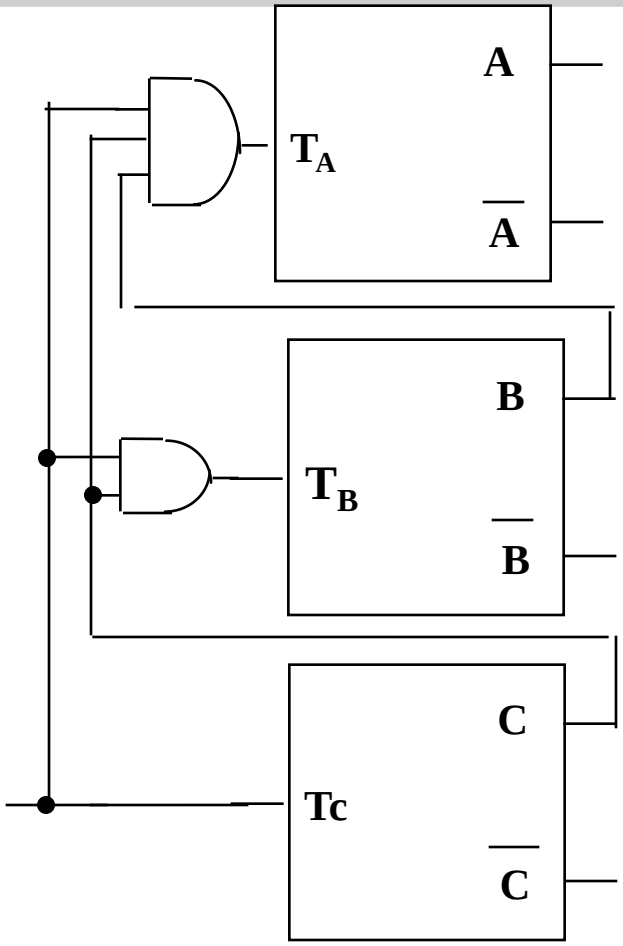




Q: Toggles High and Low with Each Input

T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

BINARY COUNTER USING T TYPE FLIP FLOPS



State Table for Binary Counter

Present State			Next State			F-F Inputs		
A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

TOGGEL FLIP FLOP

BC \ A	0	1
00	0	0
01	0	0
11	1	1
10	0	0

T_A

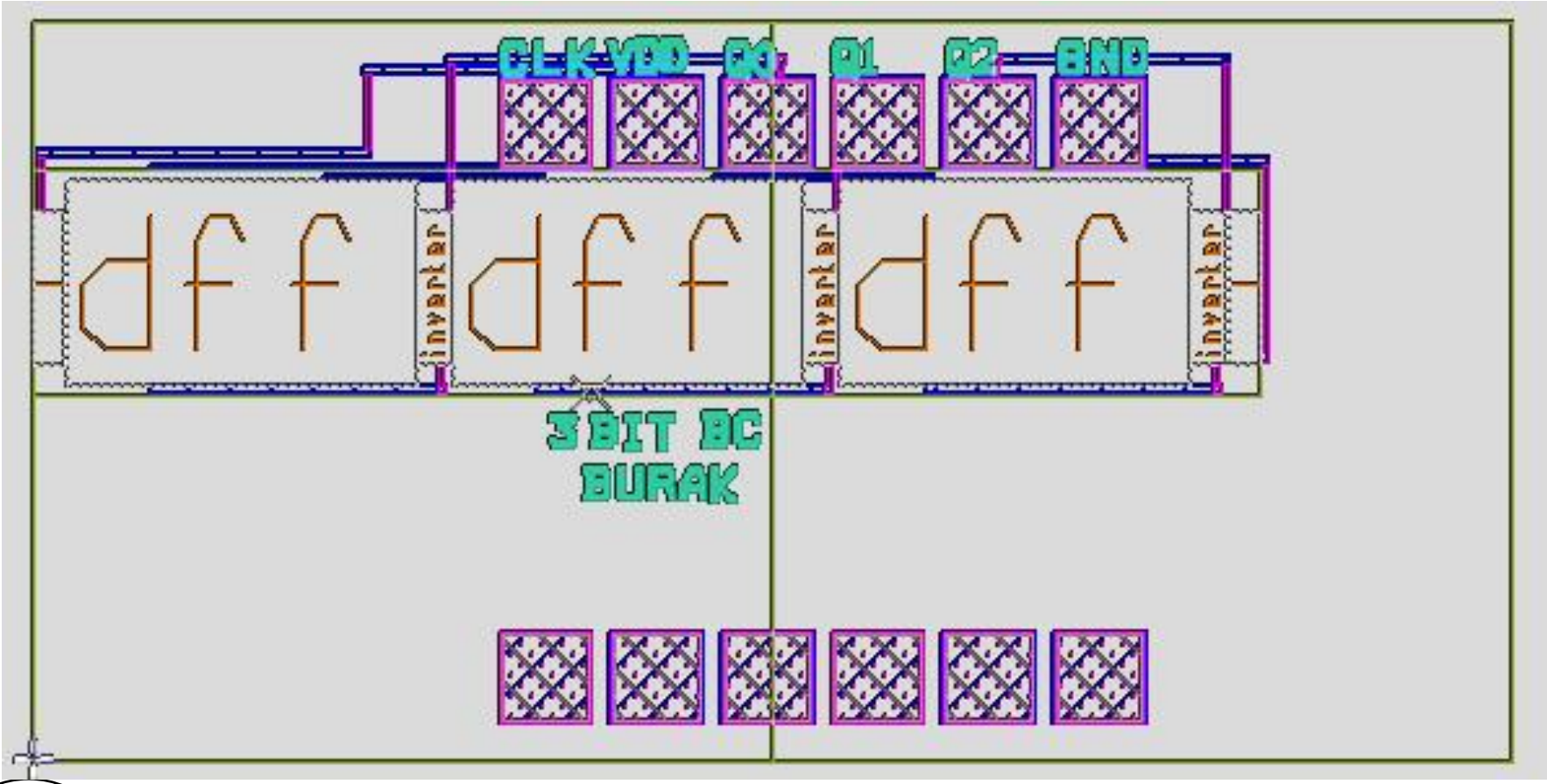
BC \ A	0	1
00	0	0
01	1	1
11	1	1
10	0	0

T_B

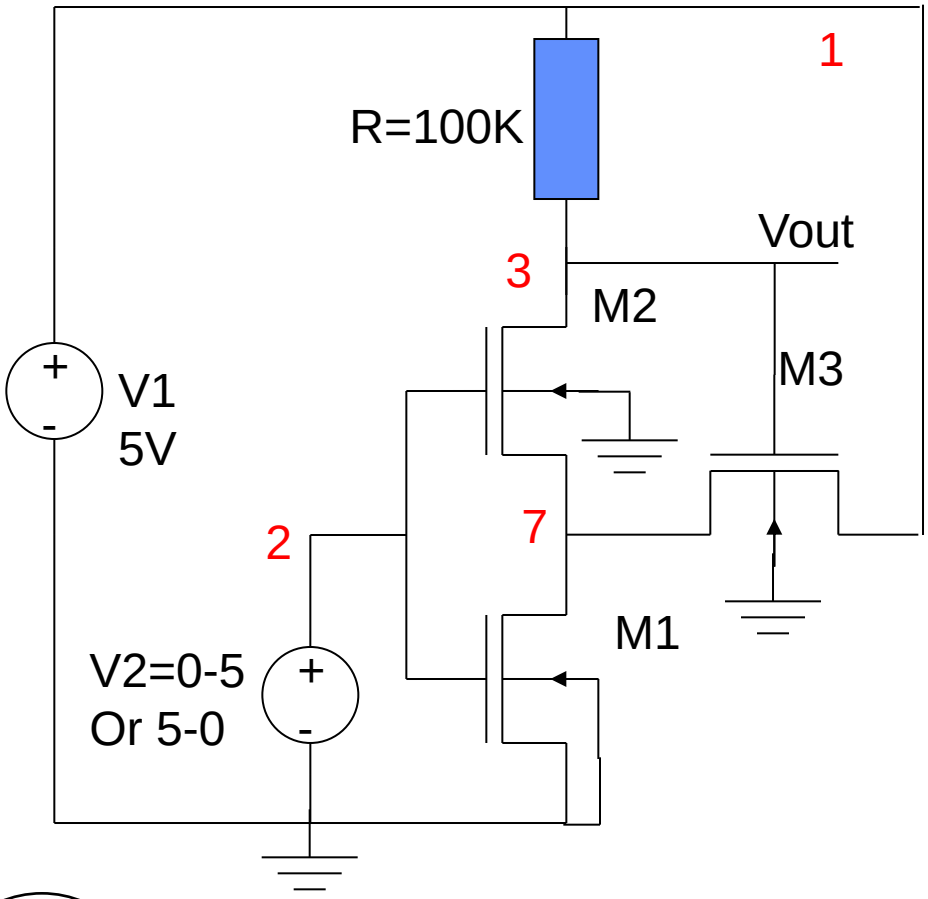
BC \ A	0	1
00	1	1
01	1	1
11	1	1
10	1	1

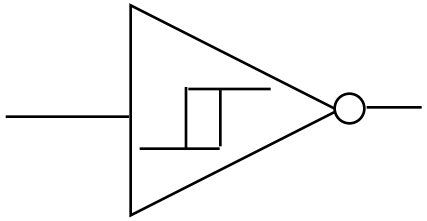
T_C

3-BIT BINARY COUNTER WITH D FLIP FLOPS

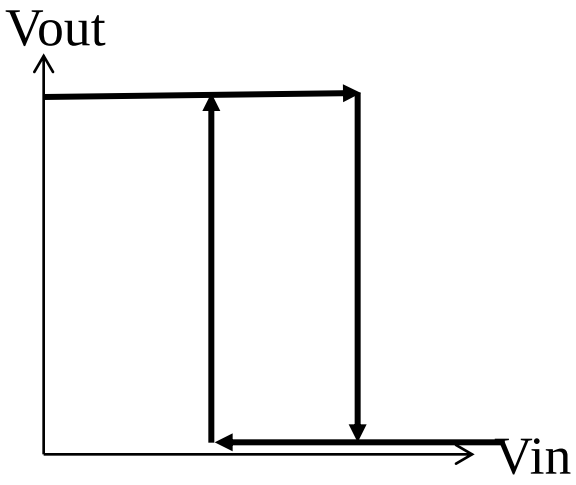


INVERTER WITH HYSTERESIS



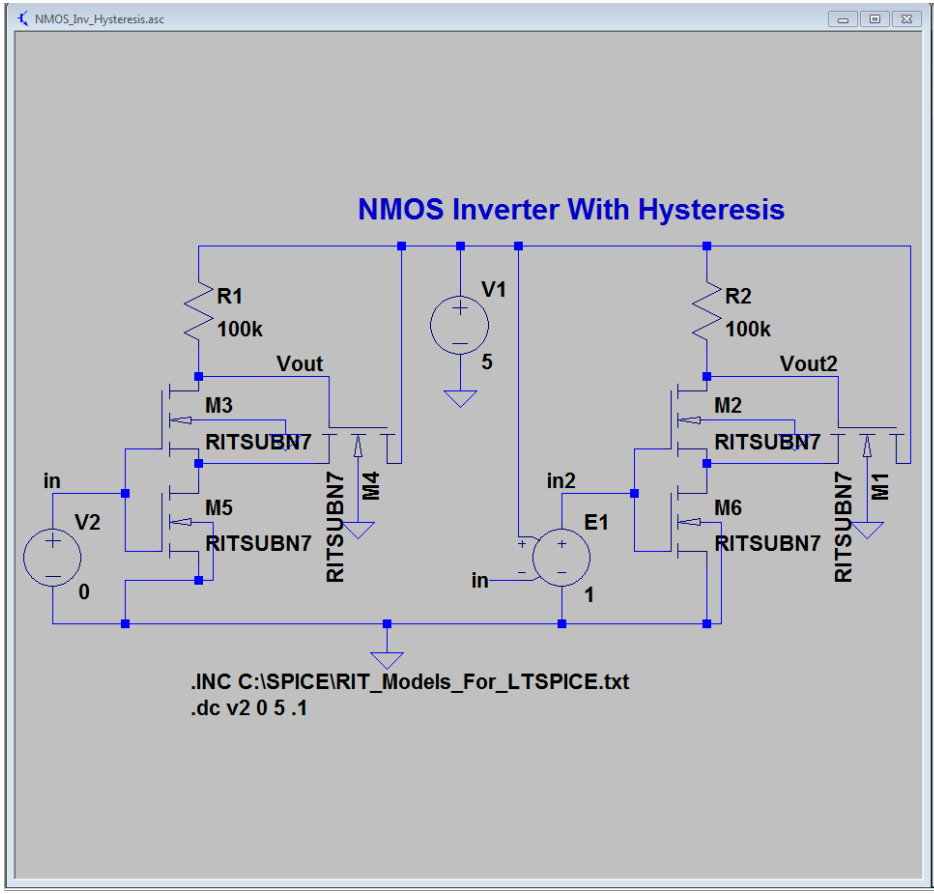


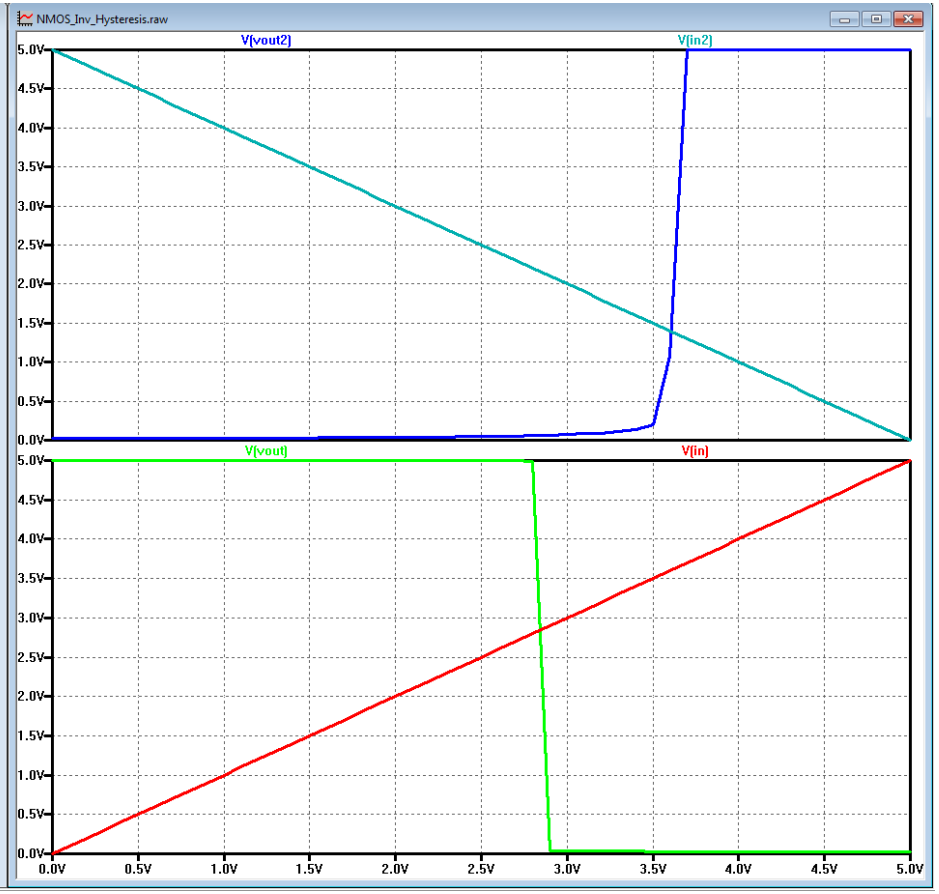
Inverter with Hysteresis



The voltage on node 7 is different depending on if Vout is high or low. Changing the Voltage from source to substrate which changes the threshold voltage of M2

INVERTER WITH HYSTERESIS

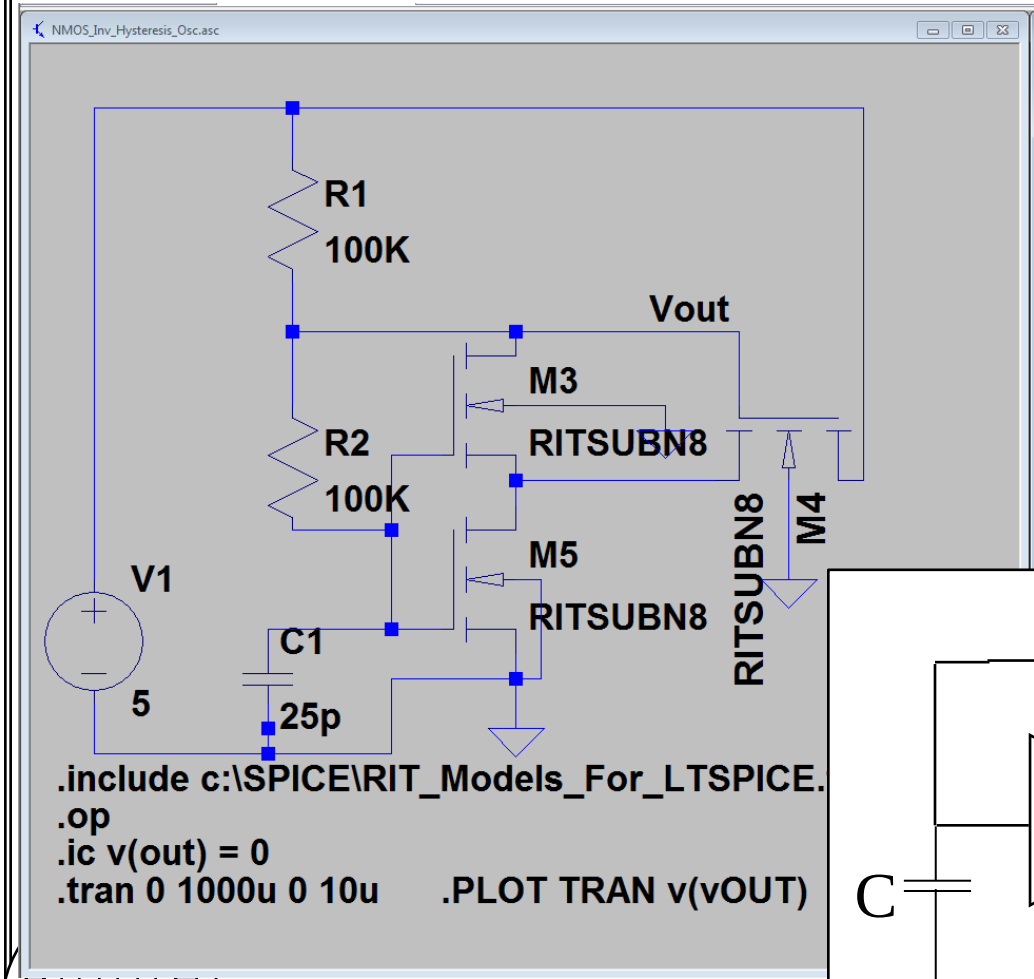


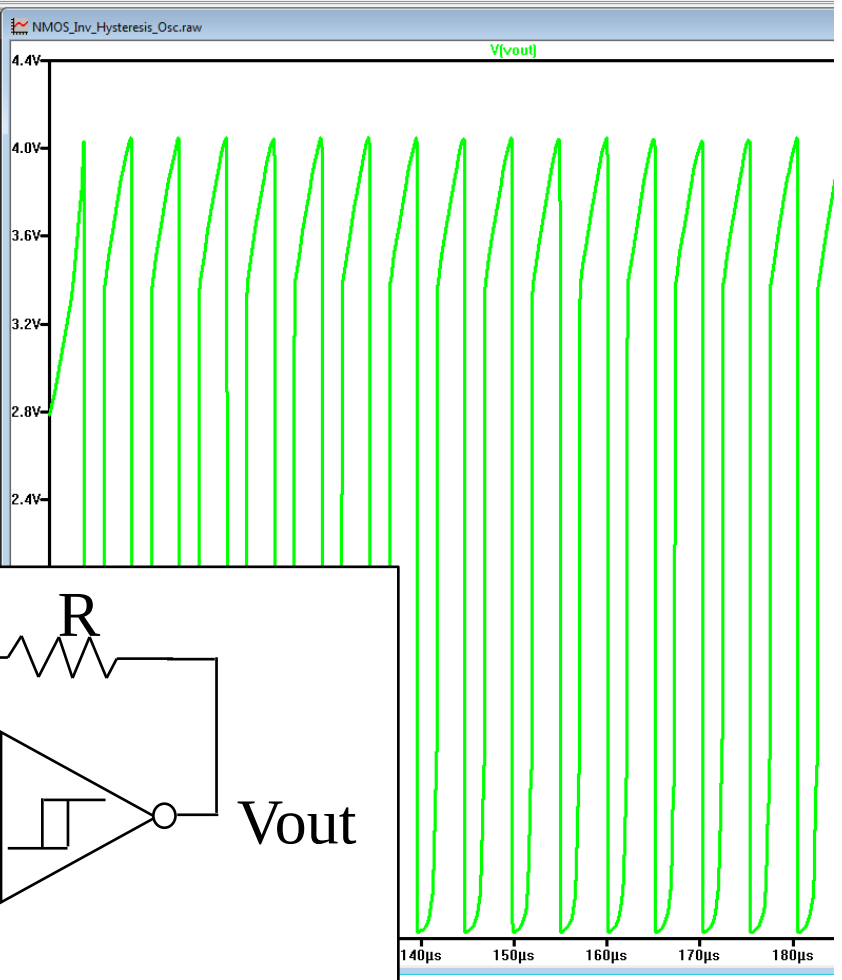


SPICE shows inverter has hysteresis

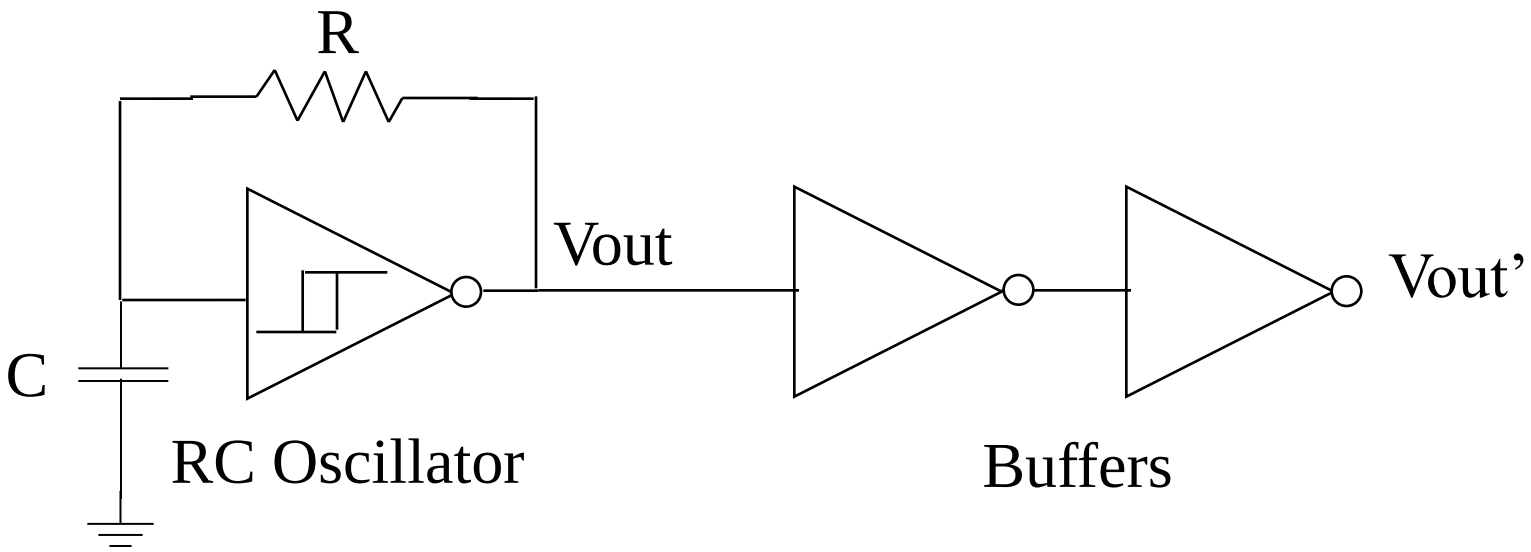
(Flip Blue output about the y-axis and superimpose on Red-Green Plot)

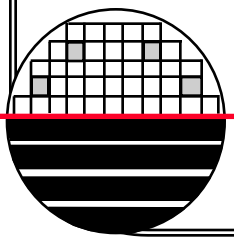
RC OSCILLATOR USING INVERTER WITH HYSTERESIS



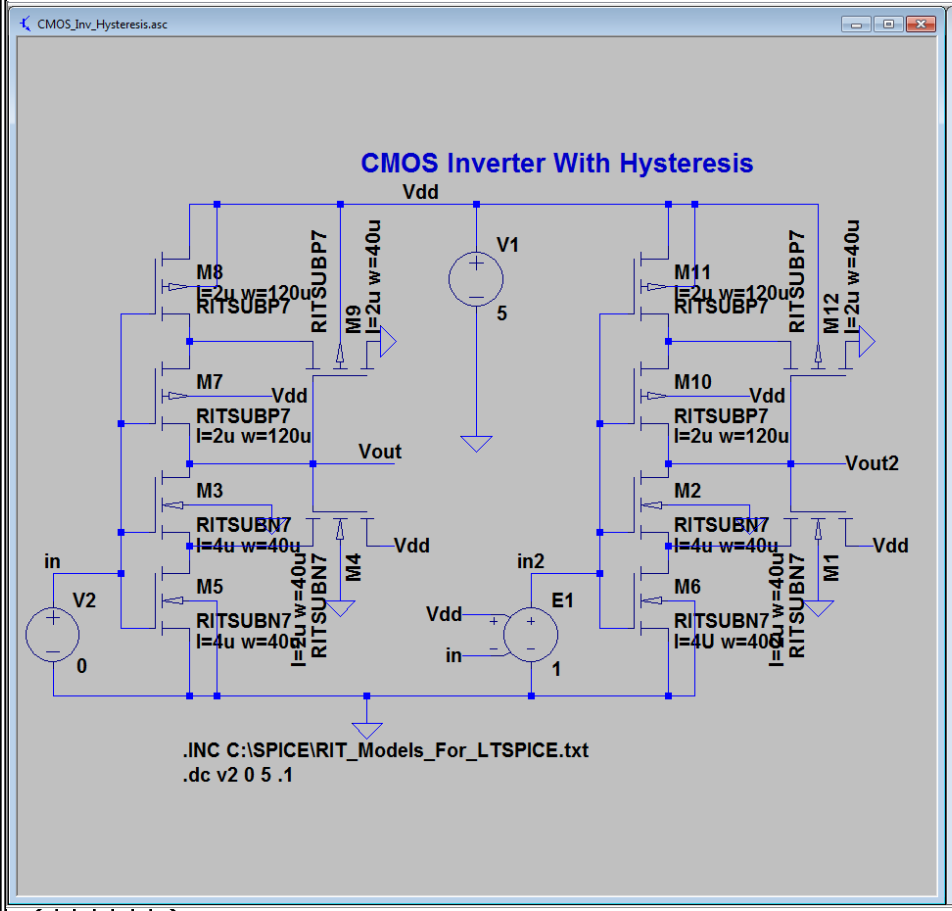


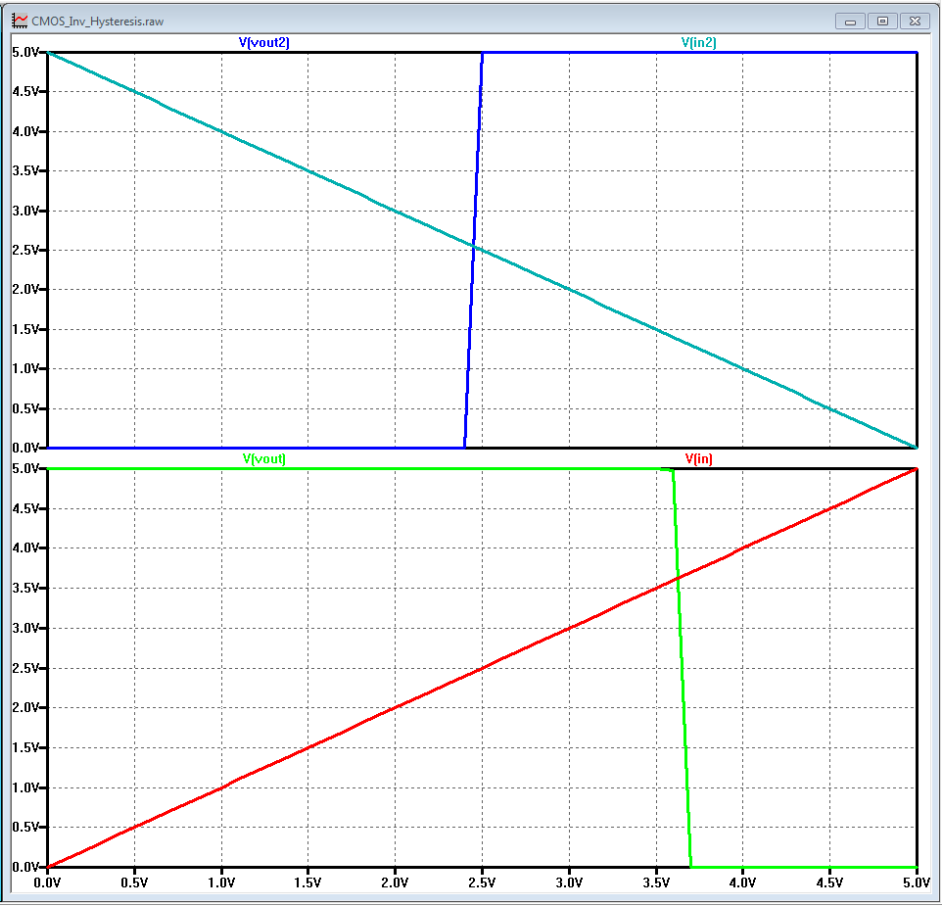
BUFFERS





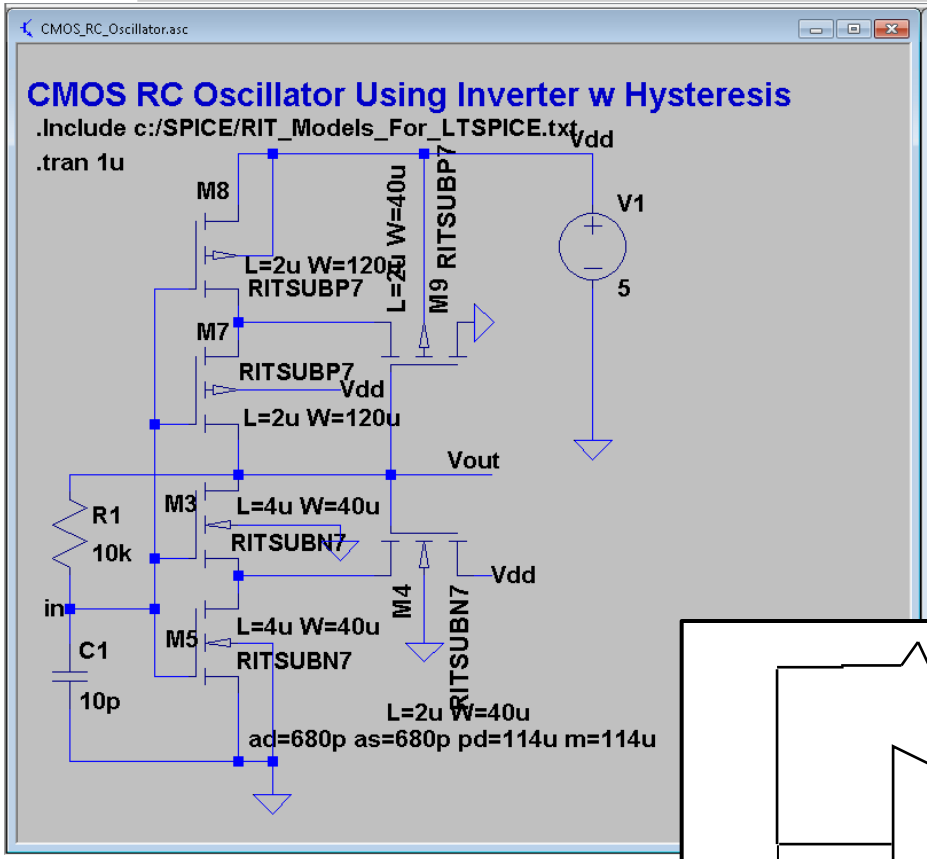
CMOS INVERTER WITH HYSTERESIS

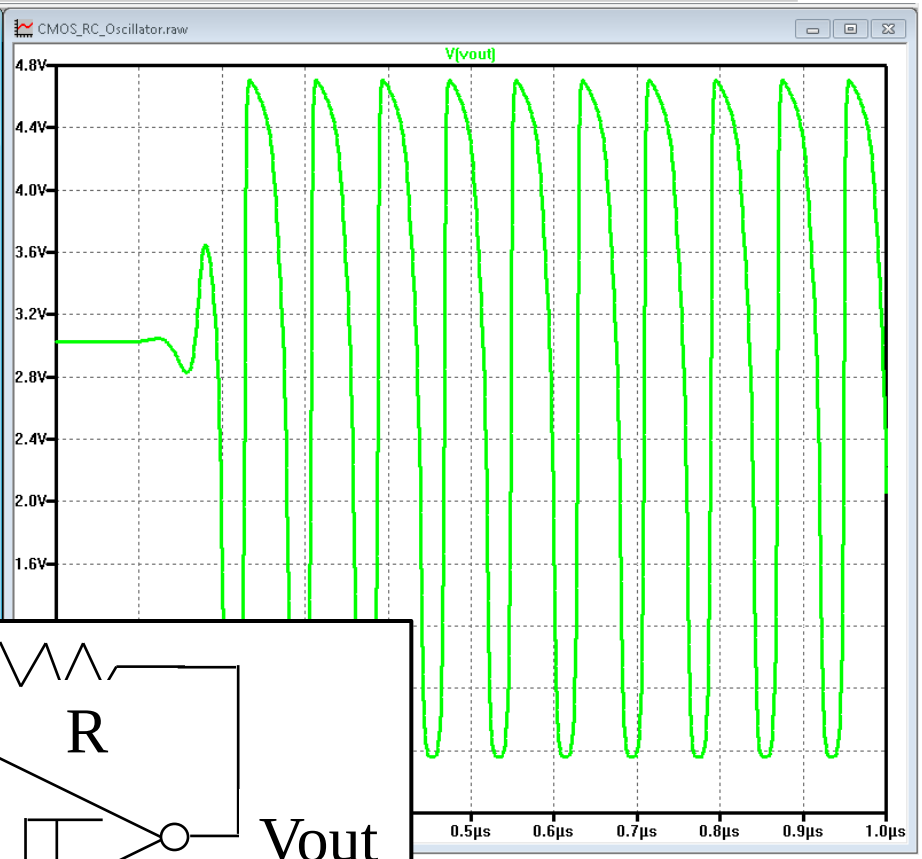


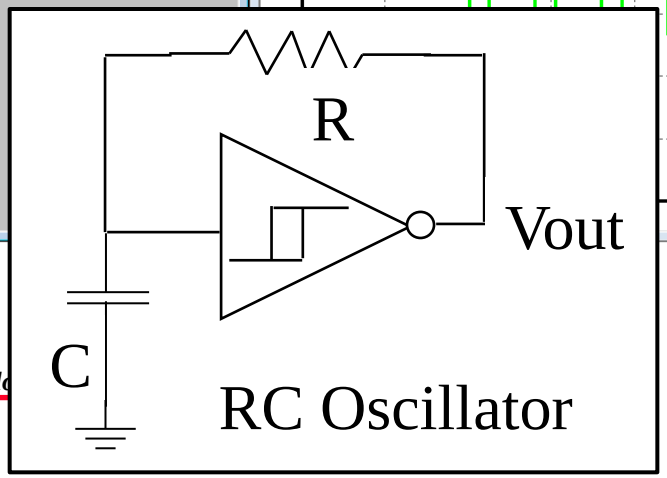


SPICE show this inverter has hysteresis

OSCILLATOR CMOS INVERTER WITH HYSTERESIS

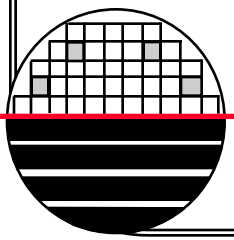






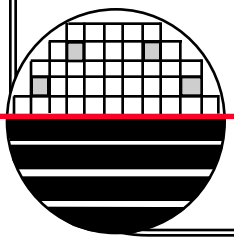
REFERNCES

1. Hodges Jackson and Saleh, Analysis and Design of Digital Integrated Circuits, Chapter 4.
2. Sedra and Smith, Microelectronic Circuits, Sixth Edition, Chapter 13.
3. Dr. Fuller's Lecture Notes, http://people.rit.edu/lffeee



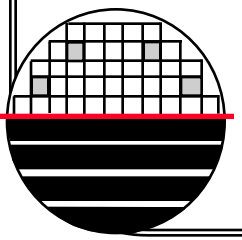
HOMEWORK – LOGIC

1. Design a pseudo NMOS NAND gate. Use 1um technology. Show it will work using SPICE.
2. Look up the data sheet for the MM74C14 CMOS inverter with hystersis. Design a 10 Khz oscillator.
3. Use SPICE (transistor level) to simulate the 1 to 4 Demultiplexer.
4. Use SPICE (transistor level) to simulate the positive edge triggered D-type Flip-Flop.
5. Use SPICE to simulate a CMOS RC Oscillator with Buffers.



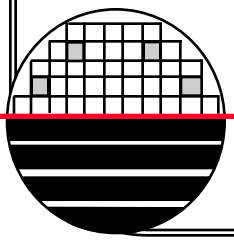
SPICE MODELS FOR MOSFETS

```
*SPICE MODELS FOR RIT DEVICES - DR. LYNN FULLER 4-10-2014
*LOCATION DR.FULLER'S WEBPAGE - http://people.rit.edu/lffeee/CMOS.htm
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=1u W=200u
.MODEL RIT4007N7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=1u W=200u
.MODEL RIT4007P7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



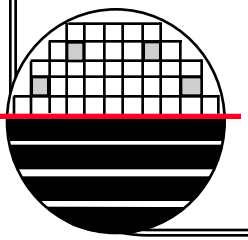
SPICE MODELS FOR MOSFETS

*Used for ALD1103 chips
*Note: Properties L=10u W=880u
.MODEL RITALDN3 NMOS (LEVEL=3
+TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0= 1215 VTO=0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5
+NSUB=1.57E16 XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)
*
*Used for ALD1103 chips
*Note: Properties L=10u W=880u
.MODEL RITALDP3 PMOS (LEVEL=3
+TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0=550 VTO=-0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5
+NSUB=1.57E16 XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)



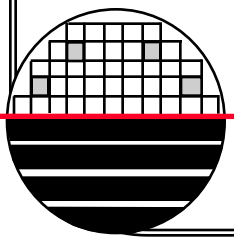
SPICE MODELS FOR MOSFETS

```
*4-4-2013 LTSPICE uses Level=8
*For RIT Sub-CMOS 150 process with L=2u
.MODEL RITSUBN8 NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013  LTSPICE uses Level=8
*For RIT Sub-CMOS 150 process with L=2u
.MODEL RITSUBP8 PMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



SPICE MODELS FOR MOSFETS

```
* From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL RITSUBP7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



SPICE MODELS FOR MOSFETS

```
*4-4-2013  LTSPICE uses Level=8
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSN     NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013  LTSPICE uses Level=8
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSP     PMOS (LEVEL=8
+TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
```