ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Data Conversion Circuits

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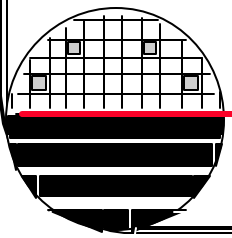
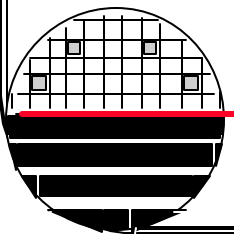


INTRODUCTION

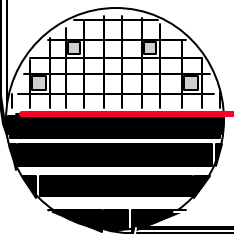
Analog electronic circuits are different from digital circuits in that the signals are expected to have any value rather than two discrete values. Primitive analog components include the diode, mosfet, BJT, resistor, capacitor, etc,. Analog circuit building blocks include single stage amplifiers, differential amplifiers, constant current sources, voltage references, etc. Basic analog electronic ciruits include the operational amplifier, inverting amplifier, non-inverting amplifier, integrator, bistable multivibrator, peak detector, comparator, RC oscillator, etc. Mixed-mode analog integrated circuits include D-to-A, A-to-D, etc.

This document will introduce some mixed-mode analog/digital electronic circuits.

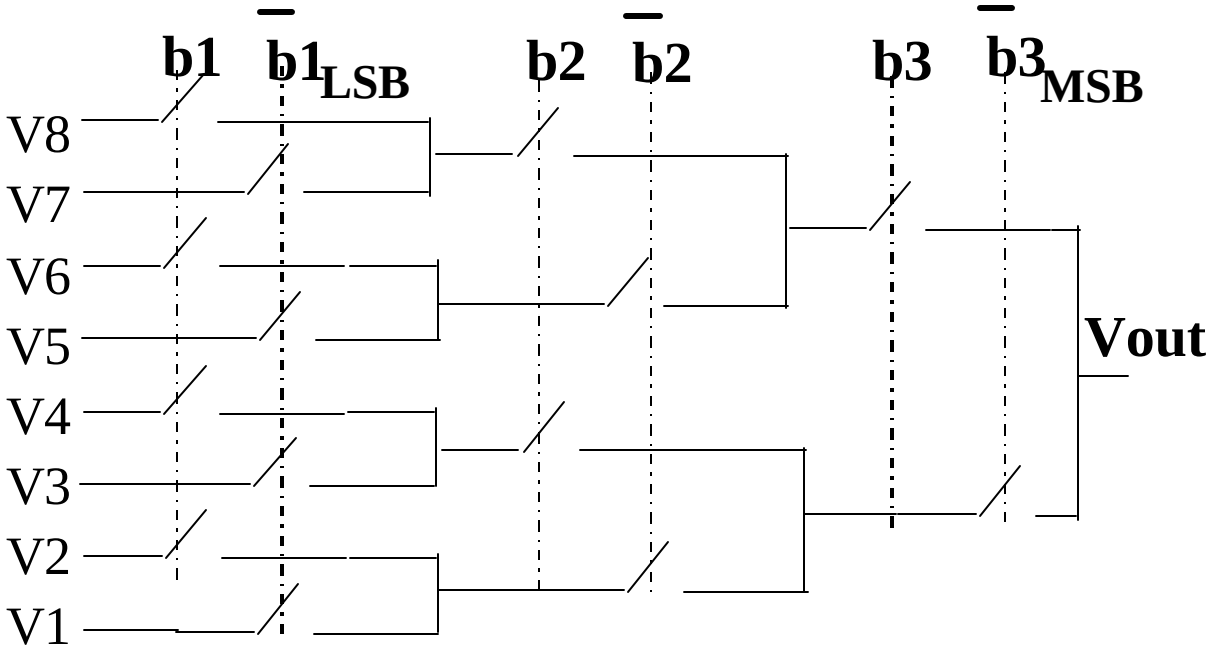


OUTLINE

Analog Multiplexer
D to A
A to D
Binary Counter A to D
Flip Flops
Shift Registers/Counters
Design Examples
Blue Tooth
References
Homework

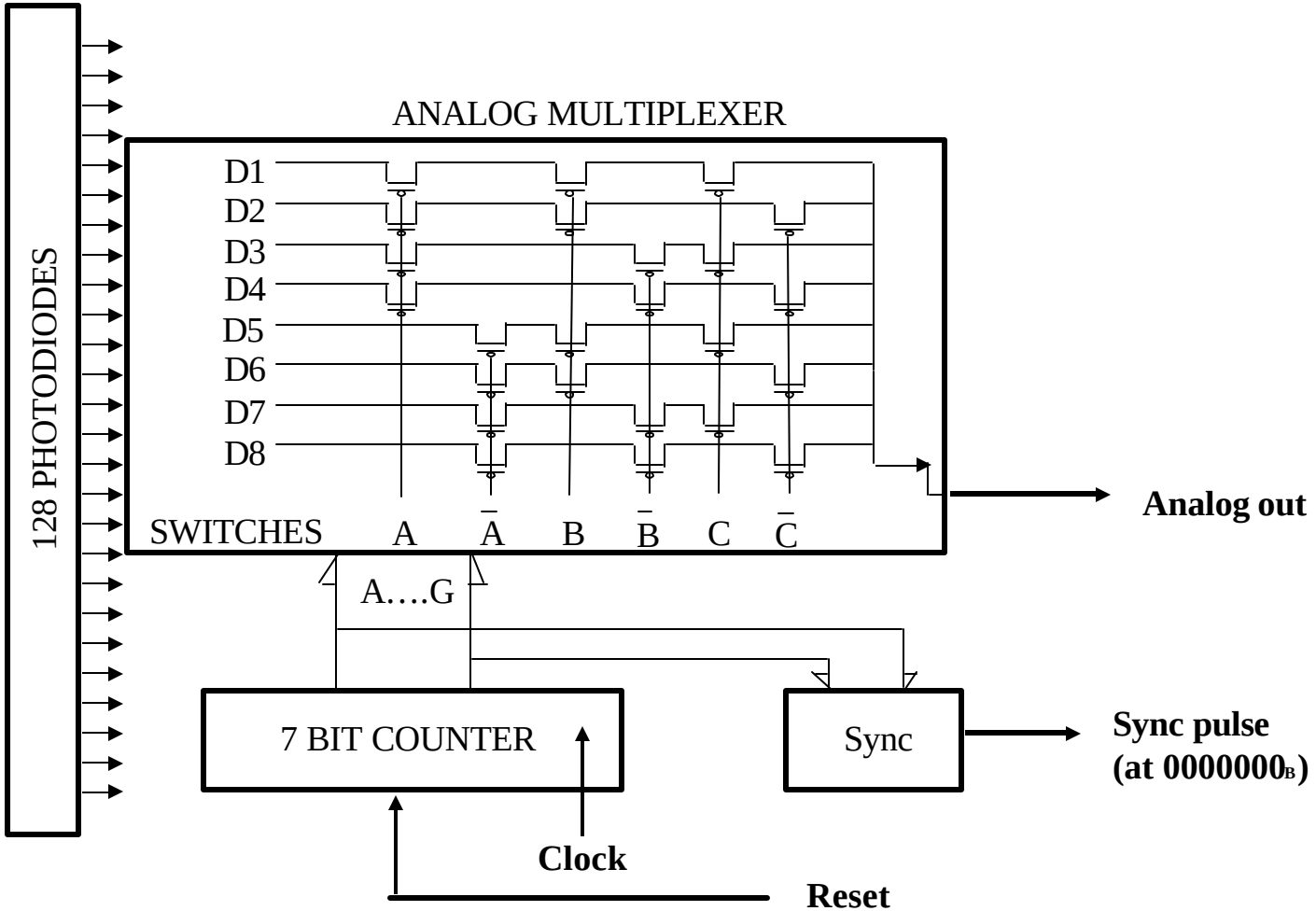


3 BIT ANALOG MULTIPLEXER

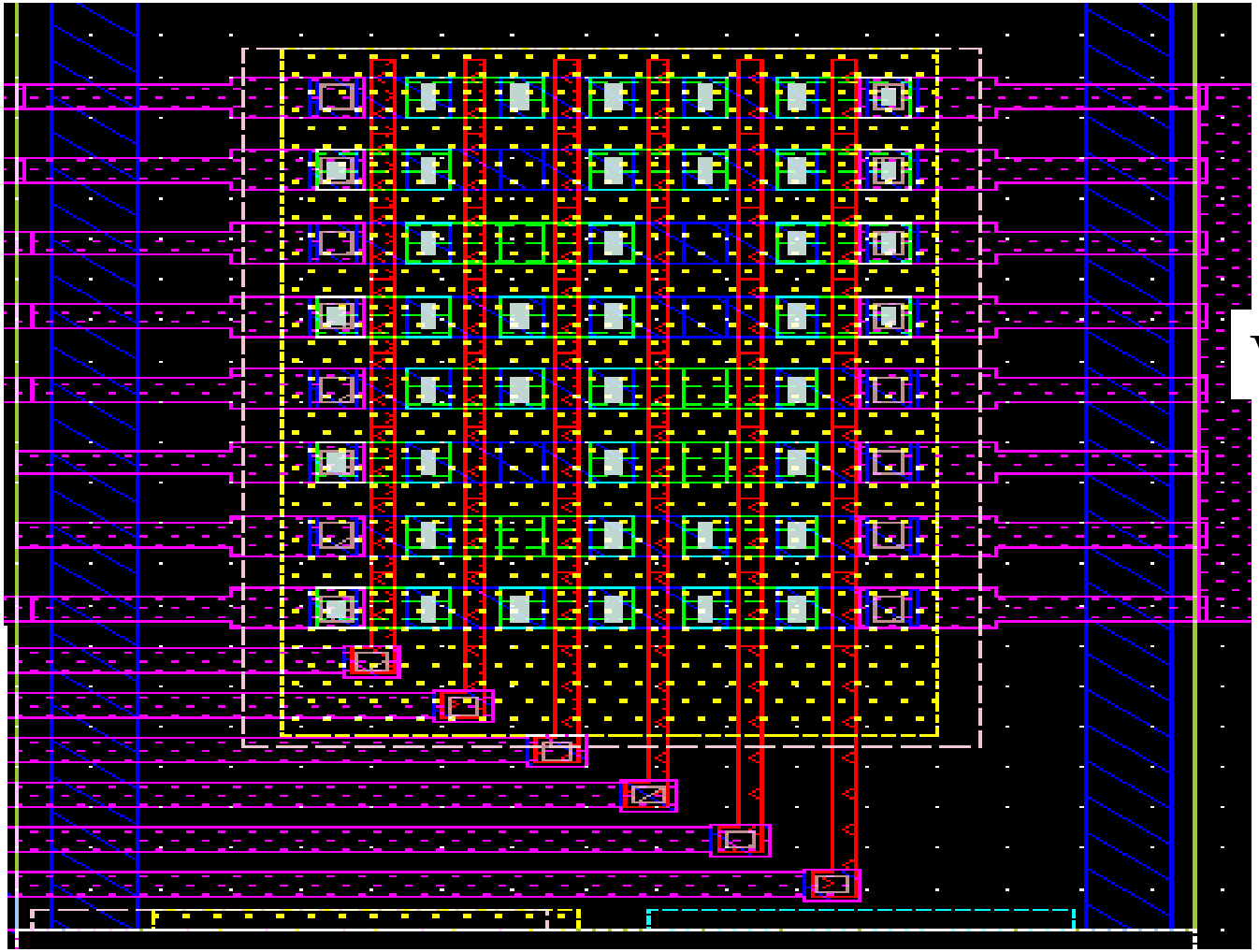


MSB b3	b2	LSB b1	Vout
0	0	0	V1
0	0	1	V2
0	1	0	V3
0	1	1	V4
1	0	0	V5
1	0	1	V6
1	1	0	V7
1	1	1	V8

ANALOG MULTIPLEXER APPLICATION

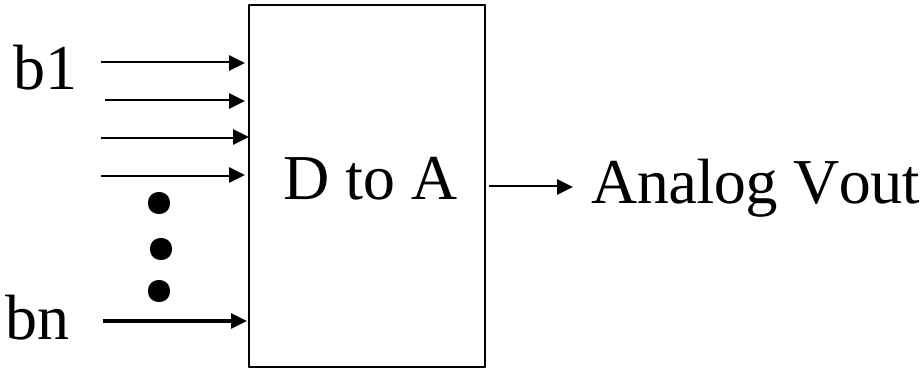


CMOS ANALOG MULTIPLEXER LAYOUT



DIGITAL TO ANALOG CONVERSION

A digital word of n bits is converted to an analog voltage. If n = 3 then 2^n or 8 different analog values are possible. If n=10 then 1024 different analog values are possible.

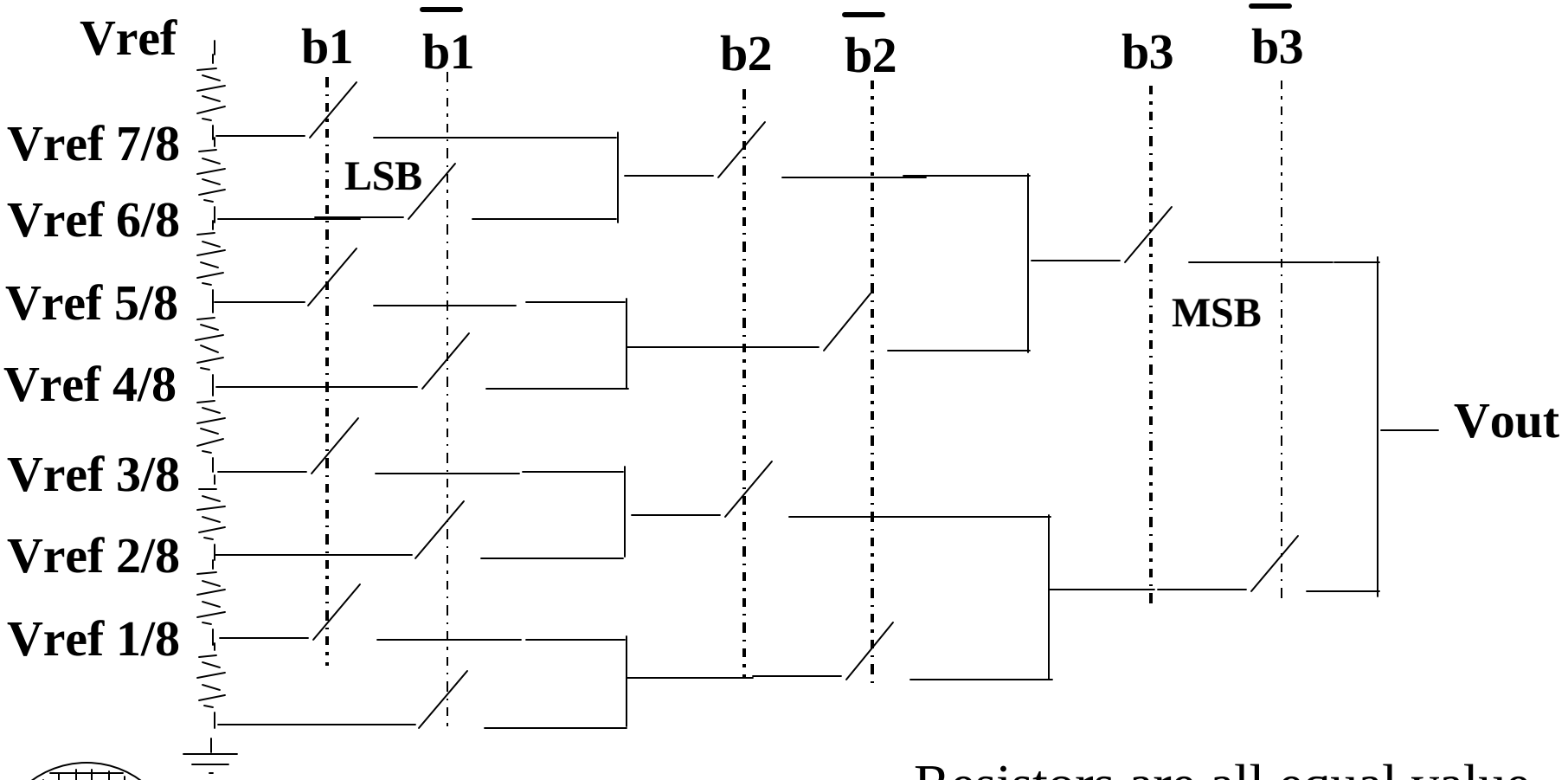


For example if the reference voltage is 3 volts and n = 3 and the digital word is 101 then the Analog Vout = 3V x 5/8 = 1.875V

$2^n=8$

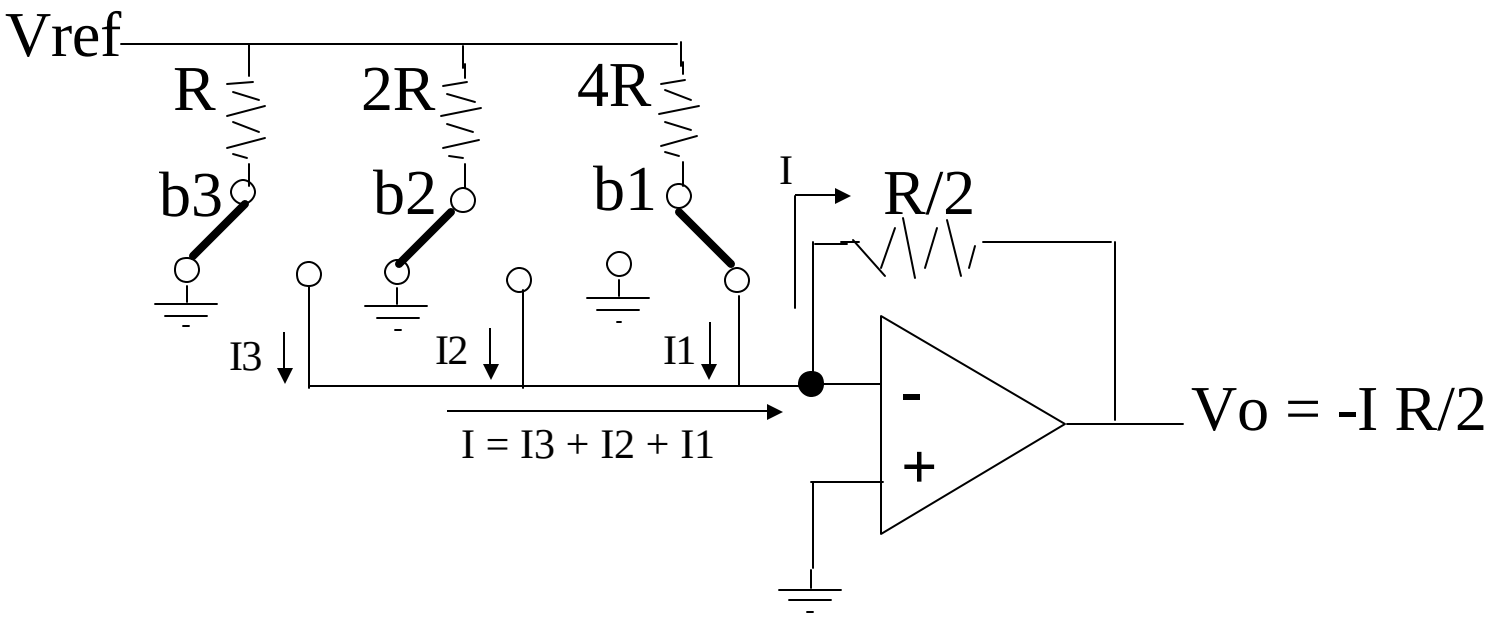
101=5

3 BIT D TO A



Resistors are all equal value

BINARY-WEIGHTED RESISTOR D TO A

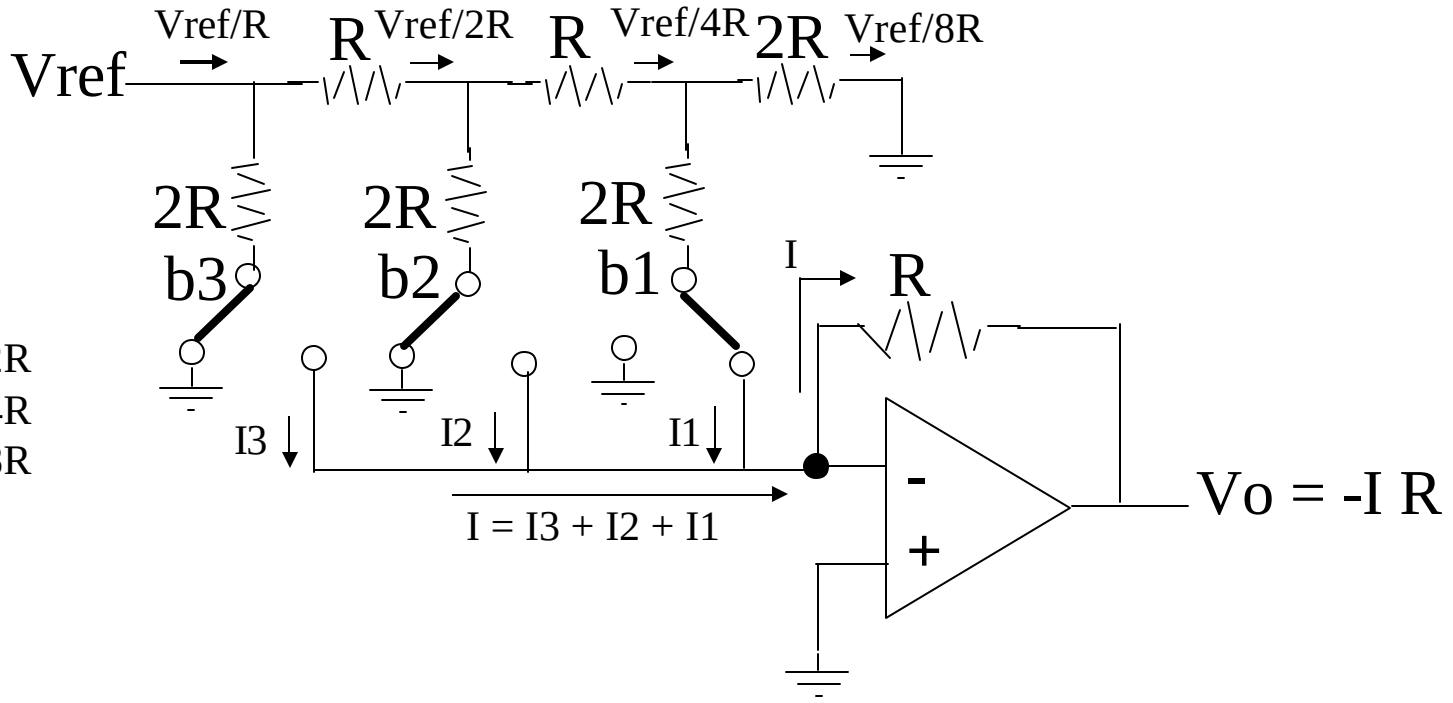


With the switches as shown $Vo = \frac{-Vref\ R/2}{4R} = -Vref/8$

What is Vo for a 101 digital input?

How is this architecture extended to more bits?

R-2R RESISTOR LADDER D TO A

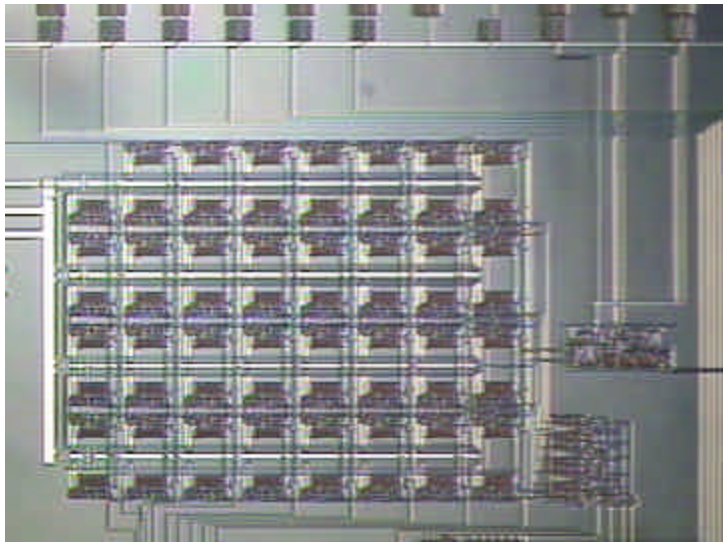


With the switches as shown $Vo = \frac{-Vref\ R}{8R} = -Vref/8$

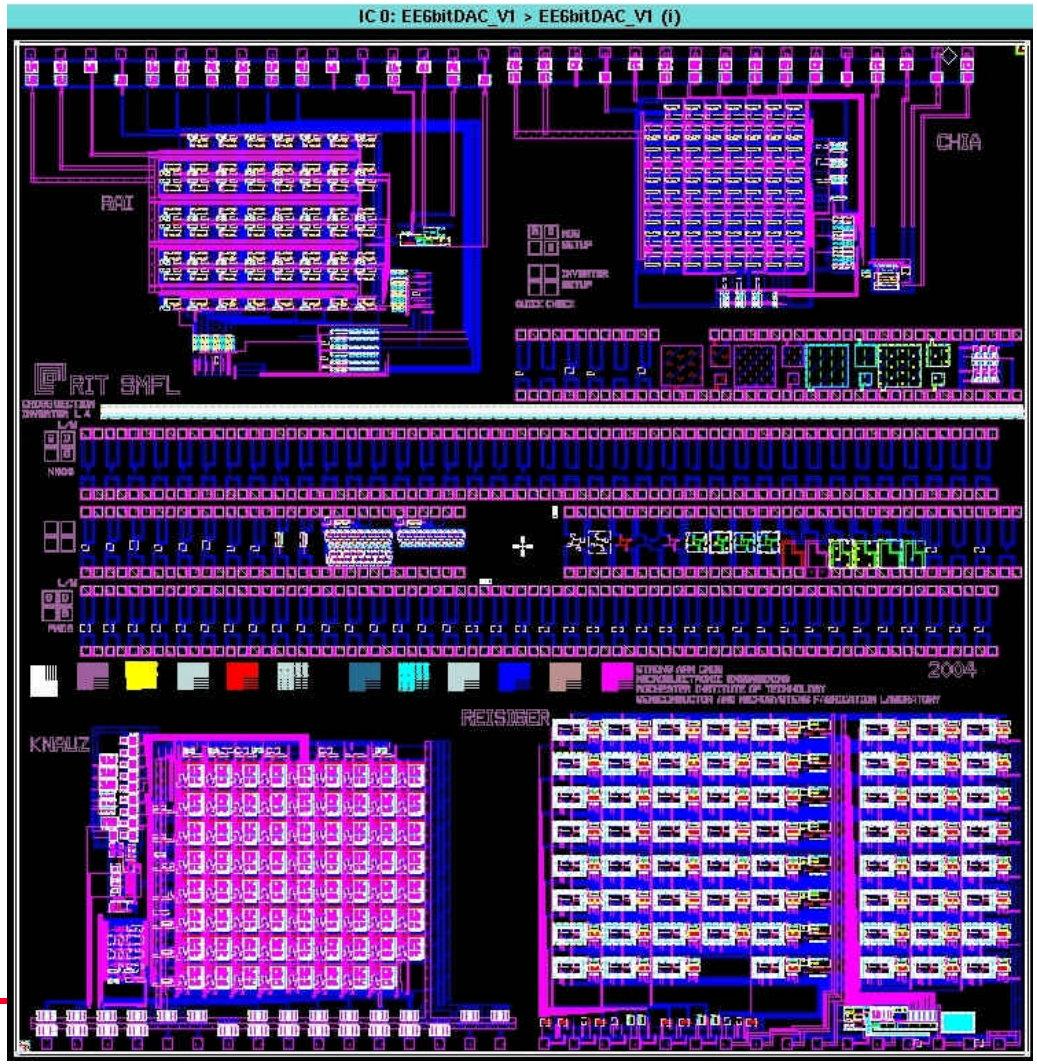
What is Vo for a 101 digital input?

How is this architecture extended to more bits?

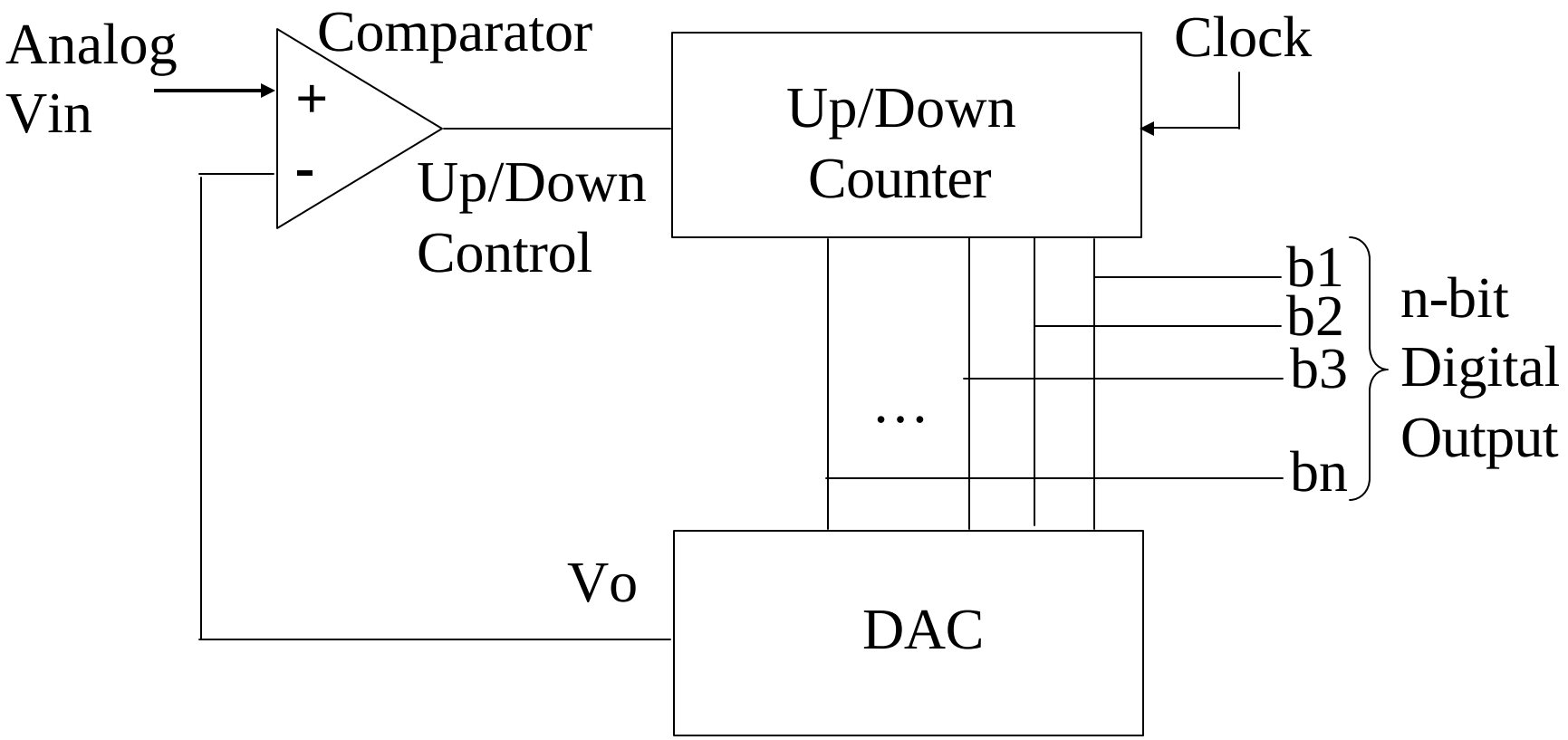
DAC LAYOUT



DAC1 Rai	DAC2 Chia
Test Devices Saxer	
DAC4 Knauz	DAC3 Reisiger



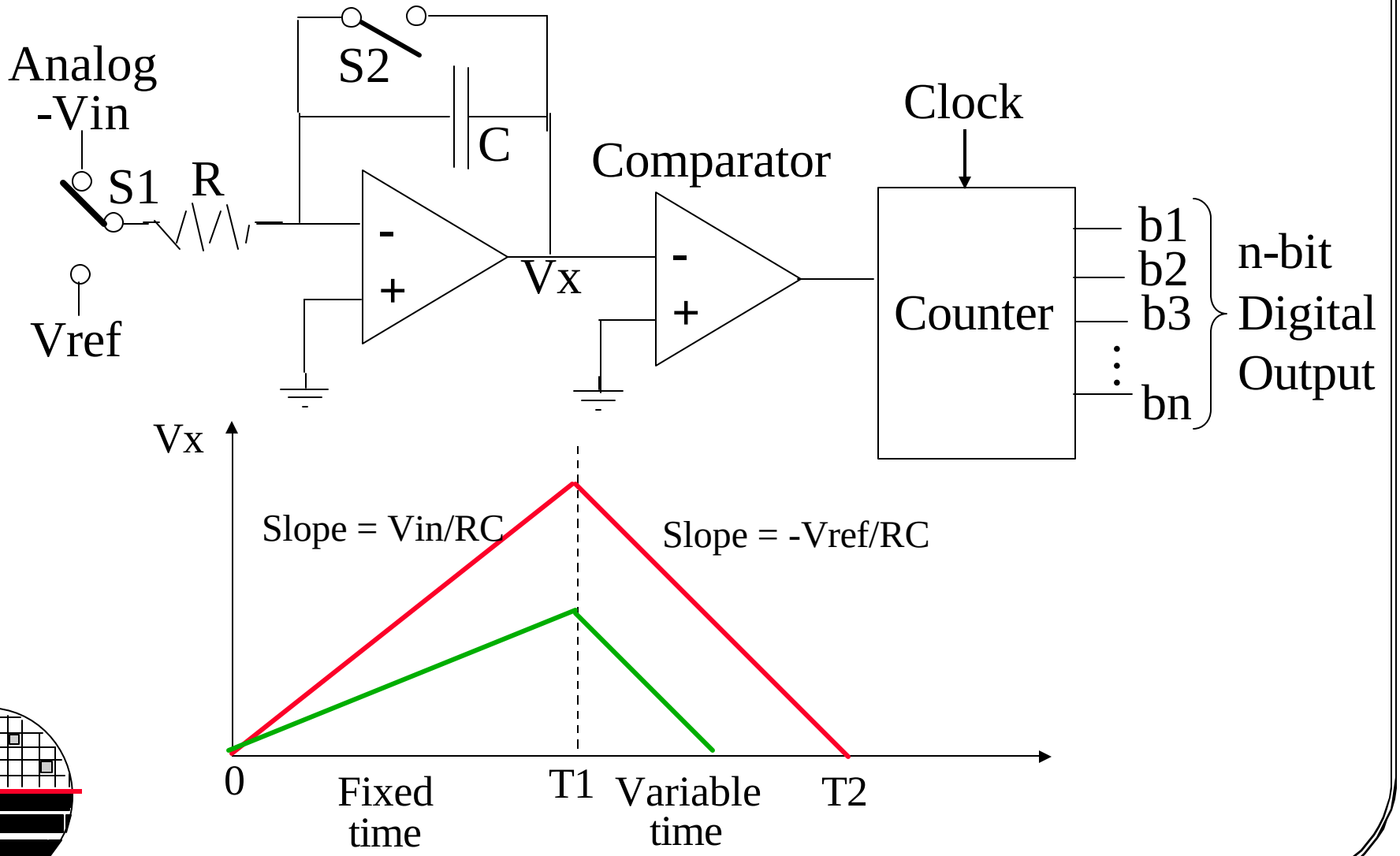
FEEDBACK-COMPARATOR A TO D CONVERTER



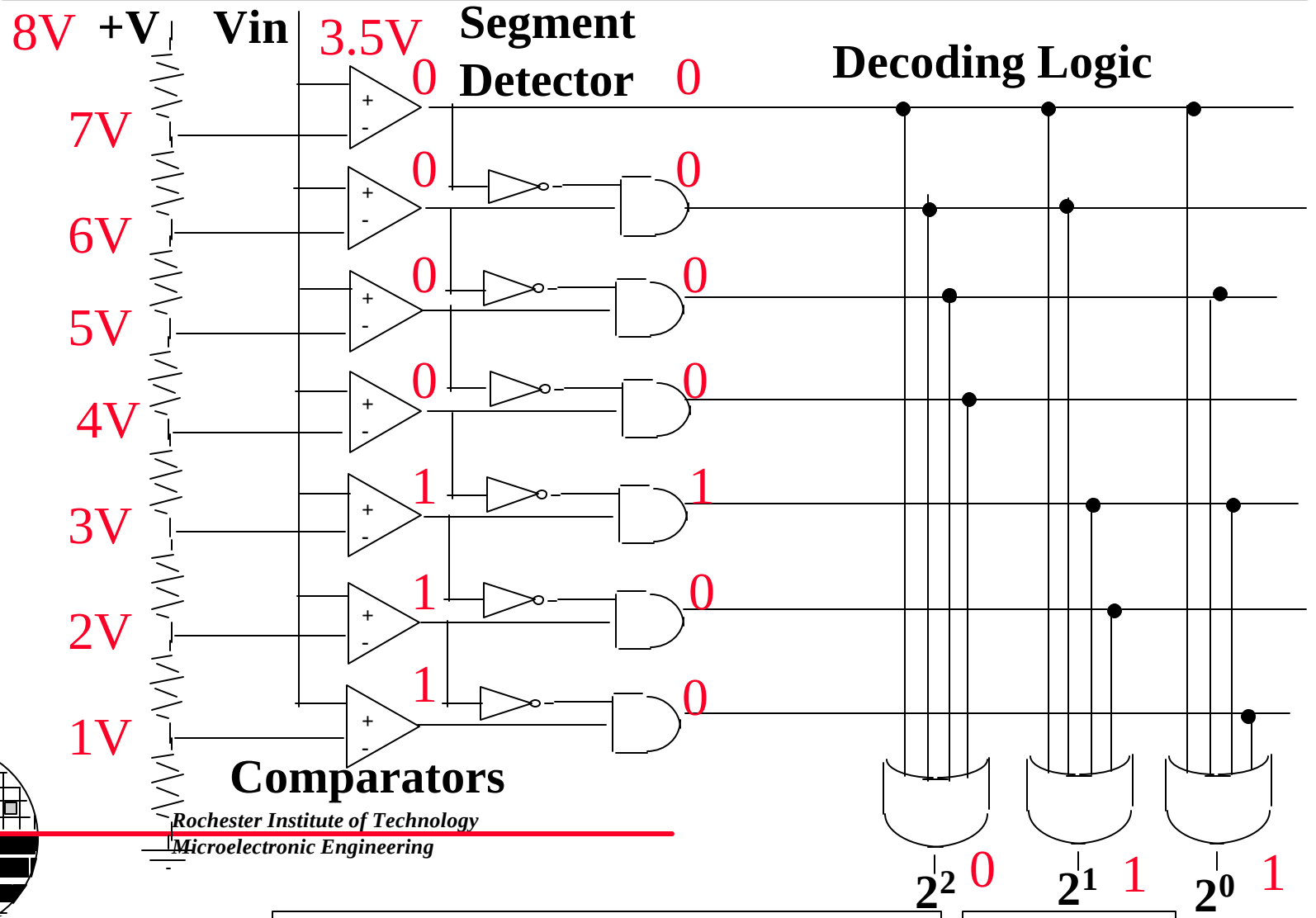
Analog Vin must be less than DAC Vref.

Could take a lot of clock cycles (time) for each conversion.

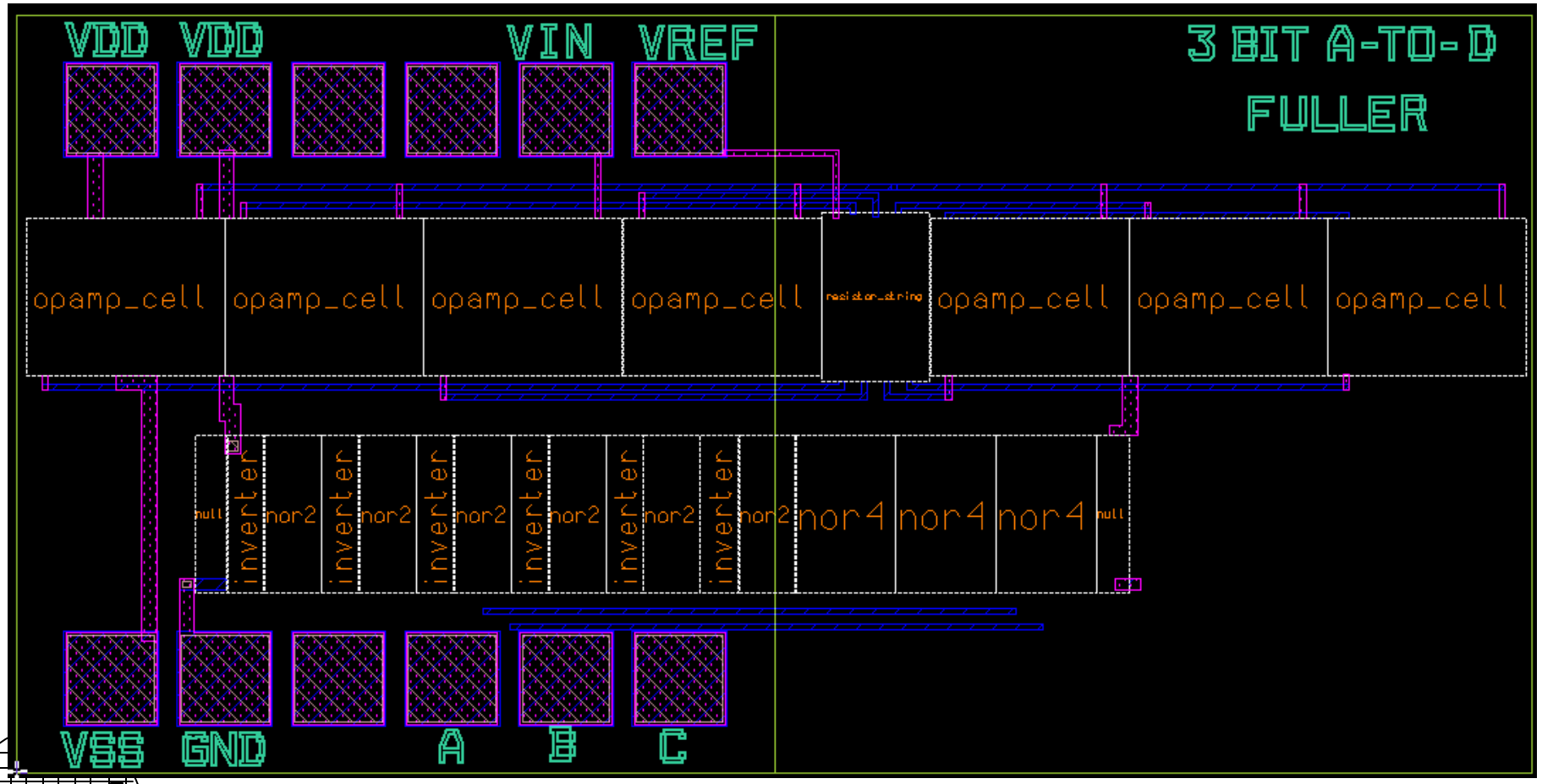
DUAL SLOPE A TO D CONVERTER



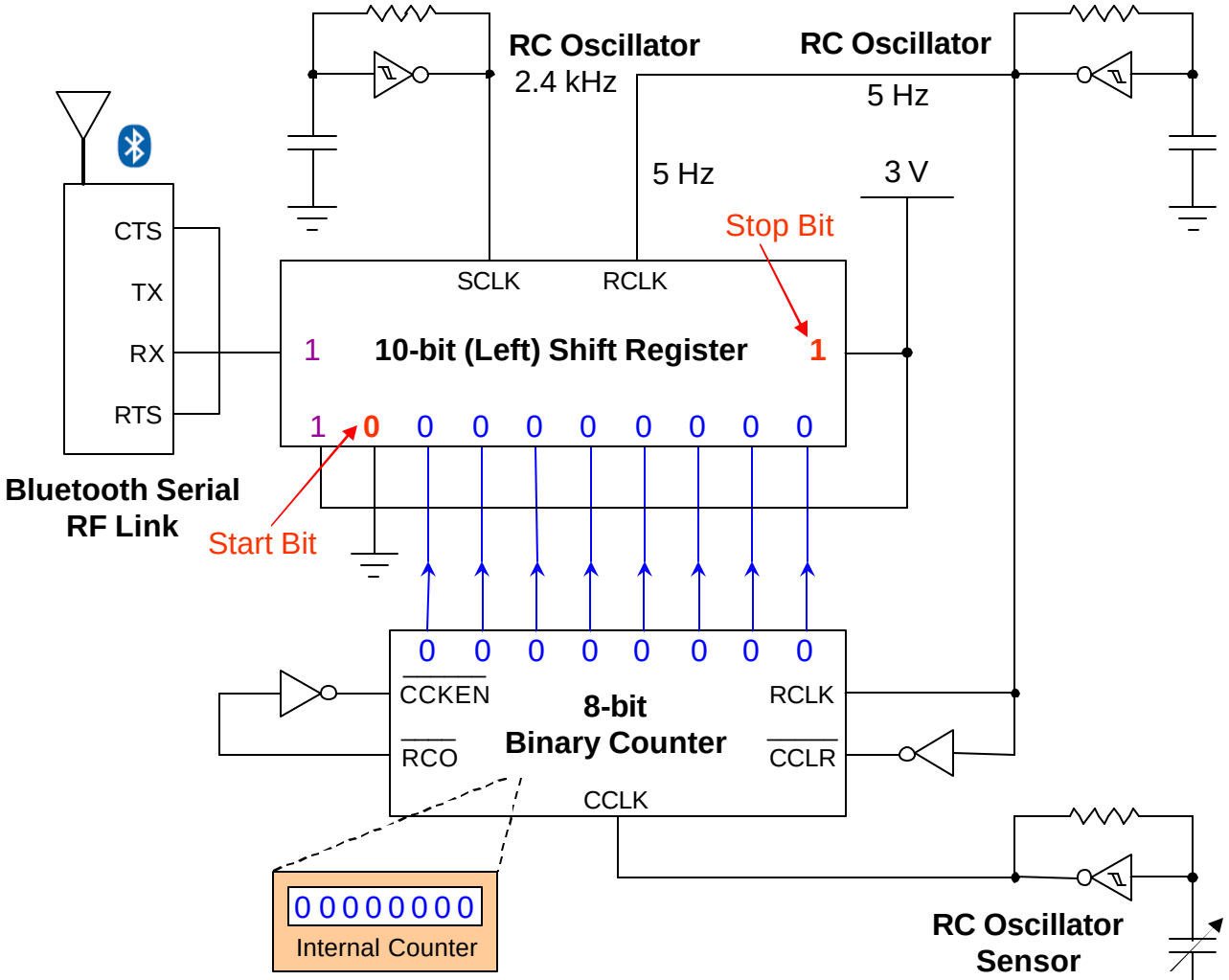
3 BIT FLASH ANALOG TO DIGITAL CONVERTER



LAYOUT OF FLASH A TO D

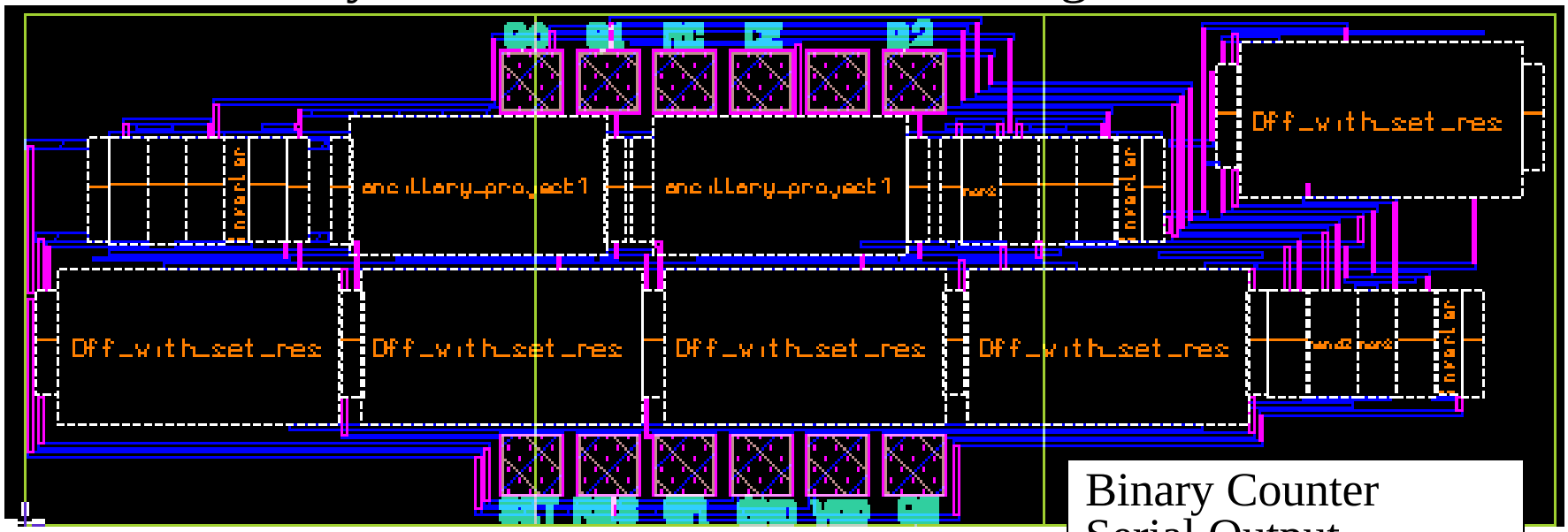


WIRELESS CAPACITANCE TO DIGITAL CONVERTER



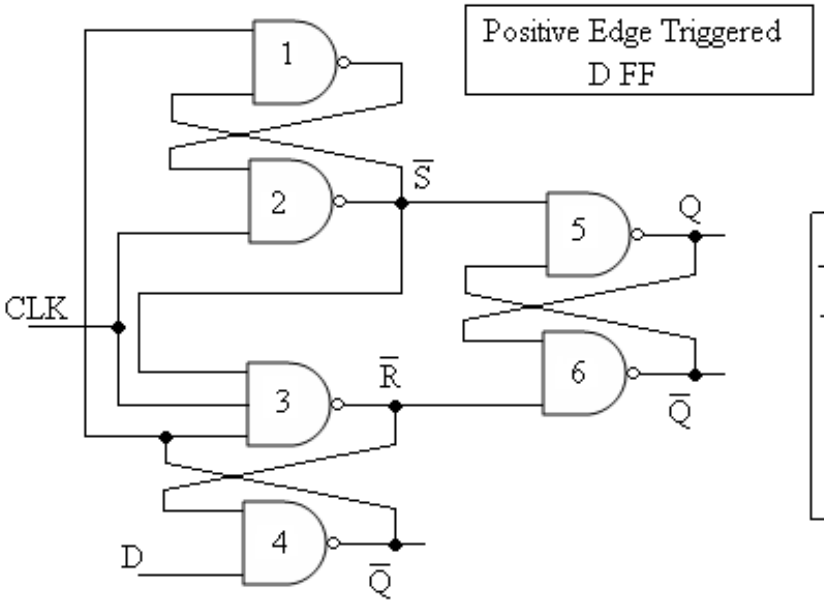
UP/DOWN COUNTER AND SHIFT REGISTERS

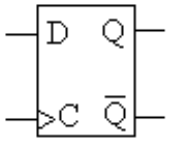
Many of these circuits need Up/Down counters and shift registers. In the next few pages we will look at one type of counter and see how to modify it to also function as a shift register.



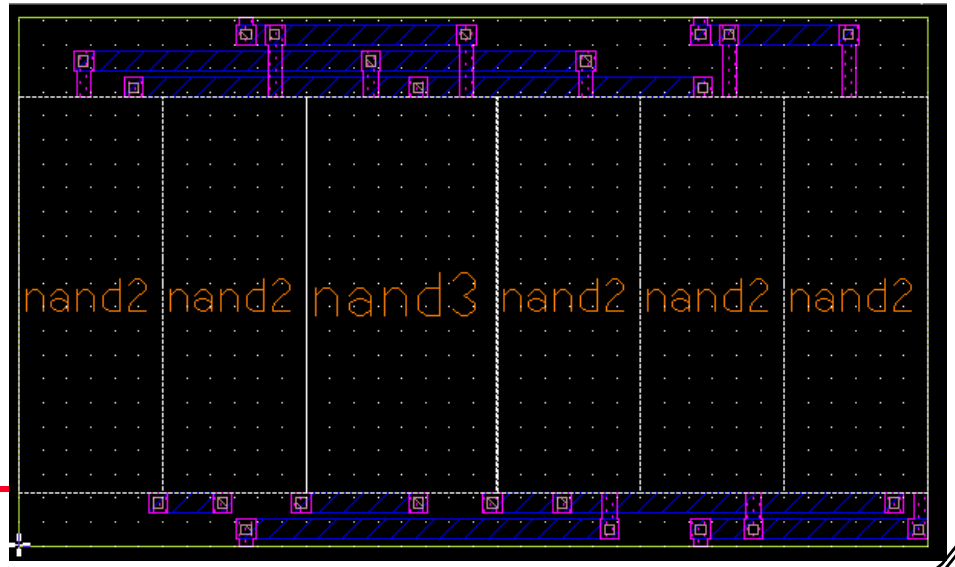
Binary Counter
Serial Output
Asynchronous Reset
Count Up Enable
Shift Out Clock Input
Count Up Clock Input
Start Bit and Stop Bit

EDGE TRIGGERED D TYPE FLIP FLOP

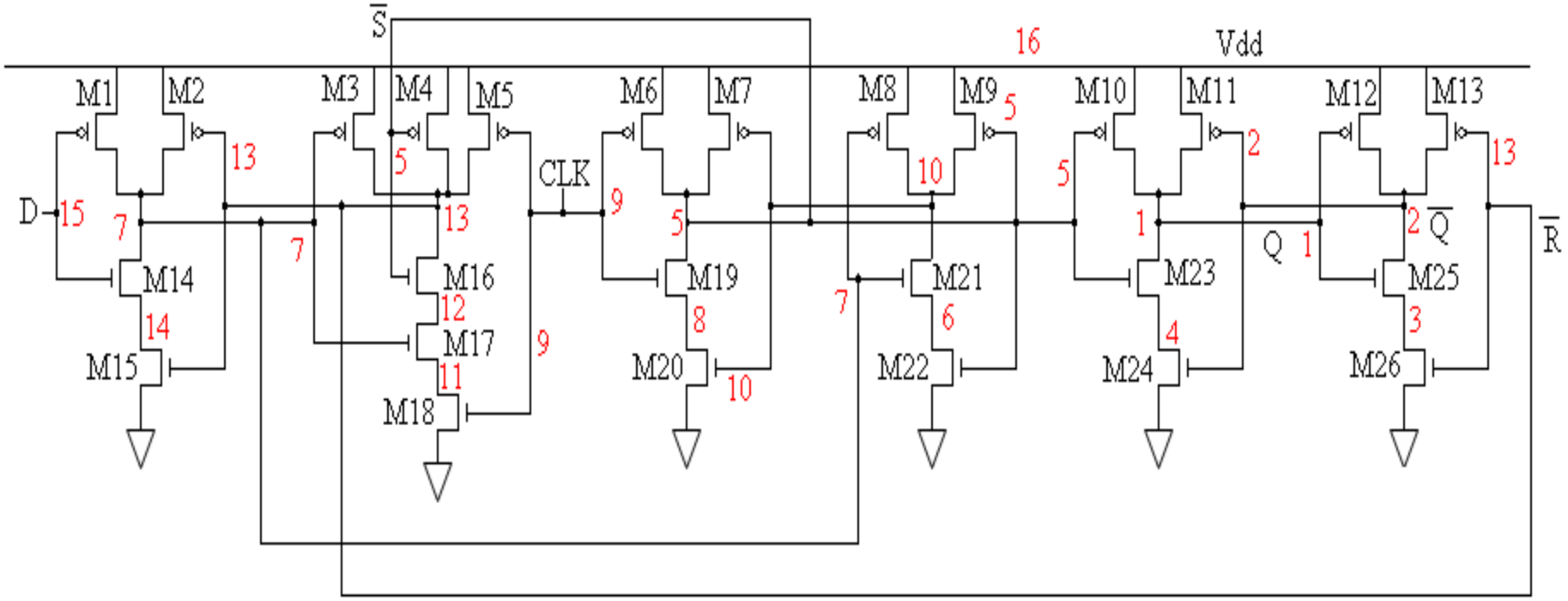




Inputs		Outputs	
D	C	Q^+	$\overline{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\overline{Q}$
X	1	Q	$\overline{Q}$

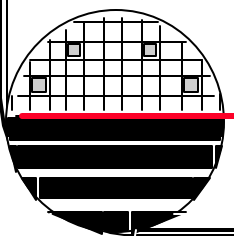


D (Edge Triggered)Flip Flop Realization



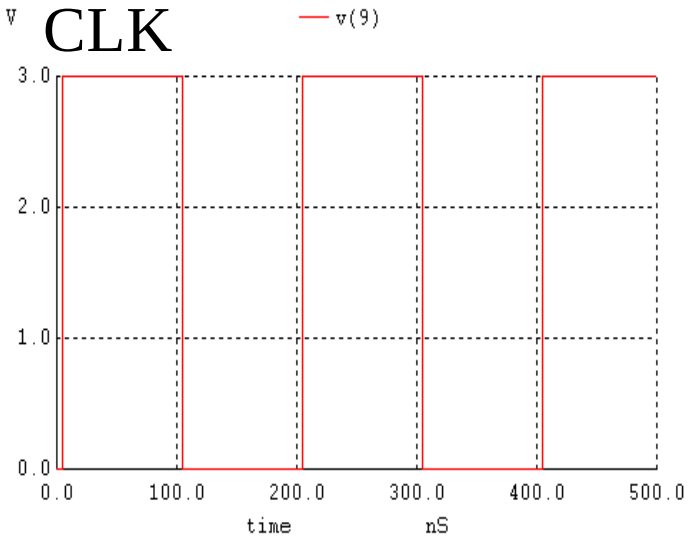
D FF (Edge Triggered) Input File:

```
.incl rit_sub_param.txt
m1 7 15 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m2 7 13 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m3 13 7 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m4 13 5 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m5 13 9 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m6 5 9 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m7 5 10 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m8 10 7 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m9 10 5 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m10 1 5 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m11 1 2 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m12 2 1 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m13 2 13 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m14 7 15 14 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m15 14 13 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m16 13 5 12 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m17 12 7 11 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m18 11 9 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m19 5 9 8 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m20 8 10 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m21 10 7 6 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m22 6 5 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m23 1 5 4 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m24 4 2 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m25 2 1 3 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m26 3 13 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
vdd 16 0 3
vd 15 0 PULSE(0 3 0NS 0NS 0NS 150NS 300NS)
vclock 9 0 PULSE(0 3 5NS 0NS 0NS 100NS 200NS)
*****transient*******
.tran 0.1n 0.5u
.end
```

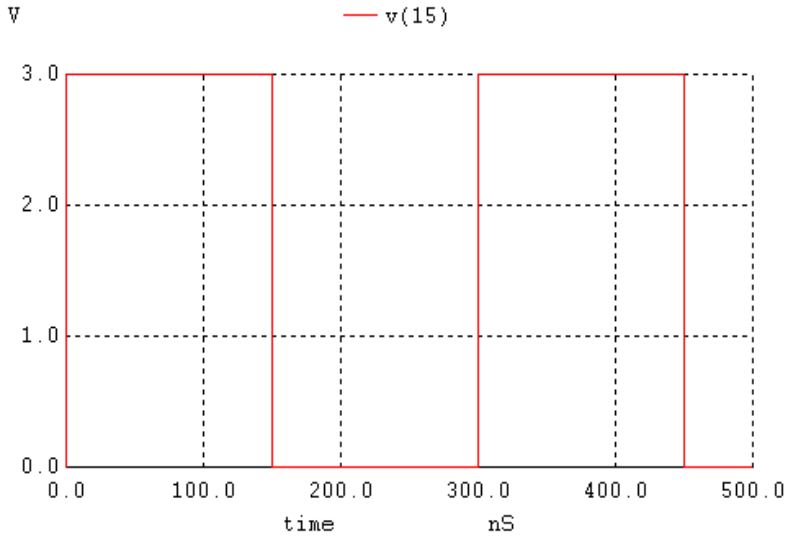


EDGE TRIGGERED D FF SIMULATION RESULTS

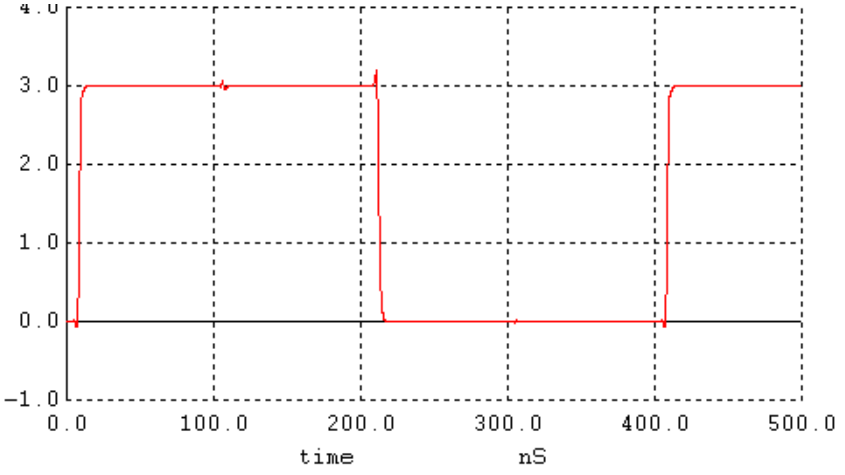
CLK



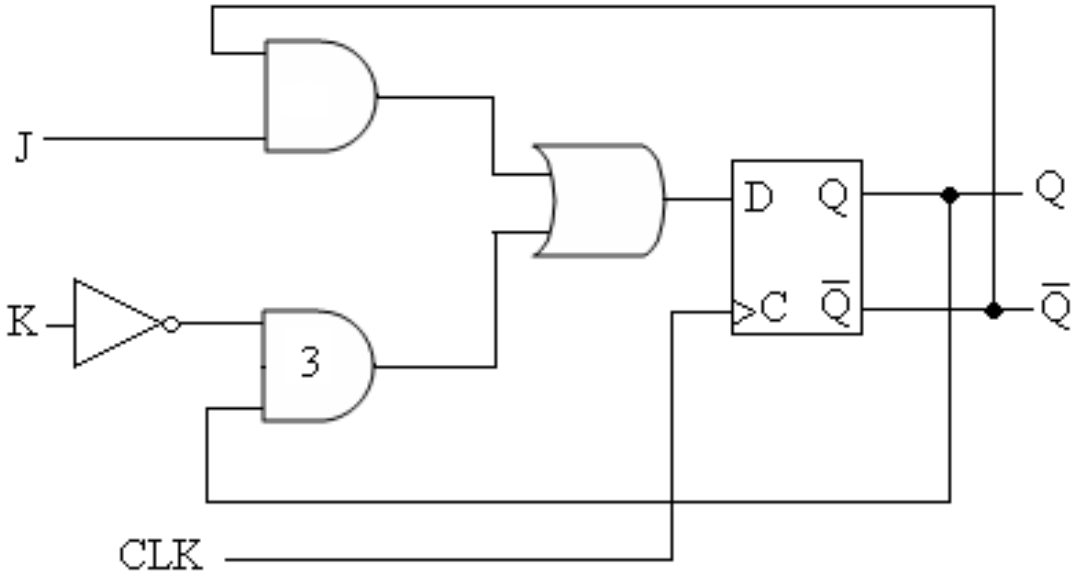
D



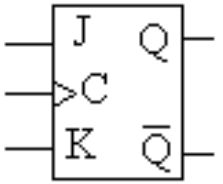
Q



JK FLIP FLOP

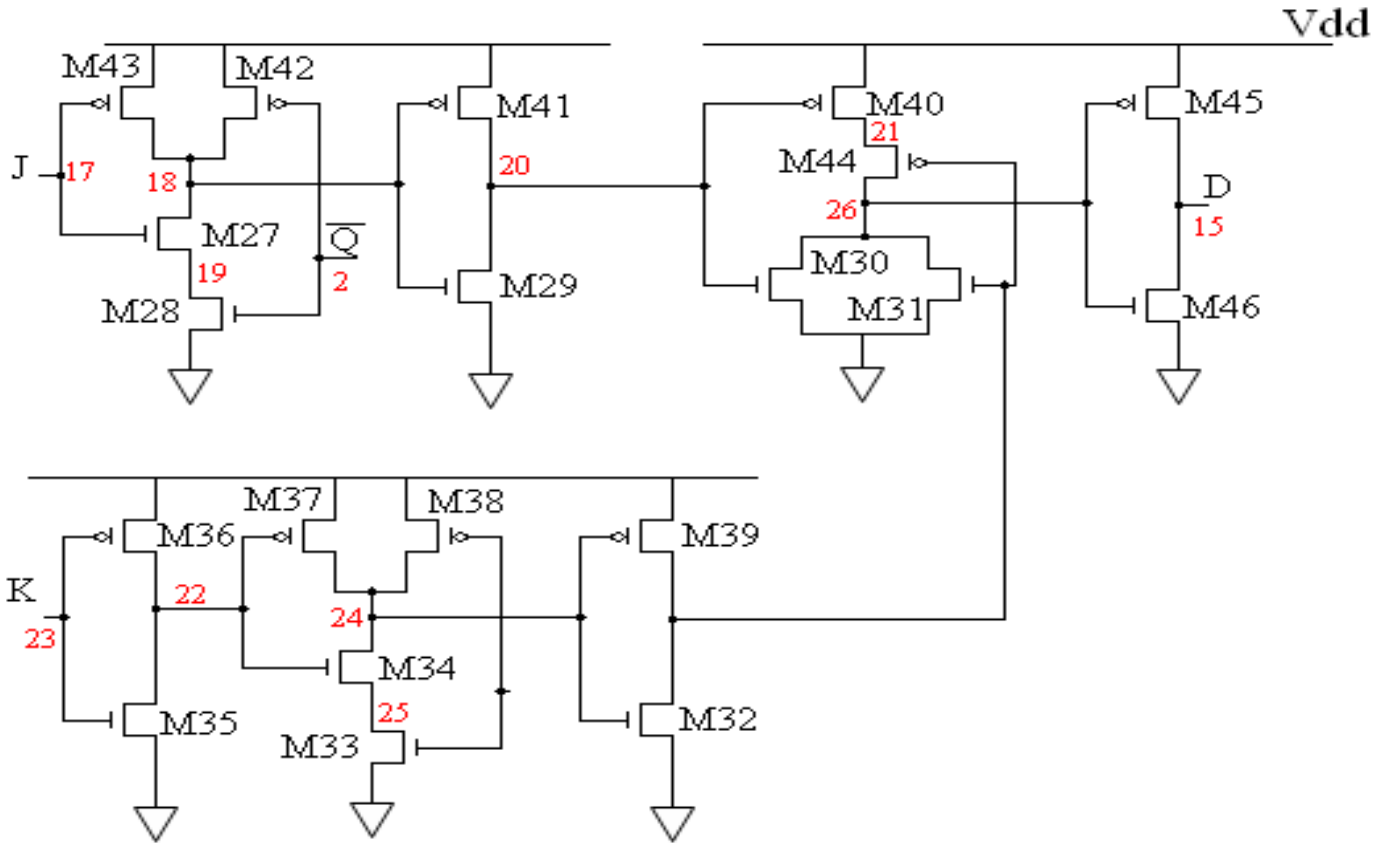


Positive Edge Triggered JK FF



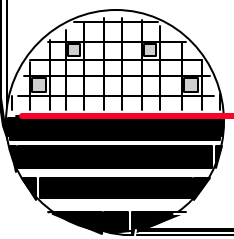
Inputs			Outputs	
J	K	C	Q^+	$\overline{Q^+}$
0	0	↑	Q	$\overline{Q}$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\overline{Q}$	Q
X	X	0	Q	$\overline{Q}$
X	X	1	Q	$\overline{Q}$

Modification to Convert D FF to JK FF



JK FF Input File:

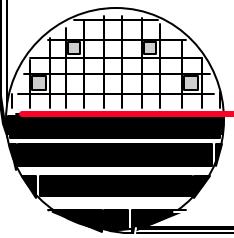
```
.incl rit_sub_param.txt
m1 7 15 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m2 7 13 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m3 13 7 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m4 13 5 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m5 13 9 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m6 5 9 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m7 5 10 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m8 10 7 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m9 10 5 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m10 1 5 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m11 1 2 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m12 2 1 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m13 2 13 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m14 7 15 14 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m15 14 13 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m16 13 5 12 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m17 12 7 11 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m18 11 9 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m19 5 9 8 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m20 8 10 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m21 10 7 6 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m22 6 5 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m23 1 5 4 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m24 4 2 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m25 2 1 3 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m26 3 13 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
```



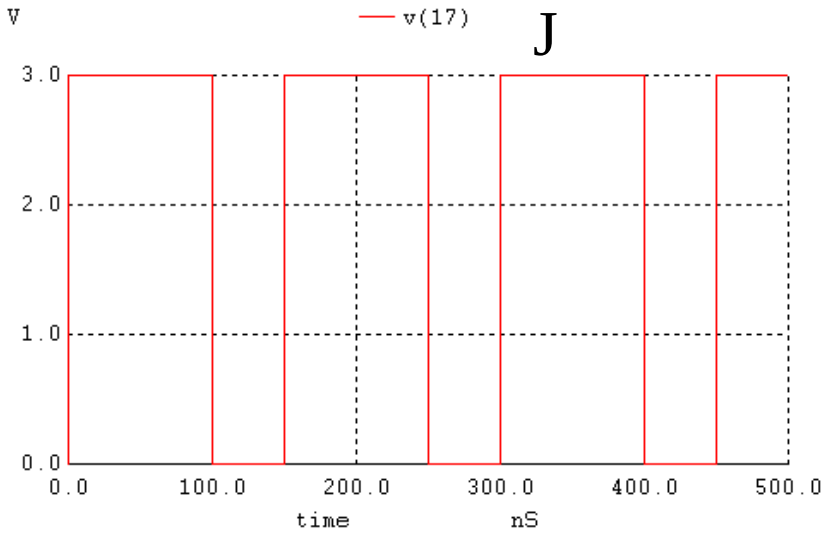
Transistors 27-46 on next page

JK FF Input File:

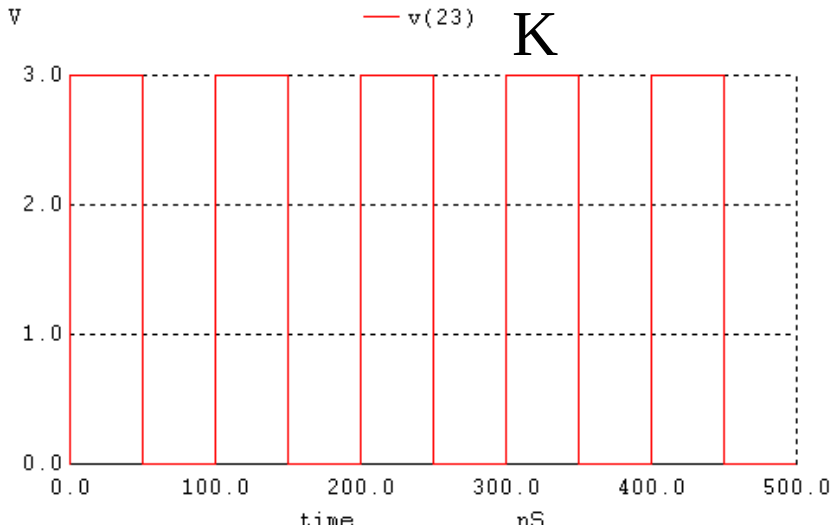
```
vdd 16 0 3
vj 17 0 PULSE(0 3 0NS 0NS 0NS 100NS 150NS)
vk 23 0 PULSE(0 3 0NS 0NS 0NS 50NS 100NS)
vclock 9 0 PULSE(0 3 50NS 0NS 0NS 50NS 150NS)
**********************
m27 18 17 19 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m28 19 2 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m29 20 18 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m30 26 20 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m31 26 25 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m32 25 24 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m33 25 1 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m34 24 22 25 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m35 22 23 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m36 22 23 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m37 24 22 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m38 24 1 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m39 25 24 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m40 21 20 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m41 20 18 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m42 18 2 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m43 18 17 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m44 26 25 21 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m45 15 26 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m46 15 26 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
*****transient*******
.tran 0.1n 0.5u
.end
```



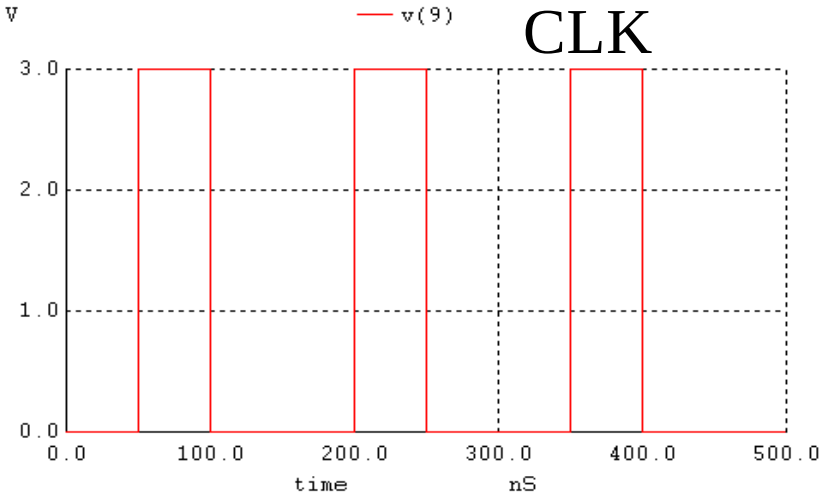
JK FF Simulation Output:



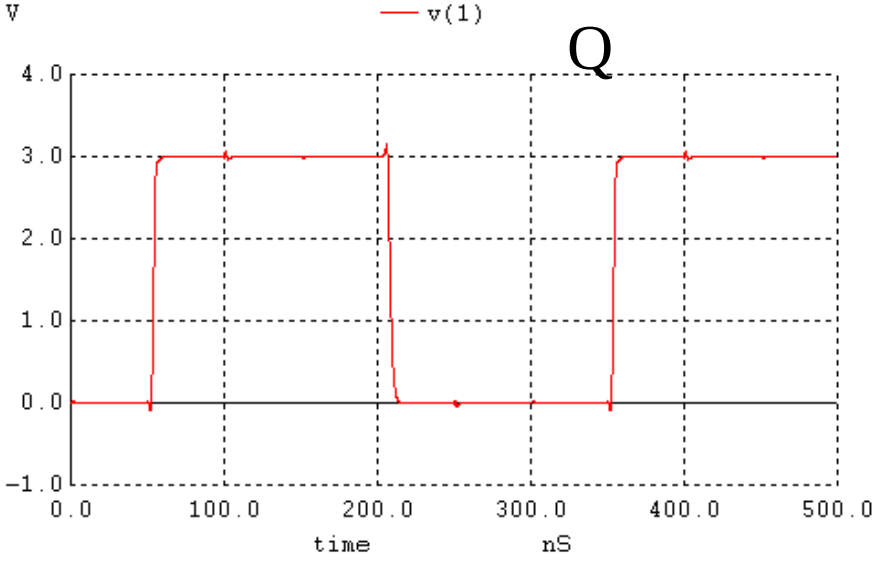
J



K

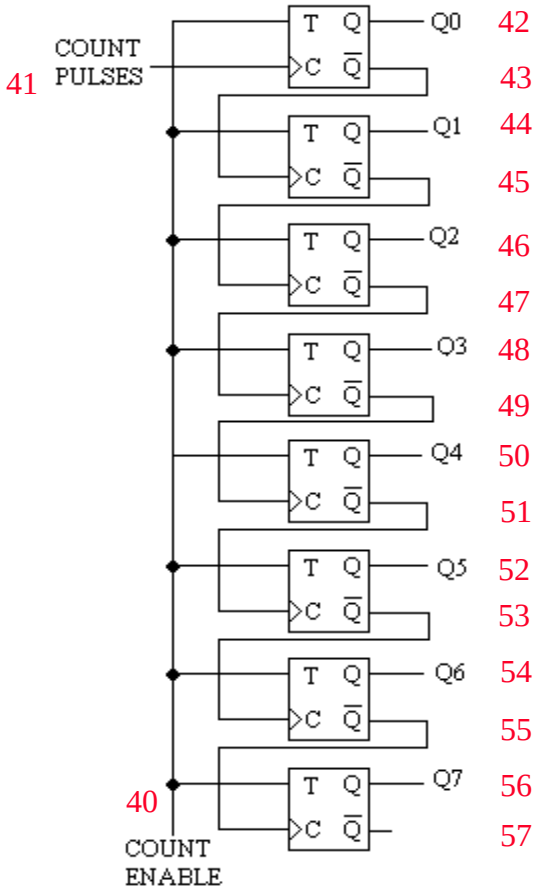


CLK



Q

Constructing 8 bit Binary Counter Using T FF



T Flip Flop is a JK FF With J and K connected together and labeled T

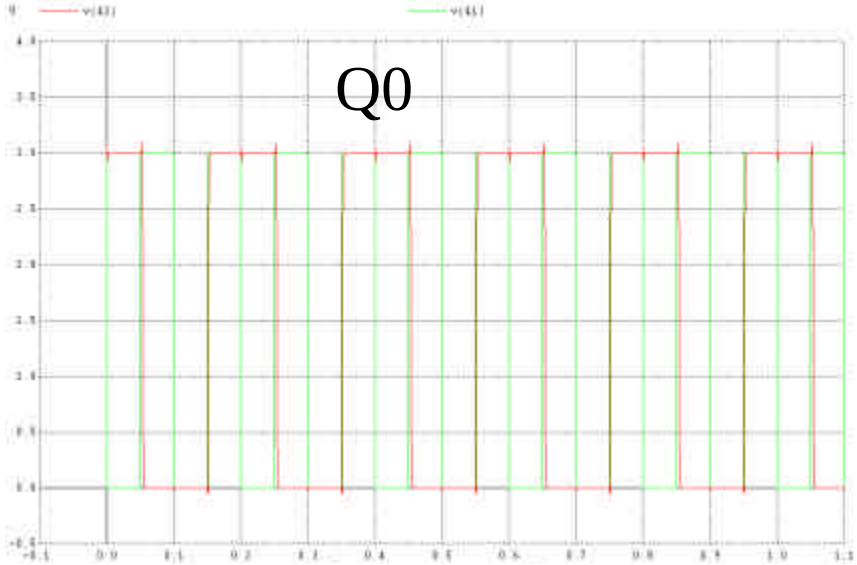
8 Bit Binary Counter Input File:

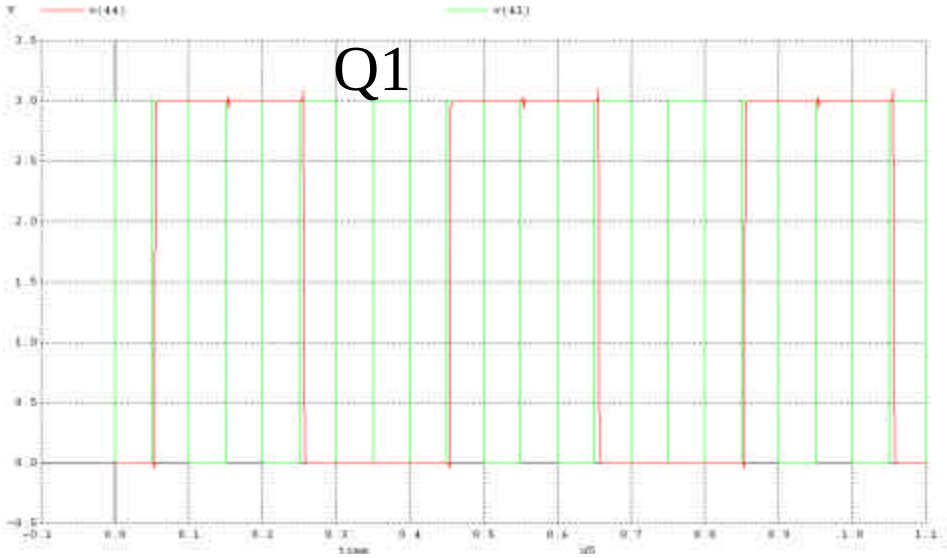
```
.incl rit_sub_param.txt
.subckt Tff 17 9 1 2
m1 7 15 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m2 7 13 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m3 13 7 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m4 13 5 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m5 13 9 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m6 5 9 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m7 5 10 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m8 10 7 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m9 10 5 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m10 1 5 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m11 1 2 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m12 2 1 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m13 2 13 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m14 7 15 14 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m15 14 13 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m16 13 5 12 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m17 12 7 11 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m18 11 9 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m19 5 9 8 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m20 8 10 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m21 10 7 6 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m22 6 5 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m23 1 5 4 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m24 4 2 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m25 2 1 3 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m26 3 13 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
vd 16 0 3
vjk 17 23 dc 0
**********************
```

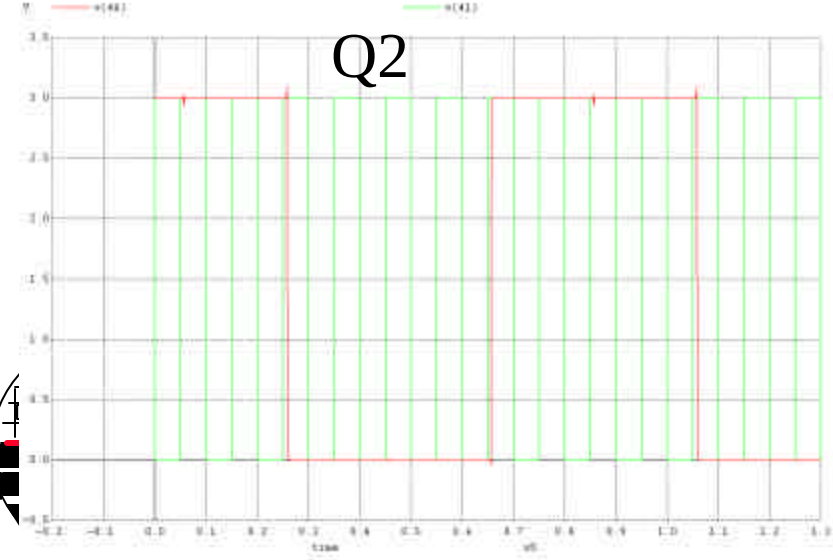
8 Bit Binary Counter Input File:

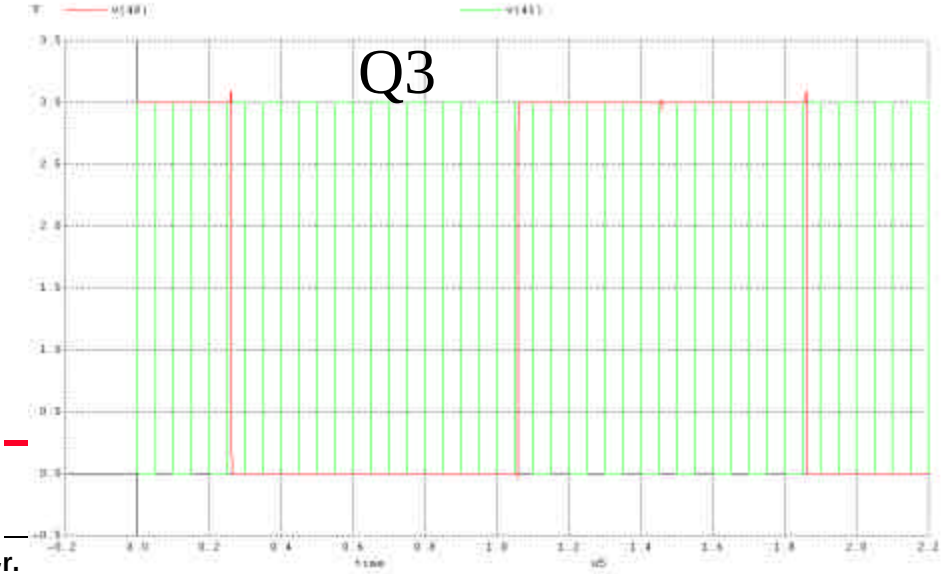
```
m27 18 17 19 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m28 19 2 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m29 20 18 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m30 26 20 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m31 26 25 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m32 25 24 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m33 25 1 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m34 24 22 25 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m35 22 23 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
m36 22 23 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m37 24 22 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m38 24 1 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m39 25 24 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m40 21 20 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m41 20 18 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m42 18 2 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m43 18 17 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m44 26 25 21 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m45 15 26 16 16 cmosp w=7.5u l=2u ad=35p pd=25u as=35p ps=25u
m46 15 26 0 0 cmosn w=3u   l=2u ad=15p pd=16u as=15p ps=16u
**************************
.ends
xB0 40 41 42 43 Tff
xB1 40 43 44 45 Tff
xB2 40 45 46 47 Tff
xB3 40 47 48 49 Tff
xB4 40 49 50 51 Tff
xB5 40 51 52 53 Tff
xB6 40 53 54 55 Tff
xB7 40 55 56 57 Tff
Vcountenable  40 0 3
vcount 41 0 PULSE(3 0 0NS 0NS 0NS 50NS 100NS)
.tran 0.1n 13u
.end
```

8 Bit Binary Counter Output:

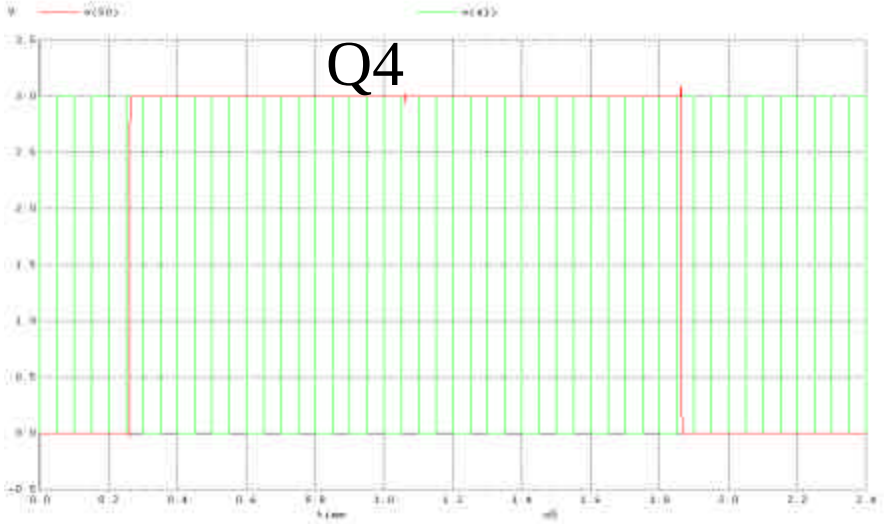


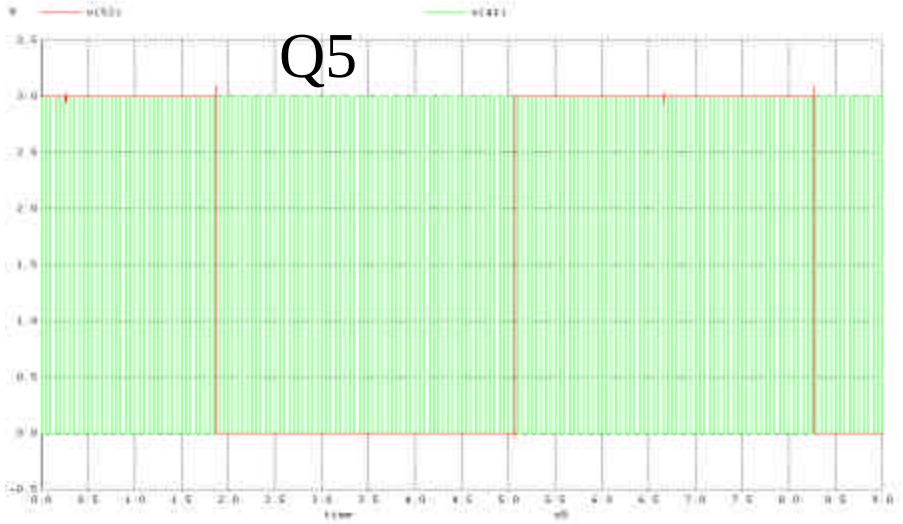


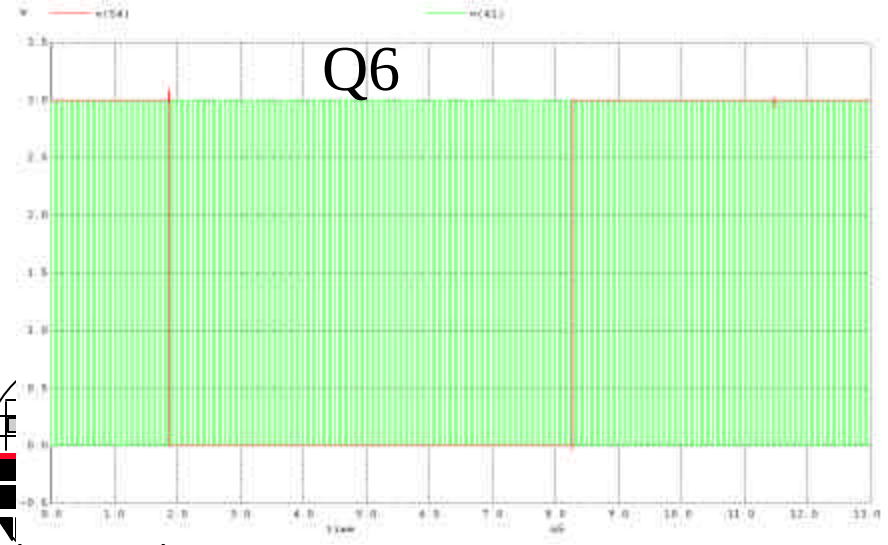


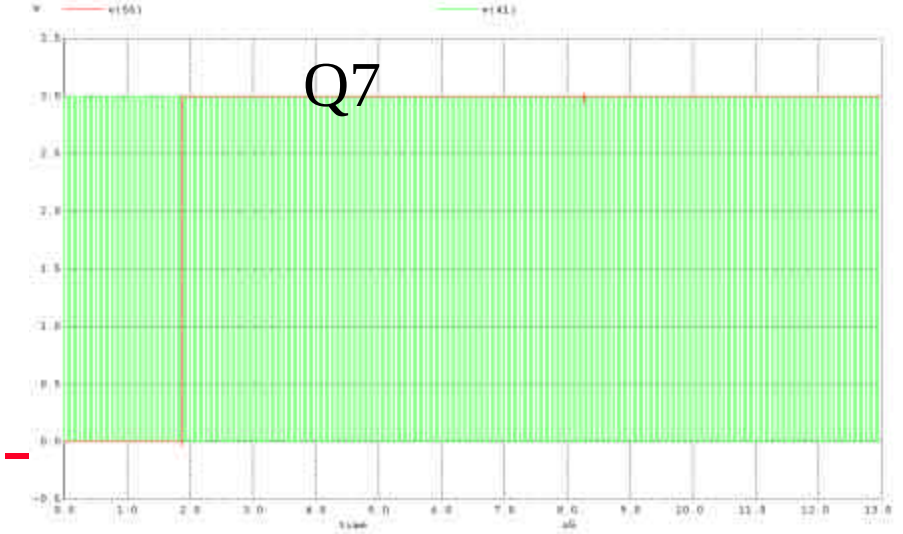


8 Bit Binary Counter Output:

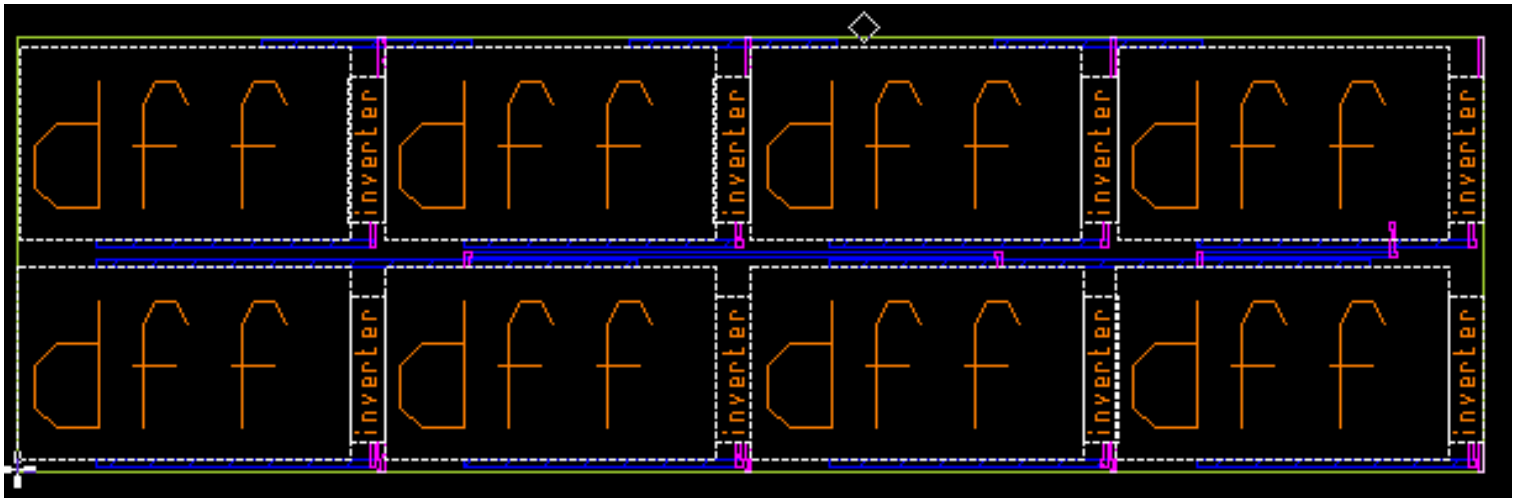


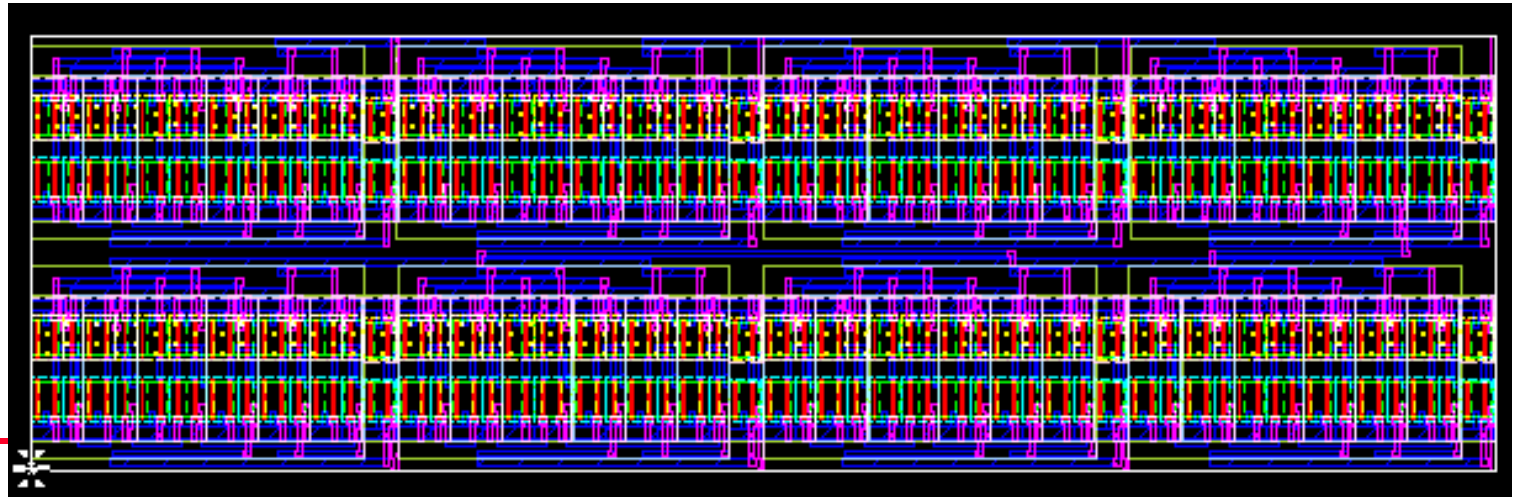




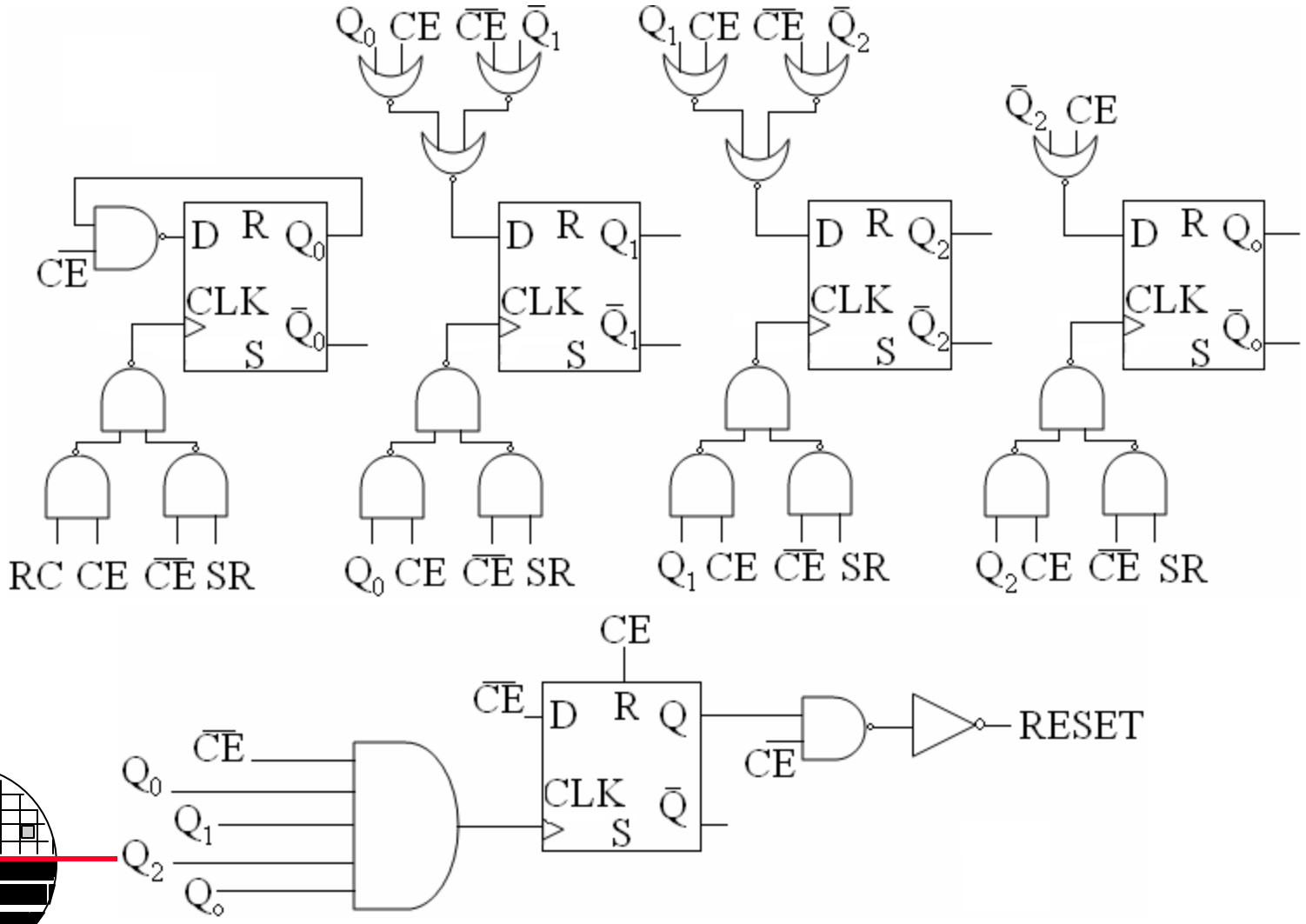


8-BIT BINARY COUNTER

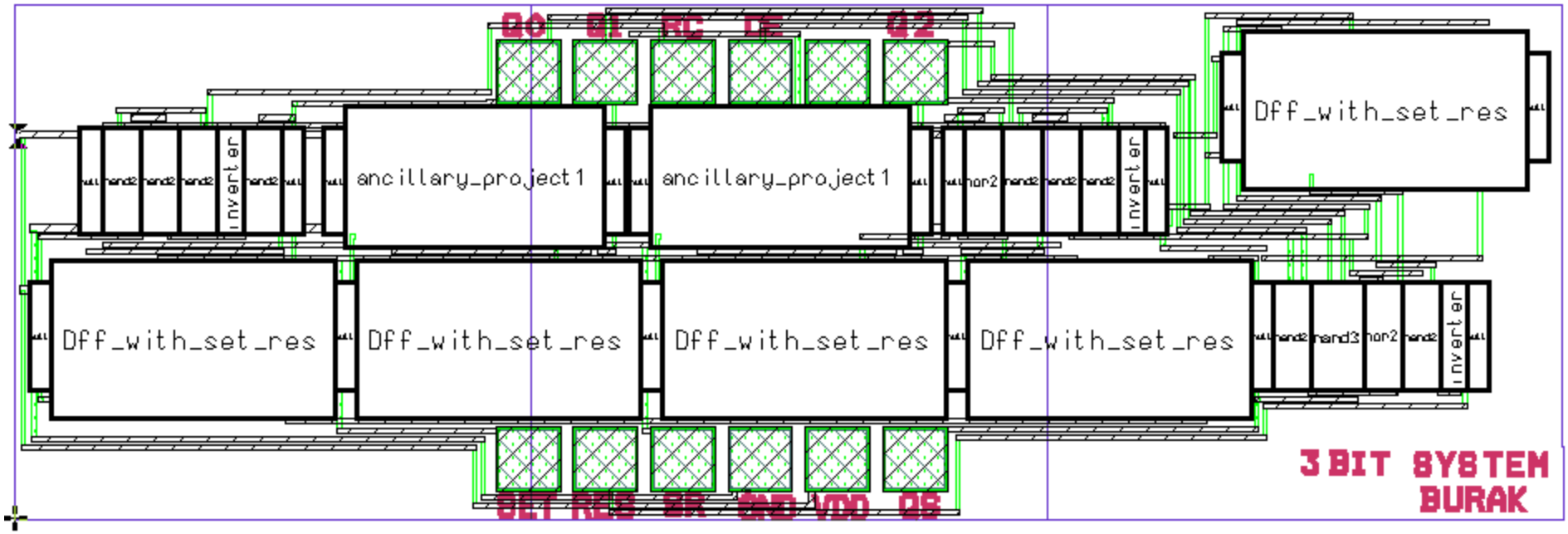


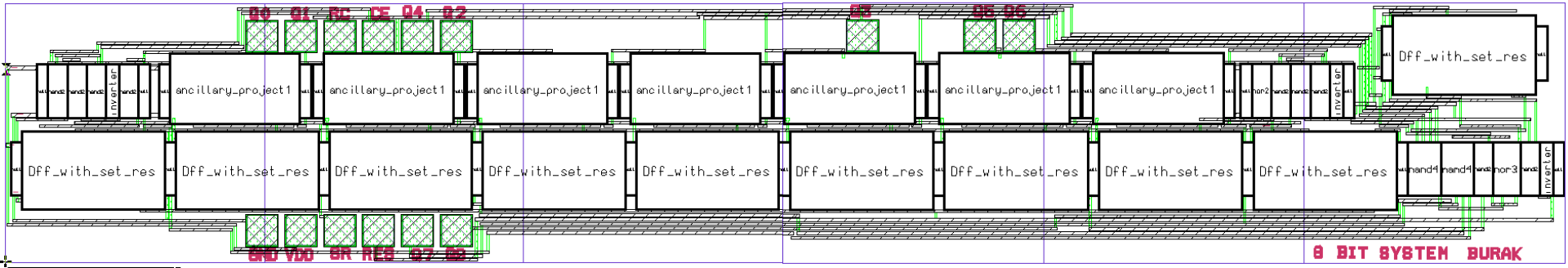


ADDITIONAL CIRCUITRY TO RESET, SHIFT, COUNT

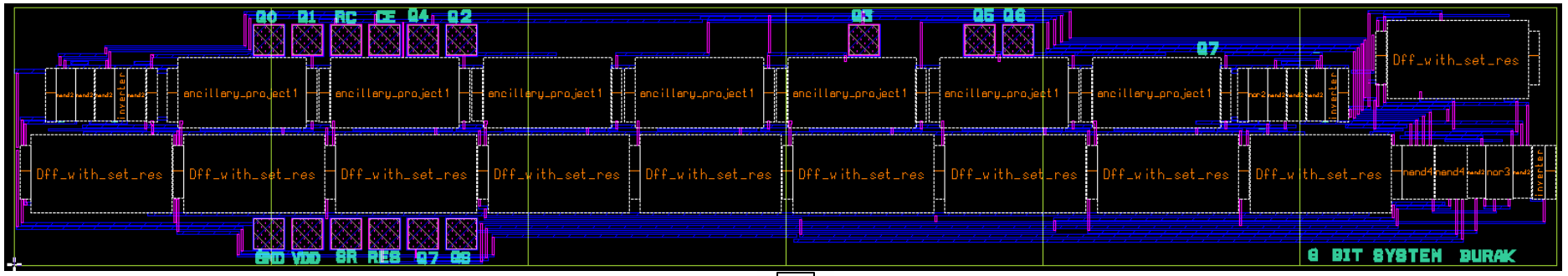


UP/DOWN COUNTER AND SHIFT REGISTERS

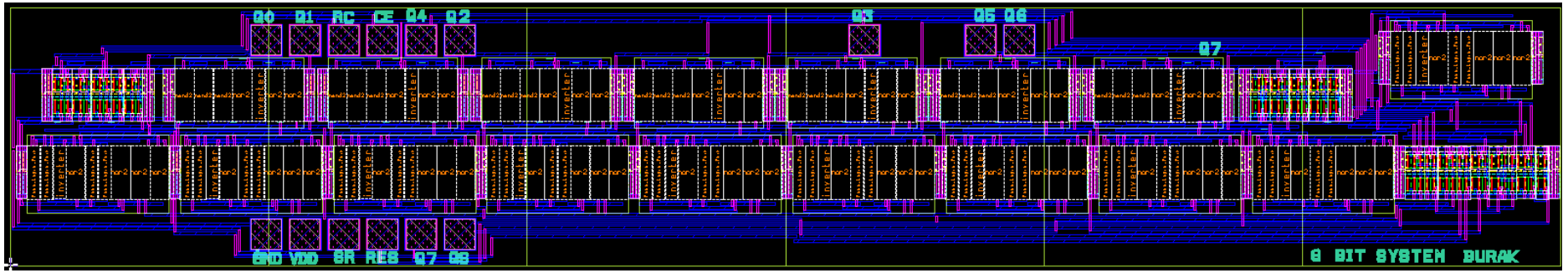




8-BIT BINARY COUNTER/SHIFT REGISTER



peek in 1 level



COUNTER AND SHIFT REGISTER

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS037

CD4034B Types

CMOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

High-Voltage Types (20-Volt Rating)

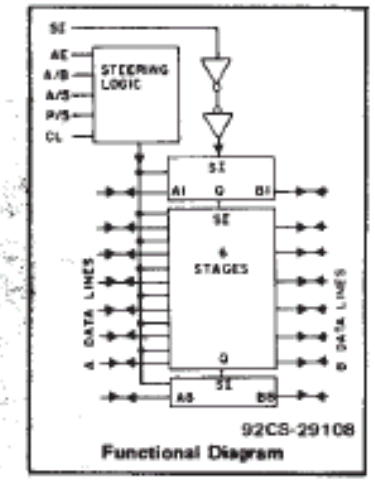
■ CD4034B is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are

Applications:

- Parallel Input/Parallel Output, Serial Input/Parallel Output, Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator



Functional Diagram

Features:

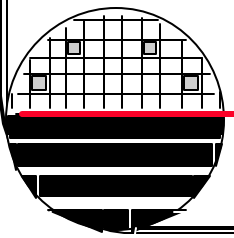
- Bidirectional parallel data input
- Parallel or serial inputs/parallel outputs
- Asynchronous or synchronous parallel data loading
- Parallel data-input enable on "A" data

REFERENCES

1. Switched Capacitor Circuits, Phillip E. Allen and Edgar Sanchez-Sinencio, Van Nostrand Reinhold Publishers, 1984.

2. "Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial," Randall L. Geiger and Edgar Sanchez-Sinencio, IEEE Circuits and Devices Magazine, March 1985, pg. 20-32.

3. Microelectronic Circuits, 5th Edition, Sedra and Smith, Chapter 9 section 9.7-9.9



HOMEWORK – DATA CONVERSION

1. Create two good homework problems and their solution related to the material covered in this document. (for next years students)

2.