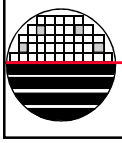
ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Testing – Device Problem Analysis

Dr. Lynn Fuller

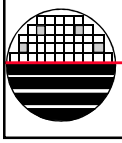
Webpage: http://people.rit.edu/lffeee
Electrical and Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Email: Lynn.Fuller@rit.edu
MicroE webpage: http://www.microe.rit.edu



4-27-2014 Device_Test.ppt

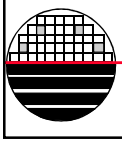
OUTLINE

Introduction
Good Device Characteristics
Various Not So Good Device Characteristics
Discussion of Characteristics
Design Errors
Fabrication Problems

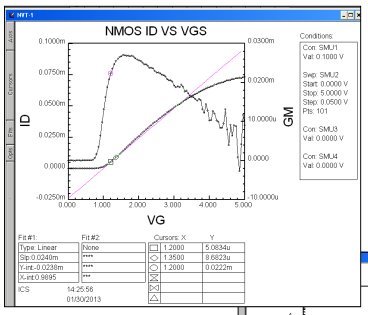


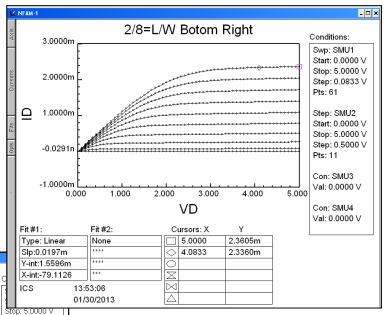
INTRODUCTION

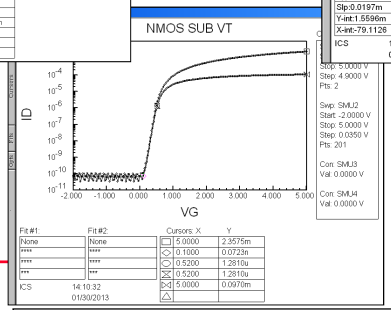
This document is a collection of test results showing problems with various semiconductor devices made in the microelectronics fabrication laboratory. The objective is to provide useful information for identification of the source of problems and to enhance the education of our students.

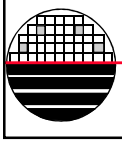


GOOD NMOS DEVICE CHARACTERISTICS



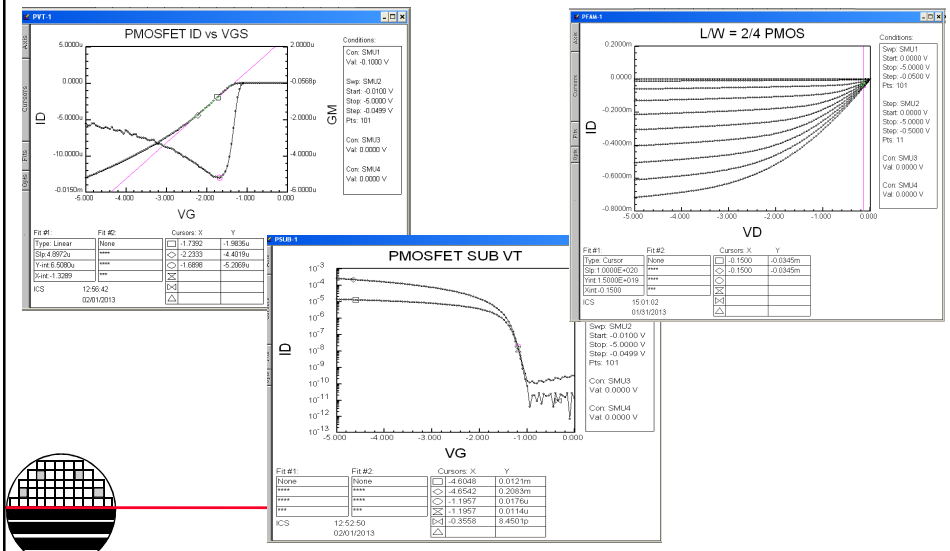






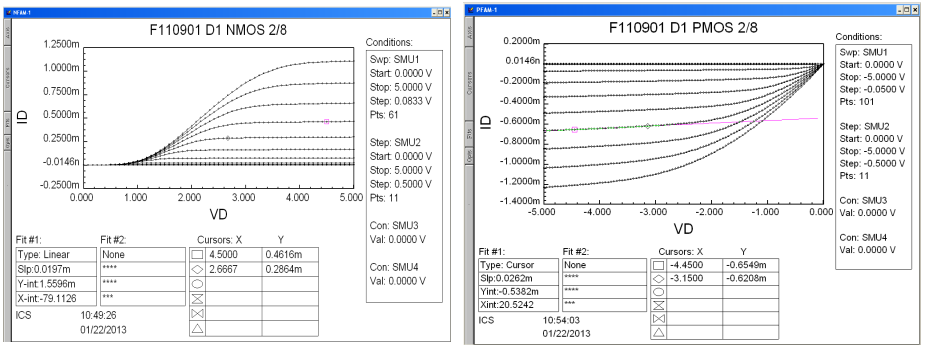
Testing – Device Problem Analysis

GOOD PMOS DEVICE CHARACTERISTICS

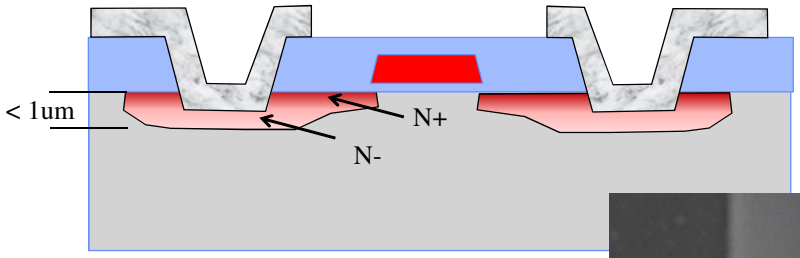


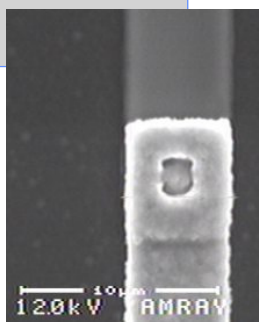
Testing – Device Problem Analysis

NON OHMIC CONTACT TO NMOS DRAIN/SOURCE IN SUB-CMOS PROCESS



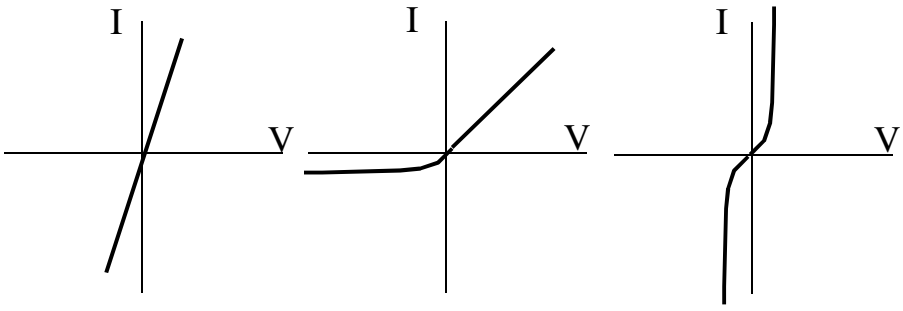
NON OHMIC CONTACT TO NMOS DRAIN/SOURCE IN SUB-CMOS PROCESS





Over etched contact cuts makes a non-ohmic (rectifying or Schottky) contact with the lighter doped n-type area of the drain/source. P-type devices have ohmic contacts.

CONTACTS TO SILICON

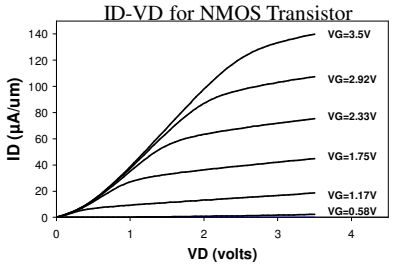


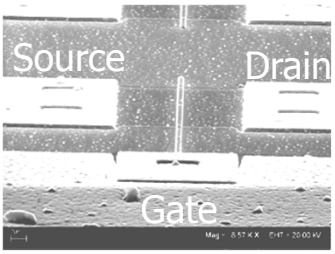
Ideal Ohmic
Al/p-silicon

Rectifying
Al/n-silicon

Tunneling Ohmic
Al/n+-silicon

NON OHMIC CONTACT TO NMOS DRAIN/SOURCE IN ADV-CMOS PROCESS

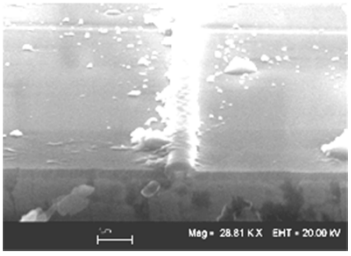




$L_{mask\ drawn} = 0.6\ \mu m$

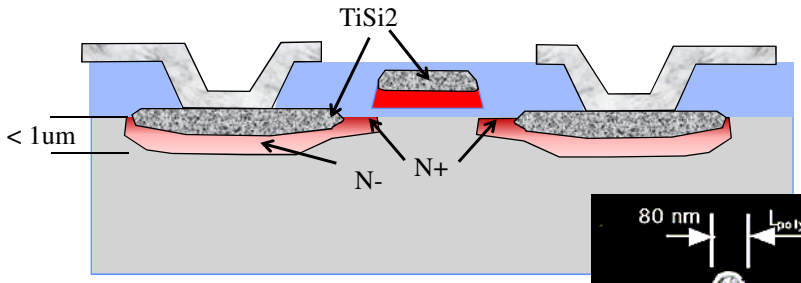
$L_{effective} = 0.4\ \mu m$

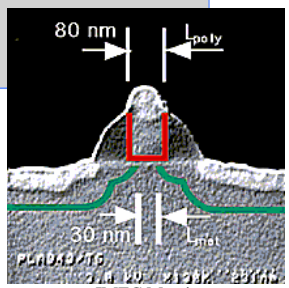
This is RIT's first sub-0.5 µm Transistor



Mike Aquilino May 2004

SILICIDE FORMATION CONSUMES SILICON

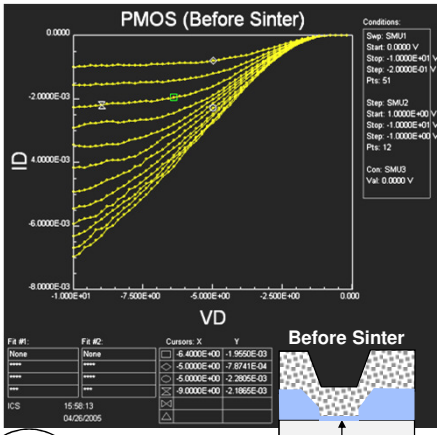


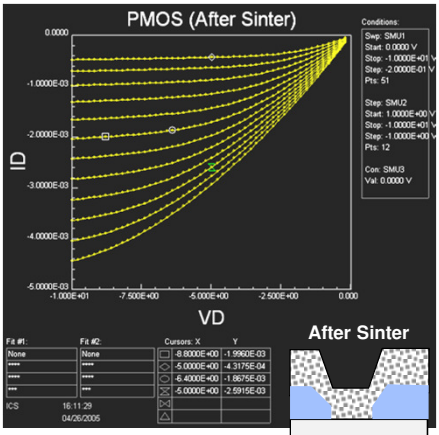


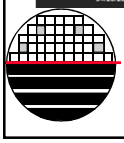
IMEC Meeting
December 1999

Too much silicide formation makes a non-ohmic (rectifying or Schottky) contact with the lighter doped n-type area of the drain/source.

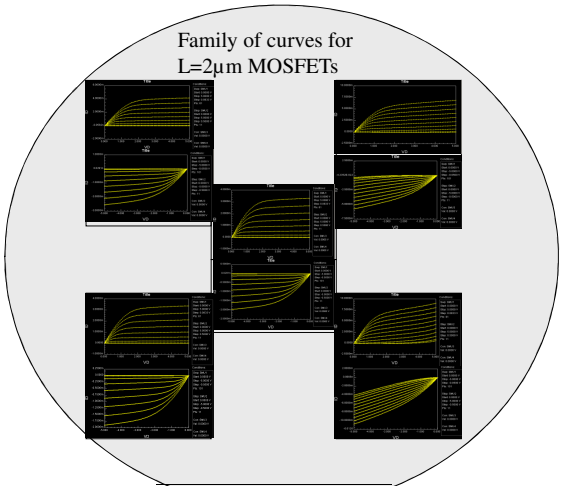
EFFECT OF SINTER ON IV CHARACTERISTICS



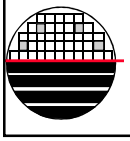




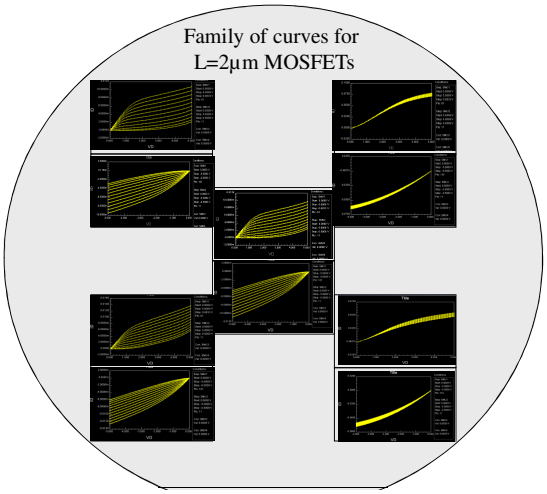
DIFFERENT LOOKING FAMILY OF CURVES AT DIFFERENT LOCATIONS ON THE WAFER



2µm/32µm L/W NMOS AND PMOS

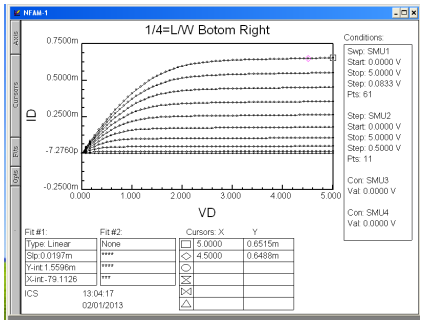


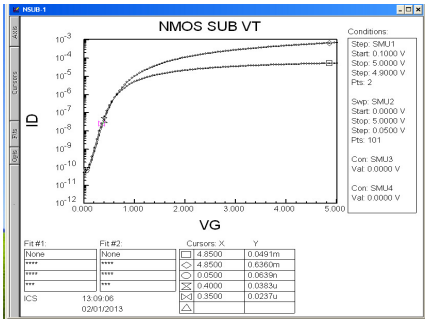
NON UNIFORMITY IN PLASMA ETCH OF POLY



2µm/32µm L/W NMOS AND PMOS

GOOD DEVICE SUB THRESHOLD CHARACTERISTICS

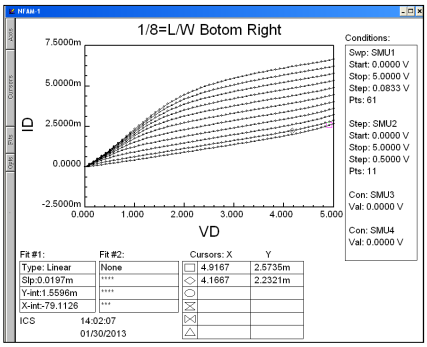


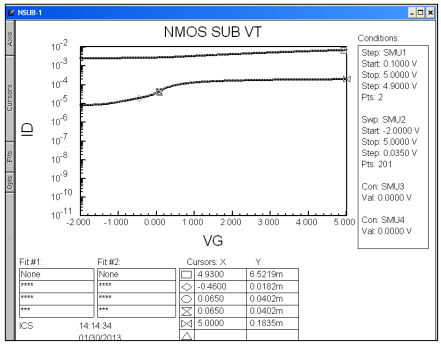


Occasionally our 1um Devices Work
Why does the sub-threshold plot not flatten out at the bottom?

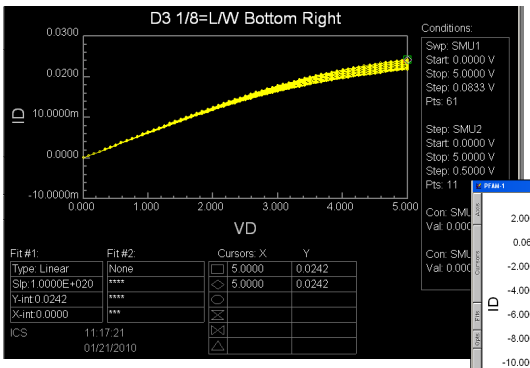
Answer: Vt is ~0.5 volt and swing is ~100mV/decade so at zero volts the device can be down 5 decades of current which is 10^{-10} it should flatten out at ~ 10^{-11} or 10^{-12} …… need higher Vt or smaller swing

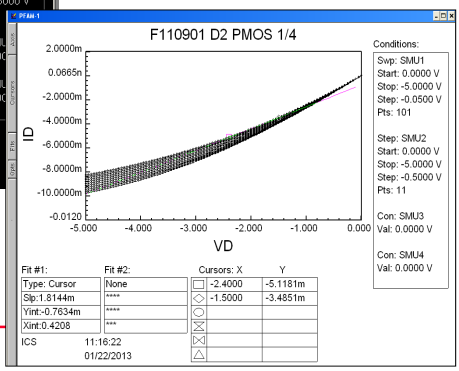
SHORT CHANNEL – BAD SUB THESHOLD



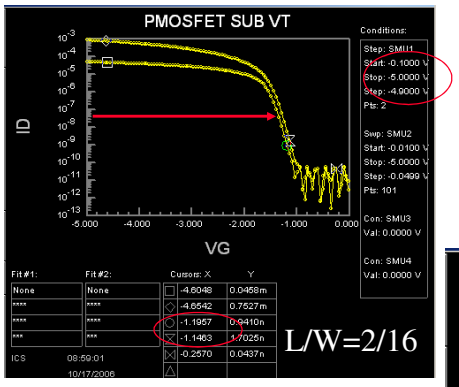


REALLY SHORT CHANNEL



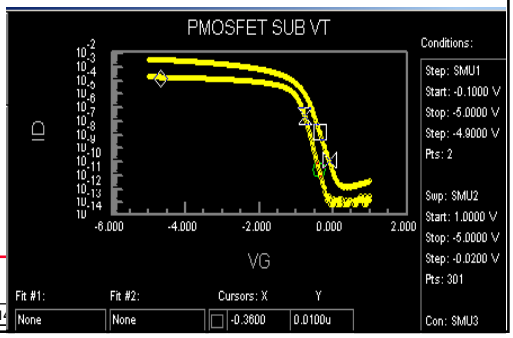


DRAIN INDUCED BARRIER LOWERING

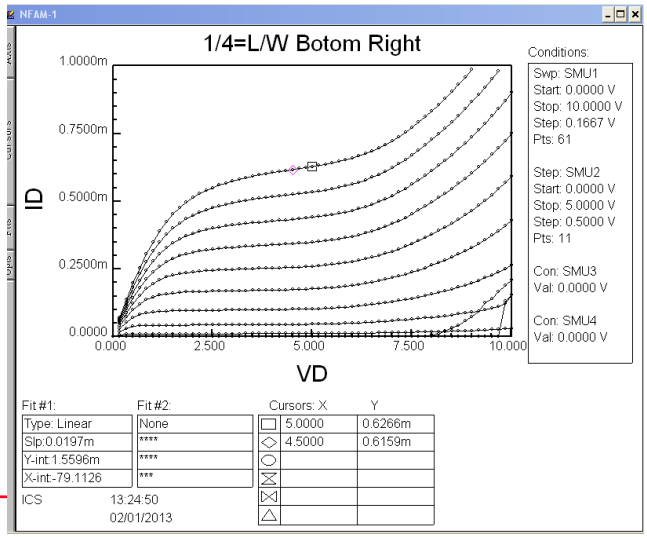


DIBL = change in VG /change in VD
at ID=1E-9 amps/µm
or 1.6E-8 amps for this
size transistor

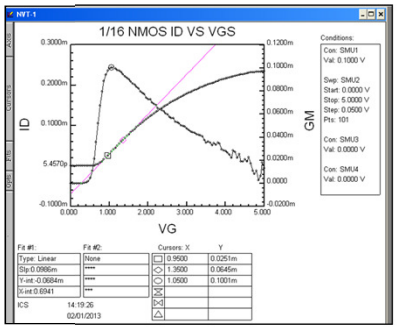
= ~ (1.1957-1.1463)/(5-0.1)
= ~ 10mV/V



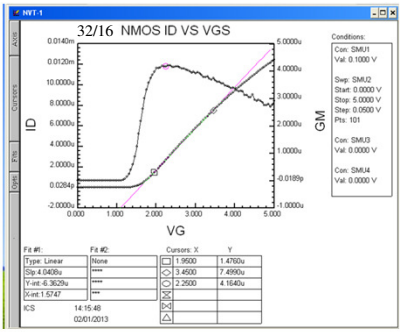
PUNCH THROUGH



MOBILITY DEGRADATION

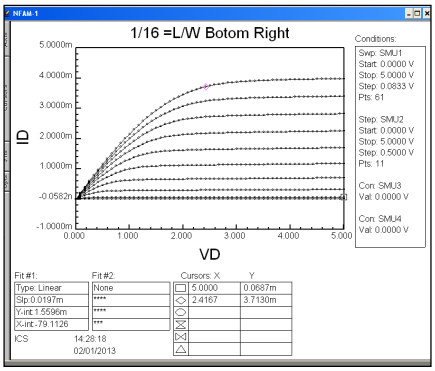


Short channel

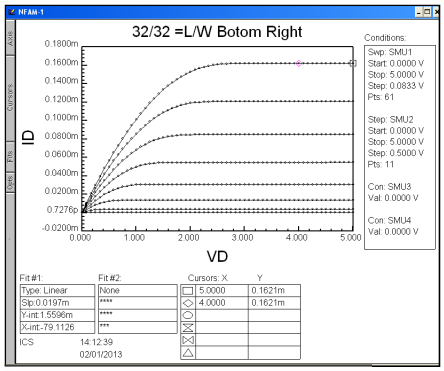


long channel

VELOCITY SATURATION



Short channel



long channel

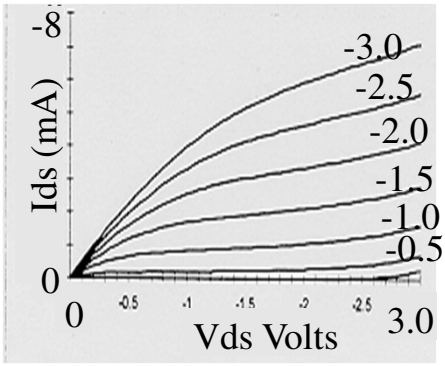
Note: Id should increase with $(Vgs-Vt)^2$ in long channel devices

RIT's FIRST SUB MICRON TRANSISTOR

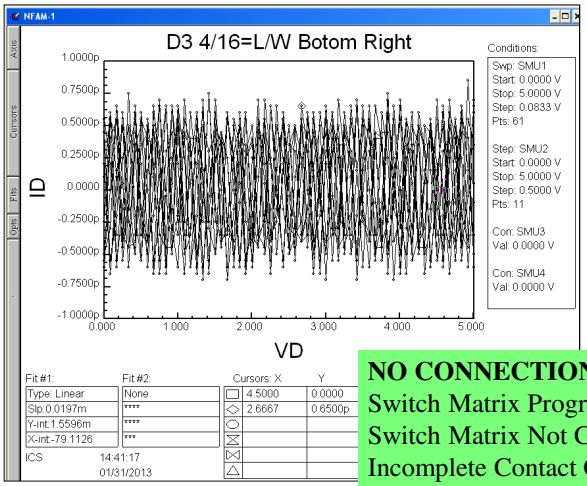
Mark Klare 7/22/94 Electron beam direct write on wafer, n-well process 5E12 dose, P+ Poly Gate PMOS, shallow BF2 D/S implant, no Vt adjust implant.

L=0.75 um
Xox=300 Å
D/S Xj = 0.25 µm
P+ poly
Nd well ~3E16

Vt = -0.15
Sub Vt Slope=130 mV/dec

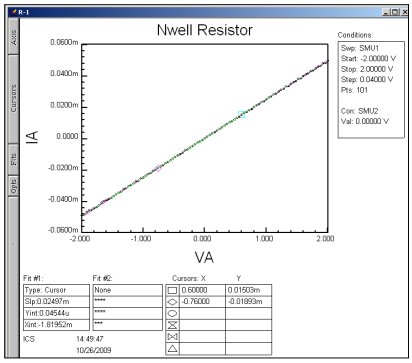


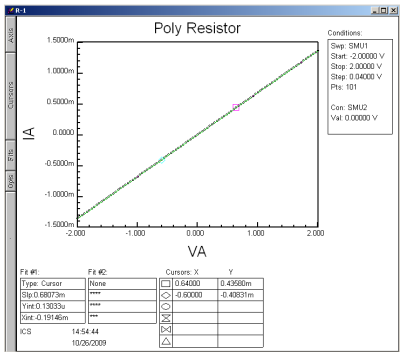
WHAT IS WRONG?



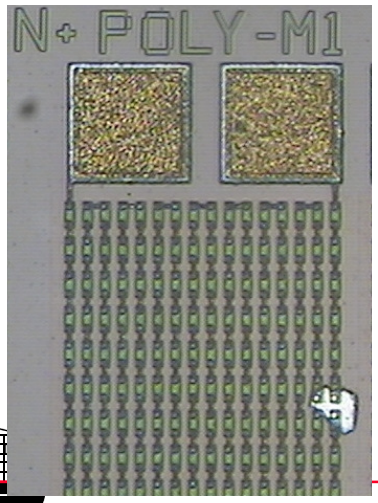
NO CONNECTION
Switch Matrix Programmed Wrong
Switch Matrix Not Copied
Incomplete Contact Cut Etch
Aluminum Oxide Between M1 and M2

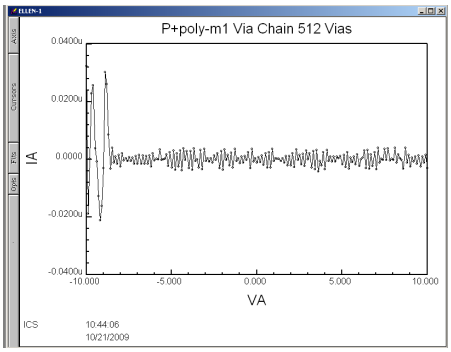
GOOD RESISTOR CHARACTERISTICS





IS THIS GOOD?

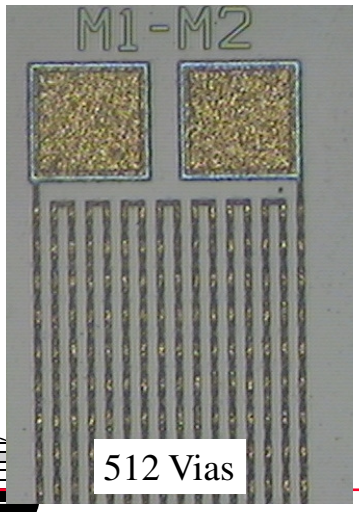




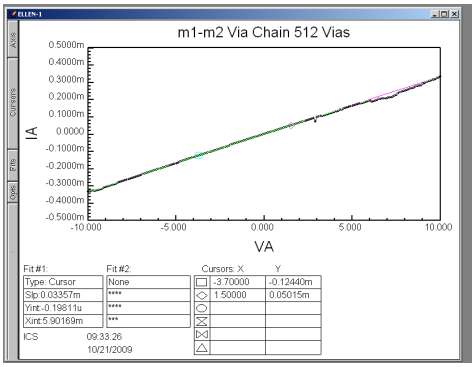
NO
Open Circuit, both electrical and visual evidence

Testing – Device Problem Analysis

IS THIS GOOD?



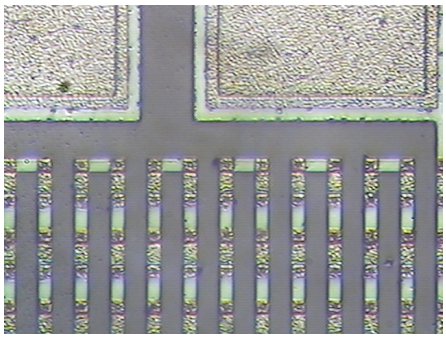
512 Vias



NO
R = 1/ slope = 1/.03357m = 29,788 ohms
which is 58 ohms/contact

Testing – Device Problem Analysis

IS THIS GOOD?



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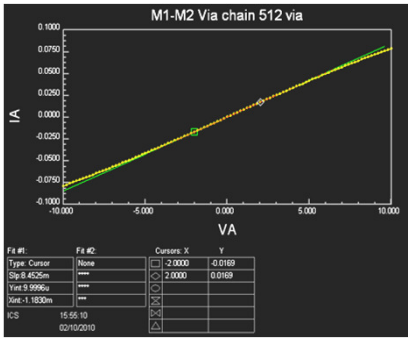
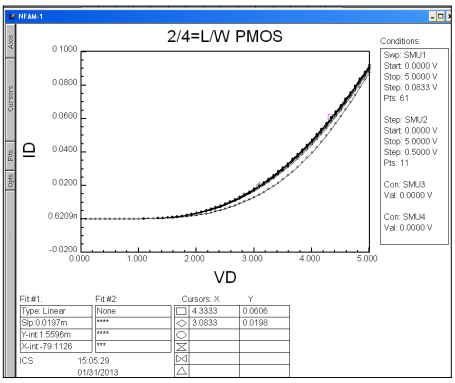


F081201

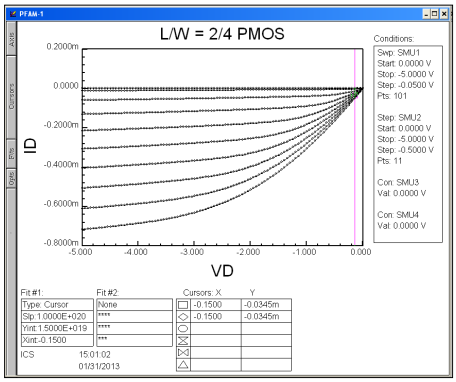
YES
M1-M2 Via chain with 512 Vias and total resistance of 118 ohms or 0.231 ohms per contact

Testing – Device Problem Analysis

WHAT IS WRONG?



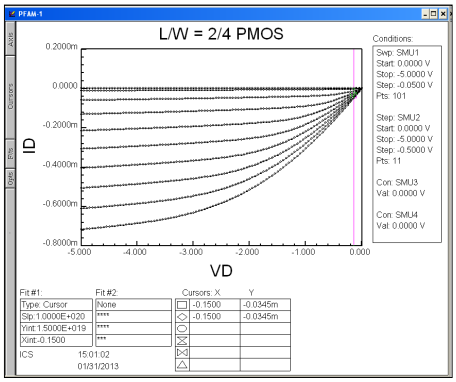
Testing PMOS with NMOS-1 Setup

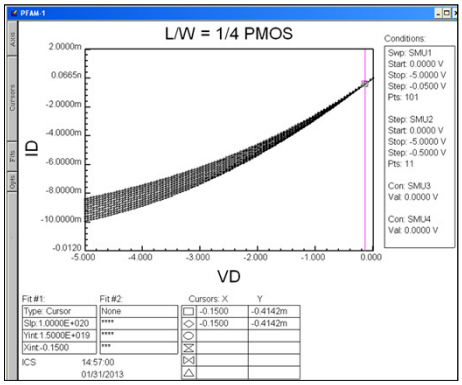


Testing PMOS with PMOS-1 Setup

Testing – Device Problem Analysis

WHAT IS WRONG?



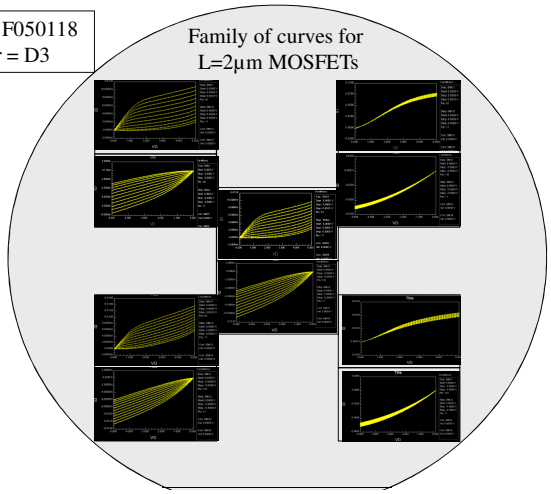


Leff is almost zero
Poly over etched making L too small
PMOS works at L/W = 2/4 but not at 1/4

NON UNIFORMITY IN PLASMA ETCH OF POLY

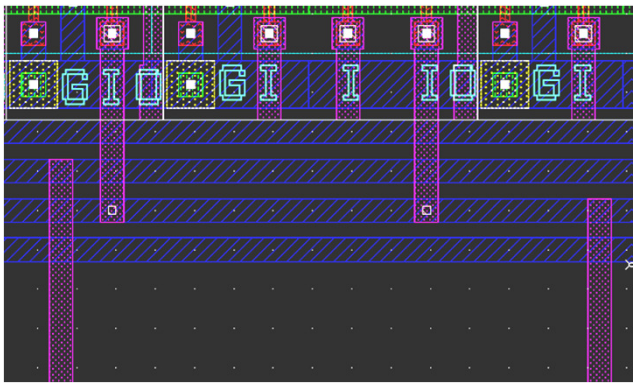
Lot Number = F050118
Wafer Number = D3

Family of curves for
L=2µm MOSFETs



2µm/32µm L/W NMOS AND PMOS

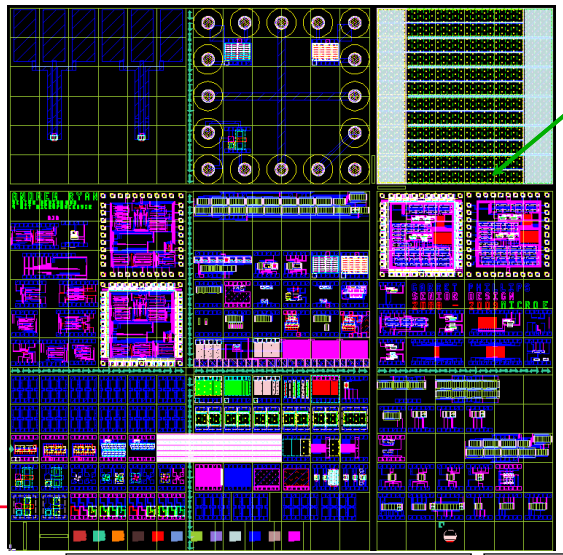
WHAT IS WRONG WITH THIS DIGITAL CIRCUIT



Design Errors – Missing Contact Cuts

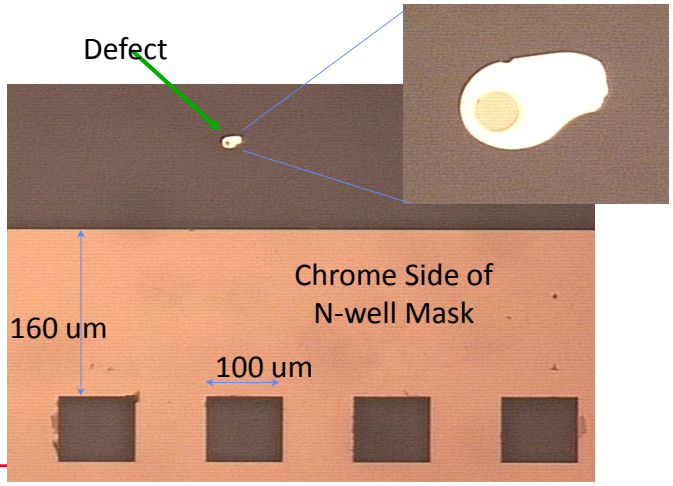
MASK DEFECTS

JOHN GALT CMOS TESTCHIP

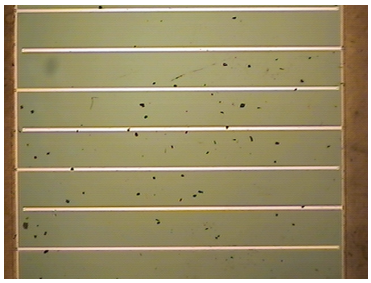


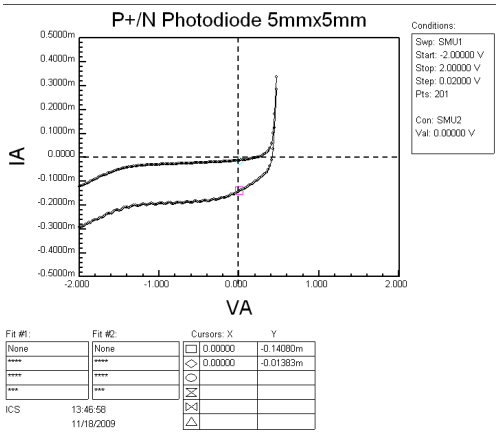
MASK DEFECT

This defect will cause a short through the pn junction of our solar cell.

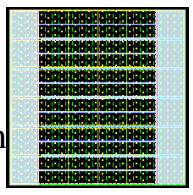


LARGE 5mm X 5mm PHOTODIODE



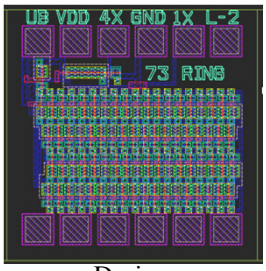


5mm
x
3.33mm

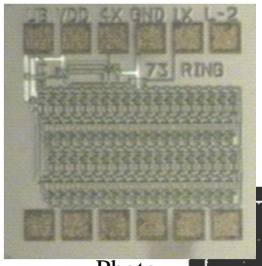


Isc = 0.15mA (short circuit current)
or 9.09 A/m2

73 STAGE RING OSCILLATOR



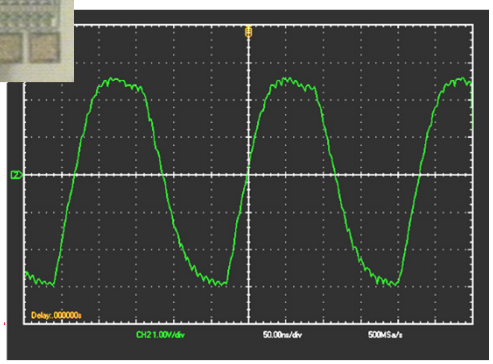
Design



Photo

The Ring Oscillator Works
Is It Working Correctly?

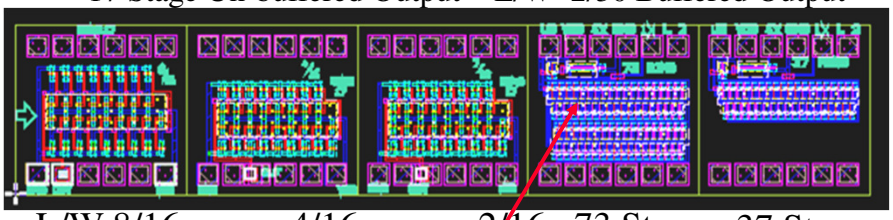
Electrical Test Results



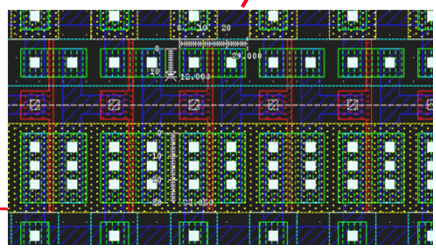
73 Stage
4X Buffer
L=2µm
5Volt Supply
Frequency = 4.37MHz
Period = T = 2 N td = 230ns
td = 1.58ns

RING OSCILLATOR LAYOUTS

17 Stage Un-buffered Output L/W=2/30 Buffered Output

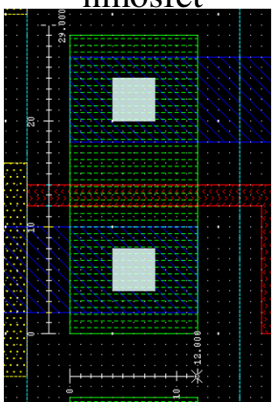


L/W 8/16 4/16 2/16 73 Stage 37 Stage

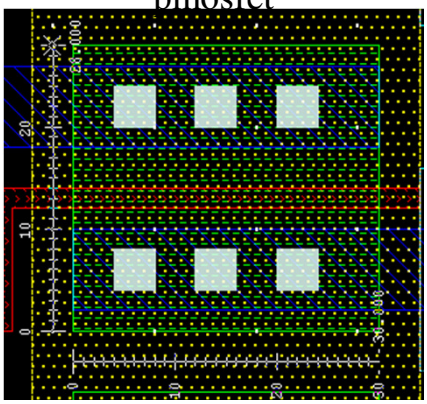


MOSFETS IN THE INVERTER OF 73 RING OSCILLATOR

nmosfet



pmosfet



73 Stage Ring Oscillator

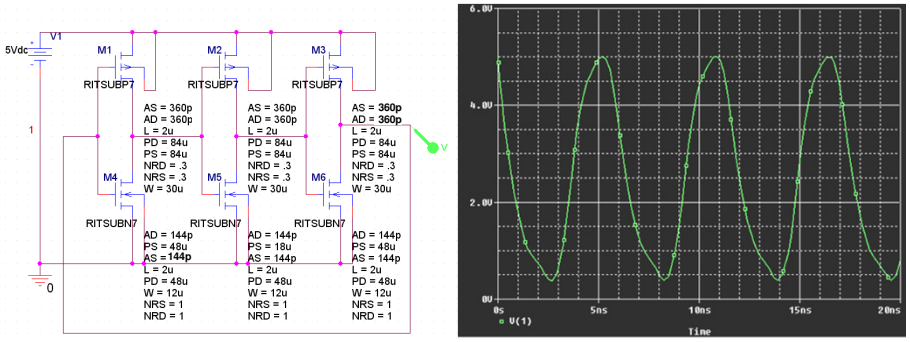
FIND DIMENSIONS OF THE TRANSISTORS

	NMOS	PMOS
L	2u	2u
W	12u	30u
AD	12ux12u=144p	12ux30u=360p
AS	12ux12u=144p	12ux30u=360p
PD	2x(12u+12u)=48u	2x(12u+30u)=84u
PS	2x(12u+12u)=48u	2x(12u+30u)=84u
NRS	1	0.3
NRD	1	0.3

73 Stage

Use Ctrl Click on all NMOS on OrCad Schematic
Use Ctrl Click on all PMOS on OrCad Schematic
Then Enter Dimensions

SIMULATED OUTPUT AT 5 VOLTS



Three Stage Ring Oscillator with Transistor Parameters for 73 Stage Ring Oscillator and Supply of 5 volts

Measured td = 1.580 nsec @ 5 V

td = T / 2N = 5.5nsec / 2 / 3

td = 0.92 nsec

REFERENCES

1. Dr Fuller's webpage on CMOS testing, http://people.rit.edu/lffeee/CMOS.htm
2. other