Double Exposure For MOSFET Polysilicon Gates

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MOTIVATION

- **Polysilicon gate size is currently set by mask dimensions**
  (Smallest gate length on sub-cmos factory mask = 1 μm)

- **Masks are expensive and time consuming to make**

- **ASML stepper has the ability to expose a wafer twice using the same mask and a small shift for the second exposure (double exposure)**

- **GOAL: To determine a method of double exposing a wafer in order to obtain smaller polysilicon gate lengths.**

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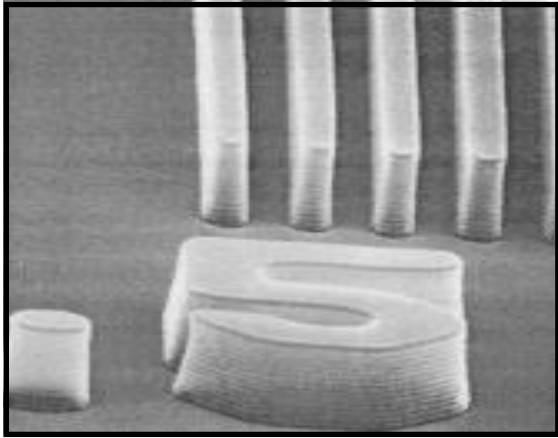
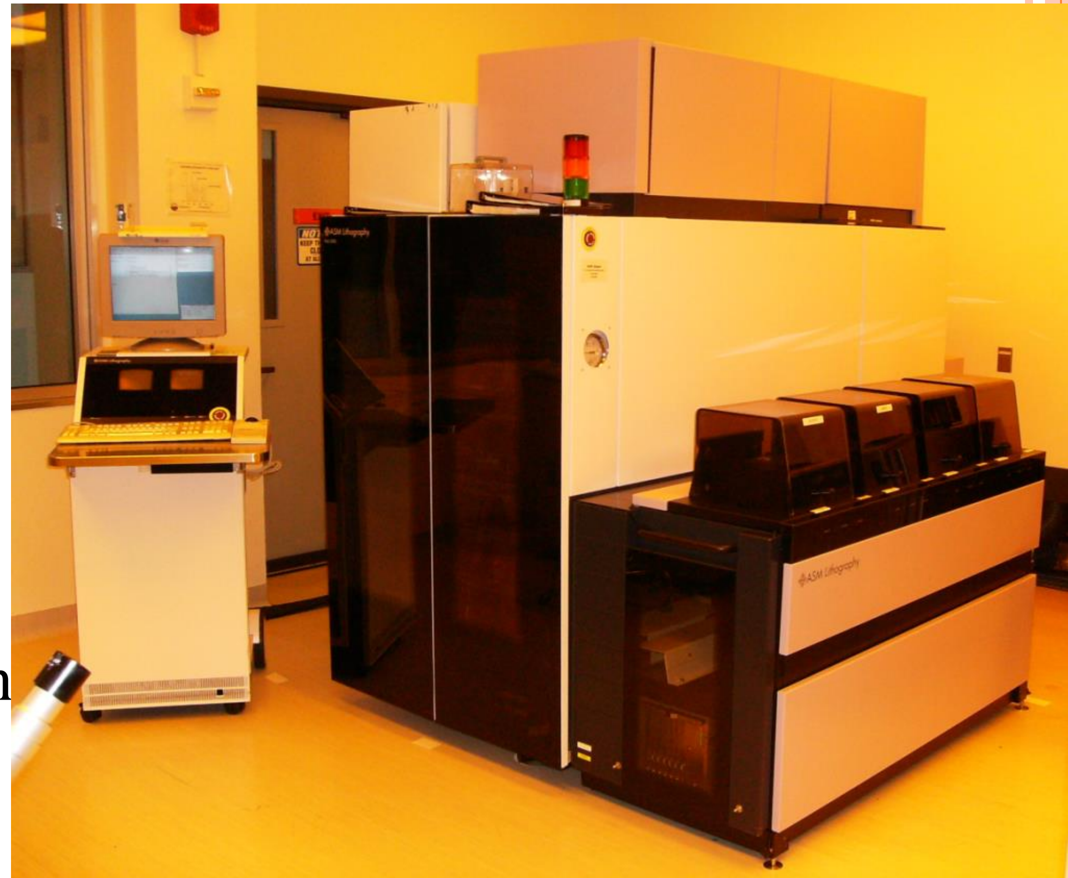
ASML 5500/200 Stepper



NA = 0.48 to 0.60 variable
σ= 0.35 to 0.85 variable
With Variable Kohler, or Variable Annular illumination
Resolution = K1 λ/NA
= ~ 0.35μm
for NA=0.6, σ =0.85
Depth of Focus = $k_2\ \lambda/(NA)^2$
= > 1.0 μm for NA = 0.6



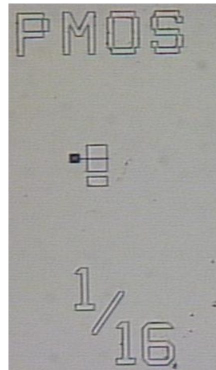
i-Line Stepper λ = 365 nm
22 x 27 mm Field Size

Process Flow

1. Coat, Expose with JG Active and Zero Level masks, and develop

2. Etch Silicon using Zero Etch recipe in the Drytek Quad and ash photoresist

3. Coat and Double Expose using JG Poly mask and develop



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Double Exposure on the ASML

Setting up the Double Exposure:

- Main Menu → Job Definition →Modify Job → Select "poly_double_expo"

- Wafer layout → Image distribution
  - In this window, type *, * in the x, y cell Index and hit the Enter key after each
  - Select image 2 (click the 3 bottom cells on the wafer layout)
  - Hit Delete
  - Put desired shift into Y (mm) and hit Enter and click Apply
  - Click Exit and continue the exposure as normal

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Shifts and Results

Shift Amount (µm)	Transistor Gate L/W (µm)	Measured Gate Length (µm)
1	2/8	1
1	1/8	0

Table 1: Result of a shift of 1 µm

Figure 1: Picture of a 2/8 µm transistor with a 1 µm shift, double exposed

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Shifts and Results (continued)

Shift Amount (µm)	Transistor Gate L/W (µm)	Measured Gate Length (µm)
0.5	1/16	0.5
0.5	2/16	1.5

Table 2: Result of a shift of 0.5 µm

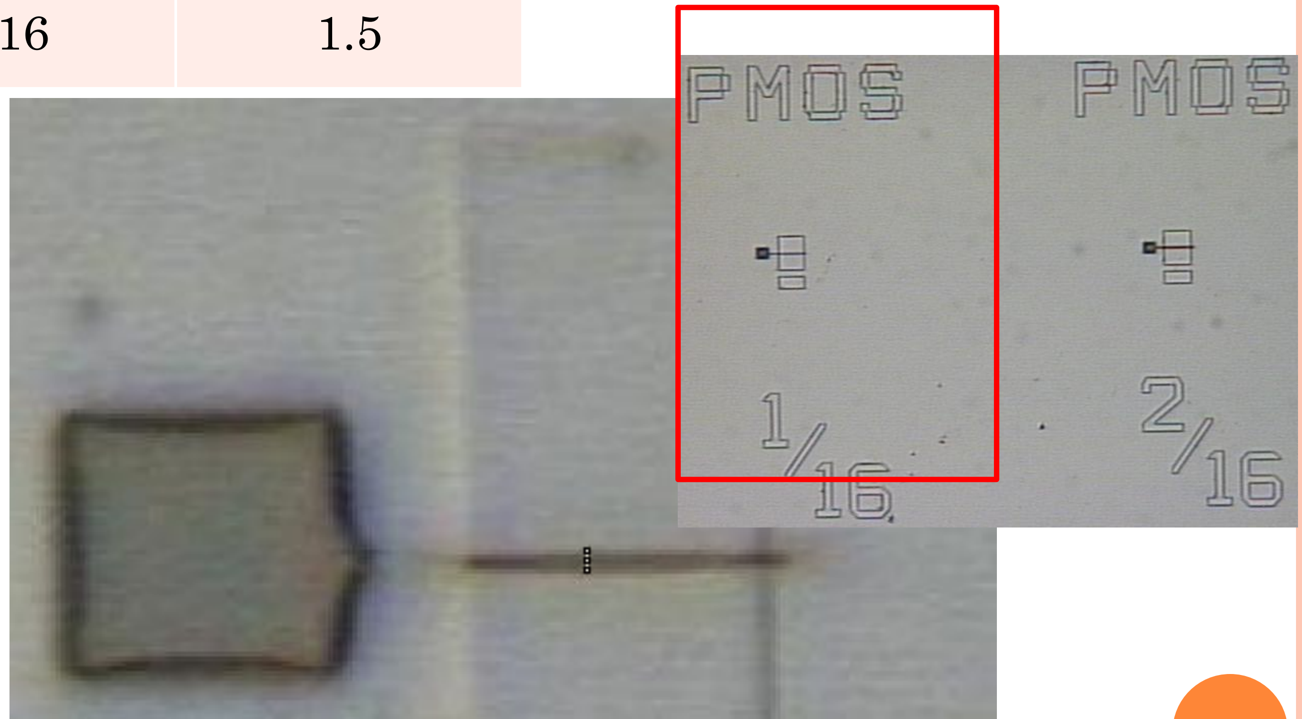

Figure 1: Screen picture of a 1/16 µm transistor with a 0.5 µm shift

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Shifts and Results (continued)

Exposure Matrix Dose Layout

100	125	150	175	200	225	250	275	300

To determine best exposure dose, exposure matrix was used with a center dose of 200 mJ/cm^2 and a step of 25 mJ/cm^2. Exposure dose layout on the wafer is shown.

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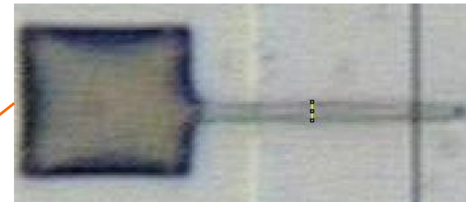
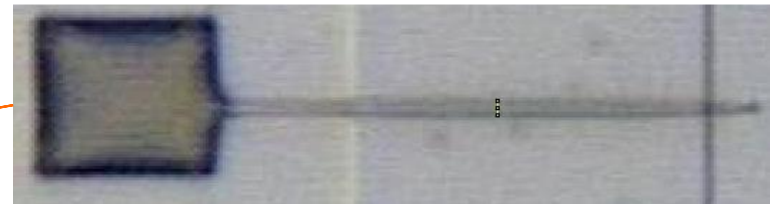
Shifts and Results (continued)

Table 3: Result of a shift of 0.75 µm at different exposure doses at 1/16 µm transistors in the same die row (except for the 125 mJ/cm^2 dose which was a 1/8 transistor)

Dose (mJ/cm^2)	Measured Gate Length (µm)
100	1
125	0.875
150	0.625
175	0.375
200 and up	unattached

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Summary

- Double exposure allows for smaller gate lengths.
- Size of an isolated photoresist line also depends on exposure dose.
- Height differences in the wafer surface affects photoresist size. (effect of different substrate reflection)
- Gate lengths below the resolution limit should be possible (i.e. <0.3um)

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