ELECTRICAL ENGINEERING
79 Lomb Memorial Dr. • Rochester, NY 14623-5603

EEEE 482 — Electronics II

Lab #0: Common-Emitter Amplifier Design

Overview

The objective of this lab is to design, simulate, and verify the performance of a common-emitter amplifier.

Background

A common-emitter amplifier is a widely used voltage amplifier due to its high gain and its reasonable tolerance to variations in transistor parameters. A discrete design for the common-emitter amplifier is shown in Figure 1. A voltage divider comprised of resistors R_1 and R_2 is used to set the DC bias voltage at the base of the BJT. (In an integrated circuit design, a current source would be used in place of some of the resistors shown in Figure 1; additionally, the current source could function as an active load.)

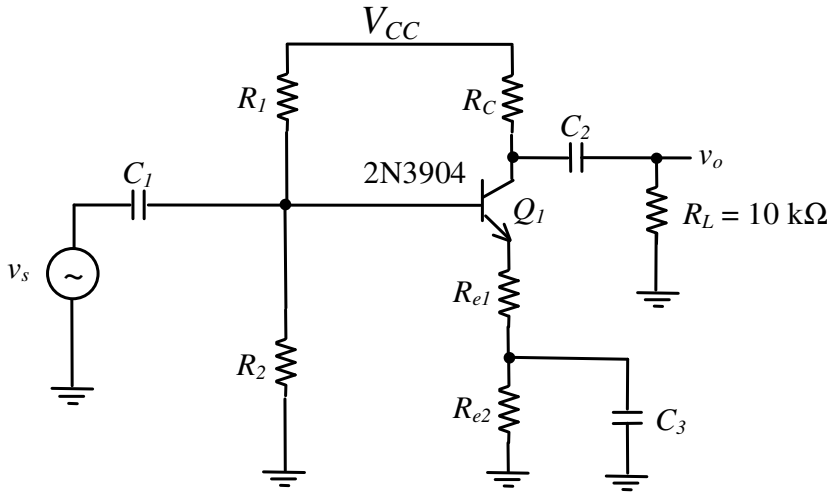

Figure 1. Common-Emitter Amplifier Schematic

Pre-Lab

Review the planned experiments and record relevant background information and equations that will be used for design of the common emitter amplifier. Design and simulate the amplifier to meet the design specifications you pick. A suggested design approach is given below.

Each student will randomly pick design specifications:

(1) a minimum value for *magnitude* of voltage gain: 20 22 24 26 28 30 [V/V] (± 10%); (note that the actual gain is negative in a common-emitter amplifier — *i.e.*, –20 V/V, etc.);

(2) a power supply voltage value: 14 15 16 [V].

The required minimum output swing specification (peak-to-peak amplitude) is 5 V less than your supply voltage. For example, if your supply voltage is 14 V, your output voltage must be able to swing ± 4.5 V, for a total peak-to-peak output swing of 14 – 5 = 9 V.

Each student must design the amplifier by selection of R_1, R_2, R_C, R_{e1} and R_{e2} using standard 5% tolerance resistor values (no parallel/series resistor combinations are allowed). Use 100 µF capacitors for C_1-C_3. The 2N3904 *npn* BJT can be found by searching for the Q2N3904 part. Load resistance is constant at 10 kΩ.

Assume V_{BE} = 0.7 V and $\boldsymbol{\beta}$ **=150,** and design for a DC collector current of about **6 mA**.

Sample design approach (you will need to refine to get to your final design, but this can provide a starting point)**:**

1. Set R_C to meet the output voltage swing specification (remember to consider both V_{CC} supply and transistor saturation).
2. Use the small-signal gain specification to determine R_{e1}. Note that the small-signal voltage gain includes the effect of R_L.
3. Choose $0.15*V_{CC} < V_B < 0.35*V_{CC}$.
4. Set $I_1=10*I_B$ → Calculate R_1
5. Set $I_2=9*I_B$ → Calculate R_2
6. Set ($R_{e1} + R_{e2}$) to get I_C.
7. Round calculated resistor values to standard 5% tolerance values (see Appendix H in Sedra & Smith), then **analyze the resulting design to verify that it meets the design specifications**. Note that the values given in Appendix H are just the significant digits. They can be multiplied by powers of 10 to get actual resistor values — *e.g.*, 560 Ω, 5.6 kΩ, 56 kΩ, etc.

Lab Exercise

Build the circuit of Figure 1 using your designed resistor values. Use a signal frequency of 10 kHz, and initial amplitude of 100 mV to measure your voltage gain. You will likely need to increase the amplitude of the input signal in order to confirm that you can accommodate the required amount of voltage swing at the output. For example, if you had a target *peak-to-peak* swing of 9 V at the output and a measured voltage gain magnitude of 30 V/V, you would need an input signal of 9/30 V = 300 mV *peak-to-peak*, or 150 mV amplitude, in order to drive the output with the target amount of swing.

- Summarize your design calculations, as well as the re-analysis of your design after rounding calculated resistor values to standard 5% tolerance values (see Appendix H in Sedra & Smith).
- Compare hardware results to simulated results. Discuss any discrepancies.