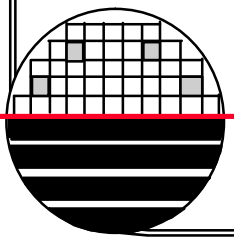
ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Factory Lithography Details, Stepper Jobs, Mask ID's, and Coat and Develop Recipes for SSI Track

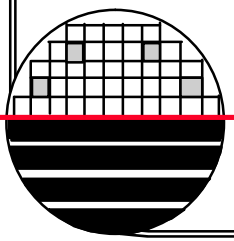
Dr. Lynn Fuller

http://www.rit.edu/~lffeee
Motorola Professor
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041
LFFEEE@rit.edu
http://www.microe.rit.edu



OUTLINE

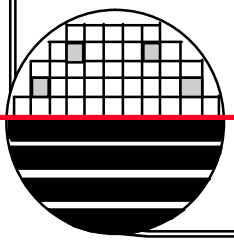
Introduction
Product/Process/Revision
Product/Mask ID's/Stepper Jobs
SSI
Canon
SMFL-CMOS Process, Lithography Details
SUB-CMOS Process, Lithography Details
ADV-CMOS Process, Lithography Details
SSI Recipes
Stepper Job, Process Files
References



INTRODUCTION

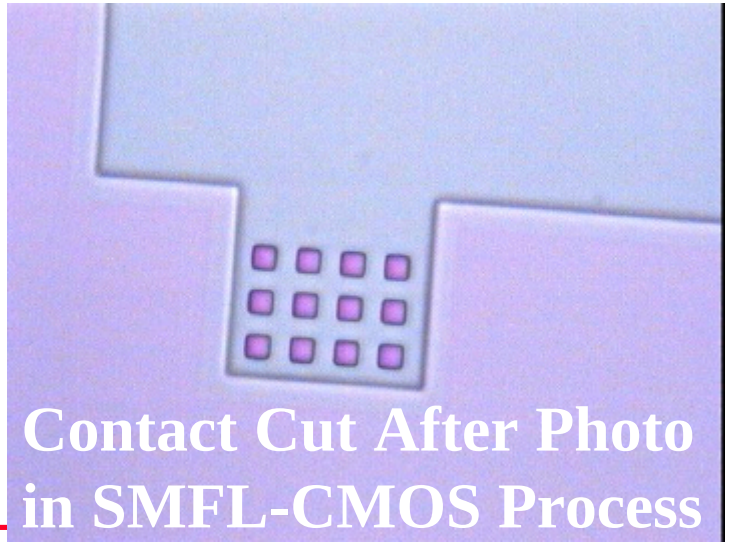
RIT has been CMOS processes since 1995. Today we run SUB-CMOS and ADV-CMOS processes for MicroE students to learn about new process technologies. We run the SMFL-CMOS process to fabricate circuits for students in EE Analog IC design courses. The p-well CMOS process has been discontinued.

RIT p-well CMOS (1995)	λ = 4 µm	Lmin = 8 µm
RIT Subµ CMOS (2000)	λ = 0.5 µm	Lmin = 1.0 µm
RIT Advanced CMOS (2003)	λ = 0.25 µm	Lmin = 0.5 µm
SMFL CMOS (2004)	λ = 1.0 µm	Lmin = 2.0 µm



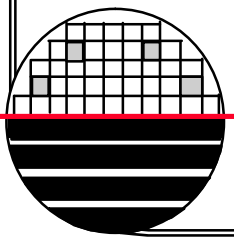
INTRODUCTION

Each of these processes have special requirements at each lithography level. The stepper job name changes with each level and with each product. The exposure dose, resist thickness, develop time and hard bake temperature changes with each level and each process. This document summarizes the information needed by factory operators for these lithography steps.



PRODUCT / PROCESS / REVISION

Product	Process	Rev
SPICE Test Chip	SMFL-CMOS	
DAC	SMFL-CMOS	
Mixed	SUB-CMOS	150
Test Chip	ADV-CMOS	150



MASK ID AND STEPPER JOB FOR SPICE TESTCHIP PRODUCT

Level	Step#	Level Name	Mask ID	Stepper Job
1	6	Nwell	STC031NWEL	FSASMFL2UM_nwell
2	18	Active	STC031ACT	FSASMFL2UM_act
3	21	Stop	STC031STOP	FSASMFL2UM_stop
4	30	Vt	STC031VT	FSASMFL2UM_vt
5	40	Poly	STC031POLY	FSASMFL2UM_poly
6	43	NDS	STC031NDS	FSASMFL2UM_nds
7	46	PDS	STC031PDS	FSASMFL2UM_pds
8	53	CC	STC031CC	FSASMFL2UM_cc
9	58	M1	STC031M1	FSASMFL2UM_m1
10	62	VIA	STC031VIA	FSASMFL2UM_via
11	66	M2	STC031M2	FSASMFL2UM_m2

MASK ID AND STEPPER JOB FOR DAC PRODUCT

Level	Step#	Level Name	Mask ID	Stepper Job
1	6	Nwell	DAC043NWELL	FSASMFL2UM_nwell
2	18	Active	DAC043ACT	FSASMFL2UM_act
3	21	Stop	DAC043STOP	FSASMFL2UM_stop
4	30	Vt	DAC043VT	FSASMFL2UM_vt
5	40	Poly	DAC043POLY	FSASMFL2UM_poly
6	43	NDS	DAC043NDS	FSASMFL2UM_nds
7	46	PDS	DAC043PDS	FSASMFL2UM_pds
8	53	CC	DAC043CC	FSASMFL2UM_cc
9	58	M1	DAC043M1	FSASMFL2UM_m1
10	62	VIA	DAC043VIA	FSASMFL2UM_via
11	66	M2	DAC043M2	FSASMFL2UM_m2

MASK ID AND STEPPER JOB FOR MIXED PRODUCT

Level	Step#	Level Name	Mask ID	Stepper Job
1	6	Nwell	MIX031NWEL	F031MIXED_nwell
2	19	Active	MIX031ACT	F031MIXED_act
3	22	Stop	MIX031STOP	F031MIXED_stop
4	30	pmosVt	MIX031VT	F031MIXED_vt
5	40	Poly	MIX031POLY	F031MIXED_poly
6	43	NLDD	MIX031NLDD	F031MIXED_lddn
7	46	PLDD	MIX031PLDD	F031MIXED_lddp
8	53	N+DS	MIX031NDS	F031MIXED_nds
9	56	P+DS	MIX031PDS	F031MIXED_pds
10	62	CC	MIX031CC	F031MIXED_cc
11	67	Metal 1	MIX031MTL	F031MIXED_metal

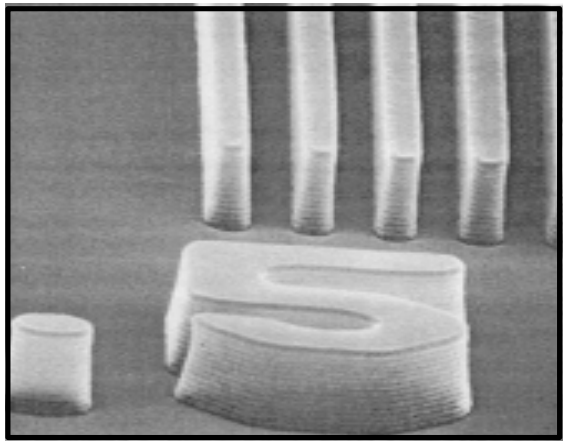
MASK ID AND STEPPER JOB FOR ADV CMOS TESTCHIP PRODUCT

Level	Step#	Level Name	Mask ID	Stepper Job
1	6	STI	ADV023STI	F023ADVCMOS_STI
2	11	NWELL	ADV023NWELL	F023ADVCMOS_nwell
3	14	PWELL	ADV023PWELL	F023ADVCMOS_pwell
4	24	VTN	ADV023VTN	F023ADVCMOS_vtn
5	27	VTP	ADV023VTP	F023ADVCMOS_vtp
6	35	POLY	ADV023POLY	F023ADVCMOS_poly
7	40	PLDD	ADV023PLDD	F023ADVCMOS_pldd
8	43	NLDD	ADV023NLDD	F023ADVCMOS_nldd
9	49	N+DS	ADV023NDS	F023ADVCMOS_nds
10	52	P+DS	ADV023PDS	F023ADVCMOS_pds
11	63	CC	ADV023CC	F023ADVCMOS_cc
12	68	METAL	ADV023M1	F023ADVCMOS_mtl

SSI COAT AND DEVELOP TRACK FOR 6” WAFERS

Use Recipe: Coat.rcp, CoatMTL.rcp,
and Develop.rcp DevFac.rcp, DevCC.rcp or DevMtl.rcp

CANON FPA-2000 i1 STEPPER



i-Line Stepper $\lambda = 365$ nm

NA = 0.52, $\sigma = 0.6$

Resolution = $0.7\ \lambda$ / NA = ~0.5 µm

20 x 20 mm Field Size

Depth of Focus = $k_2\ \lambda/(NA)^2$

= 0.8 µm

LITHOGRAPHY FOR SMFL-CMOS PROCESS

Lvl #	Level Name	Coat Recipe	Spin RPM	Xpr µm	Dose mj/cm^2	Dev Recipe	Dev Time	Hard Bake
1	Nwell	coat	3250	1.0	160	develop	50s	140C/1min
2	Active	coat	3250	1.0	185	devfac	120s	140C/1min
3	Stop	coat	3250	1.0	185	devfac	120s	140C/1min
4	Vt	coat	3250	1.0	185	devfac	120s	140C/1min
5	Poly	coat	3250	1.0	160	develop	50s	140C/1min
6	NDS	coat	3250	1.0	160	develop	50s	140C/1min
7	PDS	coat	3250	1.0	160	develop	50s	140C/1min
8	CC	coat	3250	1.0	260	devCC	200s	140C/1min
9	M1	coatmtl	2000	1.3	160	devmtl	68s	140C/2min
10	VIA	coat	3250	1.0	260	devCC	200s	140C/1min
11	M2	coatmtl	2000	1.3	160	devmtl	68s	140C/2min

LITHOGRAPHY FOR SUB-CMOS 150 PROCESS

Lvl #	Level Name	Coat Recipe	Spin RPM	Xpr µm	Dose mj/cm^2	Dev Recipe	Dev Time	Hard Bake
1	Nwell	coat	160	1.0	160	develop	50s	140C/1min
2	Active	coat	160	1.0	185	devfac	120s	140C/1min
3	Stop	coat	185	1.0	185	devfac	120s	140C/1min
4	pmosVt	coat	160	1.0	160	devfac	120s	140C/1min
5	Poly	coat	160	1.0	160	develop	50s	140C/1min
6	NLDD	coat	160	1.0	160	develop	50s	140C/1min
7	PLDD	coat	150	1.0	160	develop	50s	140C/1min
8	N+DS	coat	160	1.0	160	develop	50s	140C/1min
9	P+DS	coat	160	1.0	160	develop	50s	140C/1min
10	CC	coat	260	1.0	260	devCC	200s	140C/1min
11	Metal 1	coatmtl	160	1.3	160	devmtl	68s	140C/2min

LITHOGRAPHY FOR ADV-CMOS 150 PROCESS

Lvl #	Level Name	Coat Recipe	Spin RPM	Xpr µm	Dose mj/cm^2	Dev Recipe	Dev Time	Hard Bake
1	STI	coat	3250	1.0	160	develop	50s	140C/1min
2	NWELL	coatmtl	2000	1.3	160	devmtl	68s	140C/2min
3	PWELL	coatmtl	2000	1.3	160	devmtl	68s	140C/2min
4	VTN	coat	3250	1.0	160	devfac	120s	140C/1min
5	VTP	coat	3250	1.0	160	devfac	120s	140C/1min
6	POLY	coat	3250	1.0	160	develop	50s	140C/1min
7	PLDD	coat	3250	1.0	160	develop	50s	140C/1min
8	NLDD	coat	3250	1.0	160	develop	50s	140C/1min
9	N+DS	coat	3250	1.0	160	develop	50s	140C/1min
10	P+DS	coat	3250	1.0	160	develop	50s	140C/1min
11	CC	coat	3250	1.0	260	devCC	200s	140C/1min
12	METAL	coatmtl	2000	1.3	160	devmtl	68s	140C/2min

COAT.RCP

COAT.RCP

DEHYDRATE BAKE/
HMDS PRIMING

HMDS Vapor
Prime
140 °C, 60 sec.

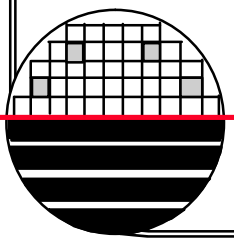
SPIN COAT

OIR 620-10
Resist
3250 rpm, 30 sec.

SOFT BAKE

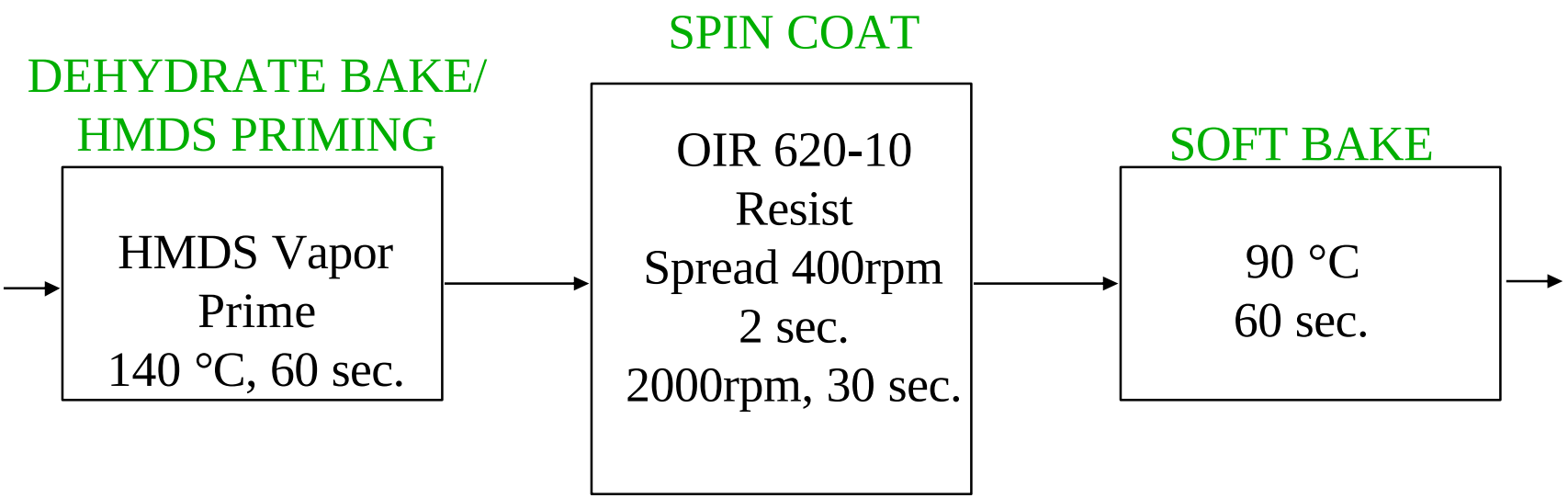
90 °C
60 sec.

Thickness of 10,000 Å



COATMTL.RCP

COATMTL.RCP



Thickness of 13,127 Å

DEVELOP.RCP

DEVELOP.RCP

DEVFAC.RCP

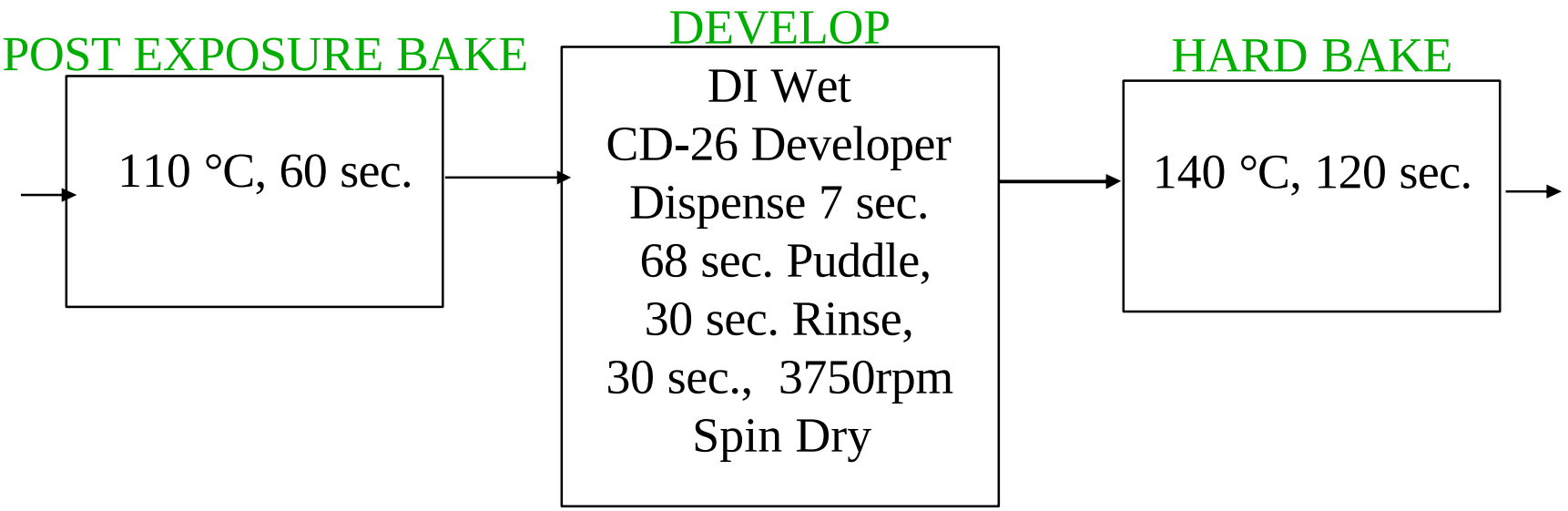
DEVFAC.RCP

DEVCC.RCP

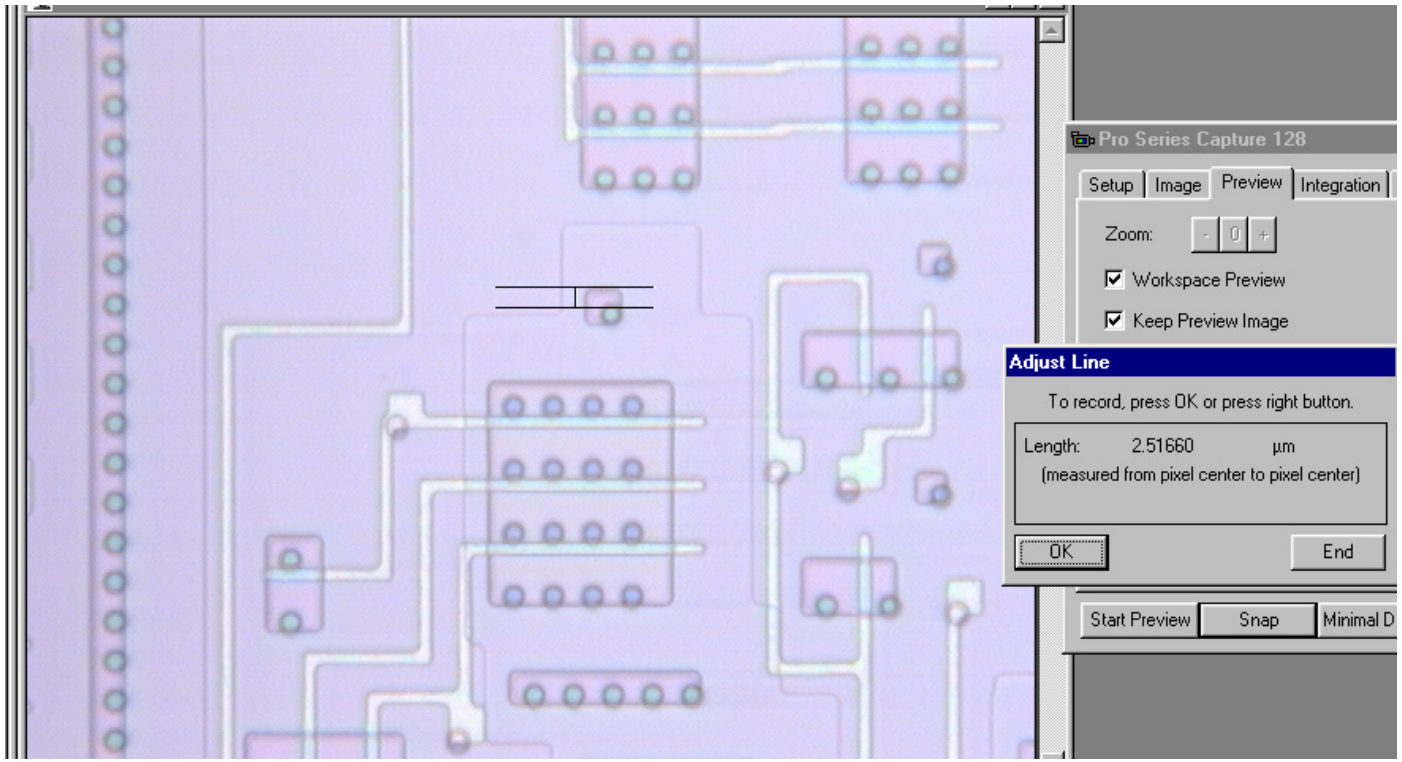
DEVCC.RCP

DEVMTL.RCP

DEVMTL.RCP

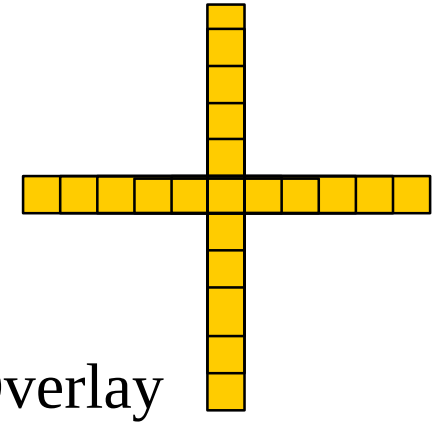


OVERLAY PROBLEM

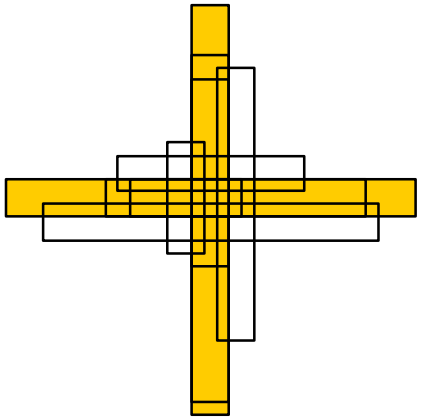


What is wrong here? Although it looks like the contact cut level is misaligned actually it is perfect. The active is misaligned high and too far left. Poly is high and too far right. All critical layers (active, poly, cc and metal) need to have good alignment relative to well in order to have good alignment relative to each other.

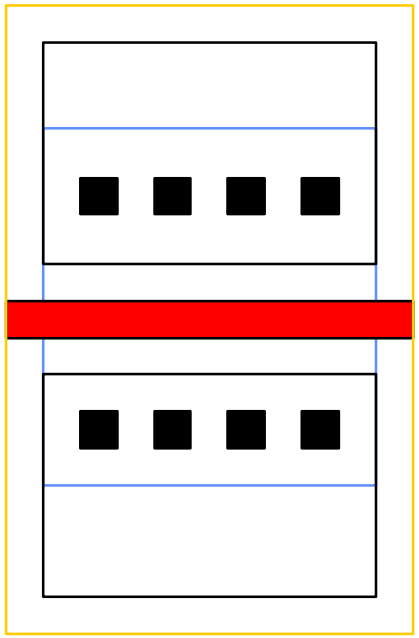
COMPOUND OVERLAY

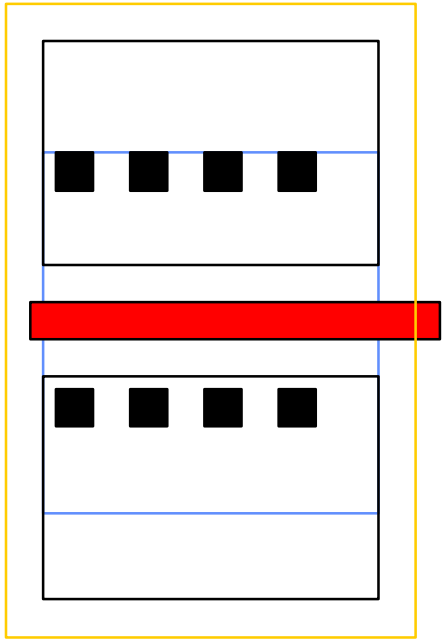


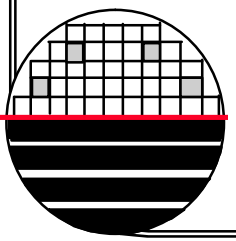
Perfect Overlay



Compound Overlay Errors



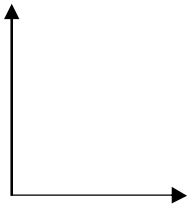




MEASURING OVERLAY ERROR

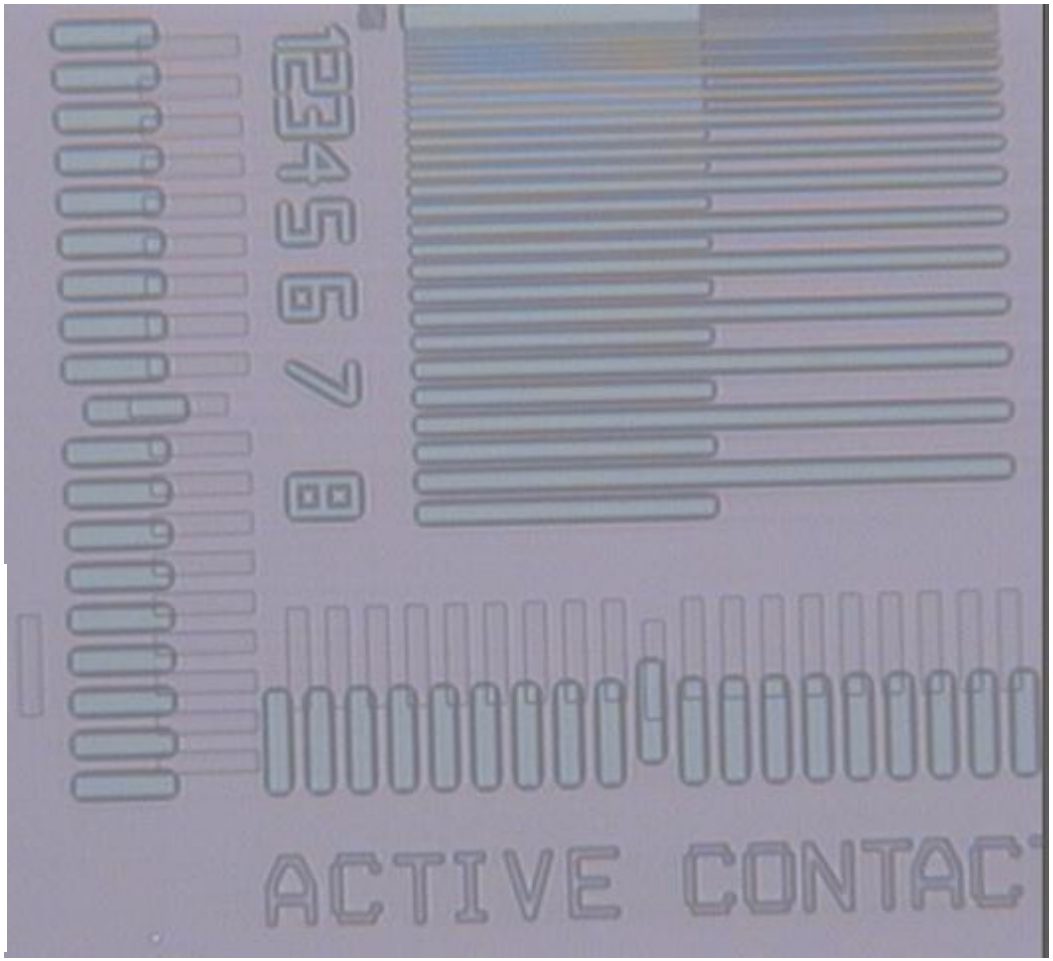
If second pattern needs to shift up and to the right the alignment offsets need to be negative values

-Y



-X

This shows alignment of contact to well. Contact needs to move 1µm up and 2 µm to the right. Thus the offsets should be set to Y= -1 and X= -2

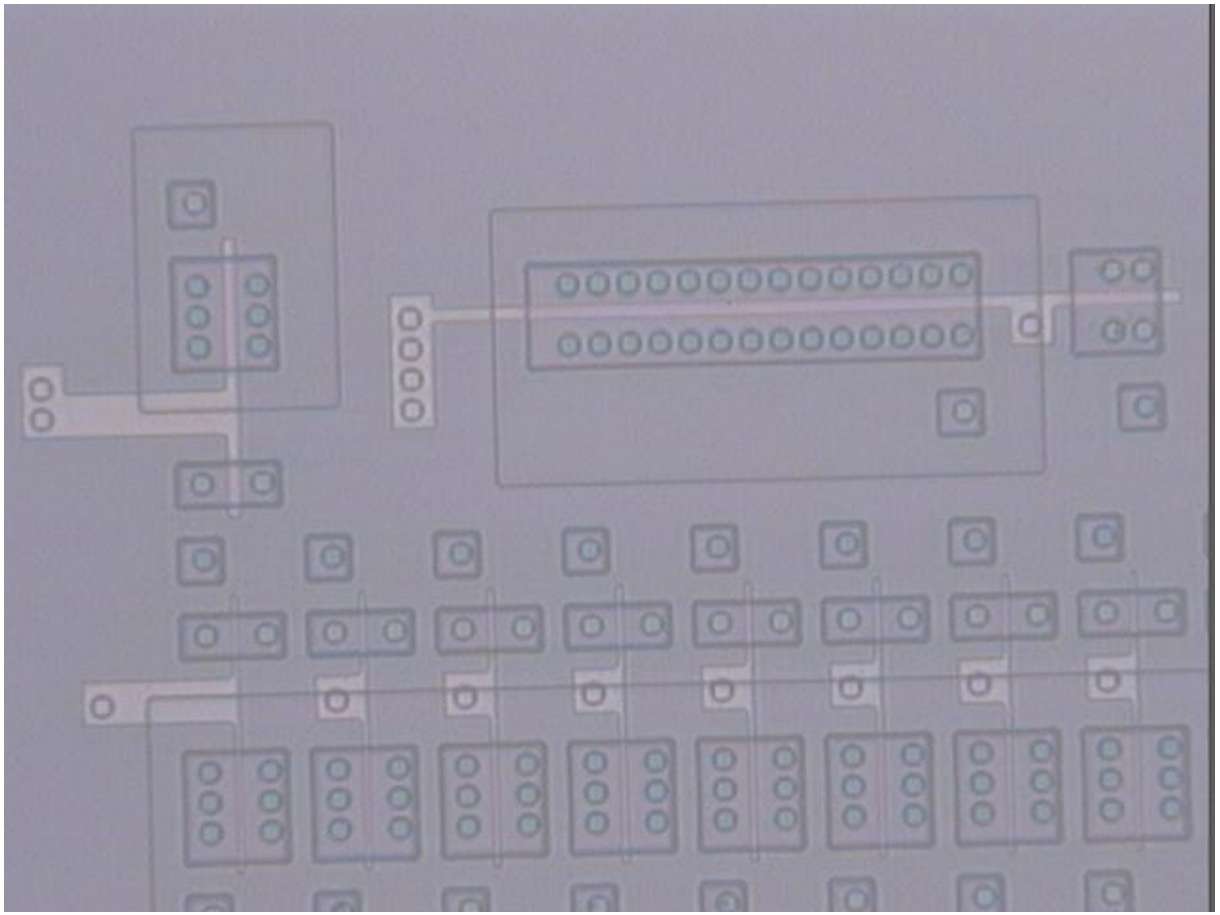


One Micron Overlay Verniers

ENTERING OFFSETS TO CORRECT OVERLAY

Alignment offsets can be entered at the Parameter Check screen. This will give a temporary shift only for the current stepper run. To introduce a permanent shift, edit the process file (ED P) and go to page /12, line 1, then enter x and y alignment offsets.

AFTER ENTERING OFFSETS AND REWORK



This is better. It shows active too far left by ~1µm, contact and poly are perfect. Looks good enough to work.

REFERENCES

1. “Silicon Processing”, Stanley Wolf
2. EMCR650 lecture notes on line at http://www.rit.edu/~lffeee
3. Microlithography, Sheats and Smith