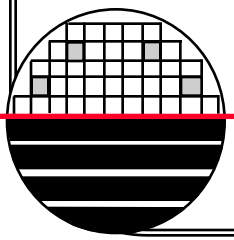
ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

High Speed Logic Circuits

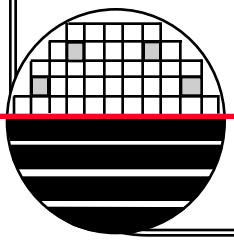
Dr. Lynn Fuller

Webpage: http://people.rit.edu/lffeee
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041
Email: Lynn.Fuller@rit.edu
Department webpage: http://www.microe.rit.edu



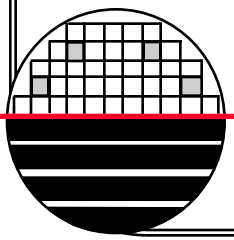
ADOBE PRESENTER

This PowerPoint module has been published using Adobe Presenter. Please click on the Notes tab in the left panel to read the instructors comments for each slide. Manually advance the slide by clicking on the play arrow or pressing the page down key.



OUTLINE

Introduction
Definitions
MOSFET Internal Capacitances
Inverter Rise and Fall times and Gate Delay
Sizing Gates for Equal Rise and Fall Times
Fan In and Fan Out Considerations
Astable Multivibrator
Two Phase Non-Overlapping Clocks
Buffers
Tristate I/O Pads with ESD protection
Power Dissipation
Energy and Delay
References
Homework



INTRODUCTION

High speed digital electronics depends on technology, design, and architecture among other things. Technology includes Strained Silicon, Silicon on Insulator, and Metal Gate, The transistors themselves can be made of different materials such as Silicon, Germanium, or Gallium Arsenide, or can be FINFETS instead of planner MOSFETS. Design includes transistor size, gate design, interconnect methodology and more. There are many design goals other than high speed such as low power, compact size, high yield (redundancy) and more. Everything is complicated by the 100's of millions of transistors in todays complicated microchips.

Because the mobility of carriers in n-type silicon is always higher than the mobility in p-type silicon the pull up transistor drive current (pmos) in an inverter will be less than the pull down transistor drive current (nmos) for transistors of equal length and width. By increasing the width the drive current can be increased.

DEFINITIONS

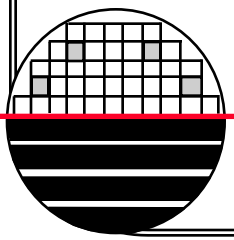
Rise Time – time for Vout of a gate to go from 10% to 90%

Fall Time – time for Vout of a gate to go from 90% to 10%

Propagation Delay or **Gate Delay** – (td) average time it takes for the output of a gate to get to switch using the 50% point of Vout high – Vout low. Also td = ½ (td_{LTH} + Td_{HTL})

Low to High Delay (td_{LTH}) – time for output to go from low to the 50% point.

High to Low Delay (td_{HTL}) – time for output to go from high to the 50% point.



RISE TIME, FALL TIME AND PROPAGATION DELAY

The system speed is determined by many factors but the basic parameter that determines the speed of the system is the individual gate propagation delay, td. The propagation delay is often used as a figure of merit to compare different technologies. For example in 1997 IBM reported their measured ring oscillator propagation delay of 9.5ps the fastest reported to date for CMOS at room temperature.

The definition of propagation is the average of td_{LTH} and the td_{HTL} for the output of a gate (typically an inverter).

Thus: $td = \frac{1}{2}(t_{HTL} + t_{HTL})$

These times are so fast they are hard to measure so td is typically extracted from the measured period of a ring oscillator. A ring oscillator is an odd number of inverters (N) in series with the output connected back to the input, which will oscillate with period T.

thus: $td = T/2N$

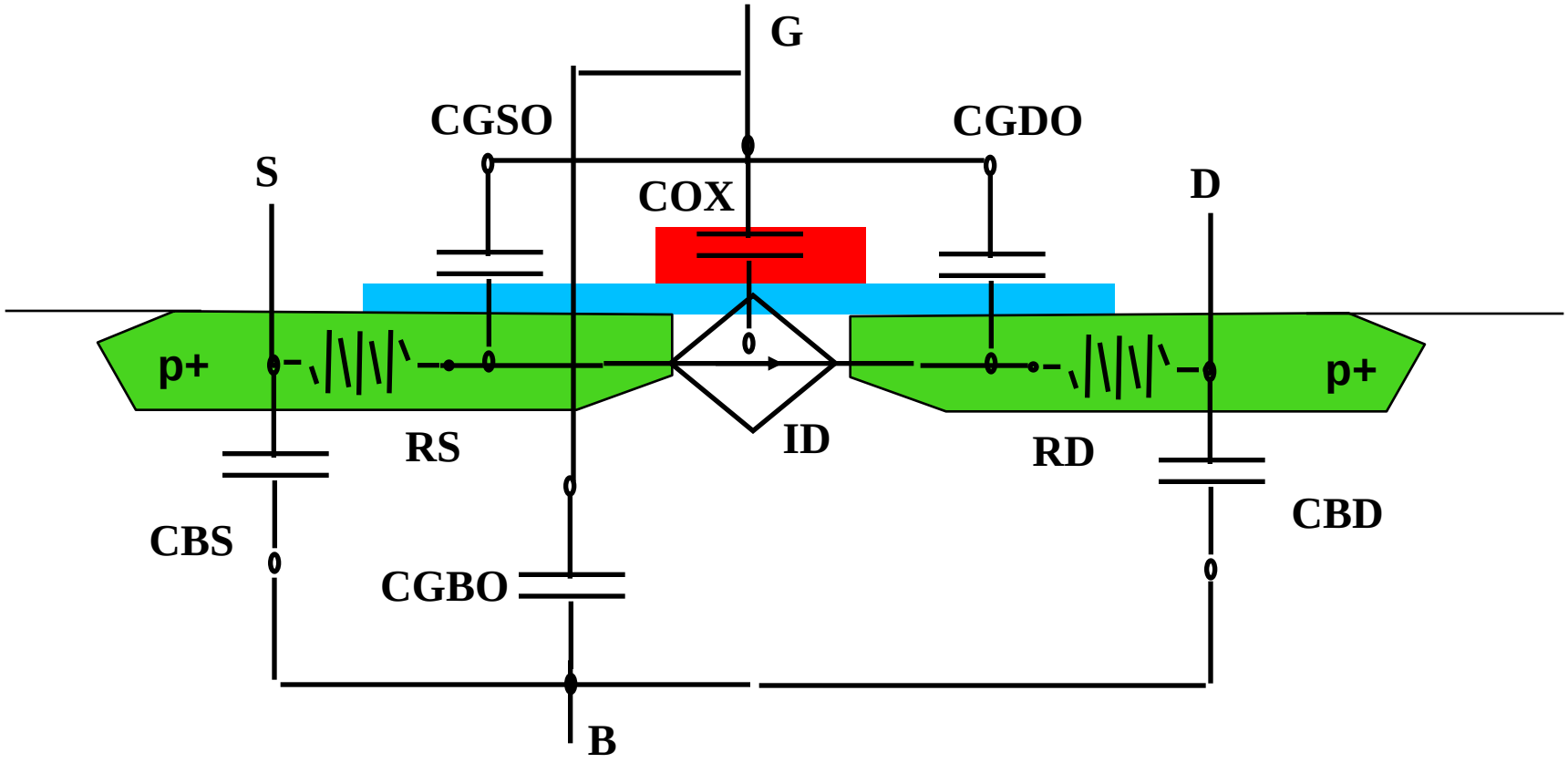
MOSFET INTERNAL CAPACITANCES

The internal capacitors for a MOSFET are associated with the gate-to-channel, Gate overlap with the Drain, Source and substrate, and the source and drain junction capacitance to the substrate. The values of these capacitors depend on the length, L, width, W, Overlap in the length and width directions, Area and perimeter of the drain and source. Further, these capacitors change with voltage (with junction space charge width) and with the circuit topology including voltage gain Miller capacitance. The models are complex however this complexity is imbedded in the more advanced SPICE models used for simulation.

We will attempt to get values for these capacitances, making simplifying approximations and assumptions.

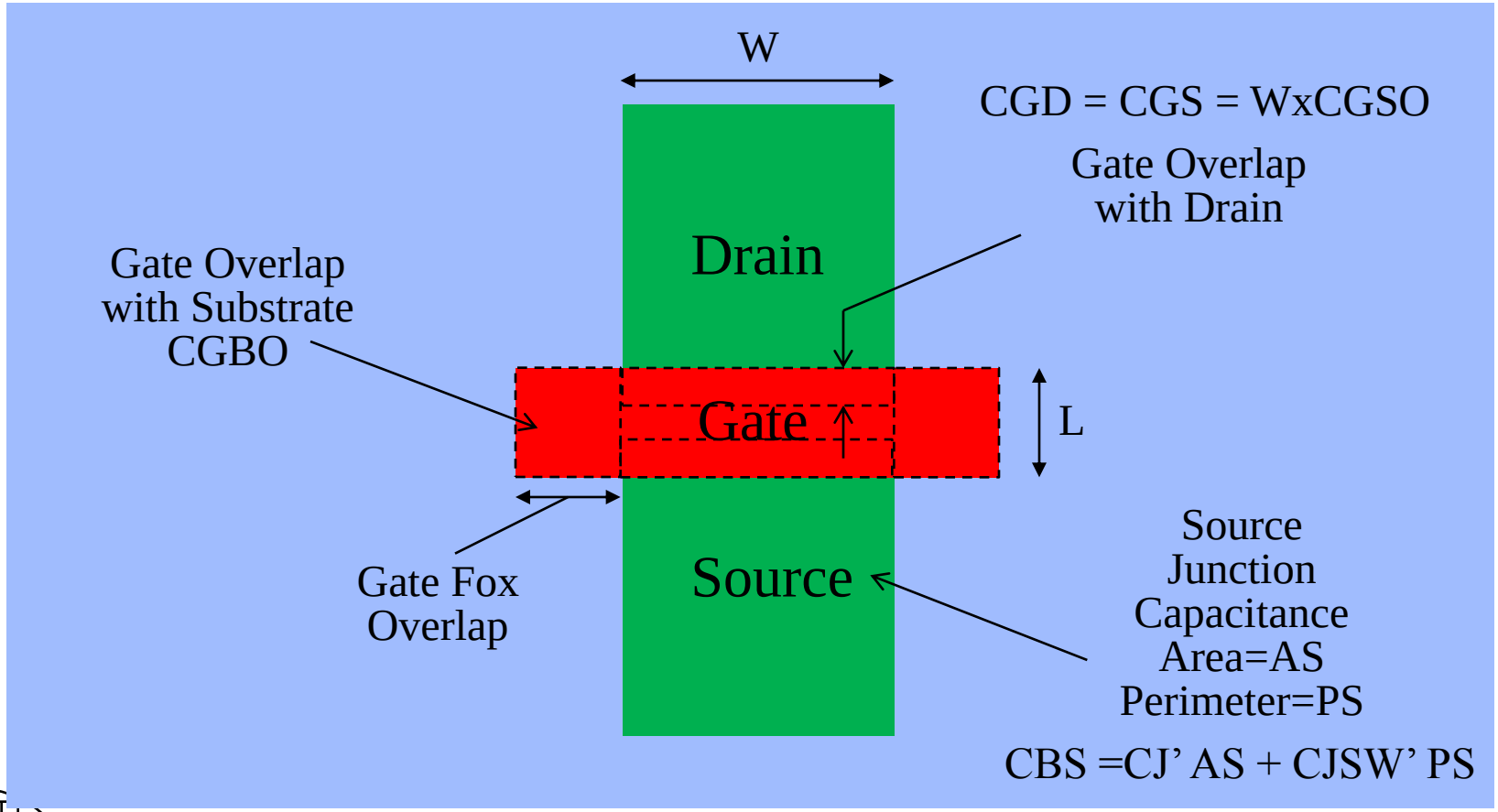
In addition we need to include the capacitance associated with the interconnect wiring. Today's complex chips have 1000's of meters of wiring.

SPICE LEVEL-1 MOSFET MODEL

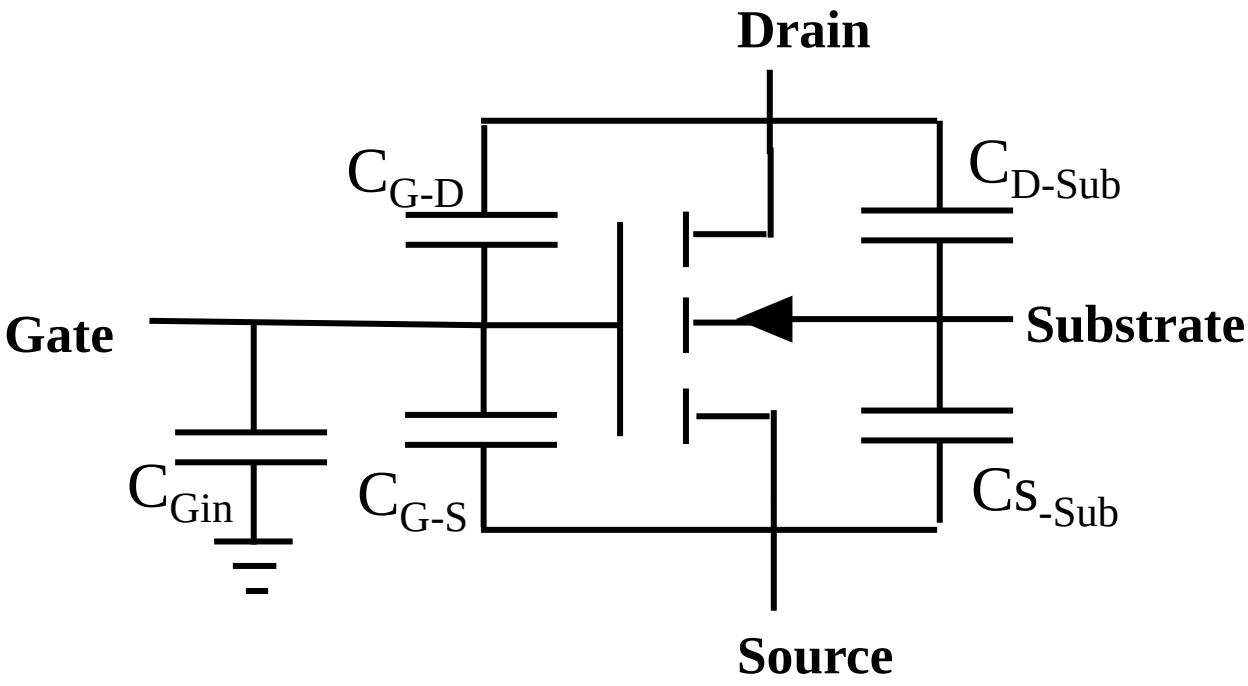


ID is a dependent current source. These C and R values are calculated separately in SPICE and multiplied by Ad, As, Pd, Ps, Nd, Ns, L, W etc. for a given MOSFET. CGBO is small compared to the other capacitors

TRANSISTOR LAYOUT SHOWING CAPACITANCE



MOSFET SHOWING CAPACITANCE



SPICE LEVEL-1 PARAMETERS FOR MOSFET

$$Cox' = \varepsilon r \varepsilon o / TOX = 3.9 \varepsilon o / TOX$$

where $\varepsilon r = 3.9$ for Oxide

$\varepsilon o = 8.85E\text{-}14$ F/cm

TOX= gate oxide thickness

CGSO is the gate-to-source overlap capacitance (per meter channel width)

CGSO = Cox' (mask overlap in L direction + LD) F/m

CGDO is the gate-to-drain overlap capacitance (per meter channel width)

CGDO = Cox' (mask overlap in L direction + LD) F/m

CGBO is the gate-to-bulk overlap capacitance (per meter of overlap)

$CGBO = C_{field\_oxide}$ * mask overlap in W direction F/m

$C_{field\_oxide} = \varepsilon r \varepsilon o / XFieldOX$

SPICE LEVEL-1 PARAMETERS FOR MOSFET

CBD zero bias bulk to drain junction capacitance

CBD = CJ' AD + CJSW' PD

CBS zero bias bulk to source junction capacitance

CBS = CJ' AS + CJSW' PS

CJ is the zero bias bulk junction bottom capacitance per square meter of junction area. CJ = $\varepsilon_r\varepsilon_o$ / W where W is width of space charge layer.

$$CJ = \varepsilon_r\varepsilon_o / [2\varepsilon_r\varepsilon_o (\Psi o - VA)/qNsub]^{-m} \quad F/m2$$

where ε_r = 11.7 F/cm for Silicon

Ψo = PB = (KT/q) ln (NSUB/ni) + 0.56

m = junction grading coefficient = 0.5

MJ is the junction grading coefficient = 0.5

CJSW is the zero bias bulk junction sidewall capacitance per meter of junction perimeter. CJSW = CJ XJ

MJSW is the junction grading coefficient = 0.5

SPICE LEVEL-1 PARAMETERS FOR MOSFET (cont.)

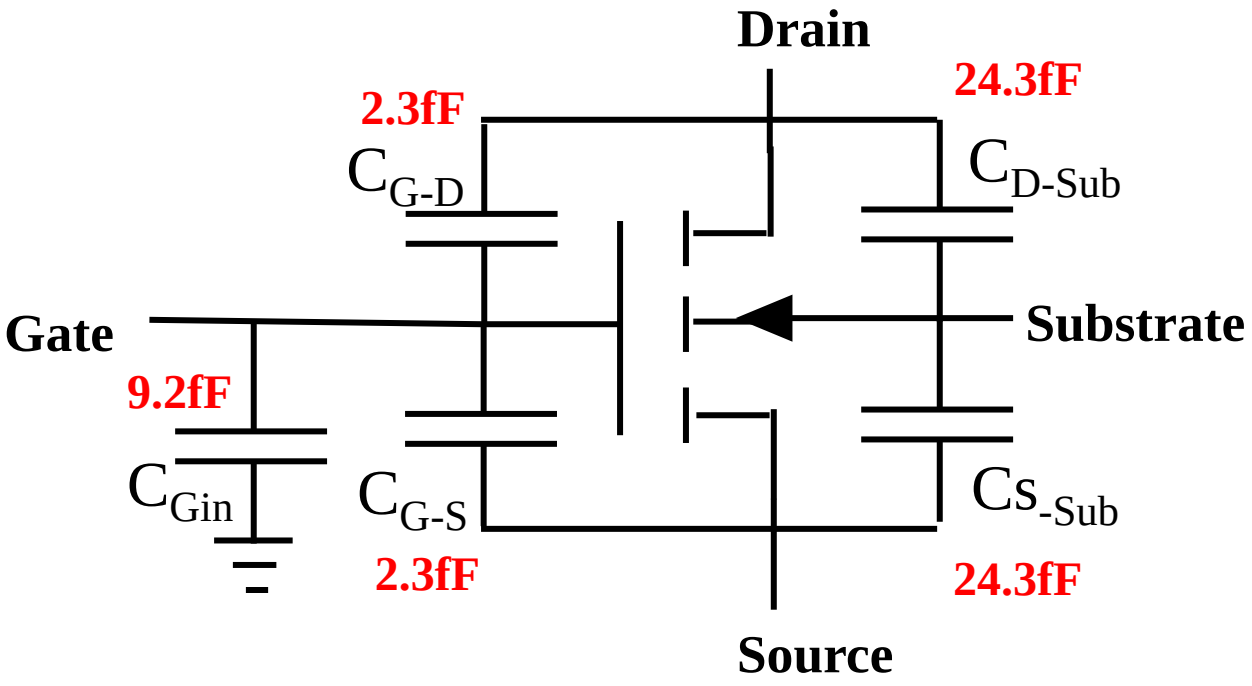
For ~1um Technology L= 1um and W=5um

Xox=150Å Xj=1um VDD=5 V AD=25um2
Field Fox=6500Å VTO =1 V PD=20um
Nsub=3E16cm-3 Gate Fox Overlap=2um
N+D/S = 1E19 cm-3 Gate to Drain Overlap LD=0.1um

Cox'= eoer/Xox=8.85e-14(F/cm)x3.9/150E-8cm = 2.30E-7 F/cm2
CGin=Cox' Area=2.30E-7(F/cm2)x2umx5um = 9.2 fF
Cfield'= eoer/Fox = 8.85e-13(F/cm)x3.9/6500E-8cm=5.31E-9F/cm2
CG-Sub=Cfield'xArea=2x5.31E-9x2umx1um=0.21fF
CGDO=Cox'x LD=2 x 2.30E-7 x 0.1um=4.6e-12F/cm
CGD=CGDOxW=4.6E-12 x 5um=2.3fF
Cj'=eoer/Wsc=5.41E-8F/cm2
CJ=Cj'x Area=5.41E-8(F/cm2)x25um2=13.5fF
Cjsw'=eoer Xj/Wsc=5.41E-12 F/cm
CJ2=Cjsw'x PD = 5.41E-12 x 20um=10.8fF

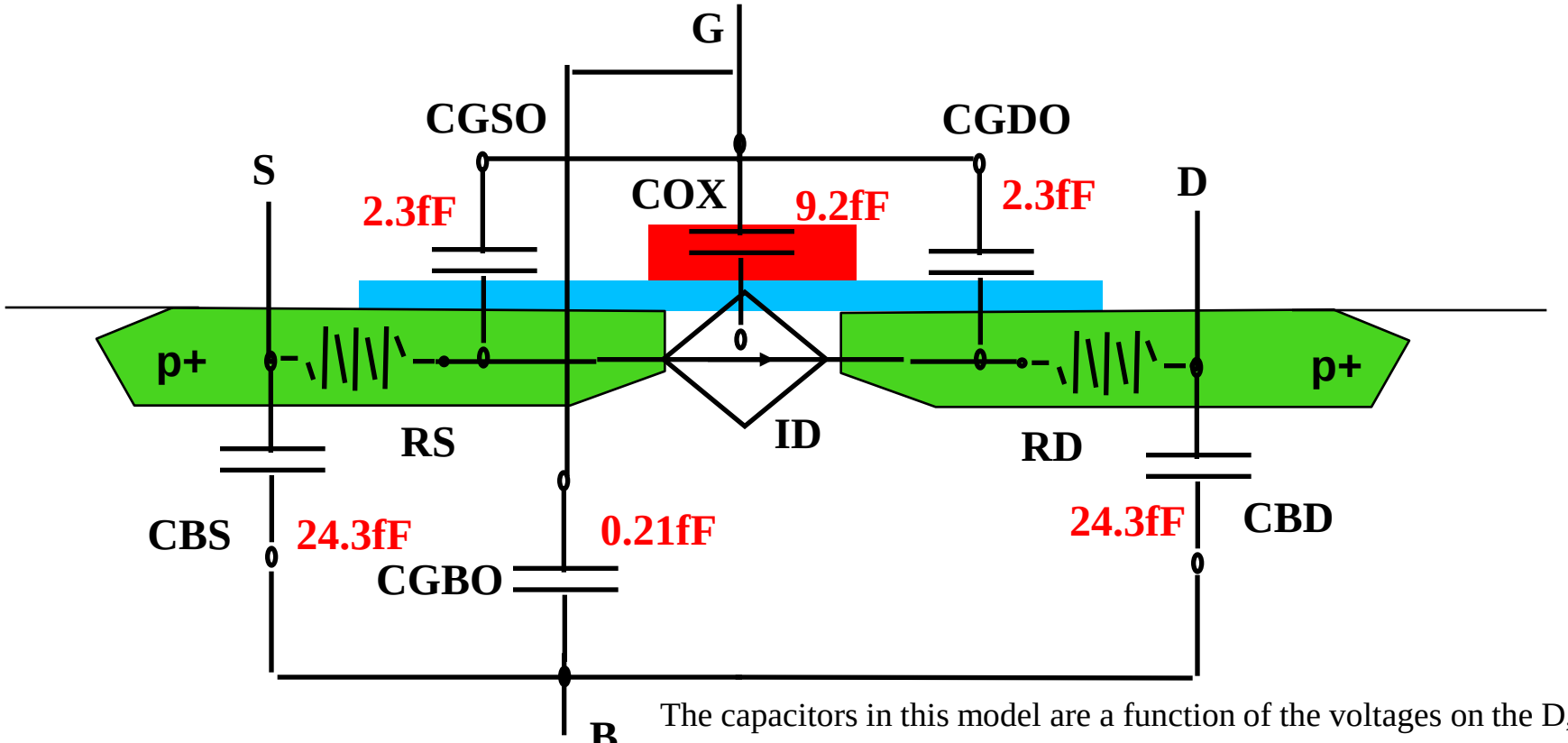
} CBD

MOSFET SHOWING CAPACITANCE



$$CG = C_{Gin} + C_{G-S} + C_{G-D}(1-Av)$$
$$= 9.2fF + 2.3fF + 2.3fF \times (1- -5) = \sim 25.3fF$$

SPICE LEVEL-1 MOSFET MODEL



The capacitors in this model are a function of the voltages on the D, G, S and B terminals. CGDO is across a voltage gain in many circuits so that capacitor will appear to be larger do to Miller effect.

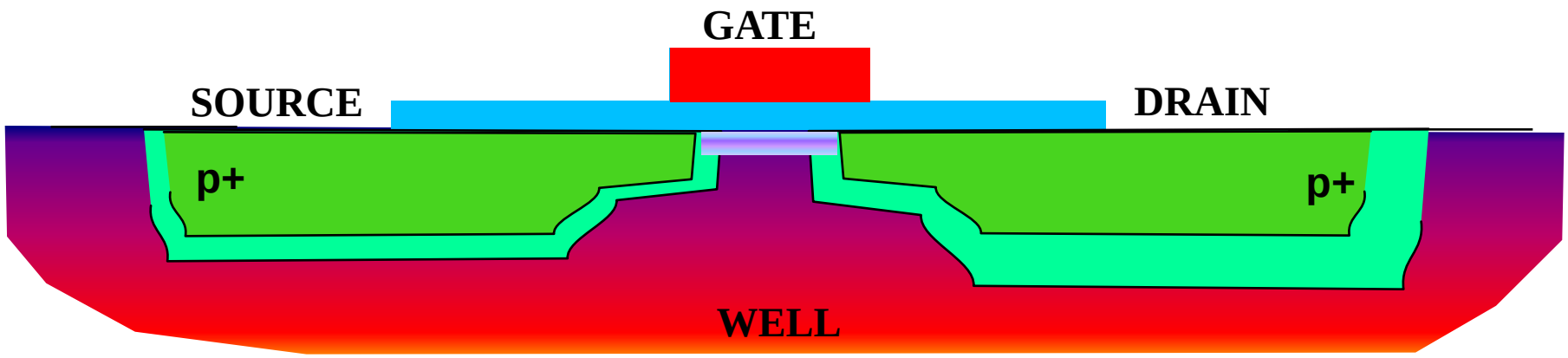
$$CG = C_{Gin} + C_{G\text{-}S} + C_{G\text{-}D}\,(1\text{-}Av)$$
$$= 9.2fF + 2.3fF + 2.3fF \times (1 - -5) = \sim 25.3fF$$

GATE TO DRAIN OVERLAP, JUNCTION CAPACITANCE

Since the Drain and Source Junction Capacitance is large we want to keep the area of the Drain and Source as small as we can. The doping concentration on both sides of the junction determine the space charge layer width and ultimately the junction capacitance. We can minimize that by careful well design. Today's wells are shallow and are not uniformly doped. Retrograde wells provide higher doping near but slightly below the surface to reduce punch through. The deeper parts of the drain and source contact area are to provide robust contacts. If these intersect the wells where the wells are lighter doped the junction capacitance will be lower.

The Gate to Drain overlap capacitance is multiplied by the Miller effect so it is one of the larger capacitances. To reduce this overlap the Poly is oxidized after being etched (Poly ReOx) before the Drain and Source is ion implanted. This reduces the overlap because the ion implant of the D/S is placed further away from the gate.

GATE TO DRAIN OVERLAP, JUNCTION CAPACITANCE



The Gate to Drain overlap capacitance is reduced if the Poly is oxidized before the Drain and Source is ion implanted.

CMOS INVERTER SHOWING CAPACITANCE

During switching one transistor is off while the other is in saturation. The self capacitance is the capacitance connected to the output. One $C_{D\text{-}sub}$ and the overlap capacitance from gate to drain. The capacitance from gate to drain is a Miller capacitance and is $Cm' = C_{D\text{-}sub}$

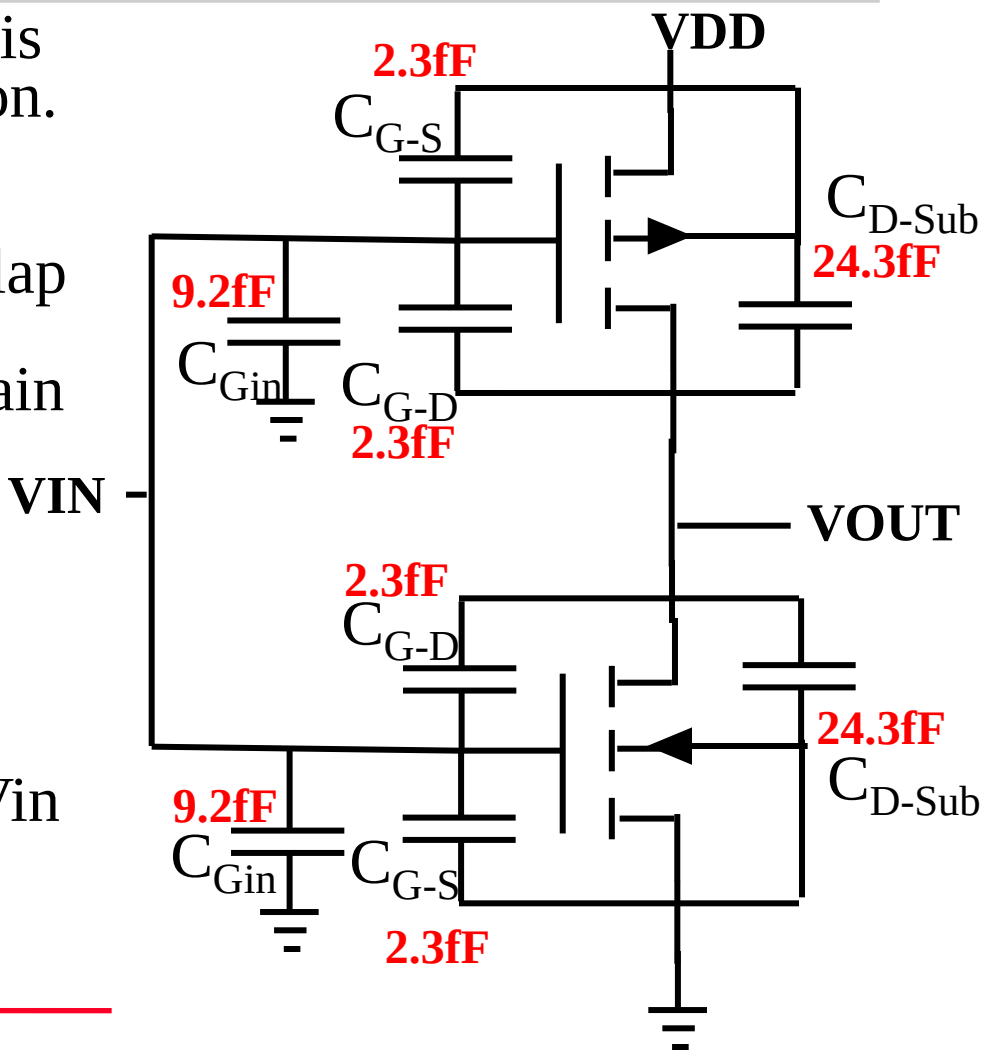
In this example:

Cself = (24.3fF + 2.3fF)

Cself=26.6fF

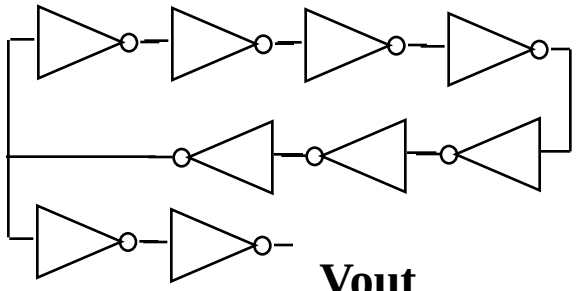
CG is everything connected to Vin Including miller effect

CG=25.3fF



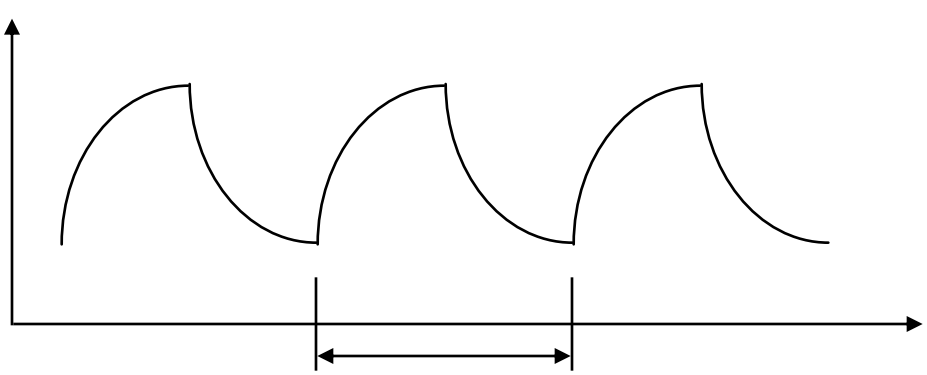
RING OSCILLATOR, td, THEORY

Seven stage ring oscillator, N=7
with two output buffers



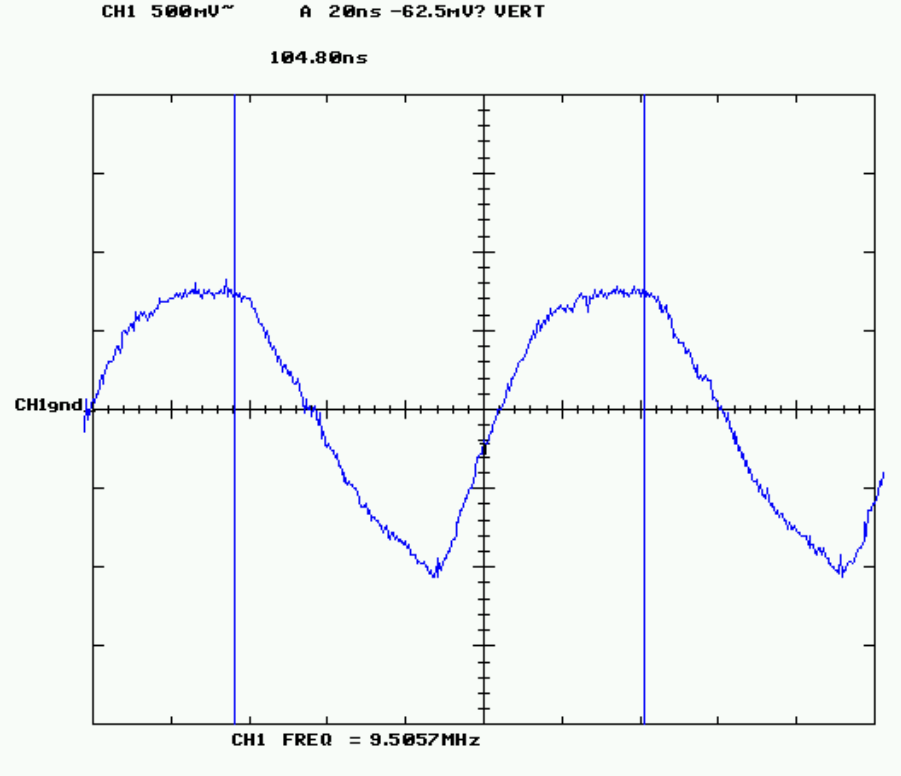
td = T / 2 N

td = gate delay
N = number of stages
T = period of oscillation

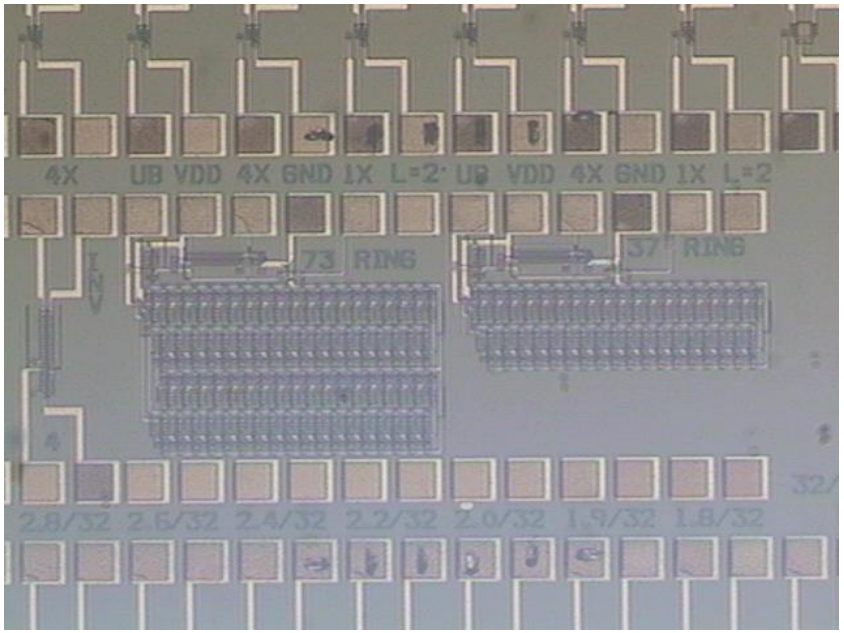


T = period of oscillation

MEASURED RING OSCILLATOR OUTPUT



RIT 2µm CMOS Ring Oscillator

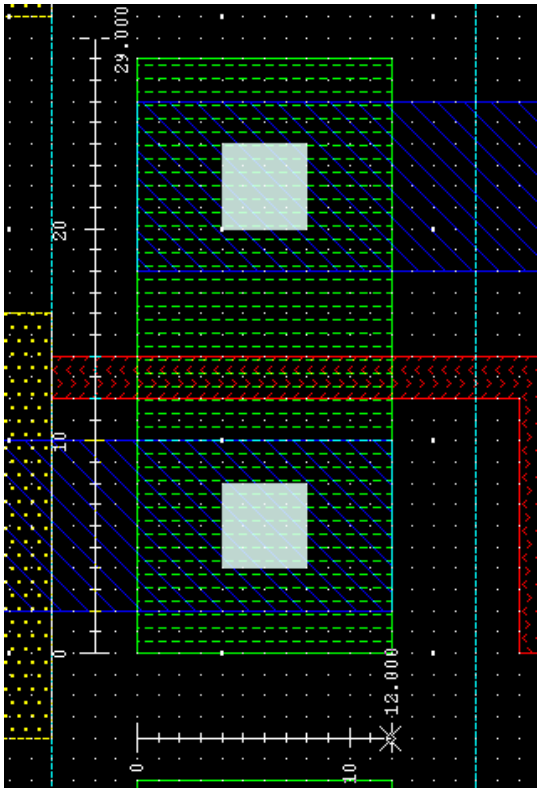


73 Stage Ring at 5V

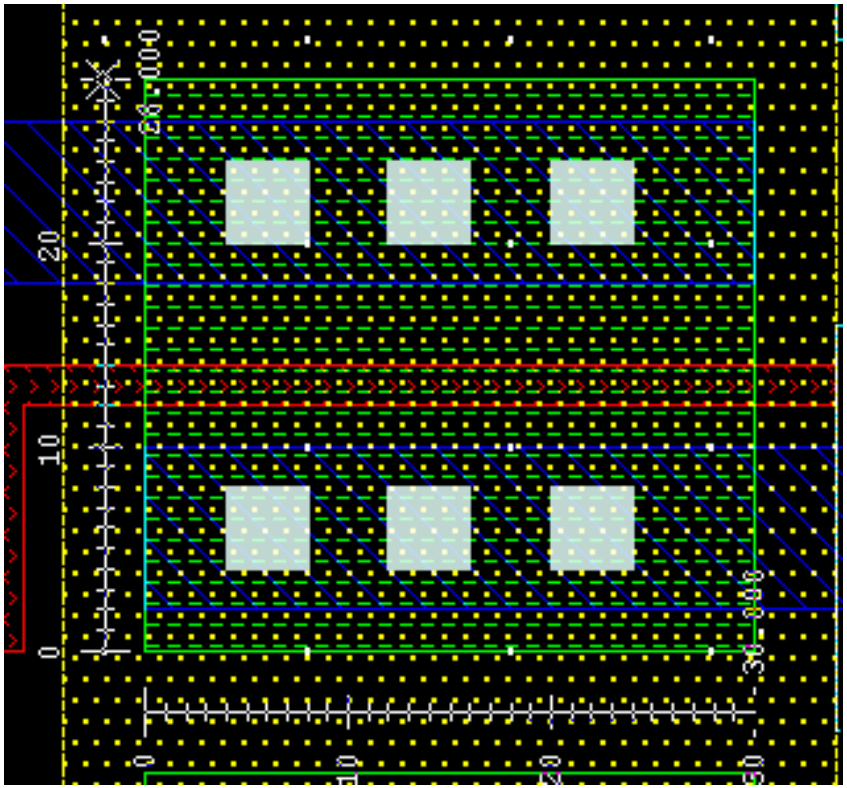
td = 104.8ns / 2(73) = 0.718 ns

MOSFETS IN THE INVERTER OF 73 RING OSCILLATOR

nmosfet



pmosfet



73 Stage Ring Oscillator

FIND DIMENSIONS OF THE TRANSISTORS

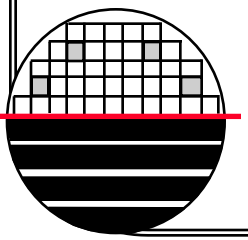
	NMOS	PMOS
L	2u	2u
W	12u	30u
AD	12ux12u=144p	12ux30u=360p
AS	12ux12u=144p	12ux30u=360p
PD	2x(12u+12u)=48u	2x(12u+30u)=84u
PS	2x(12u+12u)=48u	2x(12u+30u)=84u
NRS	1	0.3
NRD	1	0.3

73 Stage

Use Ctrl Click on all NMOS on OrCad Schematic
Use Ctrl Click on all PMOS on OrCad Schematic
Then Enter Dimensions

SPICE MODELS FOR MOSFETS

```
*4-4-2013 LTSPICE uses Level=8
*For RIT Sub-CMOS 150 process with L=2u
.MODEL RITSUBN8 NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013  LTSPICE uses Level=8
*For RIT Sub-CMOS 150 process with L=2u
.MODEL RITSUBP8 PMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



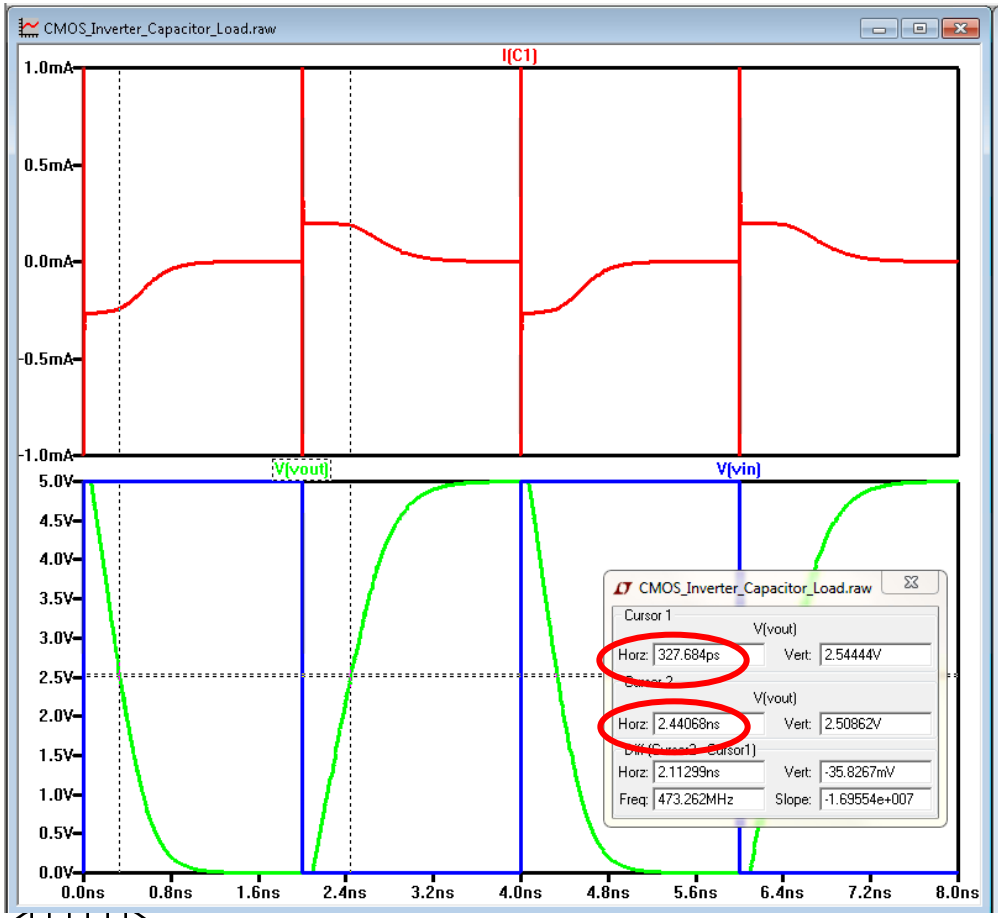
FIND DIMENSIONS OF THE TRANSISTORS

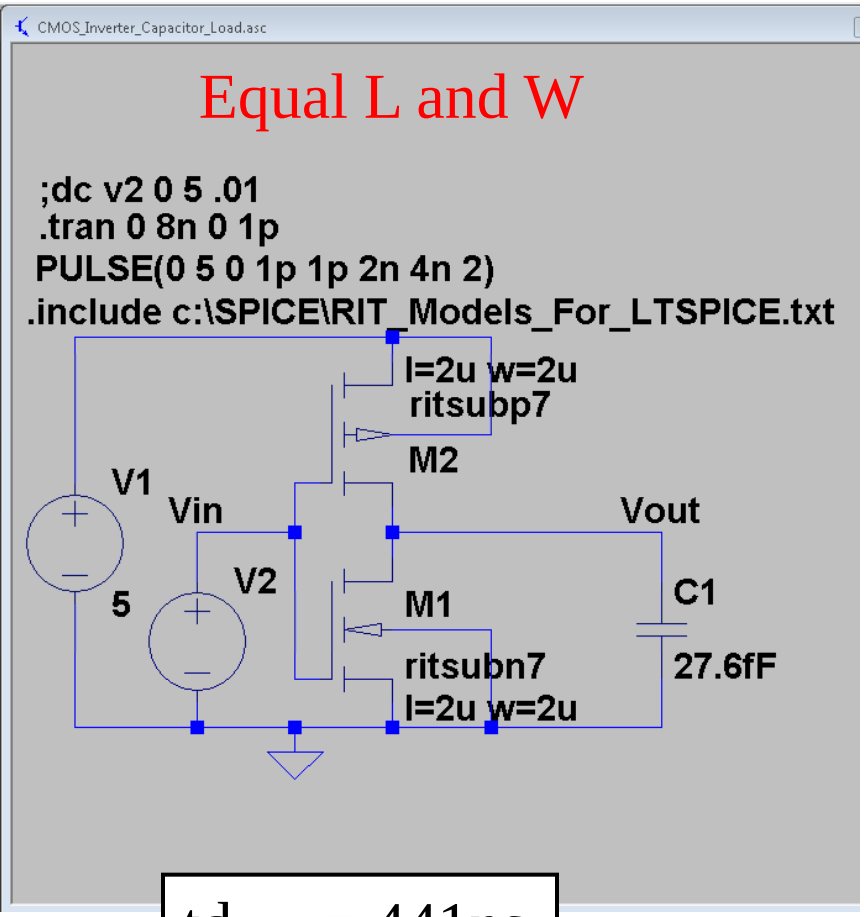
73 Stage

	NMOS	PMOS
L	2u	2u
W	12u	30u
AD	12ux12u=144p	12ux30u=360p
AS	12ux12u=144p	12ux30u=360p
PD	2x(12u+12u)=48u	2x(12u+30u)=84u
PS	2x(12u+12u)=48u	2x(12u+30u)=84u
NRS	1	0.3
NRD	1	0.3

Use Ctrl Click on all NMOS on OrCad Schematic
Use Ctrl Click on all PMOS on OrCad Schematic
Then Enter Dimensions

GATE DELAY FROM SPICE



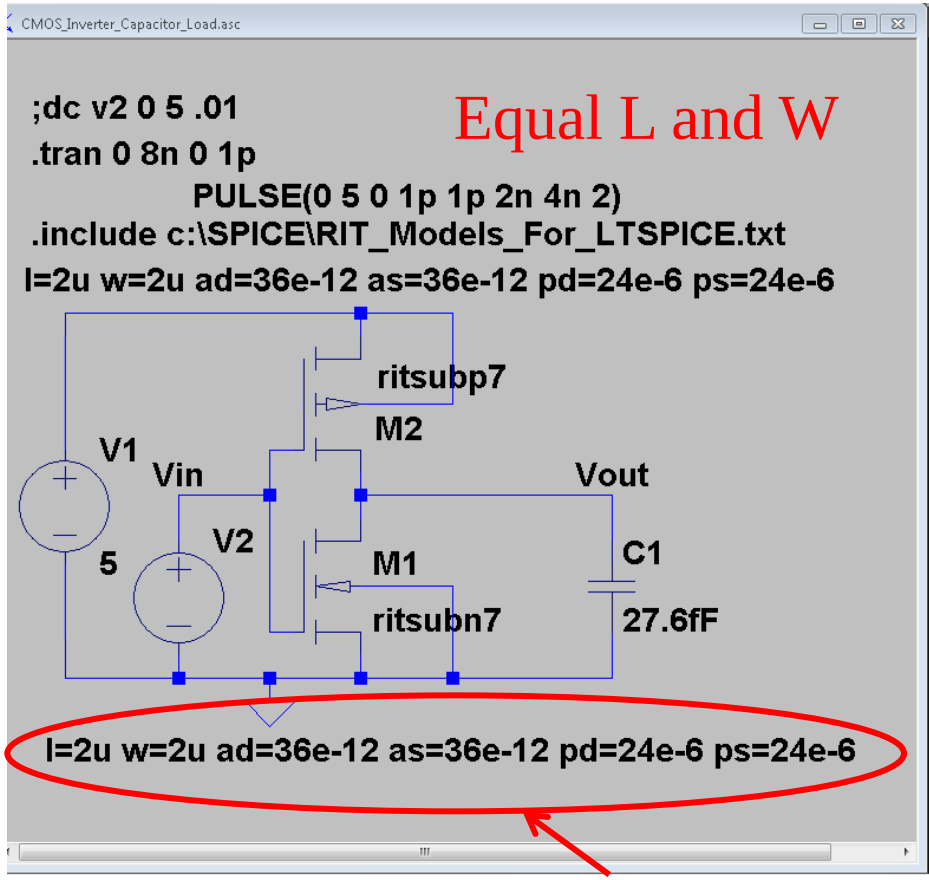


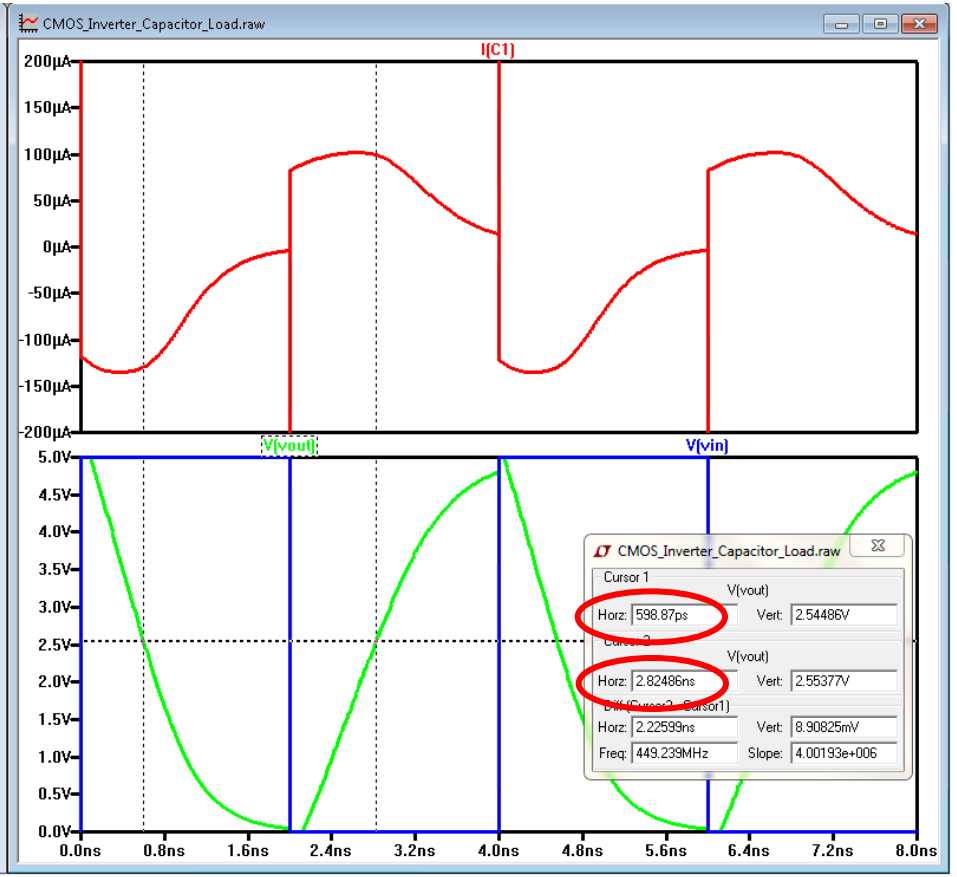
Gate delay is the time to get to 50% of the final value.

$td_{LTH} = 441ns$

$td_{HTL} = 328ns$

GATE DELAY





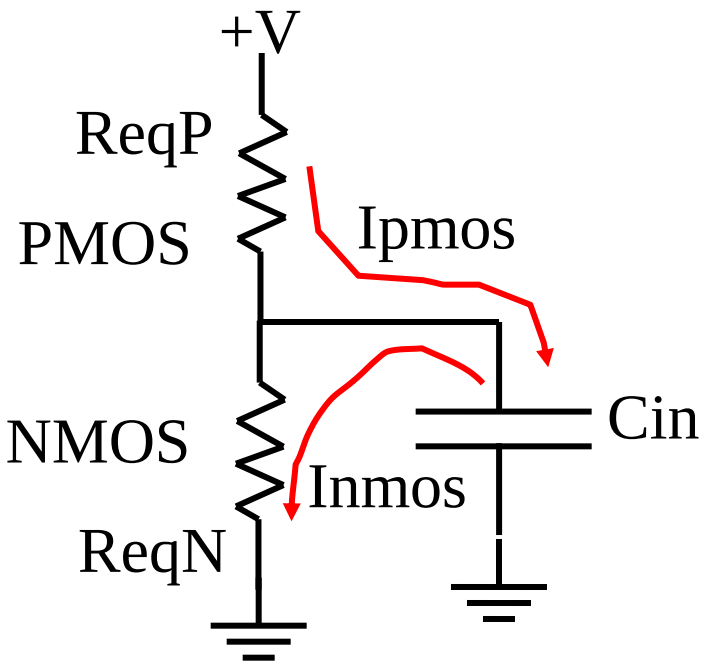
Include parameters

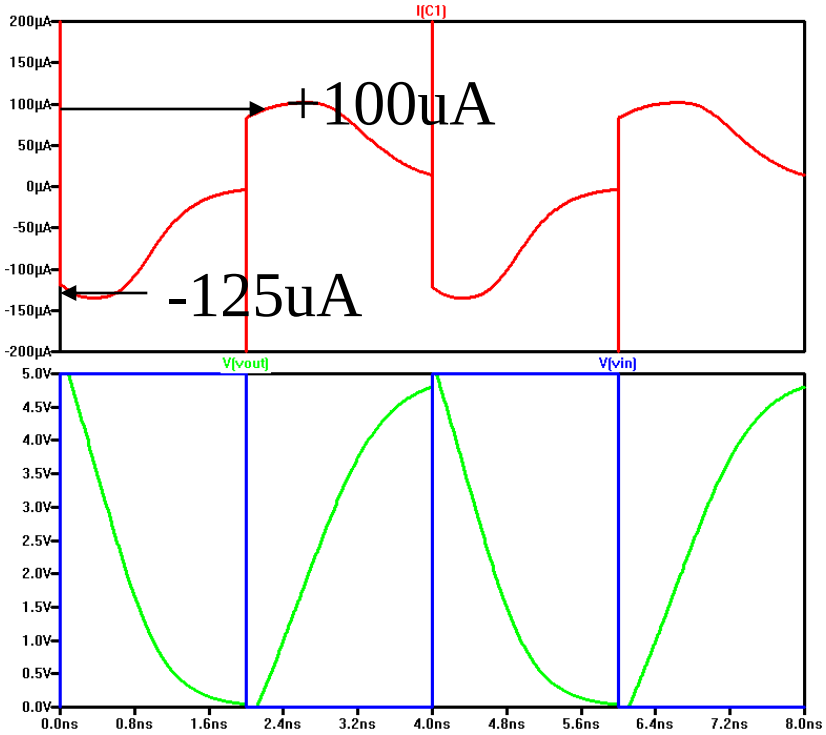
Gate delay is the time to get to 50% of the final value.

$td_{LTH} = 825ns$

$td_{HTL} = 599ns$

INVERTER MODEL FOR LTH AND HTL TRANSISTION





ReqN = ~ Vave/Iave = 3.75/125uA = 30K ohms
ReqP = ~ Vave/Iave = 3.75/100uA = 38K ohms

Gate delay is the time to get to 50% of the final value.

INVERTER RISE TIME AND FALL TIME

ReqN = ~ Vave/Iave = 3.75/125uA = 30K ohms
ReqP = ~ Vave/Iave = 3.75/100uA = 38K ohms

$$RN = 1/(q\ \mu_n\ Dose) \times Lnmos/Wnmos$$
$$RP = 1/(q\ \mu_p\ Dose) \times Lpmos/Wpmos$$

Rise/Fall time is defined as the time for Vout to go from10% to 90%.

For rise time equal to fall time the RC time constants are equal

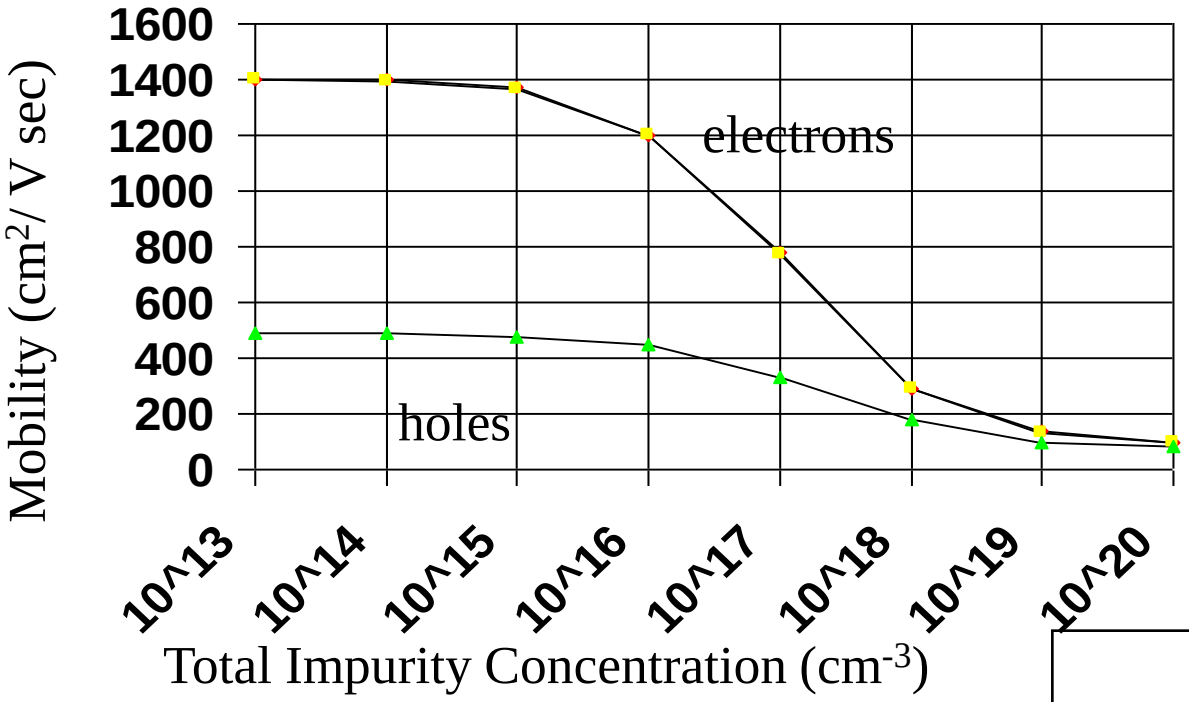
$$RN\ Cin = RP\ Cin$$
$$Lnmos/(Wnmos\ \mu n) = Lpmos/(Wpmos\ \mu p)$$
$$\mu p / \mu n = (Lpmos/Wpmos) / (Lnmos/Wnmos)$$

Often Lpmos = Lnmos

$$Finally\ \mu p / \mu n = (Wnmos/Wpmos)$$

$$\boxed{Wpmos = Wnmos\ (\mu n/\mu p)}$$

MOBILITY



Electron and hole mobilities in silicon at 300 K as functions of the total dopant concentration (N). The values plotted are the results of the curve fitting measurements from several sources. The mobility curves can be generated using the equation below with the parameters shown:

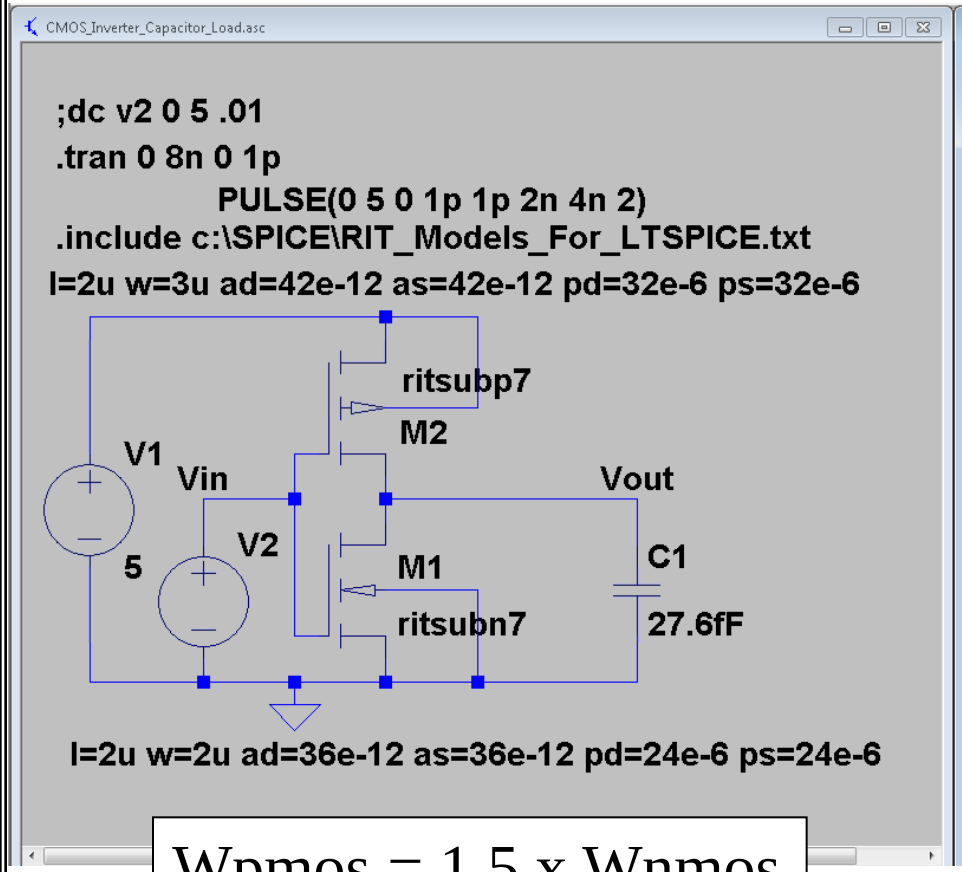
$$\mu(N) = \mu_{mi} + \frac{(\mu_{max} - \mu_{min})}{\{1 + (N/N_{ref})^{\alpha}\}}$$

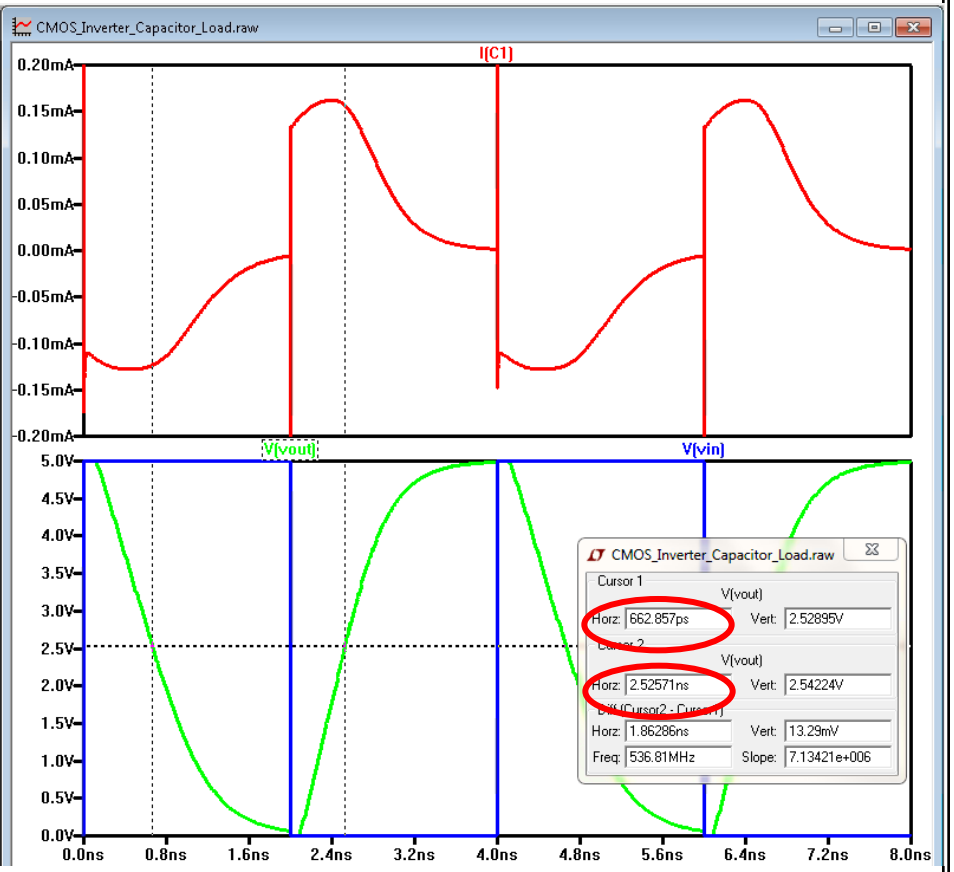
See Dr. Fuller's Mobility Calculator

From Muller and Kamins, 3rd Ed., pg 33

Parameter	Arsenic	Phosphorous	Boron
μ_{min}	52.2	68.5	44.9
μ_{max}	1417	1414	470.5
N_{ref}	9.68X10^16	9.20X10^16	2.23X10^17
α	0.680	0.711	0.719

RISE TIME EQUALS FALL TIME





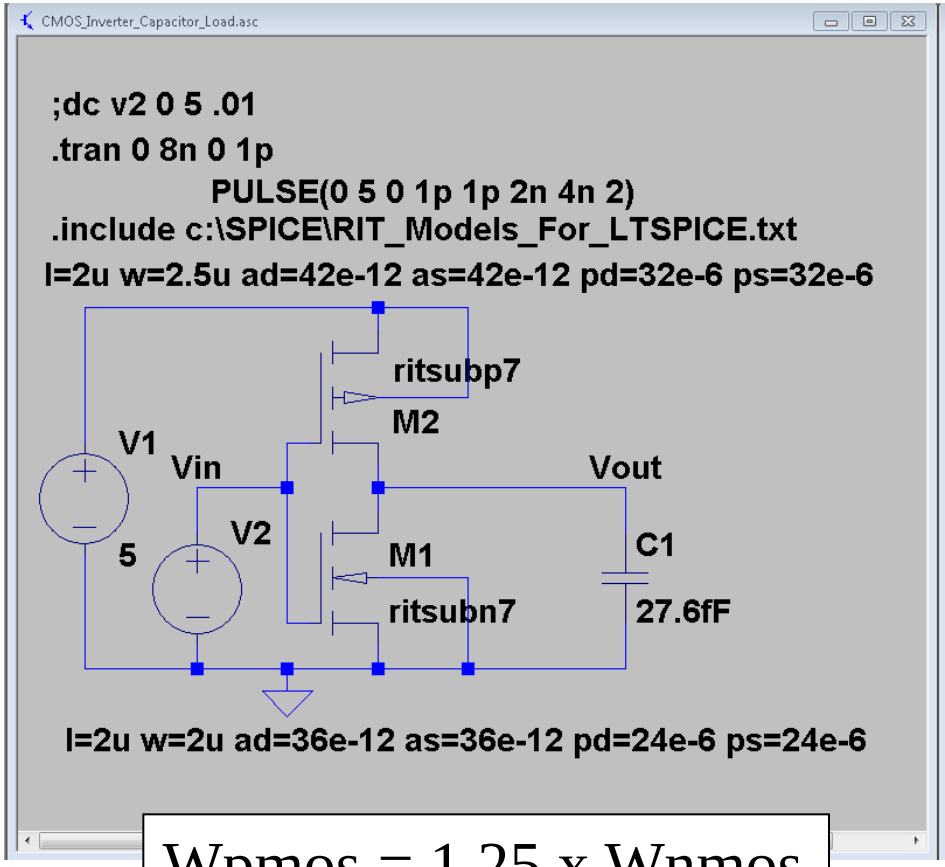
Wpmos = 1.5 x Wnmos

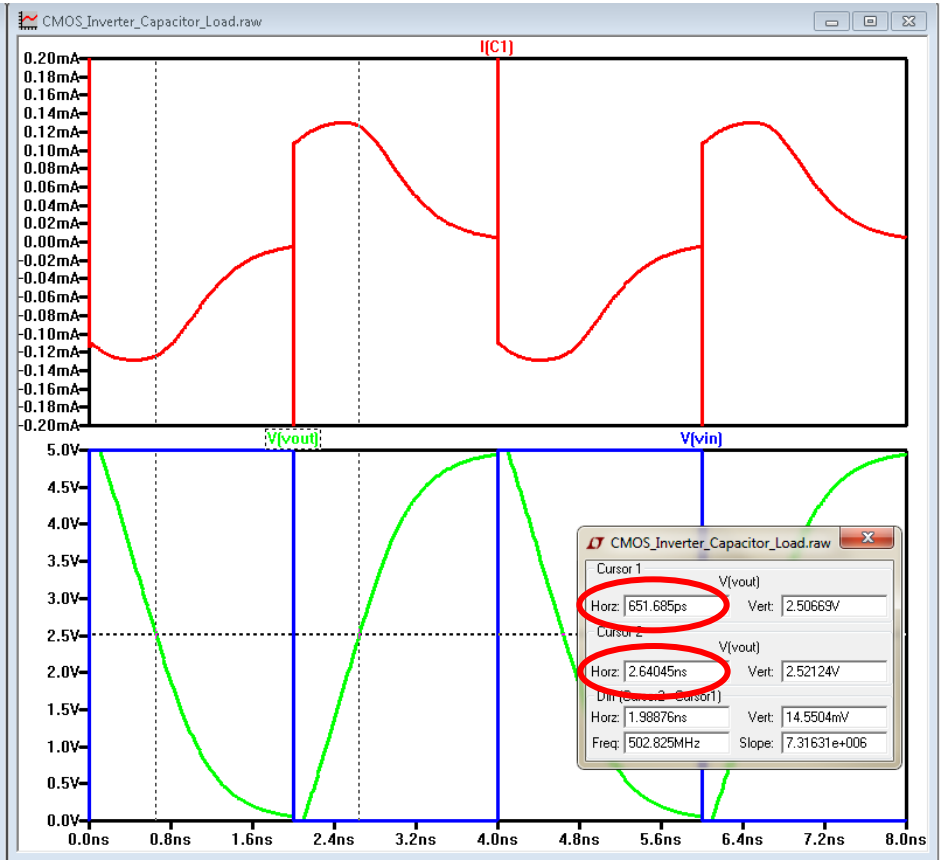
Gate delay is the time to get to 50% of the final value.

$td_{LTH} = 526ns$

$td_{HTL} = 663ns$

RISE TIME EQUALS FALL TIME





Wpmos = 1.25 x Wnmos

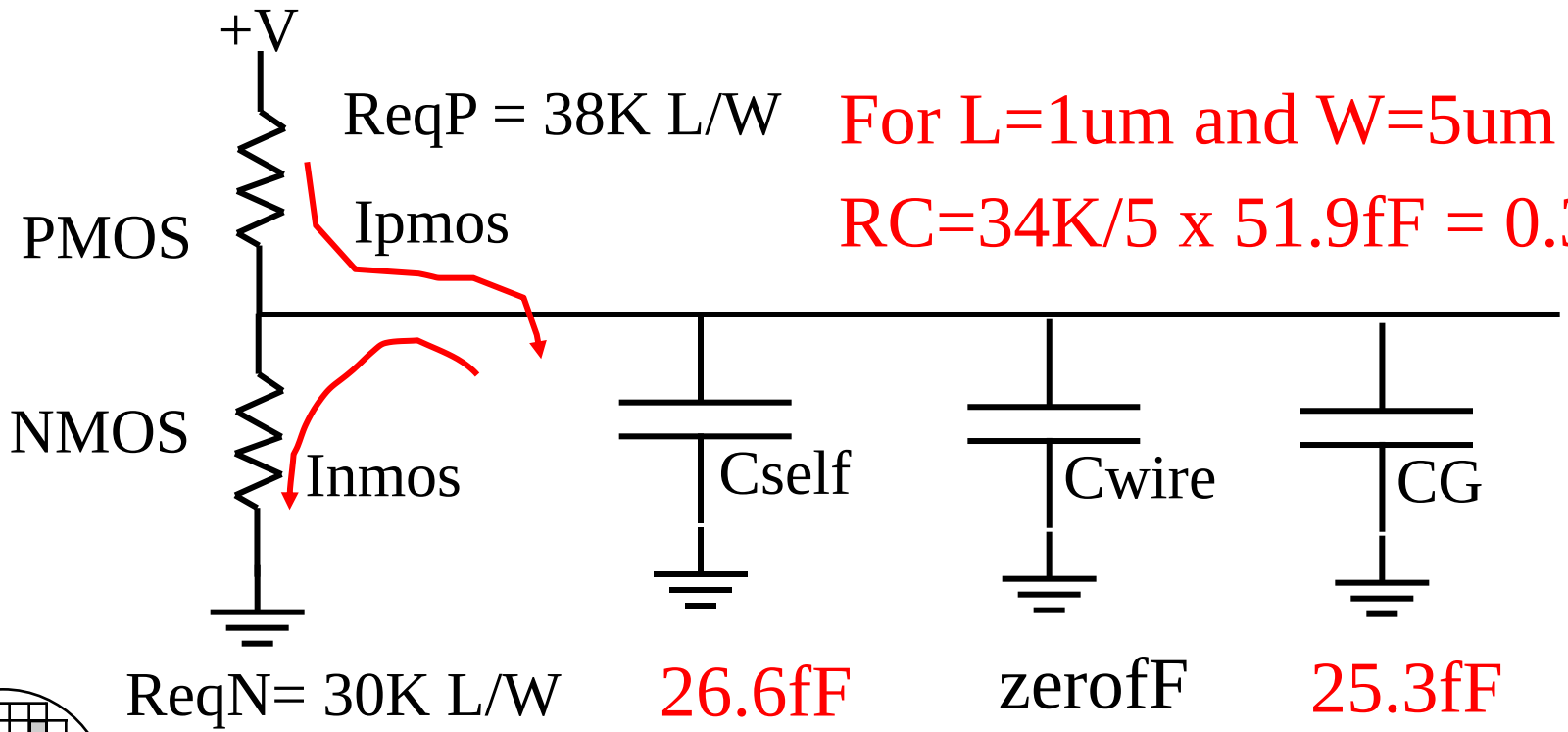
Gate delay is the time to get to 50% of the final value.

td_{LTH} = 604ns

td_{HTL} = 652ns

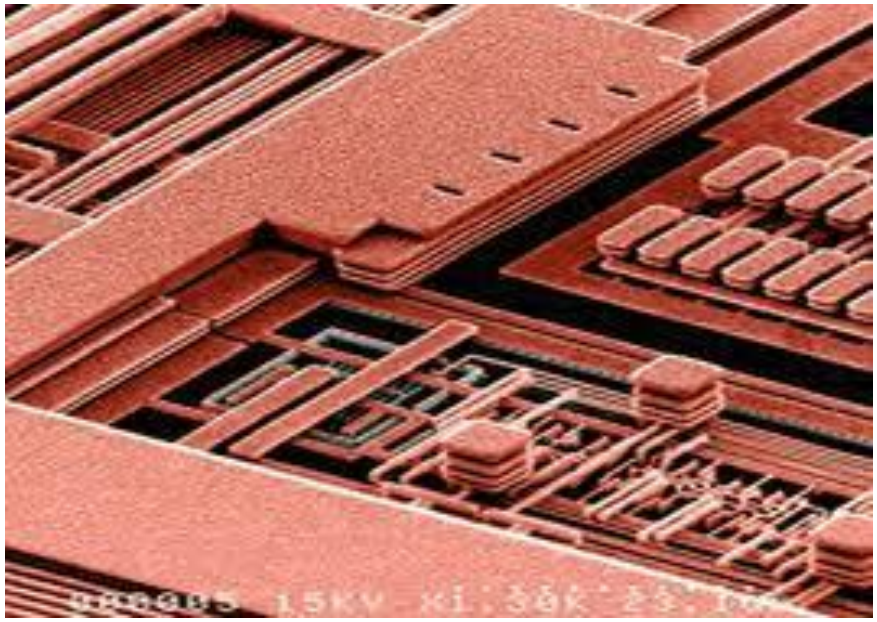
LOGIC GATE RISE TIME AND FALL TIME

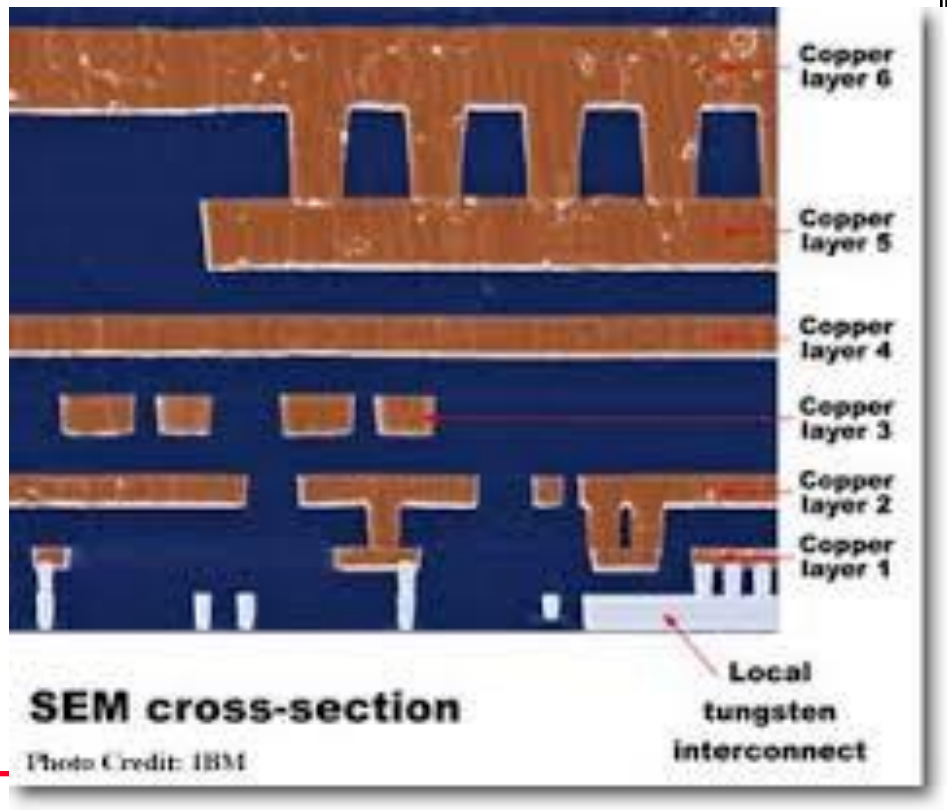
The inverter rise time is determined by the channel resistance and the capacitance to be charged or discharged.



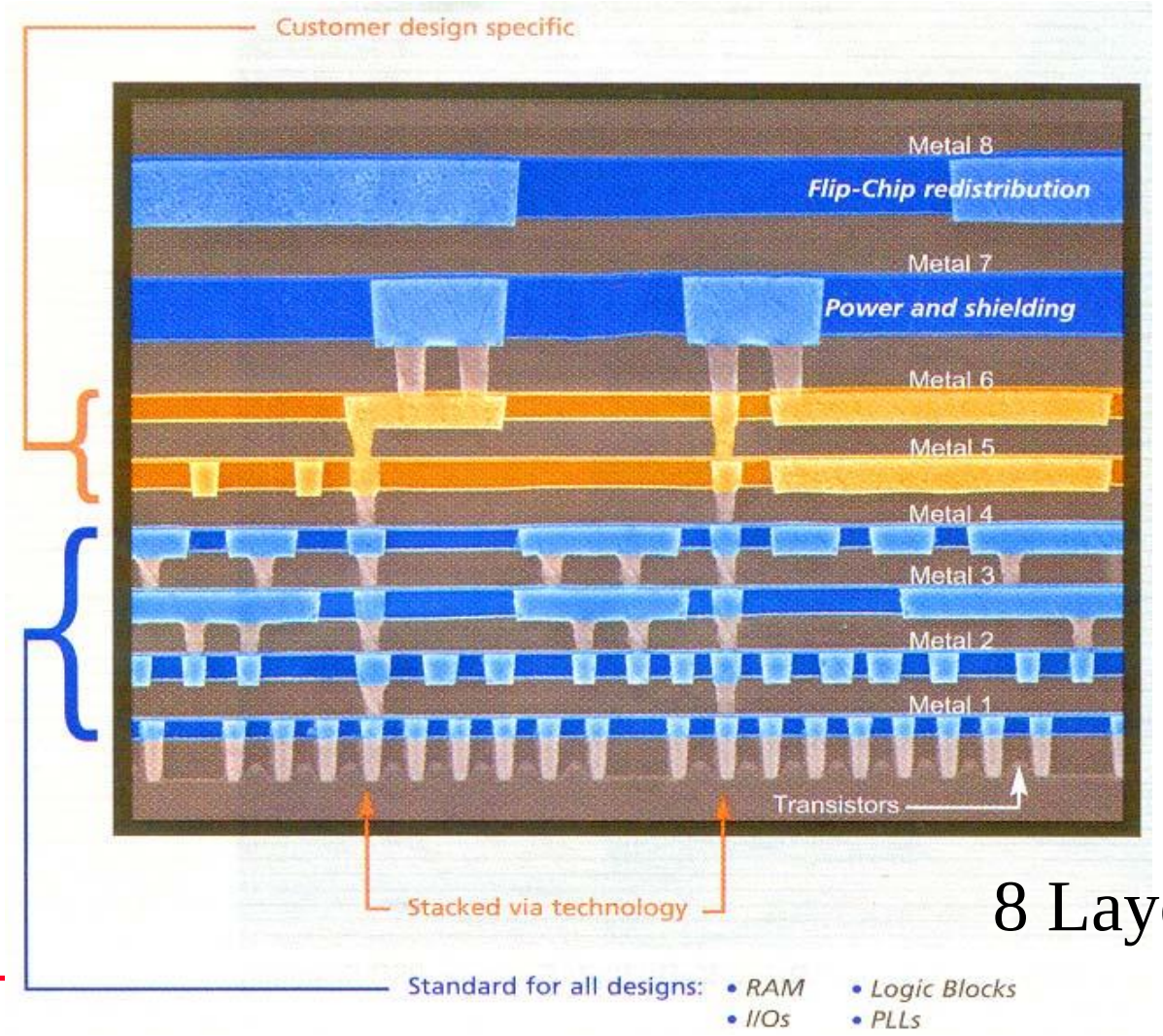
WIRE RESISTANCE AND CAPACITANCE, LOW K, CU

The wiring is typically aluminum or copper. The resistivity of aluminum is 26.5 nohm-cm and copper is 17.1 nohm-cm thus the wire will be lower resistance if copper.





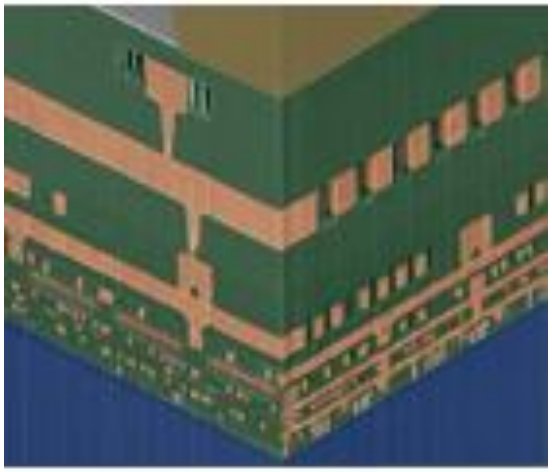
MULTILAYER METAL, W PLUGS, CMP



8 Layers Metal

LOW-K FOR INTERCONNECT

Ed's Threads 070608
Musings by Ed Korczynski on June 08, 2007

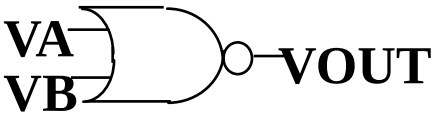


IITC 2007: Airgaps & chip-stacks
Airgaps and 3D-stacks were the big news from the 10th International Interconnect Technology Conference (IITC) recently held near the San Francisco airport. Two major new materials was presented—IBM showed rhodium (Rh) electro-chemical deposition (ECD) for ≤32nm contact plugs, and Fujitsu showed nano-clustered silicon (NCS) with low k=2.25 for a dielectric—but most new work involves the same materials combined in clever new ways. Airgap technology was covered in four oral presentations, three posters, and countless informal hallway discussions.

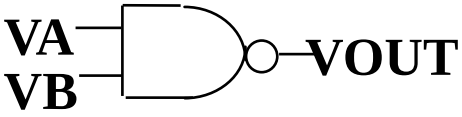
Dan Edelstein, IBM Fellow and manager of BEOL technology strategy at Yorktown Heights, NY, gave an invited talk on the many integration challenges for 32nm node interconnects, including resist poisoning from low-k outgassing, low-k damage removal, and the need for improved thin-film interfaces. "We need to keep adding innovation just to stay on the trend-line," he commented. For example, the industry has historically seen chronically low SiCOH low-k adhesion on SiCHN barrier layers—regardless of equipment, CVD precursor, or plasma preclean—due to a carbon-rich initial deposition. Adding a diverter-valve to the tool allows for stabilized precursor flow before RF power is turned on, which eliminates the carbon-rich deposition and thus solves the adhesion issue. With subtle integration challenges such as these, IBM has chosen to add airgaps as a side-loop with no new materials, tools, or baseline processes. Airgaps drop k by ~35% for any given dielectric material, Edelstein noted, adding that IBM has "shown this on gapped SiOF and low-k SiCOH, and will do it next on ULK porous SiCOH."

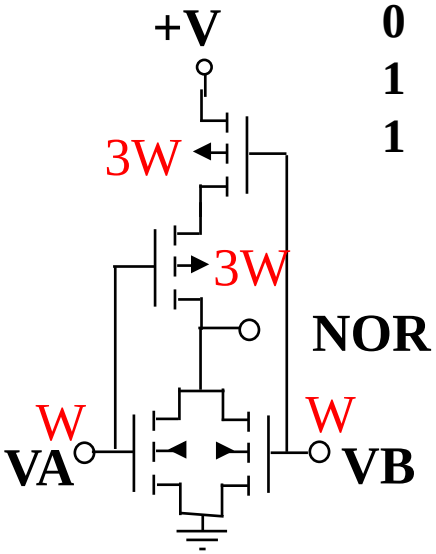
LOGIC GATES RISE TIME AND FALL TIME

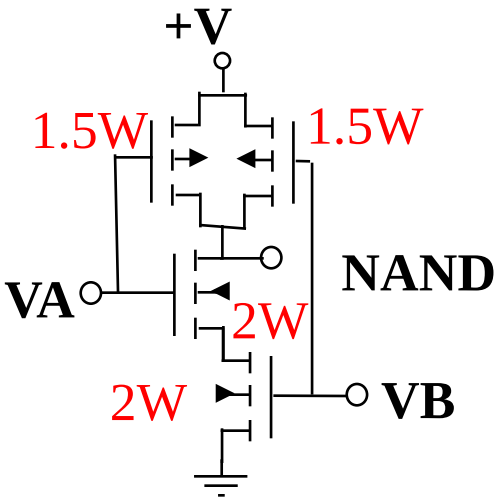
The design guide line is that the logic gate under consideration should have the same rise time and fall time as the inverter (after we adjusted the inverter for equal rise time and fall time. Assume L's are the same. $(W/L)_{pullup} = \sim 1.5\ (W/L)_{pulldown}$ based on mobility only



VA	VB	NOR	NAND
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0



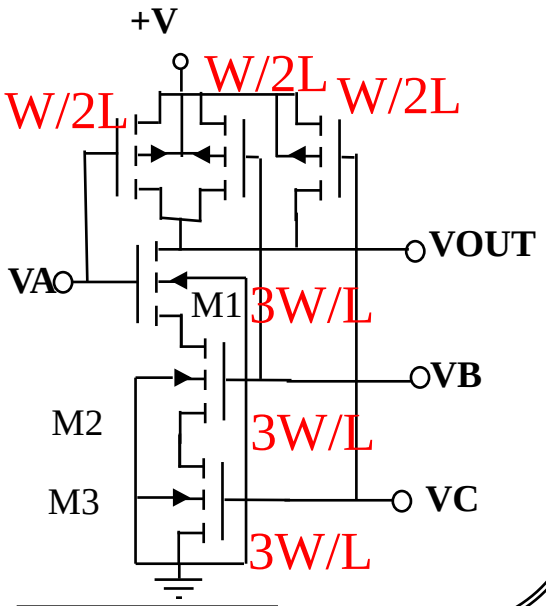




SIZING AND TIMING FOR THREE-INPUT NAND

To achieve equal rise time and fall time (and make these times approximately equal to the simple inverter rise time and fall time). The transistors length and width can be calculated. In the simple inverter the nmos W/L is the smallest values for that technology. The pmos is 1.5 times wider to give equal drive current. For a more complex gate there will be transistors in series and parallel and those combinations need to be considered when trying to achieve rise and fall times equivalent to the simple inverter. For example:

M1, M2 and M3 have a combined length of 3L So the combined width should be 3W to give drive current equivalent to the nmos in the simple inverter. Each nmos 3W/L

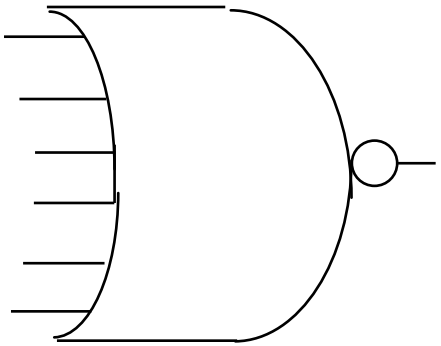


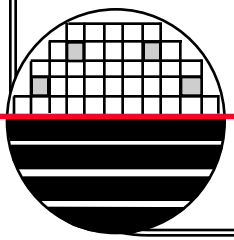
The pmos have a combined width of 3W and a length of L. The simple inverter calls for the pmos to have W/L of 1.5 so make L two times the L of the simple inverter.

FAN IN AND FAN OUT CONSIDERATIONS

Fan in refers to the number of inputs to a gate. It is common to have up to 8 inputs. In CMOS this implies that there are 8 transistors in parallel and 8 transistors in series. The 8 in parallel is not necessarily a problem but the 8 in series is because of the body effect on the threshold voltage of some of the transistors if they are all in the same well (at Vss or Vdd for p-well or n-well respectively) The solution to this problem is to use a Pseudo CMOS logic gate where the series transistors are replaced by a single transistor with the gate wired to VDD or Ground for NMOS or PMOS respectively. This transistor is always on.

Fan-In = 6

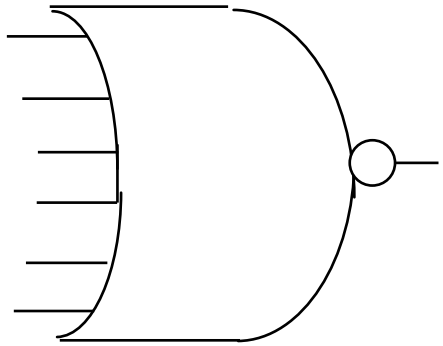




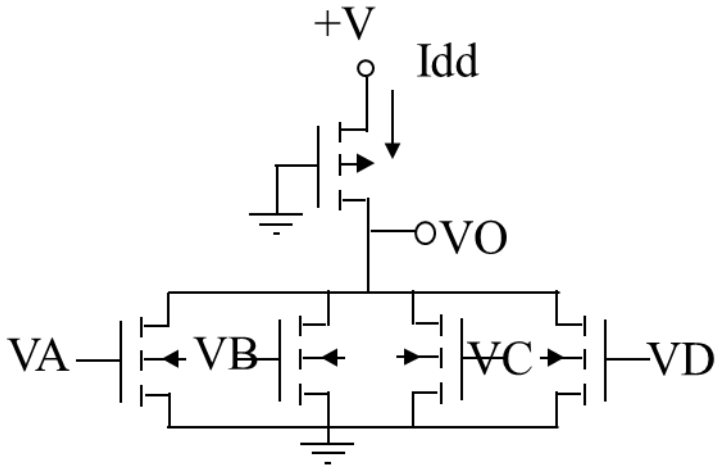
FAN IN AND FAN OUT CONSIDERATIONS

What is the correct sizing for the transistors in this gate?

Fan-In = 6



1.5W



2W

4 Input NOR

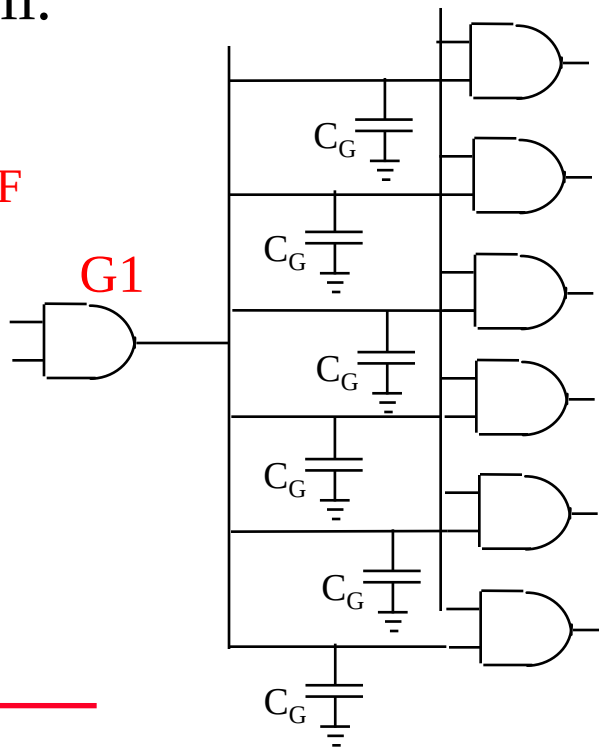
FAN OUT GATE CAPACITANCE

Fan out refers to the number of gates connected to the output of a gate. Each gate adds more capacitance to be charged or discharged during switching which has implications on rise time, fall time and gate delay. The size (W and L) of the MOSFETS in the gate, G1, can be set to keep the gate delay small.

$C_G = C_{Gin +} C_{G-S} + C_{G-D} (1-Av)$
$= 23fF + 2.3fF + 2.3fF \times (1- -5) = \sim 25fF$

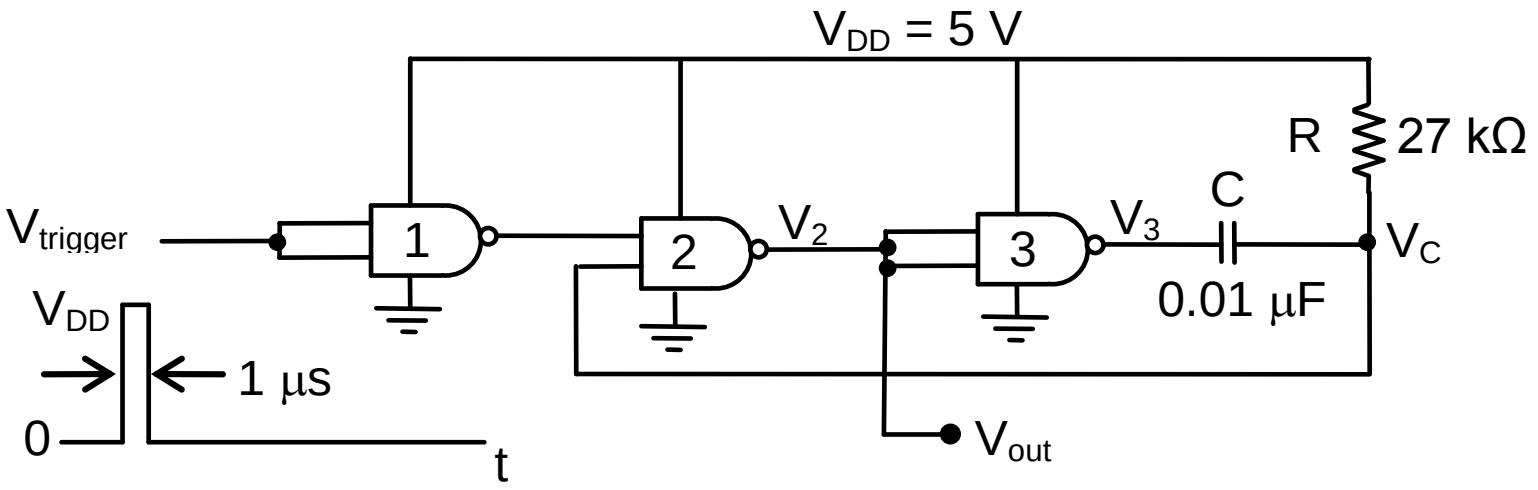
Fan-Out = 6

$C_{fan-out}$ = Fan-Out x (C_G)
= 6 x 25fF = 150fF



MONO STABLE MULTIVIBRATOR

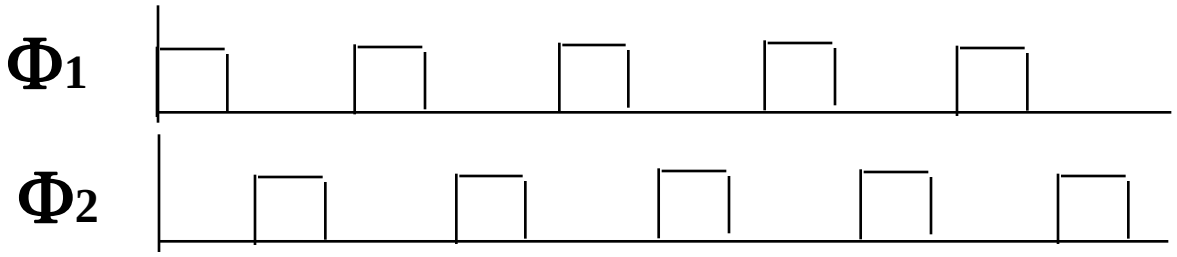
This circuit will give a pulse at Vout whose width depends on RC time constant.

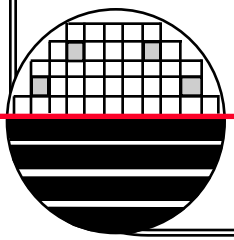


Start with Vtrigger=0 and Vc=0

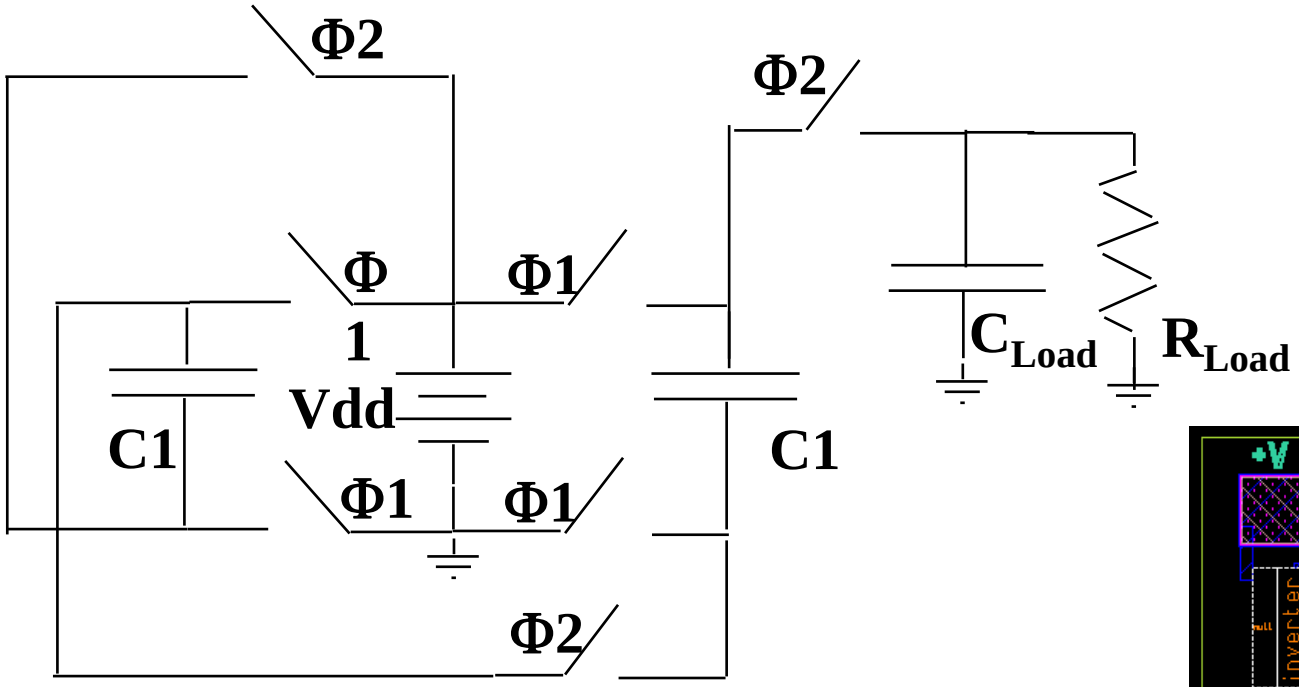
TWO PHASE NON OVERLAPPING CLOCK

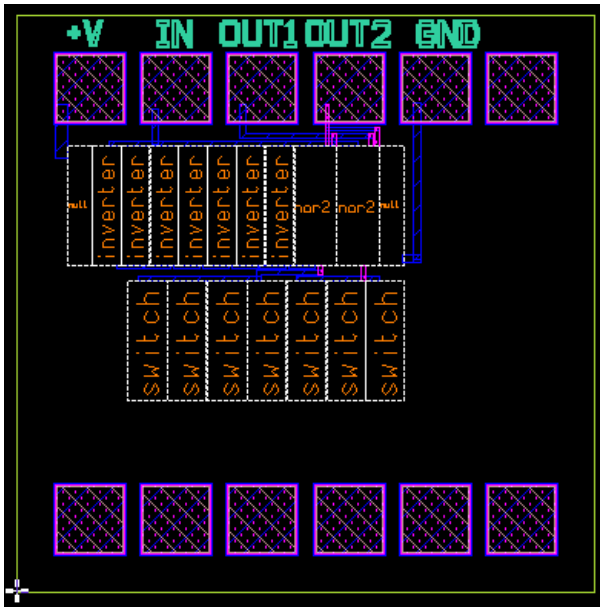
Synchronous circuits that use the two phase non overlapping clock can separate input quantities from output quantities used to calculate the results in feedback systems such as the finite state machine.





SWITCHED CAPACITOR VOLTAGE DOUBLER

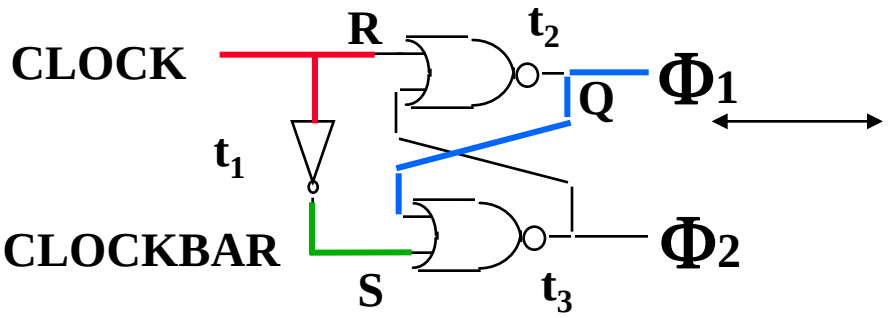




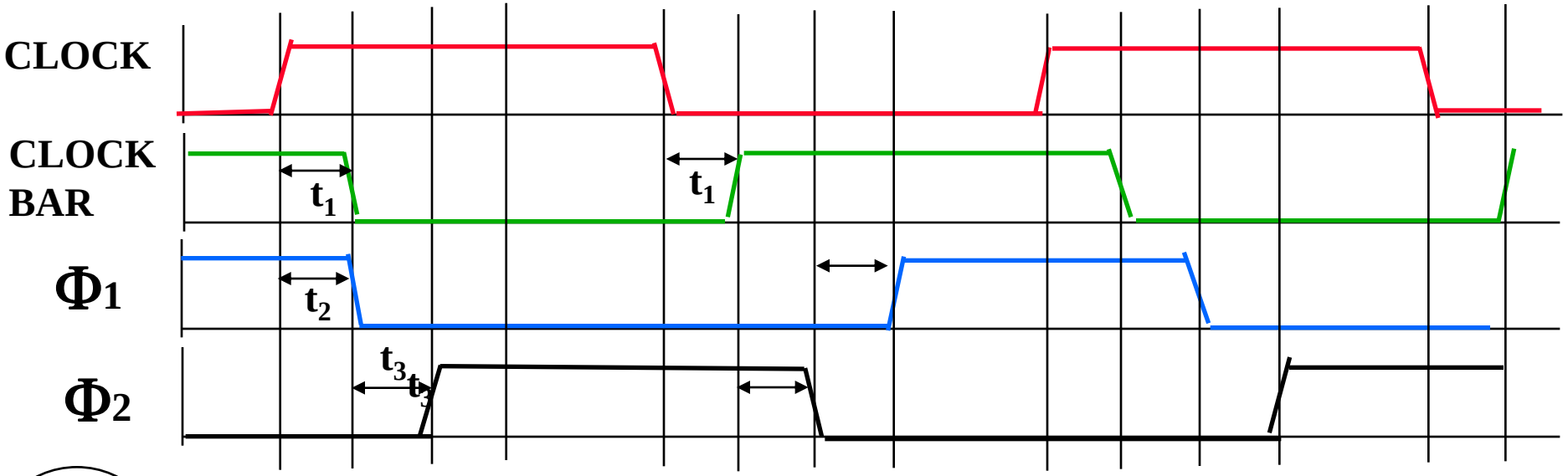
Another example for two phase non overlapping clocks

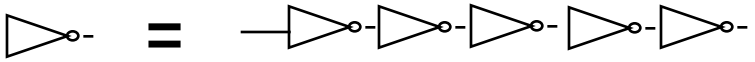
TWO-PHASE CLOCK GENERATORS

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

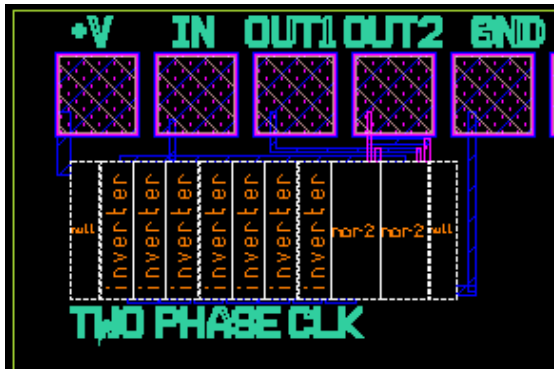


R	S	Q
0	0	Qn-1
0	1	1
1	0	0
1	1	INDETERMINATE

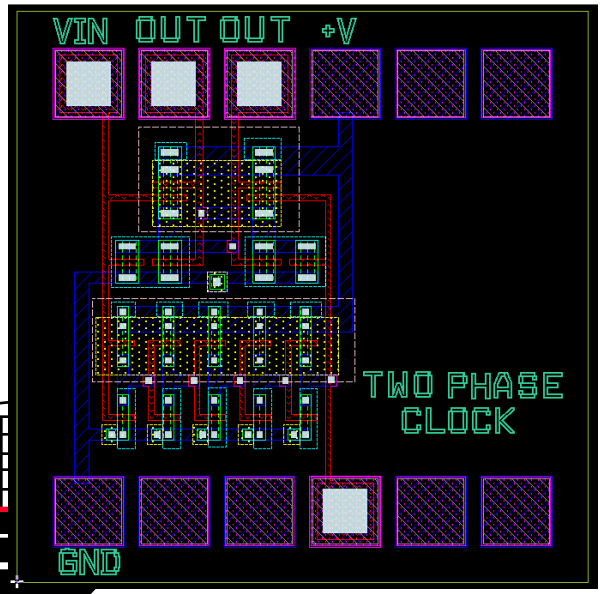


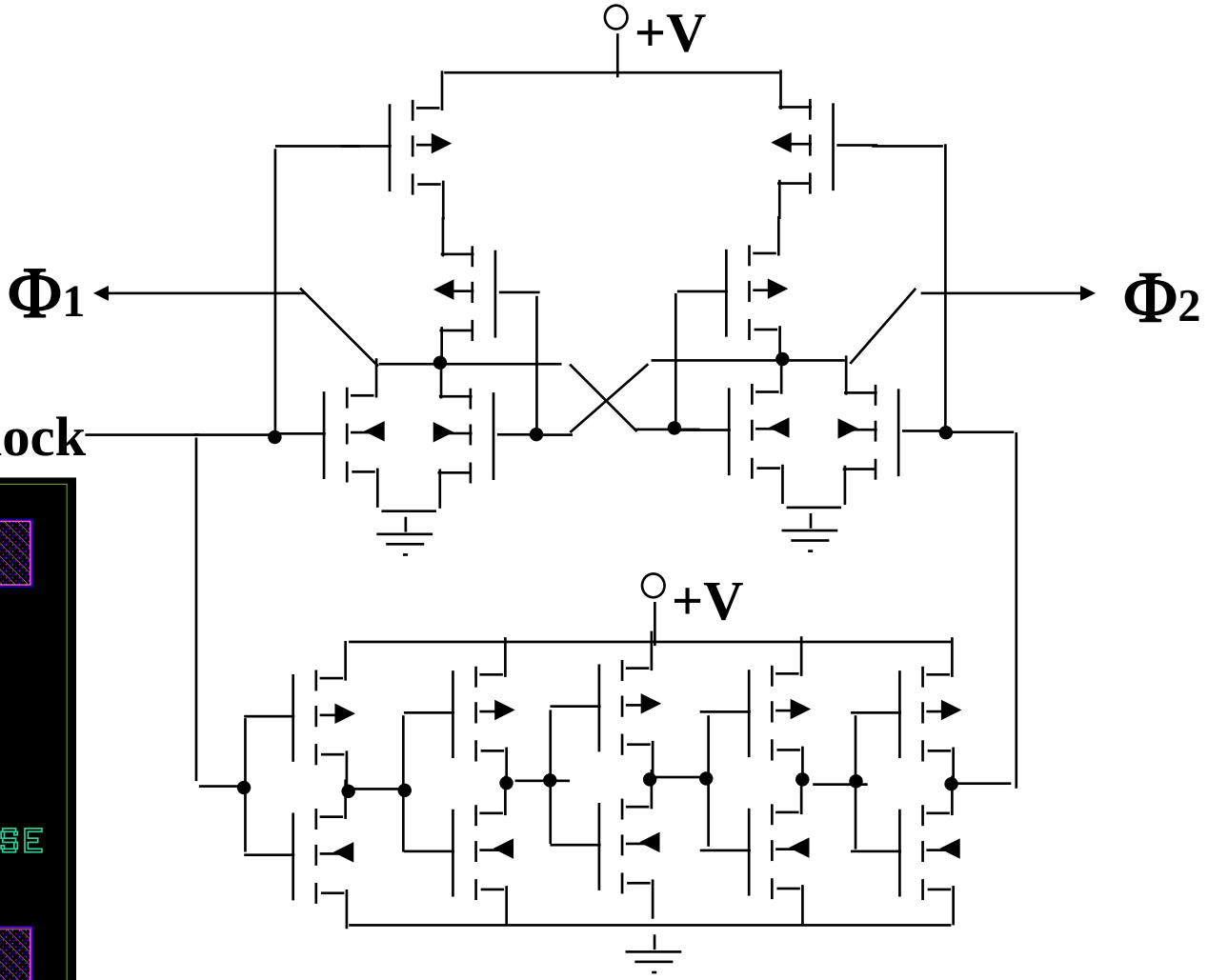


TRANSISTOR LEVEL SCHEMATIC OF 2 PHASE CLOCK

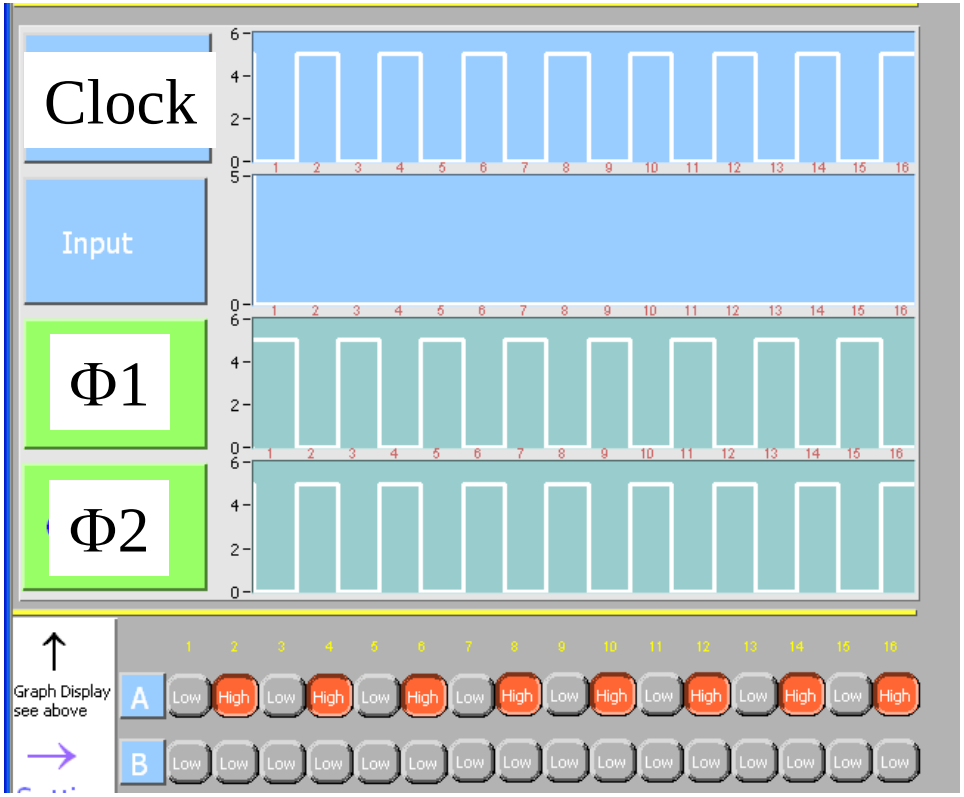


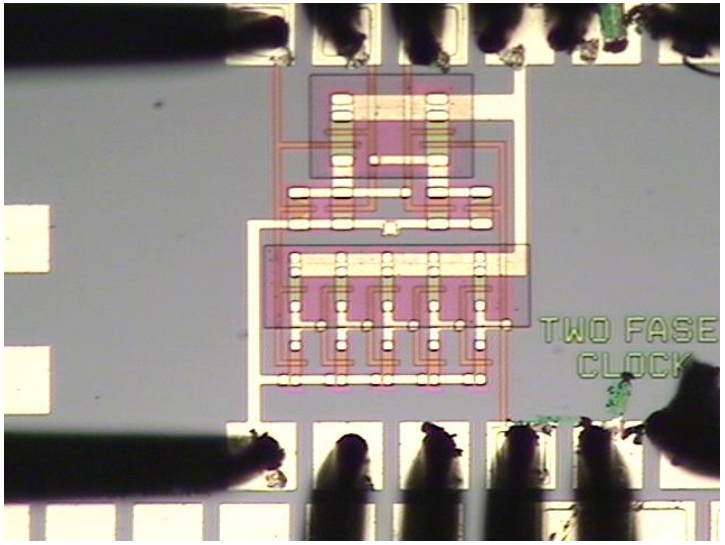
Layout

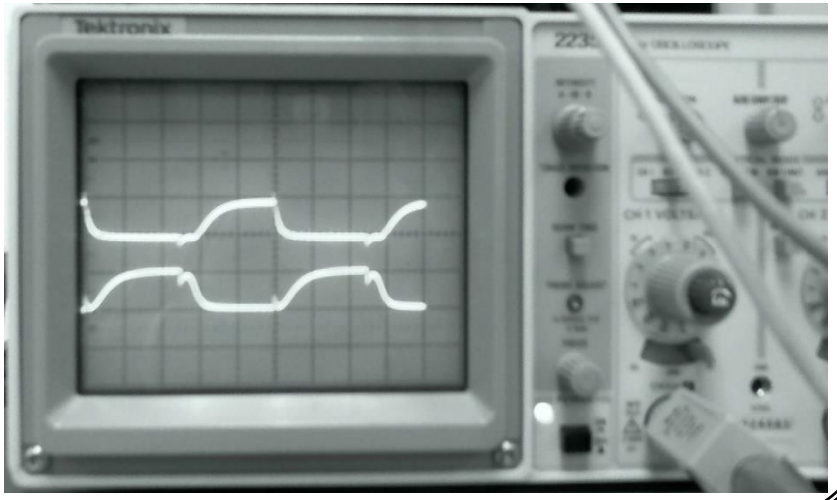




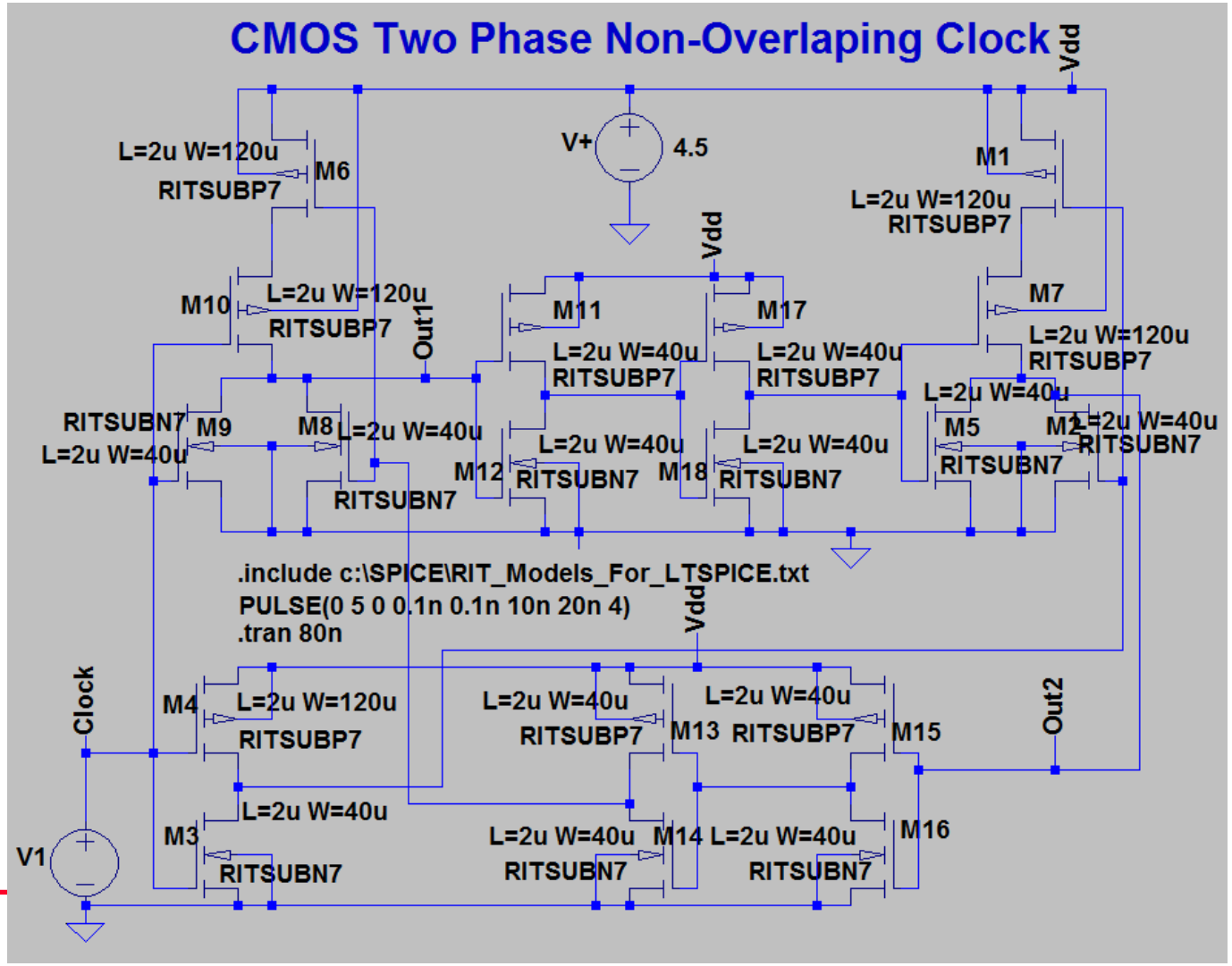
TWO PHASE NON OVERLAPPING CLOCK



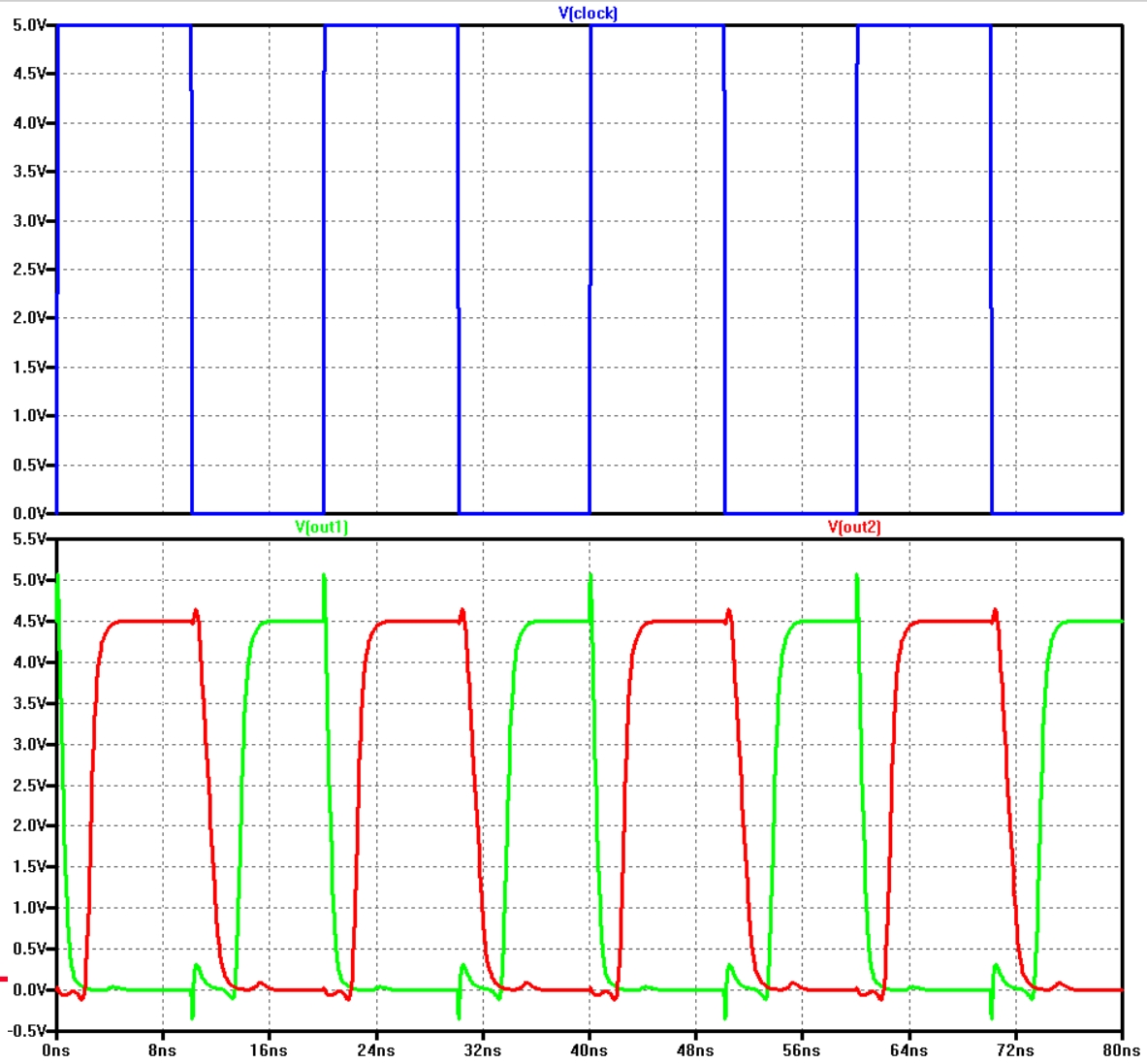




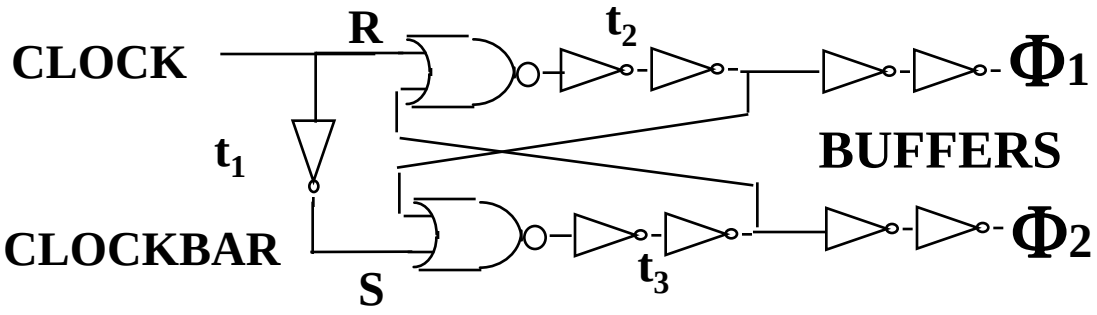
CMOS TWO PHASE NON-OVERLAPPING CLOCK

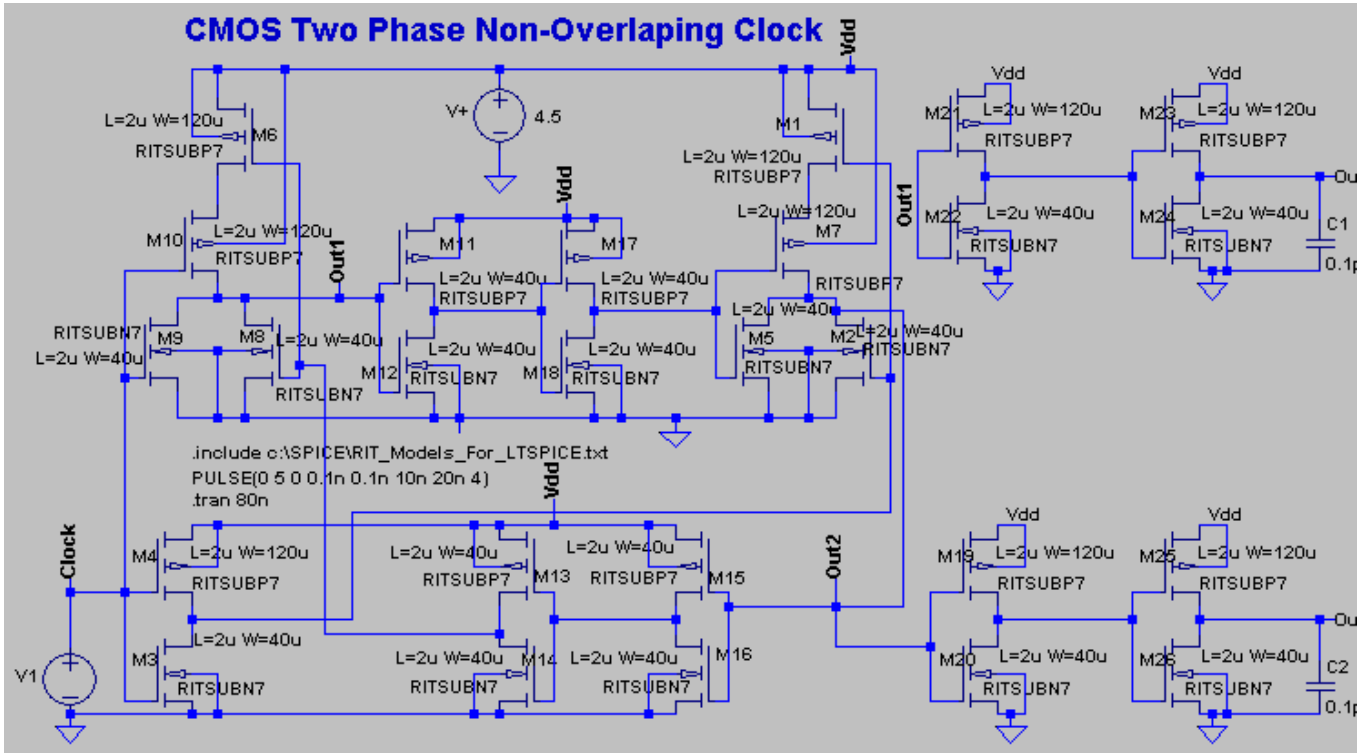


CMOS TWO PHASE NON-OVERLAPPING CLOCK

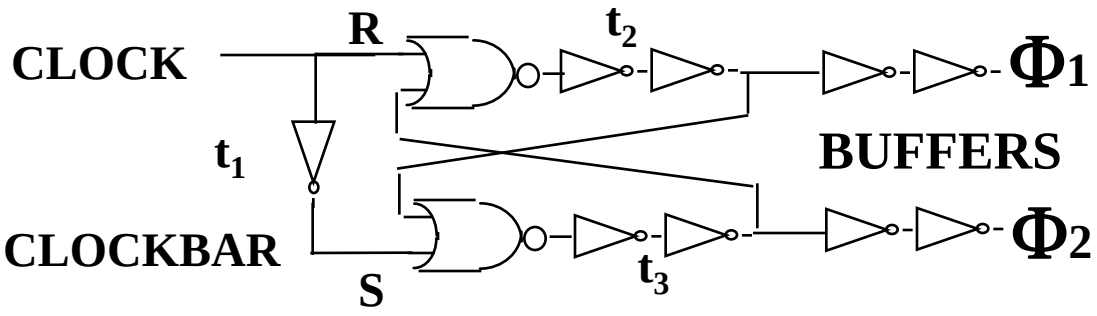


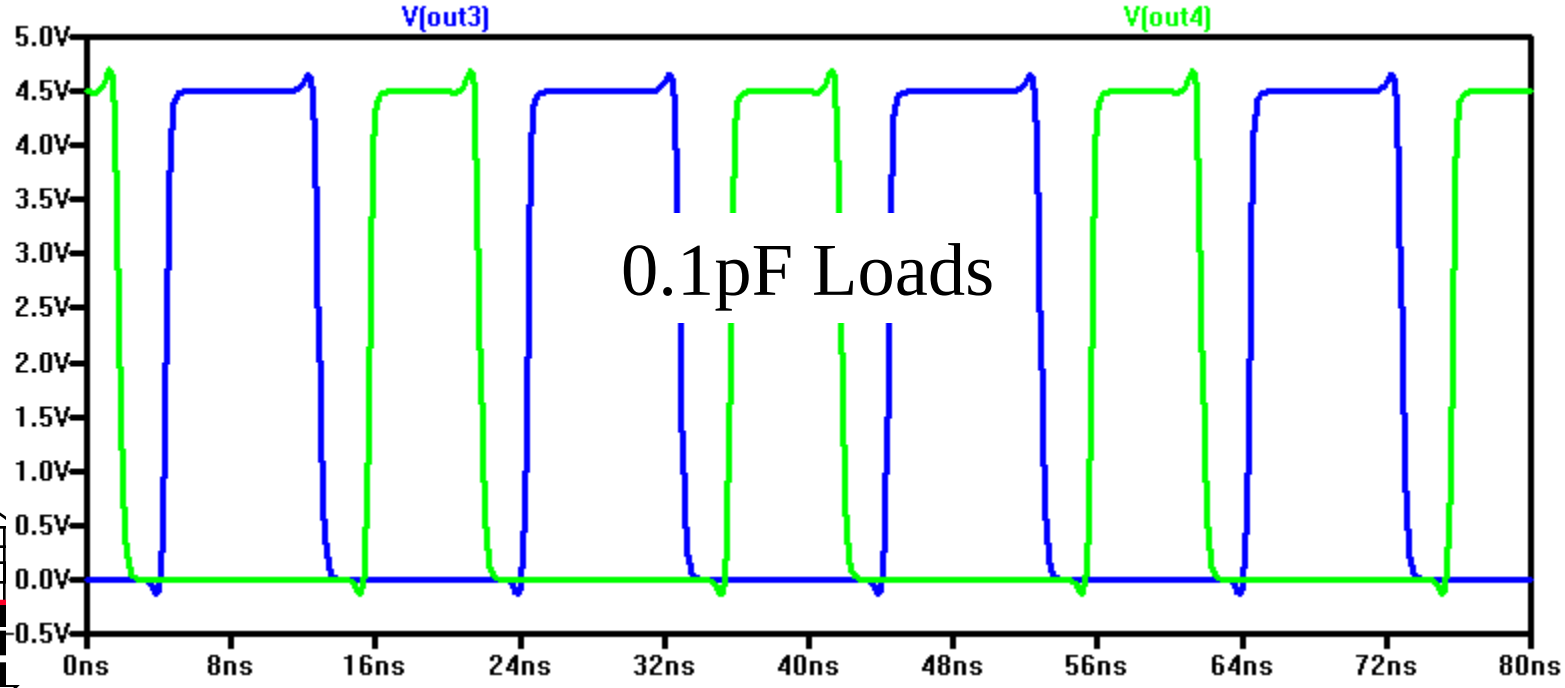
SIMULATION NON-OVERLAPPING CLOCK + BUFFERS



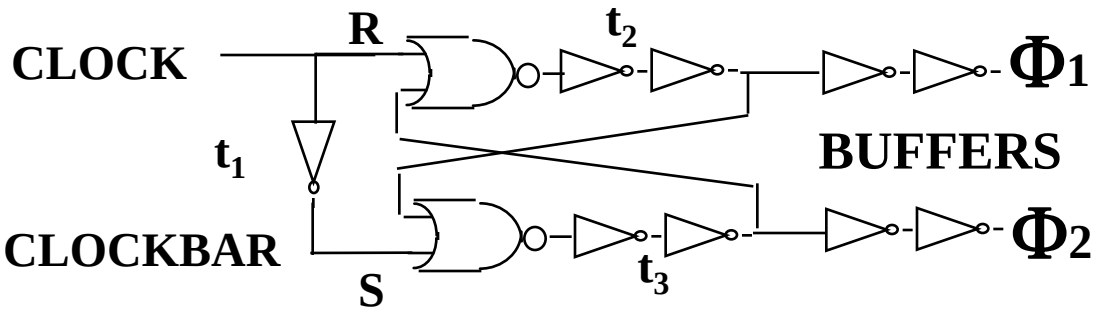


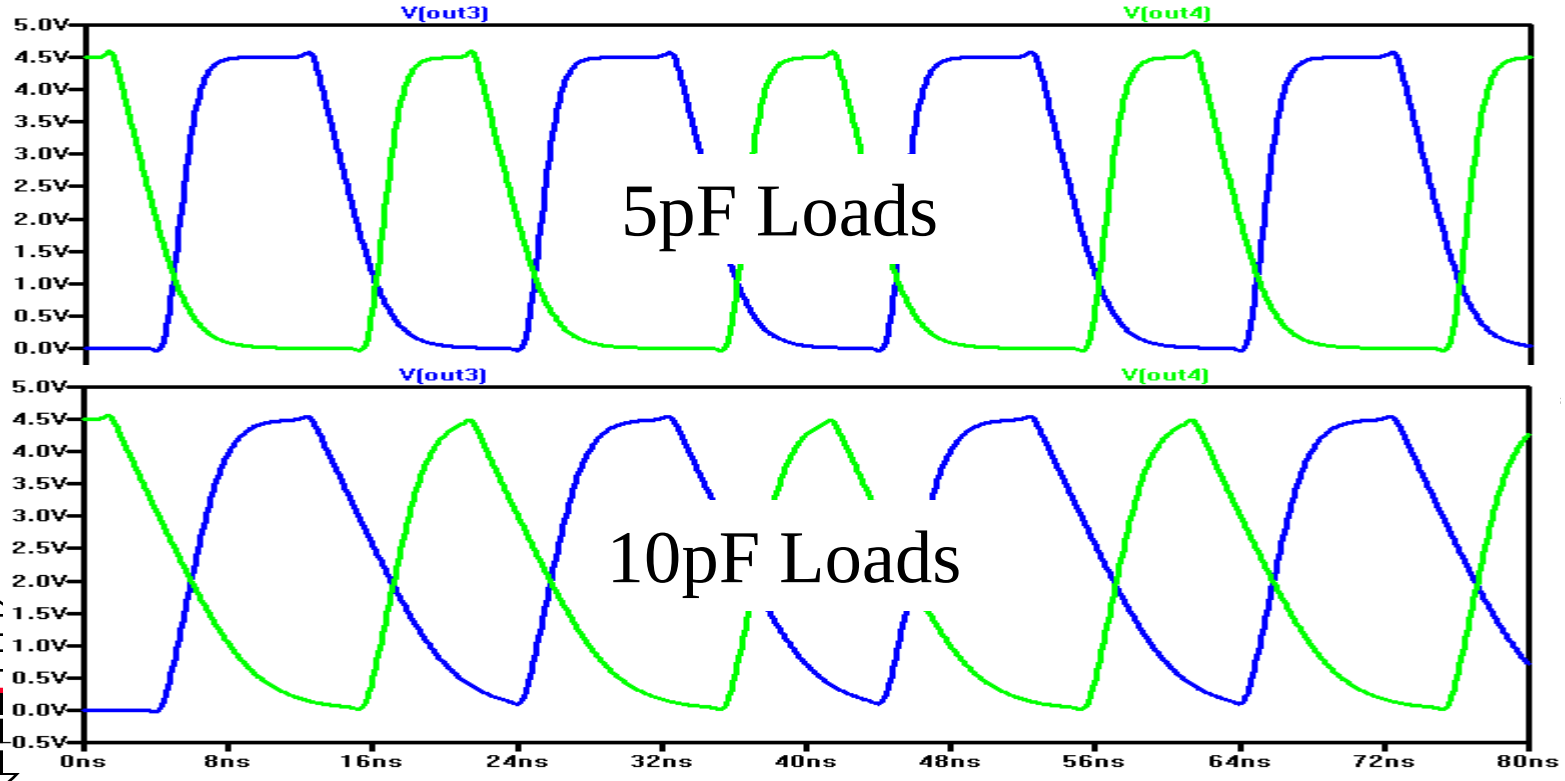
SIMULATION NON-OVERLAPPING CLOCK + BUFFERS



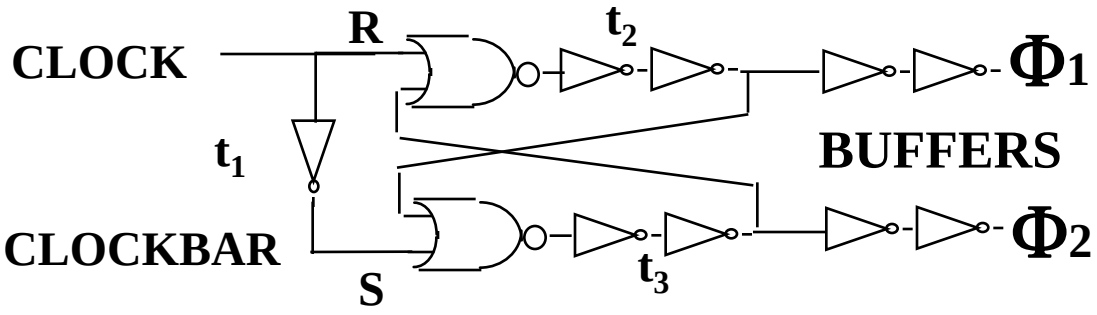


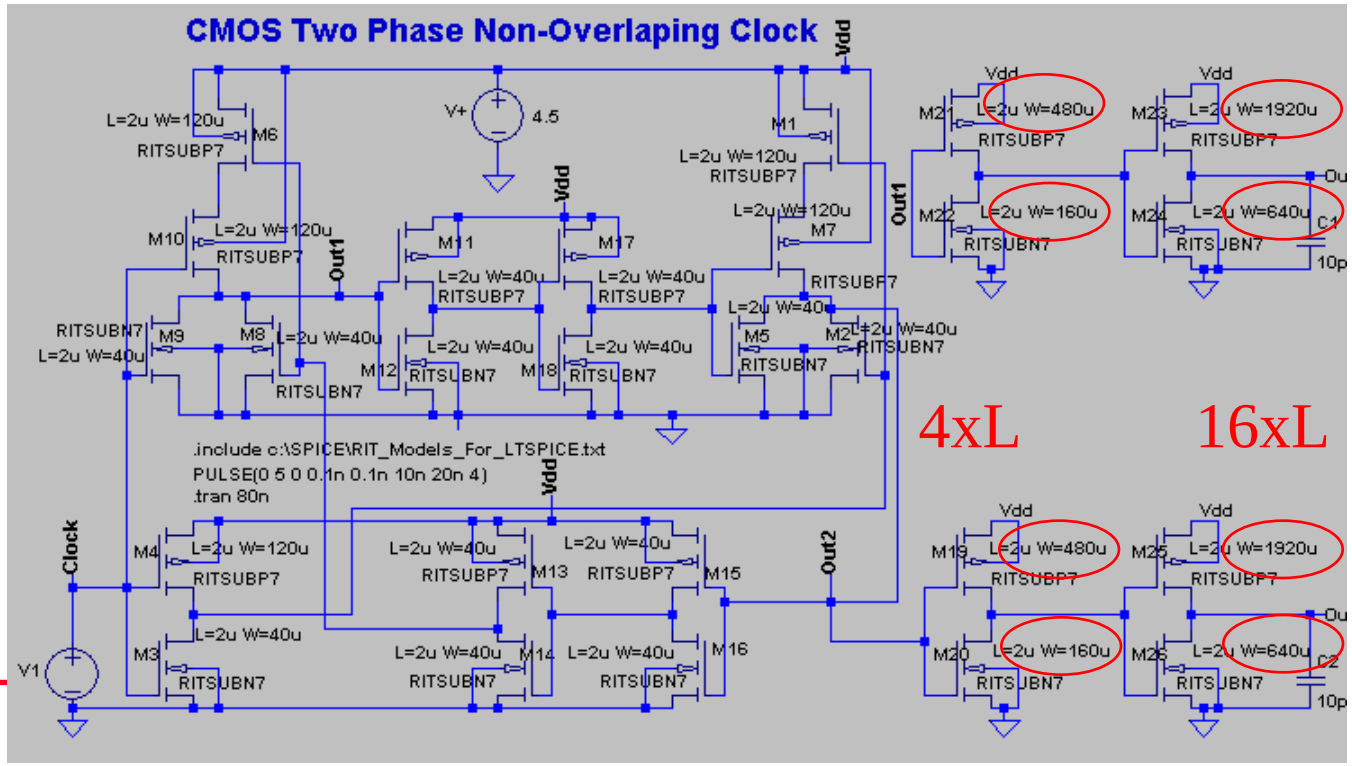
SIMULATION NON-OVERLAPPING CLOCK + BUFFERS



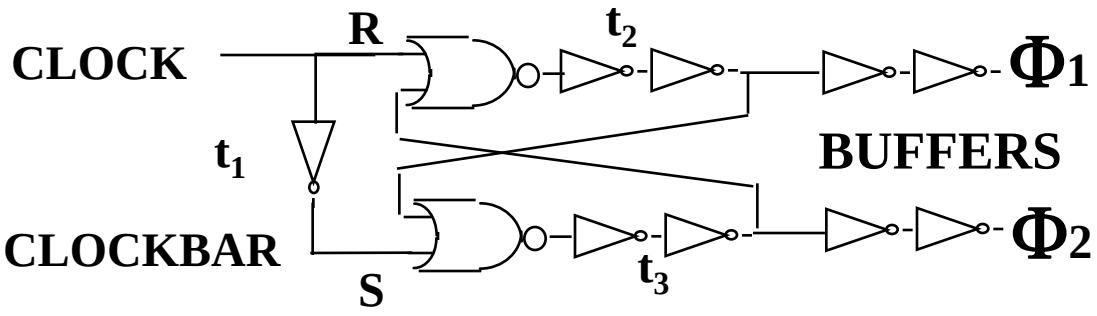


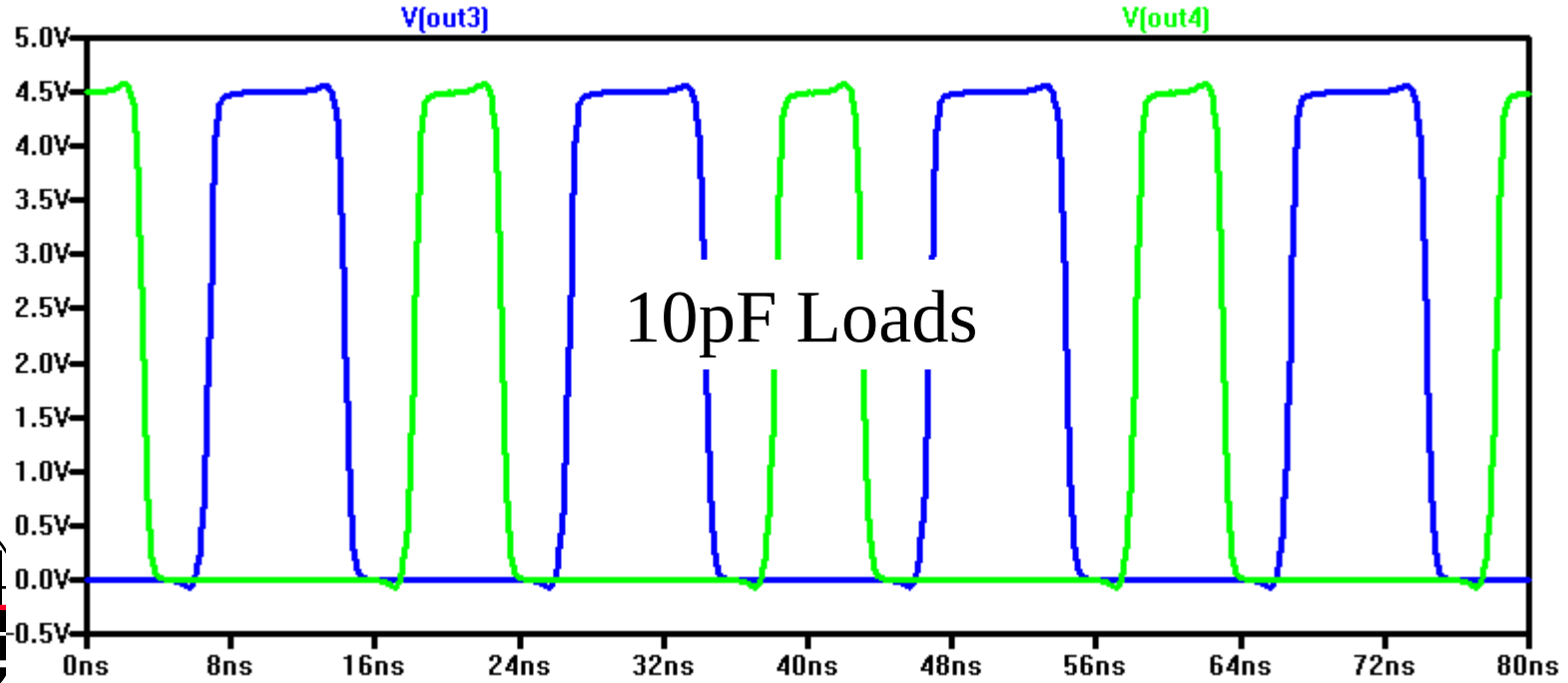
SIMULATION NON-OVERLAPPING CLOCK + BUFFERS





SIMULATION NON-OVERLAPPING CLOCK + BUFFERS

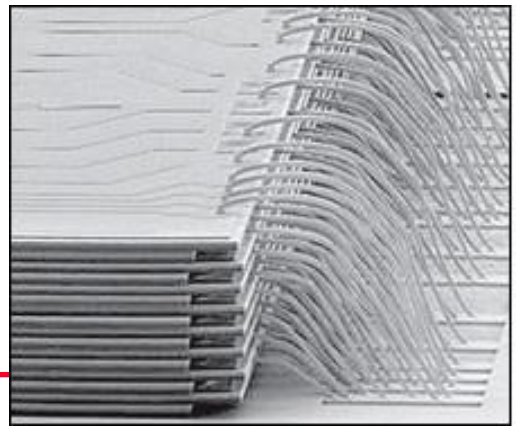


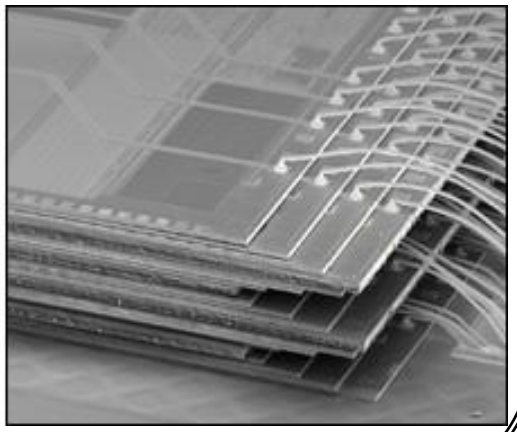


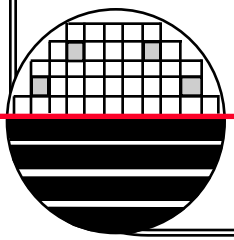
CMOS TRISTATE INPUT OUTPUT PAD

The Input/Output/Tristate Pad is the interface between the chip and the rest of the system. The pad is typically connected via a printed circuit board (PCB) to other chips, other PCB's, and other devices.

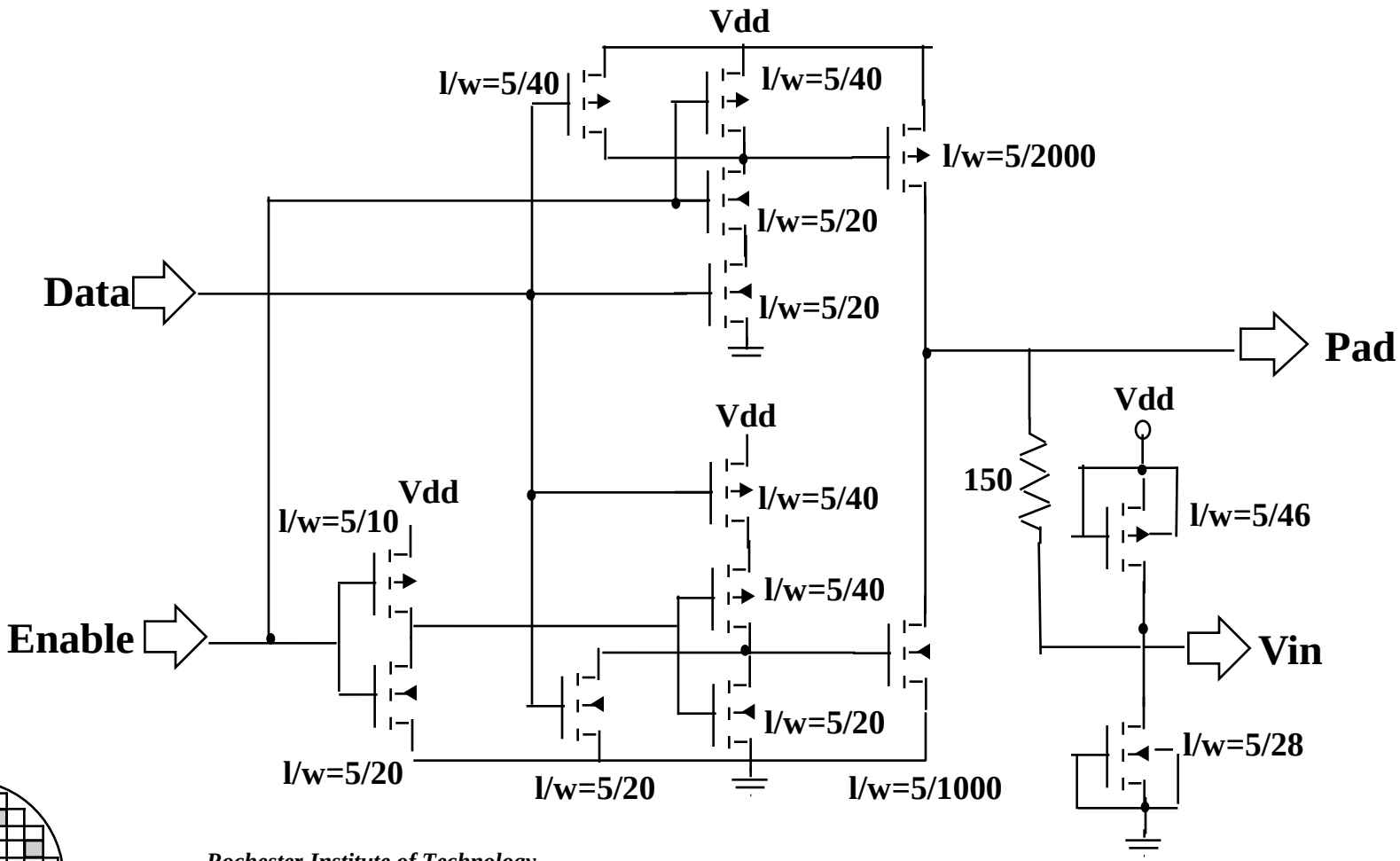
If an oscilloscope probe is connected to a chip it represents a large capacitive load (~10pF) in parallel with a 1MEG or 10MEG resistor. If the chip is connected in parallel with other chips (as is done in memory) via a data bus it represents a large capacitive load to the chip. In the case of a data bus the pad could be for an input or an output signal or high impedance (thus Tri State) Also, these pads are subject to possible electrostatic discharge (ESD) as connections are made to the pads.



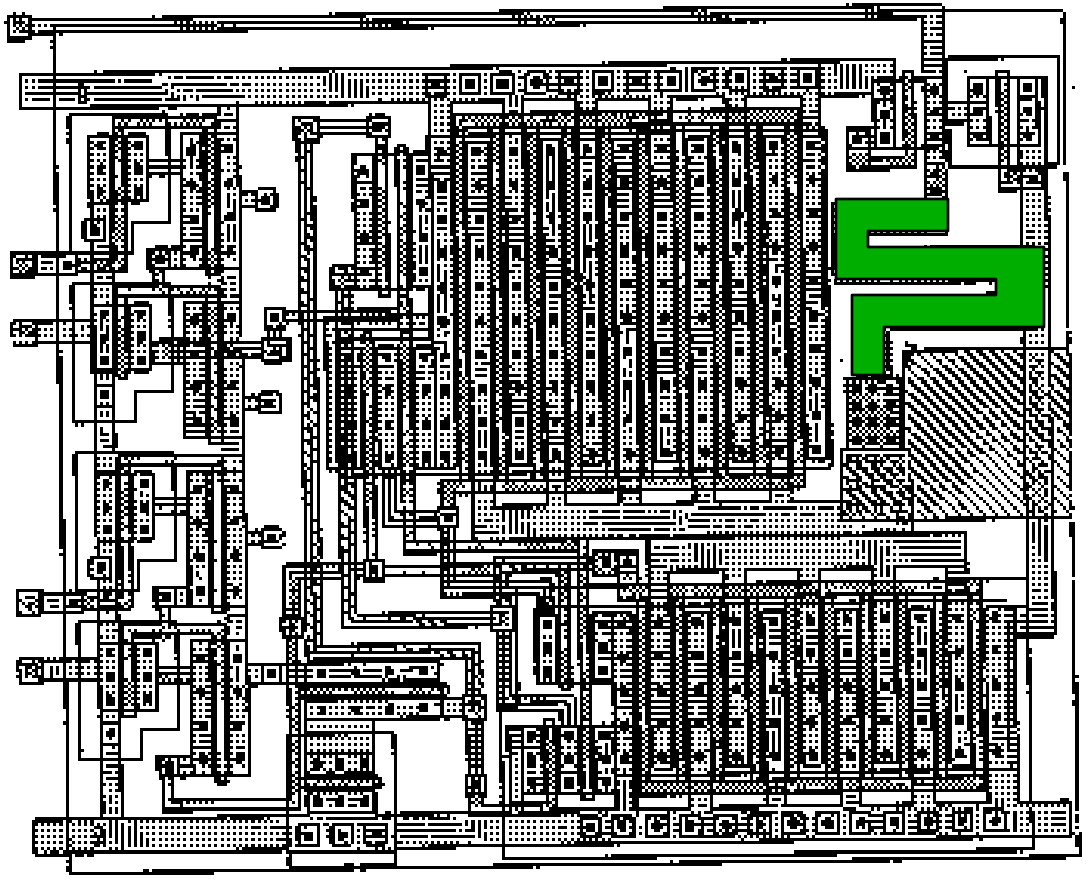




TRISTATE I/O PAD WITH ESD PROTECTION - SCHEMATIC



TRISTATE I/O PAD WITH ESD PROTECTION - LAYOUT

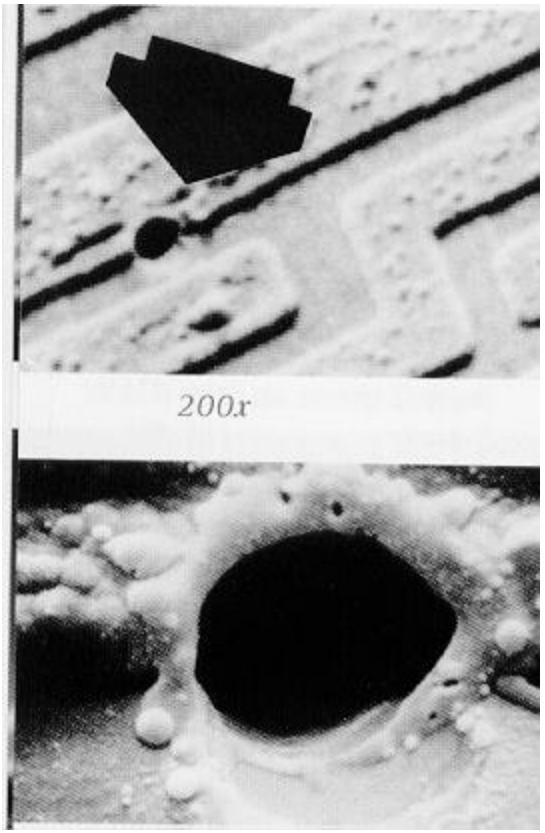


ELECTROSTATIC DISCHARGE

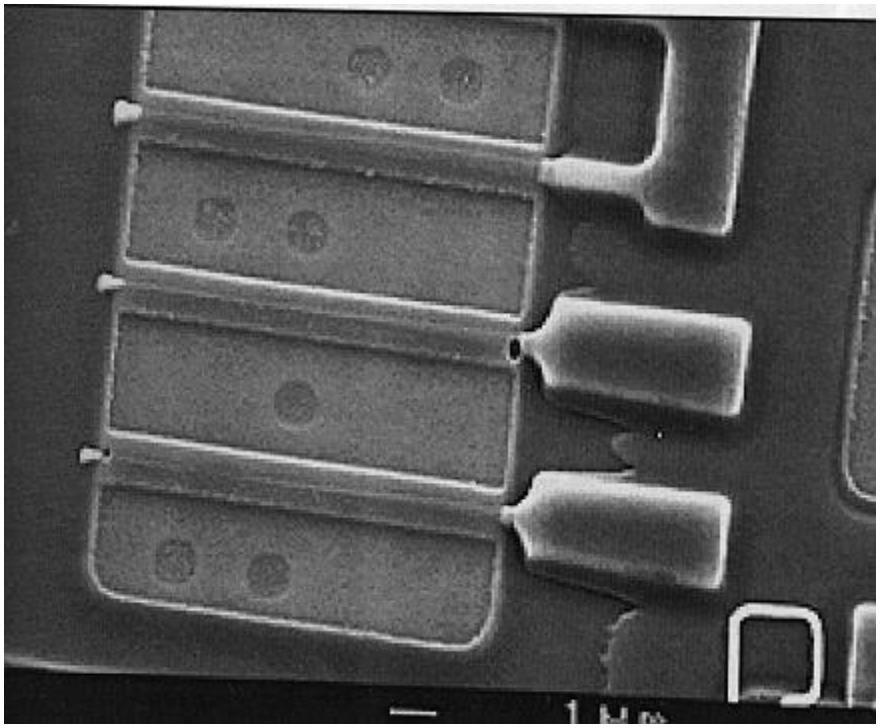
Electrostatic Discharge (ESD)

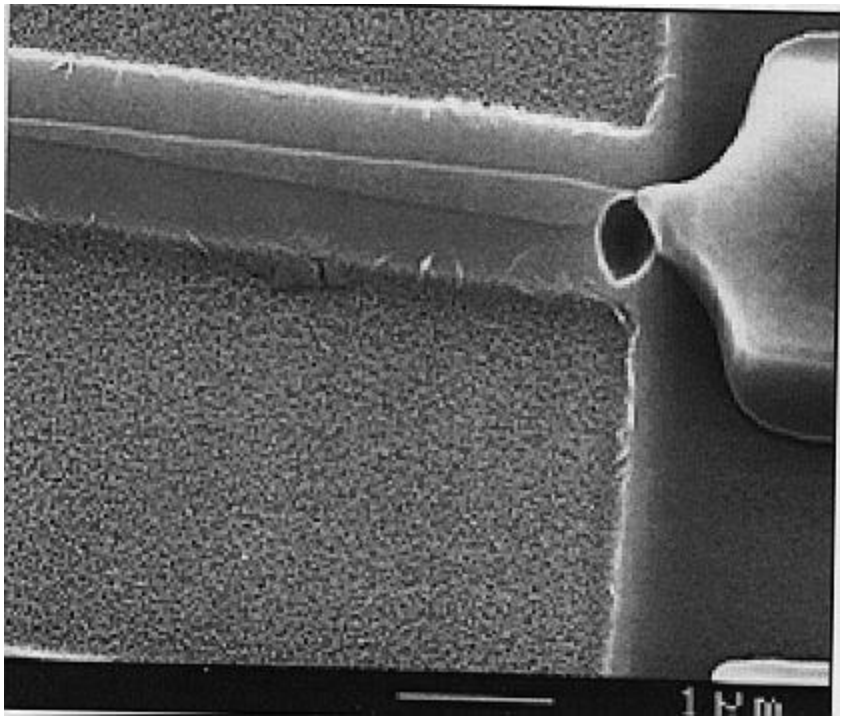
Dielectric Breakdown Strength of SiO2 is approximately 8 E6 V/cm, thus a 250 Å gate oxide will not sustain voltages in excess of 20 V

Triboelectricity (electricity produced by rubbing two materials together) can generate high voltages. A person walking across a room can generate 20,000 Volts and if discharged into an IC can cause immediate failure or damage that will reduce operating life. Even with proper handling several hundred volts can be applied to the IC. Therefore, protection circuitry is needed to provide a safe path for discharge of this electricity.

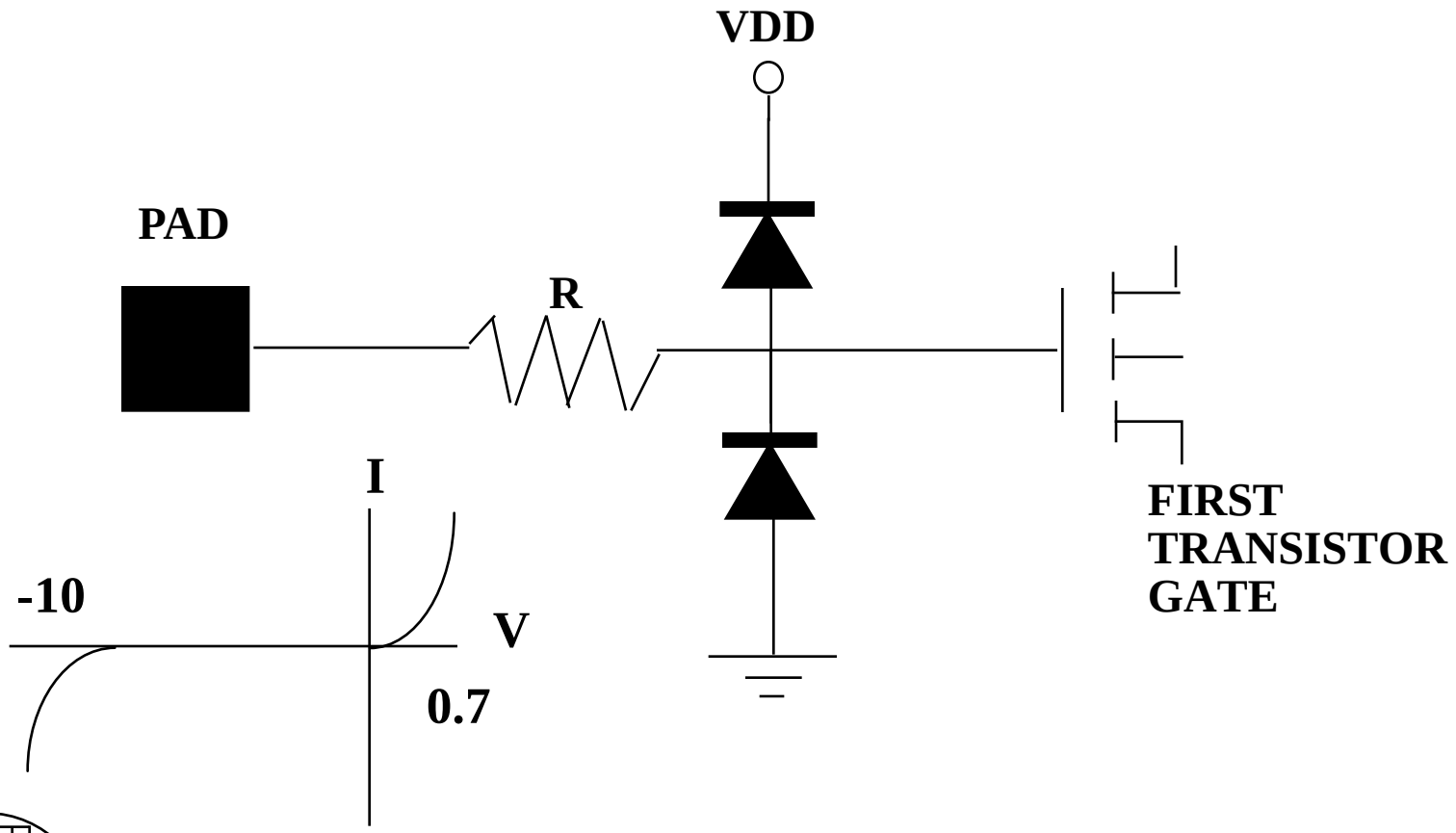


ESD DAMAGE



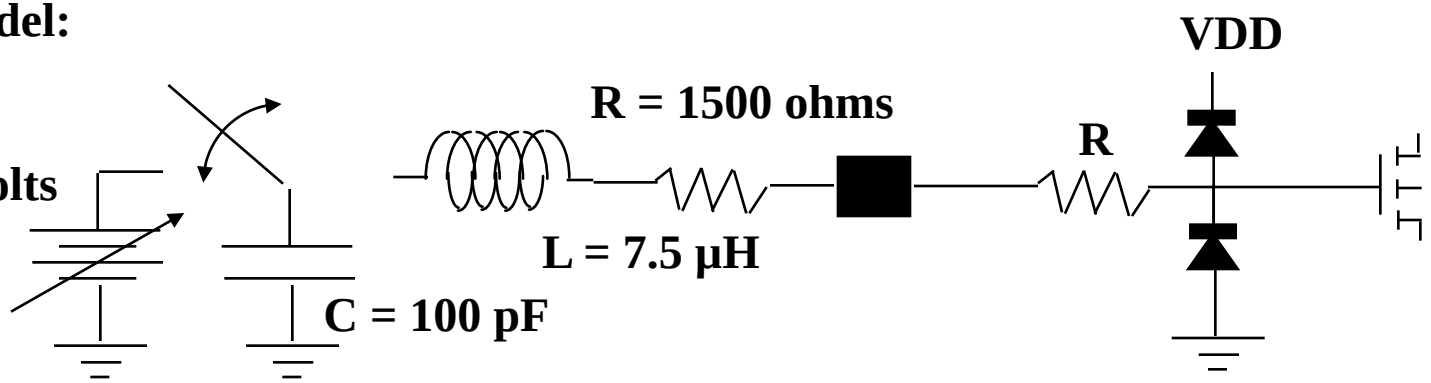


ELECTROSTATIC DISCHARGE - PROTECTION CIRCUITRY

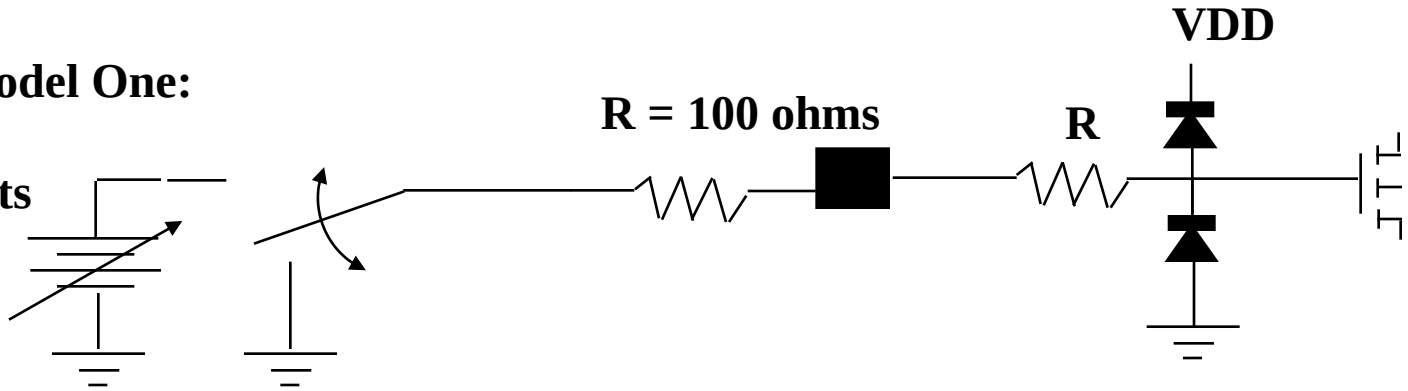


ELECTROSTATIC DISCHARGE - MODEL

Human Model:



Machine Model One:

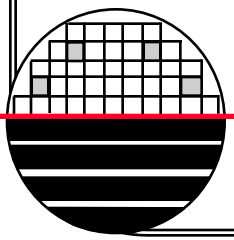


Machine Model Two
L = 1.0 µH
C = 200 pF
R = 10 ohms

Charged Device Model
L = 50 nH
C = 10 pF
R = 1 ohms

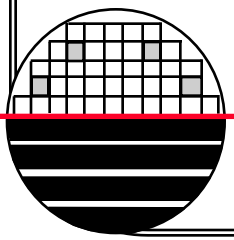
REFERNCES

1. Hodges Jackson and Saleh, Analysis and Design of Digital Integrated Circuits, Chapter 4.
2. Sedra and Smith, Microelectronic Circuits, Sixth Edition, Chapter 13.
3. Dr. Fuller's Lecture Notes, http://people.rit.edu/lffeee



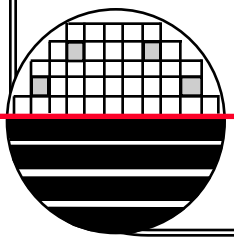
HOMEWORK – HIGH SPEED LOGIC

1. Investigate a 100nm ring oscillator. Does the number of stages change the period of oscillation, explain. Does the number of stages change the inverter gate delay, td, explain. Does the size of the transistors affect the period of oscillation, explain. Does the supply voltage, VDD, affect the period of oscillation, explain. Does the temperature affect the period of oscillation, explain.
2. Use SPICE to illustrate some of the questions in problem 1.
3. The simple hand calculation for inverter gate delay, td, uses Resistors to represent the PMOS and NMOS transistors and capacitors to represent the gate self capacitance and input capacitance. Assume the wiring capacitance is zero. How are the resistors and capacitors different for 1um technology compared to 100nm technology. Provide approximate values for the resistors and capacitors for both technologies.



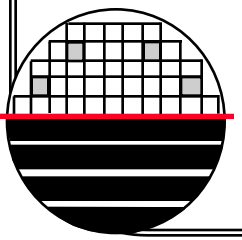
HOMEWORK – HIGH SPEED LOGIC

4. Pro 4
5. Pro 5
6. Pro 6



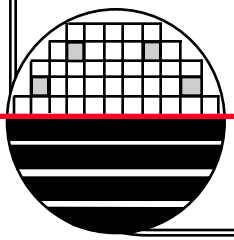
SPICE MODELS FOR MOSFETS

```
*SPICE MODELS FOR RIT DEVICES - DR. LYNN FULLER 4-10-2014
*LOCATION DR.FULLER'S WEBPAGE - http://people.rit.edu/lffeee/CMOS.htm
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=1u W=200u
.MODEL RIT4007N7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=1u W=200u
.MODEL RIT4007P7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



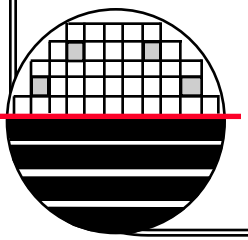
SPICE MODELS FOR MOSFETS

```
*Used for ALD1103 chips
*Note: Properties L=10u W=880u
.MODEL RITALDN3 NMOS (LEVEL=3
+TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0= 1215 VTO=0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5
+NSUB=1.57E16 XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)
*
*Used for ALD1103 chips
*Note: Properties L=10u W=880u
.MODEL RITALDP3 PMOS (LEVEL=3
+TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0=550 VTO=-0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5
+NSUB=1.57E16 XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)
```



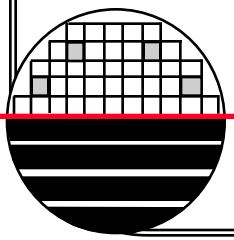
SPICE MODELS FOR MOSFETS

```
*4-4-2013 LTSPICE uses Level=8
*For RIT Sub-CMOS 150 process with L=2u
.MODEL RITSUBN8 NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013  LTSPICE uses Level=8
*For RIT Sub-CMOS 150 process with L=2u
.MODEL RITSUBP8 PMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



SPICE MODELS FOR MOSFETS

```
* From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL RITSUBP7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



SPICE MODELS FOR MOSFETS

```
*4-4-2013  LTSPICE uses Level=8
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSN     NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013  LTSPICE uses Level=8
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSP     PMOS (LEVEL=8
+TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
```