ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Introduction to Digital Electronics

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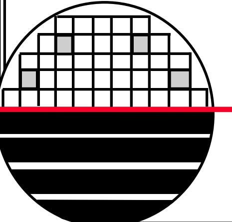

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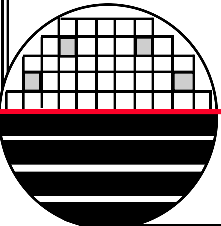

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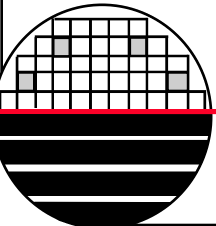
OUTLINE

Brief History of IC Industry
Basic Logic Functions
Logic (Really Continuous Signals)
VTC and Noise Margin
Transient Characteristics
Power Dissipation
Digital Circuit Design
PMOS, NMOS, CMOS
CAD, VLSI
Standard Cell Design
System on a Chip (SOC)
Challenges Ahead
References
Homework



INTRODUCTION

Industry rankings not including foundries

Rank 2012	Rank 2011	Rank 2010	Rank 2009	Company	Country of origin	Revenue (million $ USD)	2012/2011 changes	Market share
1	1	1	1	Intel Corporation	United States	$47,543	-2.4%	15.7%
2	2	2	2	Samsung Electronics	South Korea	$30,474	+6.7%	10.1%
3	6	9	6	Qualcomm	United States	$12,976	+27.2%	4.3%
4	3	4	4	Texas Instruments	United States	$12,008	-14.0%	4.0%
5	4	3	3	Toshiba Semiconductors	Japan	$10,996	-13.6%	3.6%
6	5	5	9	Renesas Electronics (1)	Japan	$9,430	-11.4%	3.1%
7	8	6	7	Hynix	South Korea	$8,462	-8.9%	2.8%
8	7	7	5	STMicroelectronics	France / Italy	$8,453	-13.2%	2.8%
9	10	10	14	Broadcom	United States	$7,840	+9.5%	2.6%
10	9	8	13	Micron Technology (2)	United States	$6,955	-5.6%	2.3%

Source : iSuppli Corporation supplied rankings for 2010 (Semiconductor foundries are excluded)

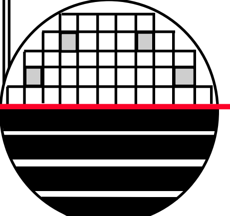
Total $304B in 2010

TSMC AND GLOBAL FOUNDRIES

TSMC, Tiwan
http://www.tsmc.com/english/default.htm

Global Foundries, Malta, New York
http://www.globalfoundries.com/
http://www.globalfoundries.com/manufacturing/fab-8-overview

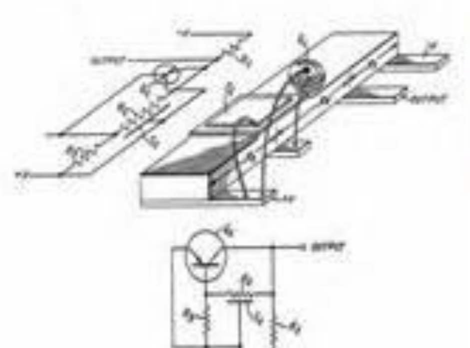
Go to these web locations and explore, watch some videos, etc.



JACK KILBY AND ROBERT NOYCE

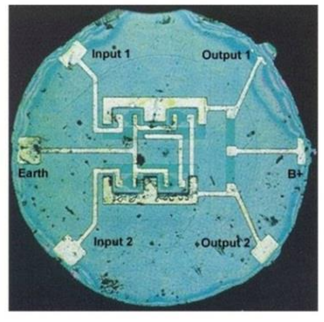
The First (2D) Integrated Circuit
Jack Kilby, Texas Instruments, 1958

- Transistor, Resistors and Capacitors on the same piece of semiconductor
- Interconnects between components not integrated
  → Low connectivity between components

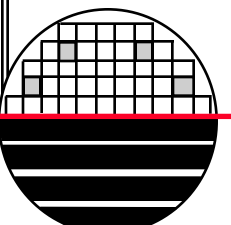


The First *Monolithic* (2D) Integrated Circuit
Robert Noyce, Fairchild Semiconductor, 1961

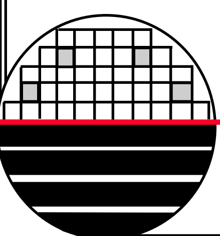
- Transistor, Resistors and Capacitors on the same piece of semiconductor
- Interconnects between components integrated
  → High connectivity between components



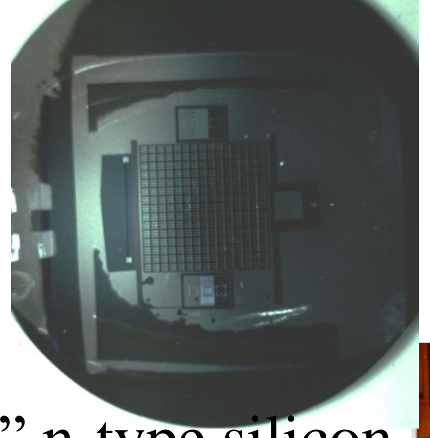
Nobel Prize in Physics 2001



JACK KILBY AT RIT 1986

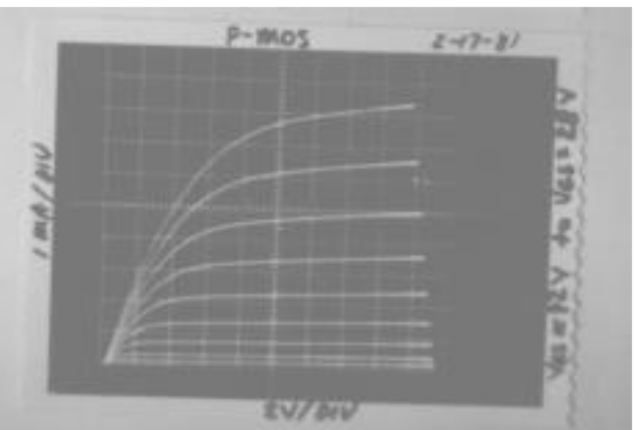


FIRST TRANSISTORS MADE AT RIT 1981

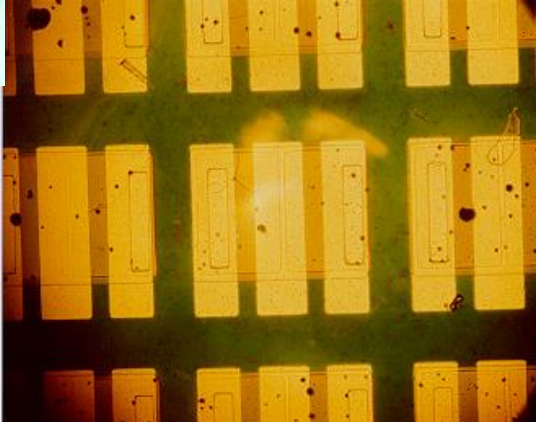


2” n-type silicon wafer

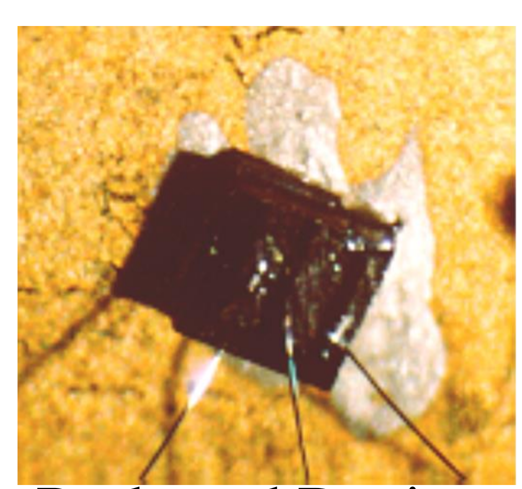
Vt = 12 volts



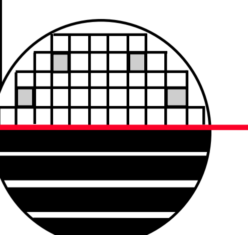
2-17-81
Rob Pearson
Jim Radak



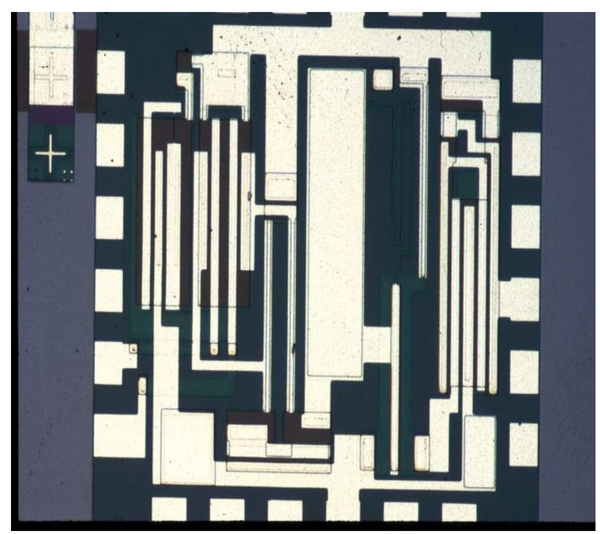
PMOS Transistors



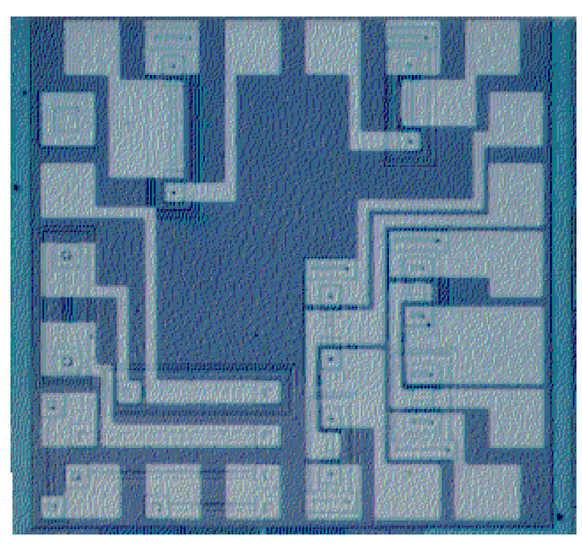
Packaged Device
Aluminum wire bonds



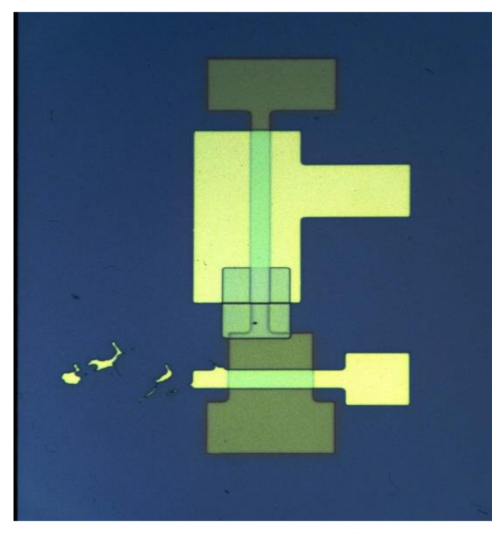
FIRST INTEGRATED CIRCUITS MADE AT RIT



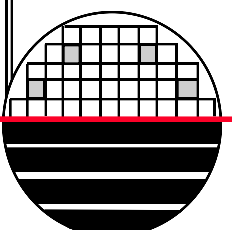
Jonathan Littlehale
All PMOS Op Amp
1985



Jim Pollard Metal
Gate CMOS
1987



Dr. Lane's
Thin Films Class
NMOS Inverter
1990's



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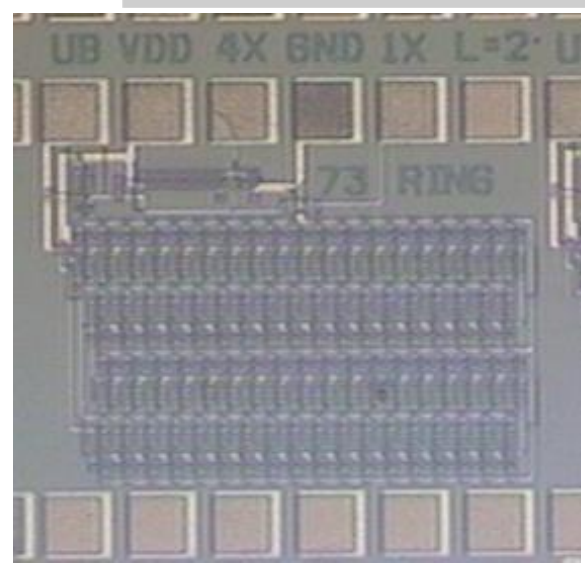
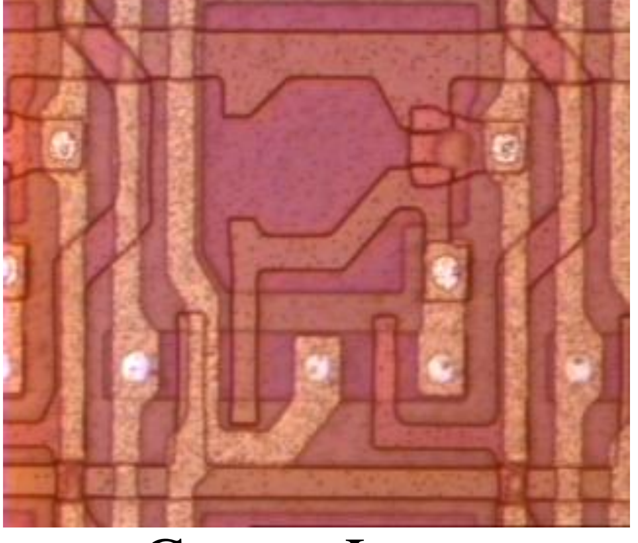
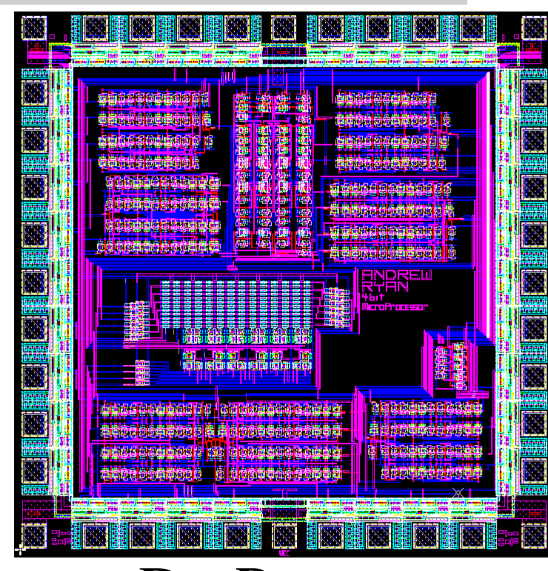
FIRST INTEGRATED CIRCUITS MADE AT RIT



Rob Saxer
2µm 73 Stage CMOS
Ring Oscillator
2000

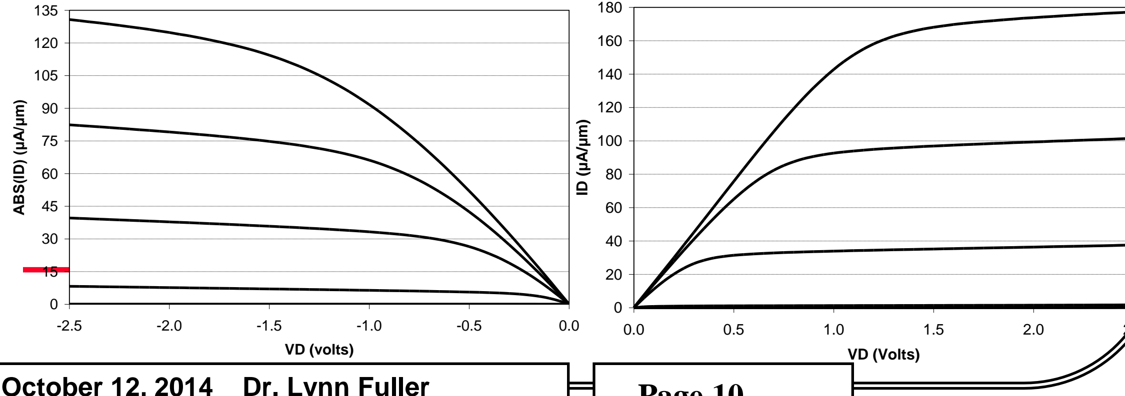


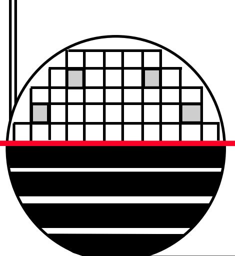
George Lungu
10,000 Pixel Imager
1999



Dr. Pearson
4-Bit Microprocessor
2005

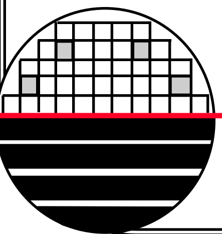
Mike Aquilino
250 nm CMOS
MOSFETS, 2006





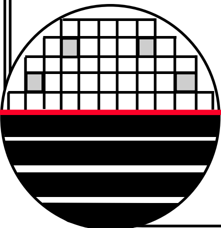
PROCESS TECHNOLOGY

Process Technology



PROCESS SELECTION

It is not necessary to know all process details to do CMOS integrated circuit design. However the process determines important circuit parameters such as supply voltage and maximum frequency of operation. It also determines if devices other than PMOS and NMOS transistors can be realized such as poly-to-poly capacitors and EEPROM transistors. The number of metal interconnect layers is also part of the process definition. Starting wafer type determines if isolated n-wells or p-wells are available.



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RIT PROCESSES

At RIT we use the Sub-CMOS and ADV-CMOS processes for most designs. In these processes the minimum poly length is 1µm and 0.5µm respectively. We use scalable MOSIS design rules with lambda equal to 0.5µm and 0.25µm. These processes use one layer of poly and two layers of metal.

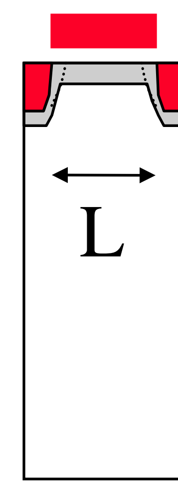
The examples on the following pages are designs that could be made with either of the above processes. As a result the designs are generous, meaning that larger than minimum dimensions are used. For example $\lambda = 0.5\mu m$ and minimum poly is 2λ which would result in transistor gate length of 1µm but are designed at 2µm for higher yield.

The design approach for digital circuits is to design primitive cells and then use the primitive cells to design basic cells which are then used in the project designs. A layout approach is also used that allows for easy assembly of these cells into more complex cells.

RIT SUBμ CMOS

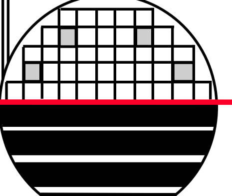
RIT Subμ CMOS

150 mm wafers
Nsub = 1E15 cm-3
Nn-well = 3E16 cm-3
Xj = 2.5 μm
Np-well = 1E16 cm-3
Xj = 3.0 μm
LOCOS
Field Ox = 6000 Å
Xox = 150 Å
Lmin= 1.0 μm
LDD/Side Wall Spacers
2 Layers Aluminum



Long
Channel
Behavior

3.3 Volt Technology
VT's = +/- 0.75 Volt
Robust Process (always works)
Fully Characterized (SPICE)



RIT SUBμ CMOS

NMOSFET

PMOSFET

N+ Poly

5000 Å
Field Oxide

p+ well
contact

N+ D/S

LDD

P-well

N-well

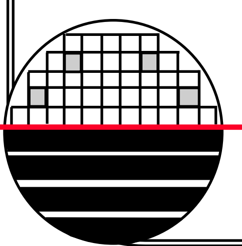
LDD

P+ D/S

n+ well
contact

Channel Stop

Substrate 10 ohm-cm



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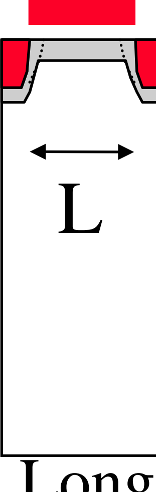
RIT ADVANCED CMOS VER 150

RIT Advanced CMOS

150 mm Wafers
Nsub = 1E15 cm-3 or 10 ohm-cm, p
Nn-well = 1E17 cm-3
Xj = 2.5 µm
Np-well = 1E17 cm-3
Xj = 2.5 µm
Shallow Trench Isolation
Field Ox (Trench Fill) = 4000 Å
Dual Doped Gate n+ and p+
Xox = 100 Å
Lmin = 0.5 µm , Lpoly = 0.35 µm, Leff = 0.11 µm
LDD/Nitride Side Wall Spacers
TiSi2 Salicide
Tungsten Plugs, CMP, 2 Layers Aluminum



Long Channel Behavior

Vdd = 3.3 volts
Vto=+- 0.75 volts

RIT ADVANCED CMOS

NMOSFET

PMOSFET

N+ Poly

P+ Poly

p+ well
contact

N+ D/S

LDD

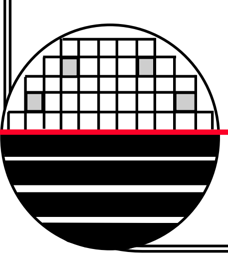
P-well

N-well

LDD

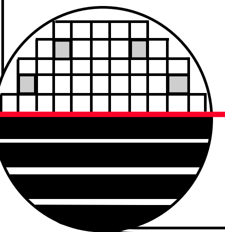
P+ D/S

n+ well
contact



DIGITAL ELECTRONICS

Digital Electronics



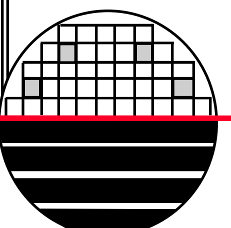
DIGITAL INTEGRATED CIRCUITS

BOOLEAN ALGEBRA IS BASED ON TWO DISCRETE LEVELS CALLED LOW OR HIGH (0 OR 1). (from George Boole, 1815-1864)

BOOLEAN ALGEBRA USES FUNCTIONS SUCH AS “INVERT”, “AND”, “OR” TO EVALUATE INPUTS AND GENERATE “OUTPUTS”.

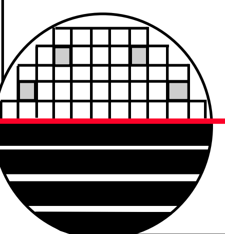
THE TERM “BINARY LOGIC” IS USED TO DESCRIBE DEVICES THAT FOLLOW THE RULES OF BOOLEAN ALGEBRA.

EACH SUB CIRCUIT OR “GATE” SHOULD HAVE ITS INPUTS AND OUTPUTS AT 0 OR 1 (Except Briefly During Switching)



BASIC LOGIC FUNCTIONS

INV, NAND NOR
Truth Tables
Sum of Products, Product of Sums
XOR, XNOR, MUX
Sequential Logic
RS, D, JK, T Flip Flops



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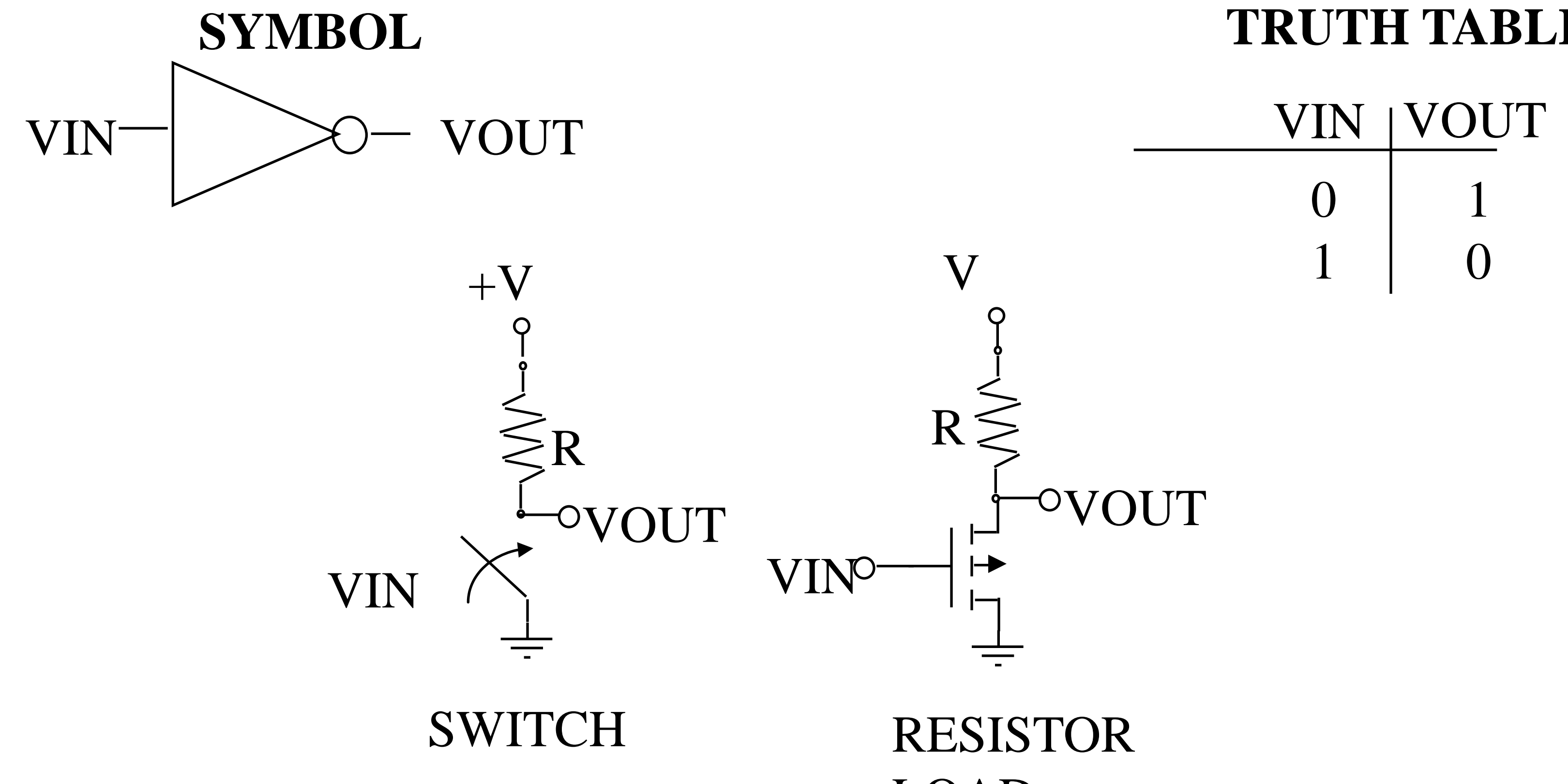
INVERTER



Rochester Institute of Technology
Microelectronic Engineering

VOLTAGE TRANSFER CURVE

VIN VOUT

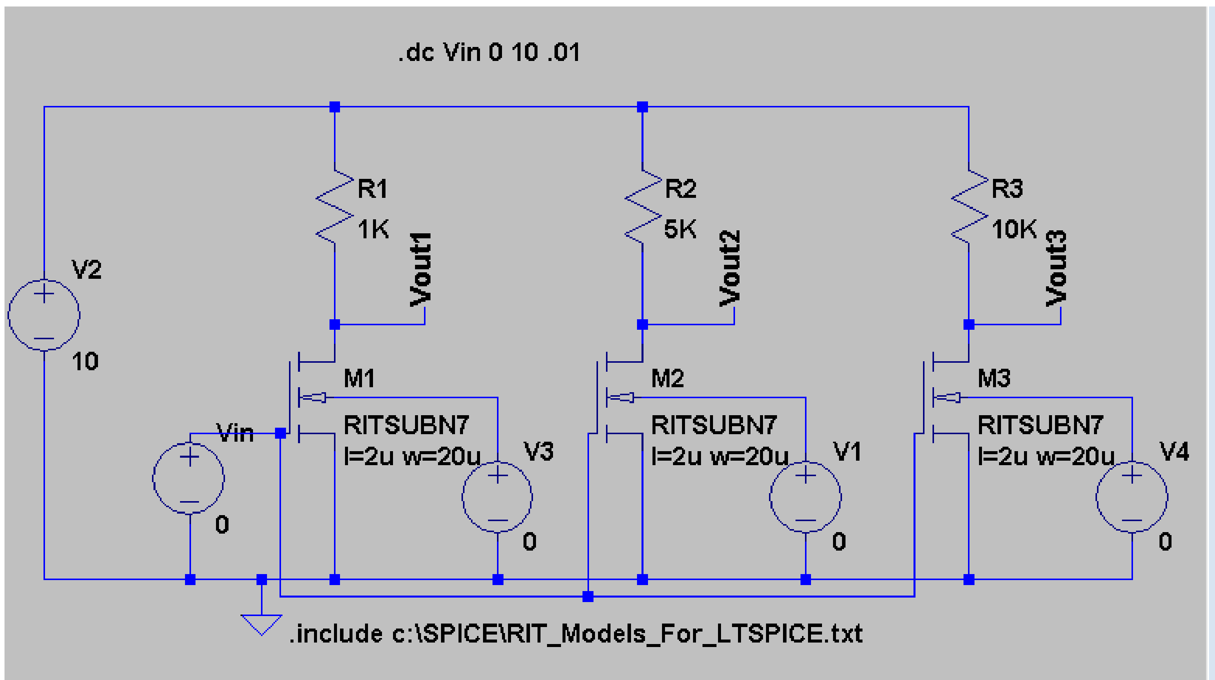
V
R
VOUT
VIN

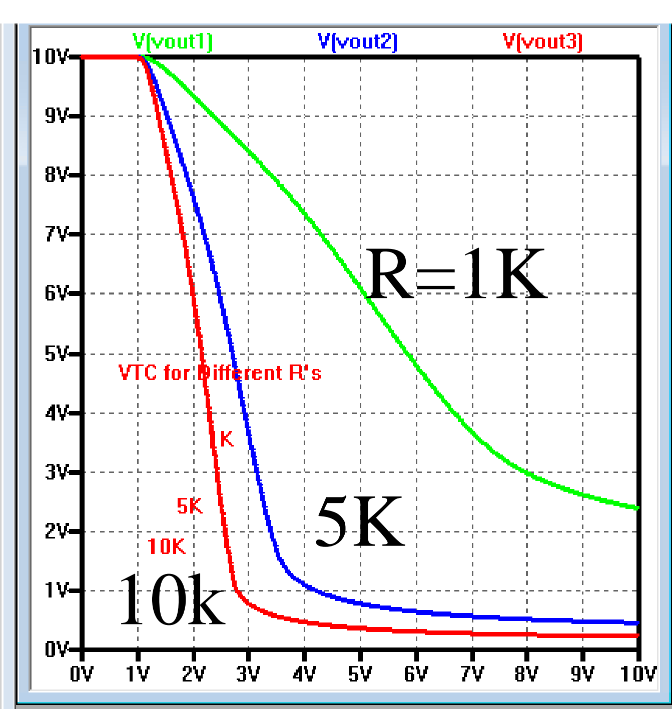
RESISTOR
LOAD

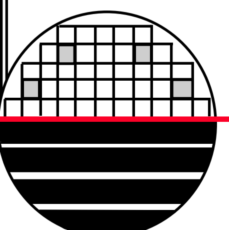
VOUT
+V
Voh
Idd
Slope = Gain
VoL
0
VIN
0
Vinv
ViL
Vih
+V

NML, noise margin low, Δ0 =ViL-VoL
NMH, oise margin high, Δ1 =VoH-ViH

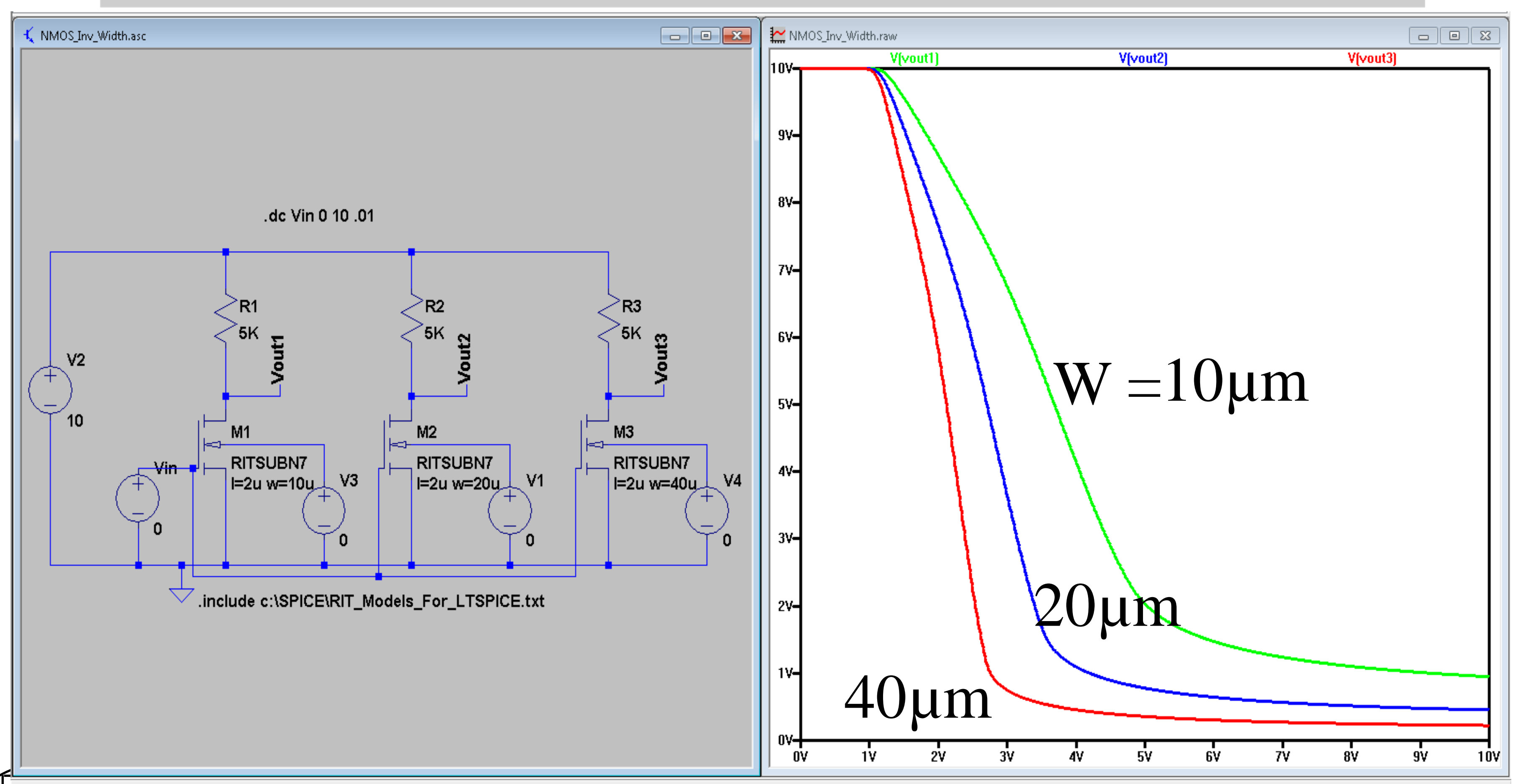
LTSPICE - INVERTER VTC – FOR DIFFERENT RL



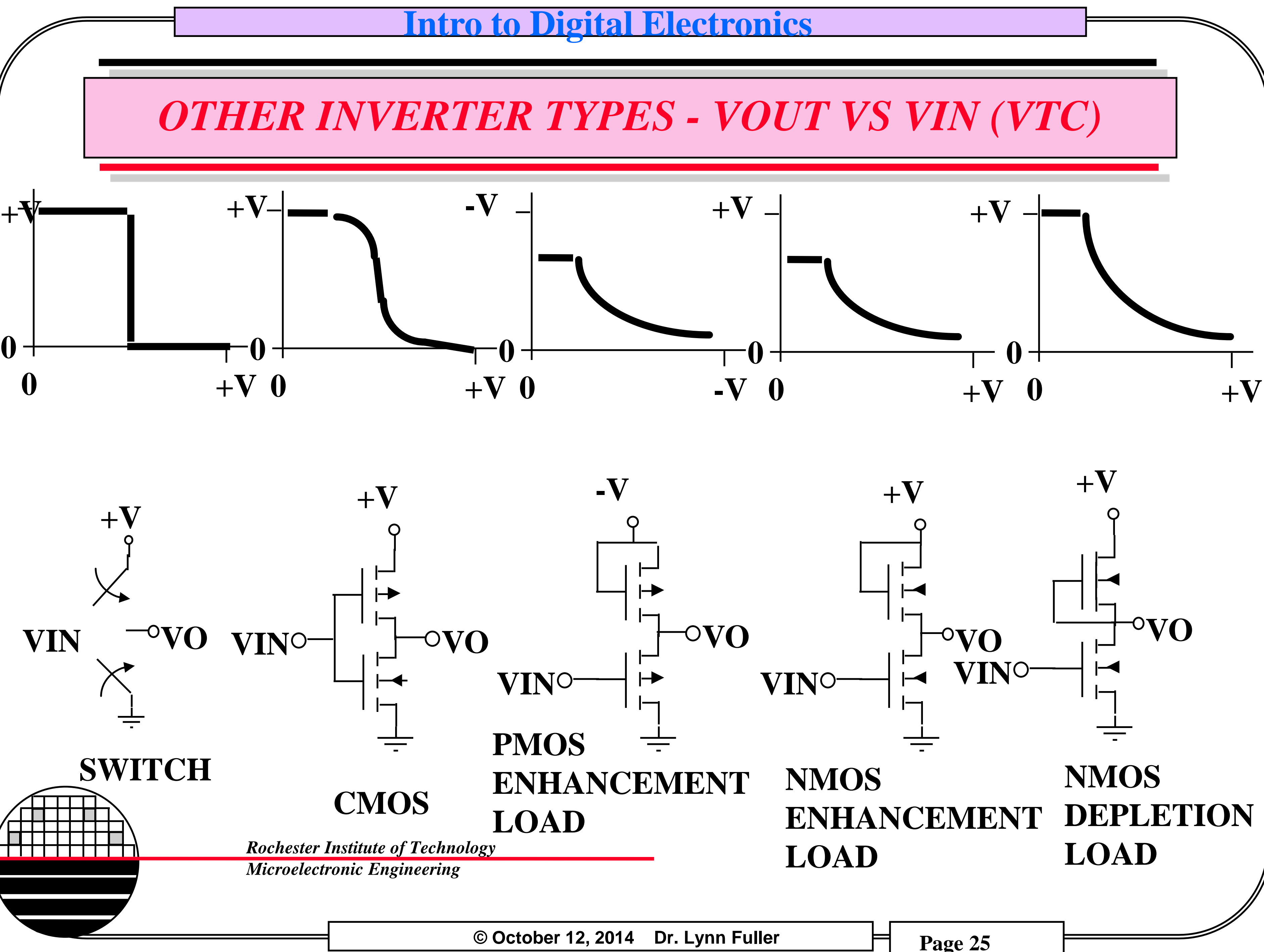




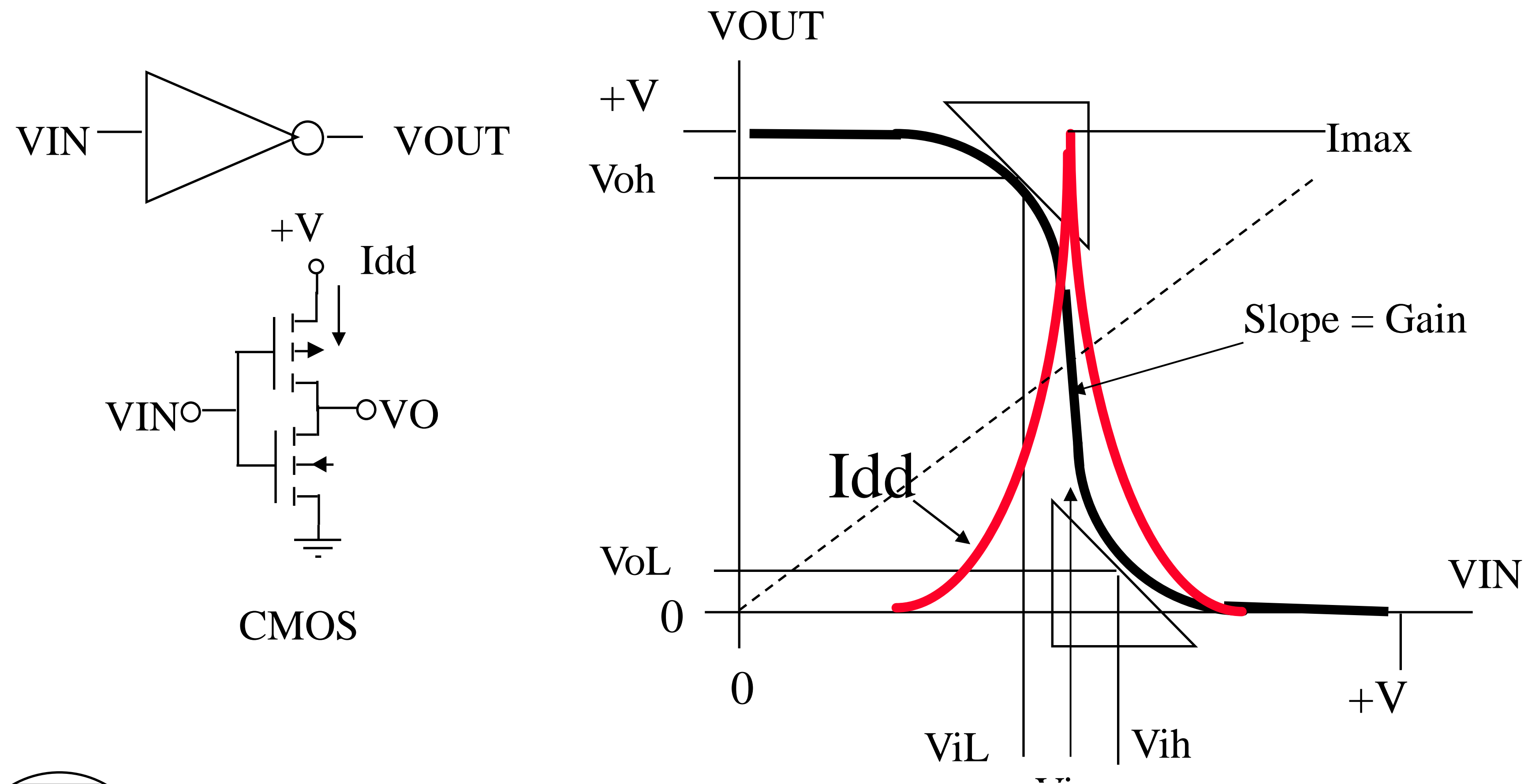
LTSPICE - INVERTER FOR DIFFERENT NMOS W



OTHER INVERTER TYPES - VOUT VS VIN (VTC)

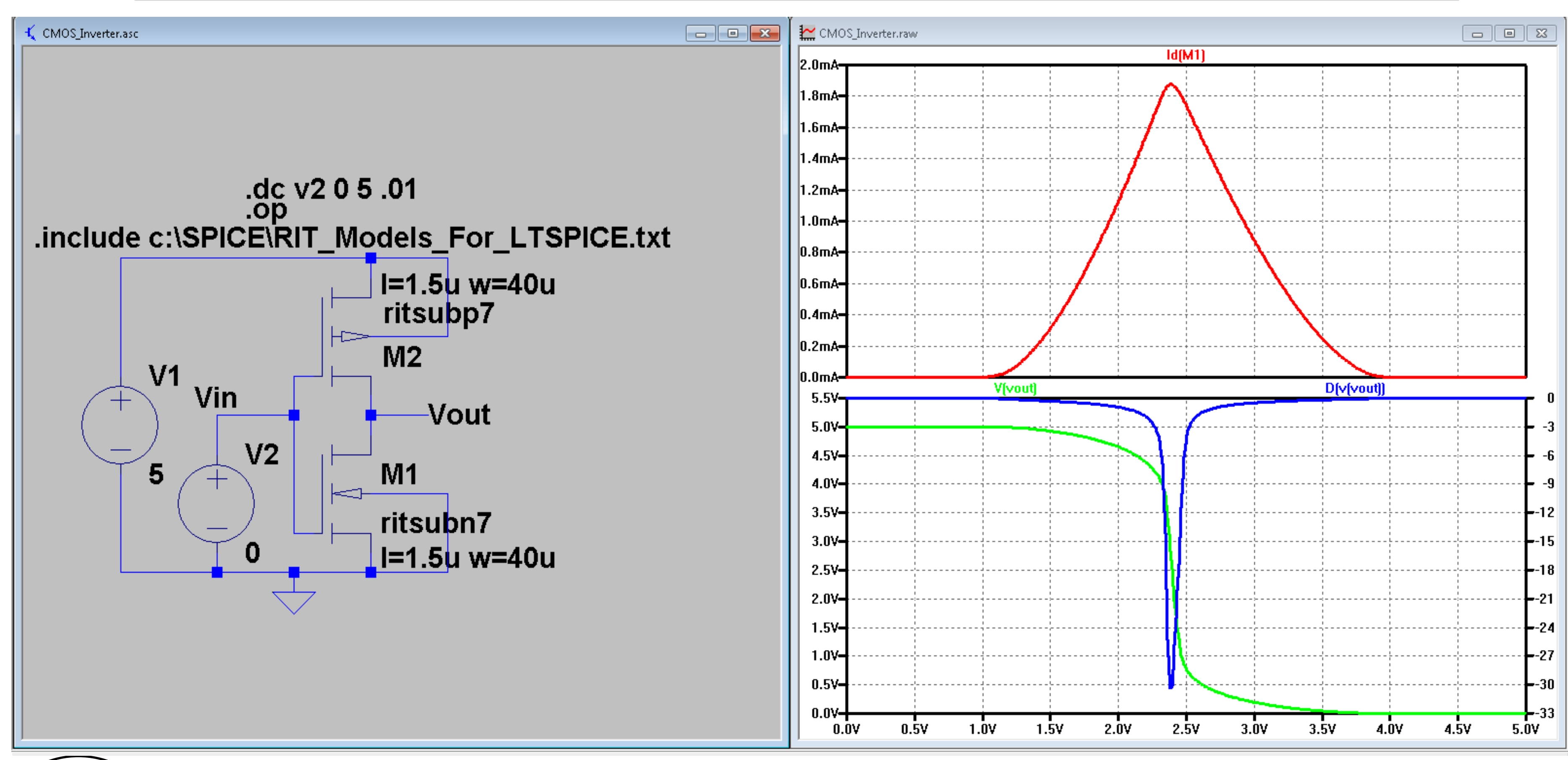


CMOS INVERTER



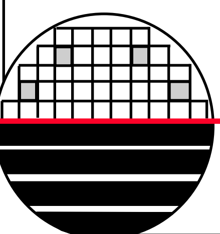
NML, noise margin low, Δ0 =ViL-VoL
NMH, noise margin high, Δ1 =VoH-ViH

LTSPICE – CMOS INVERTER

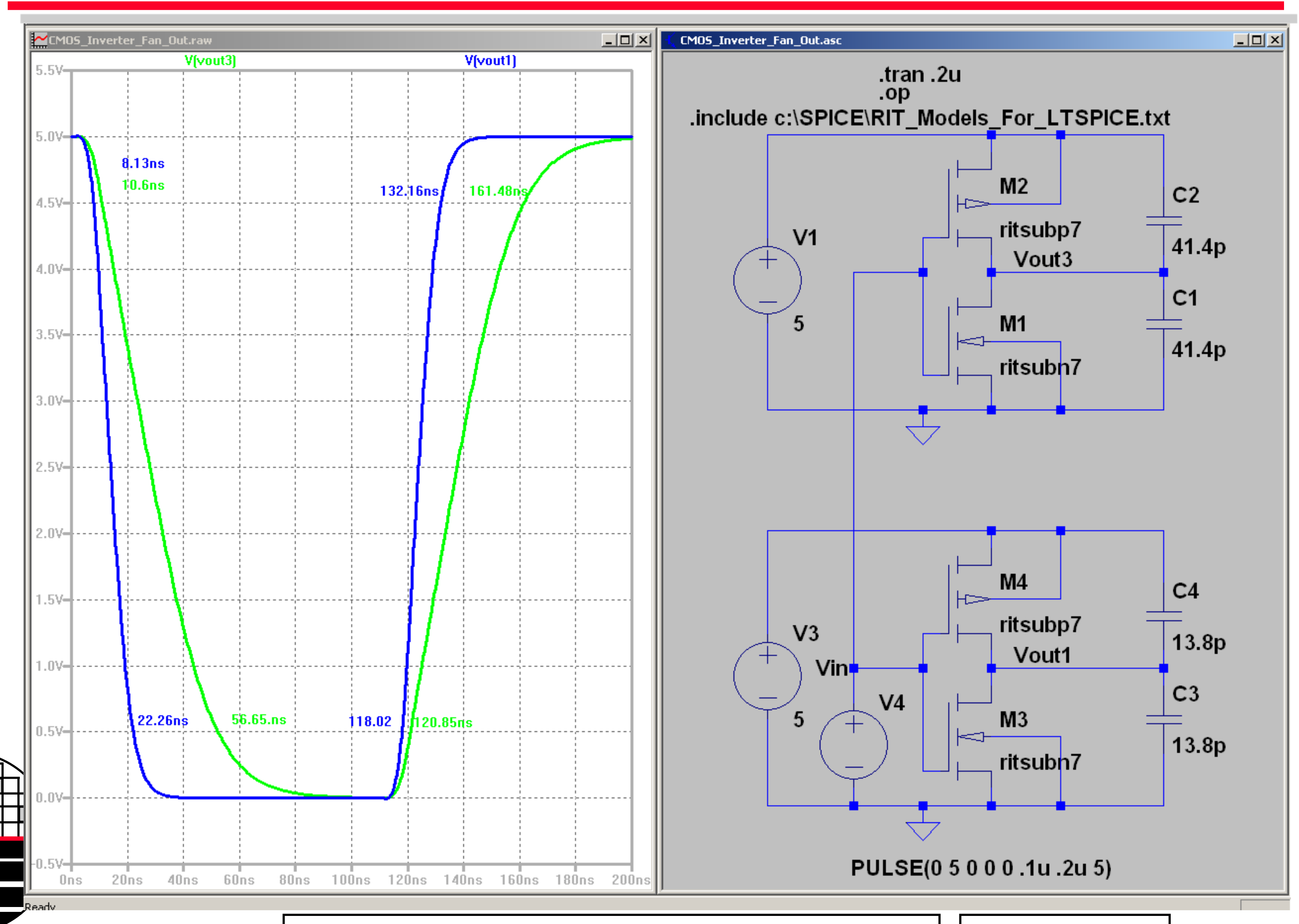


INVERTER PROPERTIES

- DC Properties
  - Noise Margins
  - Current, I
  - Size
- Transient Properties
  - Rise/Fall Time
  - Fan Out

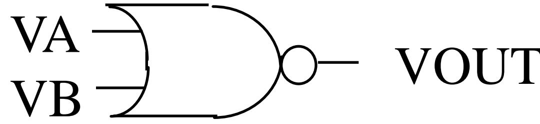


RISE TIME AND FALL TIME LTSPICE SIMULATION



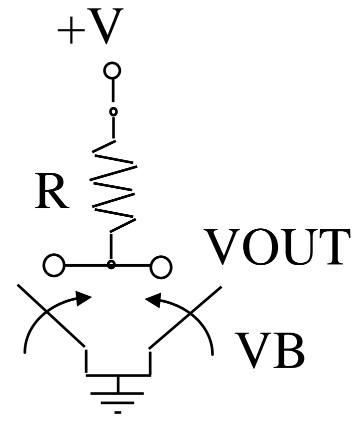
NOR GATE

SYMBOL



TRUTH TABLE

VA	VB	VOUT
0	0	1
0	1	0
1	0	0
1	1	0



SWITCH

V

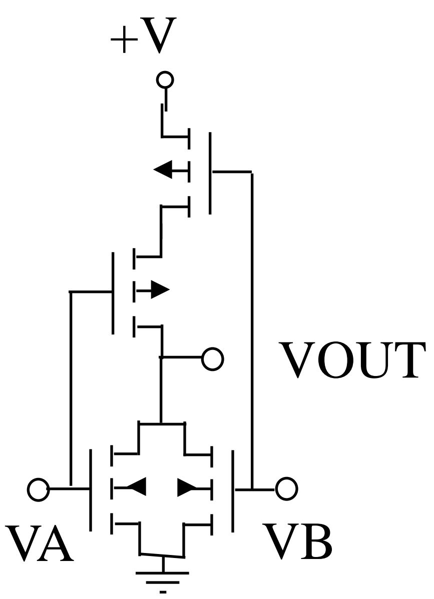
R

VOUT

VA

VB

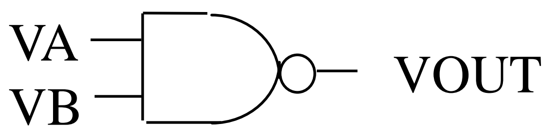
RESISTOR LOAD



CMOS

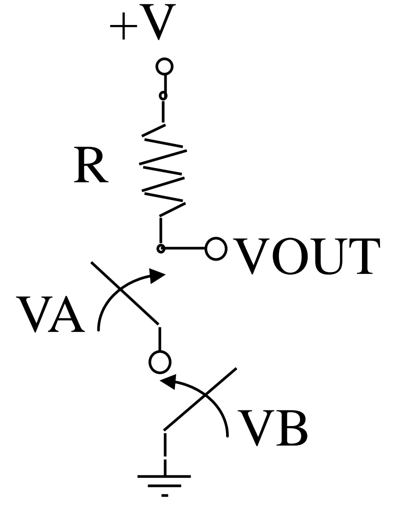
NAND GATE

SYMBOL

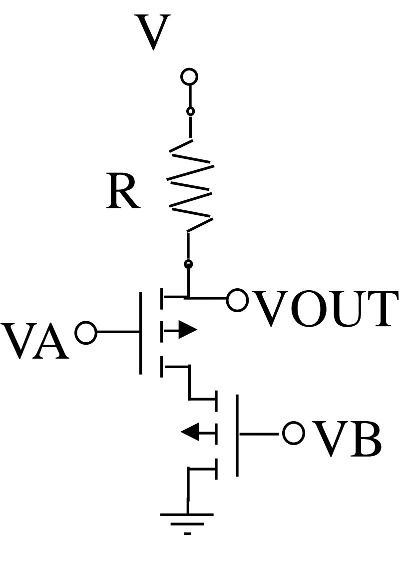


TRUTH TABLE

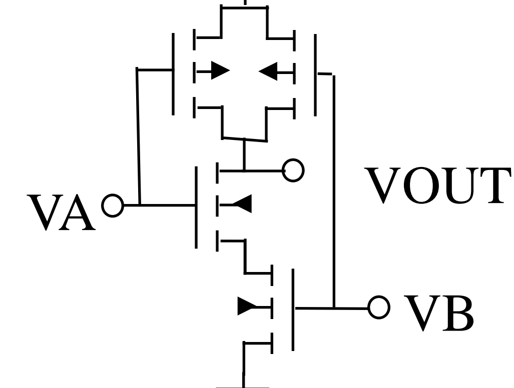
VA	VB	VOUT
0	0	1
0	1	1
1	0	1
1	1	0



SWITCH



RESISTOR LOAD



CMOS

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OTHER LOGIC GATES

AND

VA, VB → VOUT

VA	VB	VOUT
0	0	0
0	1	0
1	0	0
1	1	1

OR

VA, VB → VOUT

VA	VB	VOUT
0	0	0
0	1	1
1	0	1
1	1	1

3 INPUT AND

VA, VB, VC → VOUT

VA	VB	VC	VOUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3 INPUT OR

VA, VB, VC → VOUT

VA	VB	VC	VOUT
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

ADDITION IN BINARY

IN BASE 10

```
  7
 +2
 __
  9
```

IN BINARY

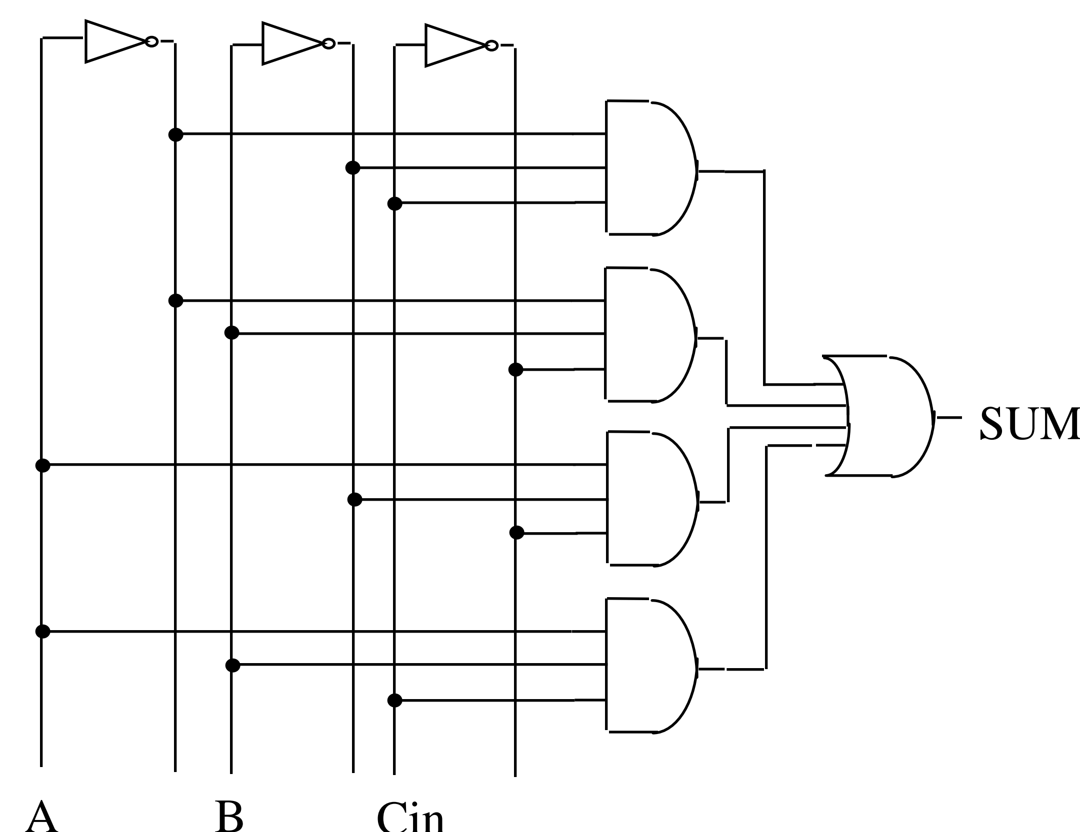
```
  11       CARRY
0111
0010
____
1001       SUM
```

Decimal	Binary
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

TRUTH TABLE FOR ADDITION RULES

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

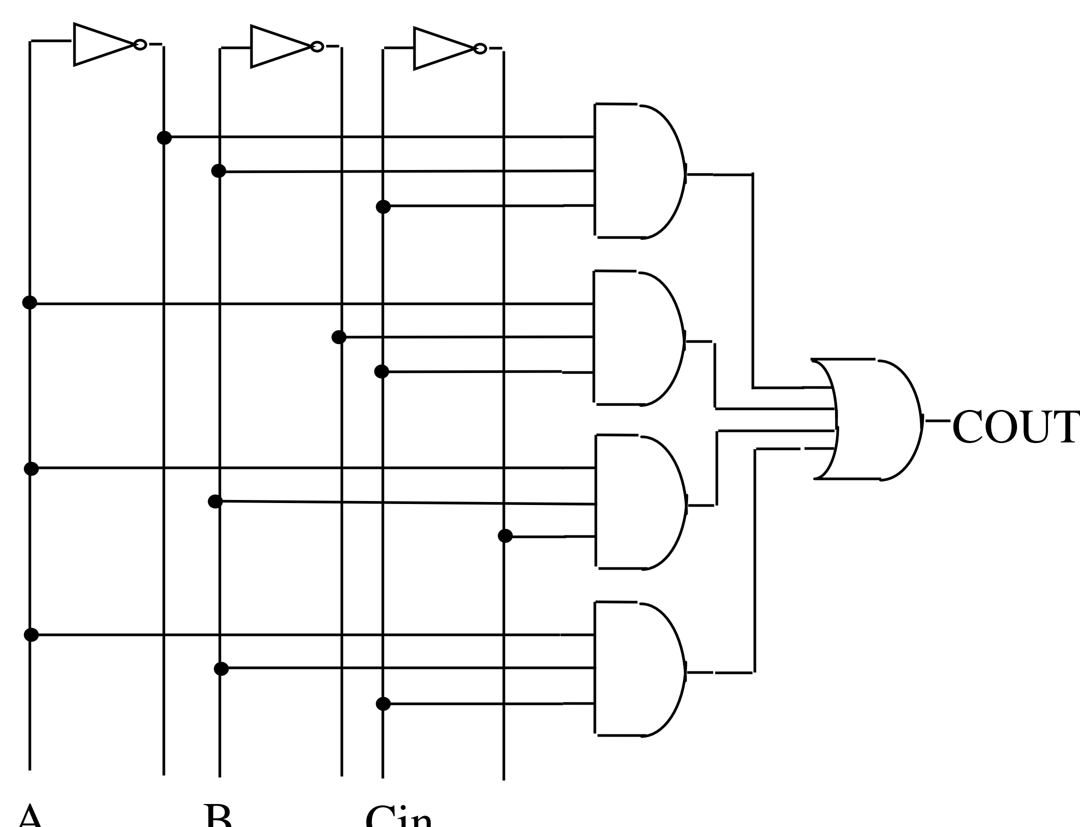
AND-OR CIRCUIT REALIZATION OF SUM



TRUTH TABLE
FOR ADDITION
RULES

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

CIRCUIT REALIZATION OF CARRY OUT (COUT)

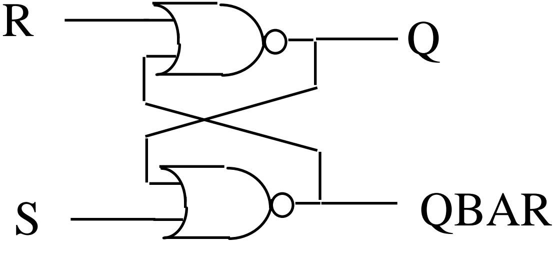


TRUTH TABLE
FOR ADDITION
RULES

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

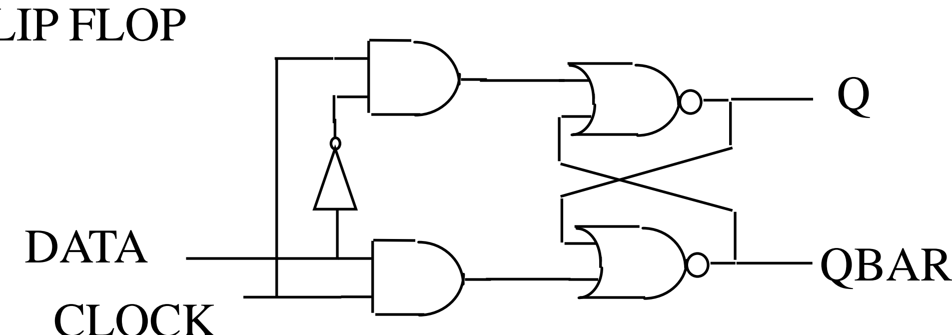
FILP-FLOPS

RS FLIP FLOP



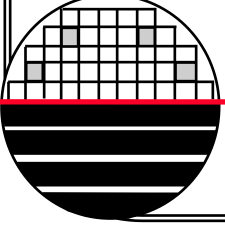
R	S	Q
0	0	Qn-1
0	1	1
1	0	0
1	1	INDETERMINATE

D FLIP FLOP

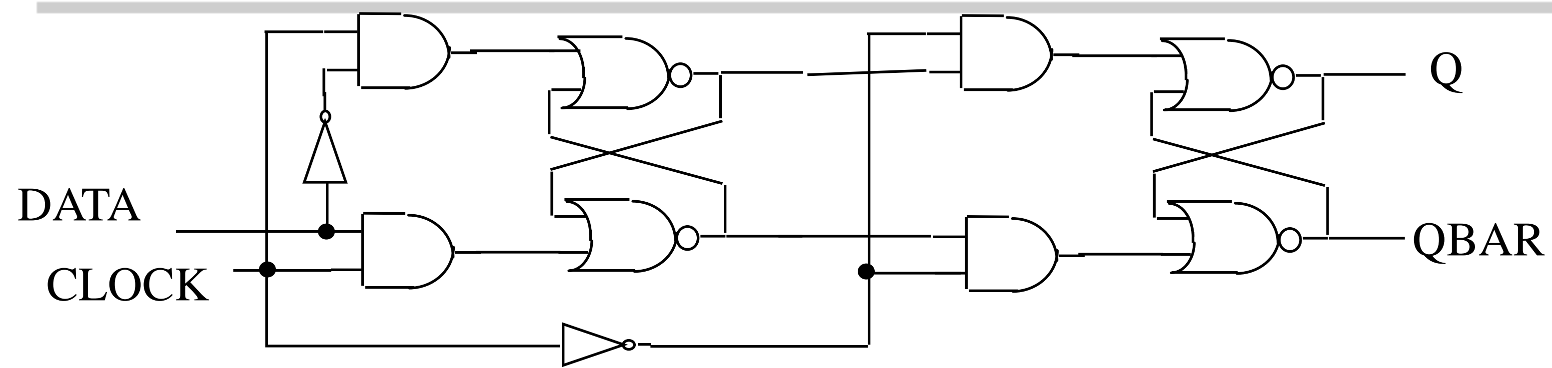


Q=DATA IF CLOCK IS HIGH

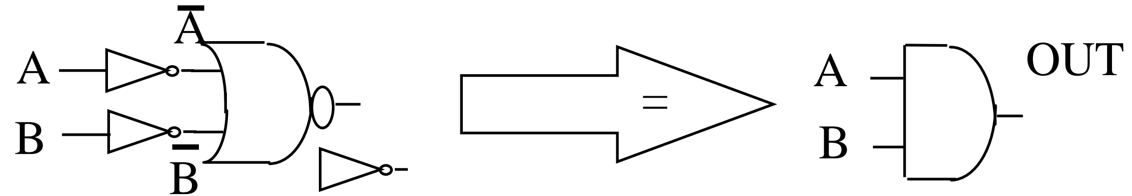
IF CLOCK IS LOW Q=PREVIOUS DATA VALUE



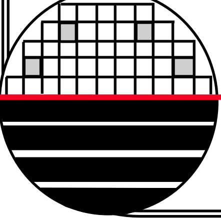
MASTER-SLAVE D FLIP FLOP



NEGATED INPUT NOR IS EQUAL TO AND



A	B	$\bar{A}$	$\bar{B}$	$\overline{OUT}$	OUT
0	0	1	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1



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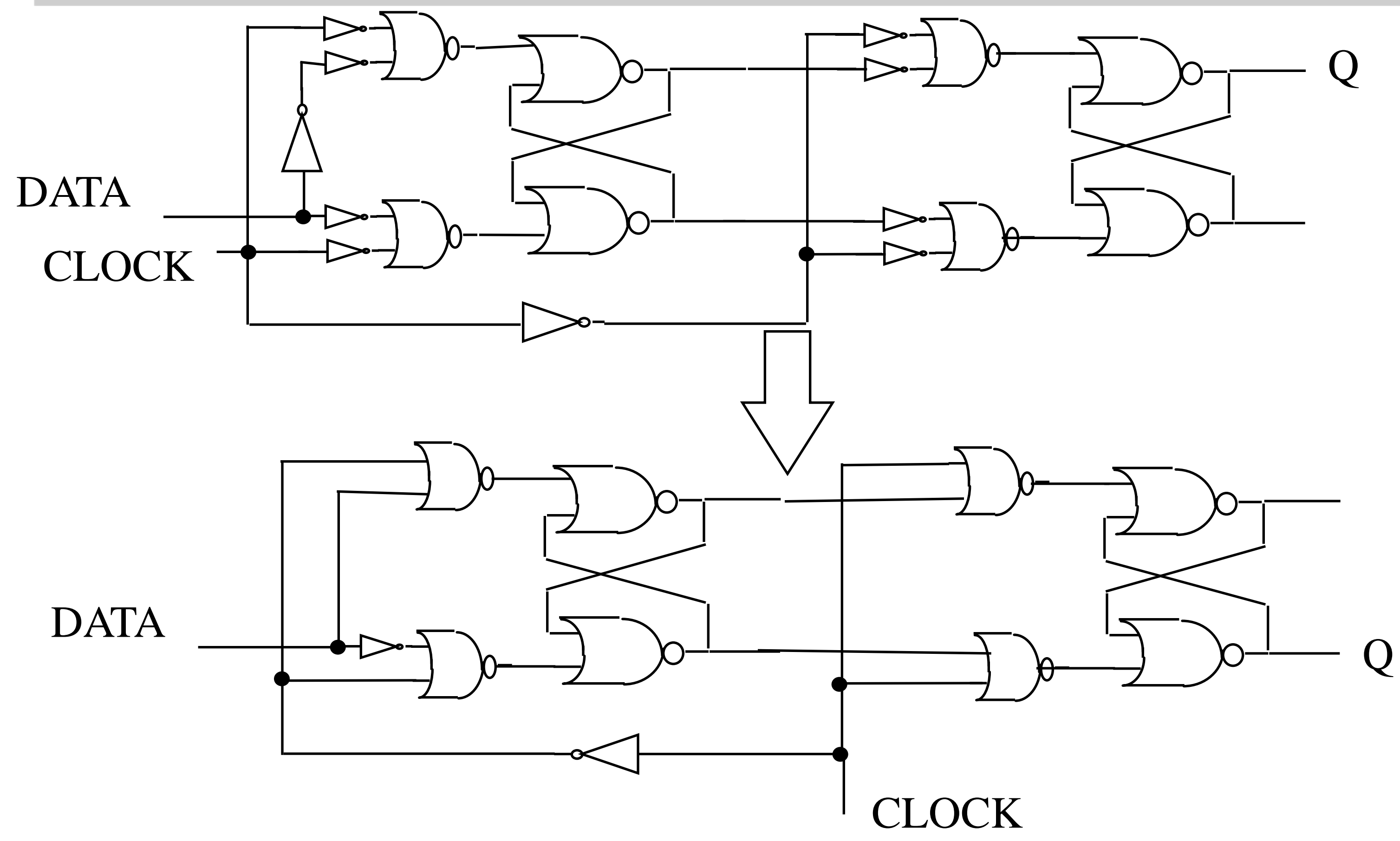
ALL NOR MASTER SLAVE D FLIP FLOP



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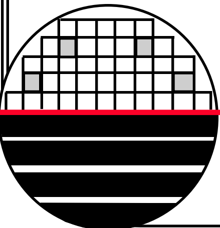
EQUAVILANT REALIZATIONS

AND-OR realizations are easily derived from truth table description of a circuits performance. Replacing the AND and OR gates with all NOR gates is equivalent. Replacing the AND and OR gates with all NAND gates is equivalent.



CIRCUIT REALIZATION FOR XOR

Exclusive OR
XOR

VA	VB	VOUT
0	0	0
0	1	1
1	0	1
1	1	0

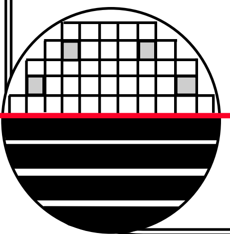
A B COUT

A B COUT

A B COUT

VLSI

VLSI
Very Large Scale Integration

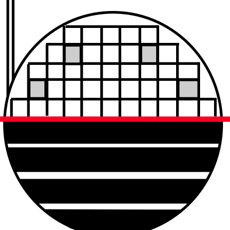


INTRODUCTION

VLSI is an acronym for Very Large Scale Integration. This includes Integrated circuits with greater than tens of thousands of transistors including multi-million or even billions of transistors.

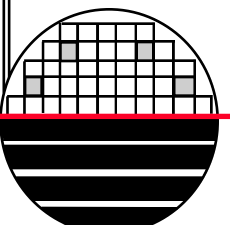
VLSI Design refers to methodologies and computer software tools for designing digital circuits with huge numbers of transistors. Some of theses methodologies and tools can also be applied to analog circuit design.

Software tools include schematic capture, SPICE analog simulation, switch level digital simulation, layout editors, layout versus schematic checking, design rule checking (DRC), auto place and routing and many more.



VLSI DESIGN

Computer software is used to check the layout, compare the layout to the schematic and make it possible to design circuits with millions of transistors with no errors.



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VLSI DESIGN METHODOLOGIES

Full Custom Design

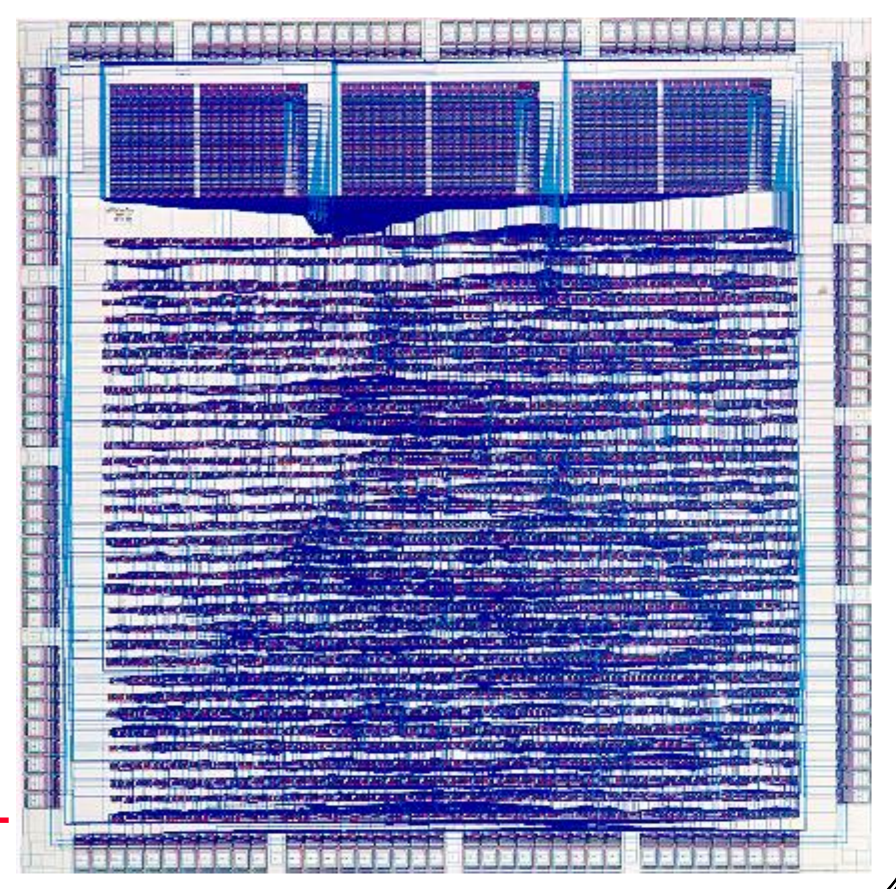
Direct control of layout and device parameters
Longer design time
High performance
fast, low power, dense

Standard Cell Design

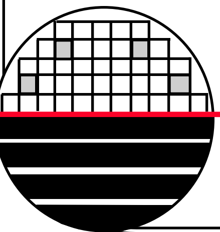
Easy to implement
Medium performance
Limited cell library selections

Gate Array or
Programmable Logic Array Design

Fastest design turn around



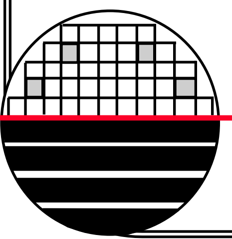
Layout Design Rules



LAMBDA BASED DESIGN RULES

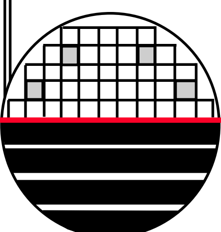
The design rules may change from foundry to foundry or for different technologies. So to make the design rules generic the sizes, separations and overlap are given in terms of numbers of lambda (λ). The actual size is found by multiplying the number by the value for lambda for that specific foundry.

For example:
RIT PMOS process λ = 10 µm and minimum metal width is 3 λ so that gives a minimum metal width of 30 µm. The RIT SUB-CMOS process has λ = 0.5 µm and the minimum metal width is also 3 λ so minimum metal is 1.5 µm but if we send our CMOS designs out to industry λ might be 0.25 µm so the minimum metal of 3 λ corresponds to 0.75 µm. In all cases the design rule is the minimum metal width = 3 λ

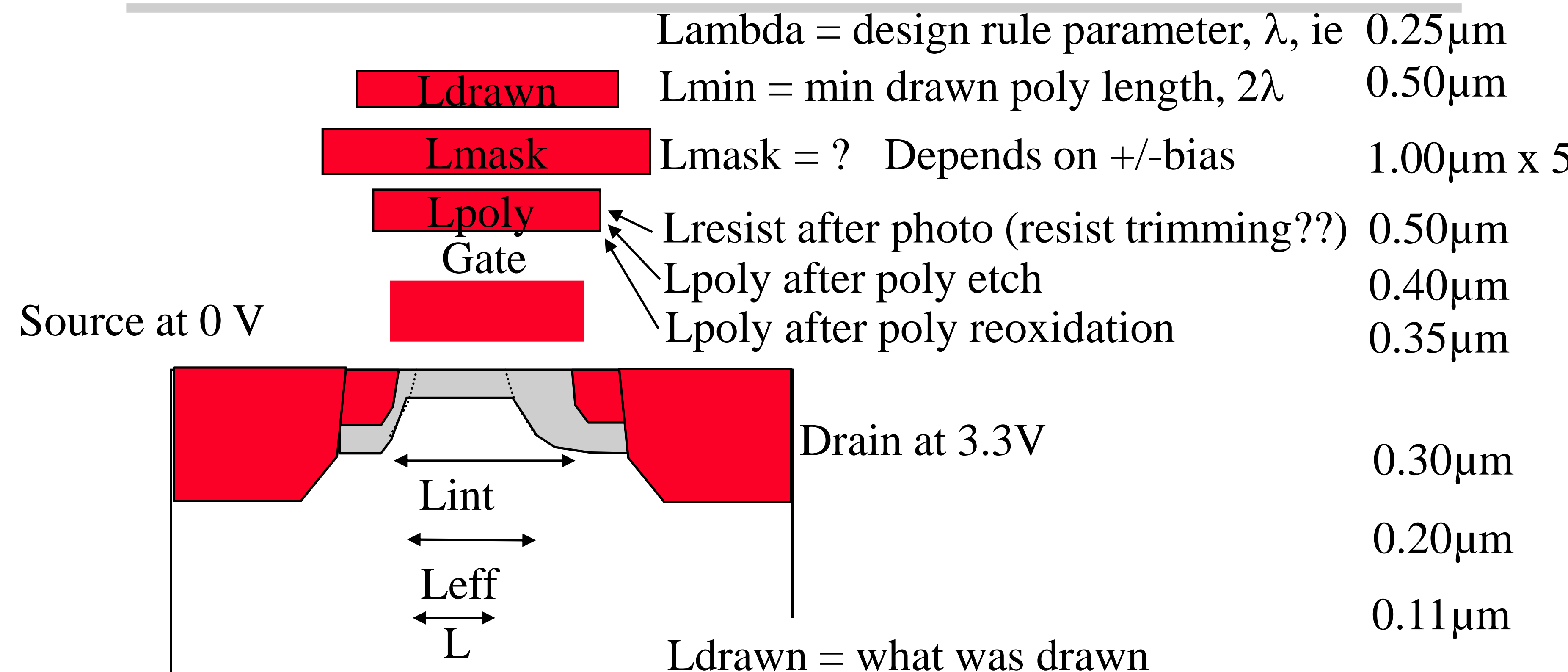


DESIGN RULES

We will use a modified version of the MOSIS TSMC 0.35 2P 4M design rules. Eventually we hope to be compatible with MOSIS but new process technology needs to be developed at RIT to do that (PECVD Tungsten, 4 layer metal). We use one layer of poly and two layers of metal. We will use the same design layer numbers with additional layers as defined on the following pages for manufacturing/maskmaking enhancements. Many of the designs will use minimum drawn poly gate lengths of 2µm where circuit architecture is the main purpose of the design. Minimum size devices (Drawn Poly = 0.5µm, etc.) are included to develop manufacturing process technology. These transistors (0.5µm drawn) yield 0.35µm Leff and are equivalent to the TSMC 0.35µm transistors.



LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L



Internal Channel Length, Lint =distance between junctions, including under diffusion
Effective Channel Length, Leff = distance between space charge layers,Vd = Vs= 0
Channel Length, L, = distance between space charge layers, when Vd= what it is
Extracted Channel Length Parameters = anything that makes the fit good (not real)

MOSIS TSMC 0.35 2POLY 4 METAL PROCESS

http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html#tech-codes

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MOSIS SCMOS Technology Codes and Layer Maps

SCN4M and SCN4M_SUBM

This is the layer map for the technology codes SCN4M and SCN4M_SUBM using the MOSIS Scalable CMOS layout rules (SCMOS), and only for SCN4M and SCN4M_SUBM. For designs that are laid out using other design rules (or technology codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

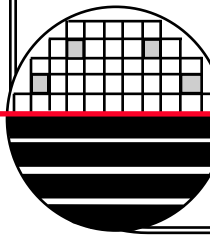
SCN4M: Scalable CMOS N-well, 4 metal, 1 poly, silicided. Silicide block and thick oxide option available only on the TSMC process.

SCN4M_SUBM: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

Fabricated on TSMC, AMIS, and Agilent/HP 0.35 micron process runs. See "Notes" section of layer map for foundry-specific options.

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	
ACTIVE	43	CAA		2	
THICK_ACTIVE	60	CTA		24	Optional for TSMC; not available for Agilent/HP nor AMIS
POLY	46	CPG		3	
SILICIDE_BLOCK	29	CSB		20	Optional for Agilent/HP; not available for AMI
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	
METAL3	62	CM3	CMT	15	
VIA3	30	CV3	CVT	21	
METAL4	31	CM4	CMQ	22	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME



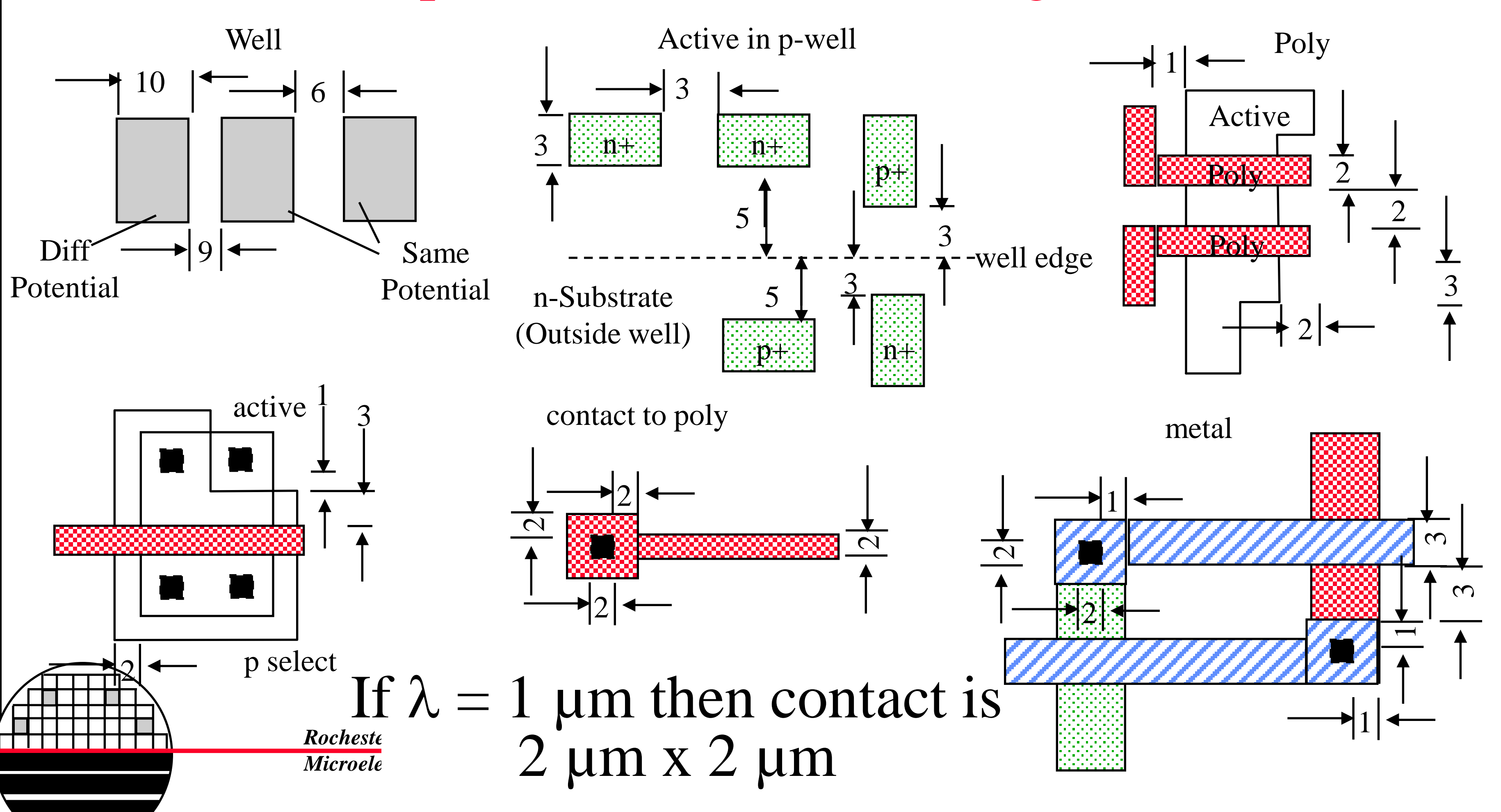
MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

MASK LAYER NAME	MENTOR NAME	GDS #	COMMENT
N WELL	N_well.i	42	
ACTIVE	Active.i	43	
POLY	Poly.i	46	
N PLUS	N_plus_select.i	45	
P PLUS	P_plus_select.i	44	
CONTACT	Contact.i	25	Active_contact.i 48 poly_contact.i 47
METAL1	Metal1.i	49	
VIA	Via.i	50	
METAL2	Metal2.i	51	
VIA2	Via2.i	61	Under Bump Metal
METAL3	Metal3.i	62	Solder Bump

These are the main design layers up through metal two

MOSIS LAMBDA BASED DESIGN RULES

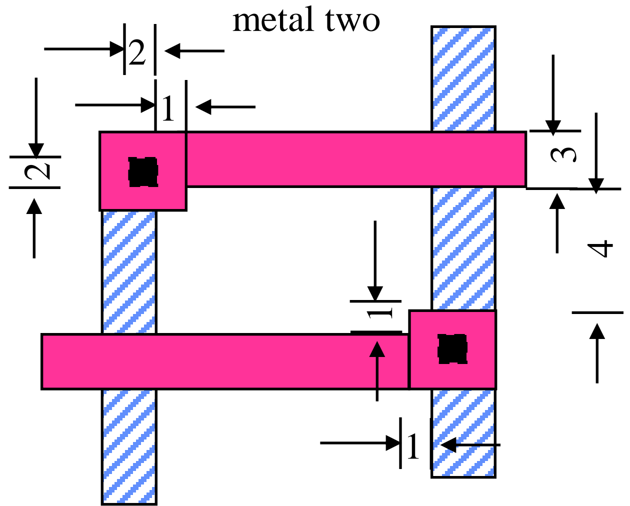
http://www.mosis.com/design/rules/



If λ = 1 µm then contact is 2 µm x 2 µm

MOSIS LAMBDA BASED DESIGN RULES

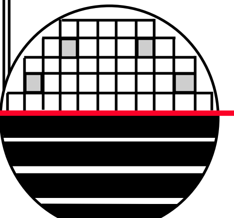
http://www.mosis.com/design/rules/



MOSIS Educational Program

Instructional Processes Include:
AMI $\lambda = 0.8$ µm SCMOS Rules
AMI $\lambda = 0.35$ µm SCMOS Rules

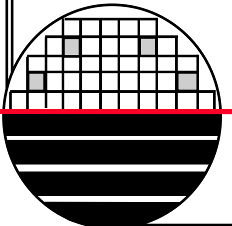
Research Processes:
go down to poly length of 65nm



MOSIS REQUIREMENTS

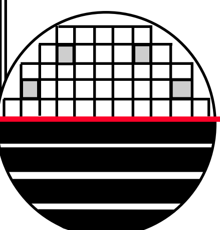
MOSIS requires that projects have successfully passed LVS (Layout Versus Schematic) and DRC (Design Rule Checking). The MENTOR tools for LVS and DRC (as they are set up at RIT) require separate N-select and P-select levels in order to know an NMOS transistor from a PMOS transistor. Although either an N-well, P-well or both will work for a twin well process, we have set up our DRC to look for N-well. (Also since we use a p-type starting wafer we can not have isolated p-wells but we can have isolated n-wells, thus drawing separate n-wells can be useful for some circuit designs.)

http://www.mosis.com



LAYOUT

Digital Circuit Layout



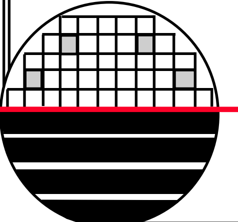
DIGITAL CIRCUITS

The design approach for digital circuits is to design primitive cells and then use the primitive cells to design basic cells which are then used in the project designs. A layout approach is also used that allows for easy assembly of these cells into more complex cells.

Primitive Cells
- INVERTER, NAND2,3,4, NOR2,3,4, NULL

Basic Cells
- XOR, MUX, DEMUX, ENCODER, DECODER
- FULL ADDER, FLIP FLOPS

Macro Cells
- BINARY COUNTER
- SRAM



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LAYOUT – GATE ARRAY

Green is Active
Dashed Yellow is N-Well
Red is Poly
Blue is Metal-One
Pink is Metal-Two
White is Contact Cut
Yellow is Via
P and N select not shown

VDD
OUT
IN
PMOS
IN
IN
IN
NMOS
GND

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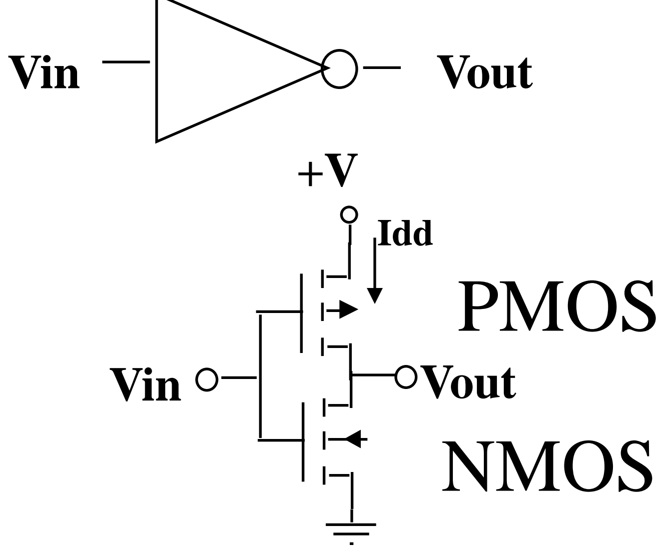
LAYOUT DETAILS FOR GATE ARRAY

1. Cells are separated from adjacent cells by off transistors
2. Well contacts are made at each of the off transistors
3. Metal-two connects thru Via to Metal-one
4. Metal-one connects thru Contact Cuts to active and Poly
5. Inputs and Outputs connections are made vertically with Metal-two
6. Routing channels exist above and below the gate array and contain horizontal metal-one interconnects between cells, with Via to Metal-two.
7. The NULL cell at the end of the gate array row satisfy design rules for extension of well beyond active, etc. It also provides a vertical routing channel which may be useful in constructing macro cells.

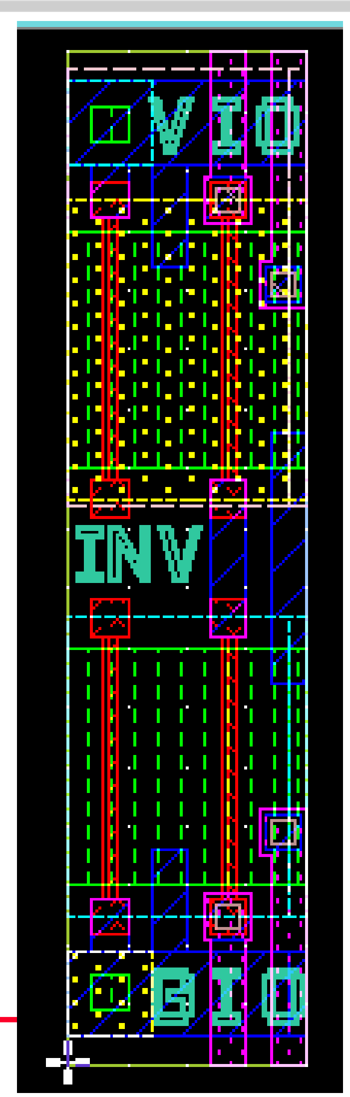
INVERTER

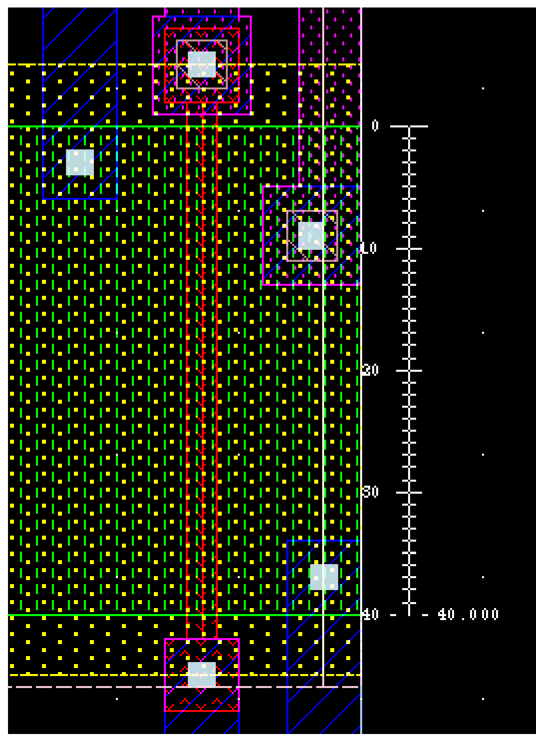


CMOS

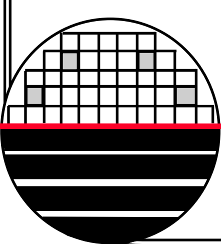
TRUTH TABLE

VIN	VOUT
0	1
1	0



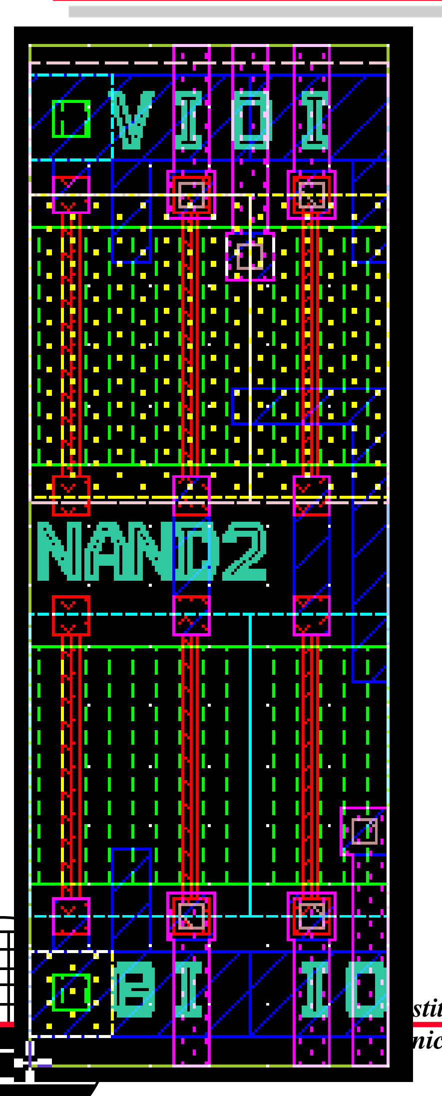


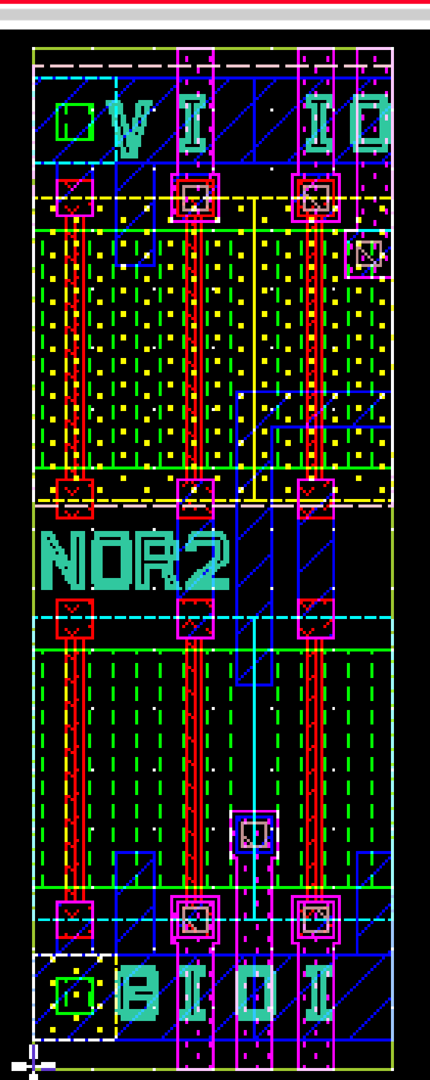
W = 40 µm
Ldrawn = 2.5µm
Lpoly = 1.0µm
Leff = 0.35 µm

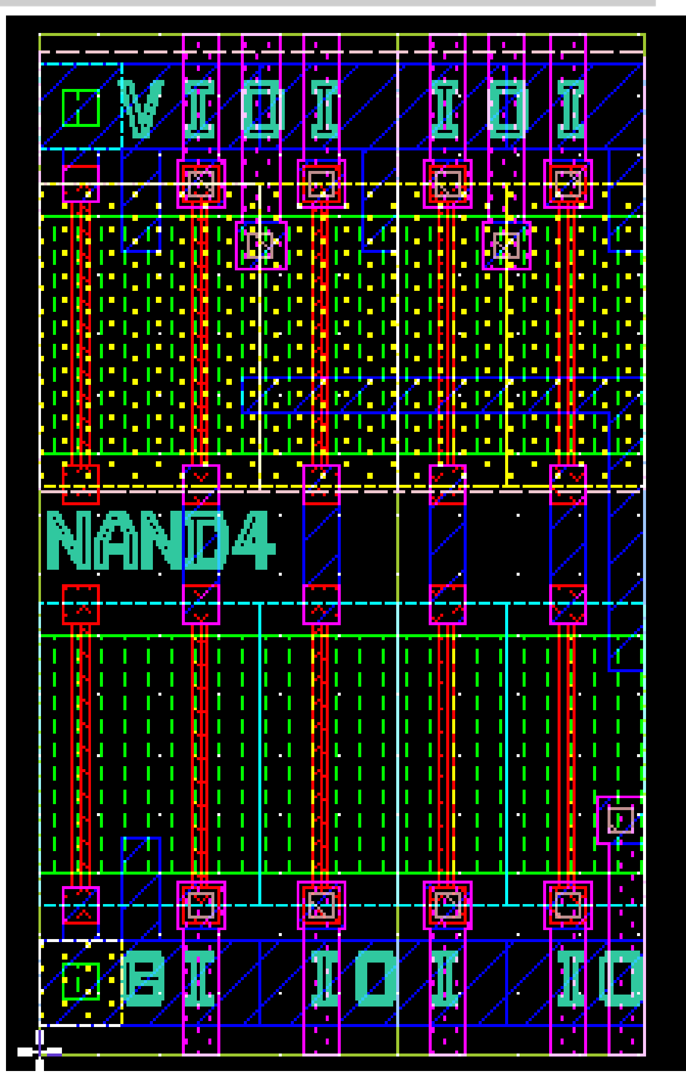


Rochester Institute of Technology
Microelectronic Engineering

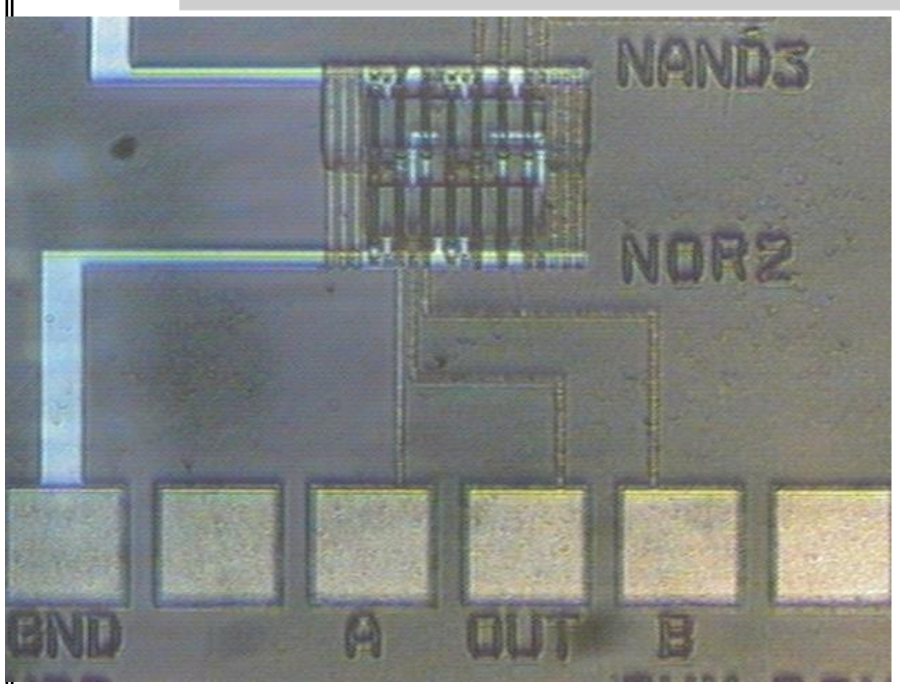
LAYOUT OF SOME PRIMITIVE CELLS

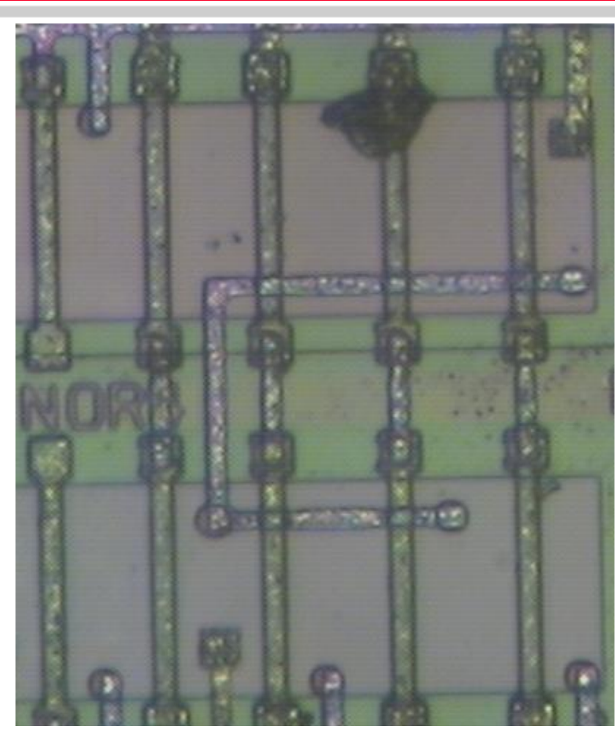






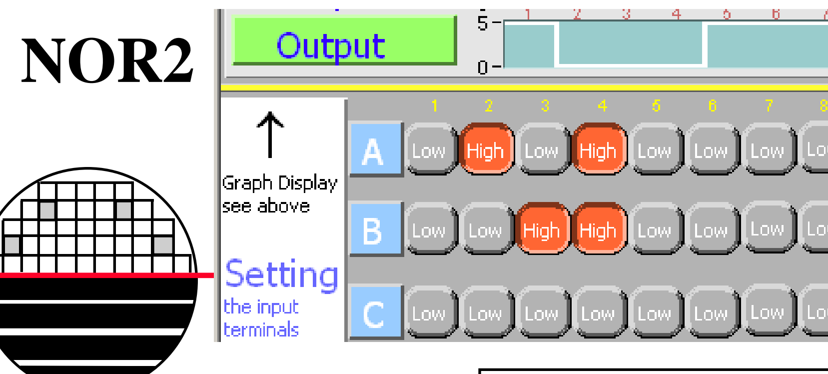
VERIFICATION NOR2 NAND3 FABRICATION & TEST

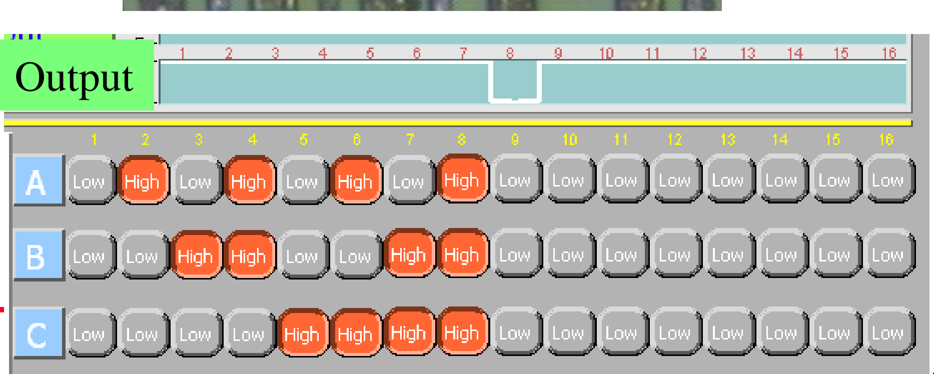




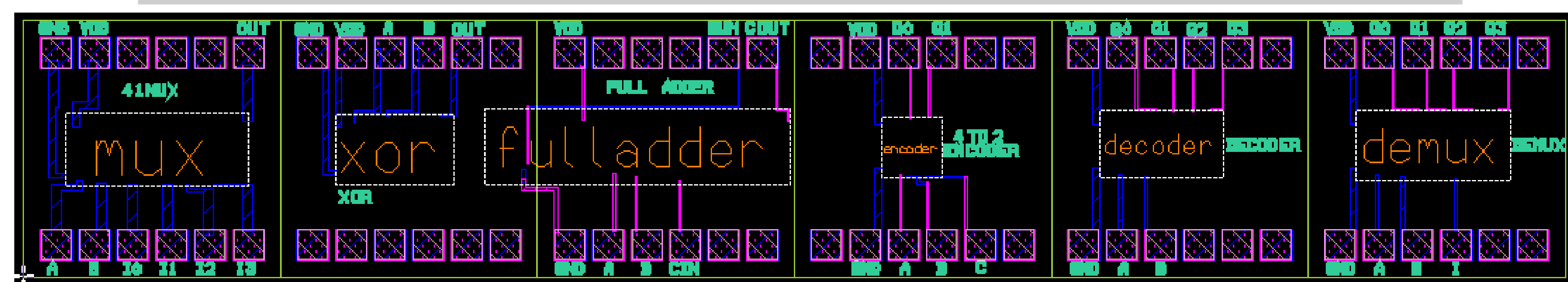
NAND3

NOR2

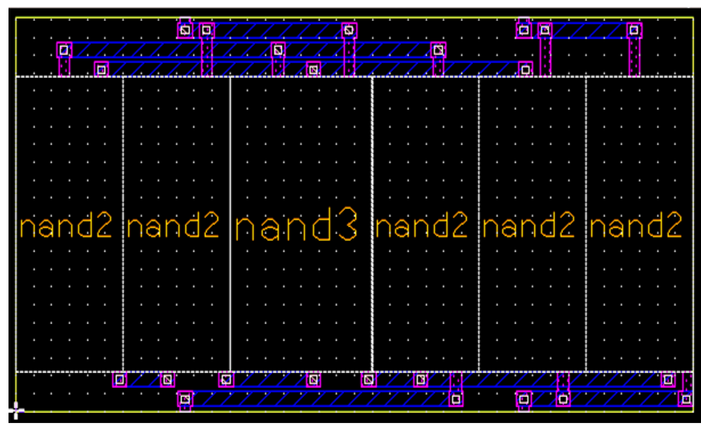




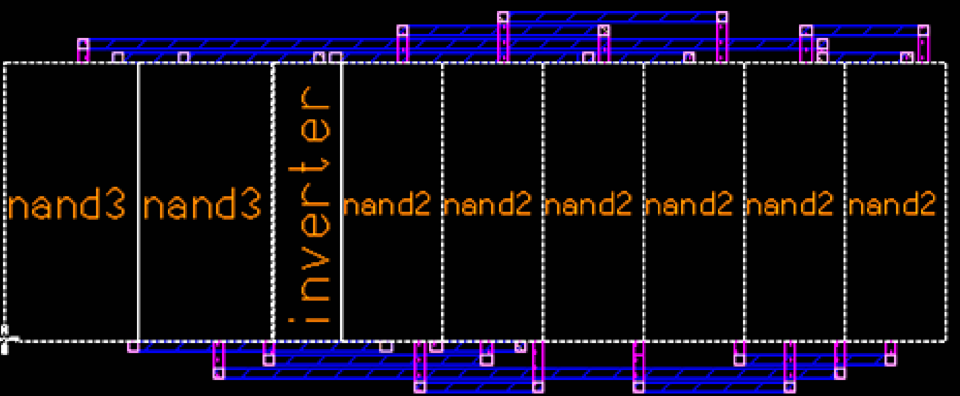
BASIC DIGITAL CELLS WITH PADS



Multiplexer XOR Full Adder Encoder Decoder Demux

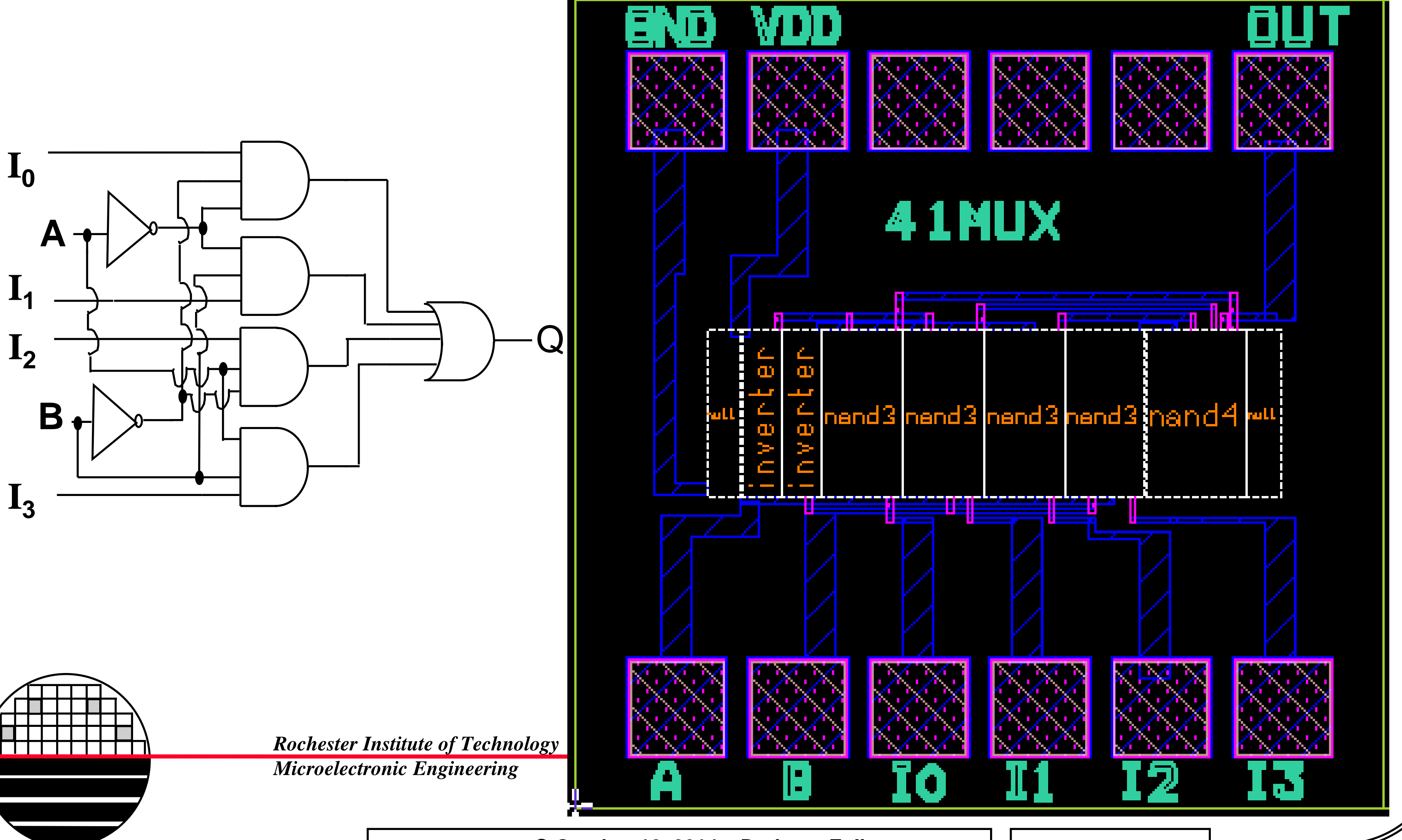


Edge Triggered D FF



JK FF

4 TO 1 MULTIPLEXER



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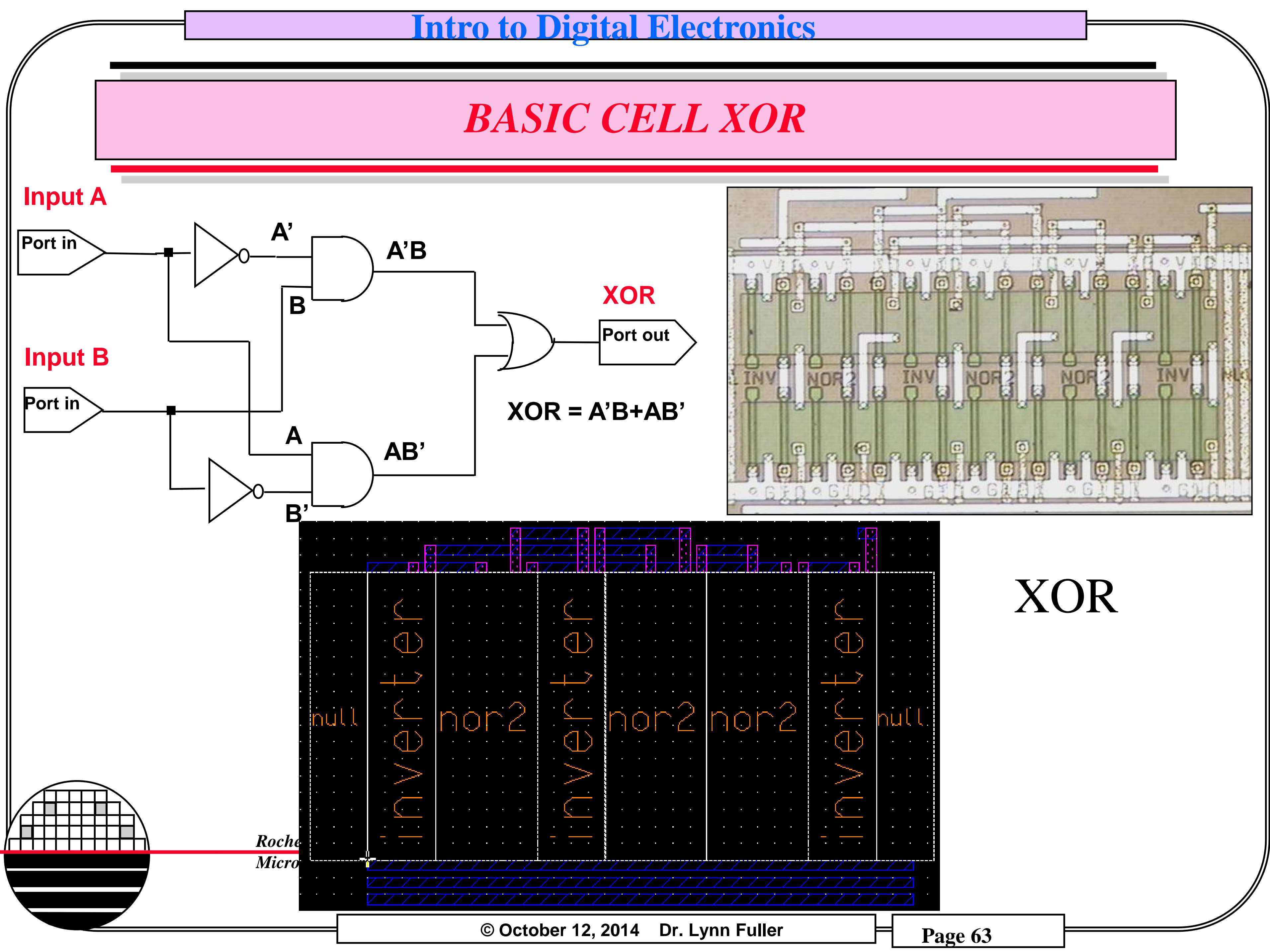
Intro to Digital Electronics
BASIC CELL XOR
Input A
Port in
A'
A'B
B
Input B
Port in
A
AB'
B'
XOR
Port out
XOR = A'B+AB'
INV
NOR2
INV
NOR2
NOR2
INV
null
inverter
nor2
inverter
nor2
nor2
inverter
null
XOR
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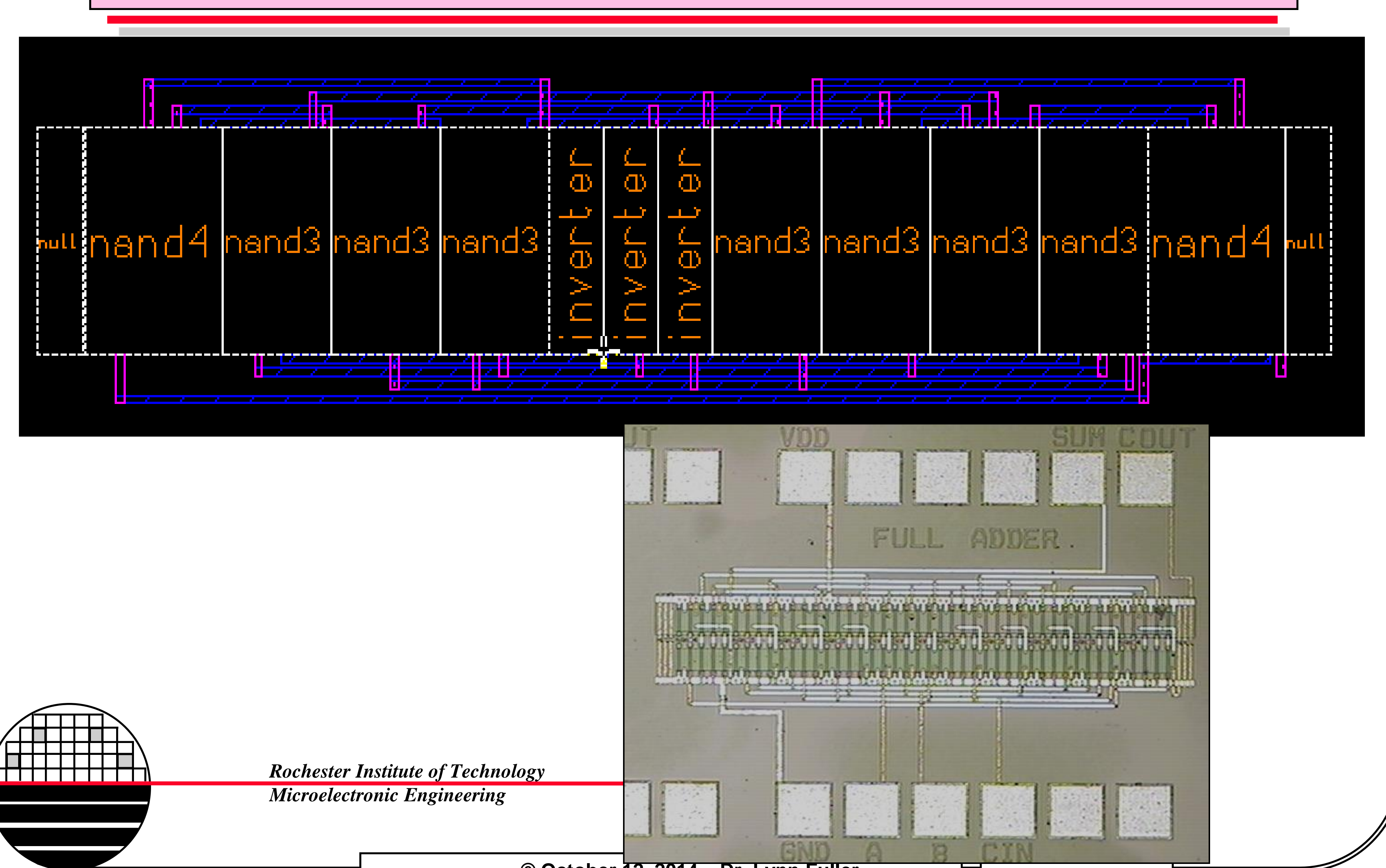
Page 63

FULL ADDER



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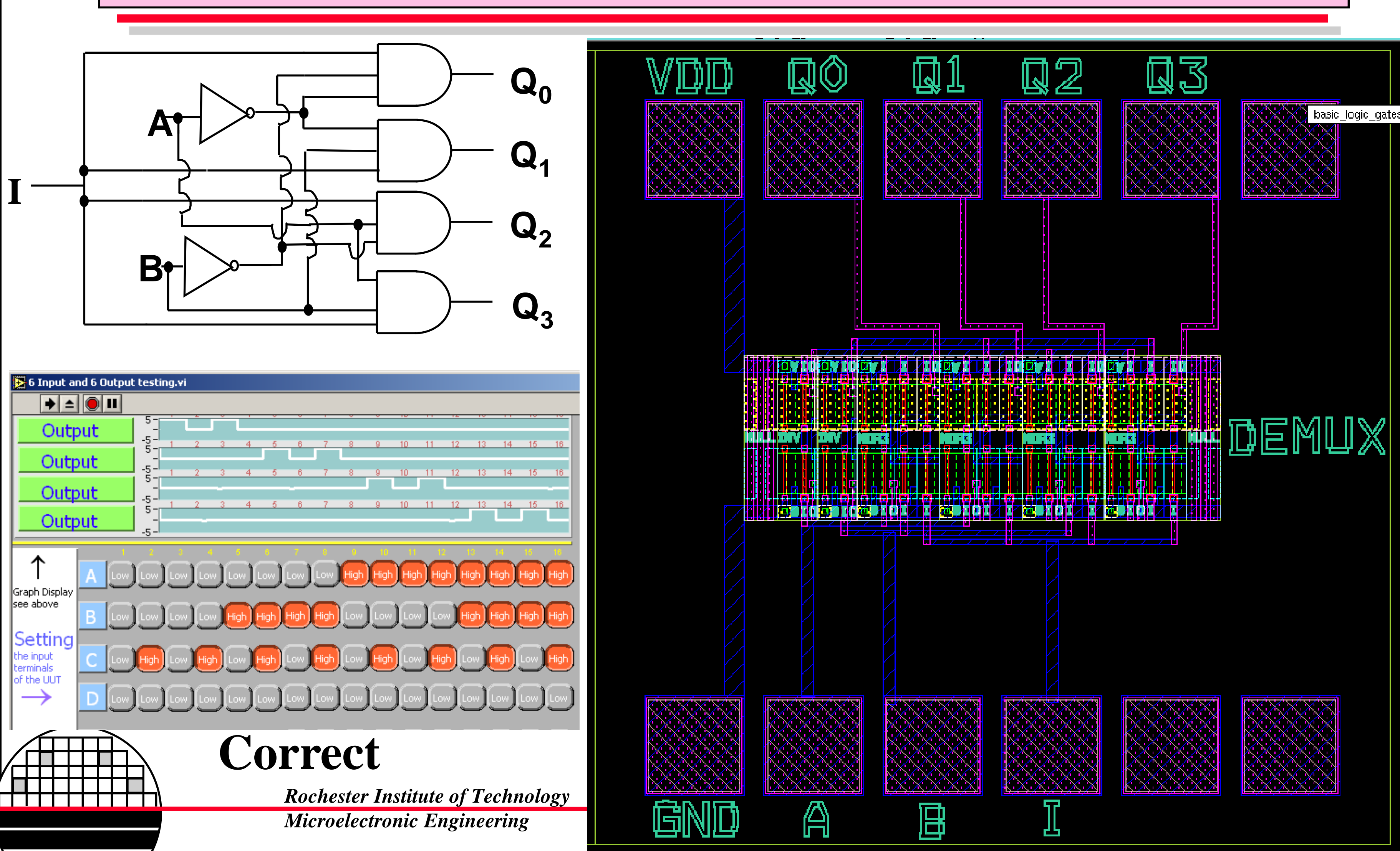
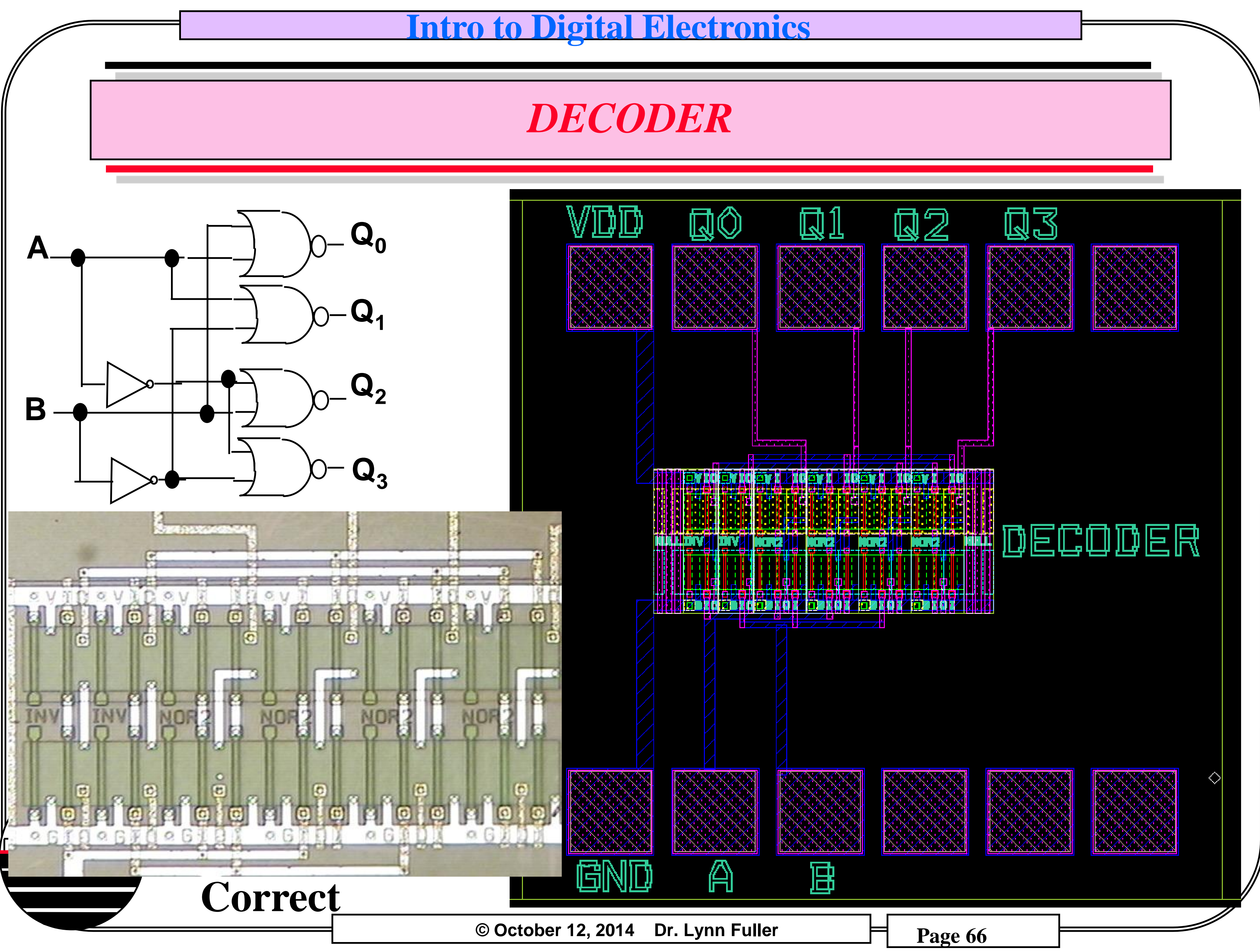
1 TO 4 DEMULTIPLEXER



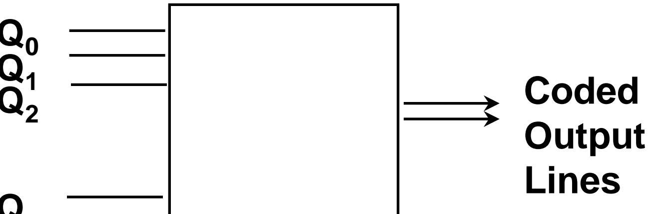
Correct

Rochester Institute of Technology
Microelectronic Engineering

DECODER

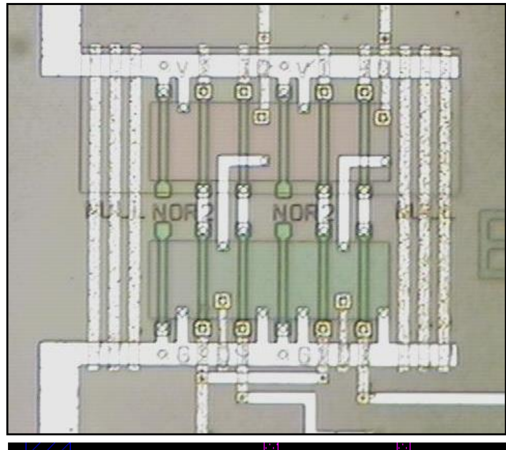


ENCODER

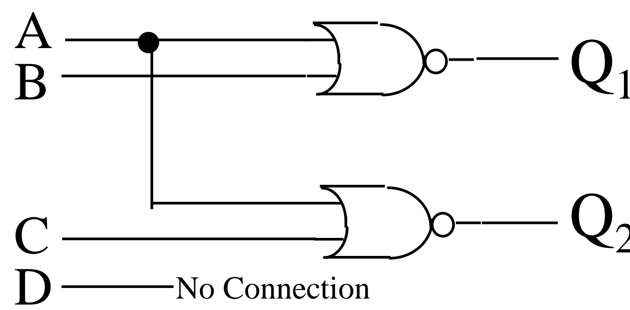


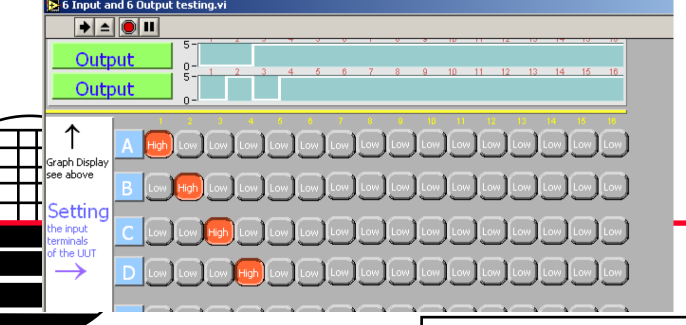
Digital Encoder

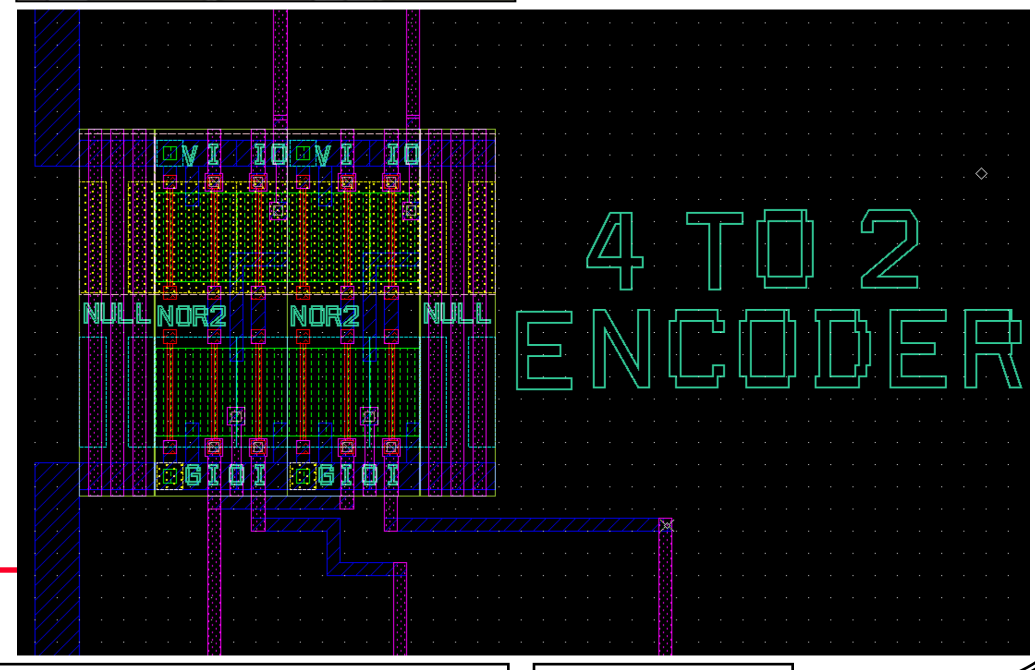
512 inputs can be coded into 9 lines which is a more dramatic benefit



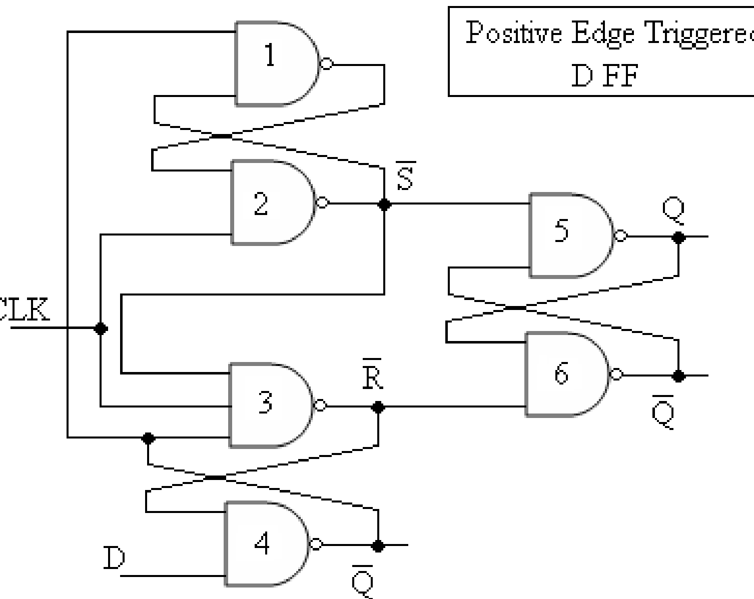
A	B	C	D	Q0	Q1
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1



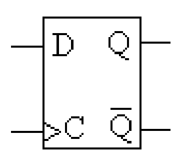




EDGE TRIGGERED D TYPE FLIP FLOP



Positive Edge Triggered
D FF



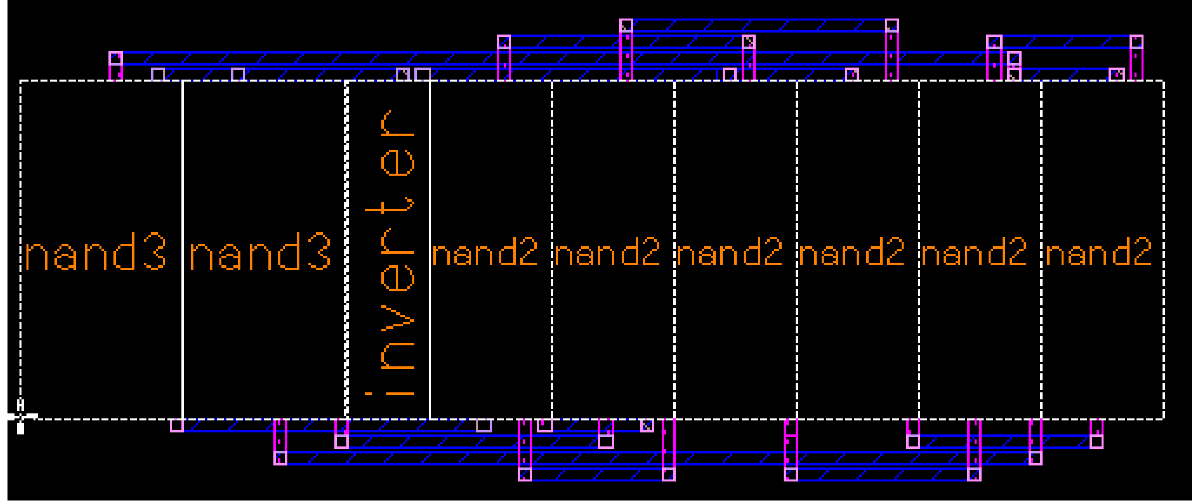
Inputs		Outputs	
D	C	Q^+	$\overline{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\overline{Q}$
X	1	Q	$\overline{Q}$

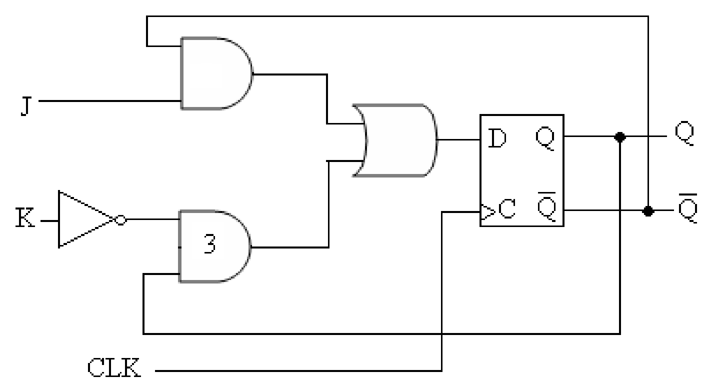
CLK D SET $\overline{Q}$ Q VDD

DFF SET RES
BURAK

RES GND

JK FLIP FLOP

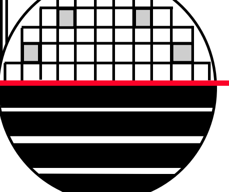




Positive Edge Triggered
JK FF

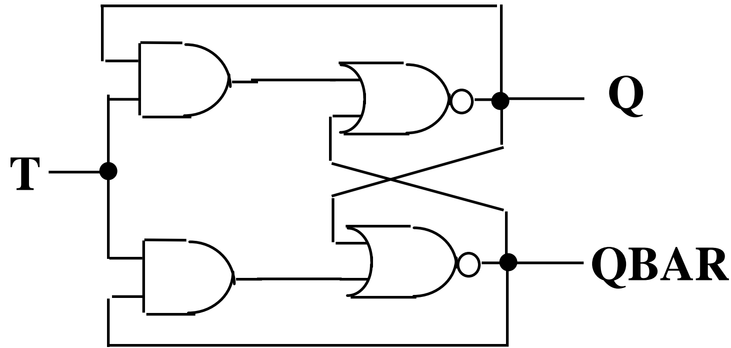
J Q
>C
K Q̄

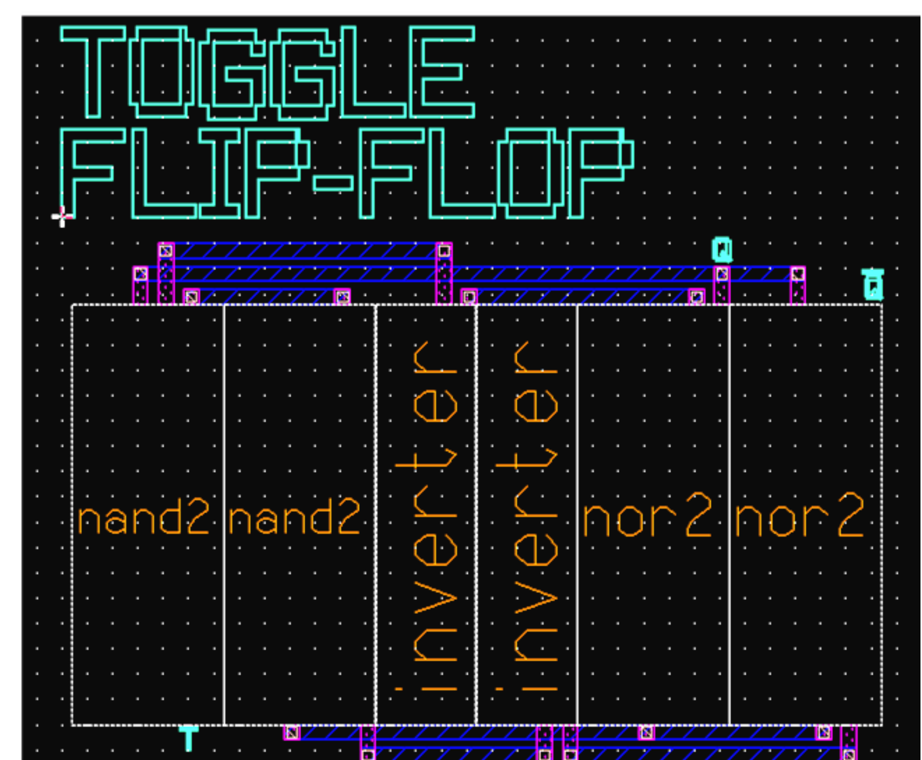
Inputs			Outputs	
J	K	C	Q^+	$\overline{Q}^+$
0	0	↑	Q	$\overline{Q}$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\overline{Q}$	Q
X	X	0	Q	$\overline{Q}$
X	X	1	Q	$\overline{Q}$



T-TYPE FILP-FLOP

TOGGEL FLIP FLOP

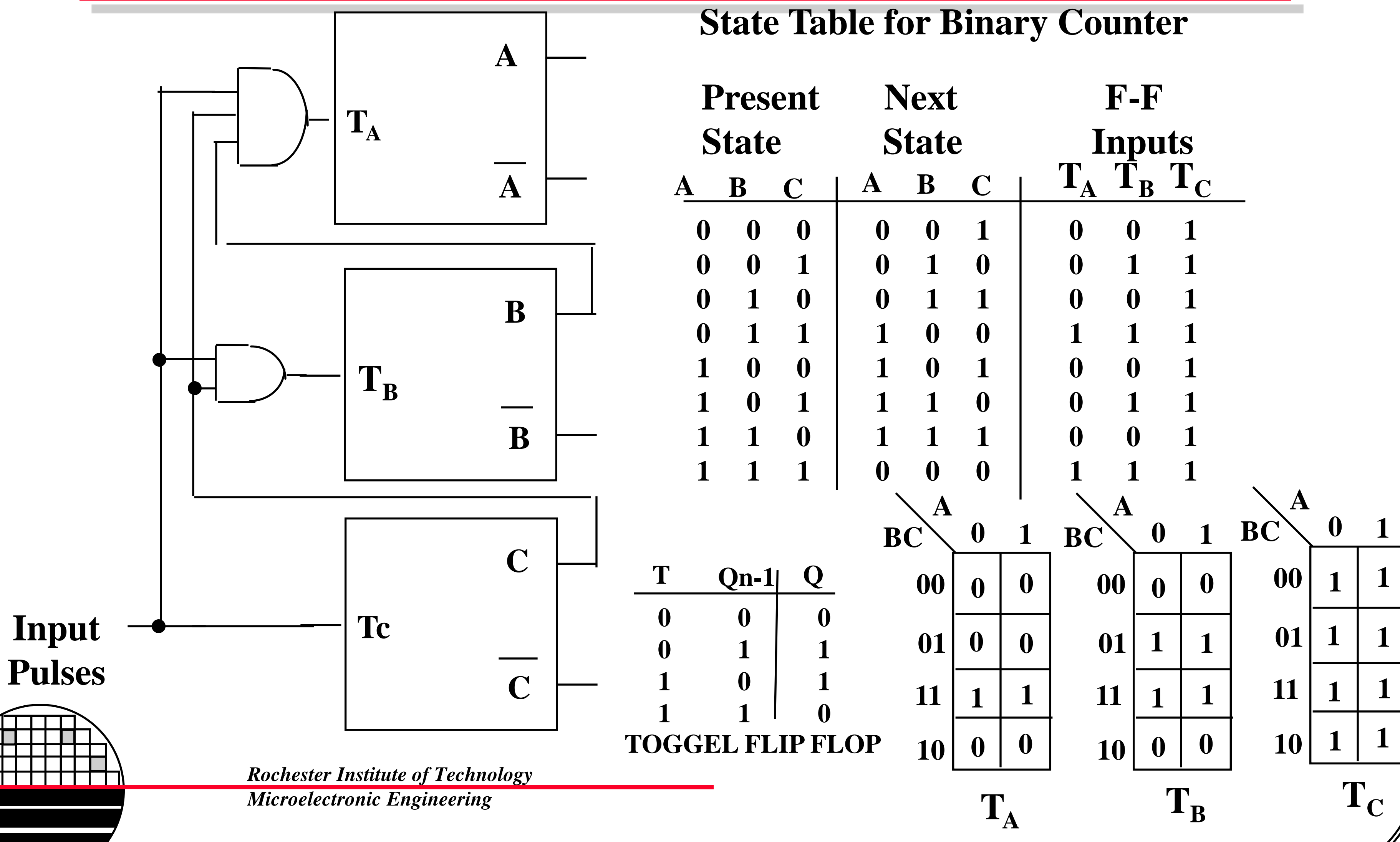




Q: Toggles High and Low with Each Input

T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

BINARY COUNTER USING T TYPE FLIP FLOPS



State Table for Binary Counter

Present State			Next State			F-F Inputs		
A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

TOGGEL FLIP FLOP

T_A

BC \ A	0	1
00	0	0
01	0	0
11	1	1
10	0	0

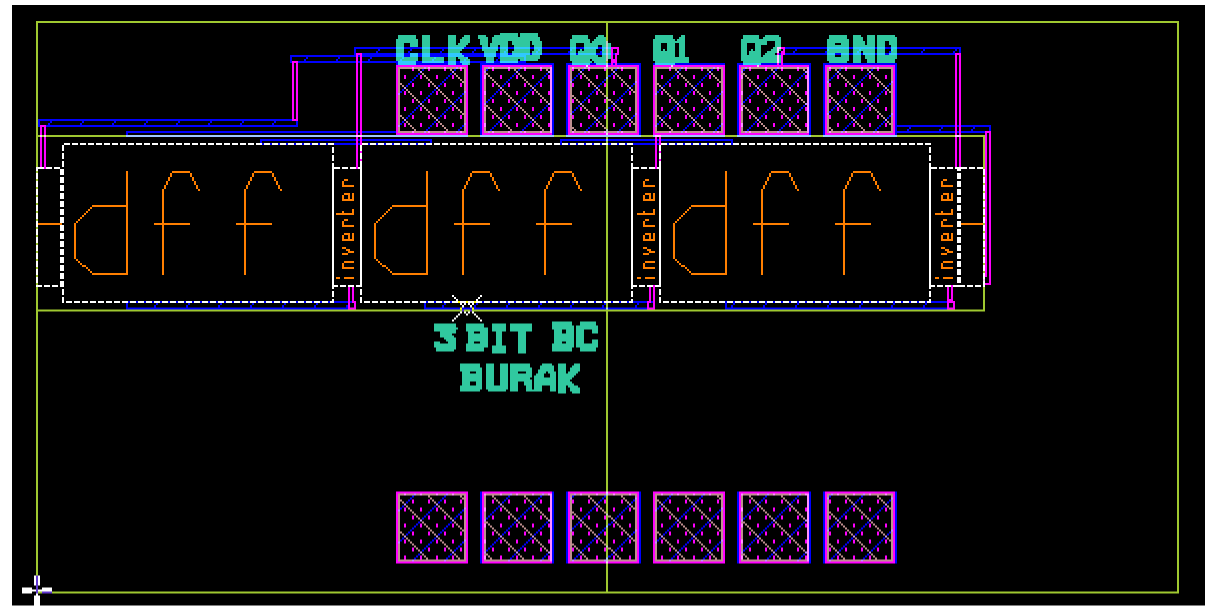
T_B

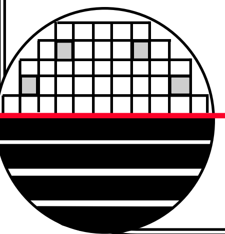
BC \ A	0	1
00	0	0
01	1	1
11	1	1
10	0	0

T_C

BC \ A	0	1
00	1	1
01	1	1
11	1	1
10	1	1

3-BIT BINARY COUNTER WITH D FLIP FLOPS





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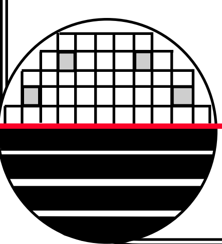
MACROCELLS

Binary Counter
SRAM



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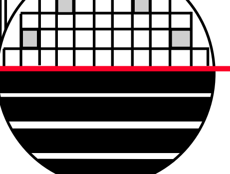
3-BIT BINARY COUNTER/SHIFT REGISTER

Binary Counter
Serial Output
Asynchronous Reset
Count Up Enable
Shift Out Clock Input
Count Up Clock Input
Start Bit and Stop Bit



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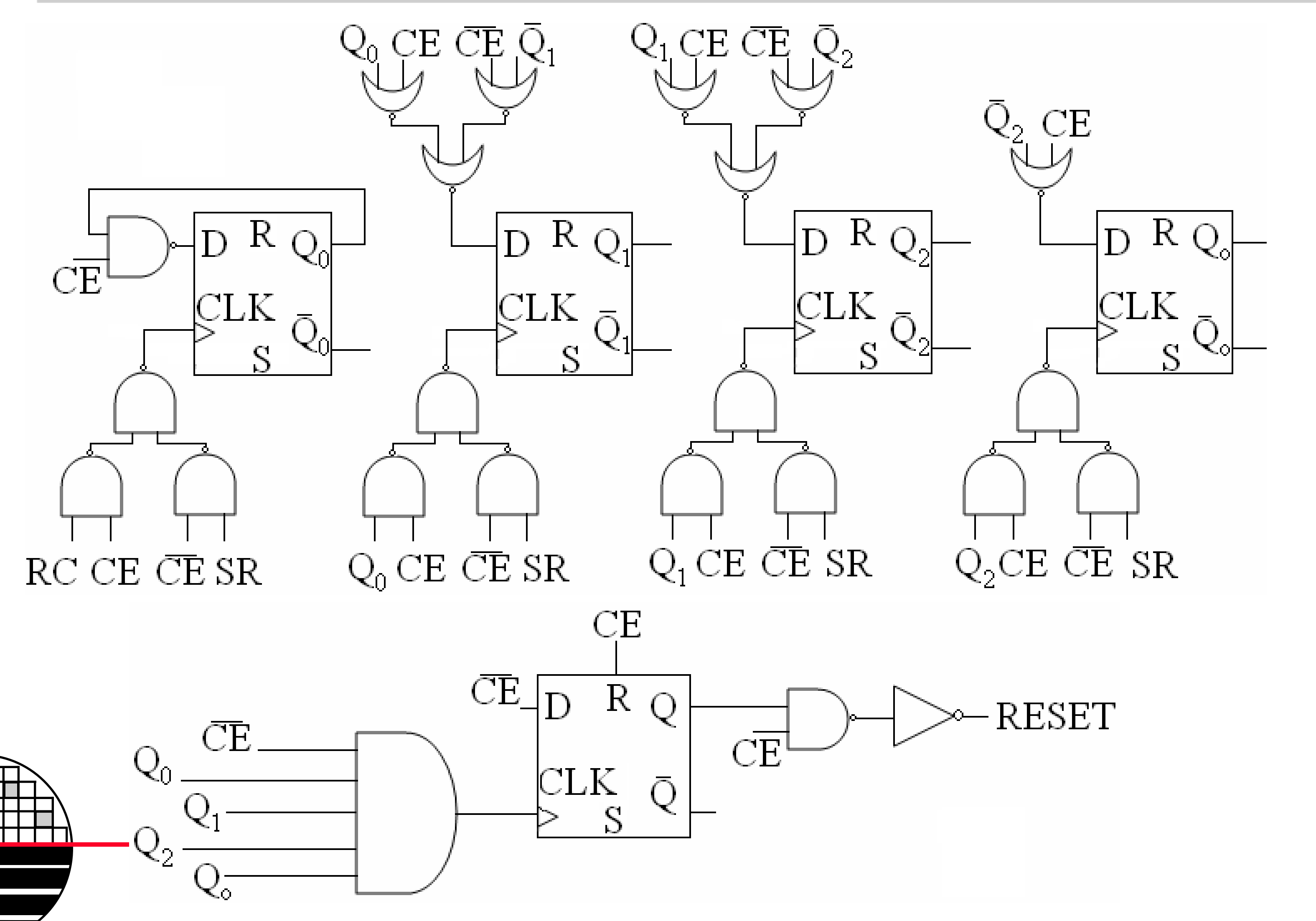
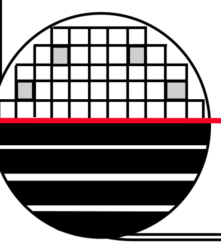
ADDITIONAL CIRCUITRY TO RESET, SHIFT, COUNT

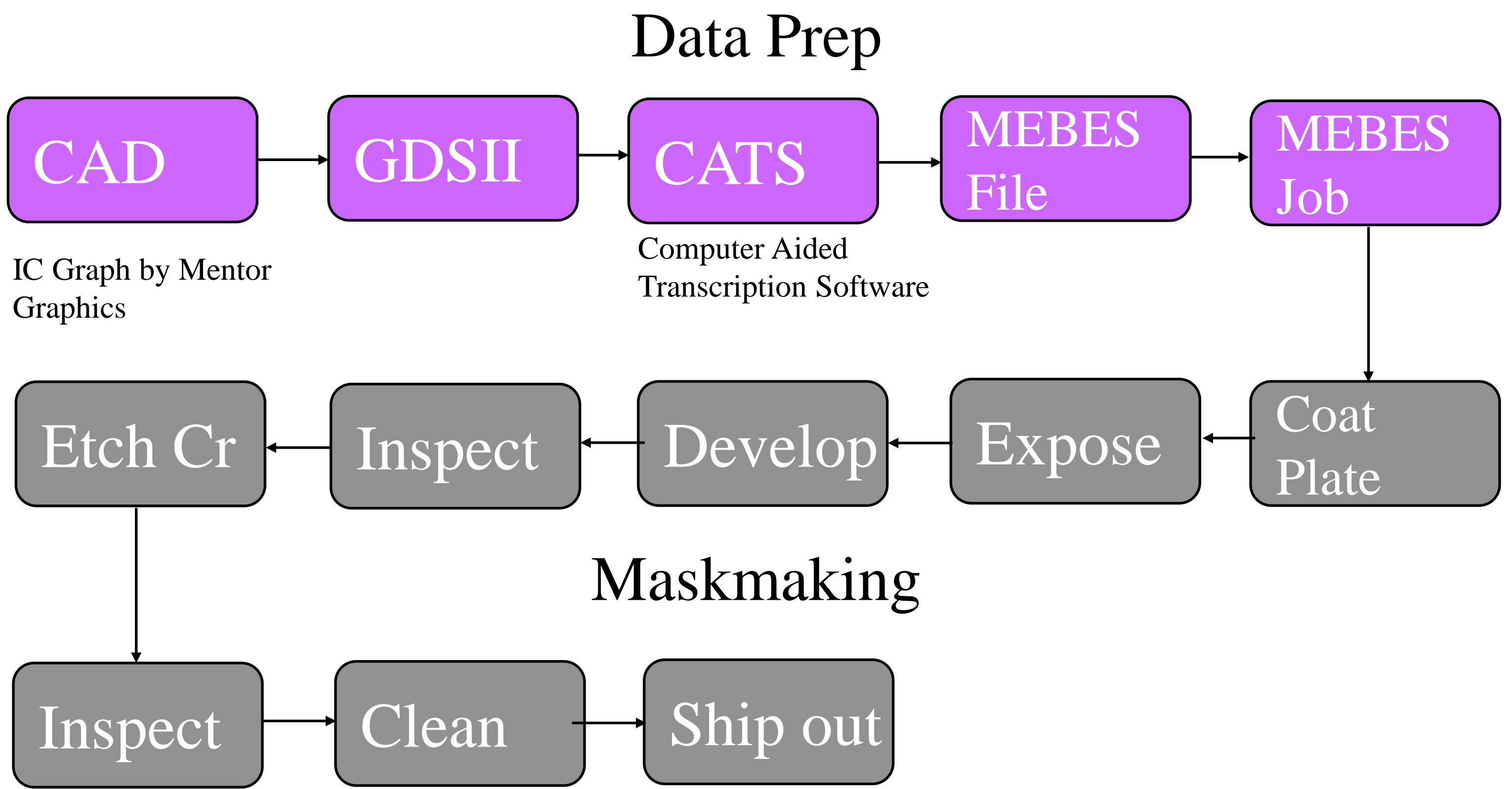


MASKMAKING

Maskmaking



MASK PROCESS FLOW



This process can take weeks and cost between $1000 and $20,000 for each mask depending on the design complexity.

OTHER MASKMAKING FEATURES

Fiducial Marks-marks on the edge of the mask used to align the mask to the stepper

Barcodes

Titles

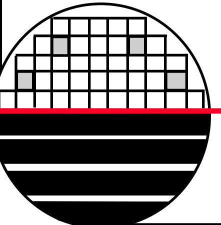
Alignment Keys- marks on the wafer from a previous level used for wafer alignment

CD Resolution Targets- lines and spaces

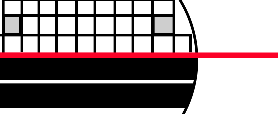
Overlay Verniers- structures that allow measurement of x and y overlay accuracy

Tiling

Optical Proximity Correction (OPC)



MEBES - Manufacturing Electron Beam Exposure System



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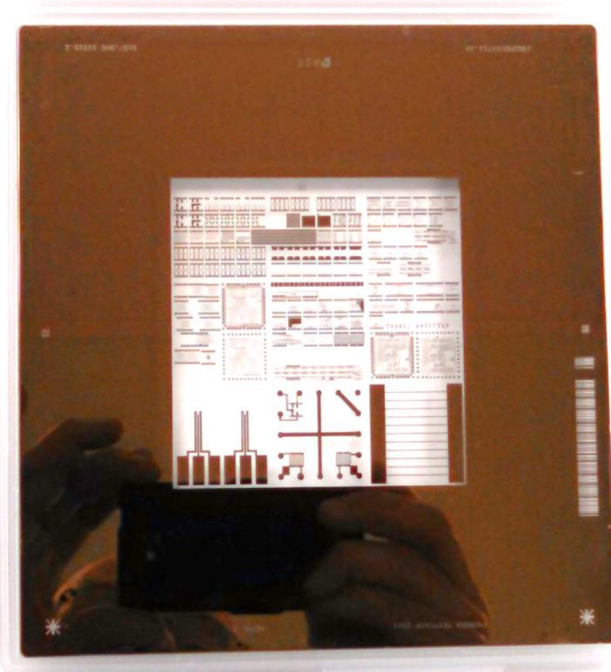
ASML RETICLE



Chrome Side
Mirrored 90°
Chip Bottom at Bottom

Non Chrome Side
As loaded into Reticle Pod, Chrome Down, Reticle Pre-Alignment Stars Sticking out of Pod

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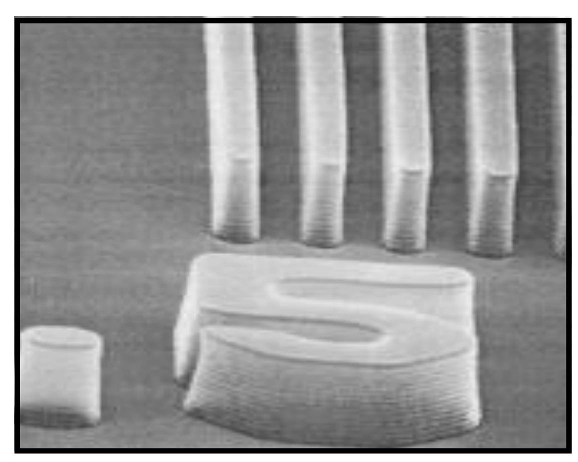
ASML 5500/200



NA = 0.48 to 0.60 variable
σ= 0.35 to 0.85 variable
With Variable Kohler, or
Variable Annular illumination
Resolution = K1 λ/NA
= ~ 0.35μm
for NA=0.6, σ =0.85
Depth of Focus = k_2 $\lambda/(NA)^2$
= > 1.0 μm for NA = 0.6

i-Line Stepper λ = 365 nm
22 x 27 mm Field Size

RIT SUB-CMOS PROCESS

NMOSFET PMOSFET

N+ Poly

0.75 um Aluminum

6000 Å Field Oxide

p+ well contact

N+ D/S

LDD

P-well

N-well

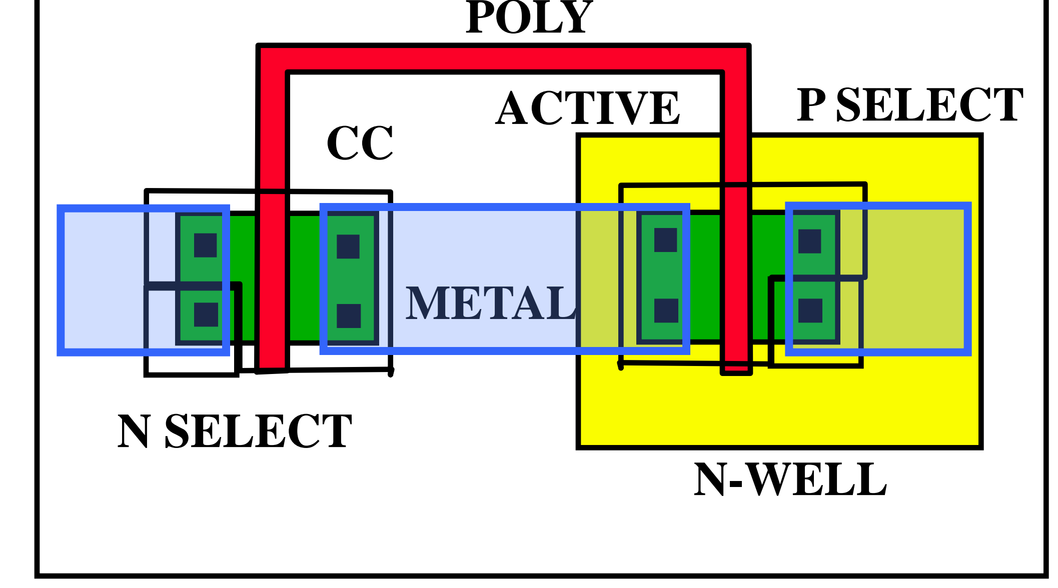
LDD

P+ D/S

n+ well contact

Channel Stop

N-type Substrate 10 ohm-cm



LVL 1 – n-WELL

LVL 2 - ACTIVE

LVL 3 - STOP

LVL 4 - PMOS VT

LVL 5 - POLY

LVL 6 – P-LDD

LVL 7 – N-LDD

LVL 8 - P+ D/S

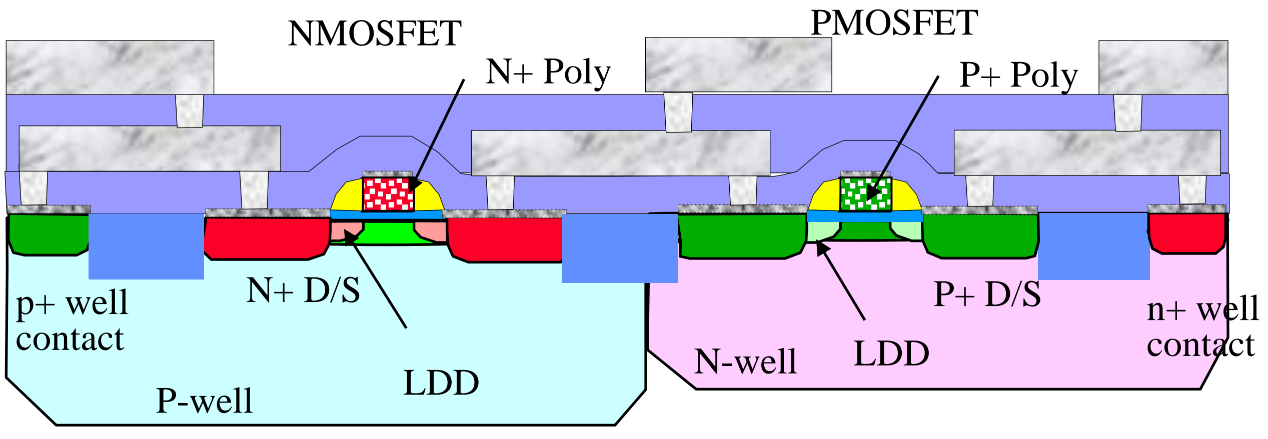
LVL 9 - N+ D/S

LVL 8 - CC

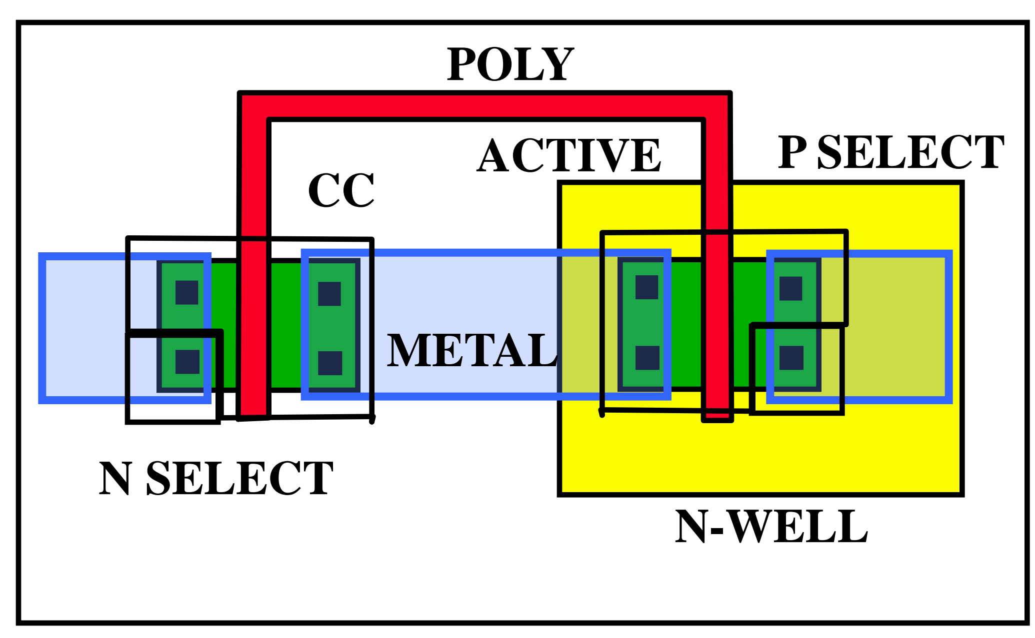
LVL 9 - METAL

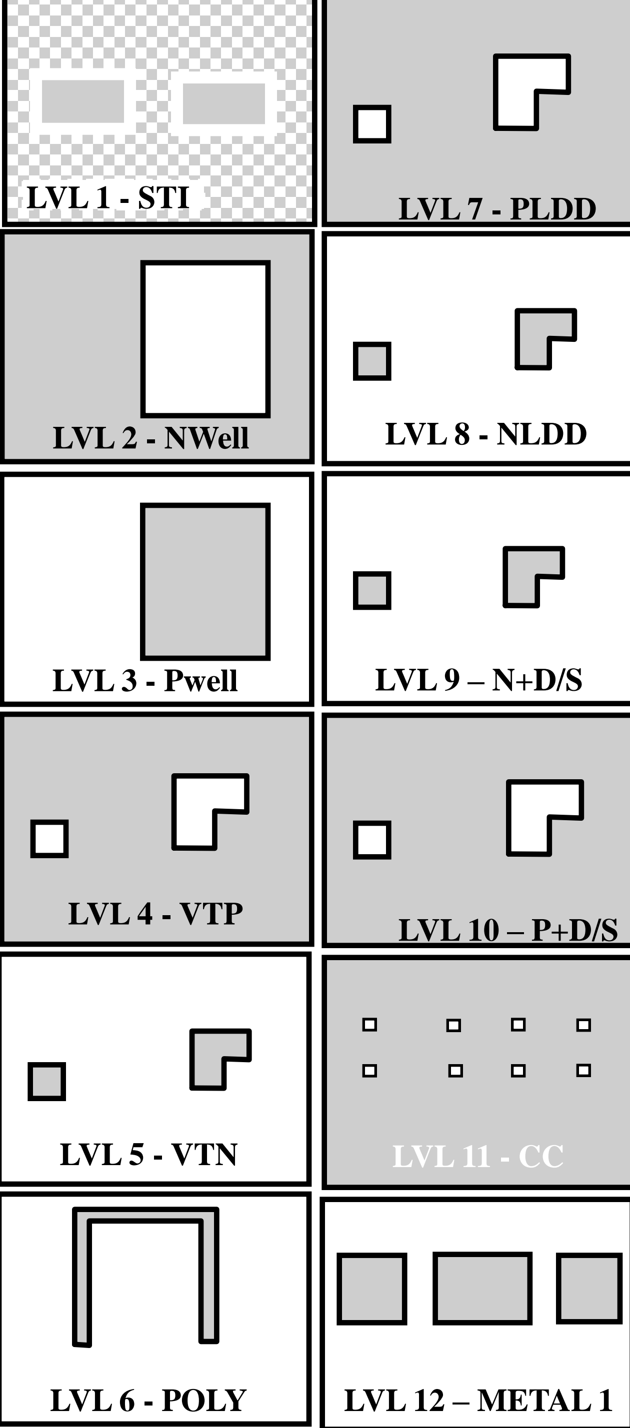
11 PHOTO LEVELS

RIT ADVANCED CMOS



12 PHOTO LEVELS + 2 FOR EACH ADDITIONAL METAL LAYER





MICROSYSTEM

Multi-Sensor MEMs Chip

Power Management

other

Signal Conditioning

Communication

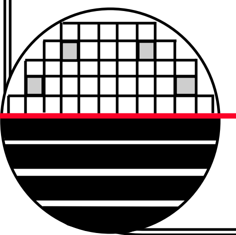
MICROCHIP

dsPIC33FJ32GP302/304,
dsPIC33FJ64GPX02/X04, and
dsPIC33FJ128GPX02/X04
Data Sheet

High-Performance, 16-bit
Digital Signal Controllers

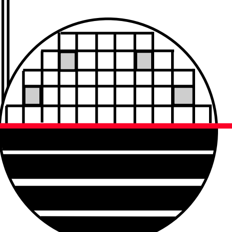
Micro Controller

Signal Conditioning
Electronics



REFERENCES

1. Silicon Processing for the VLSI Era, Volume 1 – Process Technology, 2nd, S. Wolf and R.N. Tauber, Lattice Press.
2. The Science and Engineering of Microelectronic Fabrication, Stephen A. Campbell, Oxford University Press, 1996.
3. MOSIS Scalable CMOS Design Rules for Generic CMOS Processes, www.mosis.org, and http://www.mosis.com/design/rules/



HOMEWORK – INTRO TO DIGITAL ELECTRONICS

1. Do a SPICE simulation to obtain the VTC for the inverter shown on page 16. Let the load resistor be 10K, the NMOS transistor SPICE model RITSUBN7, L=1u and W=40u. Extract Voh, Vol, Vil, ViH, Vinv, Noise Margin Low, Noise Margin High and Maximum current.
2. Do a SPICE simulation to obtain the VTC for the inverter shown on page 20. Let the NMOS and PMOS transistor SPICE model RITSUBN7 and RITSUBP7, L=1u and W=40u. Extract Voh, Vol, Vil, ViH, Vinv, Noise Margin Low, Noise Margin High and Maximum current.
3. Do a SPICE simulation to obtain the RISE TIME and FALL TIME for the inverter in problem 2 with a load capacitance equal to a fan out of 5 gates.
4. Show that the XOR realized with AND and OR gates is equivalent to an all NAND gate realization.

TRANSISTOR DIMENSIONS

L=2u

W=40u

Ad=As=40u x17u

=680p

Pd=Ps=2x(40u+17u)

=114u

Rd=Rs=100 ohm