ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Introduction to VLSI

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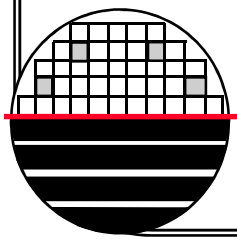

ADOBE PRESENTER

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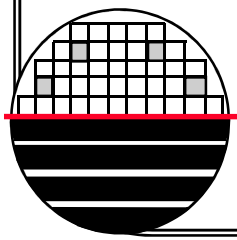
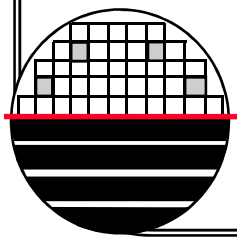


OUTLINE

- Introduction
- Process Technology
- Digital Electronics
  - Inverter with Resistor Load
  - CMOS Inverter
  - Voltage Transfer Curve (VTC)
    - Noise Margins, Rise/Fall Time
- MOSIS Layout Design Rules
- Standard Cell Design
  - Primitive, Basic, Macro Cells
- Maskmaking
- References
- Homework

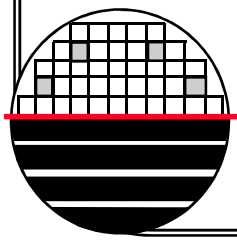


INTRODUCTION

VLSI is an acronym for Very Large Scale Integration. This includes Integrated circuits with greater than tens of thousands of transistors including multi-million or even billions of transistors.

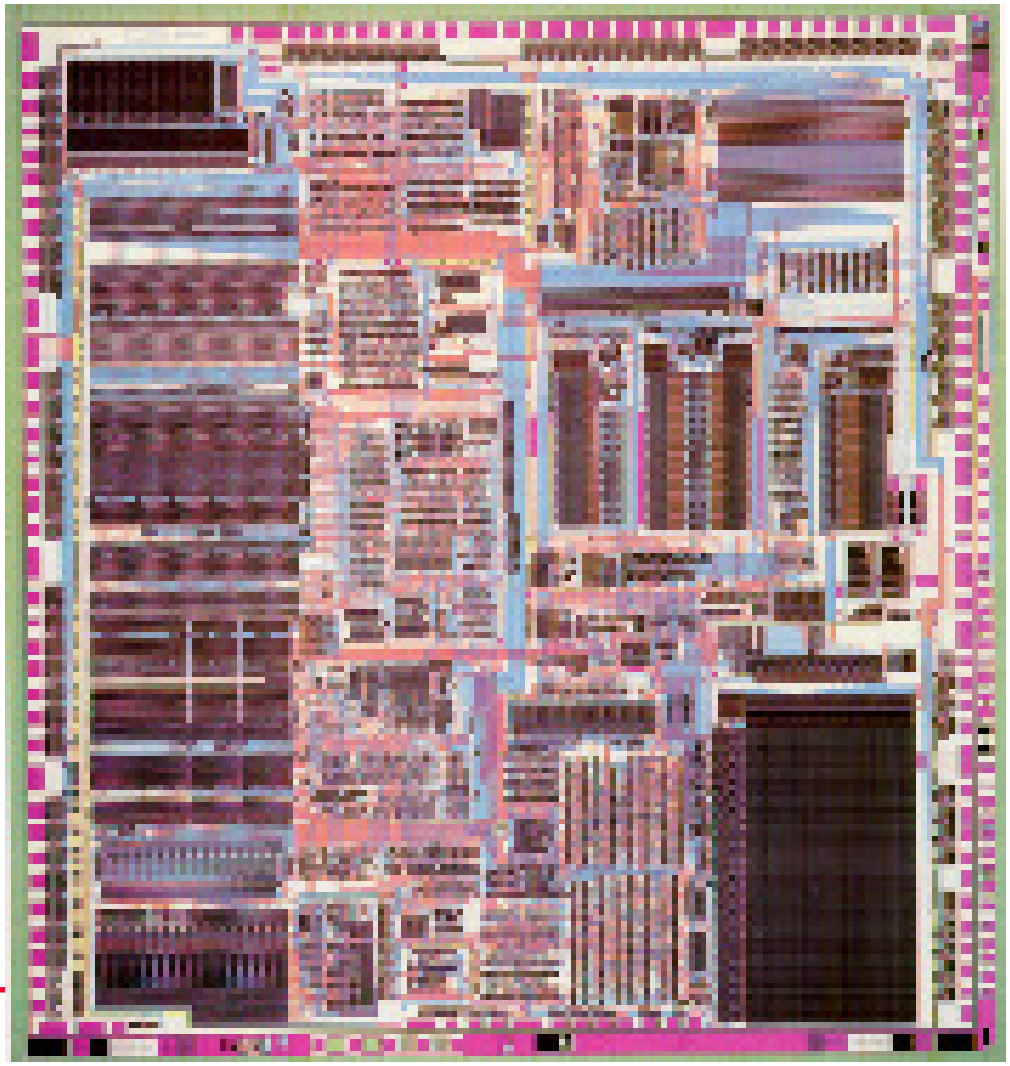
VLSI Design refers to methodologies and computer software tools for designing digital circuits with huge numbers of transistors. Some of theses methodologies and tools can also be applied to analog circuit design.

Software tools include schematic capture, SPICE analog simulation, switch level digital simulation, layout editors, layout versus schematic checking, design rule checking (DRC), auto place and routing and many more.



VLSI DESIGN

Computer software is used to check the layout, compare the layout to the schematic and make it possible to design circuits with millions of transistors with no errors.



VLSI DESIGN METHODOLOGIES

Full Custom Design

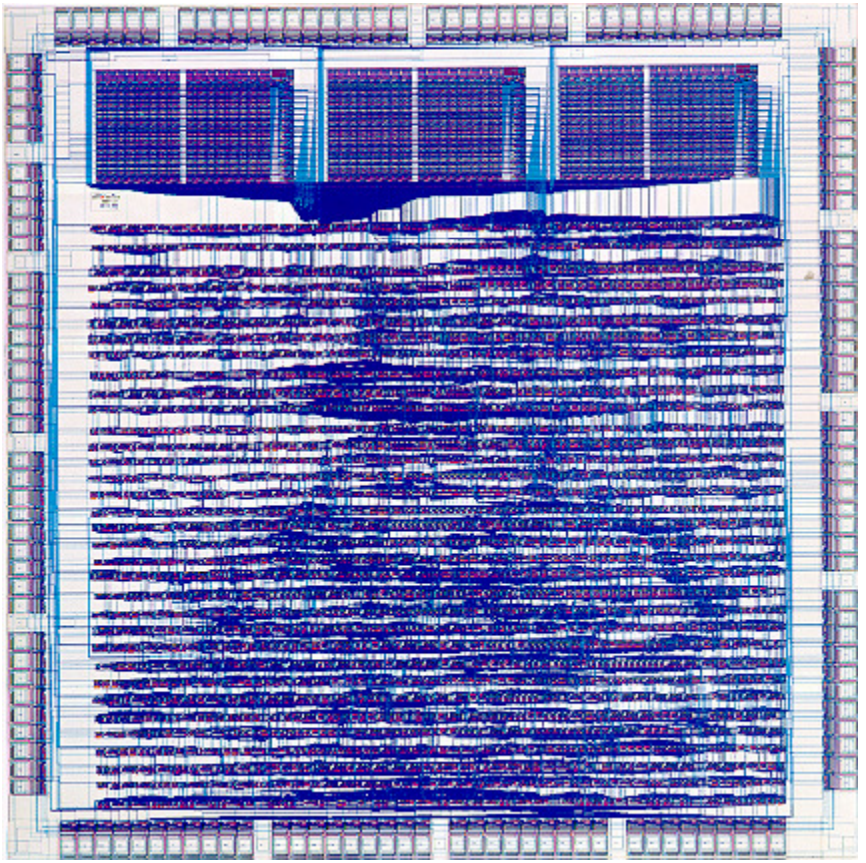
Direct control of layout and device parameters
Longer design time
High performance
fast, low power, dense

Standard Cell Design

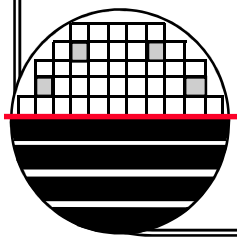
Easy to implement
Medium performance
Limited cell library selections

Gate Array or
Programmable Logic Array Design

Fastest design turn around

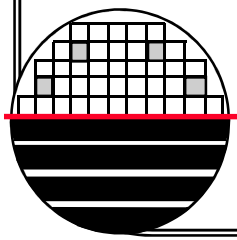


Process Technology



PROCESS SELECTION

It is not necessary to know all process details to do CMOS integrated circuit design. However the process determines important circuit parameters such as supply voltage and maximum frequency of operation. It also determines if devices other than PMOS and NMOS transistors can be realized such as poly-to-poly capacitors and EEPROM transistors. The number of metal interconnect layers is also part of the process definition. Starting wafer type determines if isolated n-wells or p-wells are available.



RIT PROCESSES

At RIT we use the Sub-CMOS and ADV-CMOS processes for most designs. In these processes the minimum poly length is 1µm and 0.5µm respectively. We use scalable MOSIS design rules with lambda equal to 0.5µm and 0.25µm. These processes use one layer of poly and two layers of metal.

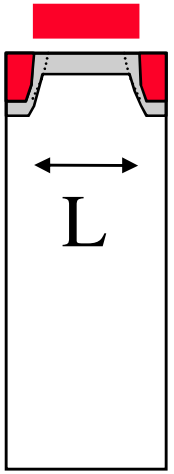
The examples on the following pages are designs that could be made with either of the above processes. As a result the designs are generous, meaning that larger than minimum dimensions are used. For example $\lambda = 0.5\mu m$ and minimum poly is 2λ but designed at 2.5µm because our poly etch is isotropic.

The design approach for digital circuits is to design primitive cells and then use the primitive cells to design basic cells which are then used in the project designs. A layout approach is also used that allows for easy assembly of these cells into more complex cells.

RIT SUBμ CMOS

RIT Subμ CMOS

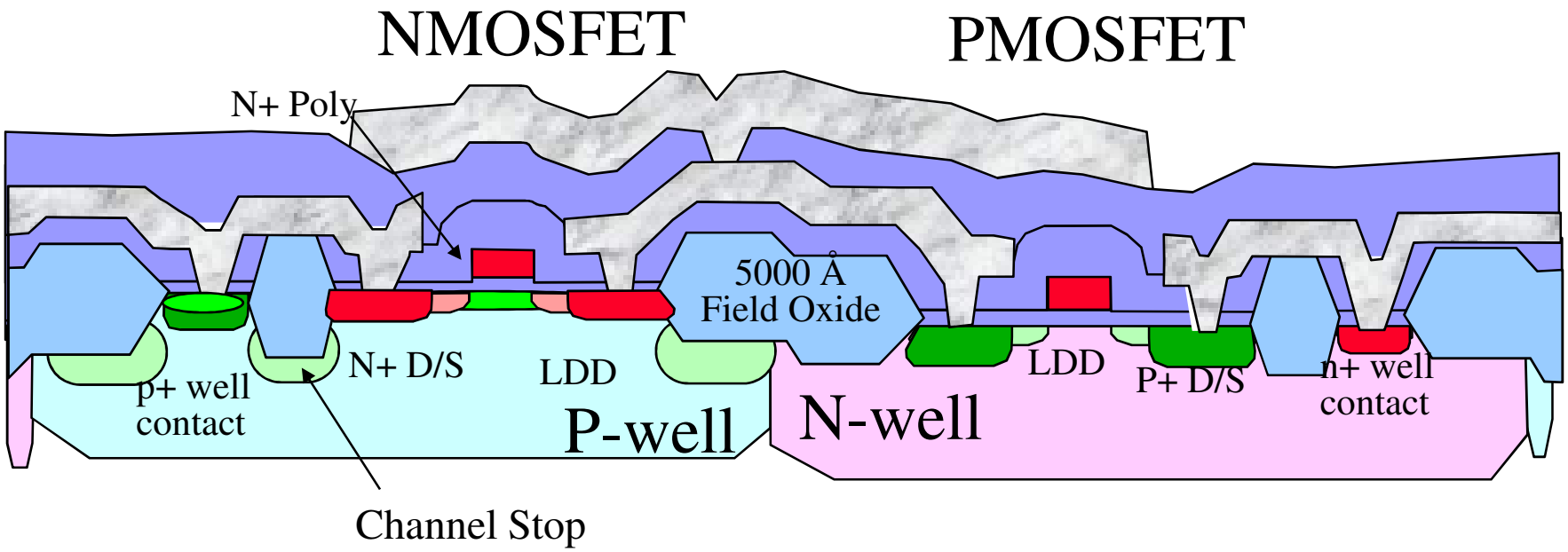
150 mm wafers
Nsub = 1E15 cm-3
Nn-well = 3E16 cm-3
Xj = 2.5 μm
Np-well = 1E16 cm-3
Xj = 3.0 μm
LOCOS
Field Ox = 6000 Å
Xox = 150 Å
Lmin= 1.0 μm
LDD/Side Wall Spacers
2 Layers Aluminum



Long Channel Behavior

3.3 Volt Technology
VT's = +/- 0.75 Volt
Robust Process (always works)
Fully Characterized (SPICE)

RIT SUBμ CMOS

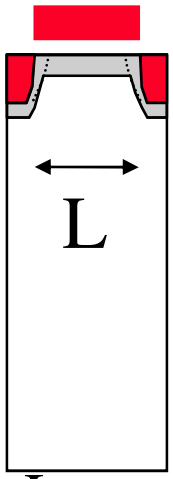


Substrate 10 ohm-cm

RIT ADVANCED CMOS VER 150

RIT Advanced CMOS

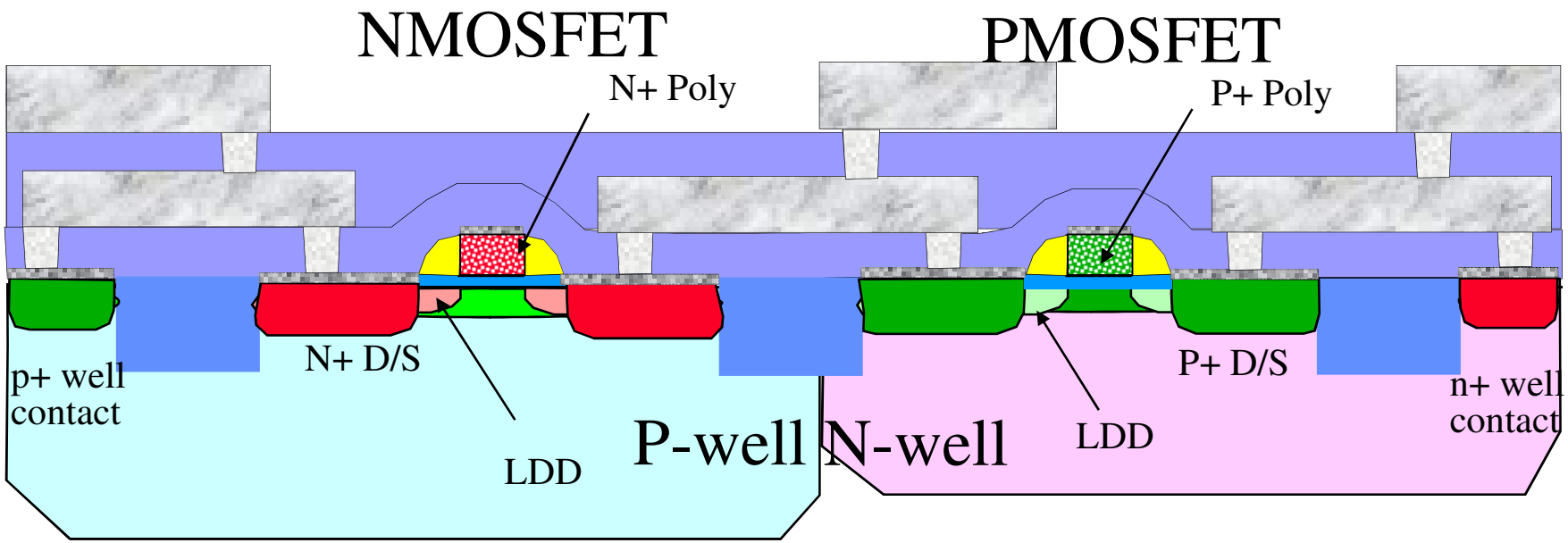
150 mm Wafers
Nsub = 1E15 cm-3 or 10 ohm-cm, p
Nn-well = 1E17 cm-3
Xj = 2.5 µm
Np-well = 1E17 cm-3
Xj = 2.5 µm
Shallow Trench Isolation
Field Ox (Trench Fill) = 4000 Å
Dual Doped Gate n+ and p+
Xox = 100 Å
Lmin = 0.5 µm , Lpoly = 0.35 µm, Leff = 0.11 µm
LDD/Nitride Side Wall Spacers
TiSi2 Salicide
Tungsten Plugs, CMP, 2 Layers Aluminum



Long Channel Behavior

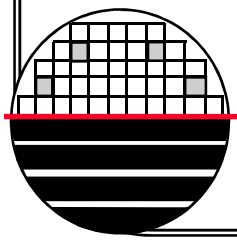
Vdd = 3.3 volts
Vto=+- 0.75 volts

RIT ADVANCED CMOS



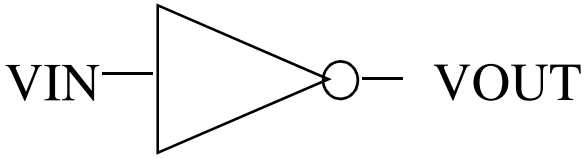
DIGITAL ELECTRONICS

Digital Electronics



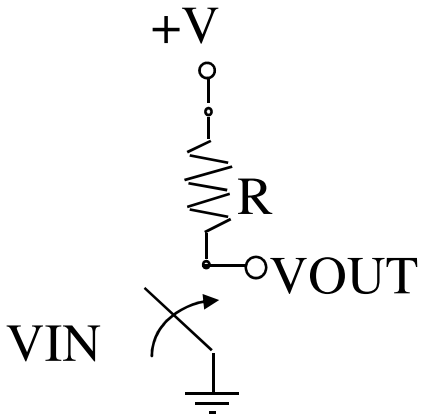
INVERTER

SYMBOL

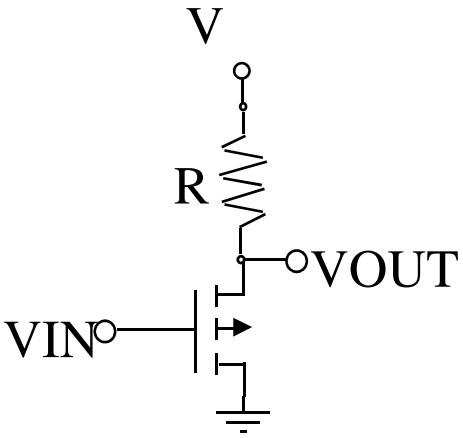


TRUTH TABLE

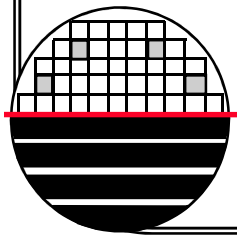
VIN	VOUT
0	1
1	0



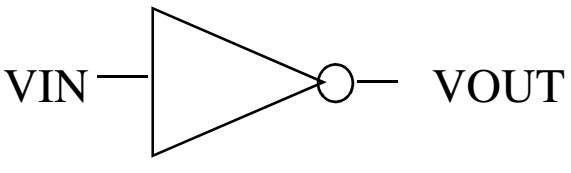
SWITCH

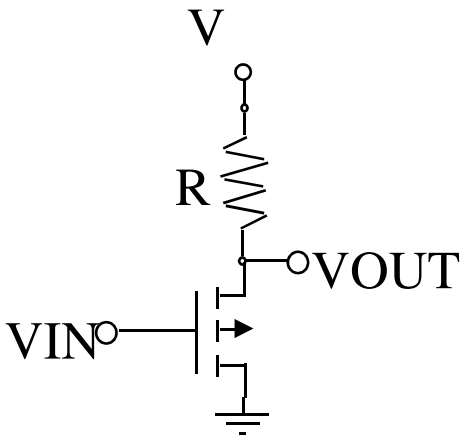


RESISTOR LOAD

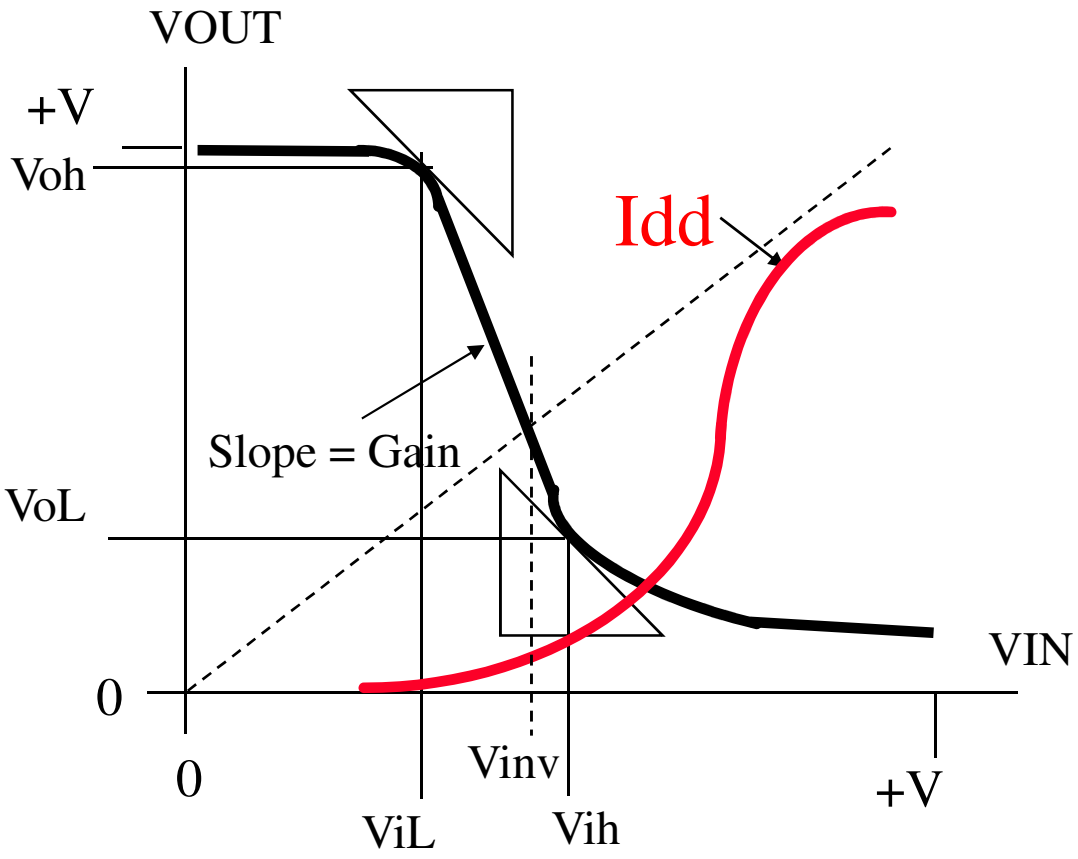


VOLTAGE TRANSFER CURVE



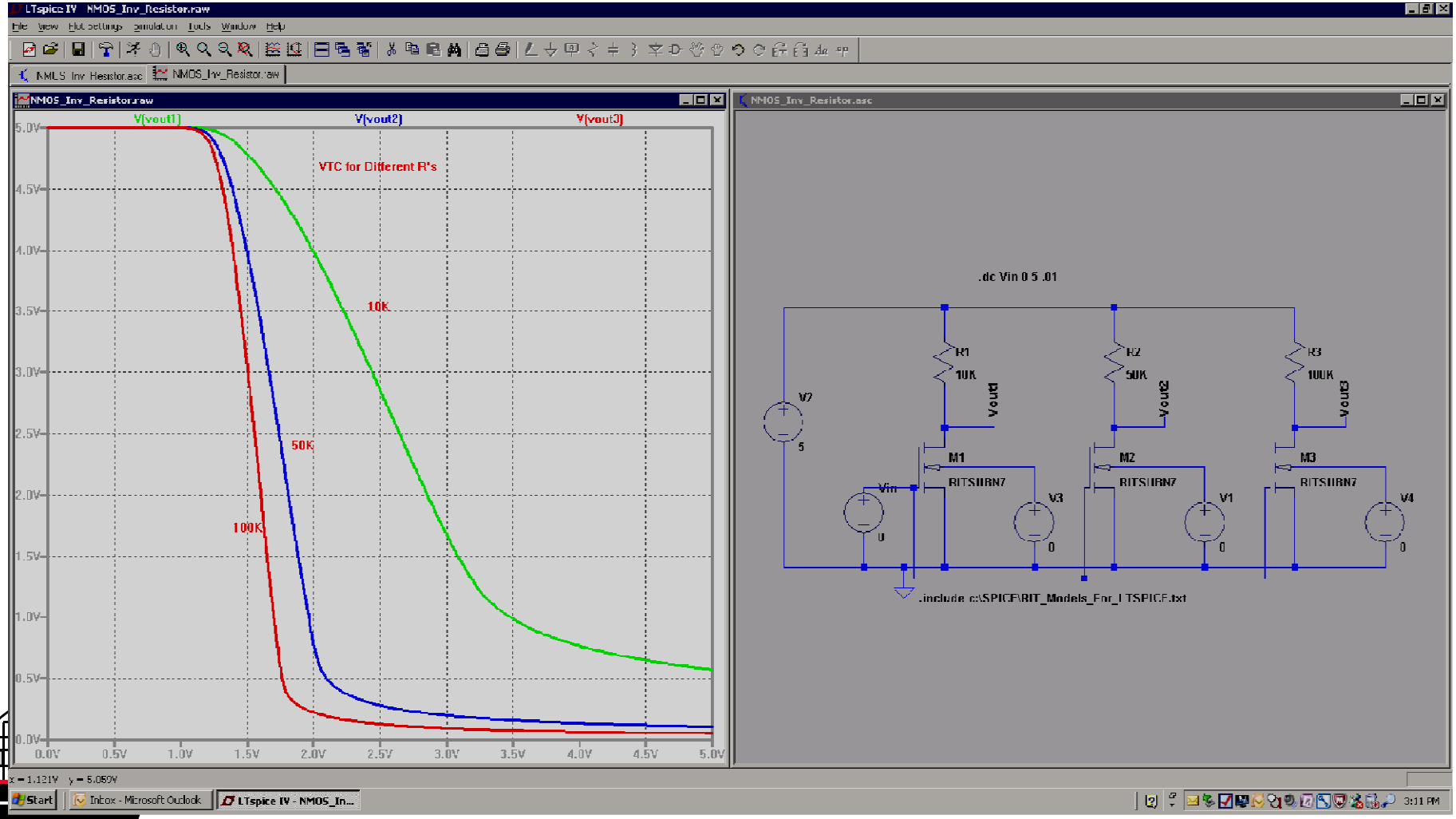


RESISTOR
LOAD

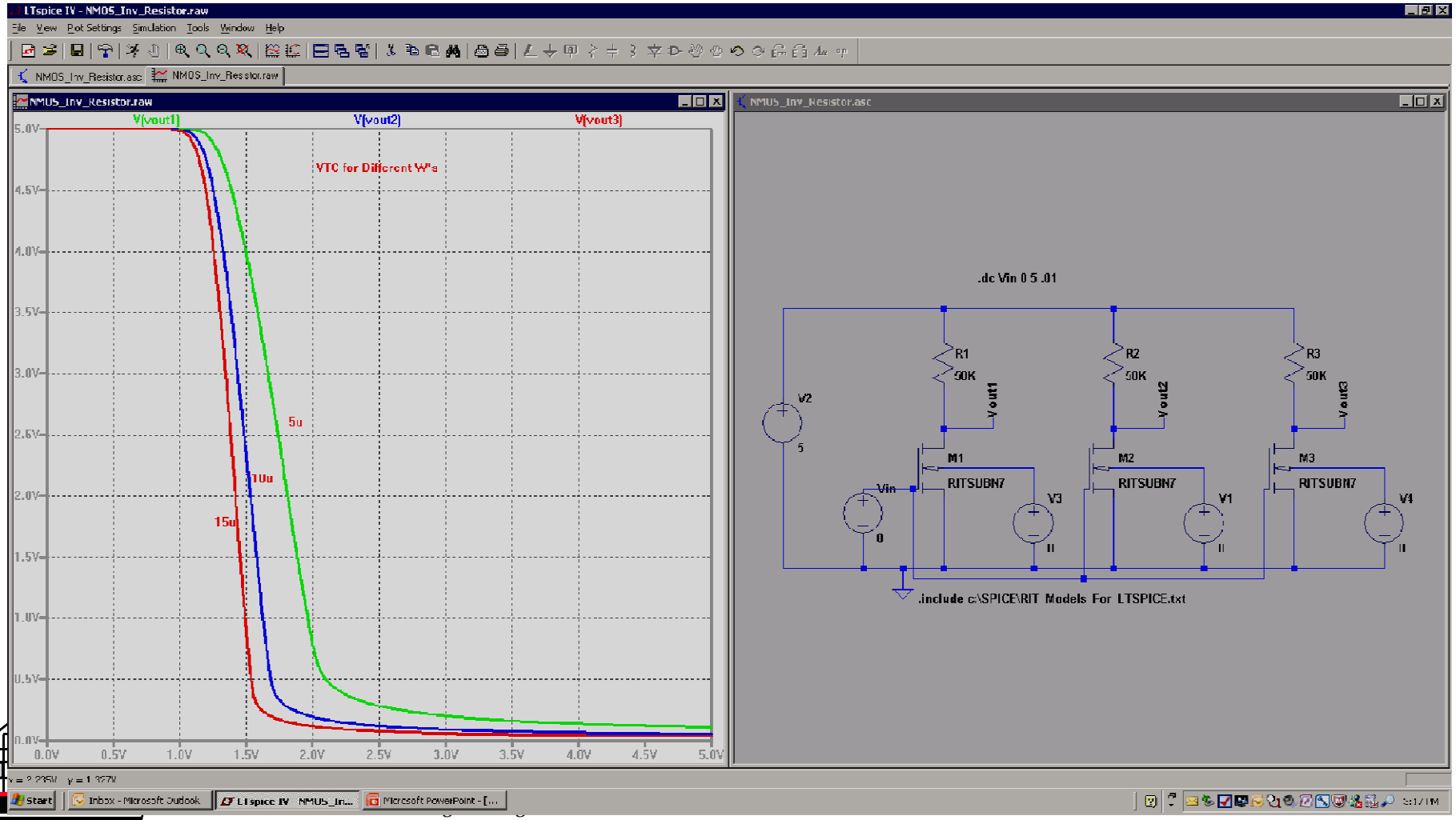


NML, noise margin low, Δ0 =ViL-VoL
NMH, oise margin high, Δ1 =VoH-ViH

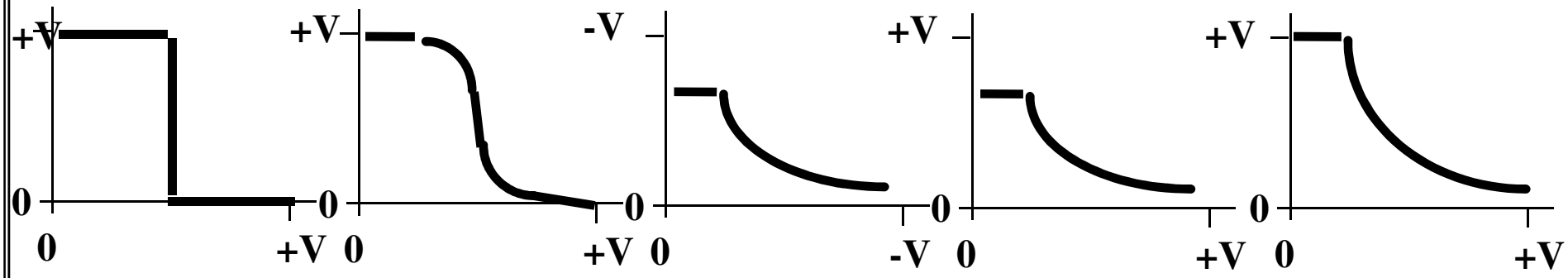
LTSPICE - INVERTER VTC FOR DIFFERENT RL

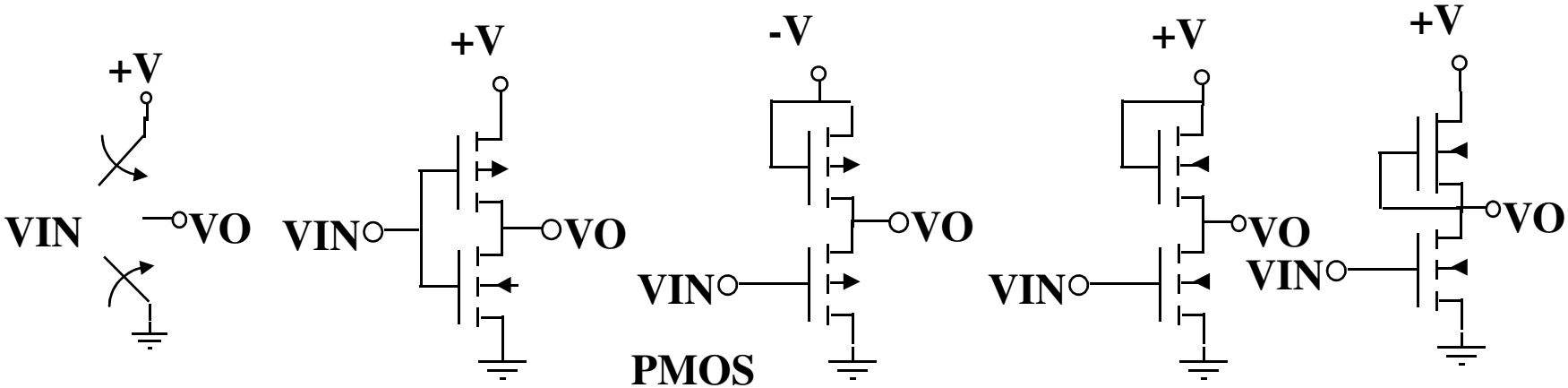


LTSPICE - INVERTER FOR DIFFERENT NMOS W



OTHER INVERTER TYPES - VOUT VS VIN (VTC)





SWITCH

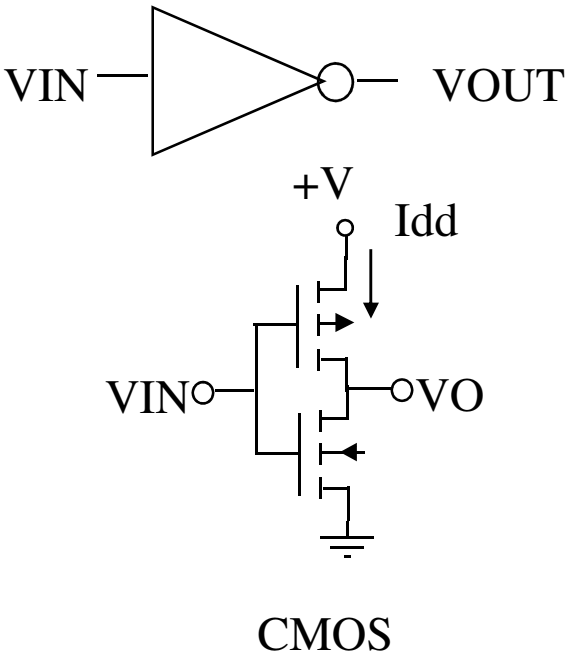
CMOS

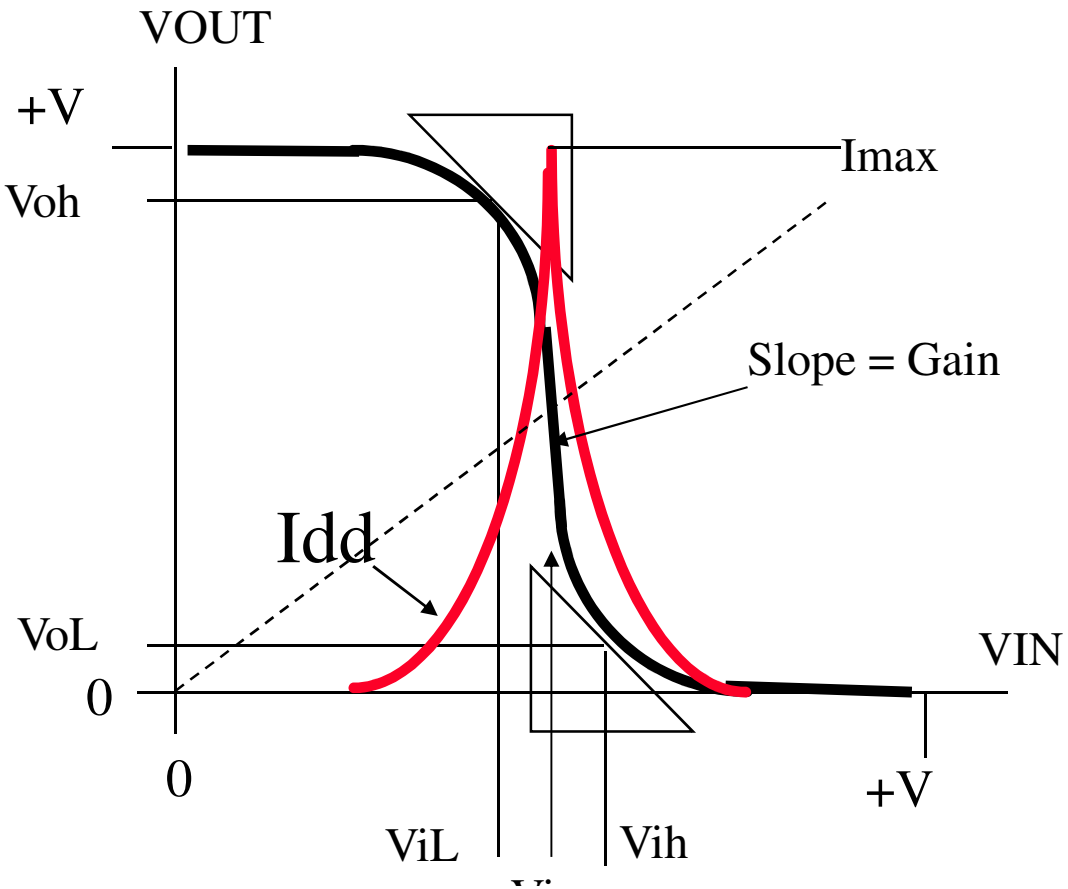
PMOS ENHANCEMENT LOAD

NMOS ENHANCEMENT LOAD

NMOS DEPLETION LOAD

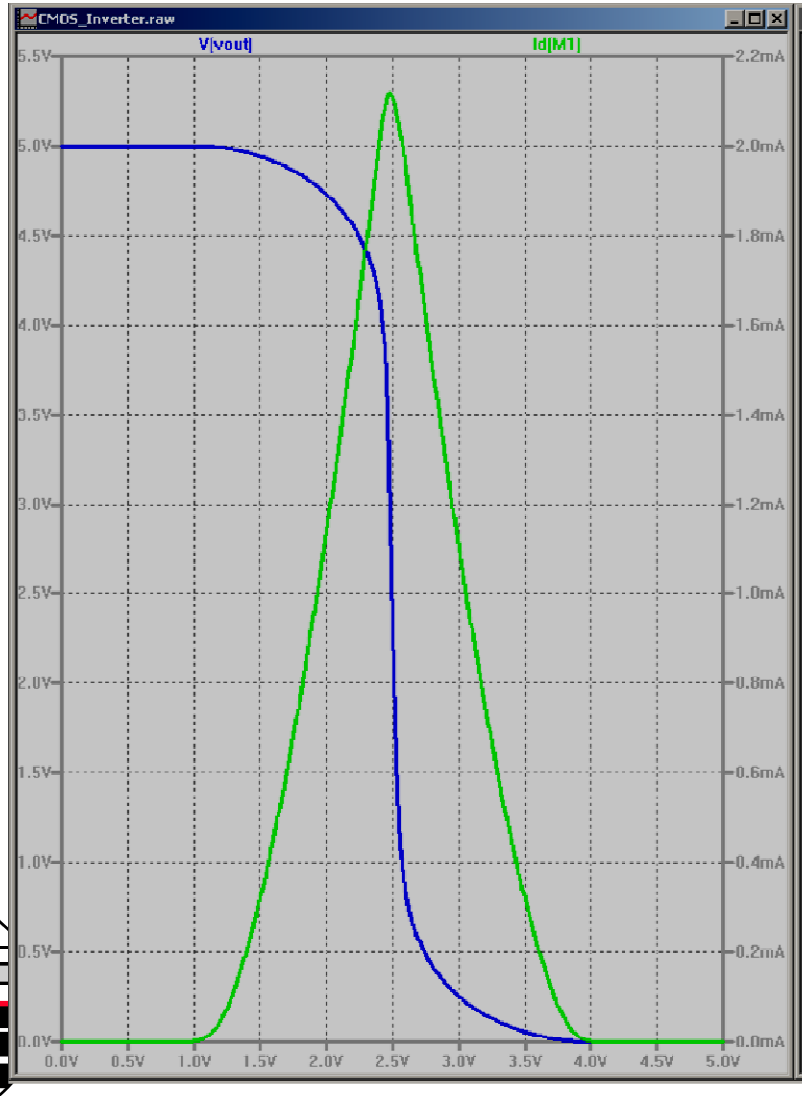
CMOS INVERTER

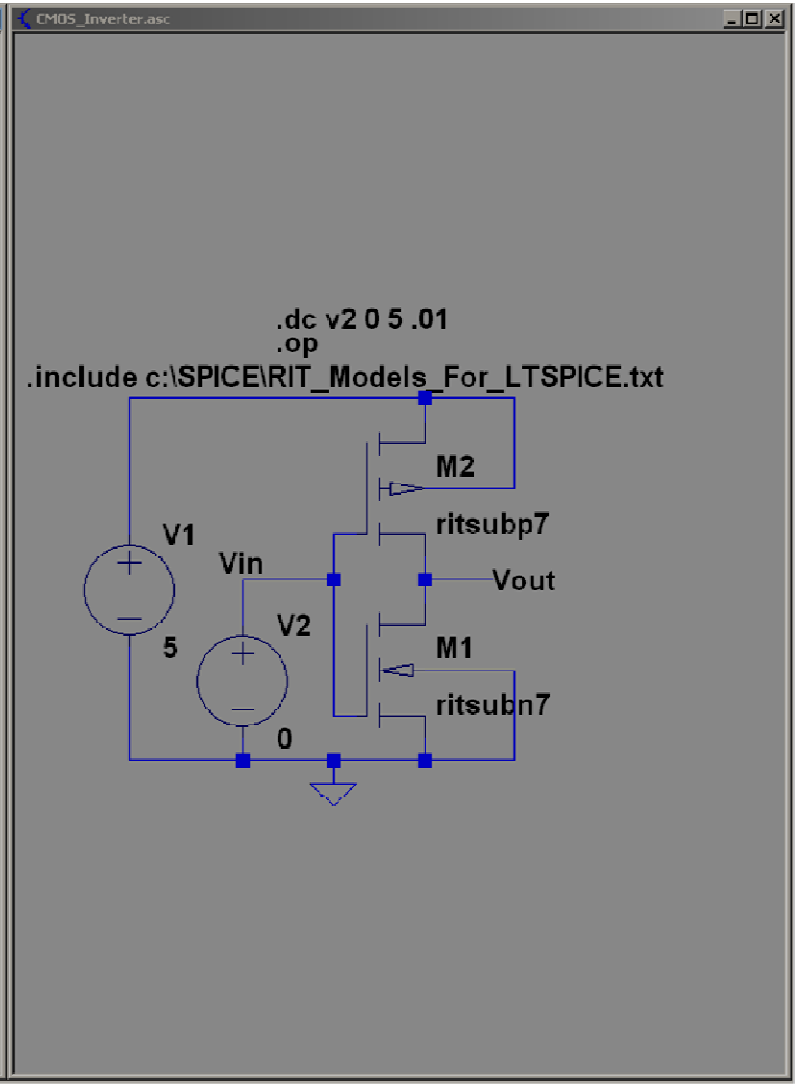




NML, noise margin low, Δ0 =ViL-VoL
NMH, oise margin high, Δ1 =VoH-ViH

LTSPICE – CMOS INVERTER

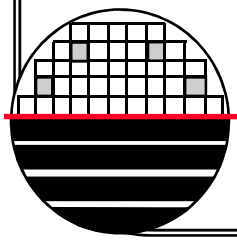




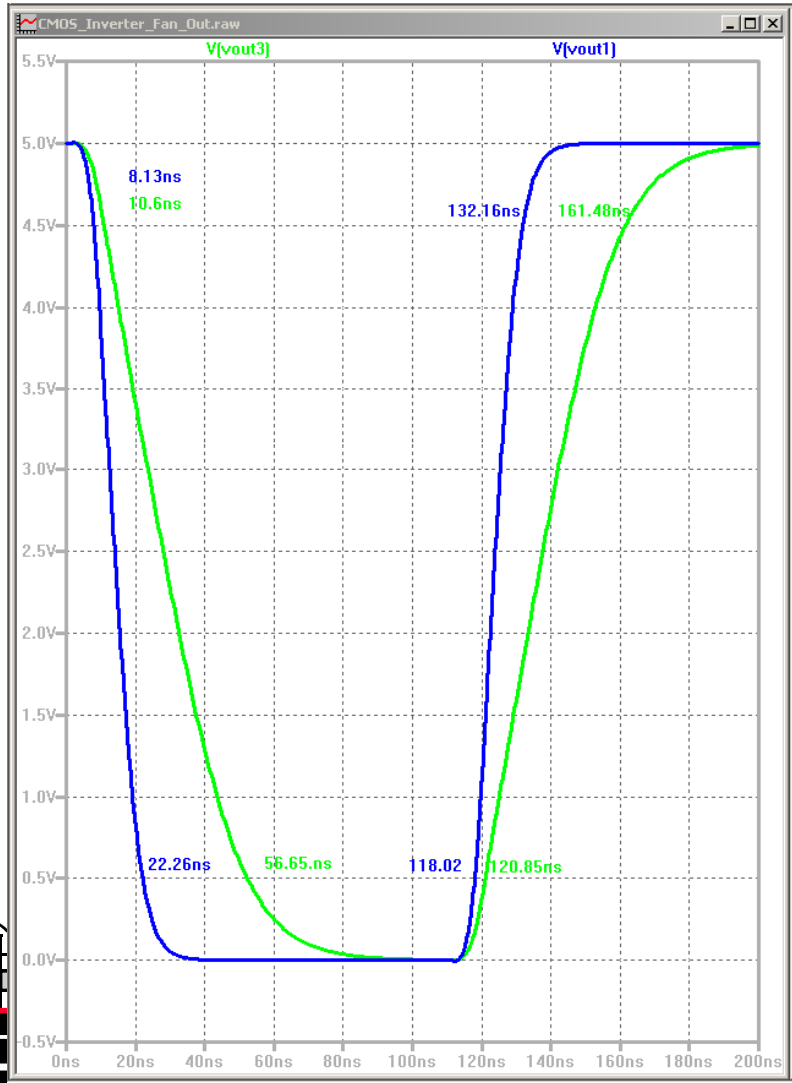
INVERTER PROPERTIES

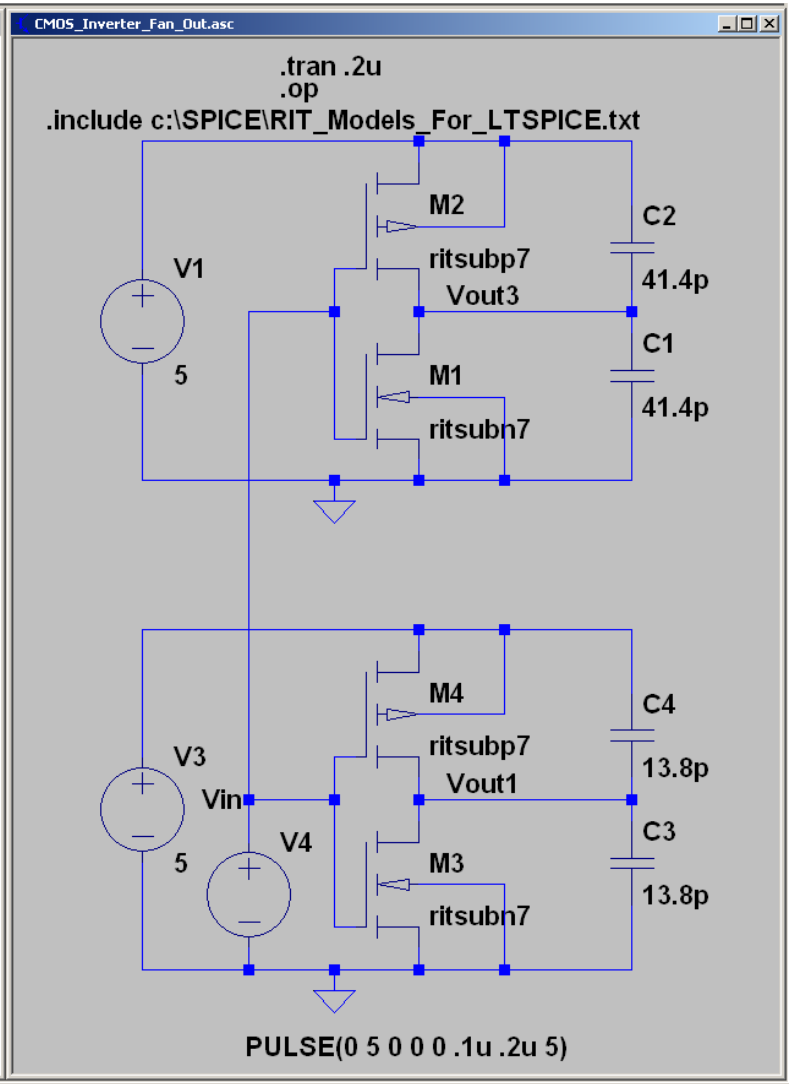
DC Properties
- Noise Margins
- Current, I
- Size

Transient Properties
- Rise/Fall Time
- Fan Out



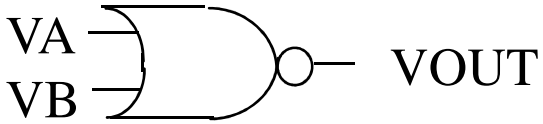
RISE TIME AND FALL TIME LTSPICE SIMULATION





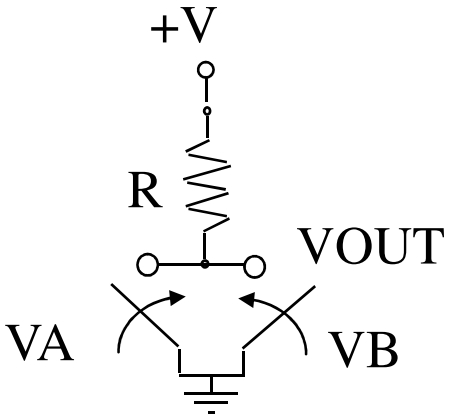
NOR GATE

SYMBOL

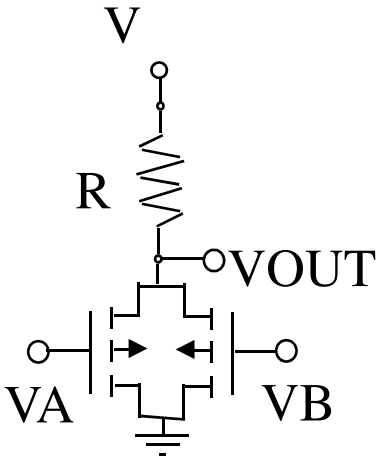


TRUTH TABLE

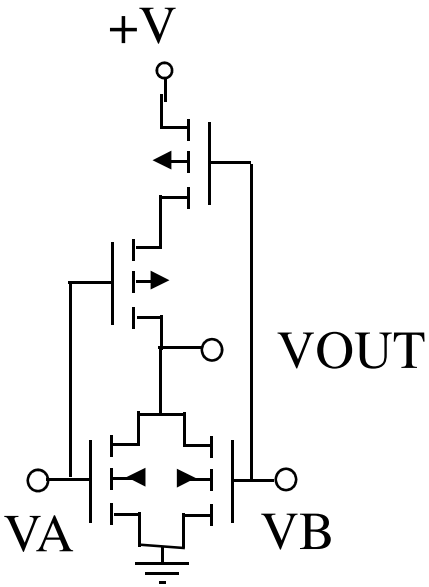
VA	VB	VOUT
0	0	1
0	1	0
1	0	0
1	1	0



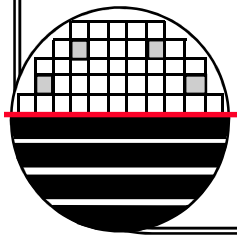
SWITCH



RESISTOR LOAD

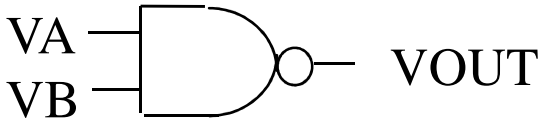


CMOS



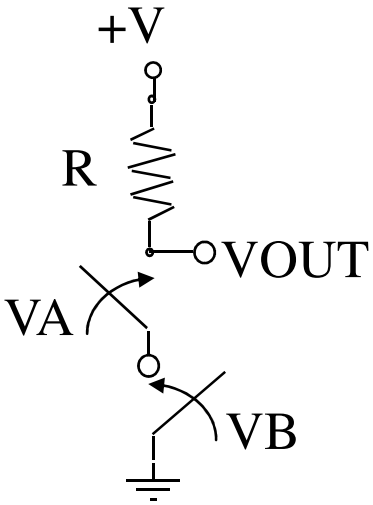
NAND GATE

SYMBOL



TRUTH TABLE

VA	VB	VOUT
0	0	1
0	1	1
1	0	1
1	1	0



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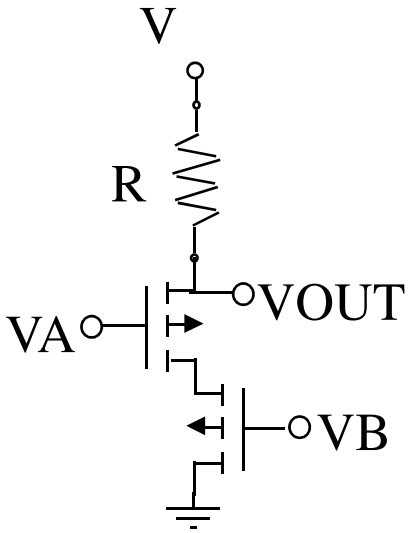

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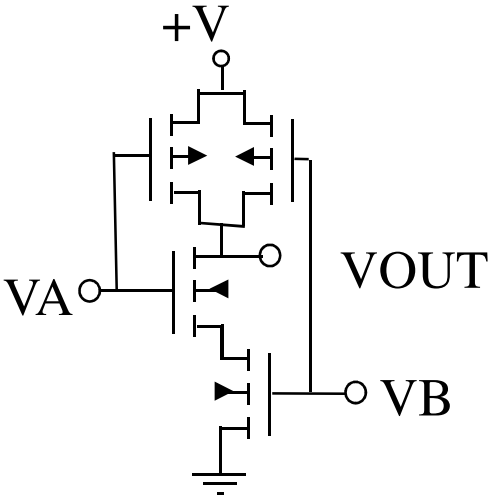
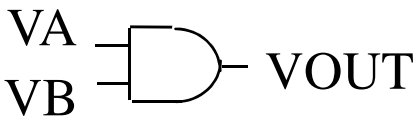


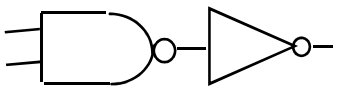
CMOS

OTHER LOGIC GATES

AND



VA	VB	VOUT
0	0	0
0	1	0
1	0	0
1	1	1



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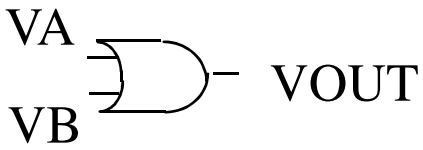
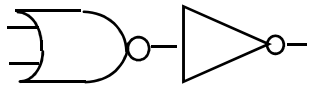
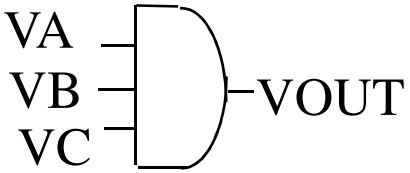


VA	VB	VOUT
0	0	0
0	1	1
1	0	1
1	1	1

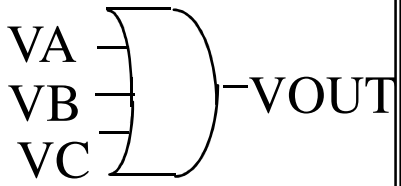


3 INPUT AND

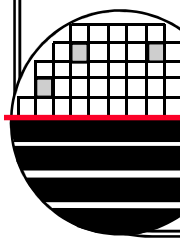


VA	VB	VC	VOUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3 INPUT OR



VA	VB	VC	VOUT
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



ADDITION IN BINARY

IN BASE 10

```
  7
 +2
 ___
  9
```

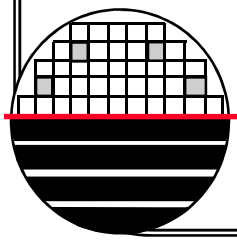
IN BINARY

```
11          CARRY
0111
0010
____
1001        SUM
```

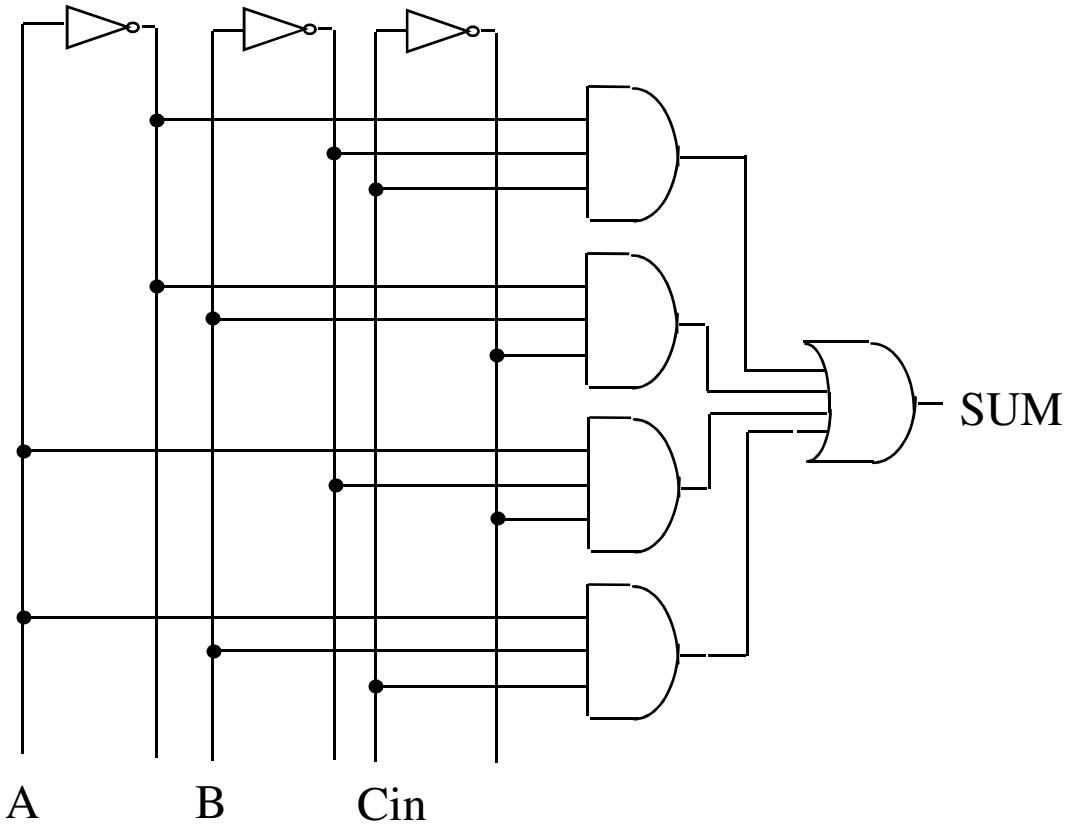
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

TRUTH TABLE
FOR ADDITION
RULES

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



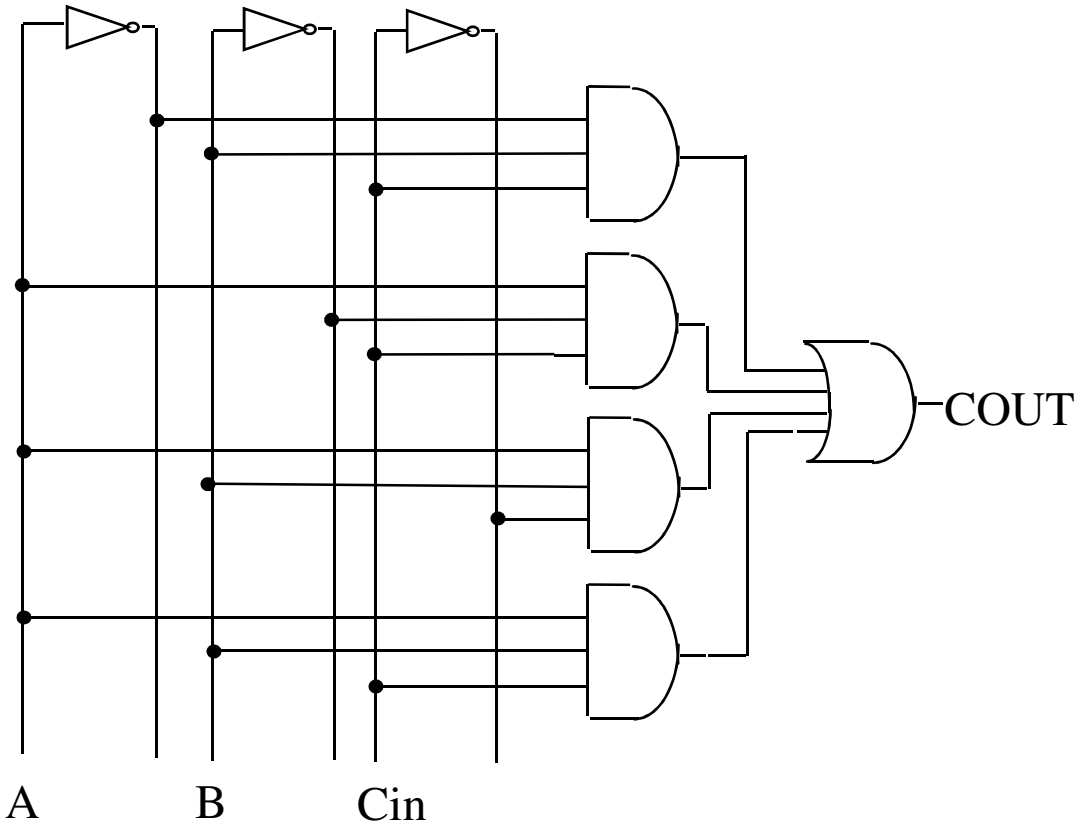
AND-OR CIRCUIT REALIZATION OF SUM



TRUTH TABLE
FOR ADDITION
RULES

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

CIRCUIT REALIZATION OF CARRY OUT (COUT)

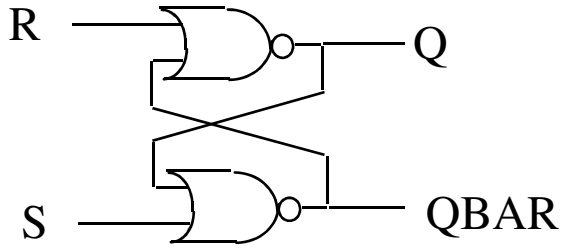


TRUTH TABLE
FOR ADDITION
RULES

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

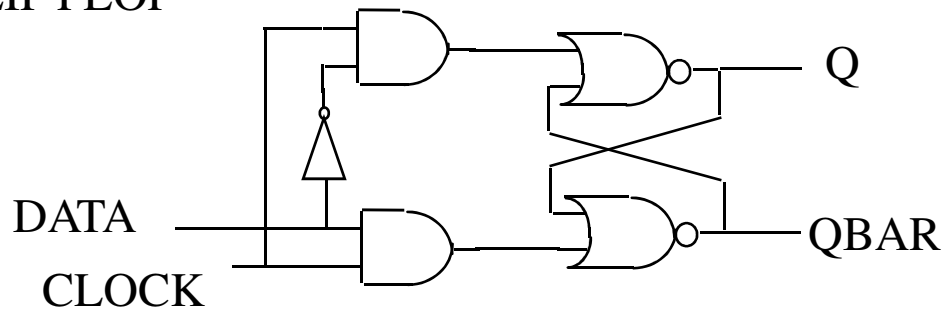
FILP-FLOPS

RS FLIP FLOP



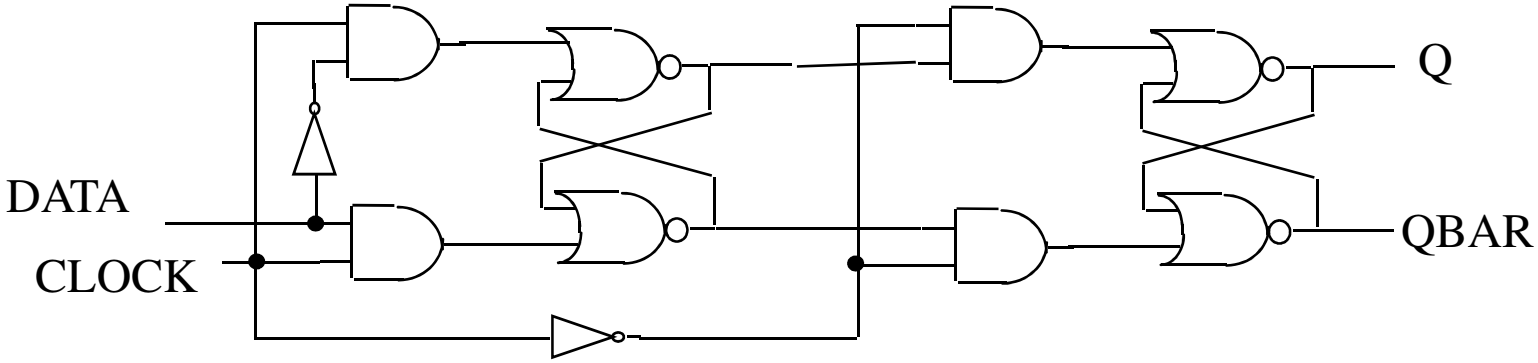
R	S	Q
0	0	Qn-1
0	1	1
1	0	0
1	1	INDETERMINATE

D FLIP FLOP

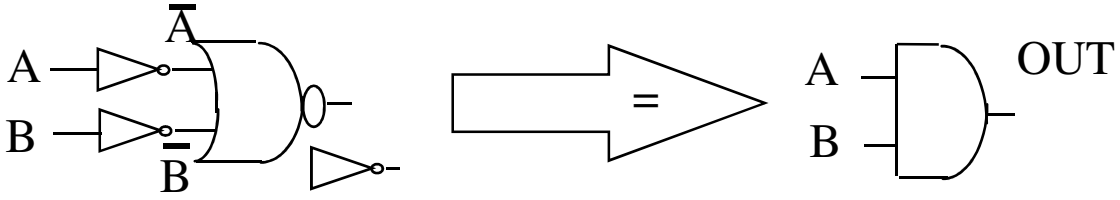


Q=DATA IF CLOCK IS HIGH
IF CLOCK IS LOW Q=PREVIOUS DATA VALUE

MASTER-SLAVE D FLIP FLOP

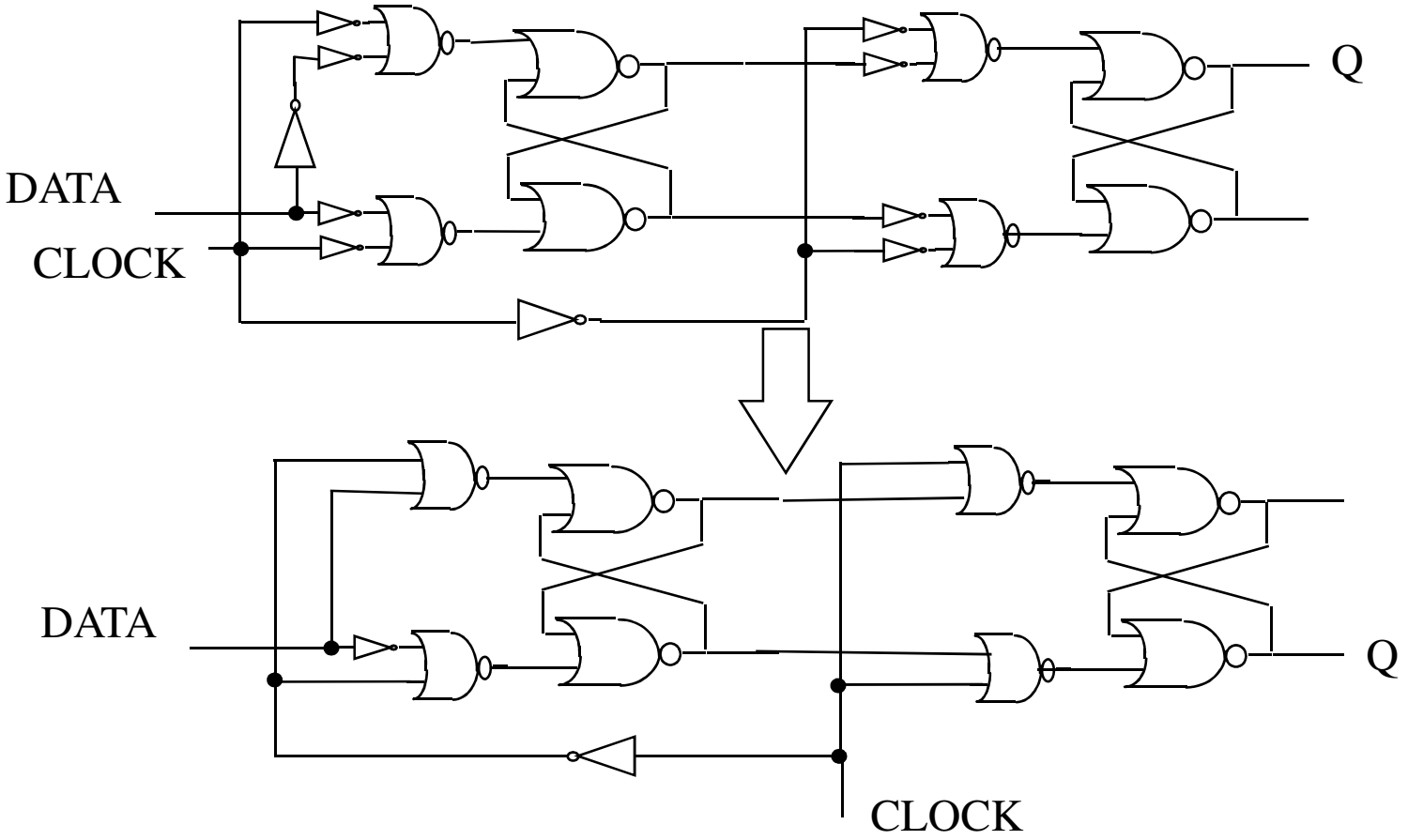


NEGATED INPUT NOR IS EQUAL TO AND



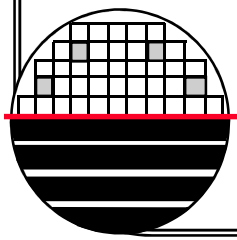
A	B	$\overline{A}$	$\overline{B}$	$\overline{OUT}$	OUT
0	0	1	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1

ALL NOR MASTER SLAVE D FLIP FLOP

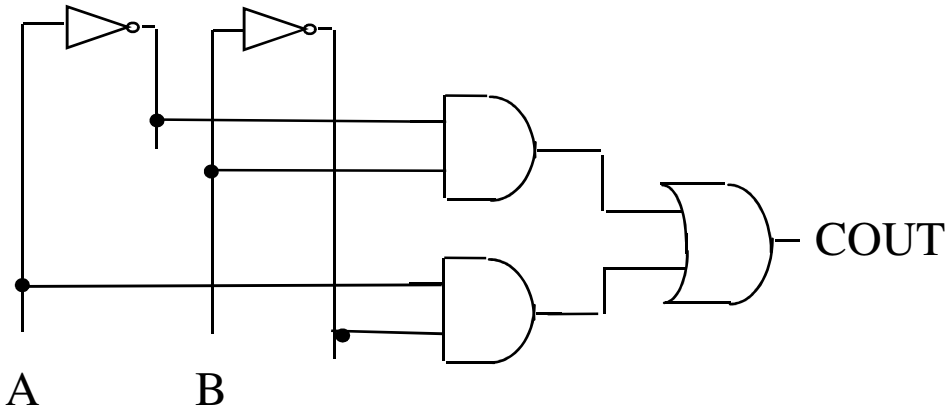


EQUAVILANT REALIZATIONS

AND-OR realizations are easily derived from truth table description of a circuits performance. Replacing the AND and OR gates with all NOR gates is equivalent. Replacing the AND and OR gates with all NAND gates is equivalent.



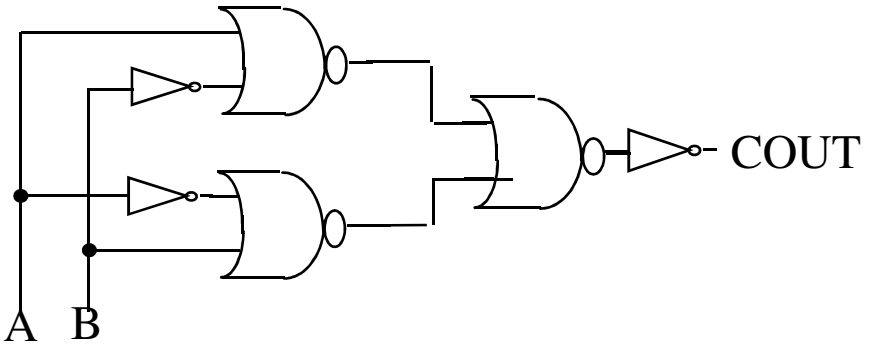
CIRCUIT REALIZATION FOR XOR

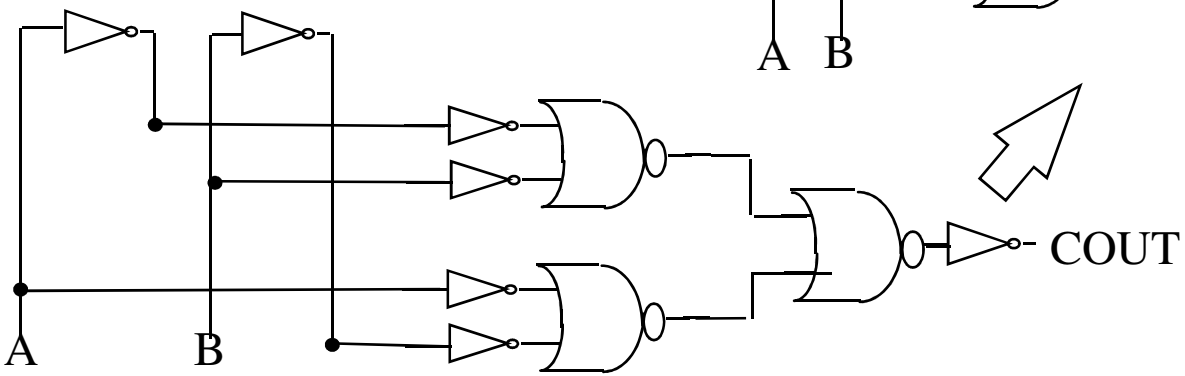


Exclusive OR

XOR

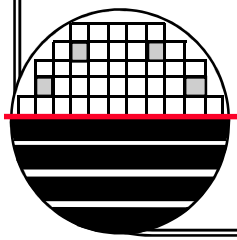
VA	VB	VOUT
0	0	0
0	1	1
1	0	1
1	1	0





LAYOUT

Layout Design Rules

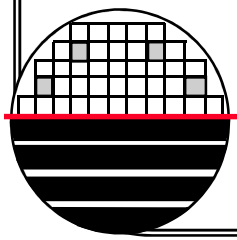


LAMBDA BASED DESIGN RULES

The design rules may change from foundry to foundry or for different technologies. So to make the design rules generic the sizes, separations and overlap are given in terms of numbers of lambda (λ). The actual size is found by multiplying the number by the value for lambda for that specific foundry.

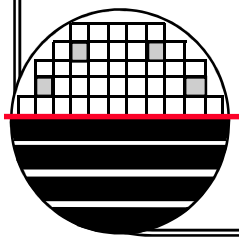
For example:

RIT PMOS process λ = 10 μm and minimum metal width is 3 λ so that gives a minimum metal width of 30 μm. The RIT SUB-CMOS process has λ = 0.5 μm and the minimum metal width is also 3 λ so minimum metal is 1.5 μm but if we send our CMOS designs out to industry λ might be 0.25 μm so the minimum metal of 3 λ corresponds to 0.75 μm. In all cases the design rule is the minimum metal width = 3 λ

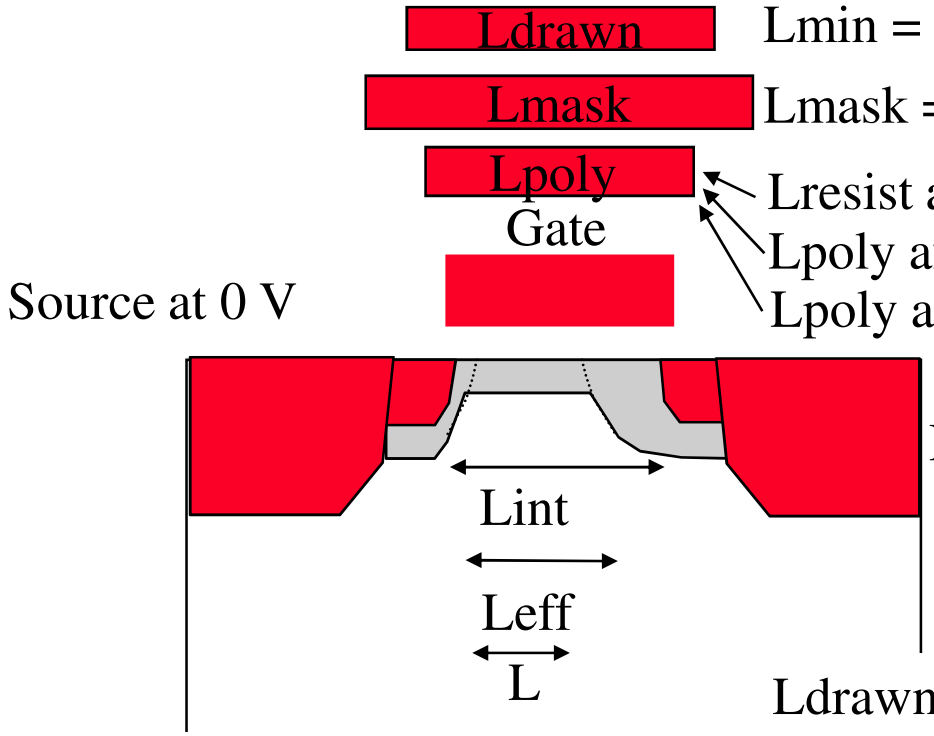


DESIGN RULES

We will use a modified version of the MOSIS TSMC 0.35 2P 4M design rules. Eventually we hope to be compatible with MOSIS but new process technology needs to be developed at RIT to do that (PECVD Tungsten, 4 layer metal). We use one layer of poly and two layers of metal. We will use the same design layer numbers with additional layers as defined on the following pages for manufacturing/maskmaking enhancements. Many of the designs will use minimum drawn poly gate lengths of 2µm where circuit architecture is the main purpose of the design. Minimum size devices (Drawn Poly = 0.5µm, etc.) are included to develop manufacturing process technology. These transistors (0.5µm drawn) yield 0.35µm Leff and are equivalent to the TSMC 0.35µm transistors.



LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L



Lambda = design rule parameter, λ, ie 0.25µm

Lmin = min drawn poly length, 2λ 0.50µm

Lmask = ? Depends on +/-bias 1.00µm x 5

Lresist after photo (resist trimming??) 0.50µm

Lpoly after poly etch 0.40µm

Lpoly after poly reoxidation 0.35µm

0.30µm

0.20µm

0.11µm

Ldrawn = what was drawn

Internal Channel Length, Lint =distance between junctions, including under diffusion

Effective Channel Length, Leff = distance between space charge layers,Vd = Vs= 0

Channel Length, L, = distance between space charge layers, when Vd= what it is

Extracted Channel Length Parameters = anything that makes the fit good (not real)

MOSIS TSMC 0.35 2POLY 4 METAL PROCESS

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http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html#tech-codes

MOSIS SCMOS Technology Codes and Layer Maps

SCN4M and SCN4M_SUBM

This is the layer map for the technology codes SCN4M and SCN4M_SUBM using the MOSIS Scalable CMOS layout rules (SCMOS), and only for SCN4M and SCN4M_SUBM. For designs that are laid out using other design rules (or technology codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

SCN4M: Scalable CMOS N-well, 4 metal, 1 poly, silicided. Silicide block and thick oxide option available only on the TSMC process.

SCN4M_SUBM: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

Fabricated on TSMC, AMIS, and Agilent/HP 0.35 micron process runs. See "Notes" section of layer map for foundry-specific options.

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	
ACTIVE	43	CAA		2	
THICK_ACTIVE	60	CTA		24	Optional for TSMC; not available for Agilent/HP nor AMIS
POLY	46	CPG		3	
SILICIDE_BLOCK	29	CSB		20	Optional for Agilent/HP; not available for AMI
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	
METAL3	62	CM3	CMT	15	
VIA3	30	CV3	CVT	21	
METAL4	31	CM4	CMQ	22	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME

MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

MASK LAYER NAME	MENTOR NAME	GDS #	COMMENT
N WELL	N_well.i	42	
ACTIVE	Active.i	43	
POLY	Poly.i	46	
N PLUS	N_plus_select.i	45	
P PLUS	P_plus_select.i	44	
CONTACT	Contact.i	25	Active_contact.i 48 poly_contact.i 47
METAL1	Metal1.i	49	
VIA	Via.i	50	
METAL2	Metal2.i	51	
VIA2	Via2.i	61	Under Bump Metal
METAL3	Metal3.i	62	Solder Bump

These are the main design layers up through metal two

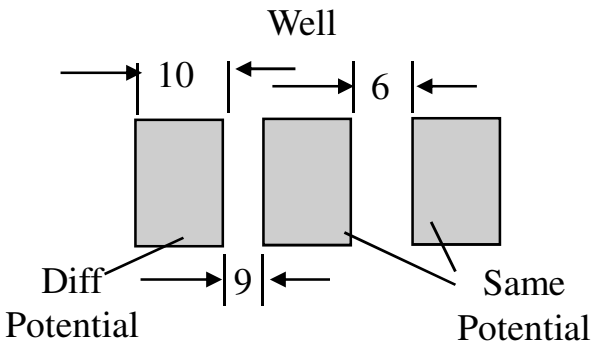
MORE LAYERS USED IN MASK MAKING

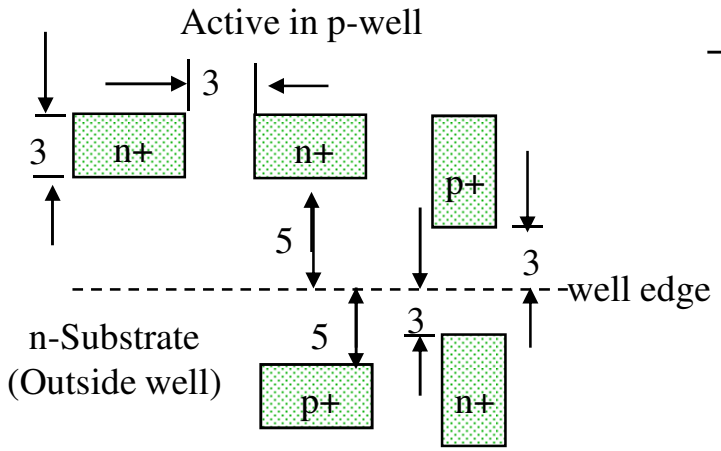
LAYER	NAME	GDS	COMMENT
	cell_outline.i	70	Not used
	alignment	81	Placed on first level mask
	nw_res	82	Placed on nwell level mask
	active_lettering	83	Placed on active mask
	channel_stop	84	Overlay/Resolution for Stop Mask
	pmos_vt	85	Overlay/Resolution for Vt Mask
	LDD	86	Overlay/Resolution for LDD Masks
	p plus	87	Overlay/Resolution for P+ Mask
	n plus	88	Overlay/Resolution for N+ Mask
	tile_exclusion	89	Areas for no STI tiling

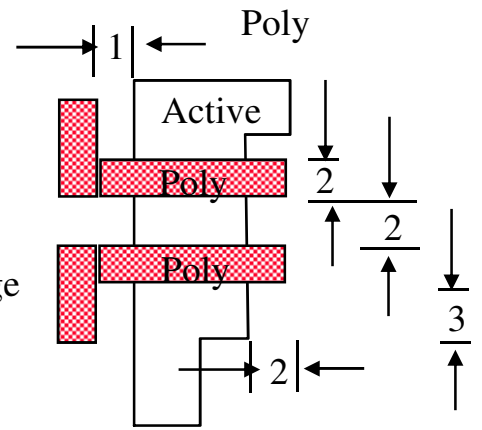
These are the additional layers used in layout and mask making

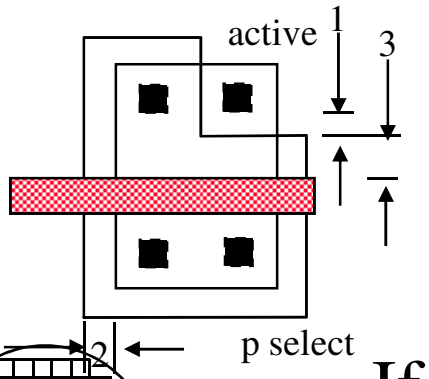
MOSIS LAMBDA BASED DESIGN RULES

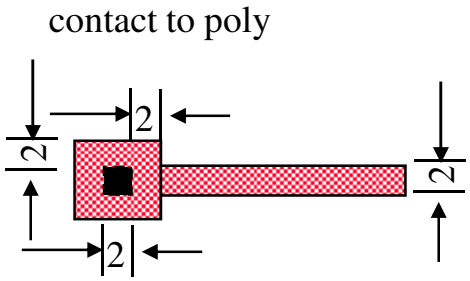
http://www.mosis.com/design/rules/

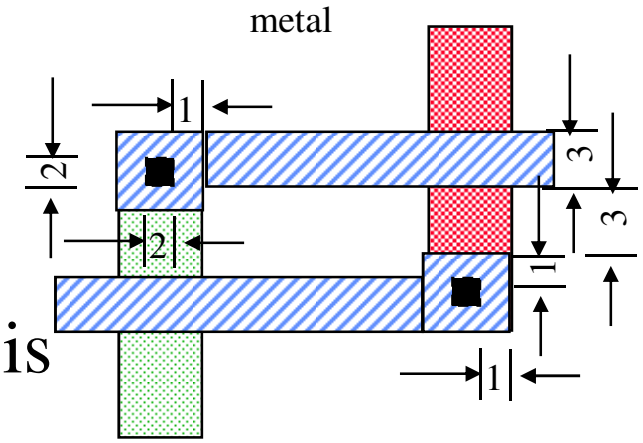








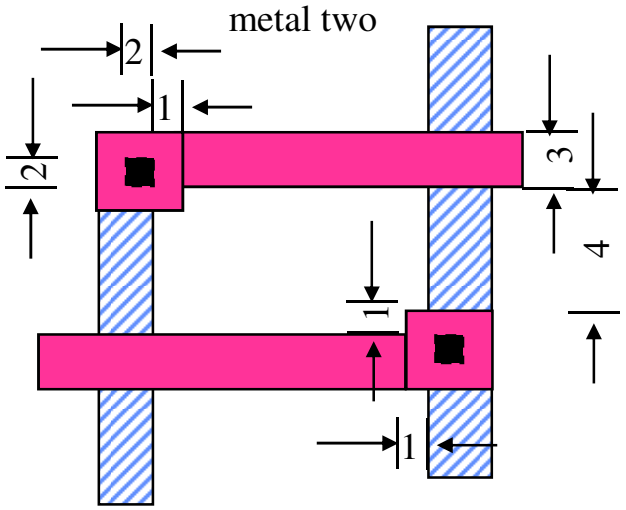




If λ = 1 µm then contact is
2 µm x 2 µm

MOSIS LAMBDA BASED DESIGN RULES

http://www.mosis.com/design/rules/



MOSIS Educational Program

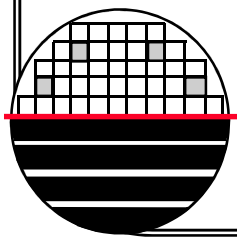
Instructional Processes Include:
AMI $\lambda = 0.8\ \mu m$ SCMOS Rules
AMI $\lambda = 0.35\ \mu m$ SCMOS Rules

Research Processes:
go down to poly length of 65nm

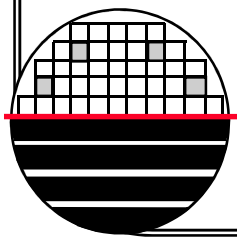
MOSIS REQUIREMENTS

MOSIS requires that projects have successfully passed LVS (Layout Versus Schematic) and DRC (Design Rule Checking). The MENTOR tools for LVS and DRC (as they are set up at RIT) require separate N-select and P-select levels in order to know an NMOS transistor from a PMOS transistor. Although either an N-well, P-well or both will work for a twin well process, we have set up our DRC to look for N-well. (Also since we use a p-type starting wafer we can not have isolated p-wells but we can have isolated n-wells, thus drawing separate n-wells can be useful for some circuit designs.)

http://www.mosis.com



Digital Circuit Layout



DIGITAL CIRCUITS

The design approach for digital circuits is to design primitive cells and then use the primitive cells to design basic cells which are then used in the project designs. A layout approach is also used that allows for easy assembly of these cells into more complex cells.

Primitive Cells

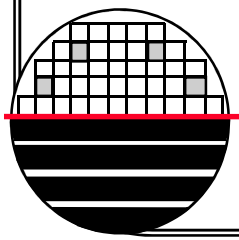
INVERTER, NAND2,3,4, NOR2,3,4, NULL

Basic Cells

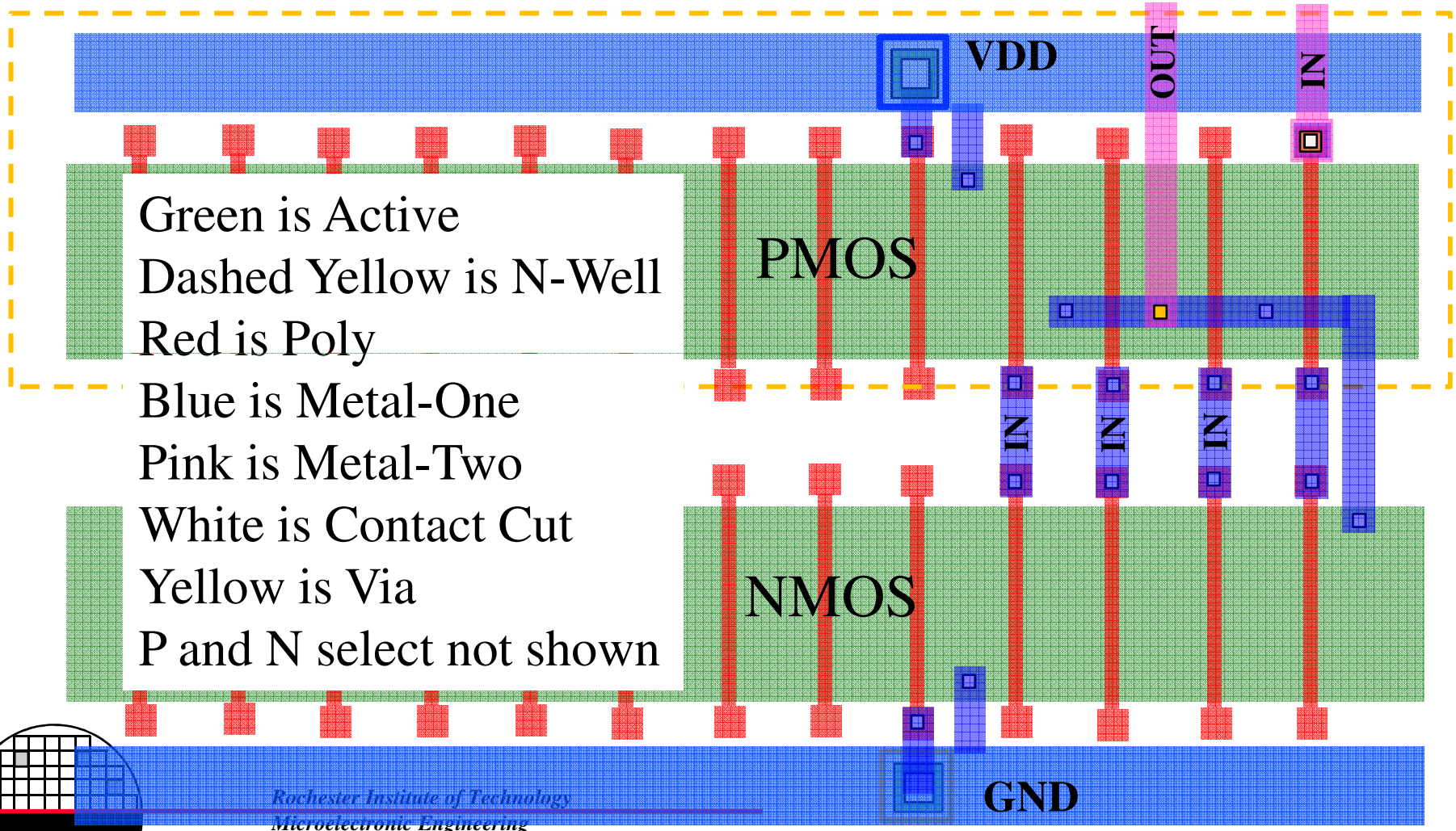
XOR, MUX, DEMUX, ENCODER, DECODER
FULL ADDER, FLIP FLOPS

Macro Cells

BINARY COUNTER
SRAM

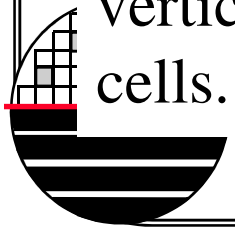


LAYOUT – GATE ARRAY

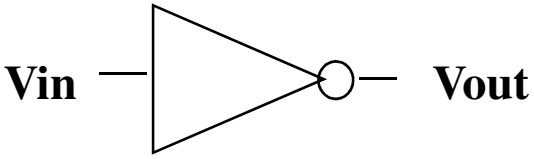


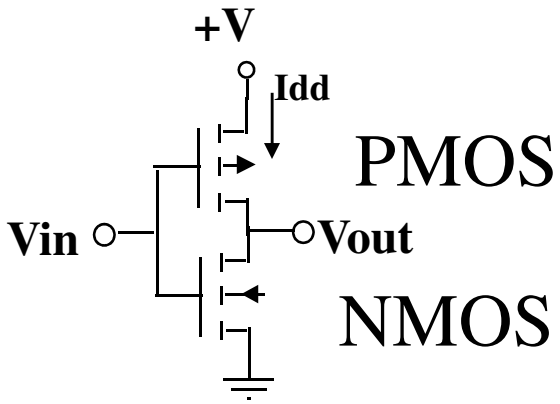
LAYOUT DETAILS FOR GATE ARRAY

1. Cells are separated from adjacent cells by off transistors
2. Well contacts are made at each of the off transistors
3. Metal-two connects thru Via to Metal-one
4. Metal-one connects thru Contact Cuts to active and Poly
5. Inputs and Outputs connections are made vertically with Metal-two
6. Routing channels exist above and below the gate array and contain horizontal metal-one interconnects between cells, with Via to Metal-two.
7. The NULL cell at the end of the gate array row satisfy design rules for extension of well beyond active, etc. It also provides a vertical routing channel which may be useful in constructing macro cells.



INVERTER

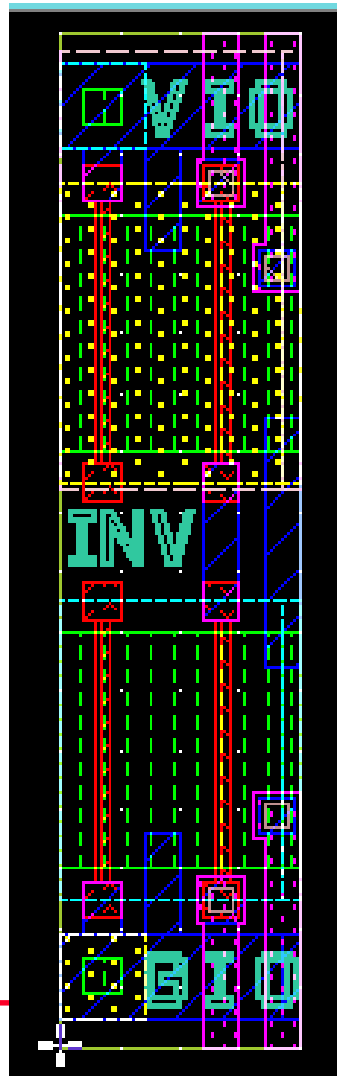


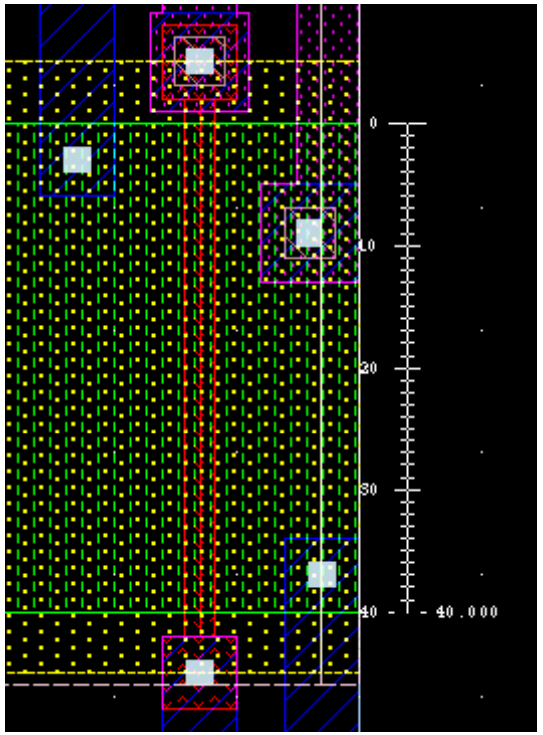


CMOS

TRUTH TABLE

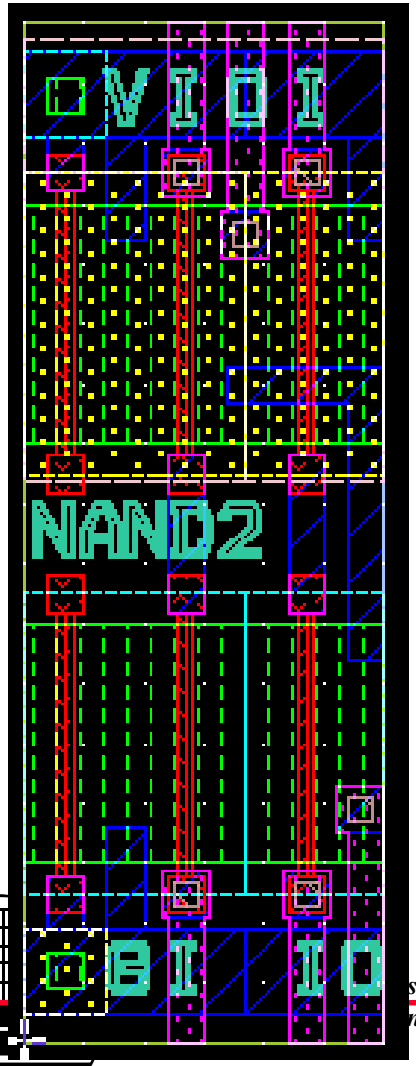
VIN	VOUT
0	1
1	0

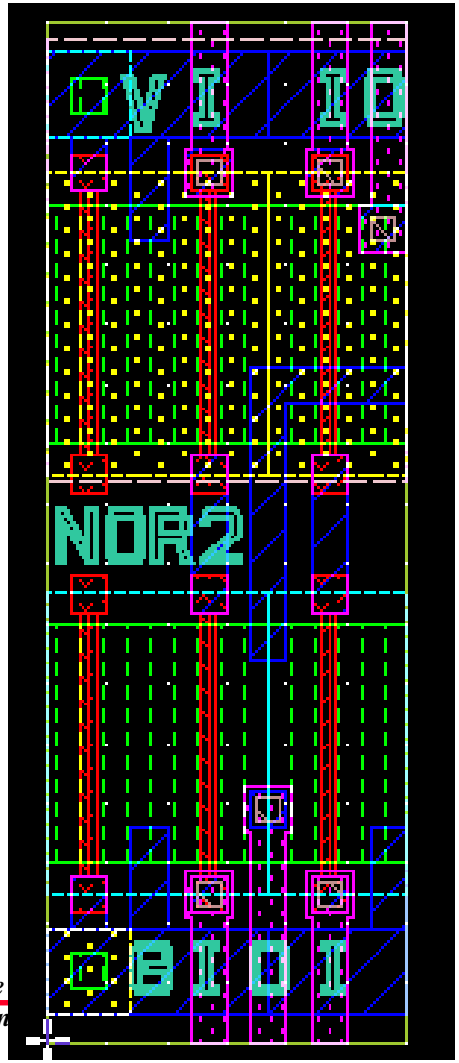


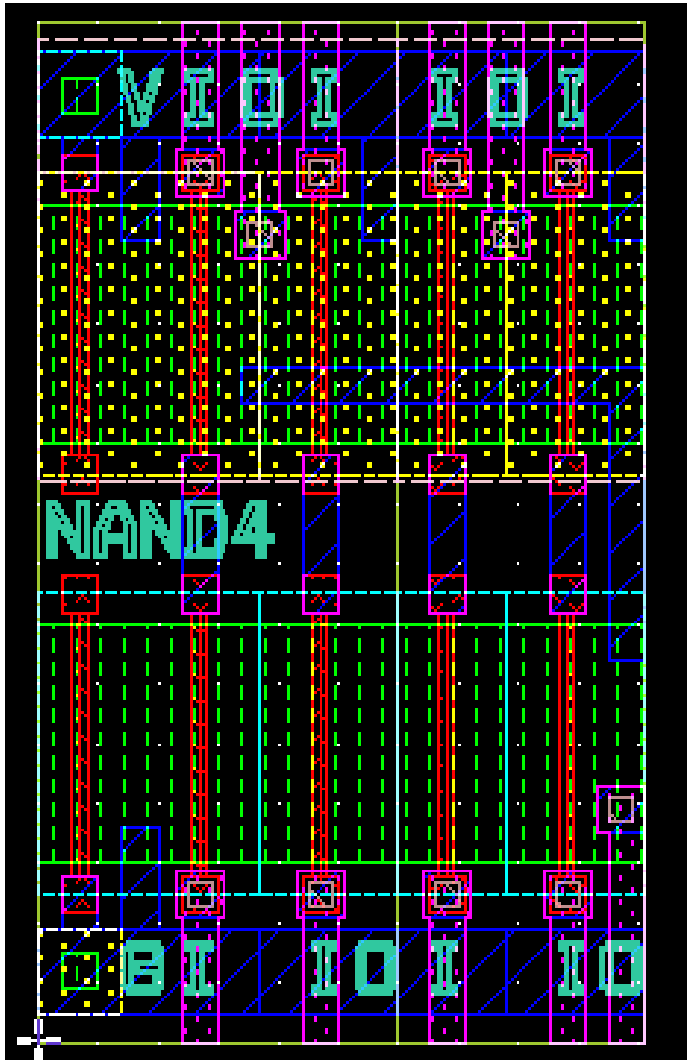


W = 40 µm
Ldrawn = 2.5µm
Lpoly = 1.0µm
Leff = 0.35 µm

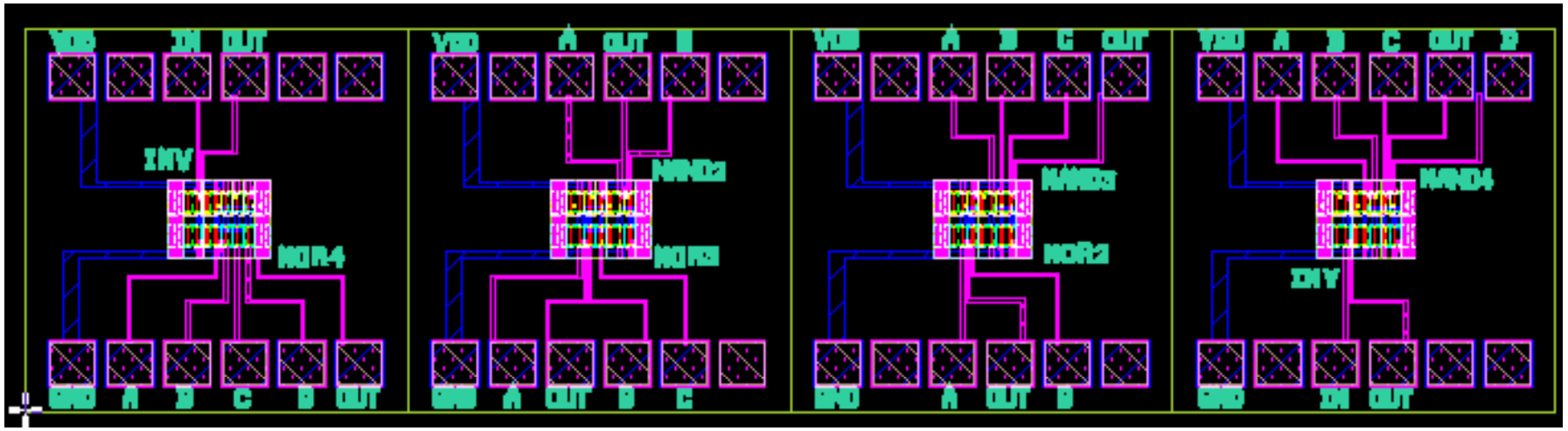
PRIMITIVE CELLS





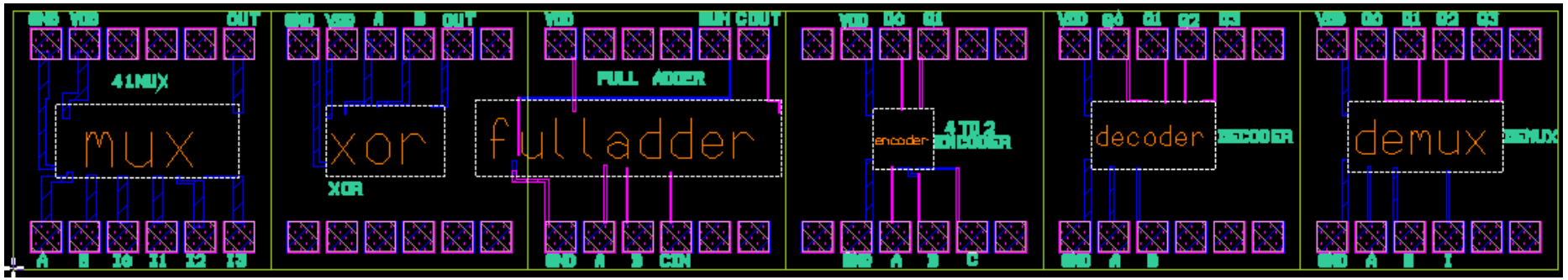


PRIMITIVE CELLS WITH PADS

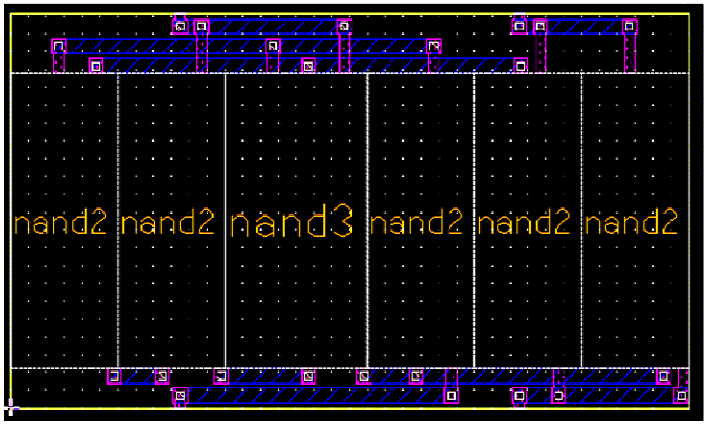


INV/NOR4 NOR3/NAND2 NOR2/NAND3 INV/NAND4

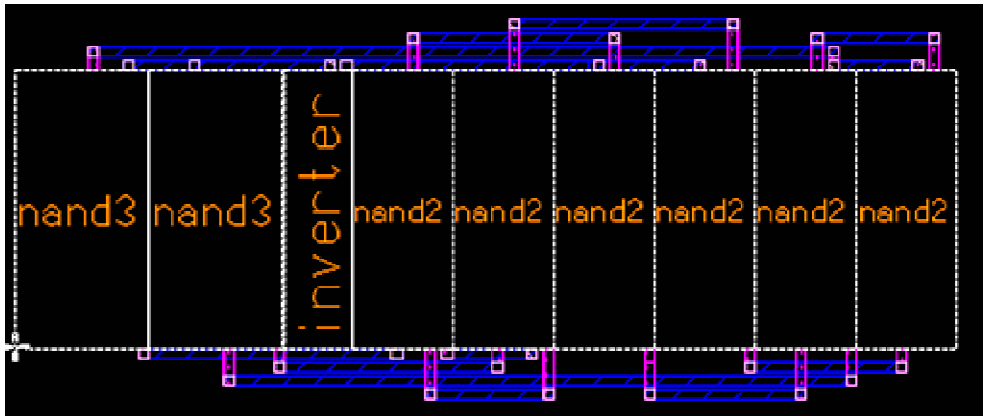
BASIC DIGITAL CELLS WITH PADS



Multiplexer XOR Full Adder Encoder Decoder Demux

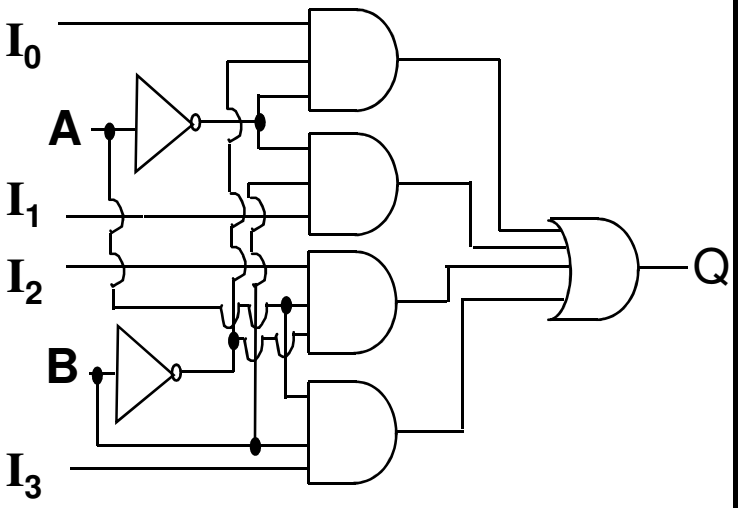


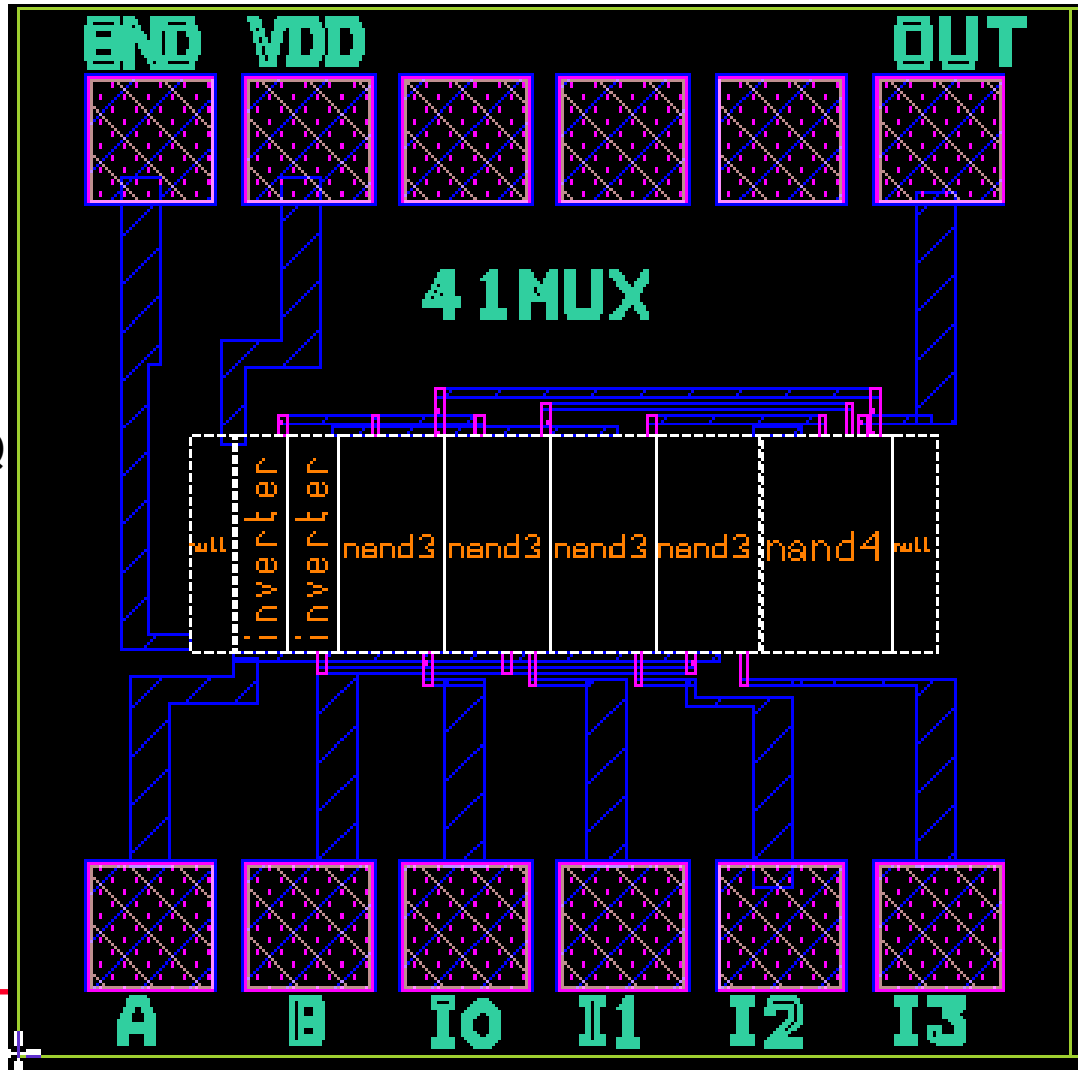
Edge Triggered D FF



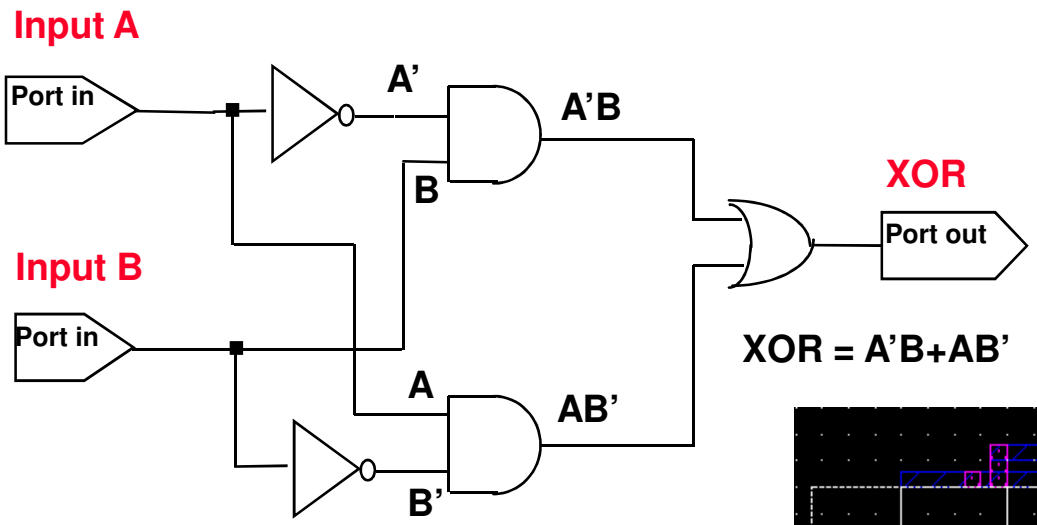
JK FF

4 TO 1 MULTIPLEXER



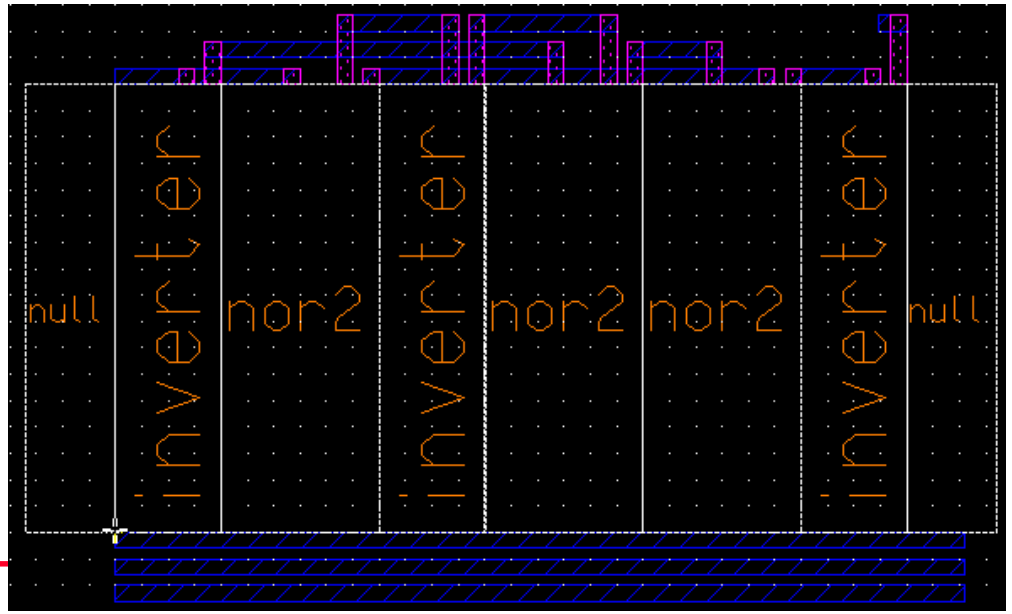


BASIC CELL XOR

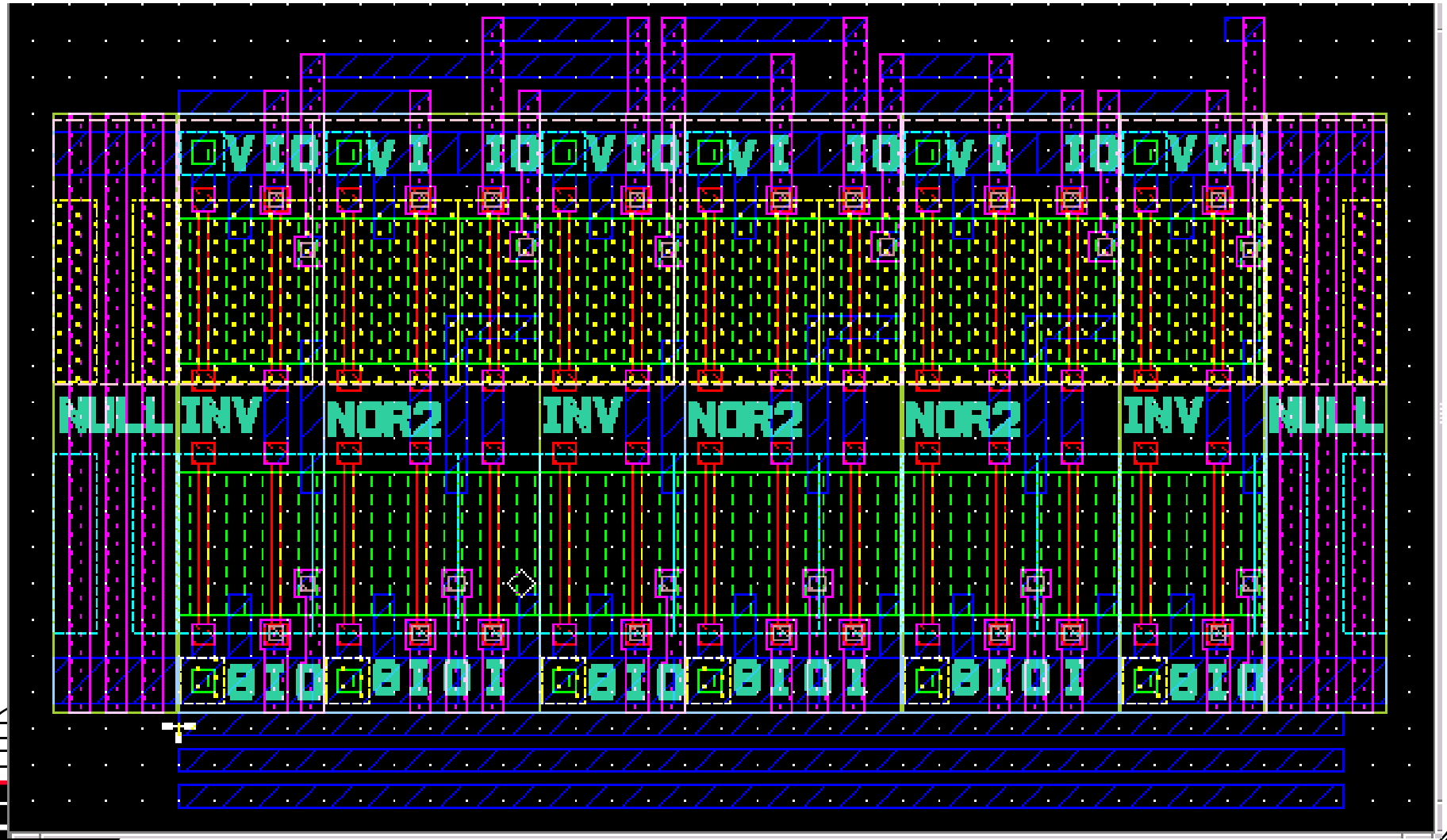


XOR = A'B+AB'

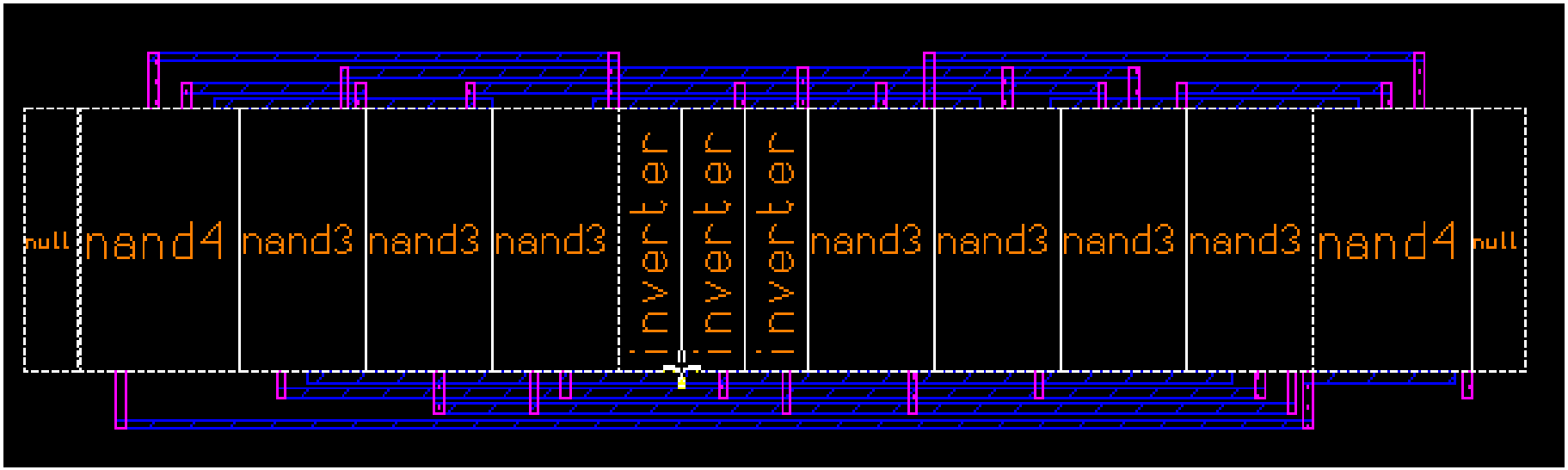
XOR

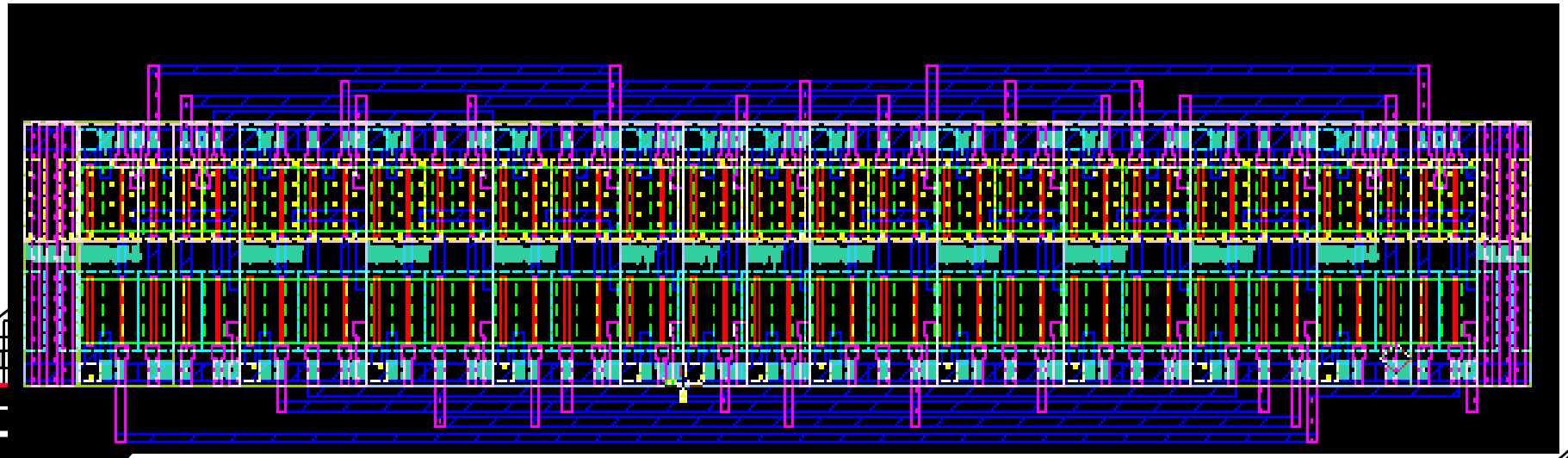


XOR

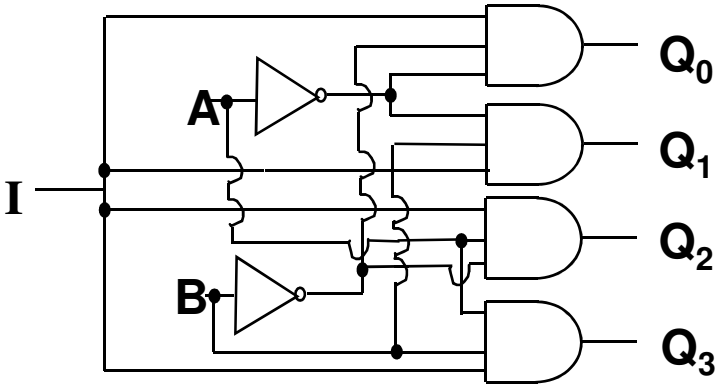

VIO
VIO
VIO
VIO
VIO
NULL
INV
NOR2
INV
NOR2
NOR2
INV
NULL
BIO
BIO
BIO
BIO
BIO

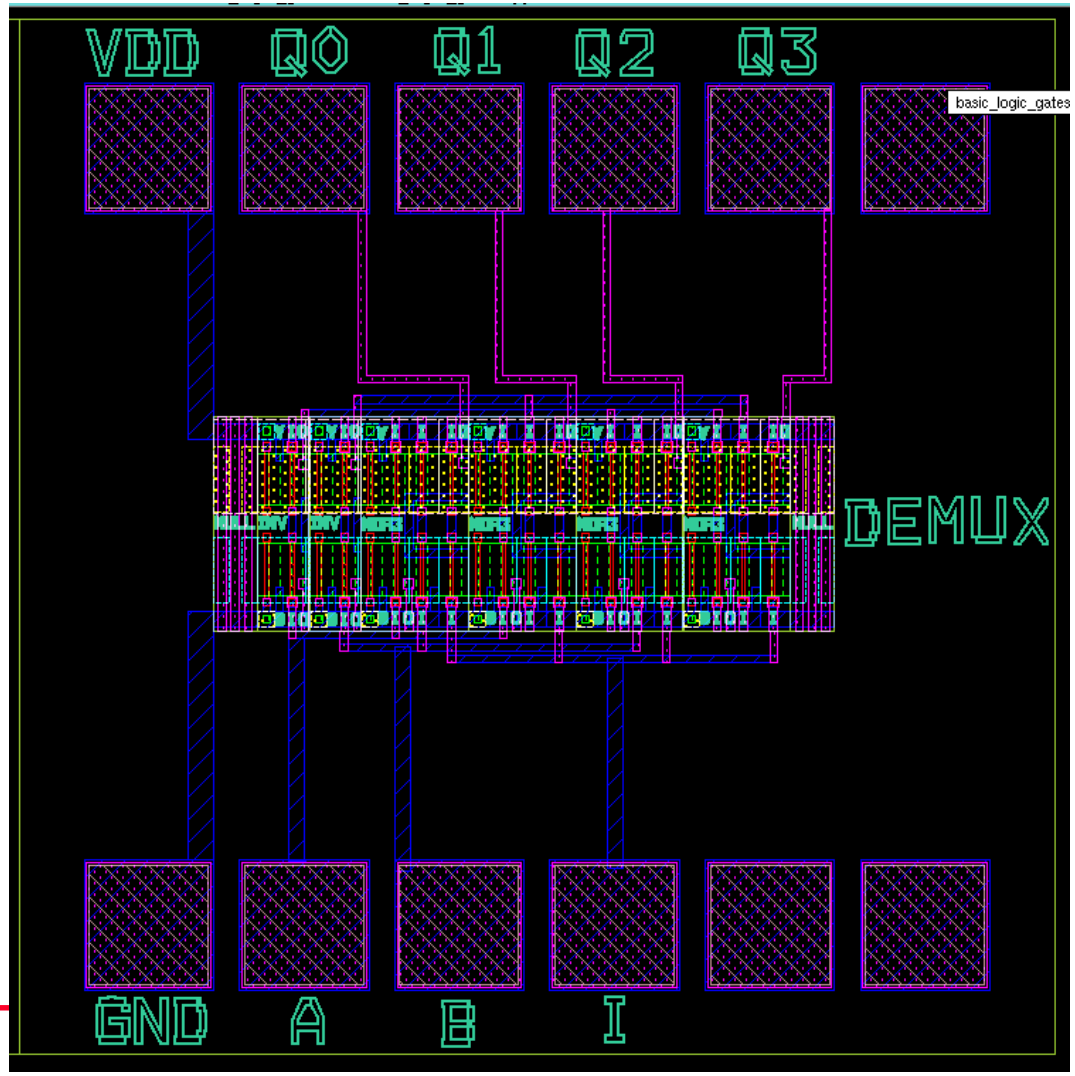
FULL ADDER

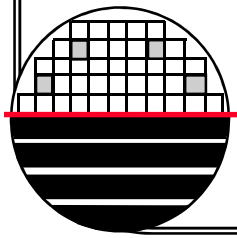

null
nand4
nand3
nand3
nand3
inverter
inverter
inverter
nand3
nand3
nand3
nand3
nand4
null



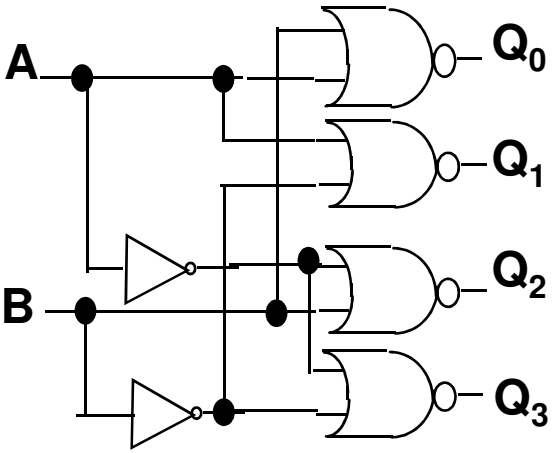
1 TO 4 DEMULTIPLEXER

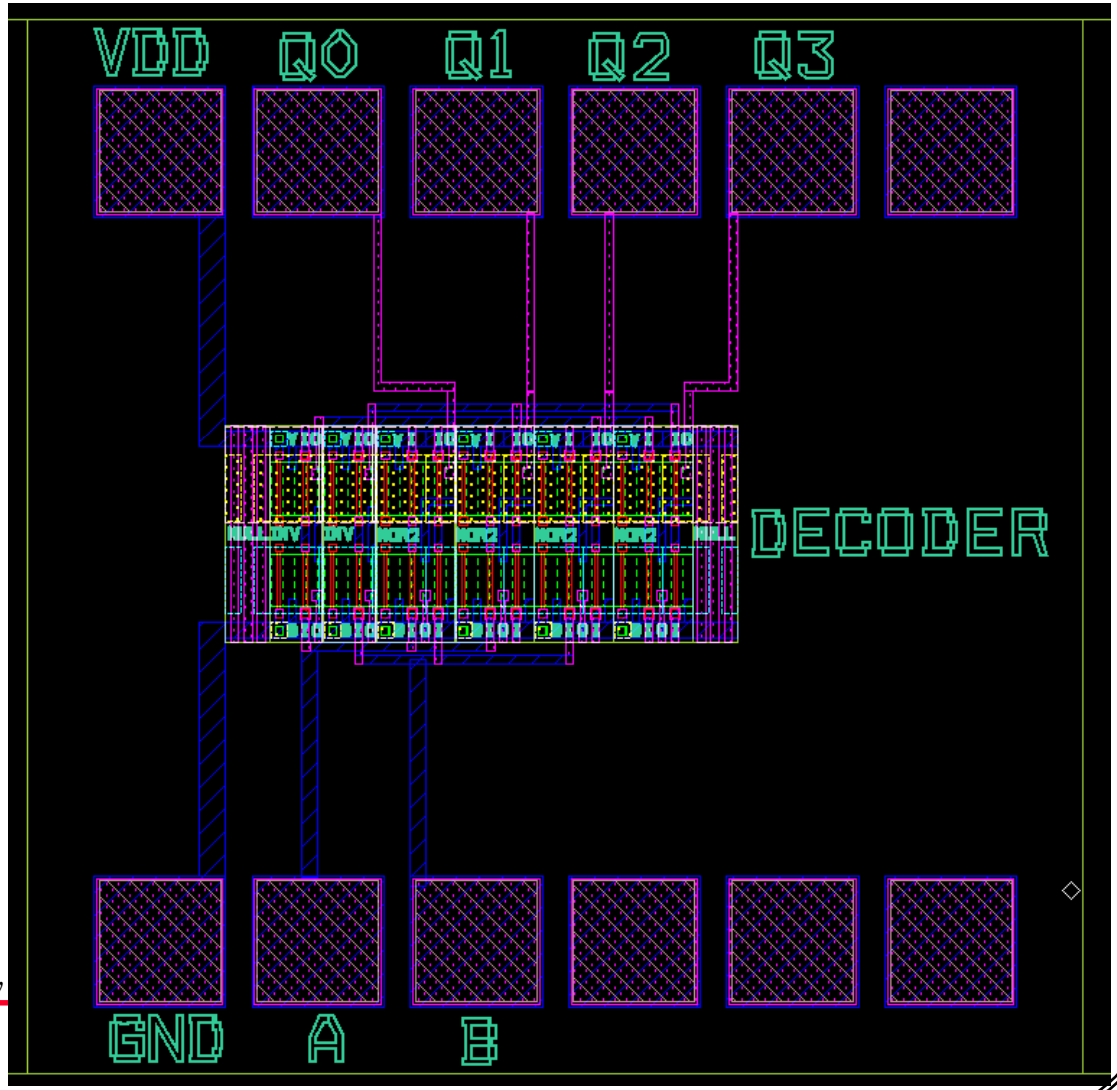


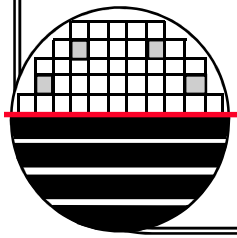




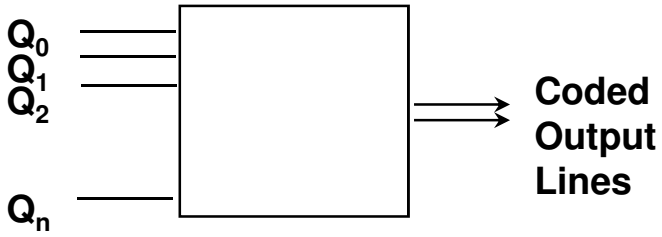
DECODER







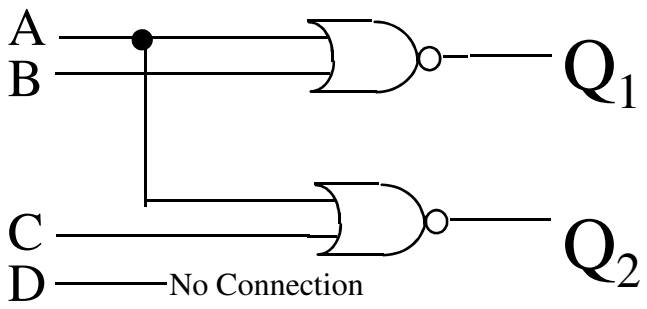
ENCODER

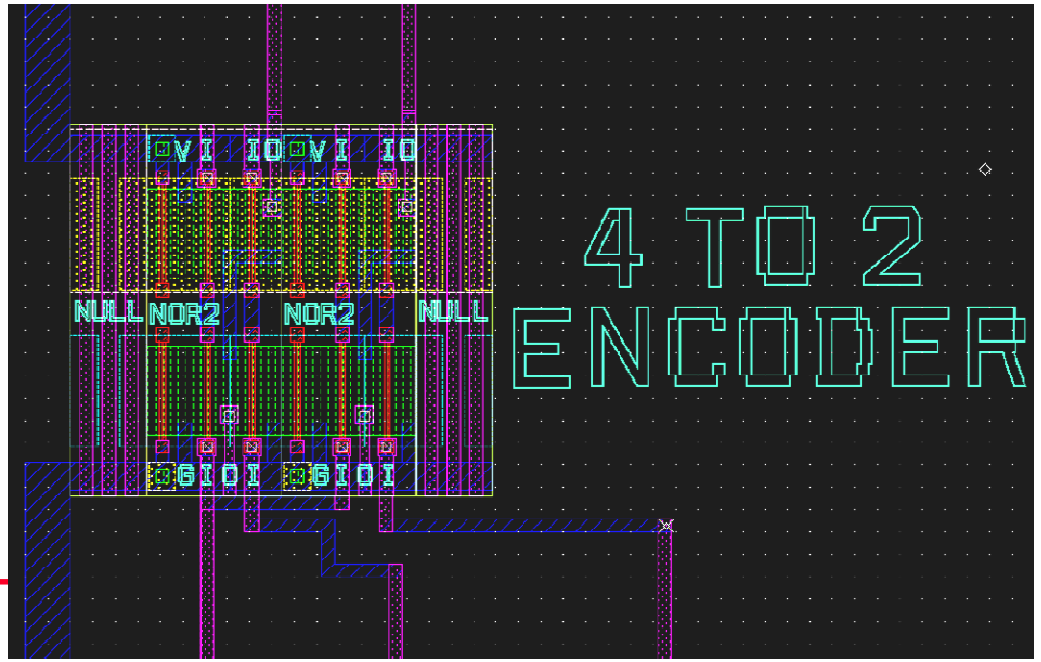


Digital Encoder

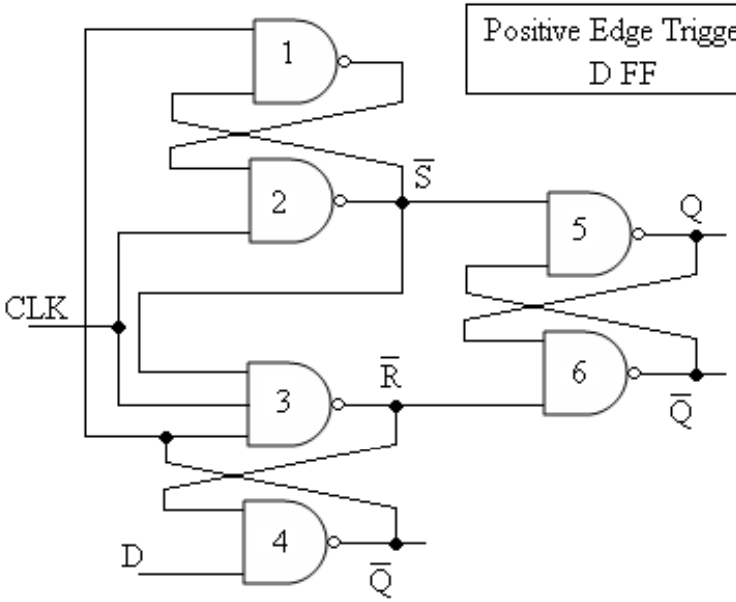
512 inputs can be coded into 9 lines which is a more dramatic benefit

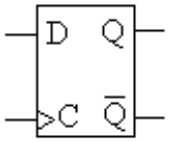
A	B	C	D	Q0	Q1
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1



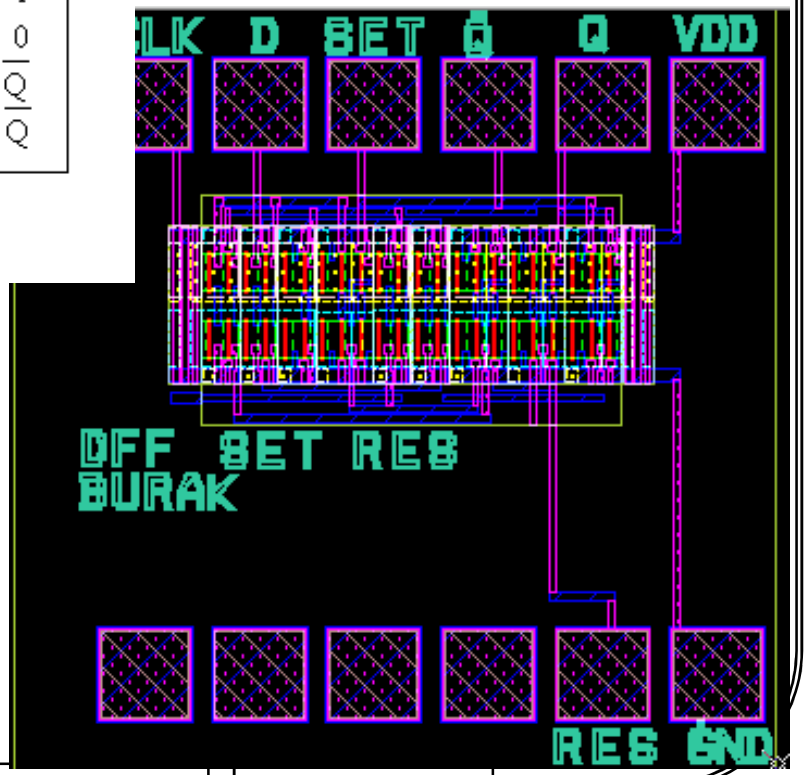


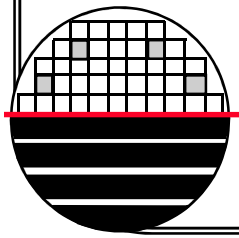
EDGE TRIGGERED D TYPE FLIP FLOP



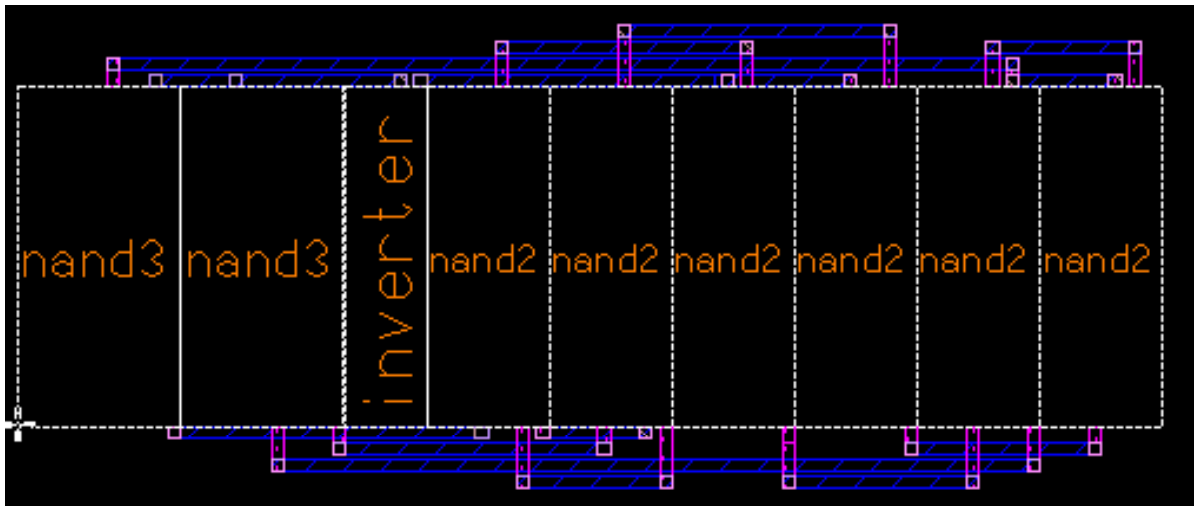


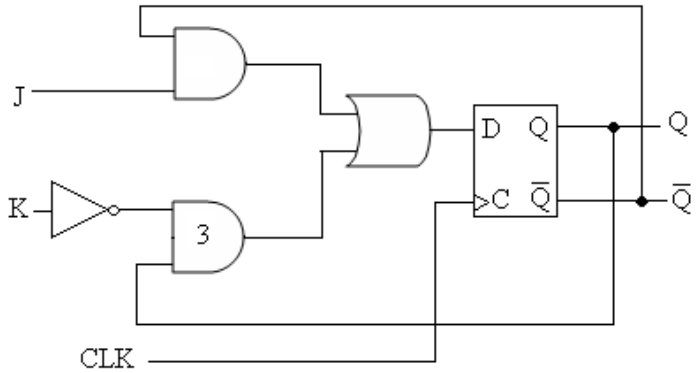
Inputs		Outputs	
D	C	Q^+	$\overline{Q^+}$
0	↑	0	1
1	↑	1	0
X	0	Q	$\overline{Q}$
X	1	Q	$\overline{Q}$



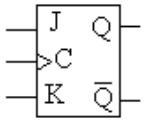


JK FLIP FLOP





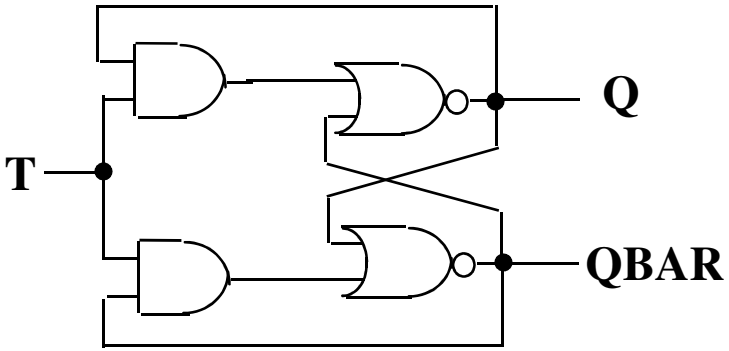
Positive Edge Triggered JK FF

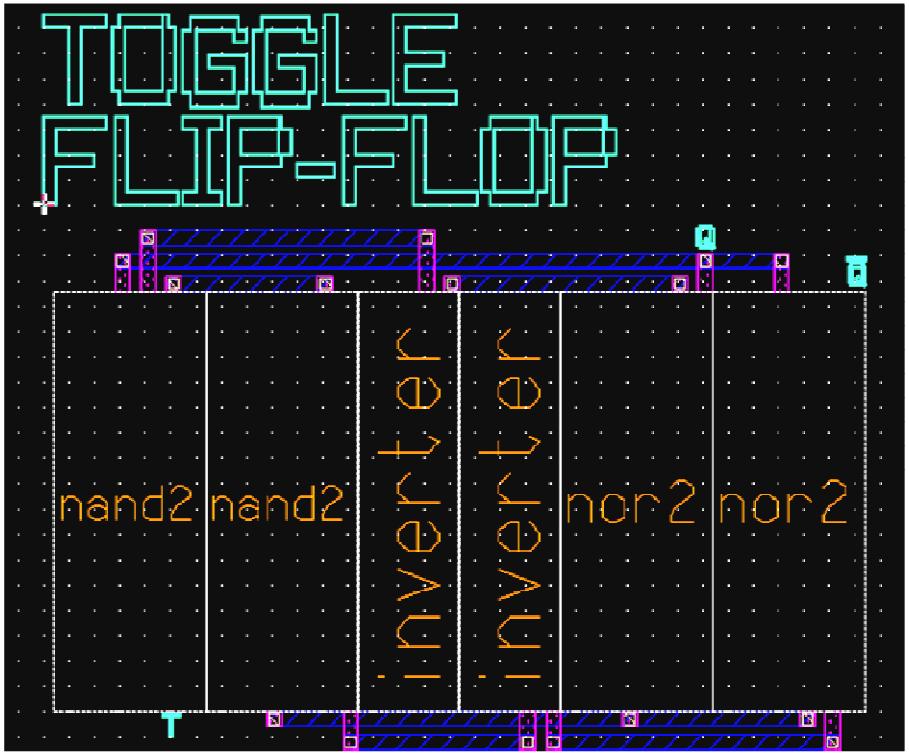


Inputs			Outputs	
J	K	C	Q^+	$\overline{Q^+}$
0	0	↑	Q	$\overline{Q}$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\overline{Q}$	Q
X	X	0	Q	$\overline{Q}$
X	X	1	Q	Q

T-TYPE FILP-FLOP

TOGGEL FLIP FLOP

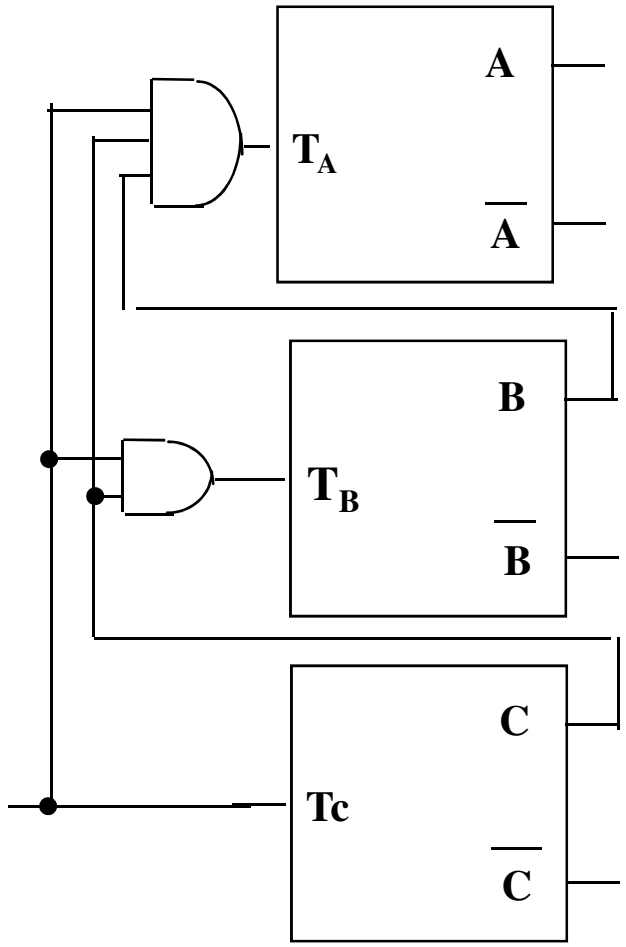




Q: Toggles High and Low with Each Input

T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

BINARY COUNTER USING T TYPE FLIP FLOPS



State Table for Binary Counter

Present State			Next State			F-F Inputs		
A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

TOGGEL FLIP FLOP

BC \ A	0	1
00	0	0
01	0	0
11	1	1
10	0	0

T_A

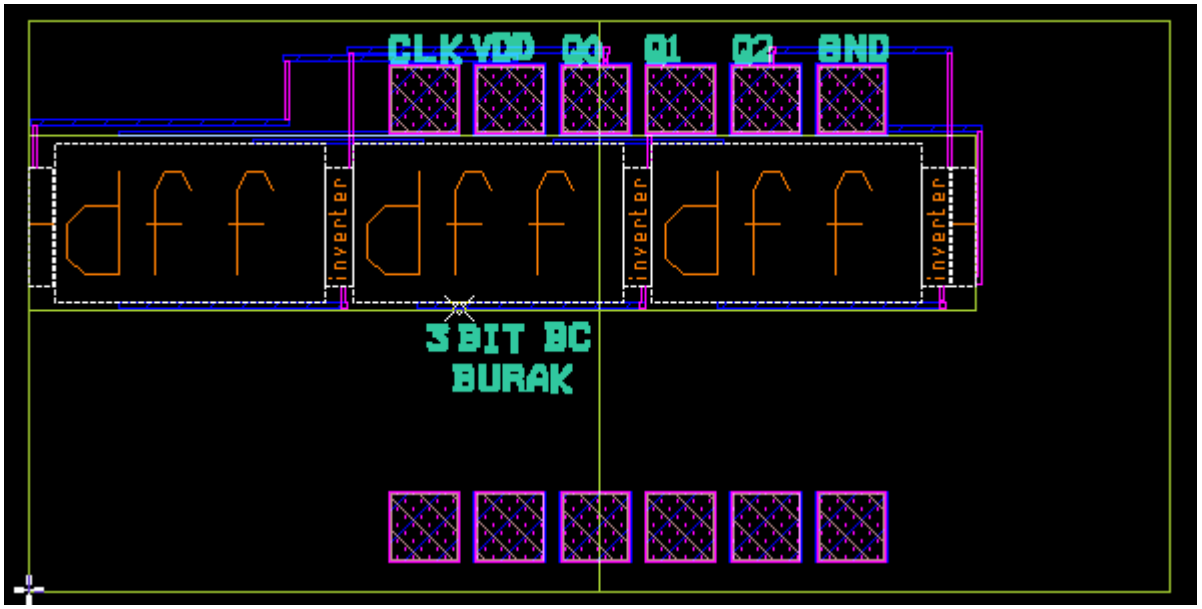
BC \ A	0	1
00	0	0
01	1	1
11	1	1
10	0	0

T_B

BC \ A	0	1
00	1	1
01	1	1
11	1	1
10	1	1

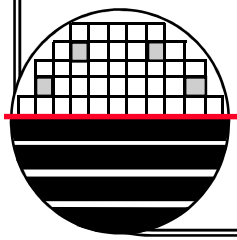
T_C

3-BIT BINARY COUNTER WITH D FLIP FLOPS

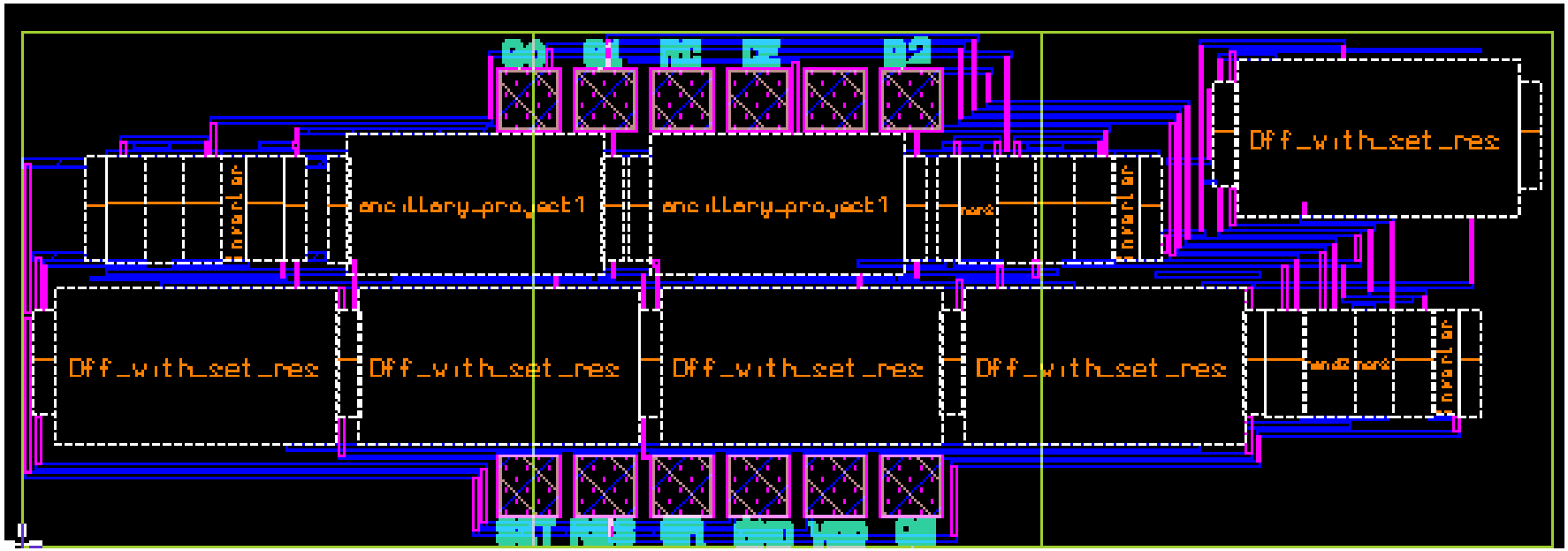


MACROCELLS

Binary Counter
SRAM

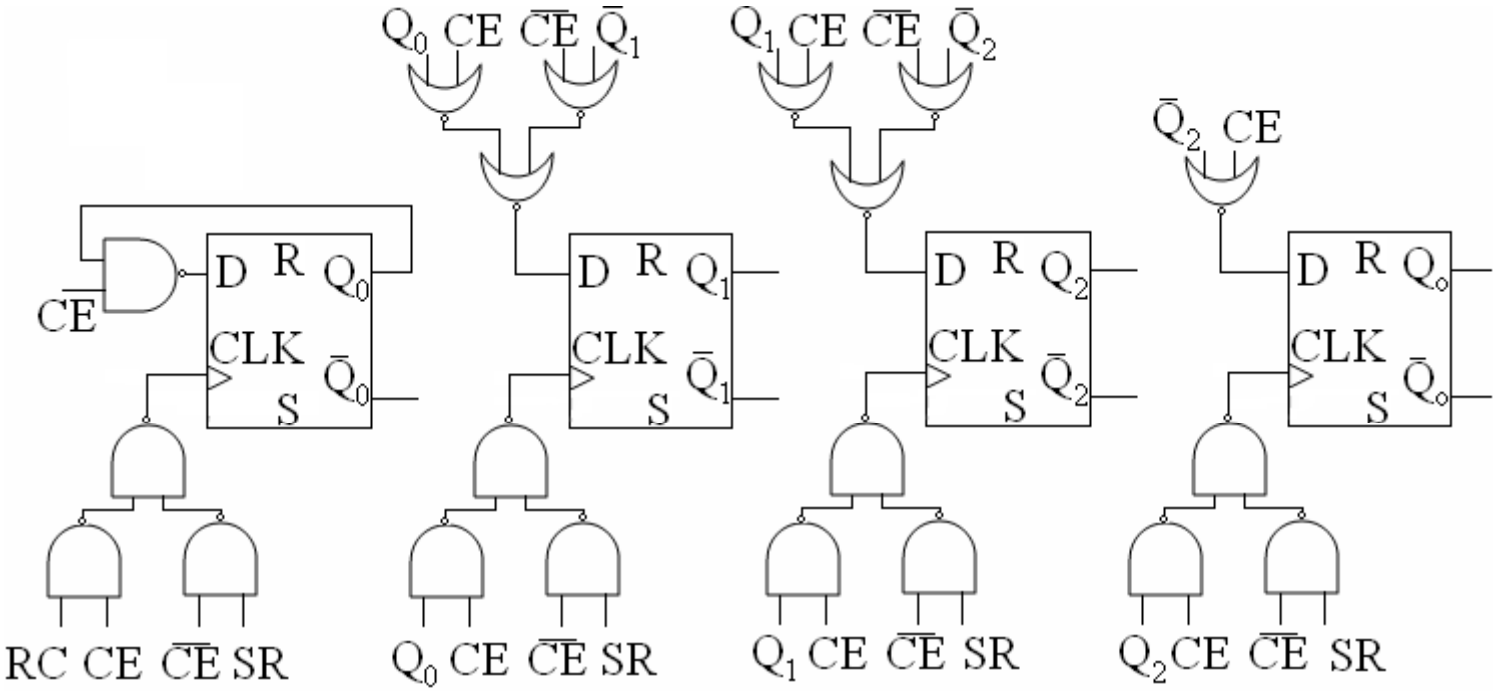


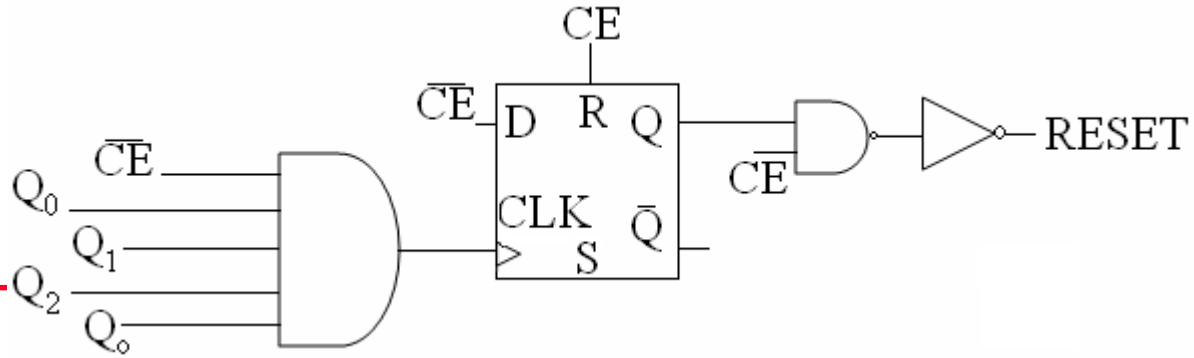
3-BIT BINARY COUNTER/SHIFT REGISTER



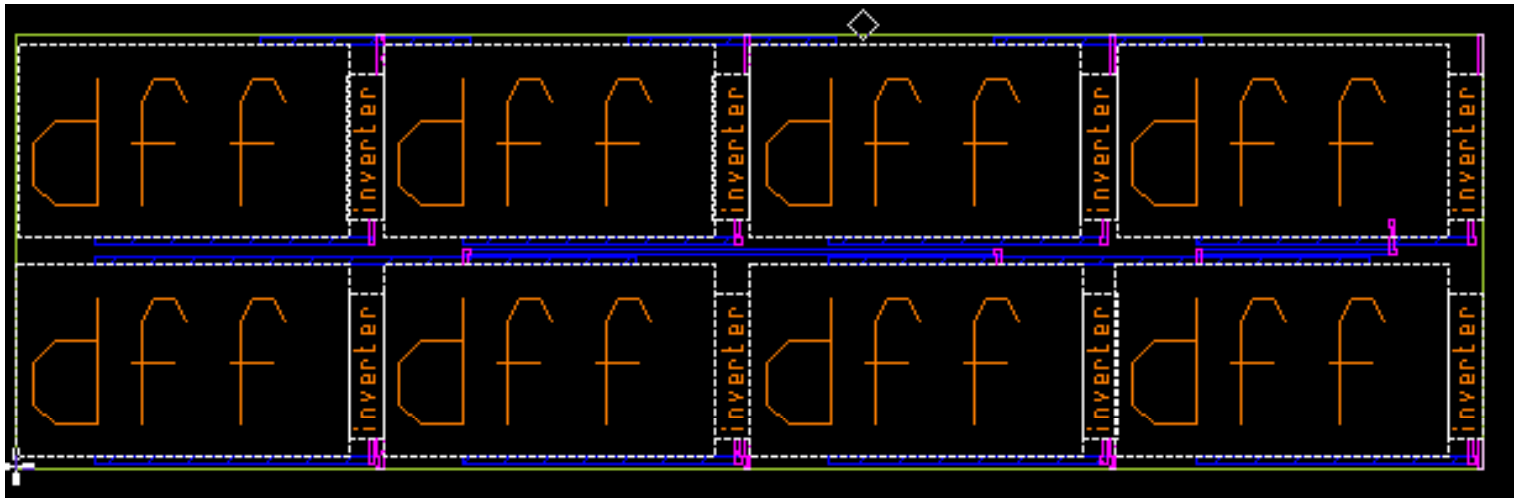
Binary Counter
Serial Output
Asynchronous Reset
Count Up Enable
Shift Out Clock Input
Count Up Clock Input
Start Bit and Stop Bit

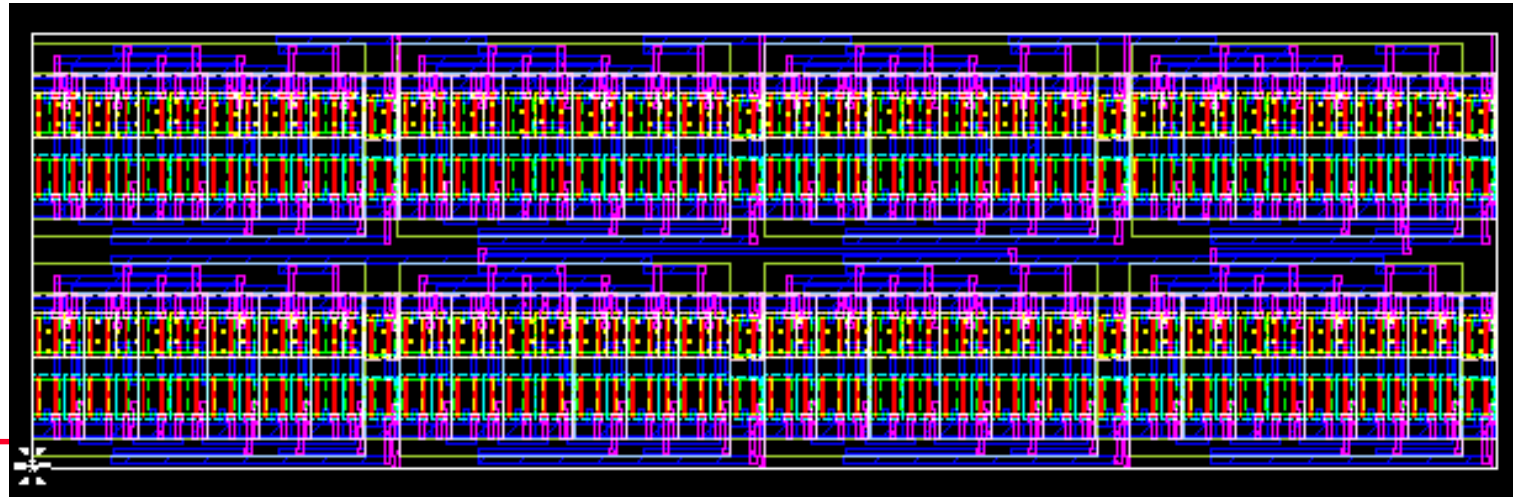
ADDITIONAL CIRCUITRY TO RESET, SHIFT, COUNT



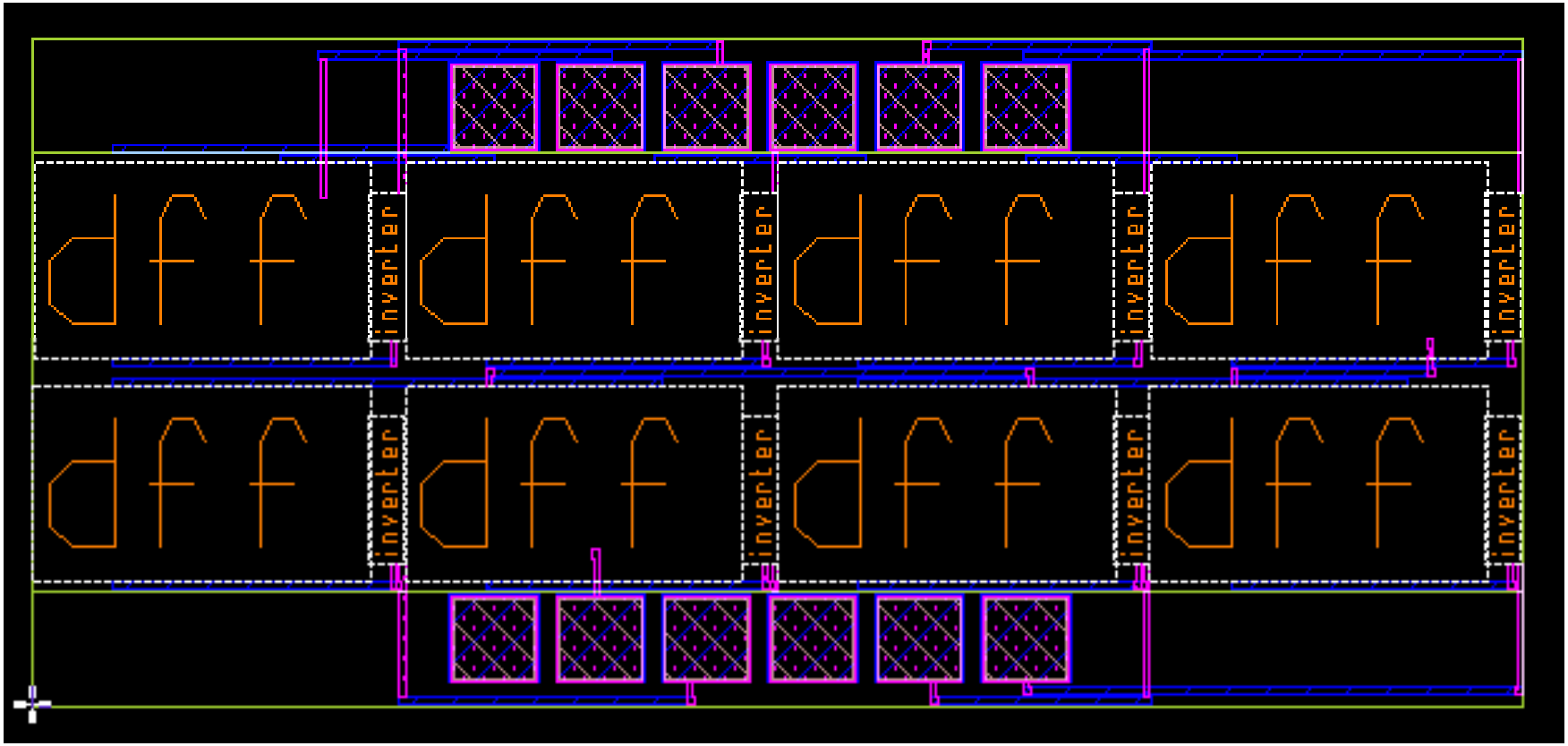


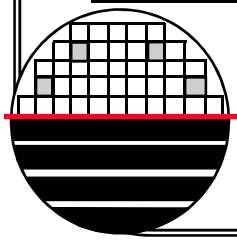
8-BIT BINARY COUNTER



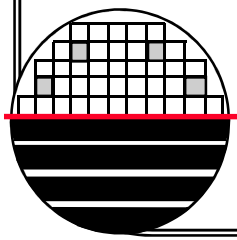


8-BIT BINARY COUNTER WITH PADS





Maskmaking

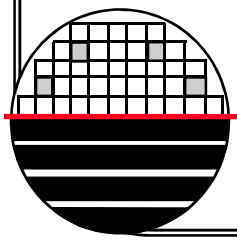


FILE FORMATS

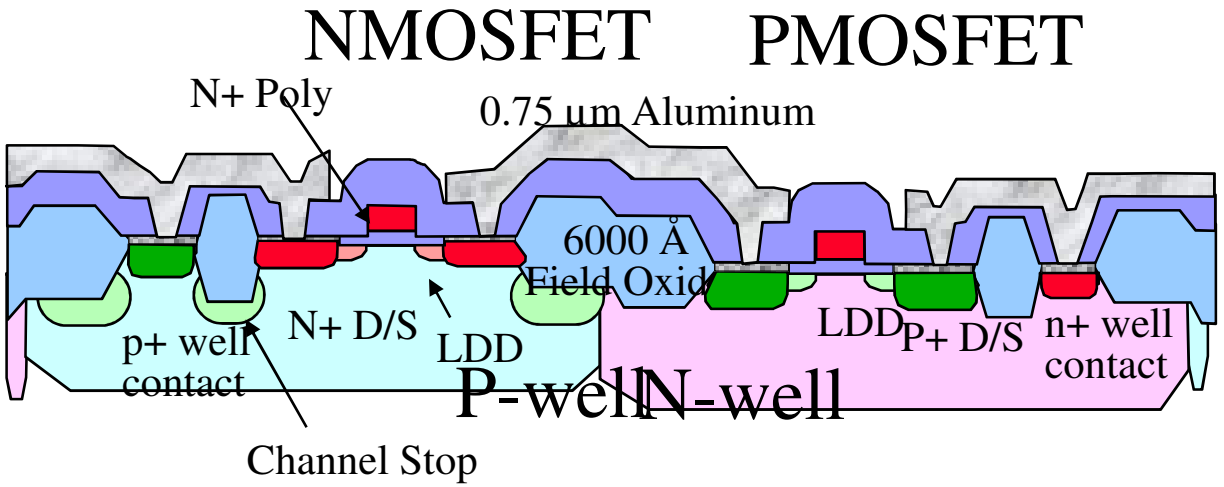
Mentor- ICGraph files (filename.iccel), all layers, polygons with up to 200 vertices

GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

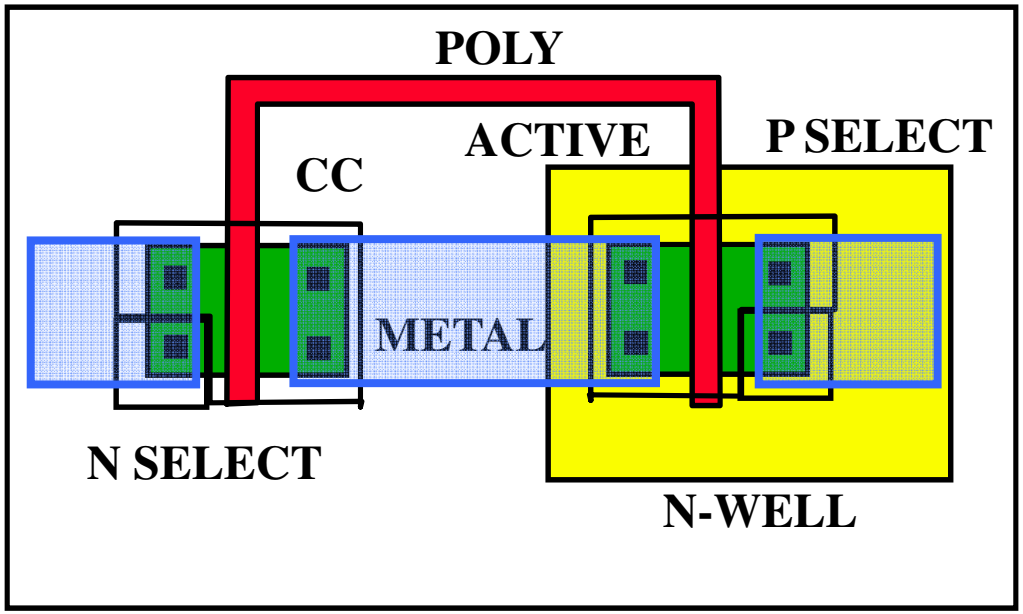
MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only

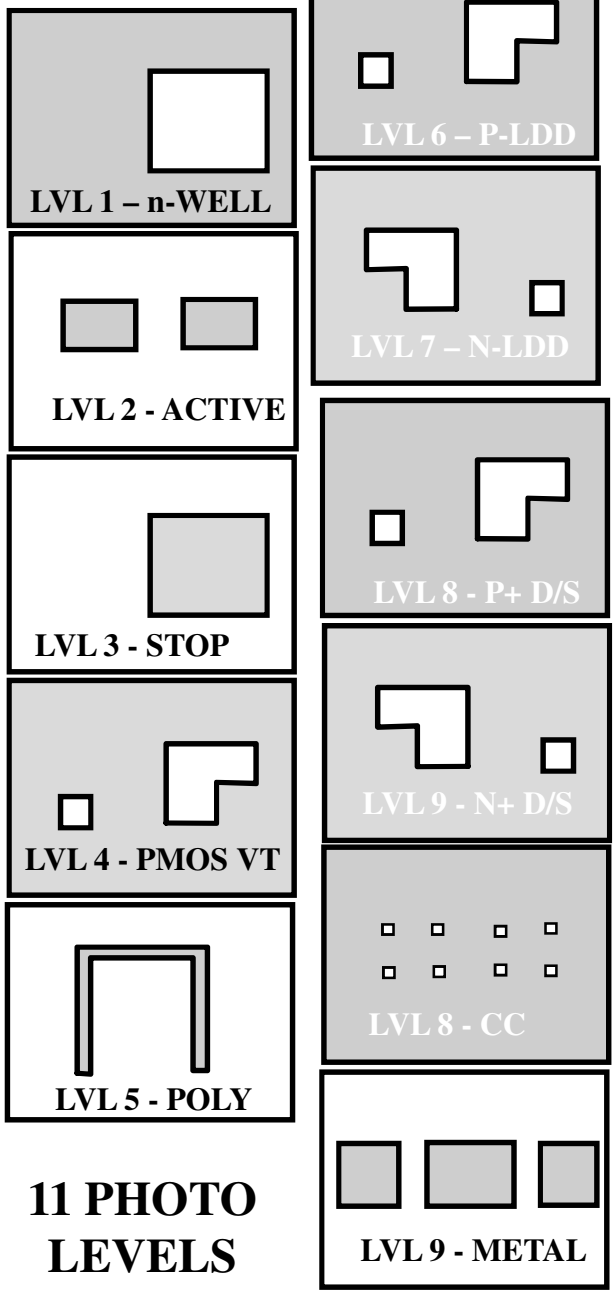


RIT SUB-CMOS PROCESS



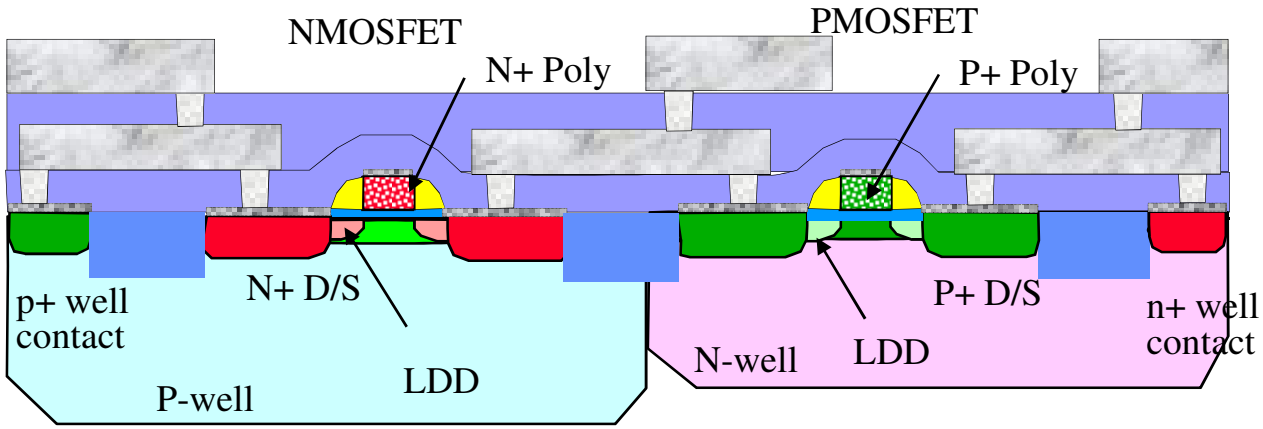
N-type Substrate 10 ohm-cm



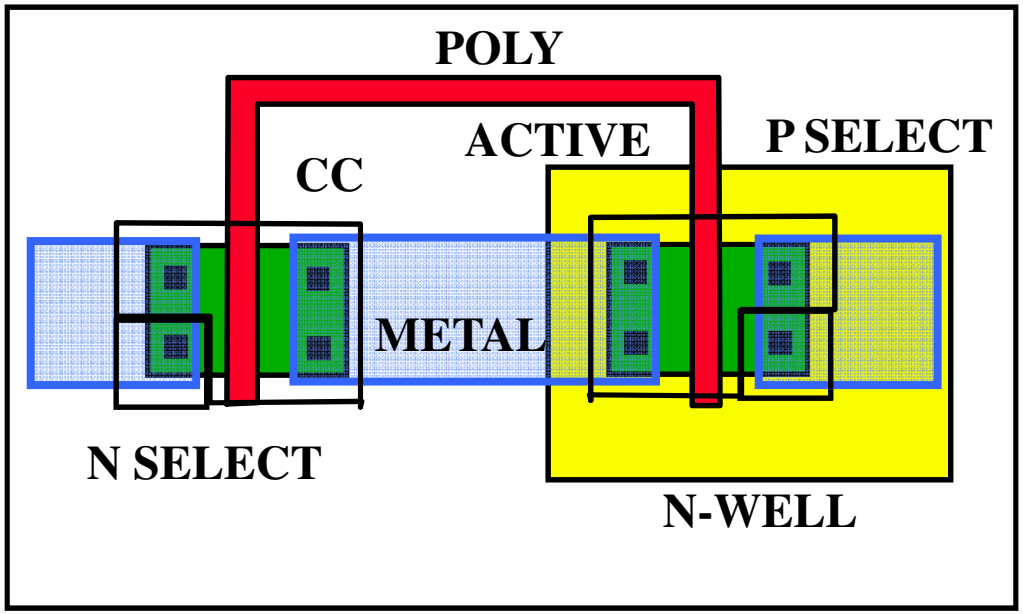


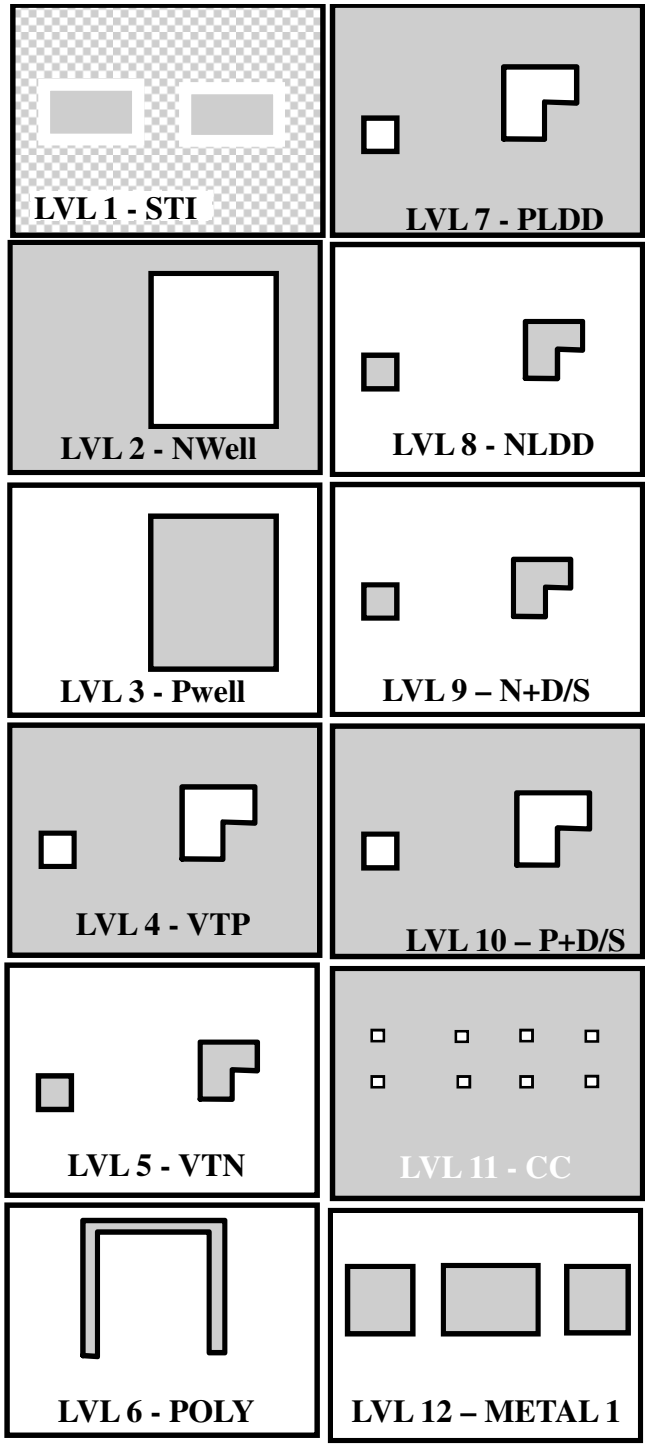
11 PHOTO LEVELS

RIT ADVANCED CMOS



12 PHOTO LEVELS + 2 FOR EACH ADDITIONAL METAL LAYER





OTHER MASKMAKING FEATURES

Fiducial Marks-marks on the edge of the mask used to align the mask to the stepper

Barcodes

Titles

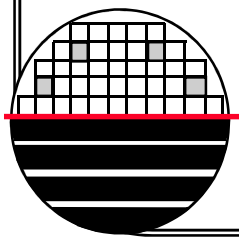
Alignment Keys- marks on the wafer from a previous level used for wafer alignment

CD Resolution Targets- lines and spaces

Overlay Verniers- structures that allow measurement of x and y overlay accuracy

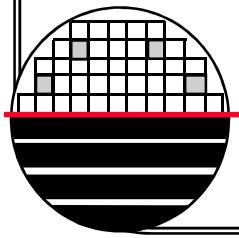
Tiling

Optical Proximity Correction (OPC)



REFERENCES

1. Silicon Processing for the VLSI Era, Volume 1 – Process Technology, 2nd, S. Wolf and R.N. Tauber, Lattice Press.
2. The Science and Engineering of Microelectronic Fabrication, Stephen A. Campbell, Oxford University Press, 1996.
3. MOSIS Scalable CMOS Design Rules for Generic CMOS Processes, www.mosis.org, and http://www.mosis.com/design/rules/



HOMEWORK – INTRO TO VLSI

1. Do a SPICE simulation to obtain the VTC for the inverter shown on page 16. Let the load resistor be 10K, the NMOS transistor SPICE model RITSUBN7, L=1u and W=40u. Extract Voh, Vol, Vil, ViH, Vinv, Noise Margin Low, Noise Margin High and Maximum current.
2. Do a SPICE simulation to obtain the VTC for the inverter shown on page 20. Let the NMOS and PMOS transistor SPICE model RITSUBN7 and RITSUBP7, L=1u and W=40u. Extract Voh, Vol, Vil, ViH, Vinv, Noise Margin Low, Noise Margin High and Maximum current.
3. Do a SPICE simulation to obtain the RISE TIME and FALL TIME for the inverter in problem 2 with a load capacitance equal to a fan out of 5 gates.
4. Show that the XOR realized with AND and OR gates is equivalent to an all NAND gate realization.