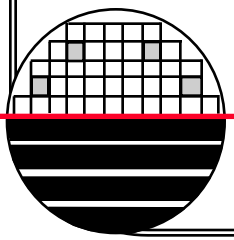
ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Introduction to LTSPICE

Dr. Lynn Fuller

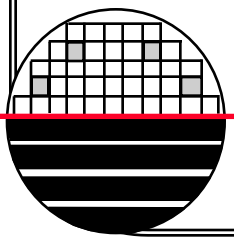
Electrical and Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041
Email: Lynn.Fuller@rit.edu
Dr. Fuller's Webpage: http://people.rit.edu/lffeee
MicroE Webpage: http://www.microe.rit.edu



© January 16, 2014 Dr. Lynn Fuller

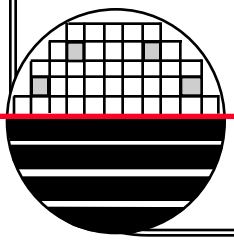
ADOBE PRESENTER

This PowerPoint module has been published using Adobe Presenter. Please click on the Notes tab in the left panel to read the instructors comments for each slide. Manually advance the slide by clicking on the play arrow or pressing the page down key.



OUTLINE

SPICE Introduction
LTSPICE
MOSFET Parameters and SPICE Models
ID-VDS Family of Curves
ID-VGS and GM-VGS Curves
Inverter DC Simulation
Ring Oscillator Transient Simulation
Conclusion
Helpful Hints
References
Homework

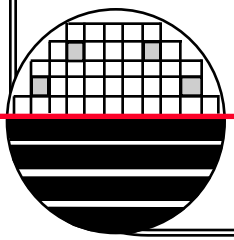


INTRODUCTION

SPICE (Simulation Program for Integrated Circuit Engineering) is a general-purpose circuit simulation program for non-linear DC, non-linear transient, and linear AC analysis. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, transmission lines, switches, and several semiconductor devices: including diodes, BJTs, JFETs, MESFETs, and MOSFETs. Circuits with large numbers of all types of components can be simulated. You can think of SPICE as a nodal network solver that outputs all the node voltages and branch currents. One node must be named "0" (the ground node) and is the reference node for all the node voltages.

SPICE input files and output files are simple text files (e.g. name.txt)

Input files include a TITLE, circuit description NET LIST, analysis directives (COMMANDS), and lists of other text files to include (INC) such as model libraries (LIB) and an .END command.

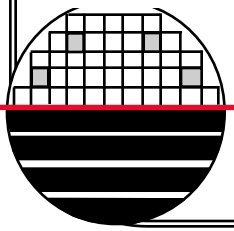


INTRODUCTION

LT SPICE – is a free SPICE simulator with schematic capture from Linear Technology. It is quite similar to PSPICE Lite but is not limited in the number of devices or nodes. Linear Technology (LT) is one of the industry leaders in analog and digital integrated circuits. Linear Technology provides a complete set of SPICE models for LT components. (This is a good choice for your home computer.)

The input file for SPICE is generated automatically from the schematic capture software. In the old days the input file was created by hand as a simple text file. SPICE can still run using a simple text file as the input but today most users prefer to use schematic capture software to create the input file.

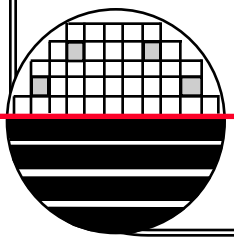
These files are read line by line. If the line starts with "*" it is a comment and what follows on that line is ignored. SPICE directives start with a "." such as .END or .INCLUDE pathneame\folder\filename.txt or .MODEL modelname NMOS (Level=7 etc etc etc.....) Upper and Lower case are treated the same (not case sensitive) thus m stands for milli, and MEG stands for mega.



MOSFET DEVICE MODELS

MOSFET Device models used by SPICE (Simulation Program for Integrated Circuit Engineering) simulators can be divided into three classes: First Generation Models (Level 1, Level 2, Level 3 Models), Second Generation Models (BISM, HSPICE Level 28, BSIM2) and Third Generation Models (BSIM3, Level 7, Level 8, Level 49, etc.) The newer generations can do a better job with short channel effects, local stress, transistors operating in the sub-threshold region, gate leakage (tunneling), noise calculations, temperature variations and the equations used are better with respect to convergence during circuit simulation.

In general first generation models are recommended for MOSFETs with gate lengths of 10um or more. If not specified most SPICE MOSFET Models default to level=1 (Shichman and Hodges)



MOSFET SPICE MODEL LEVELS

LEVEL=1 Shichman-Hodges Model
LEVEL=2 geometry-based analytic model
LEVEL=3 semi-empirical, short-channel model

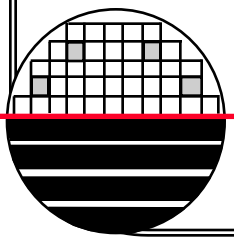
} 1st Generation

LEVEL=4 BSIM
LEVEL=28 BSIM ver 2v6

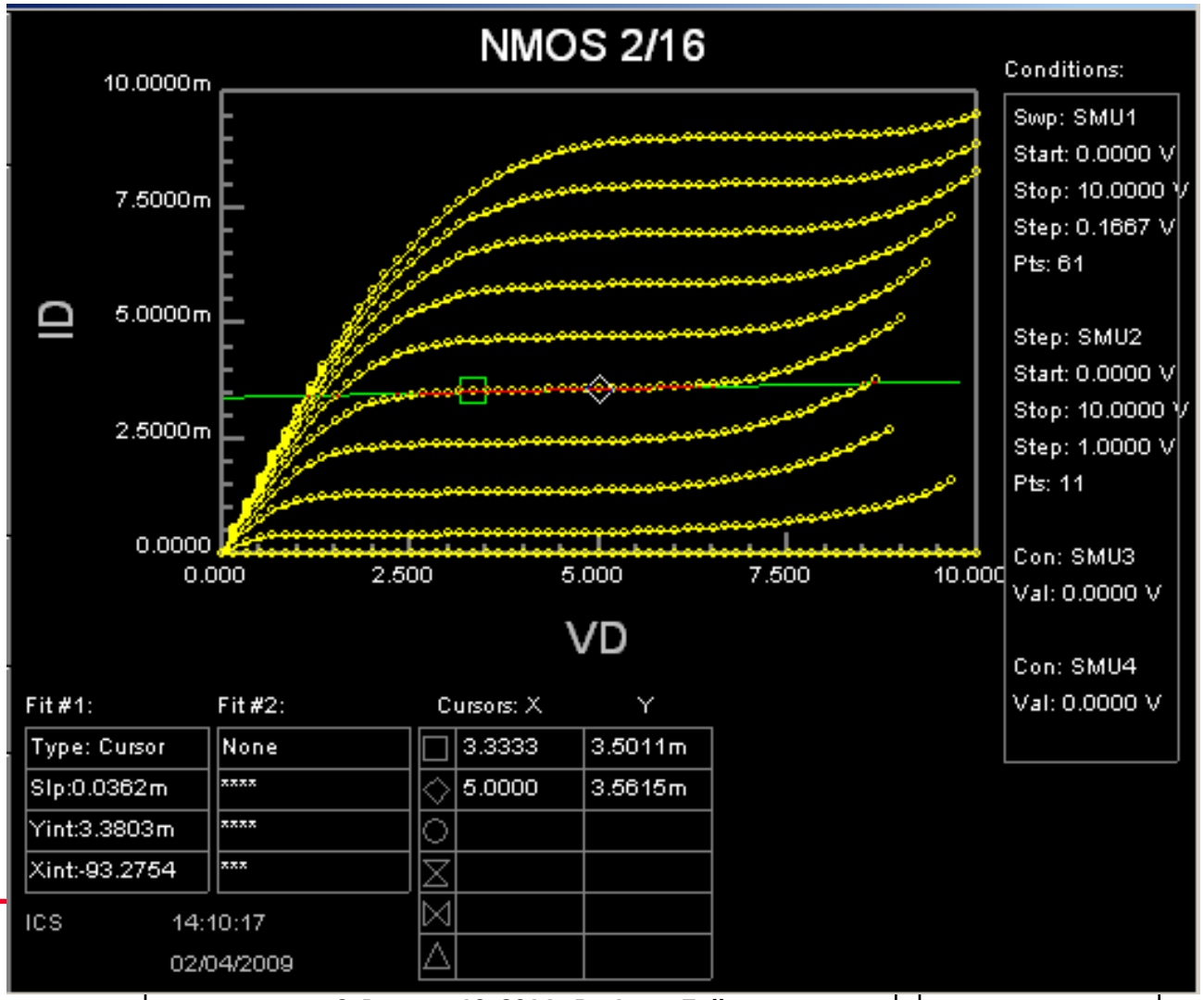
} 2nd Generation

LEVEL=7 or 8 BSIM3v1 from UC Berkeley
LEVEL=49 from Hspice is an enhanced UC Berkeley
LEVEL=53 from Hspice is full compliance Berkeley

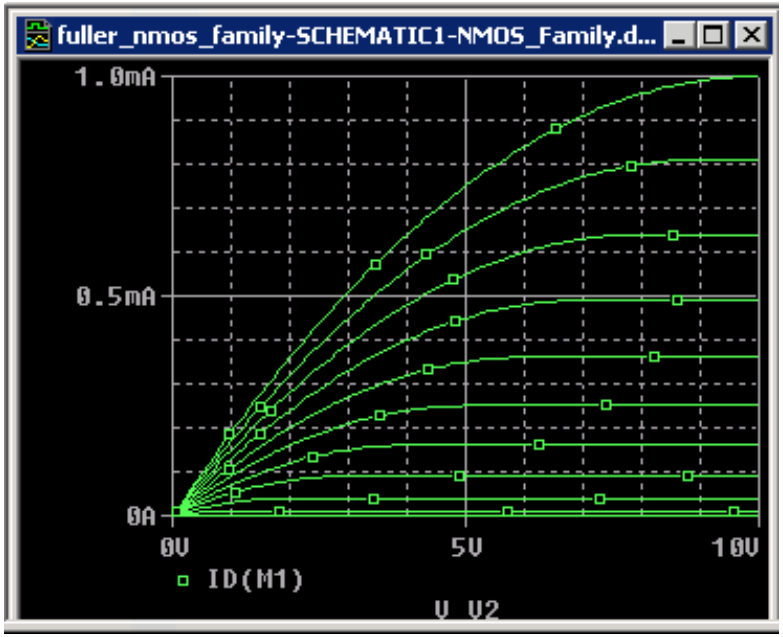
} 3rd Generation



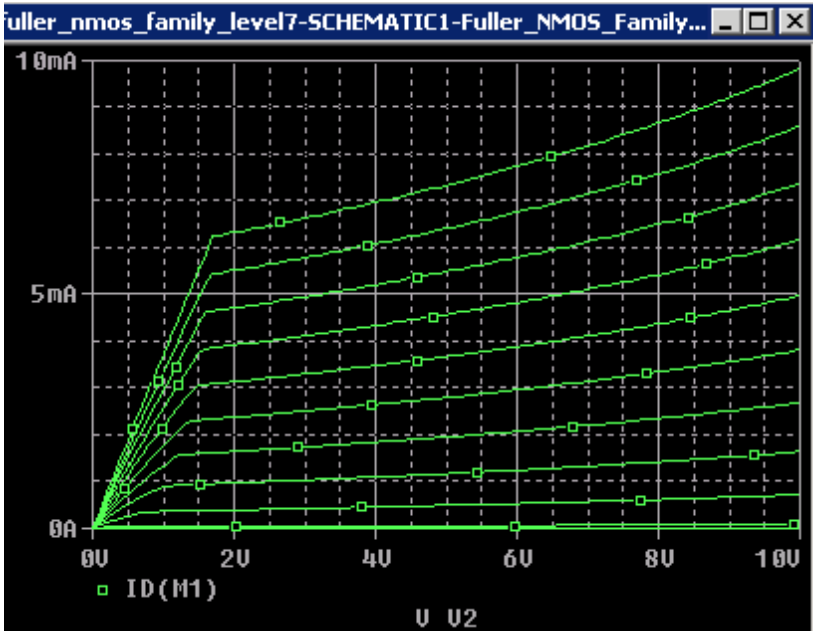
MEASURED FAMILY OF CURVES FOR RIT NMOS



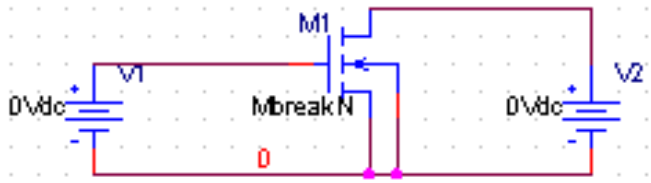
SIMULATIONS USING 1st GENERATION MODELS

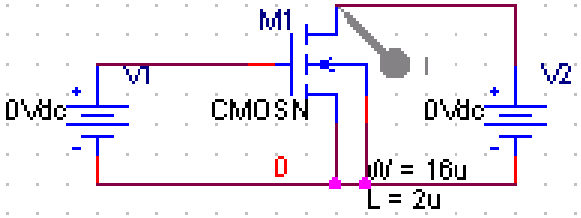


1st Generation - Level 1 Model



1st Generation - Level 2 Model





MOSFET DESCRIPTIONS

In SPICE a transistor is defined by its **name** and associated **properties or attributes** and its **model**. Its name and associated properties is given in the input file net list. Its model is given in the included library or model file or added to the input file.

For example:

* SPICE Input File (lines starting with * are comments and are ignored)

* MOSFET names start with M…. M2 is the name for the MOSFET below and its drain, gate, source

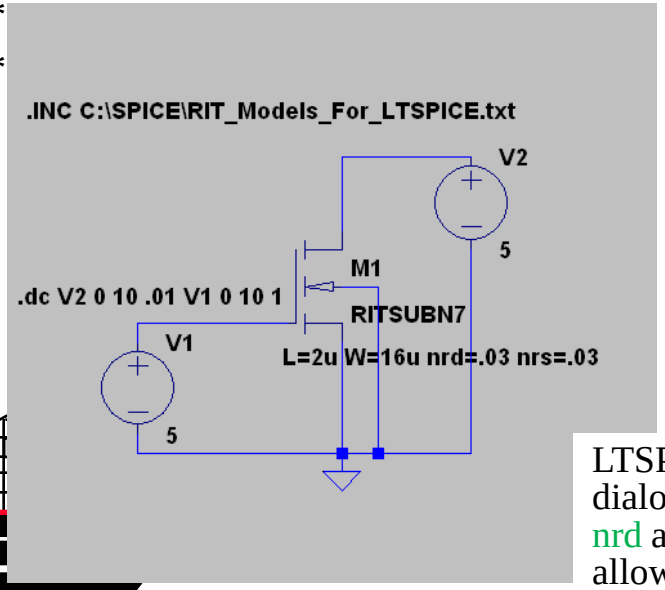
* and substrate is connected to nodes 3,2,0,0 respectively. The model name is RITSUBN7.

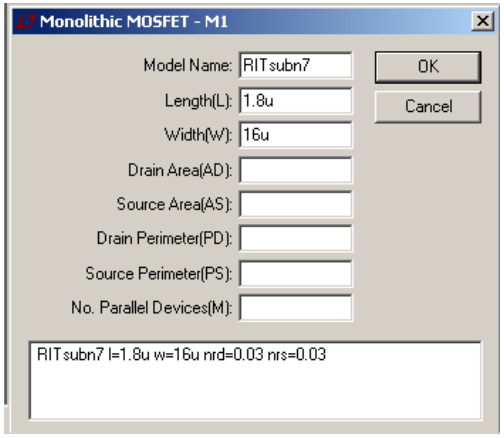
* The parameters/attributes is everything after that.

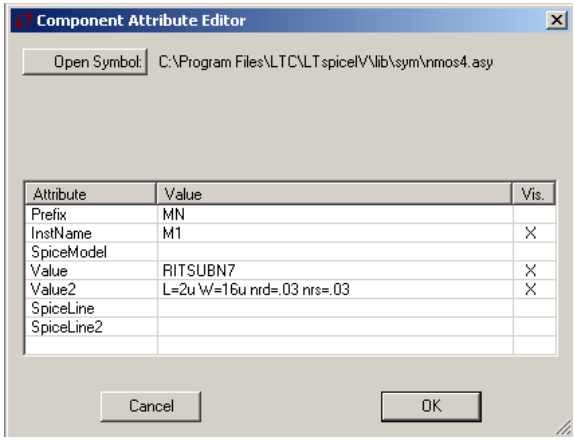
M2 3 2 0 0 RITSUBN7 L=2U W=16U ad=96e-12 as=96e-12 pd=44e-6 ps=44e-6 nrd=1.0 nrs=1.0

*

*







LTSPICE schematic showing **.Include** and **.dc** sweep commands. Properties dialog box to define L and W values. Note: attributes with no entry field nrs and nrd are typed in bottom box. Attribute Editor (CTRL click on the transistor) allows attributes with Vis.=X to be displayed on the schematic.

CHANGING THE MOSFET MODEL IN LTSPICE

There a several ways to change the model. A good way to do it is create a text file on your computer and put your models in that text file and save it in some folder. You can copy models from Dr. Fuller's webpage to start your collection of models.

See: http://people.rit.edu/lffeee/CMOS.htm

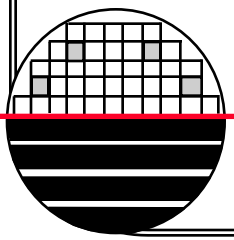
The contents of that file is shown on the page below.

Next you change the model name for your transistor by right click on the model name shown in your schematic and typing the model name used in the model file. (for example: RITSUBN7)

Finally you place a SPICE directive on your schematic by clicking on the .op icon on the top banner and type the following command:

.include Drive:\path\folder\filename

For example .inc C:\SPICE\RIT_Models_For_LTSPICE.txt

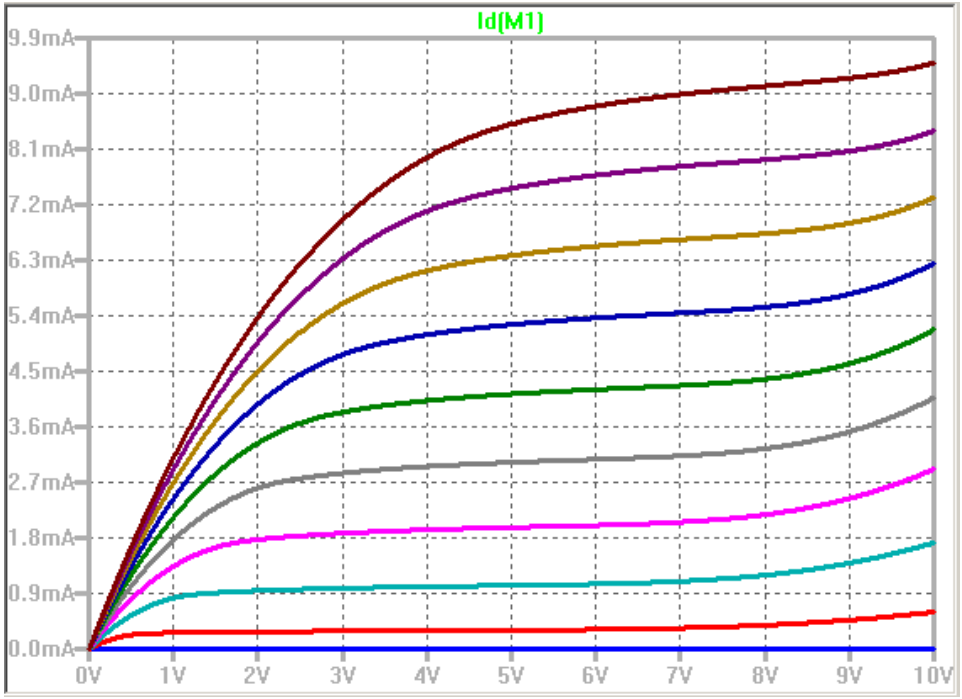


RIT_Models_for_LTSPICE

```
*SPICE MODELS FOR RIT DEVICES - DR. LYNN FULLER 12-24-2013
*LOCATION DR.FULLER'S COMPUTER C:/SPICE/MODELS/
*and also at: http://people.rit.edu/lffeee/CMOS.htm
*
.model RITMEMDIODE D IS=3.02E-9 N=1 RS=207
+VJ=0.6 CJO=200e-12 M=0.5 BV=400
*
*4-4-2013
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013
.MODEL RITSUBP7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
* From Electronics I EEEE481
.model EENMOS2 NMOS LEVEL=2
+VTO=0.7 KP=25E-6 LAMBDA=0.02 GAMMA=0.9 TOX=90E-9 NSUB=3.7E15
*
* From Electronics II EEEE482
.MODEL QRITNPN NPN (BF=416 IKF=.06678 ISE=6.734E-15 IS=6.734E-15 NE=1.259 RC=1 RB=10 VA=109)
```

Go to this location for complete file.

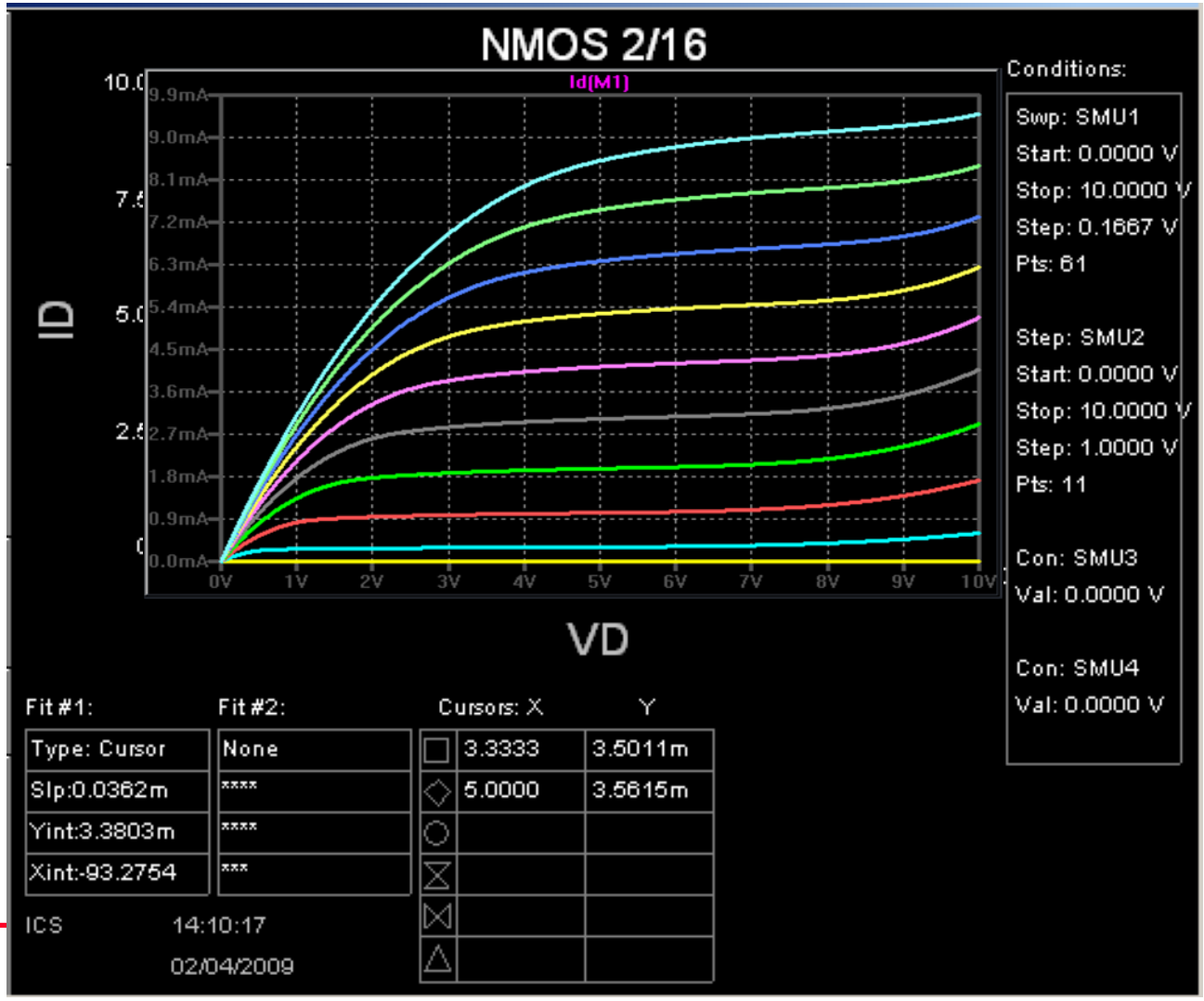
SIMULATIONS USING 3rd GENERATION MODELS



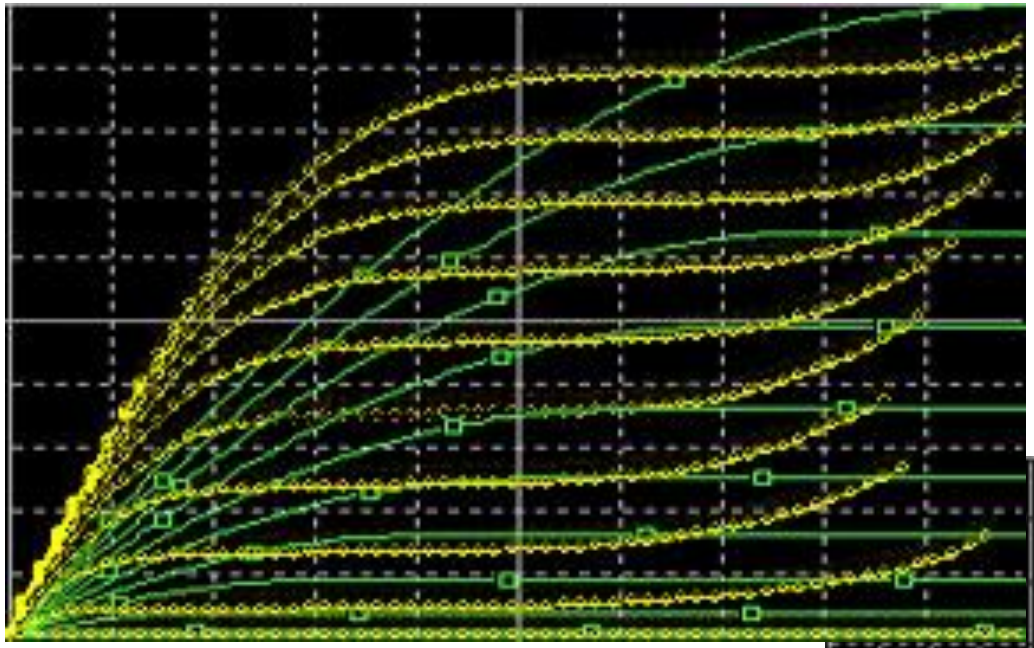
Simulated in LTSPICE using Level=7 model

Video Intro to LTSPICE.wmv

SIMULATED FAMILY OF CURVES FOR RIT NMOS

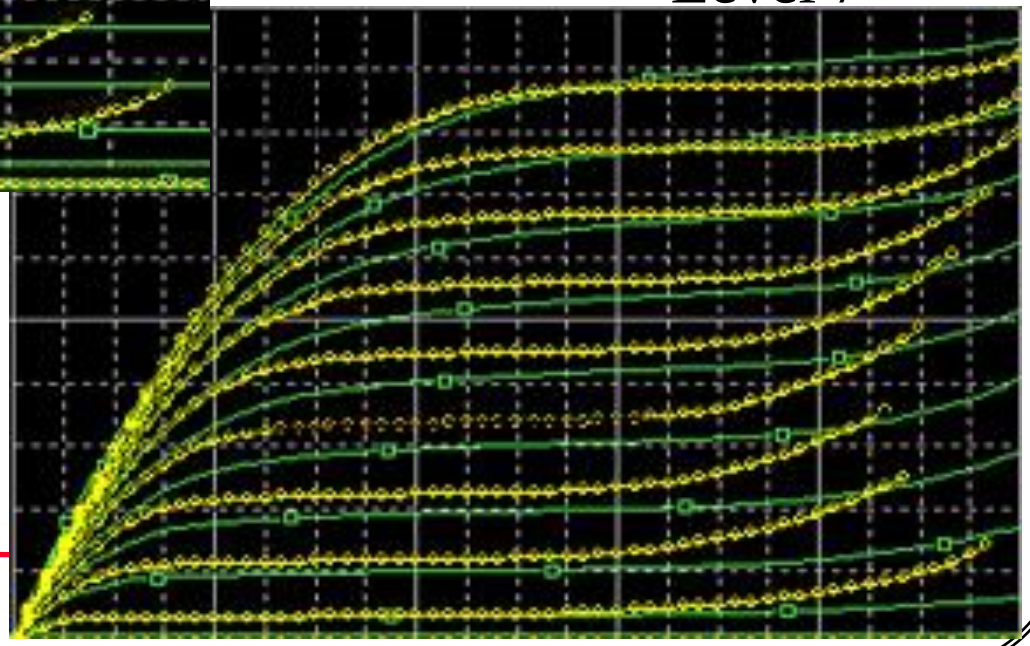


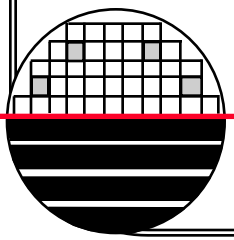
MEASURED COMPARED TO SIMULATION



Level 1

Level 7

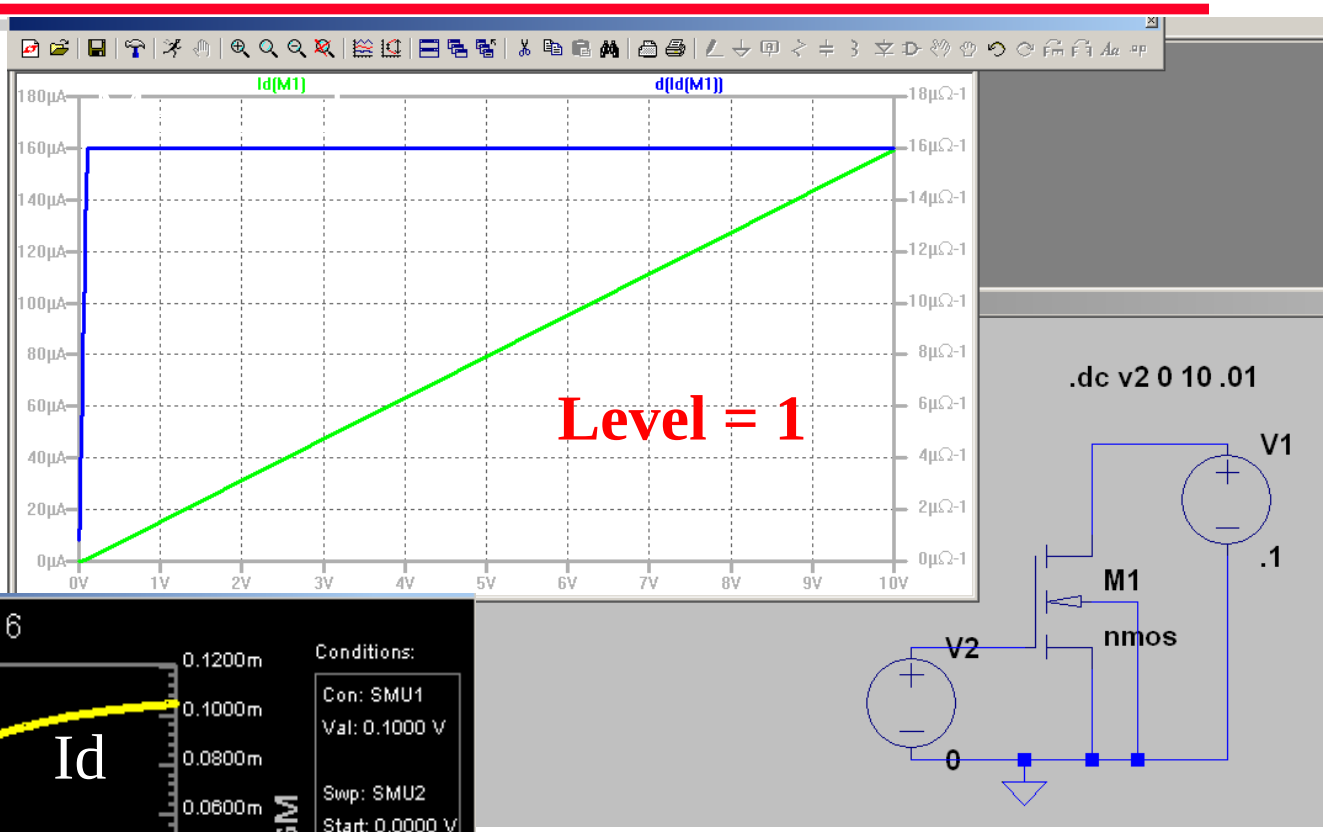


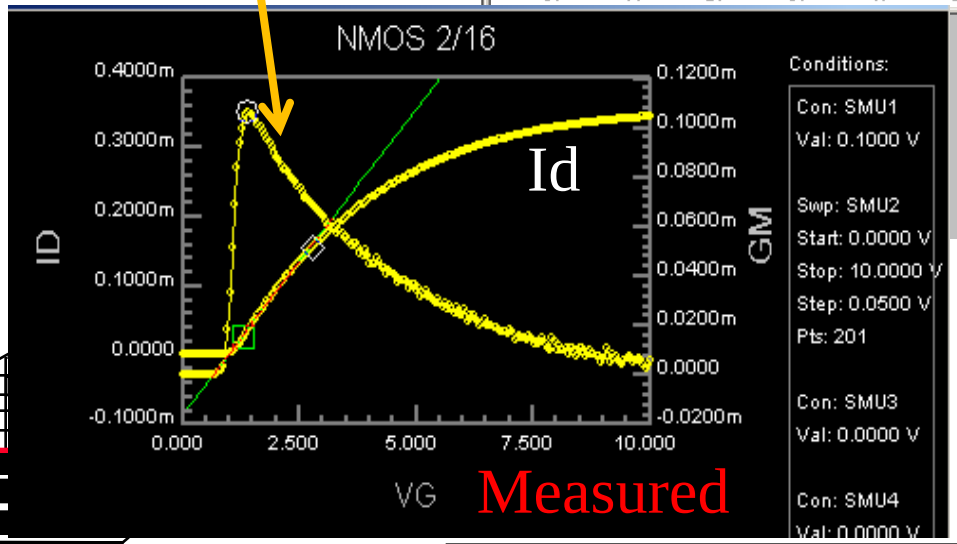


ID-VGS AND GM-VGS USING LTSPICE

gm is the derivative of drain current.

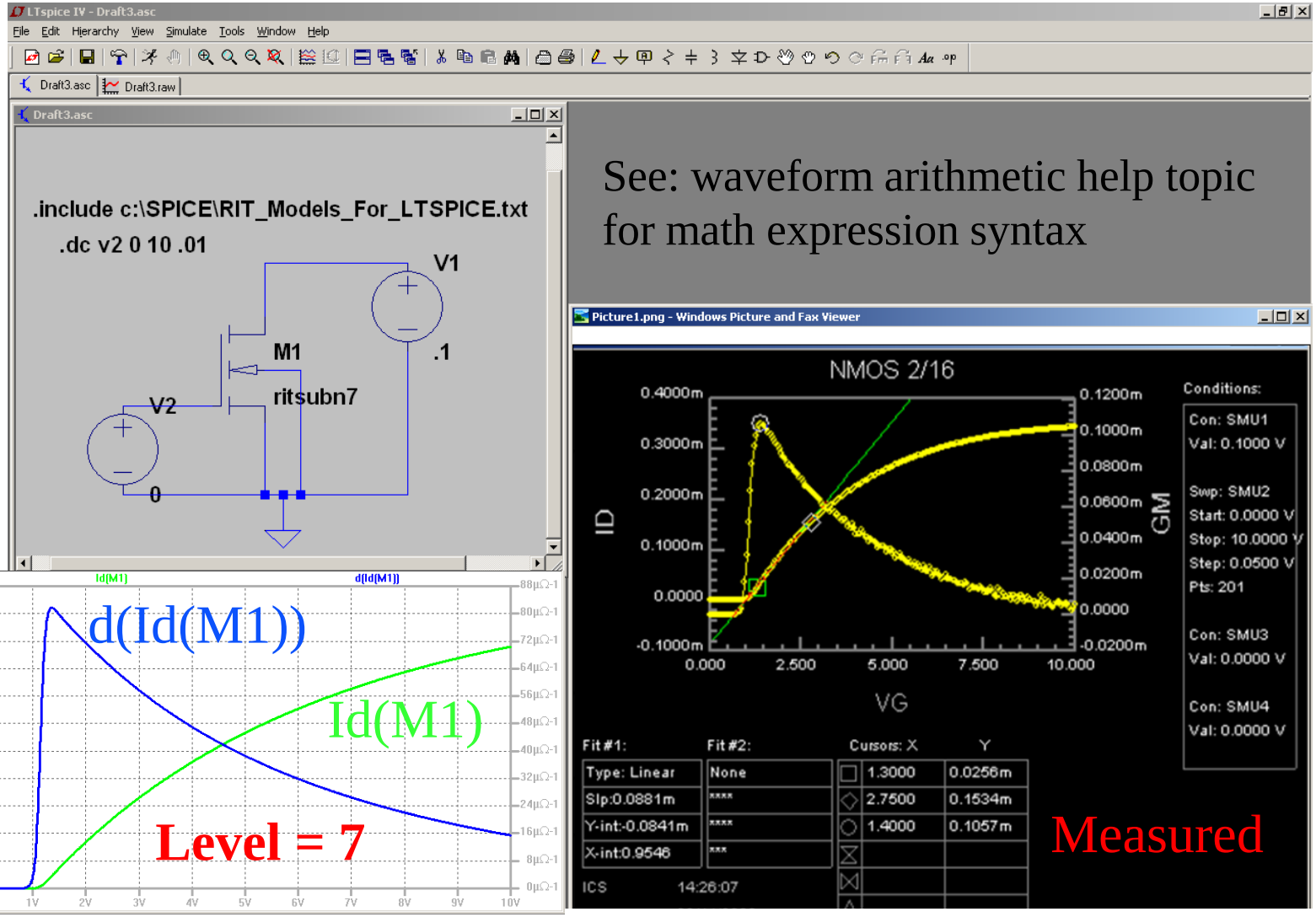
d(Id(M1))



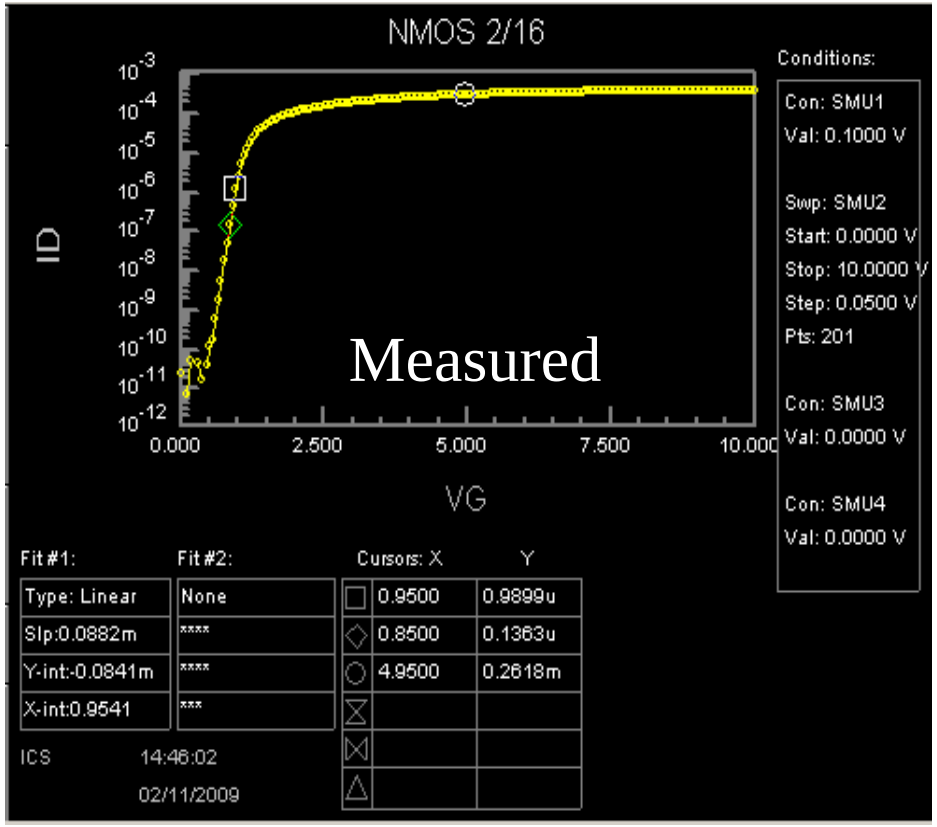


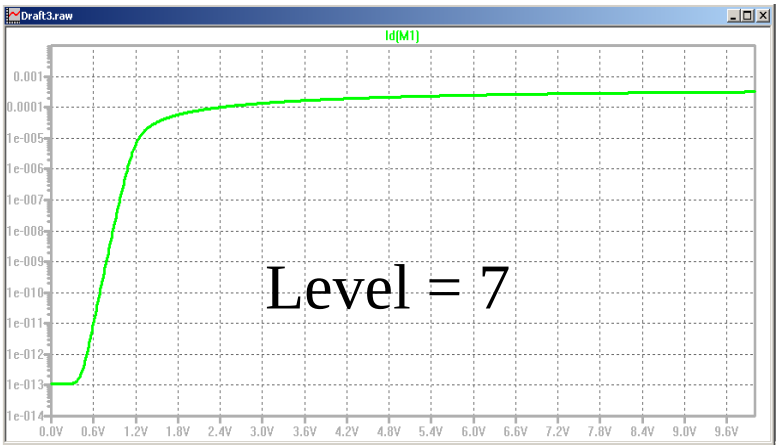
See: waveform arithmetic LTSPICE help topic for math expression syntax

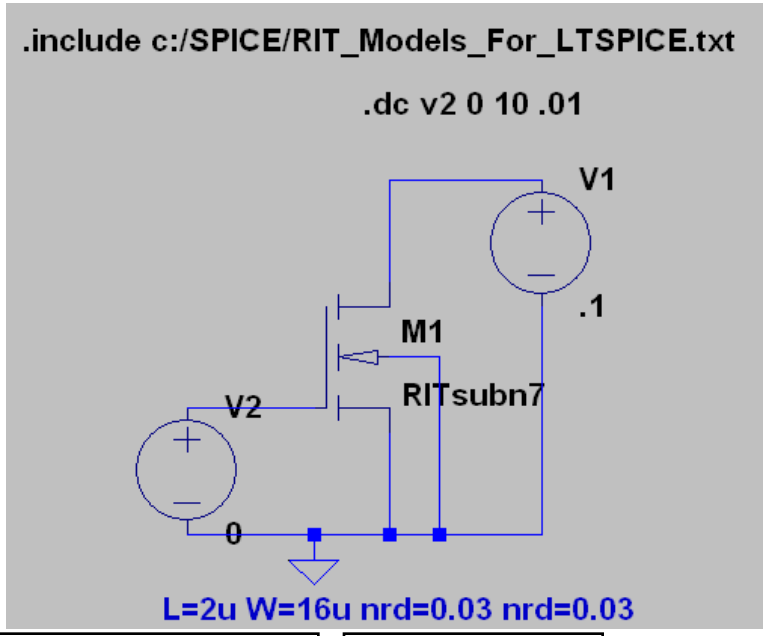
ID-VGS AND GM-VGS USING LTSPICE



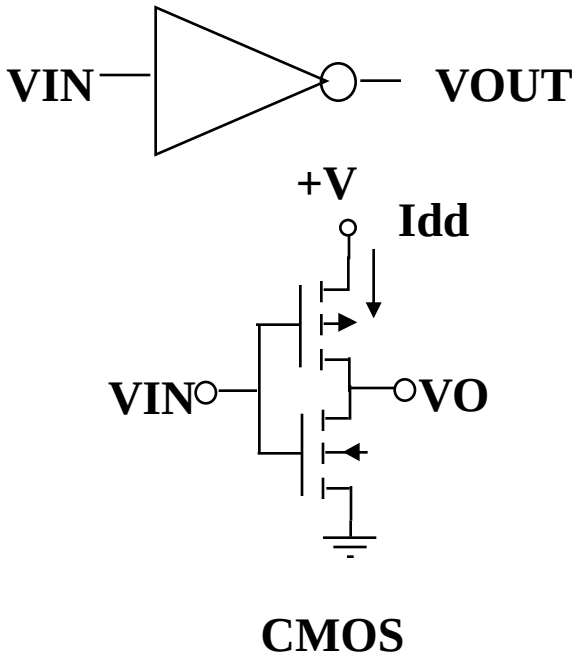
MEASURED and SIMULATED Sub-Threshold Ids-Vgs

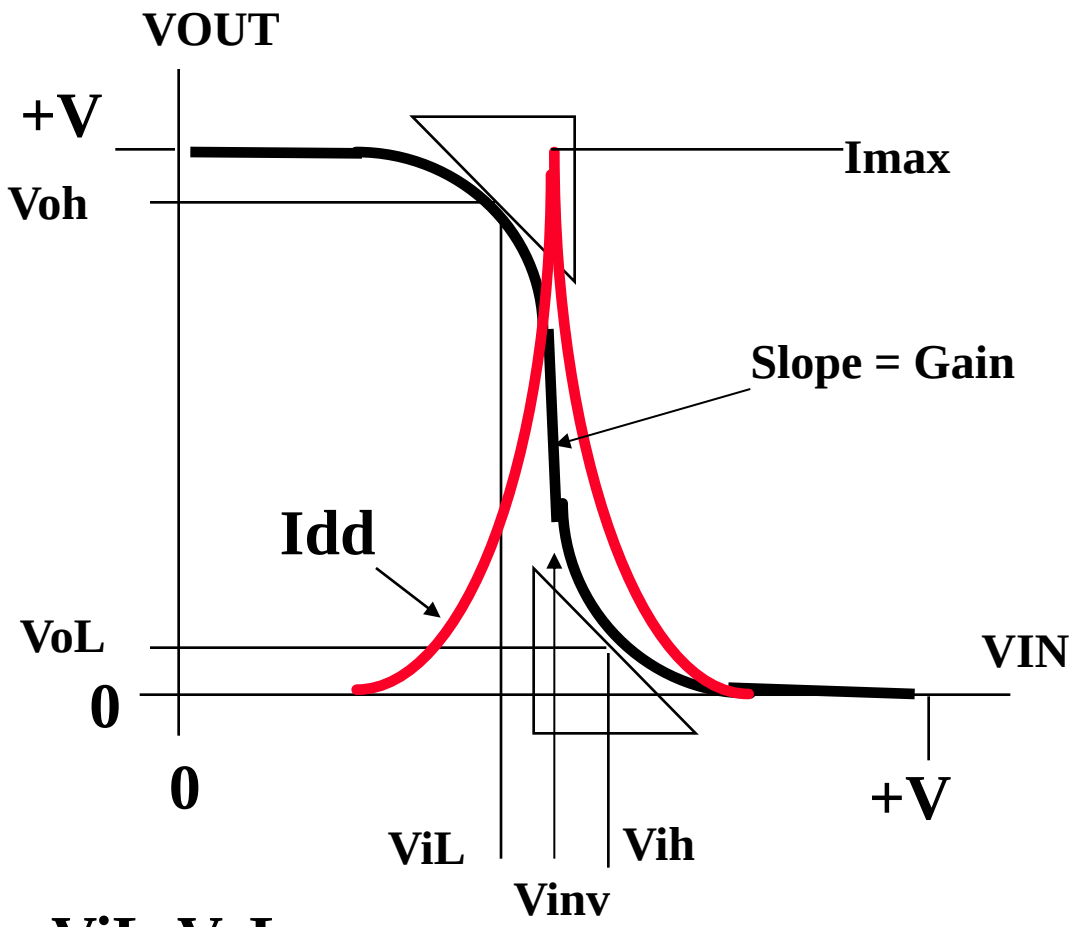






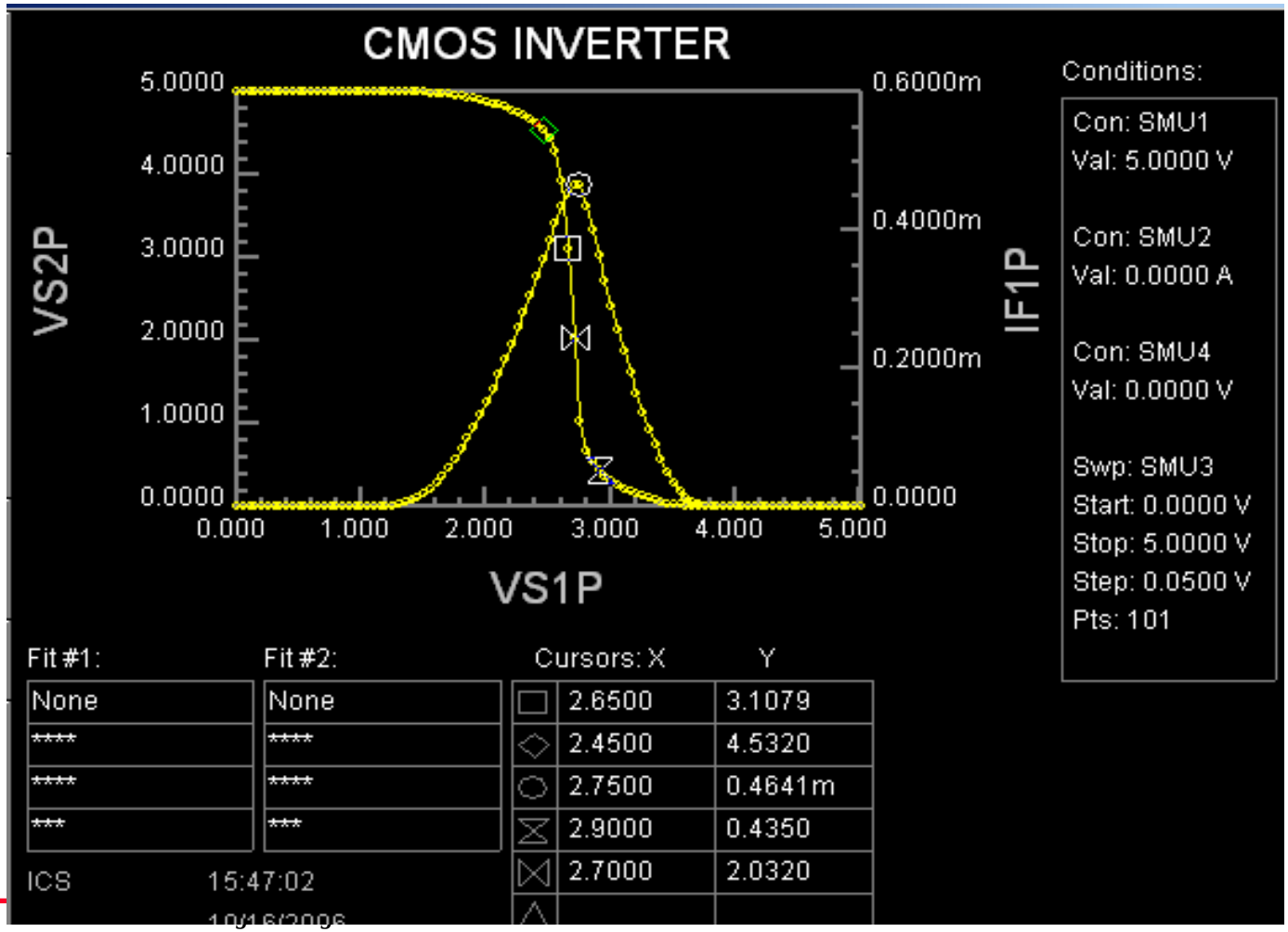
CMOS THEORETICAL INVERTER VOUT VS VIN



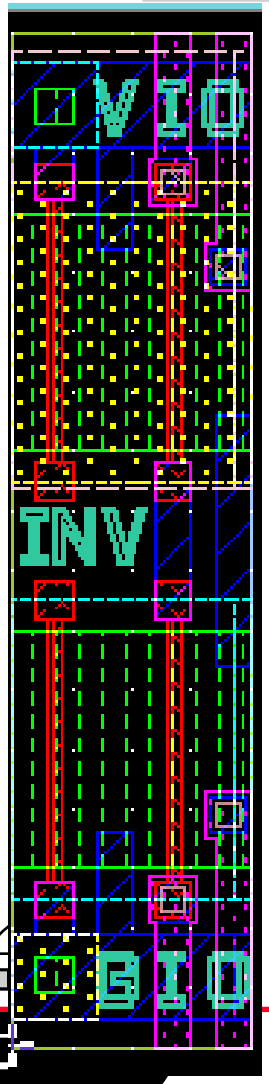


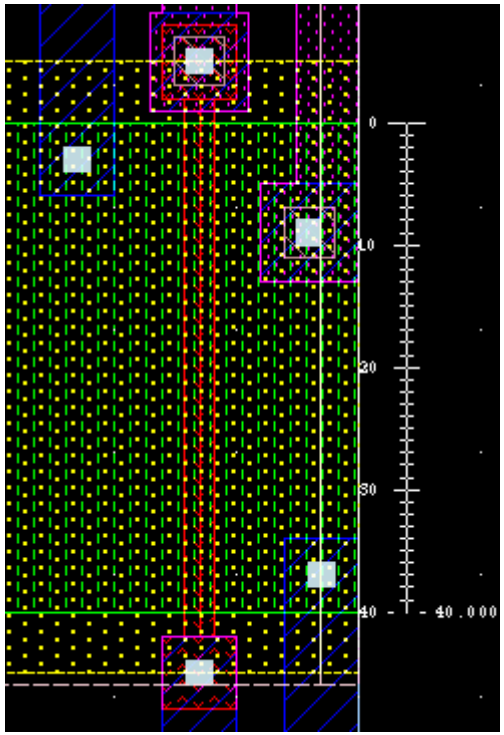
Δ0 noise margin=ViL-VoL
Δ1 noise margin=VoH-ViH

MEASURED CMOS INVERTER VOUT & I VS VIN

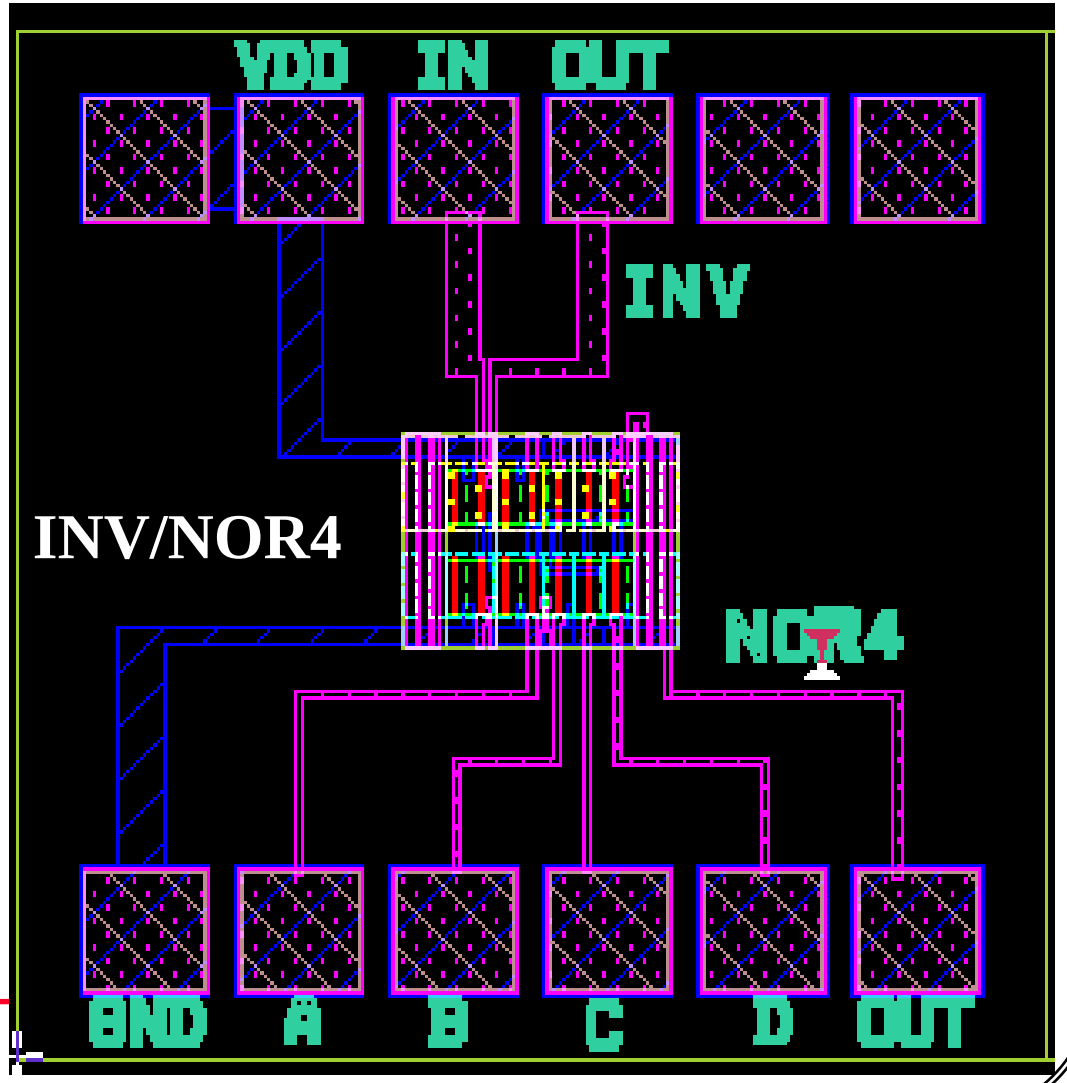


INVERTER LAYOUT WITH PADS

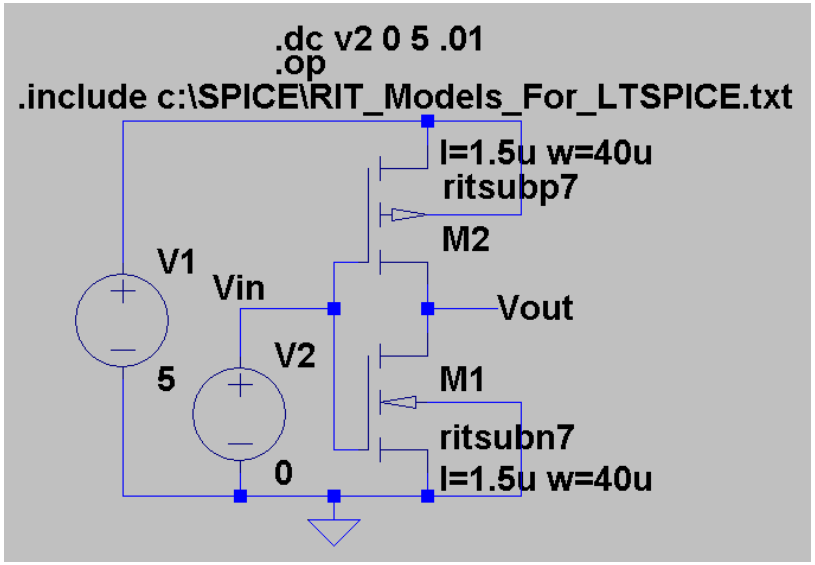


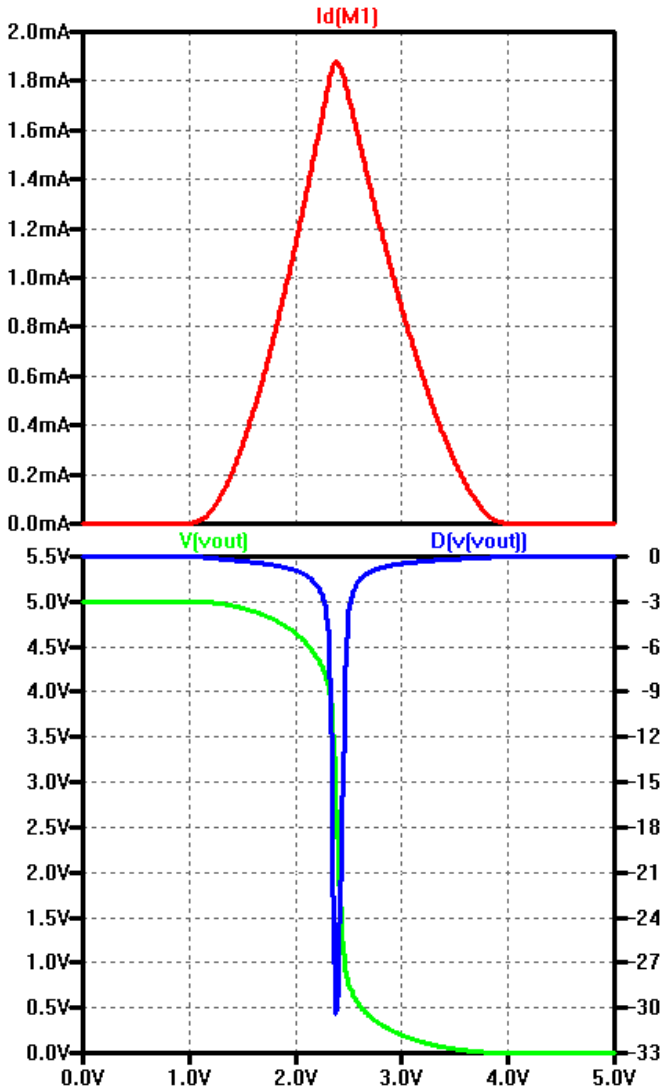


W = 40 µm
Ldrawn = 2.5µm
Lpoly = 1.5µm
Leff = ~1.0 µm



DC SIMULATION OF INVERTER VOUT & I VS VIN

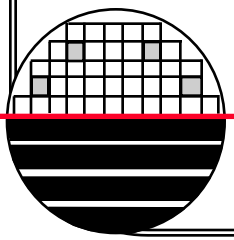




Gain = -30 V/V
Imax = 1.8mA
Vinv = 2.34
ViH = 2.61
VoH = 4.32
ViL = 2.24
Vol = 0.47
Δ0 = ViL-VoL = 1.77
Δ1 = VoH-ViH = 1.71

CONCLUSION FROM DC MODEL COMPARISON

Third generation MOSFET models such as Level 7 give better results than any of the 1st or 2nd generation models. These models are different for different processes (such as RIT's Sub-CMOS 150 or RIT's Adv-CMOS 150 processes)



RING OSCILLATOR, td, THEORY

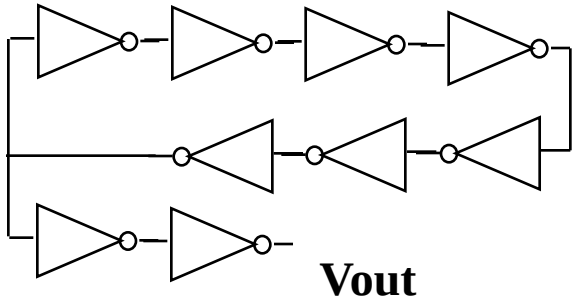
Seven stage ring oscillator with two output buffers

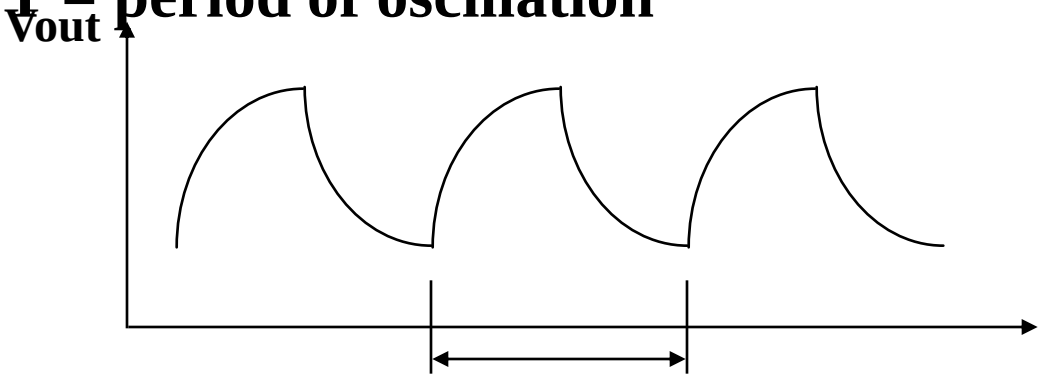
td = T / 2 N

td = gate delay

N = number of stages

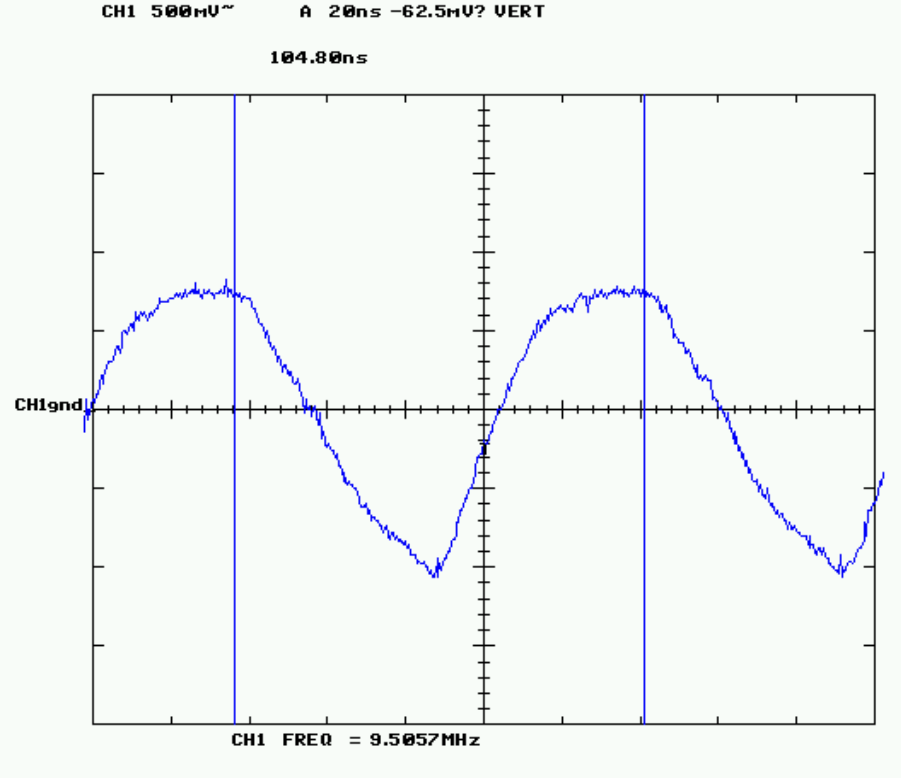
T = period of oscillation

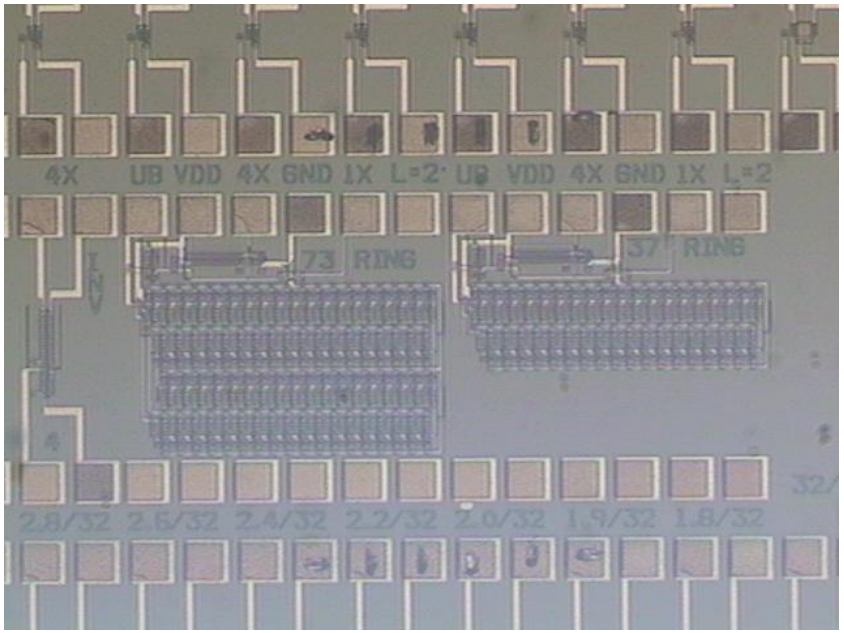




T = period of oscillation

MEASURED RING OSCILLATOR OUTPUT

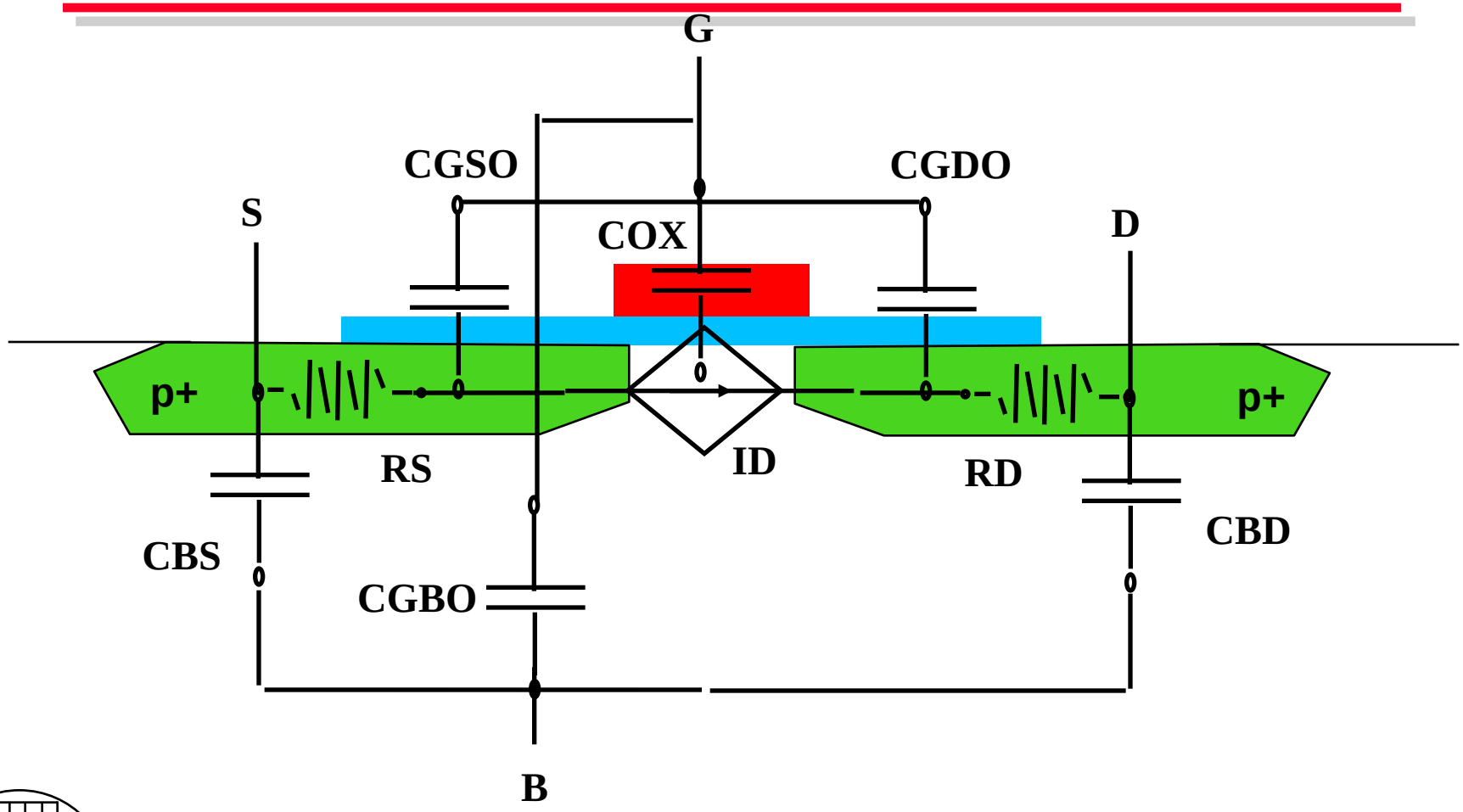




73 Stage Ring at 5V

td = 104.8ns / 2(73) = 0.718 ns

SPICE LEVEL-1 MOSFET MODEL



where ID is a dependent current source using simple long channel equations.

AC MODEL FOR MOSFETS

The AC response of a MOSFET are partially determined by the internal resistance and capacitance values. These values are calculated by SPICE using the spice model and the attributes shown below.

RS,RS	Source/Drain Series Resistance, ohms
RSH	Sheet Resistance of Drain/Source, ohms
CGSO,CGDO	Zero Bias Gate-Source/Drain Capacitance, F/m of width
CGBO	Zero Bias Gate-Substrate Capacitance, F/m of length
CJ	DS Bottom Junction Capacitance, F/m2
CJSW	DS Side Wall Junction Capacitance, F/m of perimeter
MJ	Junction Grading Coefficient, 0.5
MJSW	Side Wall Grading Coefficient, 0.5

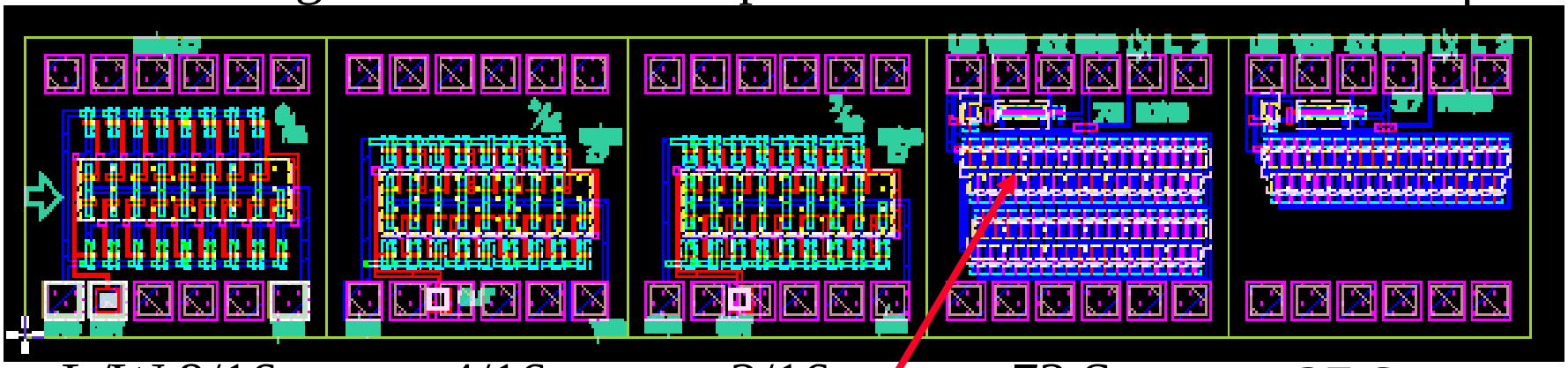
These are combined with the transistors parameters (attributes)

L, W	Length and Width
AS,AD	Area of the Source/Drain
PS,PD	Perimeter of the Source/Drain
NRS,NRD	Number of squares Contact to Channel

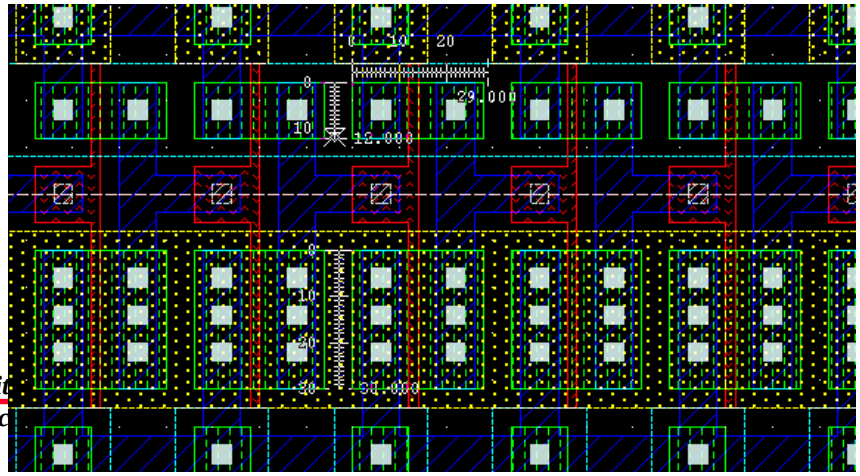
RING OSCILLATOR LAYOUTS

17 Stage Un-buffered Output

L/W=2/30 Buffered Output

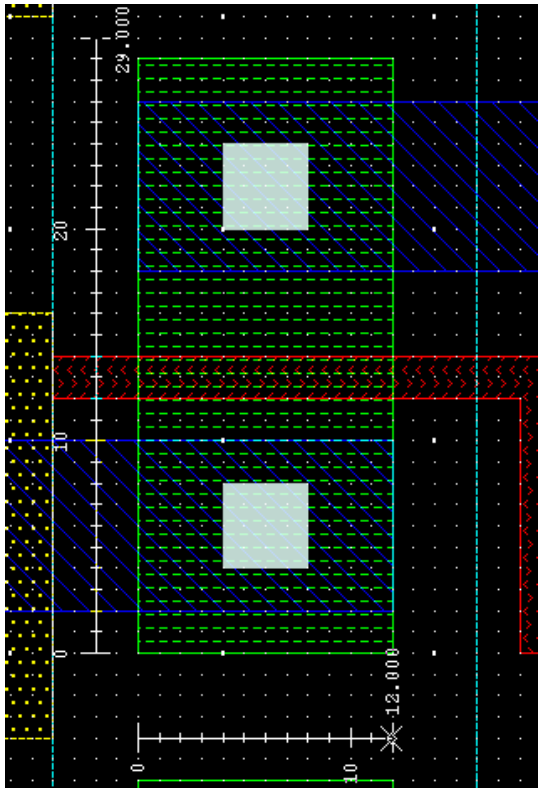


L/W 8/16 4/16 2/16 73 Stage 37 Stage

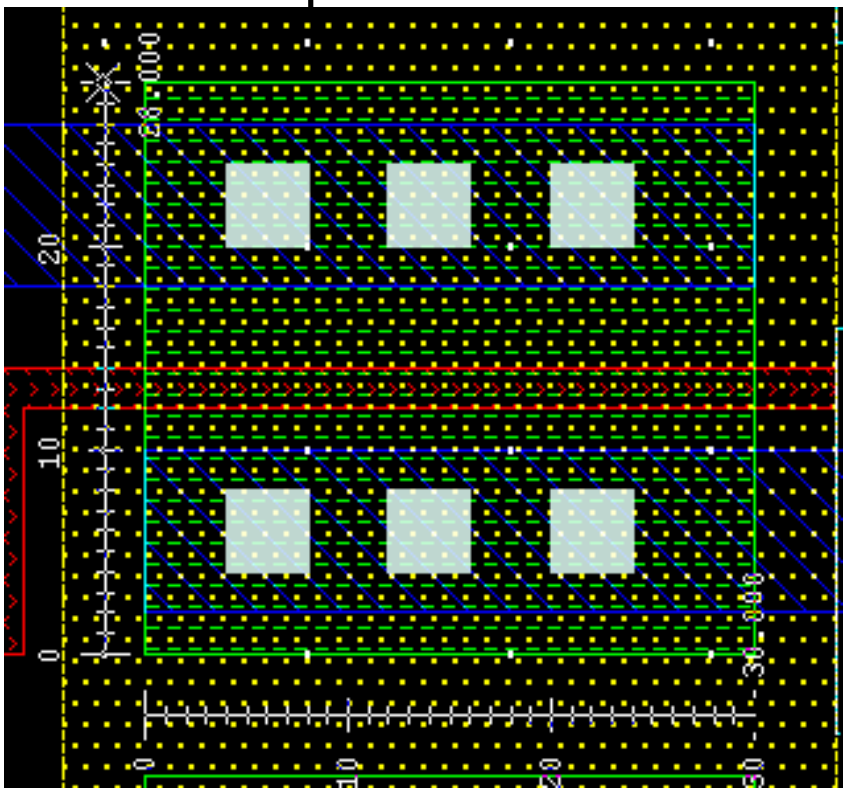


MOSFETS IN THE INVERTER OF 73 RING OSCILLATOR

nmosfet



pmosfet



73 Stage Ring Oscillator

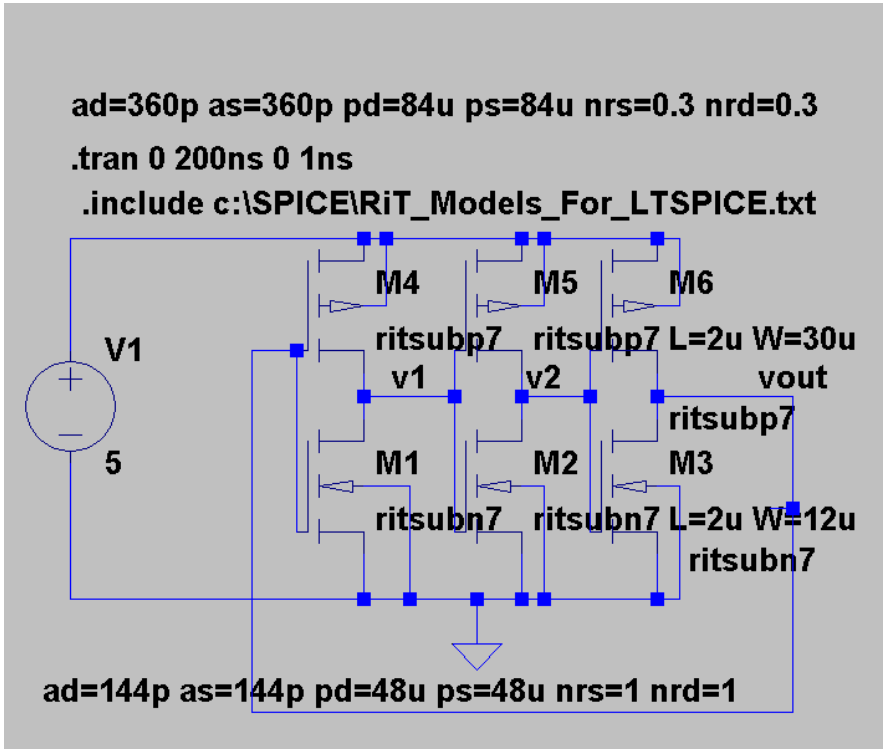
FIND DIMENSIONS OF THE TRANSISTORS

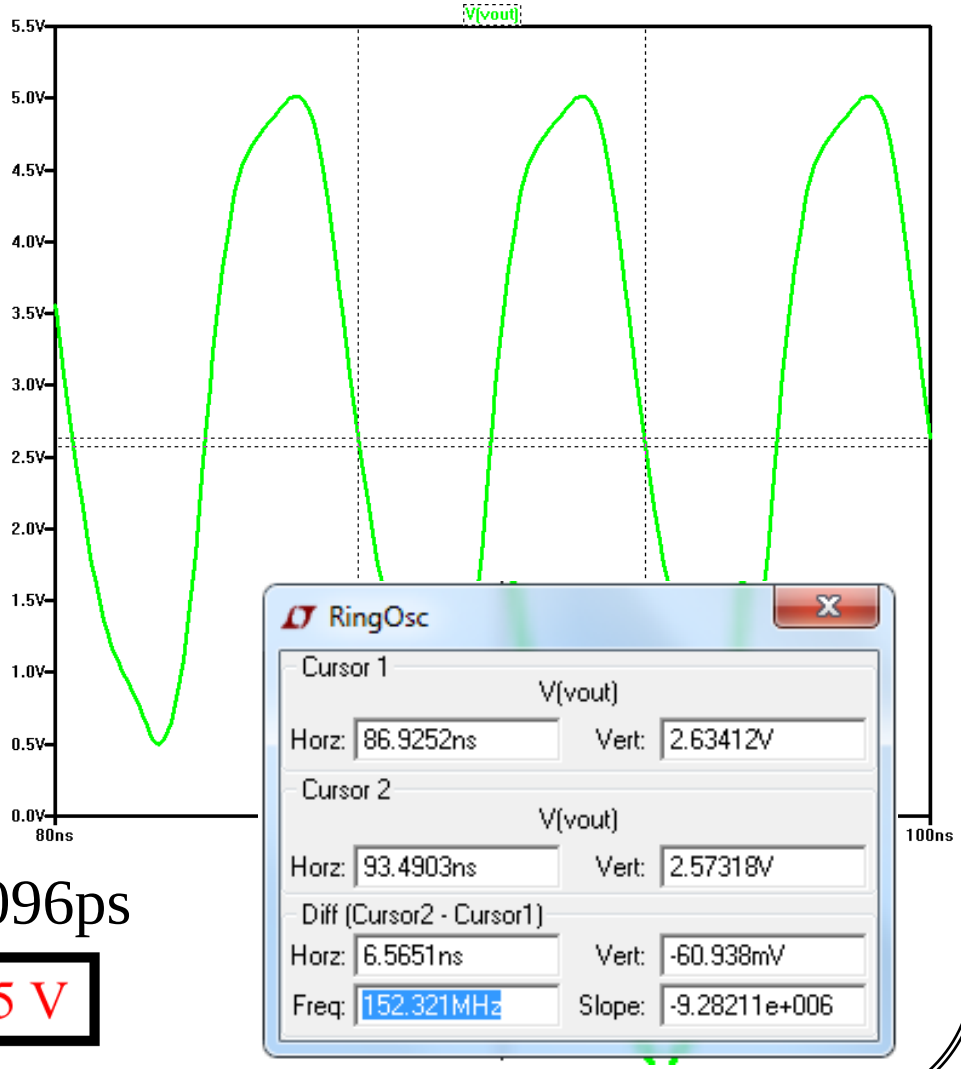
	NMOS	PMOS
L	2u	2u
W	12u	30u
AD	12ux12u=144p	12ux30u=360p
AS	12ux12u=144p	12ux30u=360p
PD	2x(12u+12u)=48u	2x(12u+30u)=84u
PS	2x(12u+12u)=48u	2x(12u+30u)=84u
NRS	1	0.3
NRD	1	0.3

73 Stage

Use Ctrl right Click on all NMOS and all PMOS\
Then enter these values. Double click in right column
X means values will be displayed on schematic.

LTSPICE SIMULATED RING OSCILLATOR AT 5 VOLTS





td = 1/(152MHz (2) 3) = 1096ps

Measured td = 0.718 nsec @ 5 V

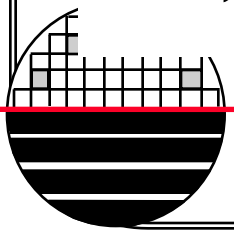
CONCLUSION

Since the measured and the simulated gate delays, td are close to correct, then the SPICE model must be close to correct. The inverter gate delay depends on the values of the internal capacitors and resistances of the transistor.

Specifically:
RS, RS, RSH
CGSO, CGDO, CGBO
CJ, CJSW

These are combined with the transistors

L, W	Length and Width
AS,AD	Area of the Source/Drain
PS,PD	Perimeter of the Source/Drain
NRS,NRD	Number of squares Contact to Channel



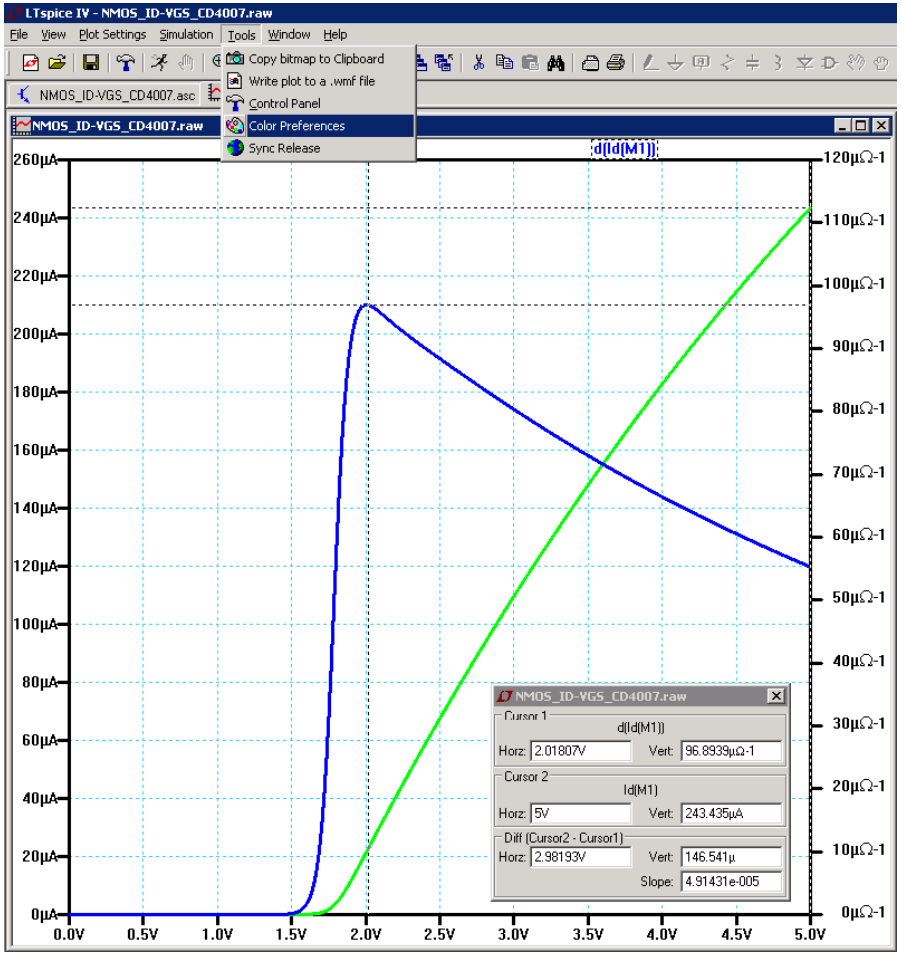
SETTING COLORS FOR LTSPICE WAVEFORM

Colors can be set using the tools menu on the top banner.

A curser can be set by left click on trace name at top of the waveform. The x and y location of the curser will be displayed.

A second curser can be set up by right click on the trace name. The x and y location of both cursers will be displayed along with the differences and slope

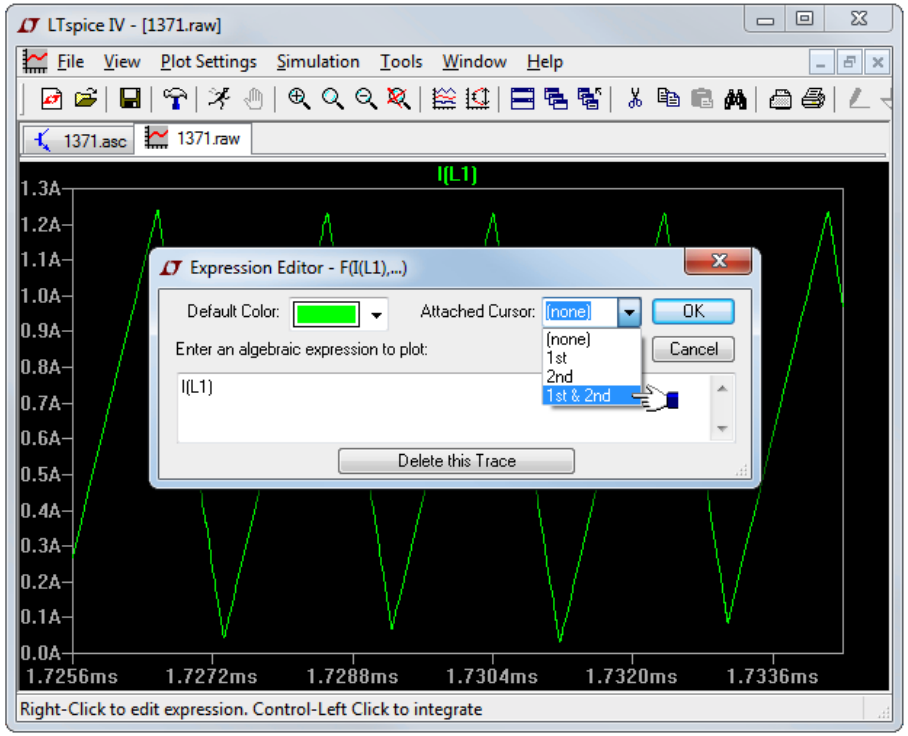
Tools also provides for copy of bitmap to clipboard function.



ATTACHING CURSORS TO THE WAVEFORM

Attached Cursors

There are up to two attached cursors available. You can attach a cursor to a trace by left mouse clicking on the trace label. You can attach both cursors to a single trace by right clicking on the trace label and selecting "1st & 2nd". You can also attach the 1st or 2nd cursor or both cursors to any trace by right clicking on that trace's label and using the Attached Cursor drop down box. The attached cursors can be dragged about with the mouse or moved with the cursor keys.

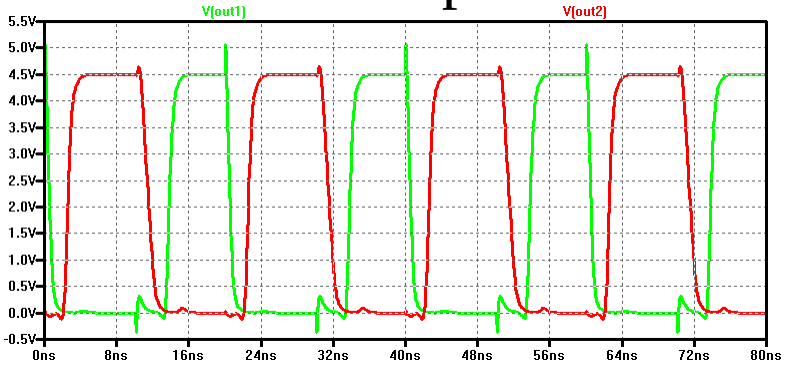


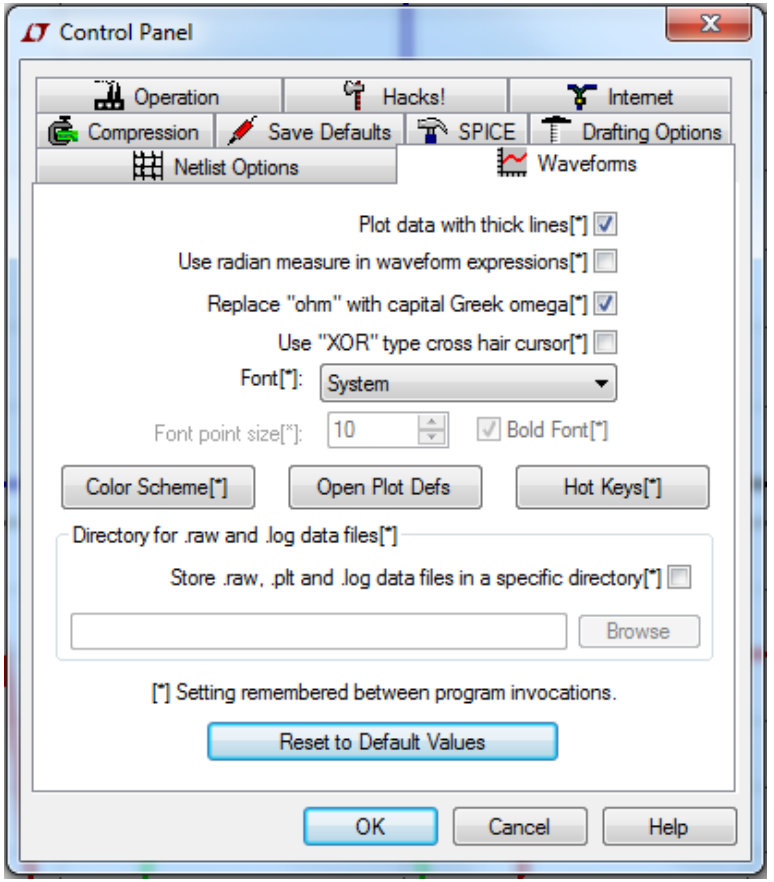
When there are active attached cursors, a readout display becomes visible that will tell you the location and difference of the cursors.

SETTING THICK LINES ON PLOTS IN LTSPICE

Under tools > Control Panel > waveforms you can select Plot data with thick lines

Default axis color and plot line thickness

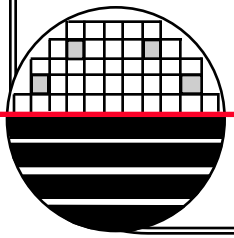




Change axis color to black and plot with thick lines

REFERENCES

1. MOSFET Modeling with SPICE, Daniel Foty, 1997, Prentice Hall, ISBN-0-13-227935-5
2. Operation and Modeling of the MOS Transistor, 2nd Edition, Yannis Tsividis, 1999, McGraw-Hill, ISBN-0-07-065523-5
3. UTMOST III Modeling Manual-Vol.1. Ch. 5. From Silvaco International.
4. ATHENA USERS Manual, From Silvaco International.
5. ATLAS USERS Manual, From Silvaco International.
6. Device Electronics for Integrated Circuits, Richard Muller and Theodore Kamins, with Mansun Chan, 3rd Edition, John Wiley, 2003, ISBN 0-471-59398-2
7. ICCAP Manual, Hewlet Packard
8. PSpice Users Guide.
9. Dr. Fuller's webpage: http://people.rit.edu/lffeee



HOMEWORK – INTRO TO LTSPICE

1. Do LTSPICE simulations for all the examples in this document.
2. Do an LTSPICE simulation for sub-CMOS 150 PMOS FET.