ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Introduction to Maskmaking

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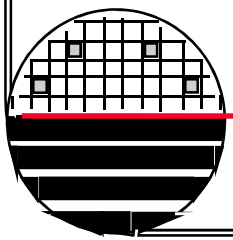
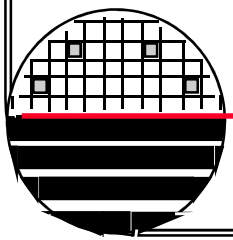


OUTLINE

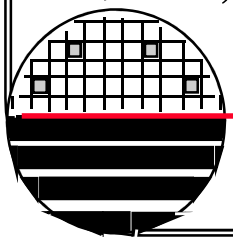
Introduction
Mask & Reticle Types
MEBES
Mask Process Flow
Pattern Generation
Example of a MEBES Job Deck
Example of a MEBES Plot Job
Mask Etching
Mask Inspection & Repair
Mask Linewidth Measurement
Mask Pellicle Operations
GCA Reticle & Fiducial Marks
Cannon Reticle & FiducialMarks
Masks for Four Different CMOS Processes
Tiling
References



INTRODUCTION

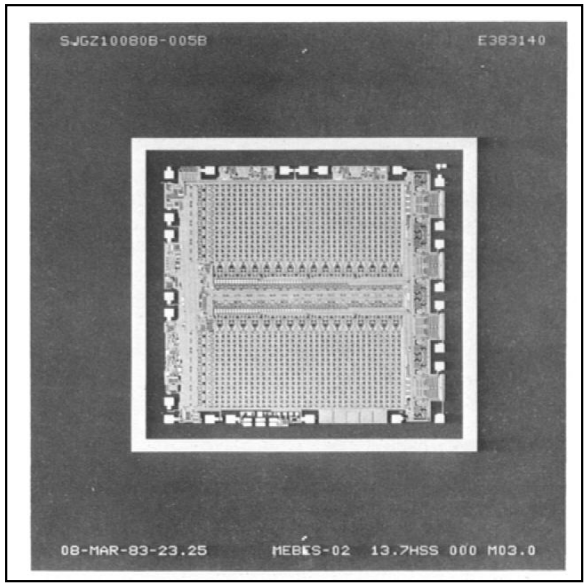
Mask Procurement Engineer: the engineer responsible for obtaining masks to make a microchip. The design file from the design engineer is merged with manufacturing information to create a purchase order for a mask set from a company that makes photomasks for the semiconductor industry (mask house). The manufacturing information needed includes, type of lithography tool (stepper (Canon, ASML), contact, etc.), reticle alignment marks, barcodes, labels, mask plate size/thickness, type of glass, etc. A detailed set of instructions on how to combine the design layers, bias, rotate, mirror and add features that are not part of the design is needed for each layer. Information about anti-reflective coatings, pellicles and inspection details also need specification.

Masks can cost $1000 to $10,000 each. A mask set can cost $200,000 or more.

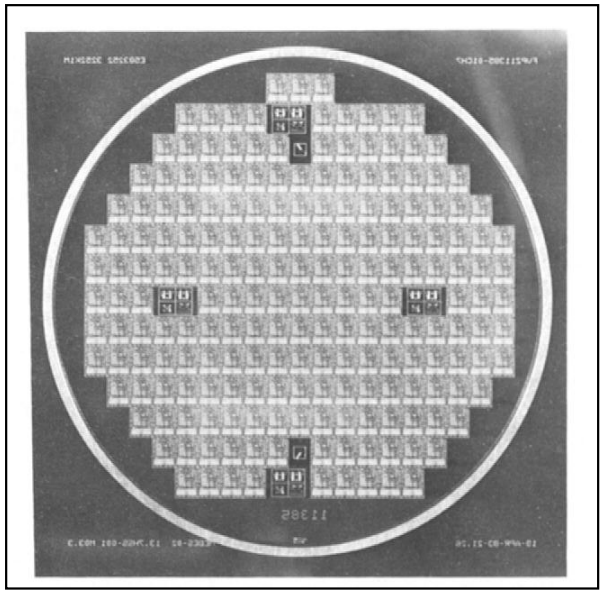


MASK AND RETICLE TYPES

Reduction reticle with pellicle:
ASML, GCA, Canon, Nikon, others

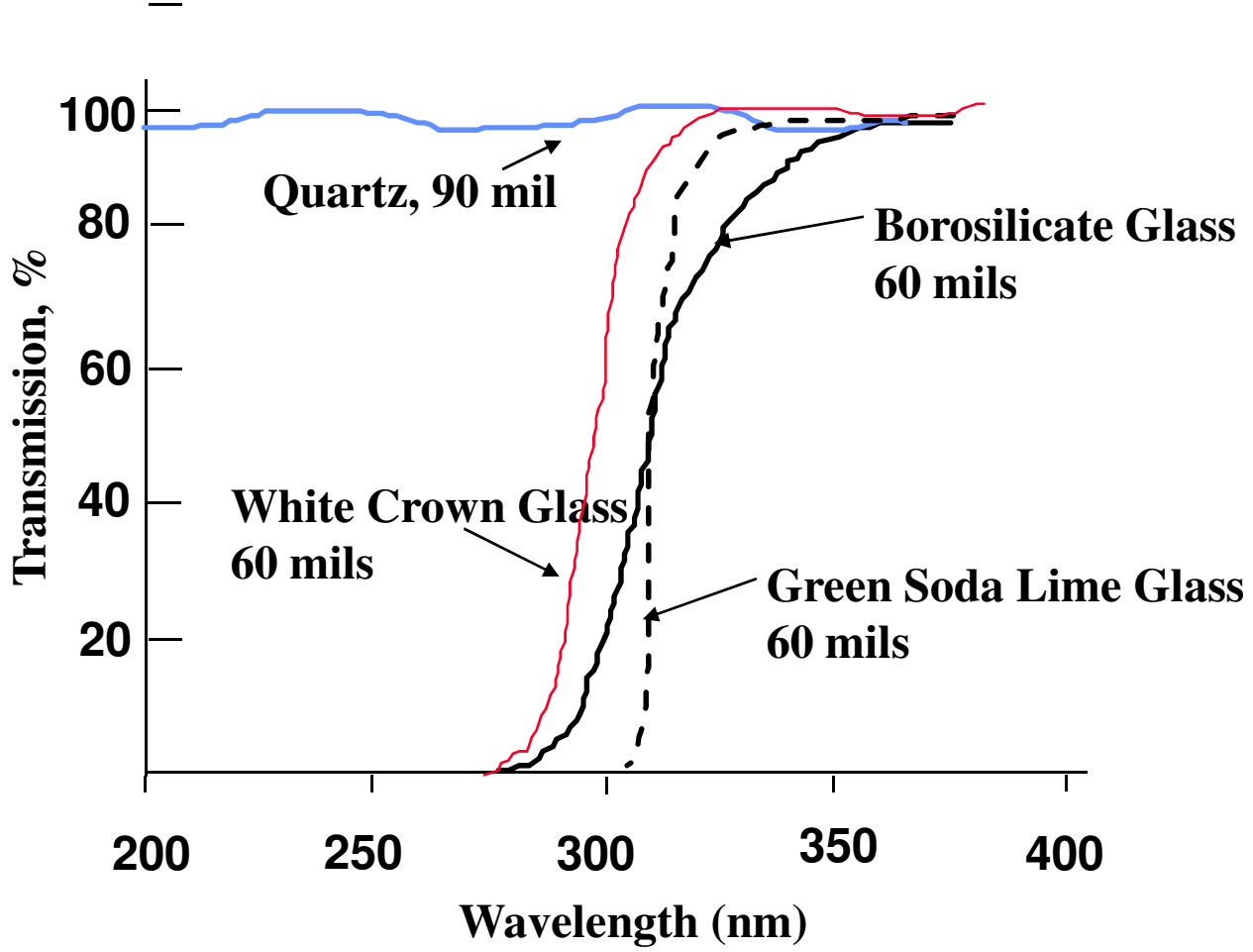


1X projection with pellicle:
Perkin Elmer Scanners



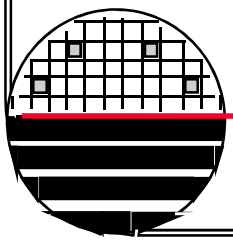
Other Types: 2X, 4X, 5X, 10X reduction, 1X contact

TRANSMISSION PROPERTIES OF OPTICAL GLASS



MEBES

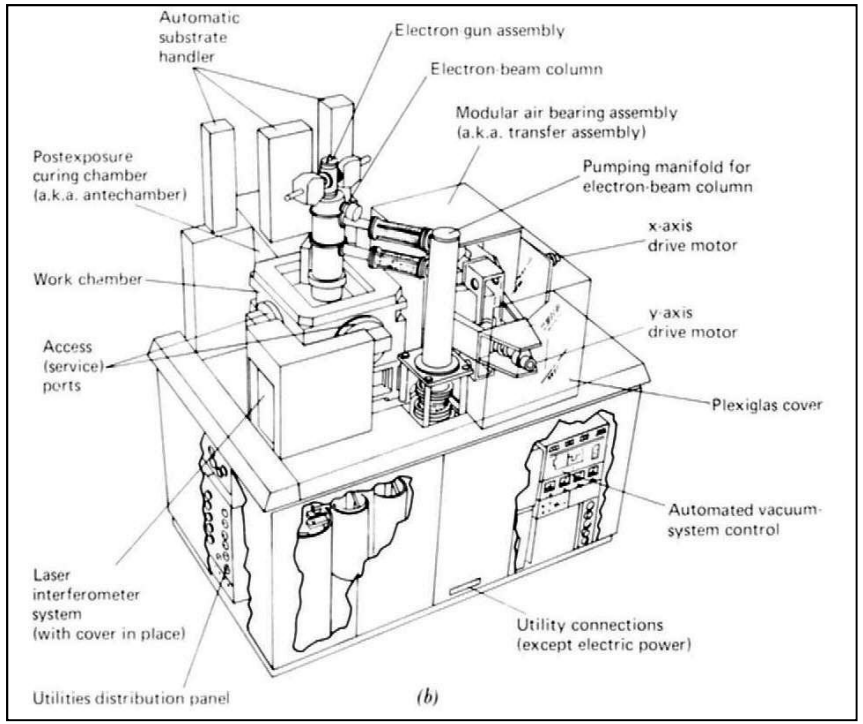
Manufacturing Electron Beam Exposure System



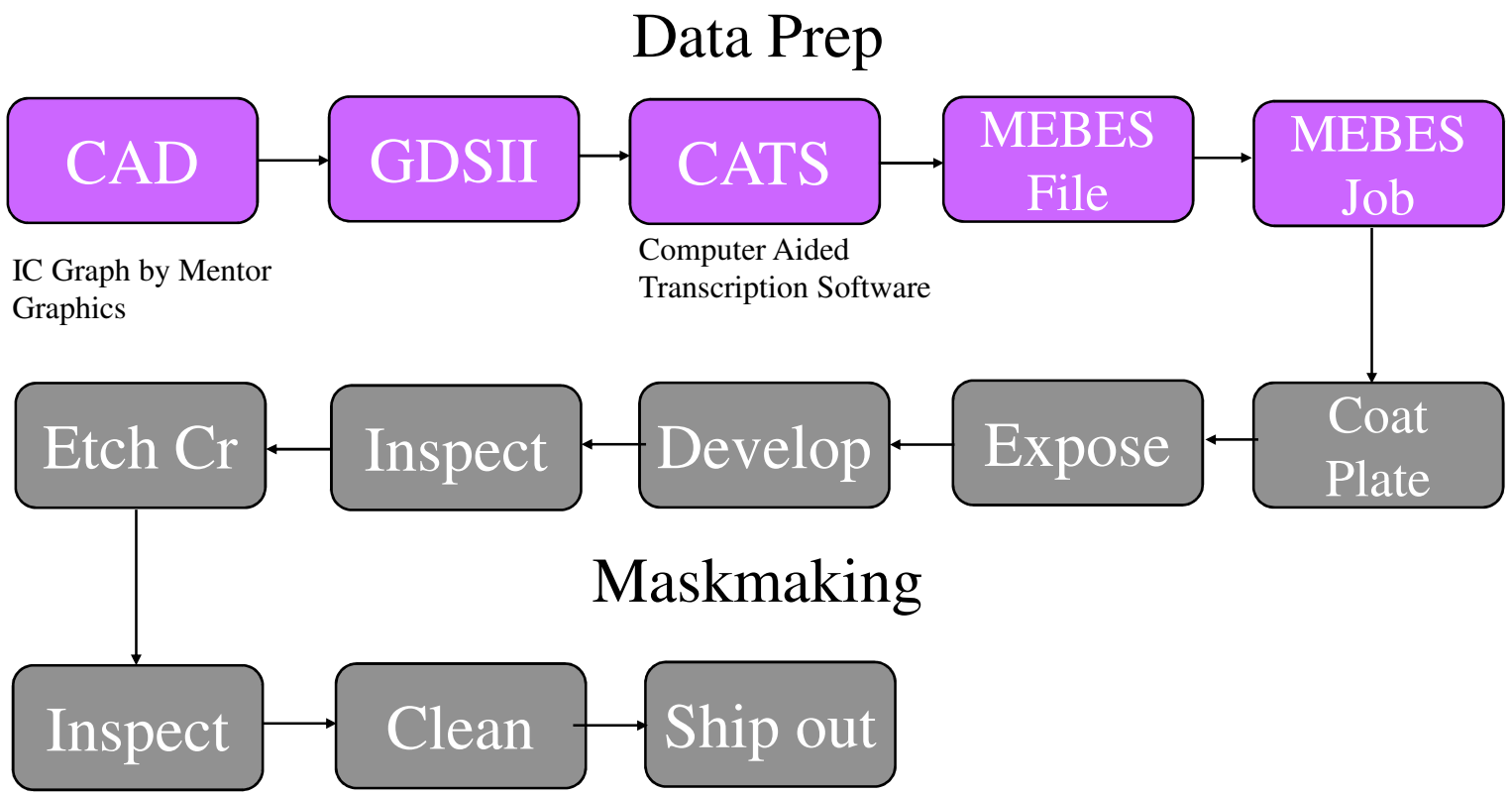
MASK IMAGING - ELECTRON BEAM

- Mask blanks are resist on chrome
- IBM used Hontas EL tools
- System is under vacuum
- 10-20kV, 10-100 nA, E-6 to -12T
- Resists used may be:

1. COP negative P(GMA-co-EA) developed in methyl ethyl ketone (MEK) and ethanol.
2. PBS [P(butene sulfone)] or other poly sulfones developed in methyl hexanone or MIAK and isoproponol.
3. Optical DNQ/novolac (eg AZ1350 in solvent) developed in NaOH or tetramethyl ammonium hydroxide (TMAH)



MASK PROCESS FLOW



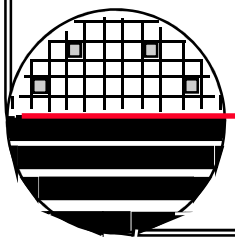
PATTERN GENERATION AND DATA PREP

1. Using Mentor Graphics Design Tools, layout the device layers and save in mentor format. Mentor- ICGraph files (filename.iccel), all layers, polygons with up to 200 vertices

2. Convert the layout information to GDSII file format. GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

3. The GDSII format is then transferred to the CATS system for fracturing (conversion to MEBES format), and other data manipulations such as rotate, mirror, size, bias, and boolean combinations. MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only

4. Save the file, transfer to the MEBES or other mask writing tool.



MOSIS TSMC 0.35 2POLY 4 METAL PROCESS

General Information
About MOSIS
Products
Processes
Prices
Support
User Group
Events
Job Openings
News

Work with MOSIS
Overview
Getting Started
Design and Test

Requests
Run Status
Project Status
Test Data

Docs and Forms
Documents
Forms/Agreements
Web Forms

Quick Reference
New Users
Experienced Users
Purchasing Agents
Design and Test
Academic Institutions
Export Program
Submit A Project

Search MOSIS
Search

http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html#tech-codes

MOSIS SCMOS Technology Codes and Layer Maps

SCN4M and SCN4M_SUBM

This is the layer map for the technology codes SCN4M and SCN4M_SUBM using the MOSIS Scalable CMOS layout rules (SCMOS), and only for SCN4M and SCN4M_SUBM. For designs that are laid out using other design rules (or technology codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

SCN4M: Scalable CMOS N-well, 4 metal, 1 poly, silicided. Silicide block and thick oxide option available only on the TSMC process.

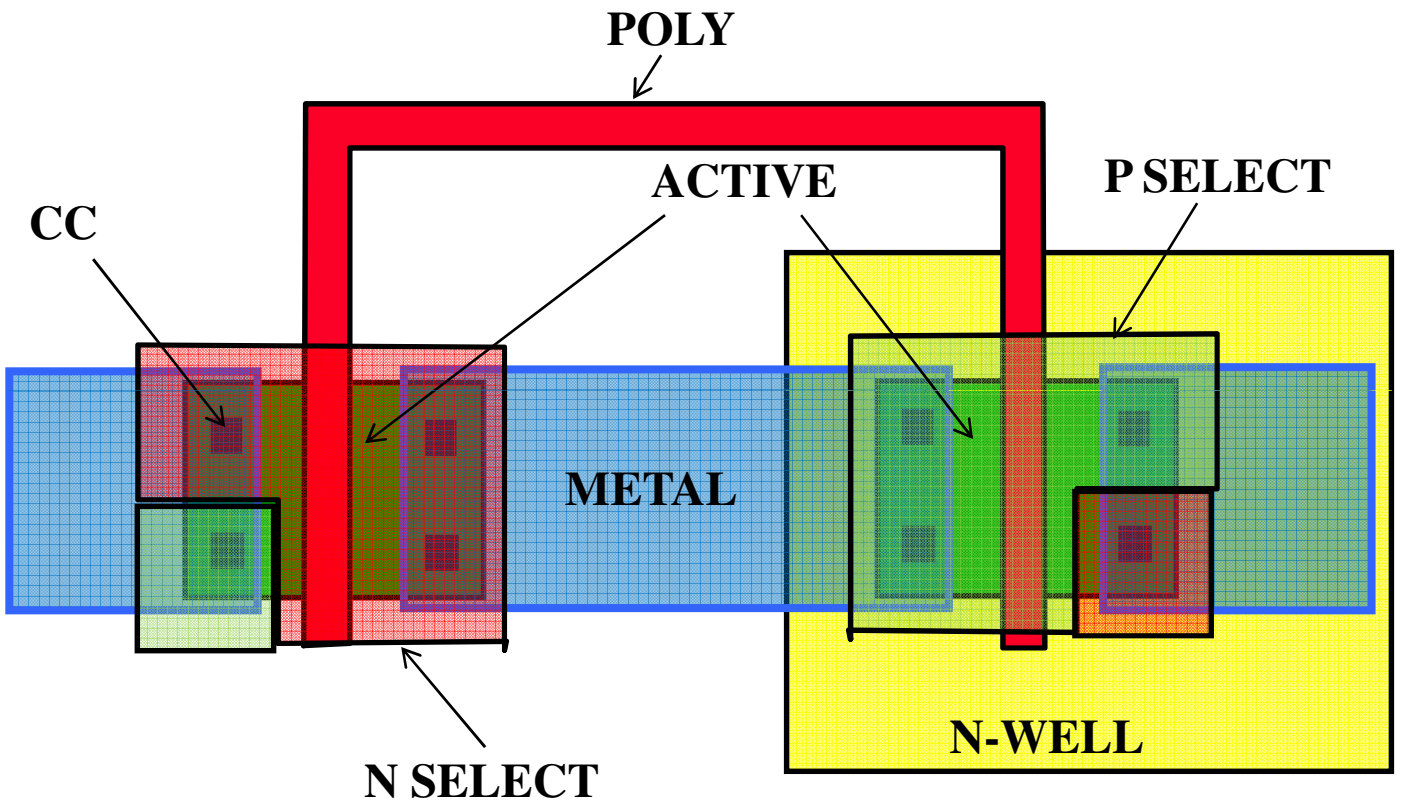
SCN4M_SUBM: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

Fabricated on TSMC, AMIS, and Agilent/HP 0.35 micron process runs. See "Notes" section of layer map for foundry-specific options.

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	
ACTIVE	43	CAA		2	
THICK_ACTIVE	60	CTA		24	Optional for TSMC; not available for Agilent/HP nor AMIS
POLY	46	CPG		3	
SILICIDE_BLOCK	29	CSB		20	Optional for Agilent/HP; not available for AMI
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	
METAL3	62	CM3	CMT	15	
VIA3	30	CV3	CVT	21	
METAL4	31	CM4	CMQ	22	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME

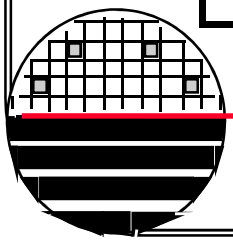
DESIGN LAYOUT OF CMOS INVERTER



7-Design Layers
up to 1st Layer of Metal

MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

MASK LAYER NAME	MENTOR NAME	GDS #	COMMENT
N WELL	N_well.i	42	
ACTIVE	Active.i	43	
POLY	Poly.i	46	
N PLUS	N_plus_select.i	45	
P PLUS	P_plus_select.i	44	
CONTACT	Contact.i	25	Active_contact.i 48 poly_contact.i 47
METAL1	Metal1.i	49	
VIA	Via.i	50	
METAL2	Metal2.i	51	



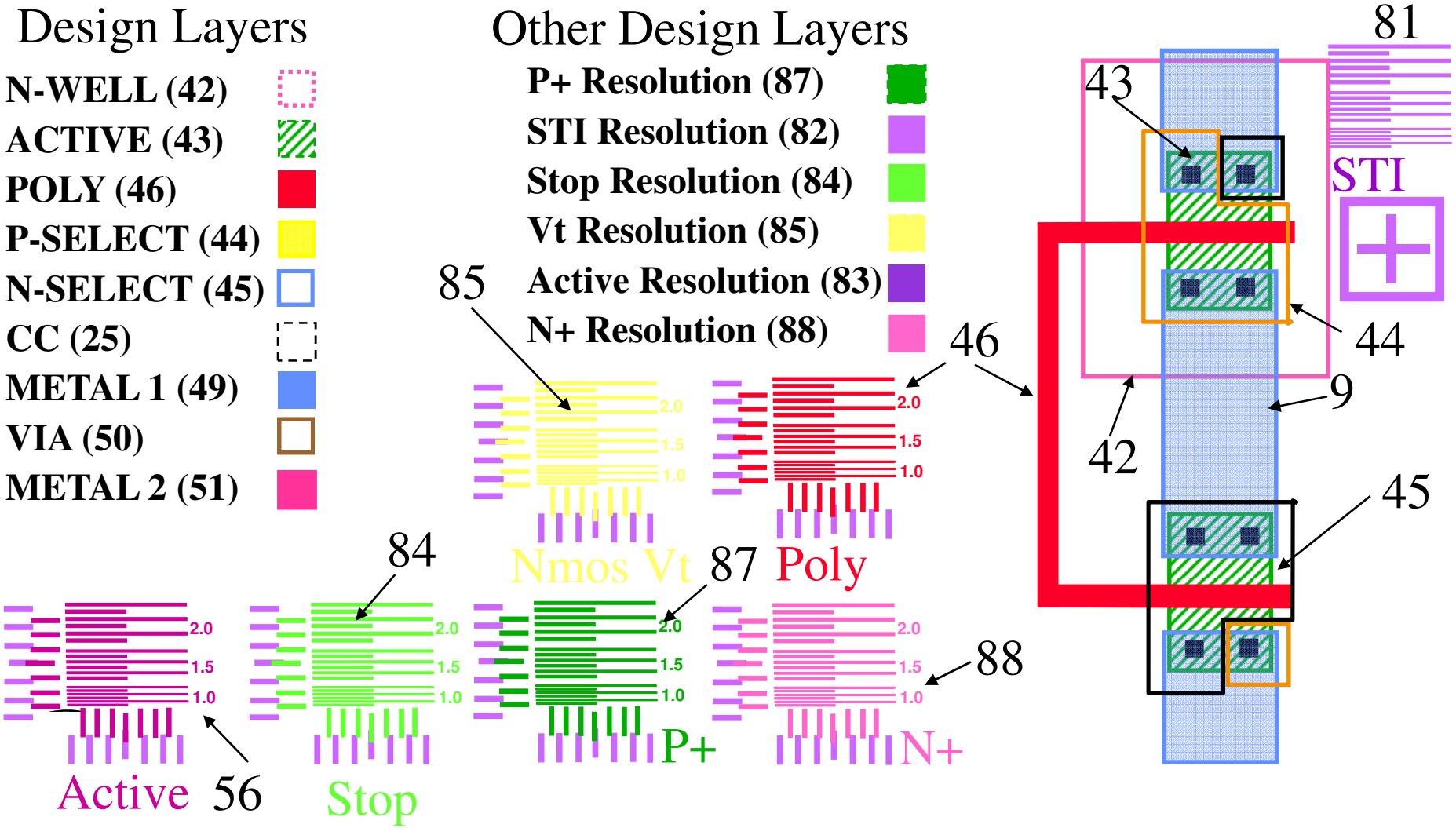
OTHER LAYERS

Design Layers

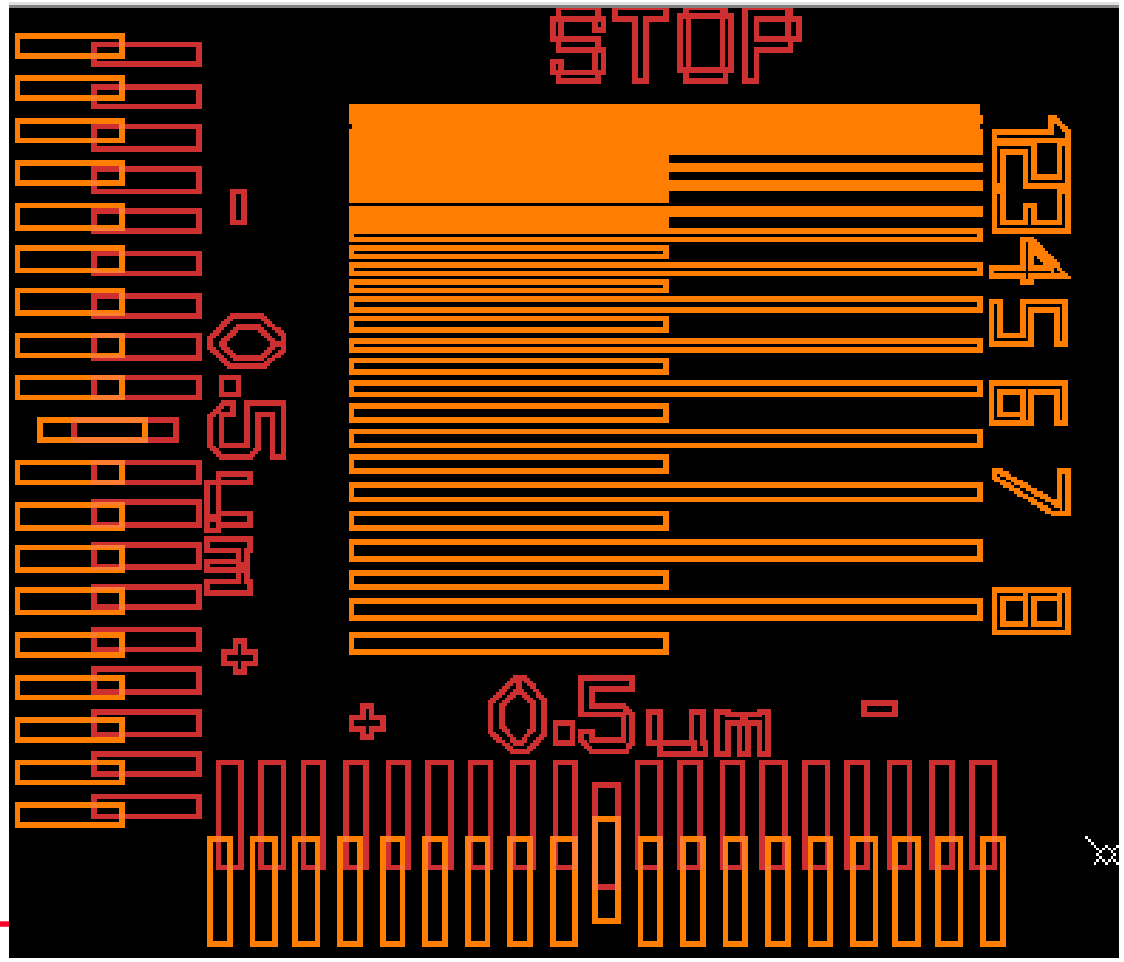
- N-WELL (42)
- ACTIVE (43)
- POLY (46)
- P-SELECT (44)
- N-SELECT (45)
- CC (25)
- METAL 1 (49)
- VIA (50)
- METAL 2 (51)

Other Design Layers

- P+ Resolution (87)
- STI Resolution (82)
- Stop Resolution (84)
- Vt Resolution (85)
- Active Resolution (83)
- N+ Resolution (88)

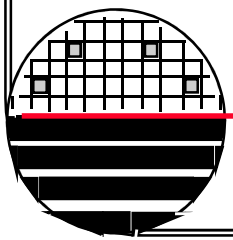


0.5 µm RESOLUTION AND OVERLAY DESIGN

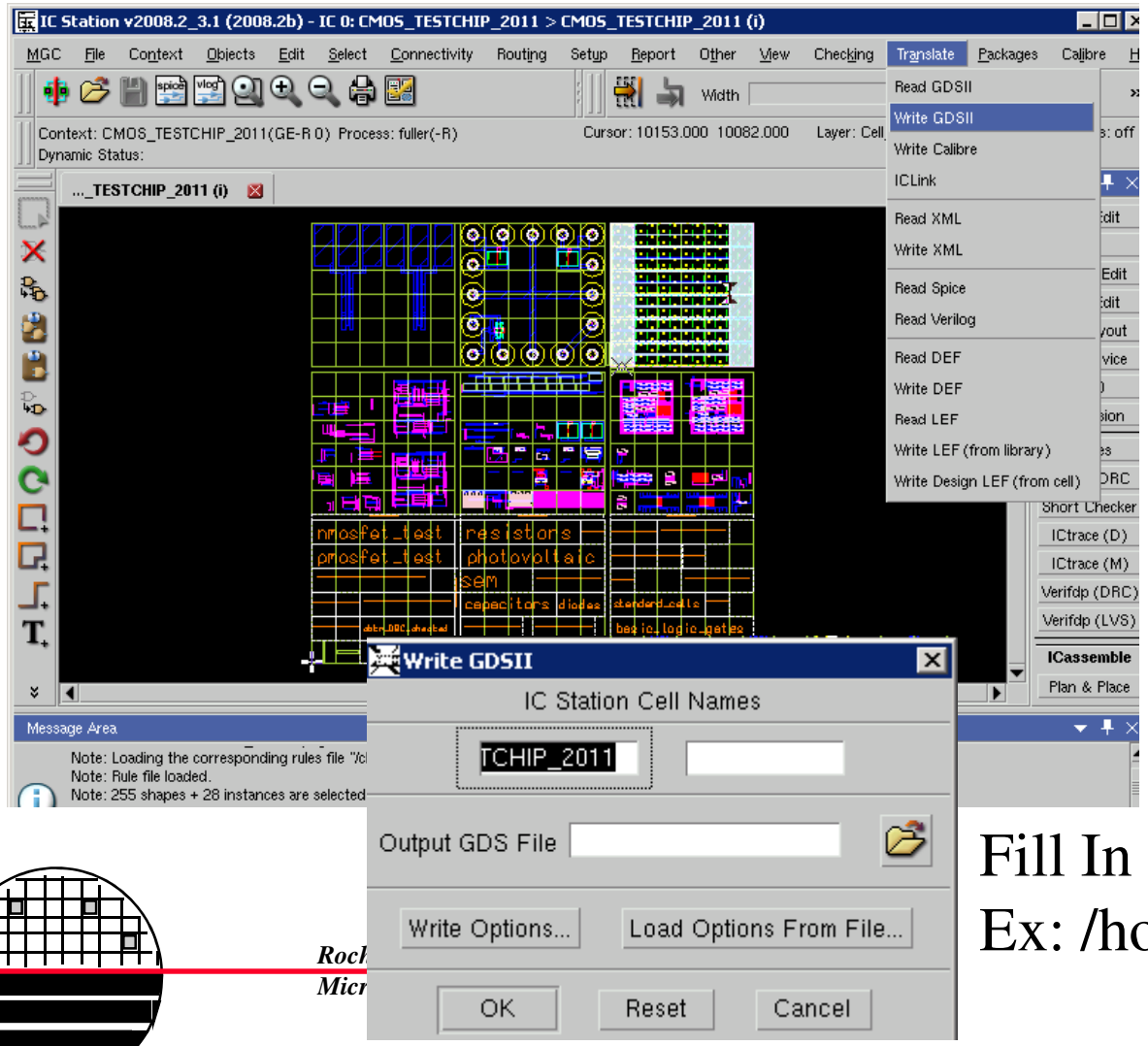


MORE LAYERS USED IN MASK MAKING

LAYER	NAME	GDS	COMMENT
	cell_outline.i	70	Not used
	alignment	81	Placed on first level mask
	nw_res	82	Placed on nwell level mask
	active_lettering	83	Placed on active mask
	channel_stop	84	Overlay/Resolution for Stop Mask
	pmos_vt	85	Overlay/Resolution for Vt Mask
	LDD	86	Overlay/Resolution for LDD Masks
	p plus	87	Overlay/Resolution for P+ Mask
	n plus	88	Overlay/Resolution for N+ Mask



CREATE GDS II FILE



Select:
Translate
WriteGDSII

Fill In Output path and filename
Ex: /home/lffeee/mychip.gds

CONVERSION FROM .ICCEL TO .GDS FORMAT

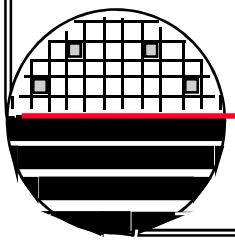
GENERATION OF GDS FILE IN MENTOR GRAPHICS SYSTEM:

1. Type: pwd for design pathname and record:
   example: **/home/sxs8853/senior**
2. Type: **iclink -co -so -i /pathname/designname -d -g filename.gds**

note: design name and filename can be the same.

3. Obtain individual plots for each mask level, label them, and attach to the order form.
4. Copy .gds file to dropbox for maskmaking at RIT
   cp <design name>.gds /dropbox/masks
5. Set protection on file so the file can be accessed

/usr/bin/chmod 644 /dropbox/masks/<design name>.gds



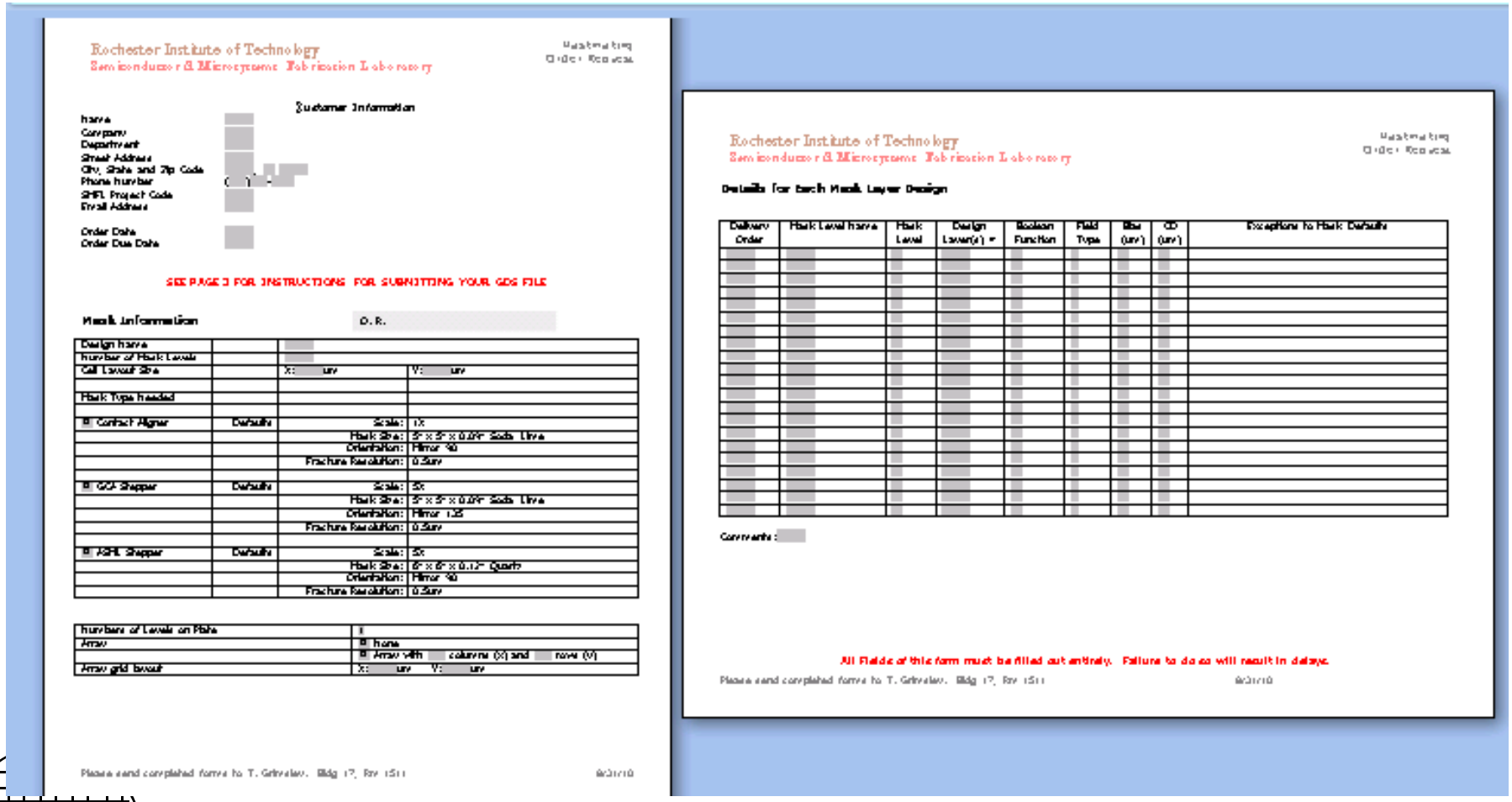
MASK PROCUREMENT

Design Layers: There may be many design layers in a design. For example the well layer and the lettering for the well layer may be on different design layers but merged to make the well mask. Resolution and overlay designs may be on different layers to be merged with other layers to make a mask. Boolean combinations are defined for the merge as well as other transformations such as bloat, rotate, and mirror. As a result this information needs to be made available to the mask provider as part of the mask order.

Clear field and Dark field describe the general appearance of the mask which is important in determining the layers in the streets between die.

Dummy features are sometimes added to a layer (tiling) such as shallow trench mask to improve performance of subsequent processes, such as CMP in the case of shallow trench.

MASK ORDER FORM



Rochester Institute of Technology
Semiconductor & Microsystems Fabrication Laboratory

Maskmaking
Order Request

Customer Information

Name
Company
Department
Street Address
City, State and Zip Code
Phone Number
SMFL Project Code
Email Address

Order Date
Order Due Date

SEE PAGE 3 FOR INSTRUCTIONS FOR SUBMITTING YOUR GDS FILE

Mask Information — O.R.

Design Name			
Number of Mask Levels			
Cell Layout Size		X: um	Y: um
Mask Type Needed			
☐ Contact Aligner	Default	Scale:	1X
		Mask Size:	5" x 5" x 0.09" Soda Lime
		Orientation:	Mirror X
		Fracture Resolution:	0.5um
☐ GCA Stepper	Default	Scale:	5X
		Mask Size:	5" x 5" x 0.09" Soda Lime
		Orientation:	Mirror Y
		Fracture Resolution:	0.5um
☐ ASML Stepper	Default	Scale:	5X
		Mask Size:	6" x 6" x 0.17" Quartz
		Orientation:	Mirror X
		Fracture Resolution:	0.5um

Number of Levels on Plate	1
Array	☐ None
	☐ Array with columns (X) and rows (Y)
Array grid layout	X: um Y: um

Please send completed forms to T. Grimsley, Bldg 17, Rm 1511 6/21/10

Rochester Institute of Technology
Semiconductor & Microsystems Fabrication Laboratory

Maskmaking
Order Request

Details for each Mask Layer Design

Delivery Order	Mask Level Name	Mask Level	Design Layer(s) #	Boolean Function	Field Type	Bias (um)	CD (um)	Exceptions to Mask Defaults

Comments:

All Fields of this form must be filled out entirely. Failure to do so will result in delays.

Please send completed forms to T. Grimsley, Bldg 17, Rm 1511 6/21/10

http://www.smfl.rit.edu/forms/Order_Request.dot

MASK ORDER FORM

Mask Information O. R.

Design Name			
Number of Mask Levels			
Cell Layout Size		X: um	Y: um
Mask Type Needed			
☐ Contact Aligner	Defaults	Scale:	1X
		Mask Size:	5" x 5" x 0.09" Soda Lime
		Orientation:	Mirror 90
		Fracture Resolution:	0.5um
☐ GCA Stepper	Defaults	Scale:	5X
		Mask Size:	5" x 5" x 0.09" Soda Lime
		Orientation:	Mirror 135
		Fracture Resolution:	0.5um
☐ ASML Stepper	Defaults	Scale:	5X
		Mask Size:	6" x 6" x 0.12" Quartz
		Orientation:	Mirror 90
		Fracture Resolution:	0.5um

http://www.smfl.rit.edu/forms/Order_Request.dot

Numbers of Levels on Plate	1
Array	☐ None
	☐ Array with columns (x) and rows (y)
Array grid layout	X: um Y: um

MASK ORDER WORKSHEET

Rochester Institute of Technology
Microelectronic Engineering

Date 12/3/2007
Requestor Dr. Lynn Fuller

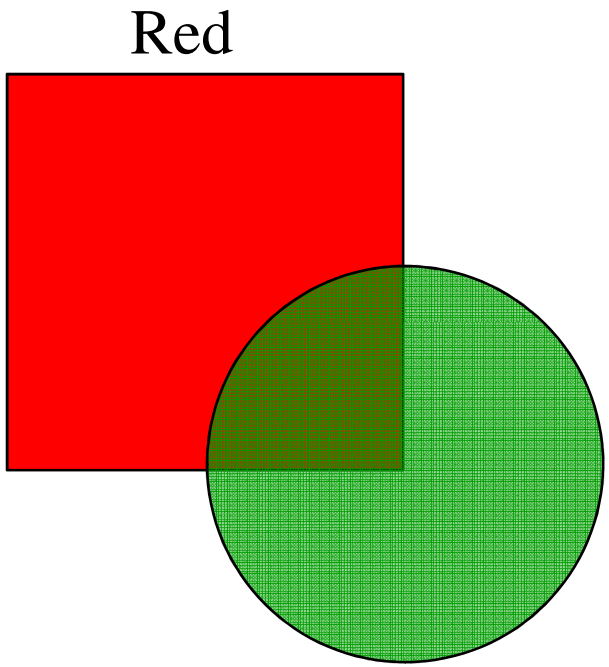
Attachment for Mask Order Form

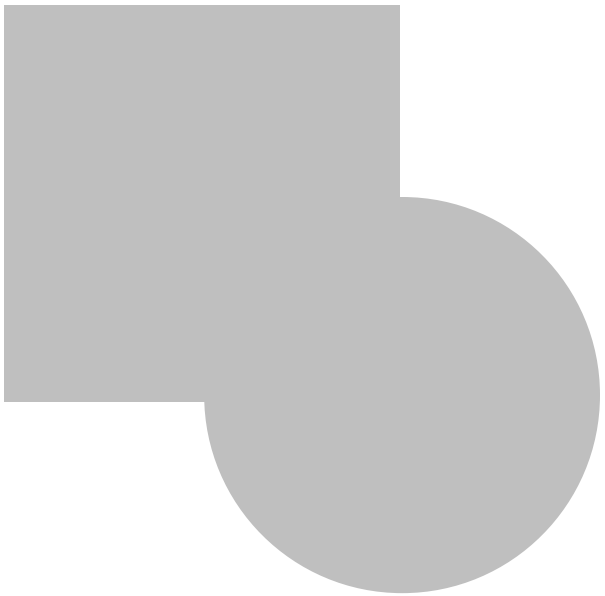
Design Description: Sub-CMOS Mixed Analog Digital Test Chip **gds File:** /home/ume/subcmos_040203.gds

Fracture Resolution	0.5	**Mirror**	135	**Plate Size**	5"x5"x0.090"
Scale Factor	5X	**Rotate**	none	**# of levels/plate**	1
Array	none				

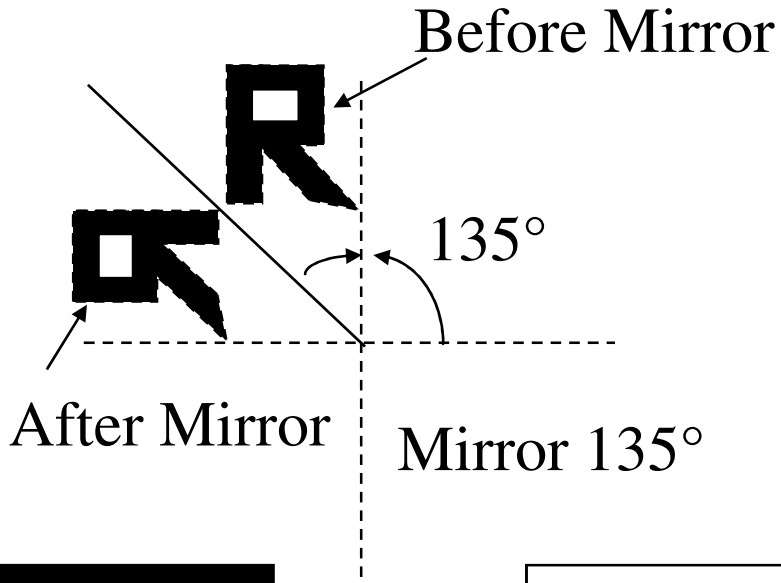
Design Layer Name	Number	Mask Level Name	Number	Boolean Function	Comments
NWELL	1	n-well.i	42	(42 OR 81 OR 82) INVERT	Dark Field Mask
		alignment	81		
		nw_res	82		
ACTIVE	2	active-area.i	43	(43 OR 83)	Clear Field Mask
		active-area.e	83		
STOP	3	n-well.i	42	(42 OR 84)	Clear Field Mask
		channel_stop	84		
PMOSVT	4	p_plus_select.i	44	(44 OR 85)	Clear Field Mask
		pmos_vt	85		
POLY	5	poly.i	46	none	Clear Field Mask, Bias layer 6 +0.5 µm
LDD-N	6	n_plus_select.i	45	(45 OR 86) INVERT	Dark Field Mask
		LDD	86		
LDD-P	7	p_plus_select.i	44	(44 OR 86) INVERT	Dark Field Mask
		LDD	86		
N+DS	8	n_plus_select.i	45	(45 OR 88) INVERT	Dark Field Mask
		n plus	88		
P+DS	9	p_plus_select.i	44	(44 OR 87) INVERT	Dark Field Mask
		p plus	87		
CC	10	contact	25	(25 OR 87 OR 47) INVERT	Dark Field Mask
		Active_contact.i	48		

BOOLEAN COMBINATIONS



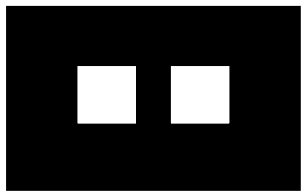


DATA PREP USING CATS

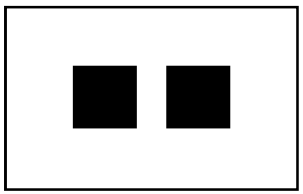


Input File: GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

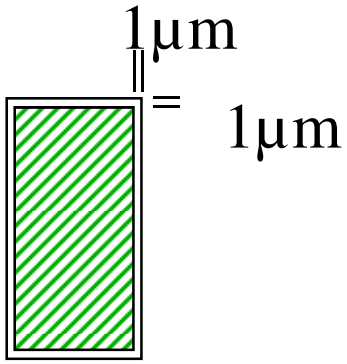
Output File: MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only



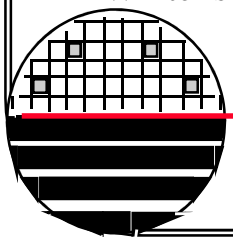
Dark Field: Black is chrome, White is Quartz.



Light Field: Black is chrome, White is Quartz.

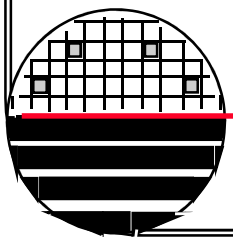


BIAS +1µm



SAVE IN MEBES FORMAT

MEBES format - files for electron beam maskmaking tool,
each file one layer
trapezoids only



CREATE A MEBES JOB DECK

SLICE EDIT, 14

14 means 5” by 5” glass

OPTICON AA=0.5, BA=0.5, PA, SA=40, VA=10

AA means address all levels = 0.5 µm

BA means beam size all levels = 0.5 µm

PA means all levels positive resist

SA means all levels spot current 40 nA

VA means all levels acceleration = 10KV

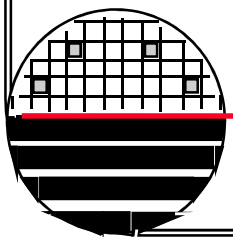
MTITLE 1, ADV-CMOS STI
DTITLE A, RIT EMCR650
ITITLE A, BARCODE
ORIENT A, ITITLE, TITLEROT=90, LOC=

CHIP1, (1,cmostestchip-LVL-01, RC=15),

first level of cmostestchip maskset

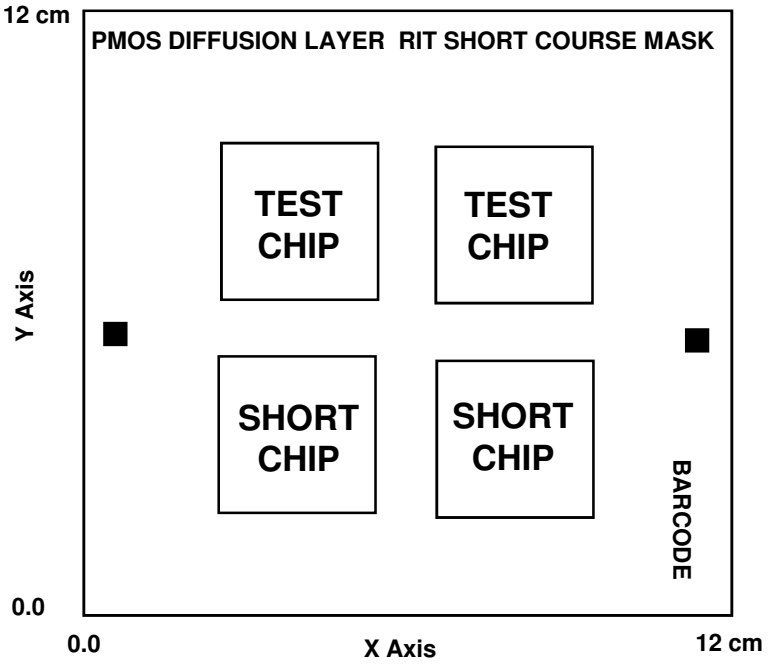
END

```
SLICE EDIT,14
OPTION AA=0.5, BA=0.5, PA, SA=250, VA=10
REPEAT A, 10
STITLE A, 10000, 10000, MEBES III SN @S
MTITLE 1,  NWELL
MTITLE 2,  ACTIVE
MTITLE 3,  STOP
MTITLE 4,  PMOS VT
MTITLE 5,  POLY
MTITLE 6,  LDD N
MTITLE 7,  LDD P
MTITLE 8,  N DS
MTITLE 9,  P DS
MTITLE 10,  CONTACT
MTITLE 11,  METAL
DTITLE A,  SUBMICRON CMOS
CHIP 1,(A,RITLOGO-50-01)
ROWS 10000/63500
CHIP 2,(A,FIDUCIA-LS-01)
ROWS 63500/63500
CHIP 3,
$ (1R,EMCR650-01-01),
$ (2,EMCR650-01-02),
$ (3,EMCR650-01-03),
$ (4,EMCR650-01-04),
$ (5,EMCR650-01-05),
$ (6,EMCR650-01-06),
$ (7,EMCR650-01-07),
$ (8,EMCR650-01-08),
$ (9,EMCR650-01-09),
$ (10,EMCR650-01-10),
$ (11,EMCR650-01-11)
ROWS 63500/63500
END
```



EXAMPLE OF A MEBES PLOT JOB

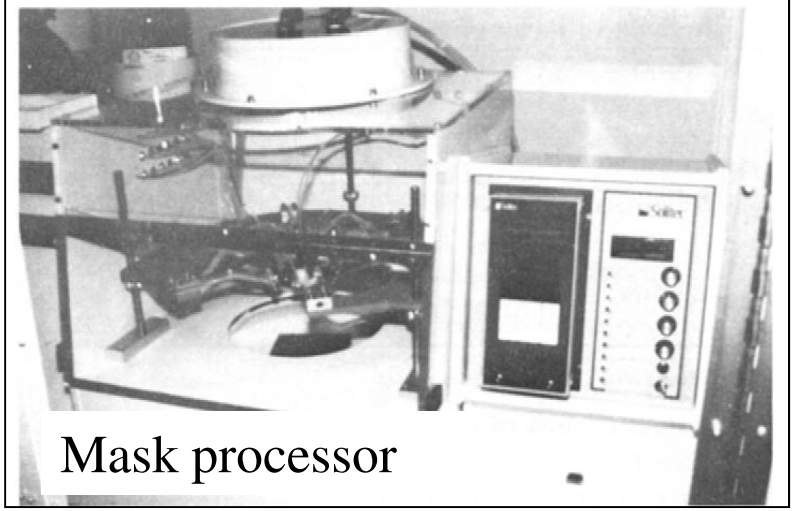
2/25/93 9:12:23 MEBES 967
REV, 4.6
SPECIFICATION FILE: JOB:SHORT.JB
DTITLE: RIT SHORT COURSE MASK
ITITLE: BARCODE
MTITLE: PMOS DIFFUSION LAYER
CASSETTE TYPE ID:14
LEVEL PLOTTED: 1
JOB SCALE: 1
JOB SCALE: 1.000000
ADDRESSING: 0.500000 MICRONS
PLOT SCALE: 1.00 TO 1 CM



ID	PATTERN	X DIMENSION	Y DIMENSION	PLACEMENT	ORIENTATION	TONE
1.	SHORTLVL.01	20000.00	20000.00	UNMIRROR	UNMIRROR	NORMAL
2.	TESTLVL.01	20000.00	20000.00	UNMIRROR	UNMIRROR	NORMAL
3.	GCA6700F1.05	2000.00	2000.00	UNMIRROR	UNMIRROR	NORMAL

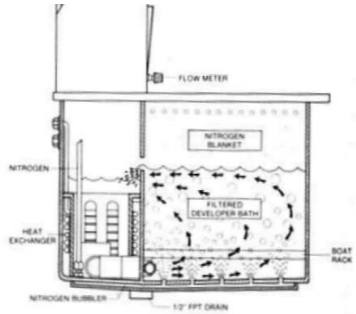
MASK PROCESSING AT RIT

1. Coat resist (if not precoated blank).
•I-line resist, DNQ/Novolac chemistry,
OCG895i 2.5 CS
2. Exposure - optical or ebeam
3. Develop in Solitec, APT or immersion.
•Sodium Hydroxide based, Shipley MF 351 Concentrate, DI:Mf 351 (4:1)
4. Rinse/Spin dry.
5. Etch in spray or immersion system: Chrome etch: cerric ammonium nitrate(CR-4,Cyantek Corp.)+ nitric acid, perchloric acid, acetic acid, cerric sulfate, etc.
6. Rinse
7. Strip resist in solvent : Sulfuric Acid+Hydrogen Peroxide(Nanostrip, Cyantek Corp.),NMP, Acetone or acid: Caro's acid, sulfuric acid.
9. Clean in: detergent (CA40) acid/base (Ammonium hydroxide).

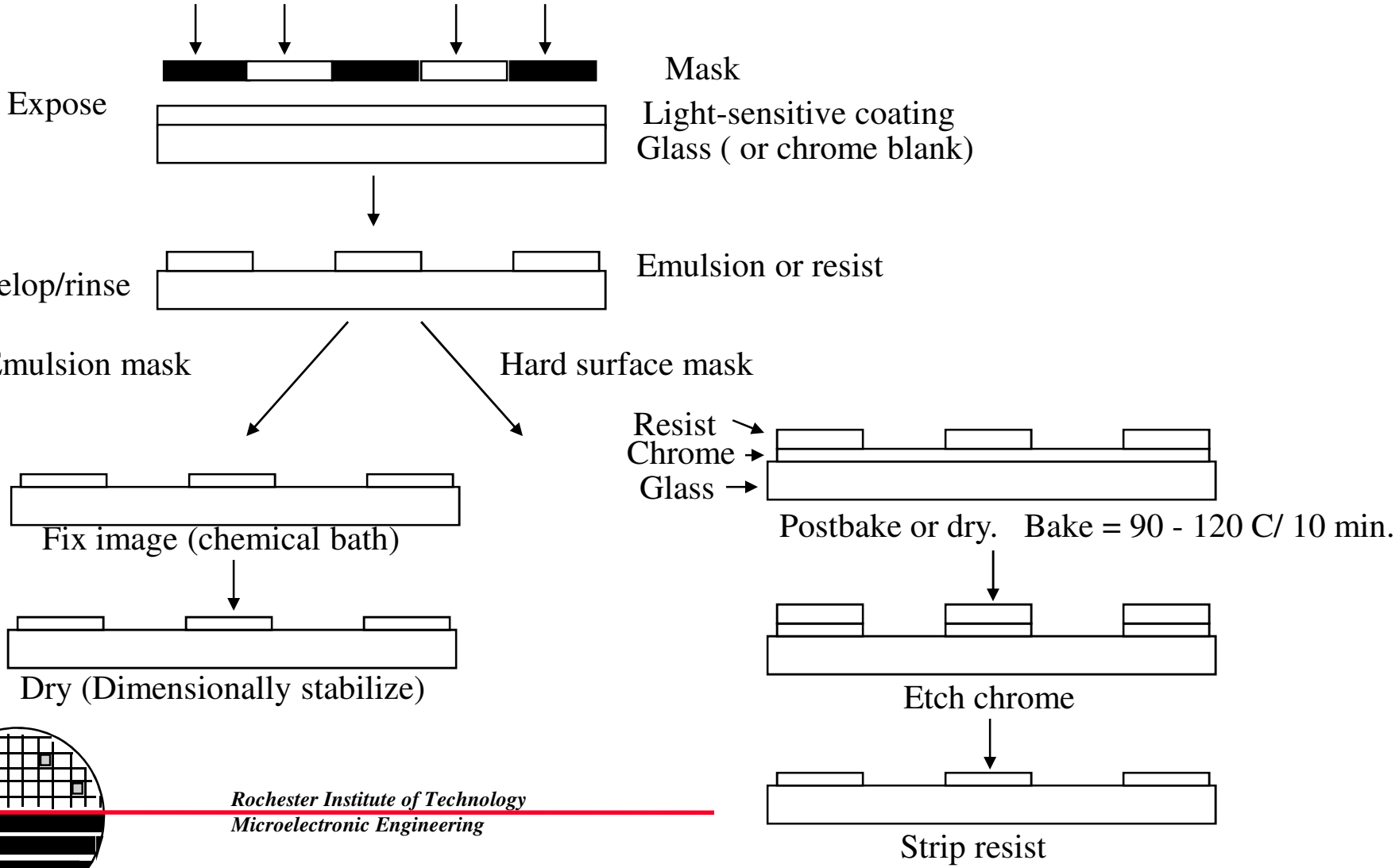


Mask processor

Wet immersion bath

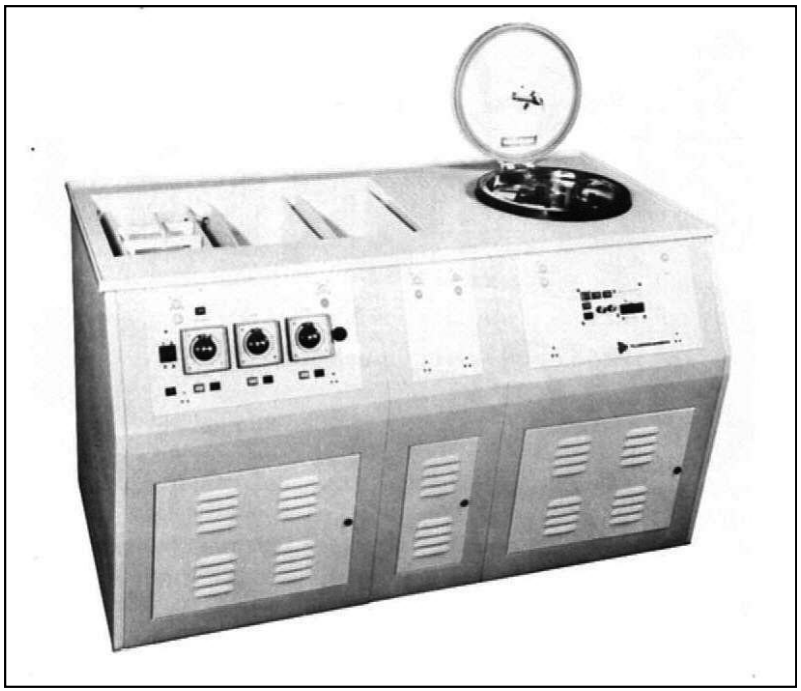


MASK CROSS SECTION

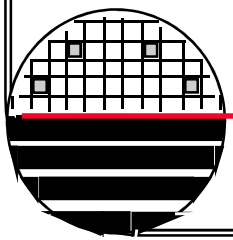


MASK ETCHING

- Wet etch used predominantly.
- Spray or immersion methods.
- Dry etch in plasma systems was limited until 1990s.
- Plasma etchers may have been employed in descum operations (oxygen only).



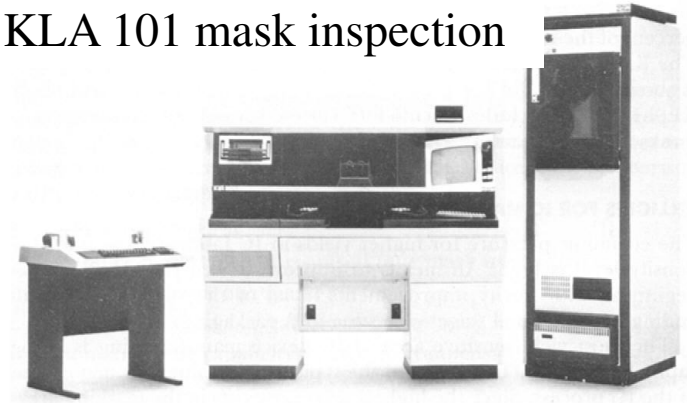
Automated spray etcher

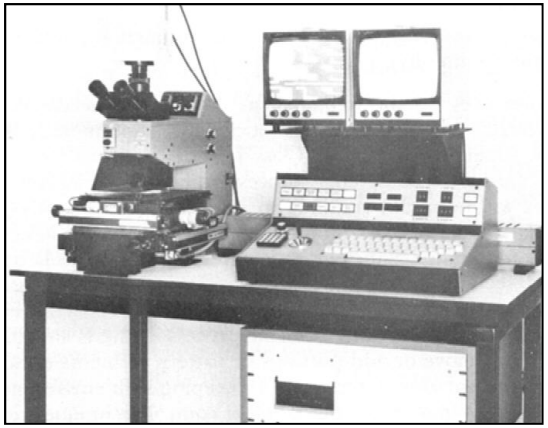


MASK INSPECTION AND REPAIR

- Mask inspection done with KLA optical defect comparison tools.
- Mask repair with Cr or Mo deposition for clear defects and laser removal for dark defects.
- Exposure to chemicals is minimal.

KLA 101 mask inspection



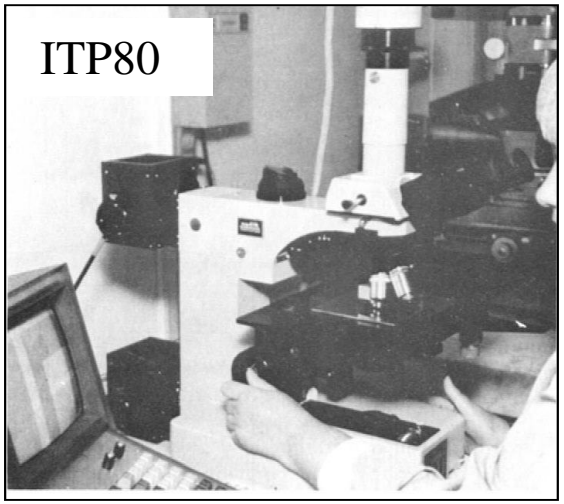


Laser opaque defect repair

MASK LINEWIDTH MEASUREMENT

Mask linewidth measurement performed by several methods:

- Nikon 2i - laser scanning of edges
- ITP TV scanning system
- Vickers image shearing system
- Confocal microscopy
- SEM methods

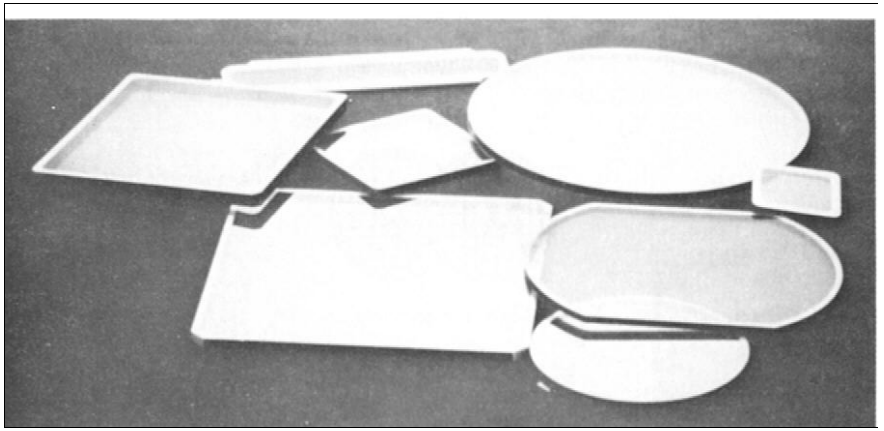



Nikon 2i

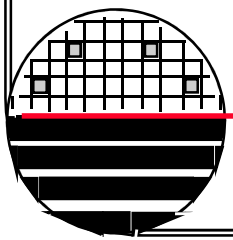
MASK PELLICLE OPERATIONS

- A pellicle is a protective mylar or nitrocellulose membrane mounted on a frame placed several mm from the mask surface.

- Pellicle operations included mounting (adhesive) and removal. Pellicle materials are commercial items and not made in a mask shop.



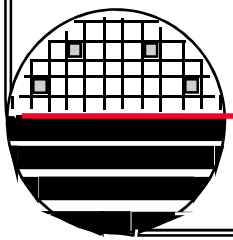
Several pellicle types and sizes



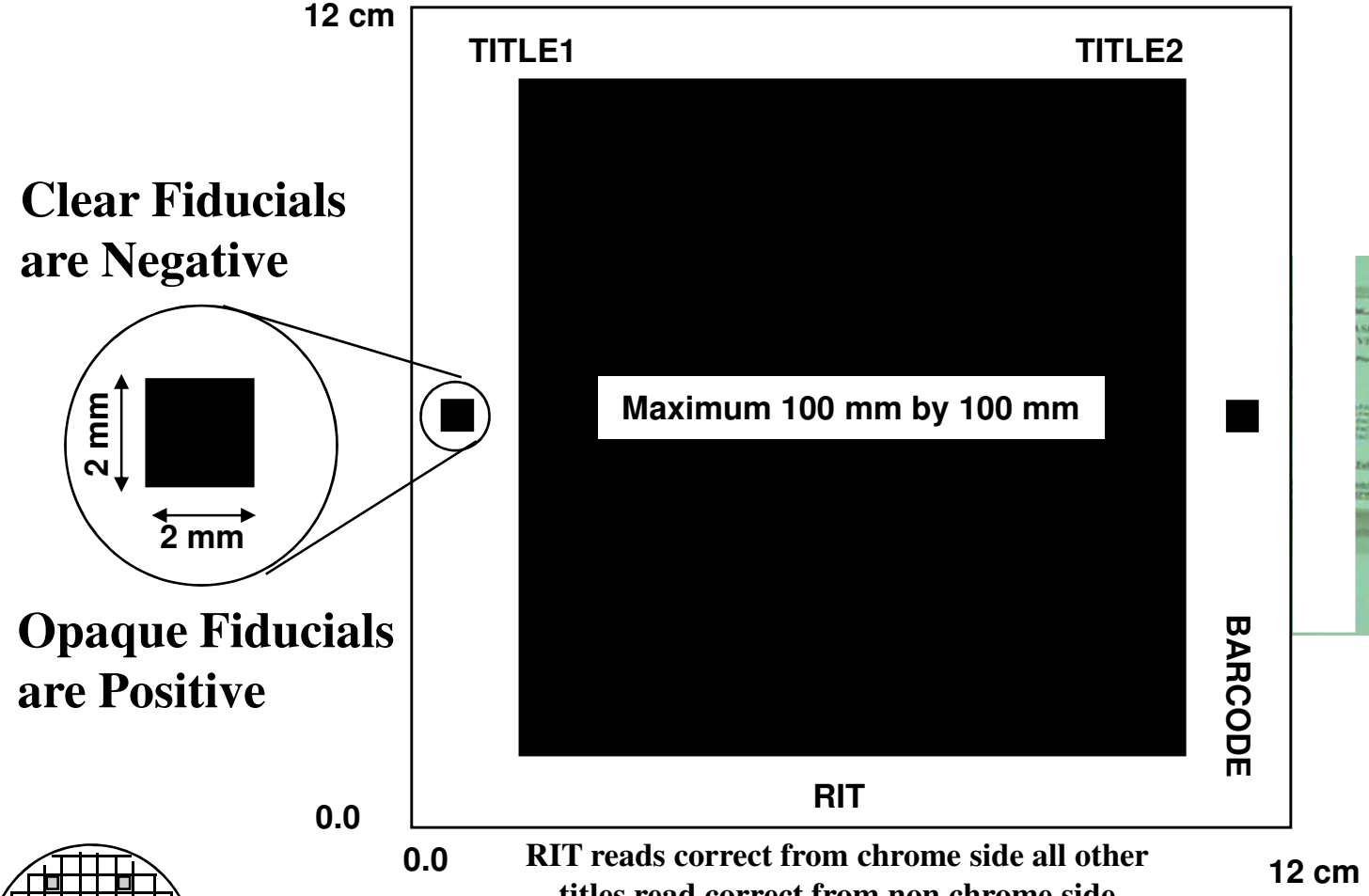
STEPPER AND CMOS PROCESS CHOICES

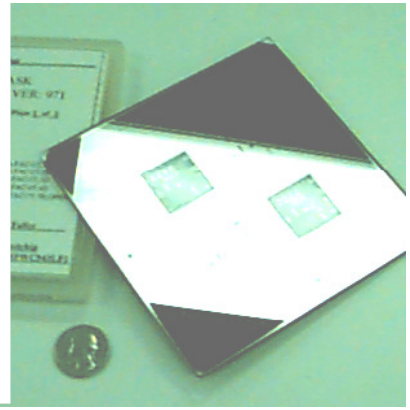
Different steppers have different fiducial marks that need to be added to the mask

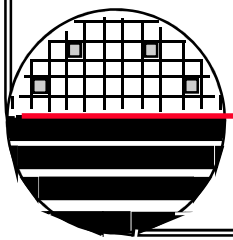
Different CMOS processes use masks differently to achieve the desired result. For example the channel stop mask is very different for p-well, SMFL-CMOS and Sub-CMOS processes as shown in the following pages.



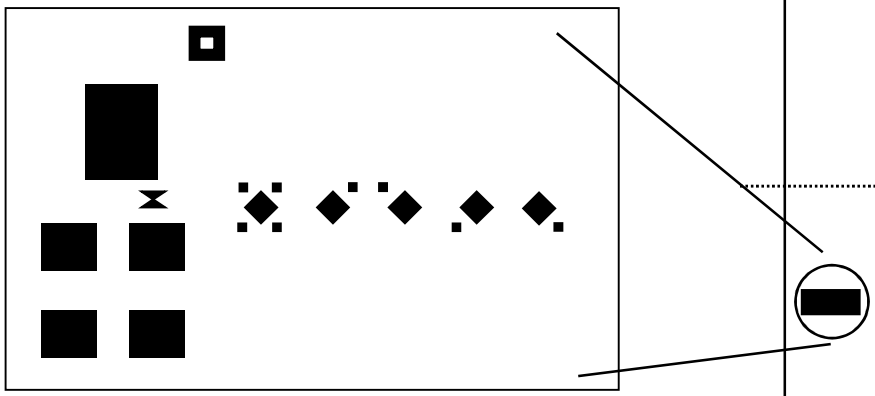
GCA RETICLE



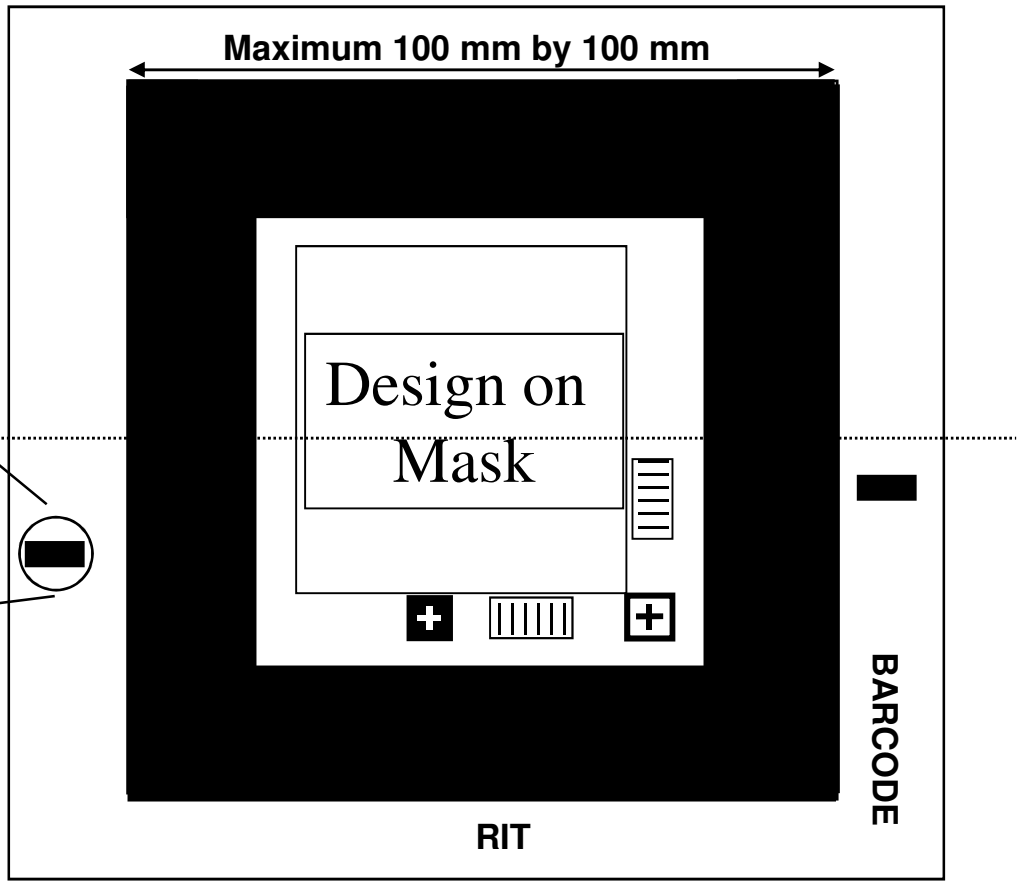




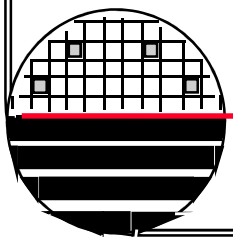
CANON RETICLE FIDUCIAL MARKS



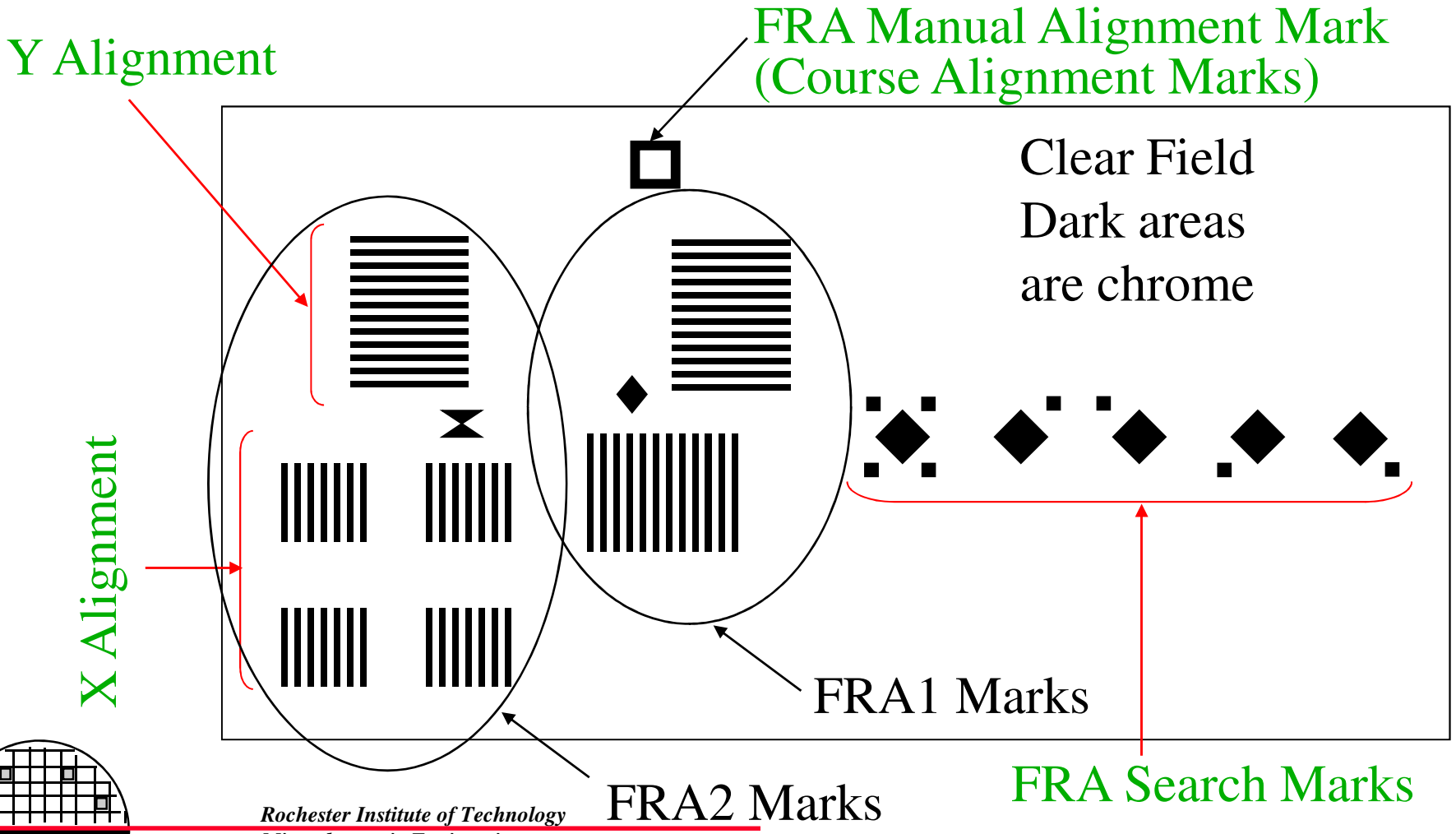
Opaque Fiducials
marks in clear field



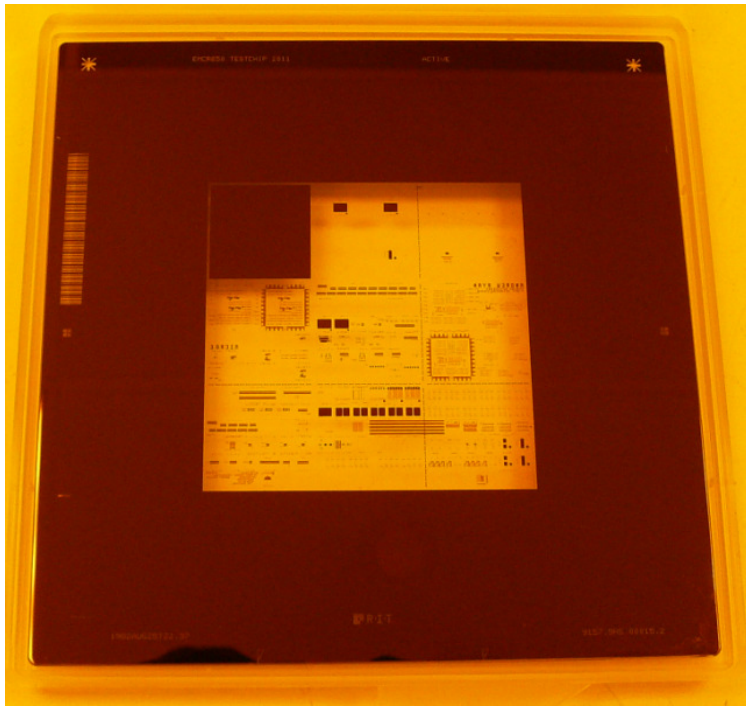
RIT reads correct from chrome side all other titles read correct from non chrome side



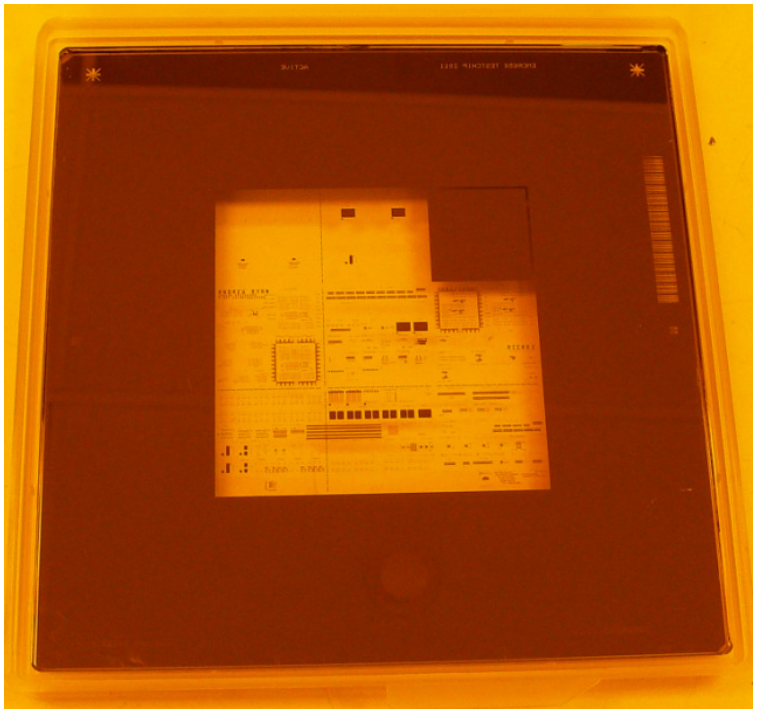
CANON FINE RETICAL ALIGNMENT (FRA) MARKS



ASML RETICLE

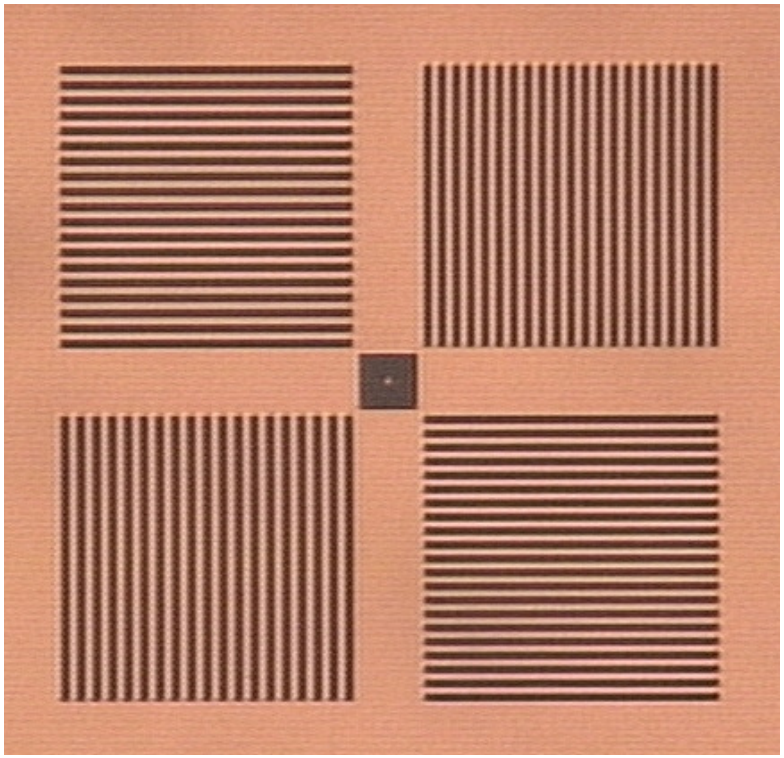


Chrome Side
Mirrored 90°
Chip Bottom at Bottom

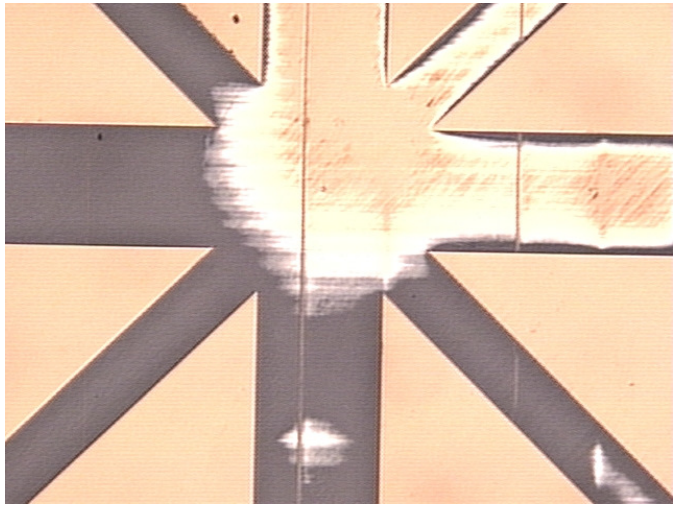


Non Chrome Side
As loaded into Reticle Pod,
Chrome Down, Reticle Pre-Alignment Stars Sticking out of Pod

ASML FIDUCIAL AND PRE ALIGNMENT MARKS

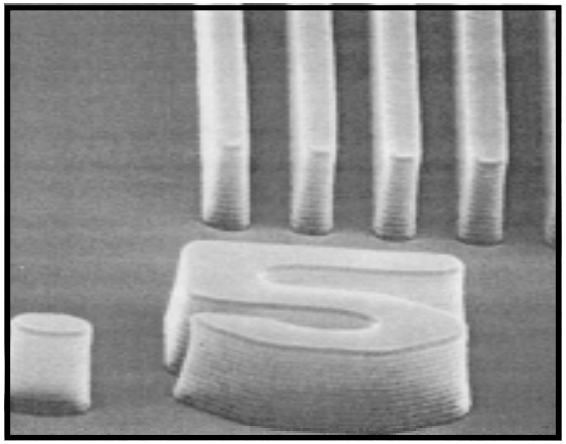


Fiducial Mark

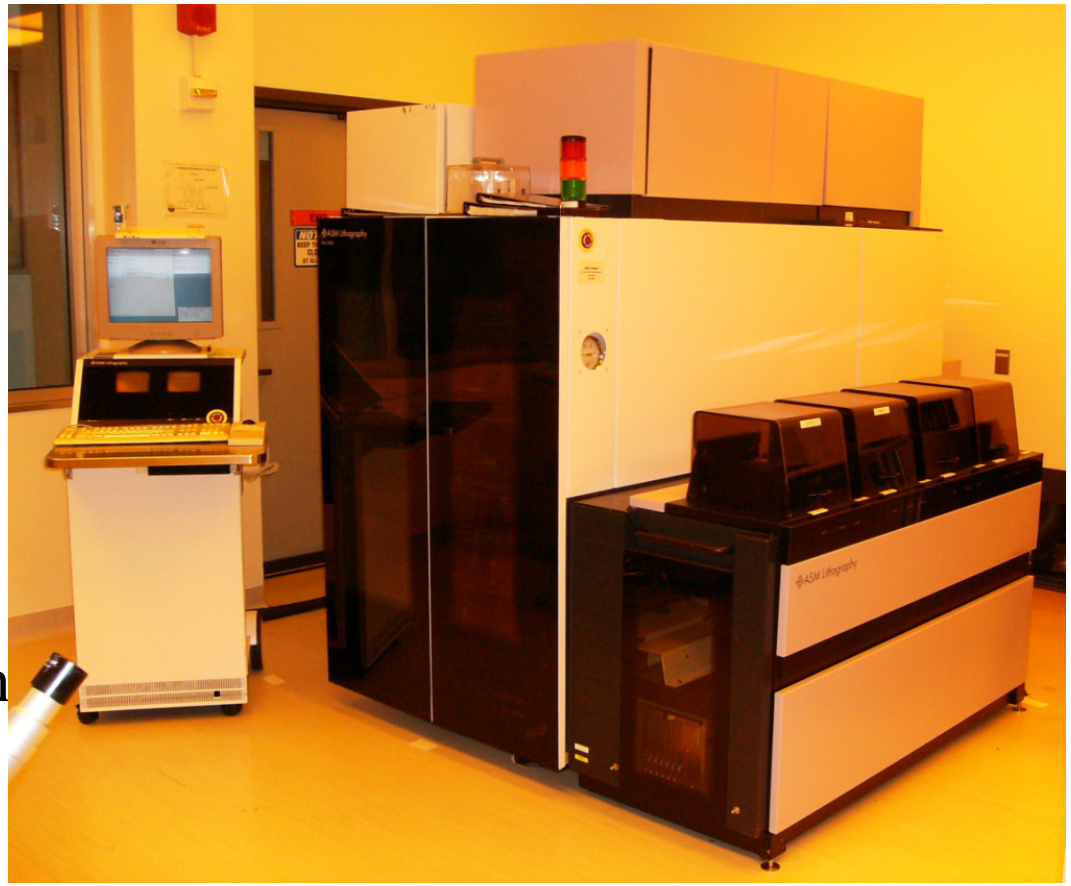


Prealignment Mark

ASML 5500/200



NA = 0.48 to 0.60 variable
σ= 0.35 to 0.85 variable
With Variable Kohler, or
Variable Annular illumination
Resolution = K1 λ/NA
= ~ 0.35μm
for NA=0.6, σ =0.85
Depth of Focus = k_2 λ/(NA)^2
= > 1.0 μm for NA = 0.6



i-Line Stepper λ = 365 nm
22 x 27 mm Field Size

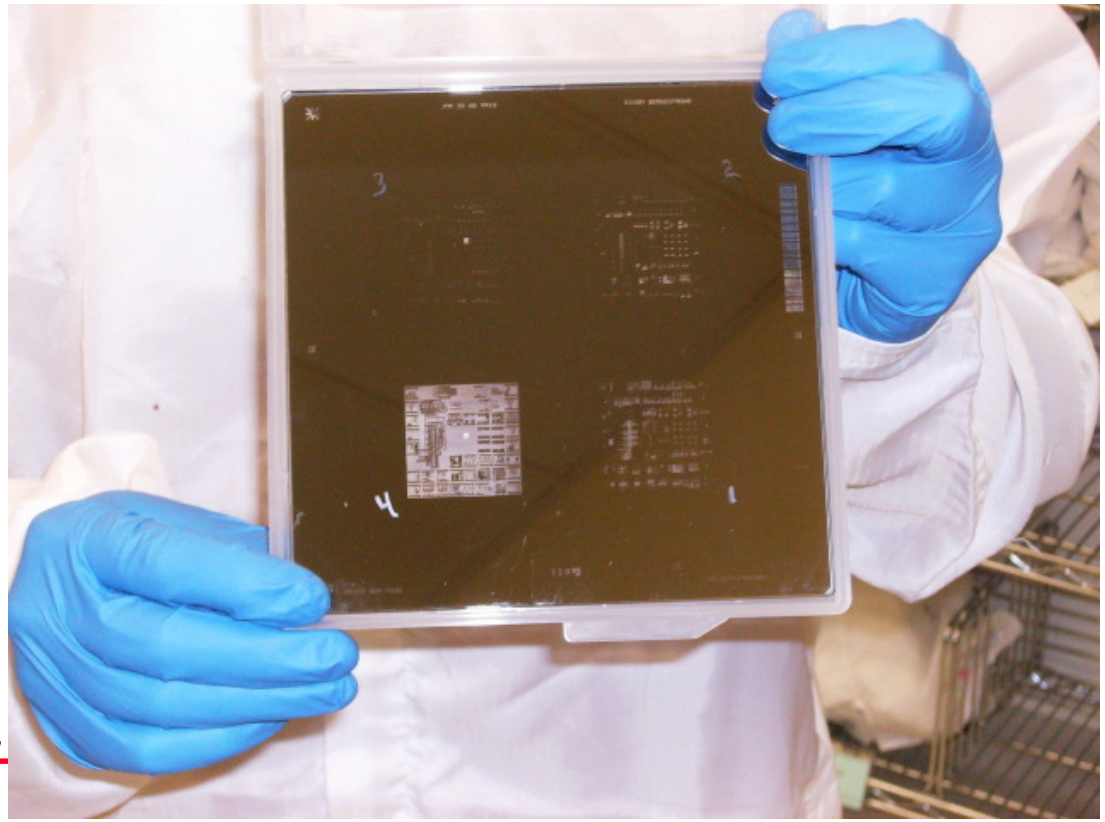
ASML RETICLE 4 LEVELS PER MASK

Masks with 4 levels

Saves money, time, inventory

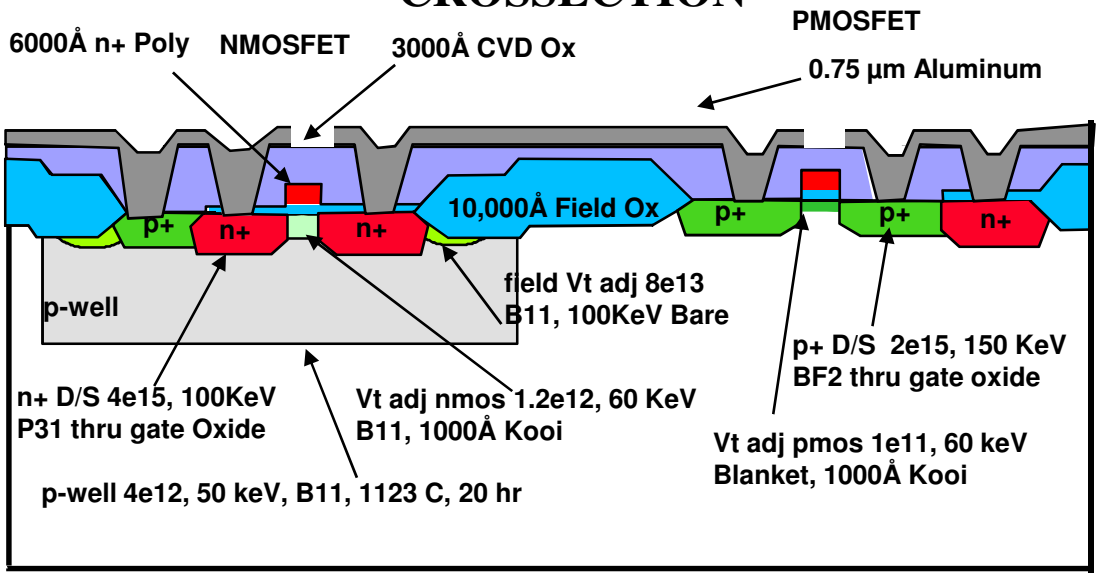
Chip size 10mm by 10mm

Stepper Job Name = PMOS



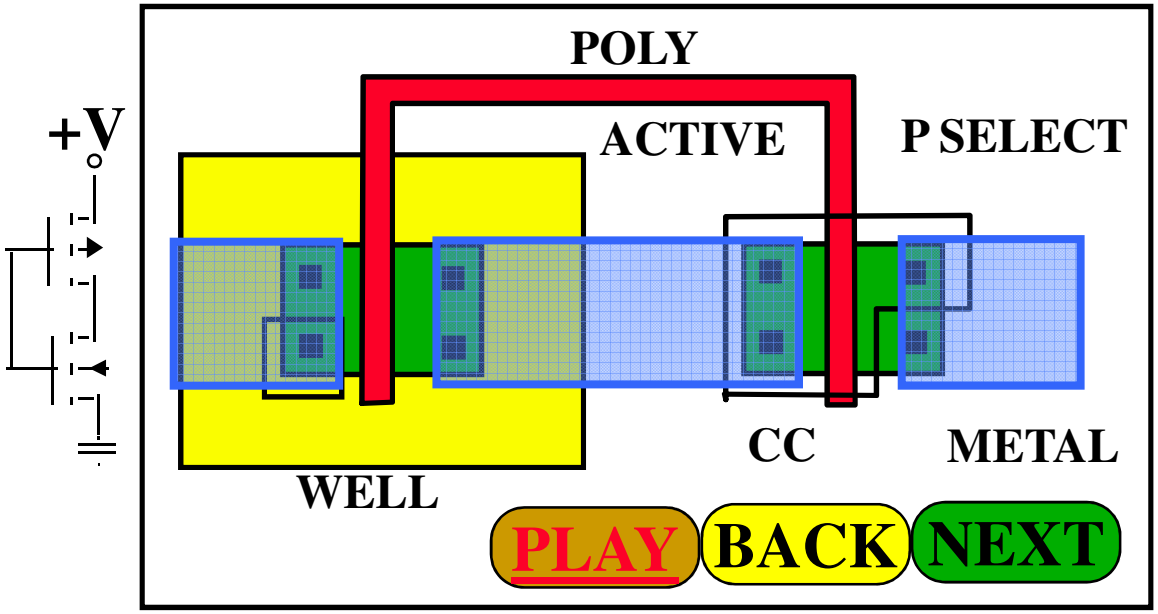
RIT P-WELL CMOS PROCESS

CROSSECTION

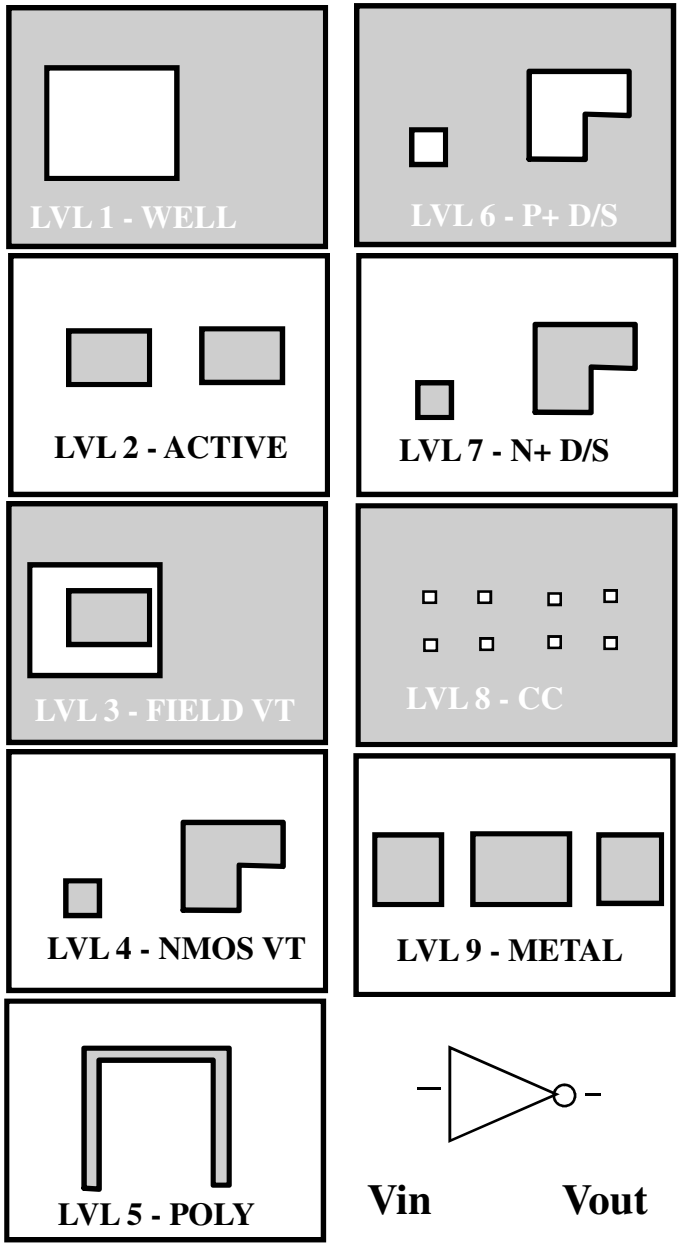


n-type substrate 10 ohm-cm (100)

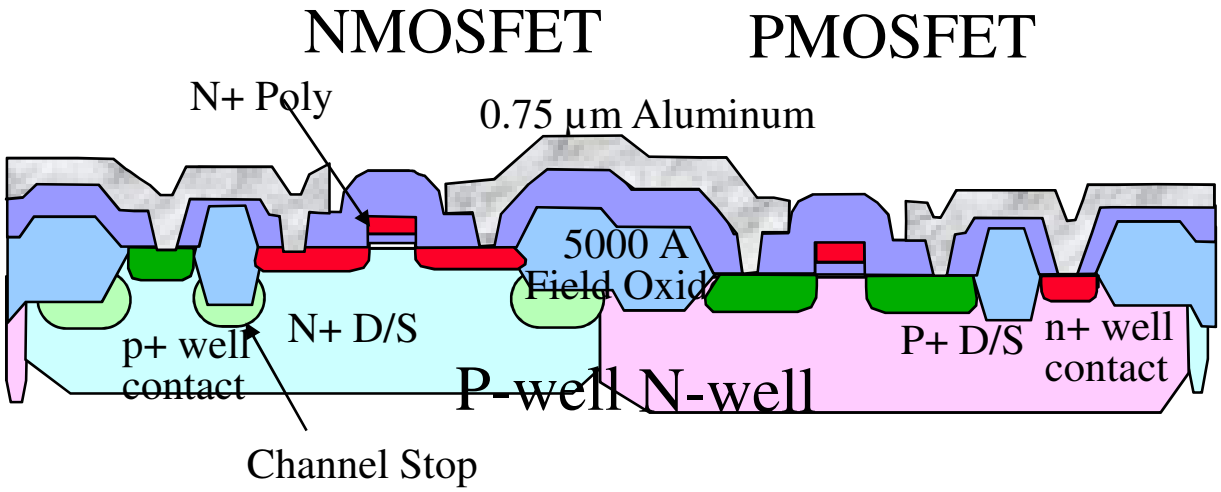
SIX LAYOUT LEVELS

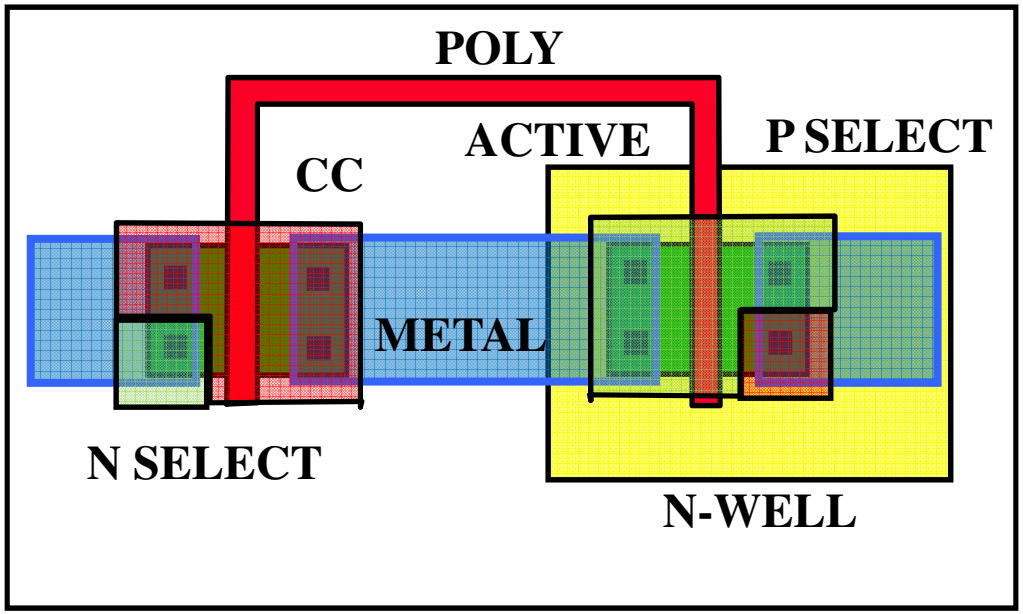


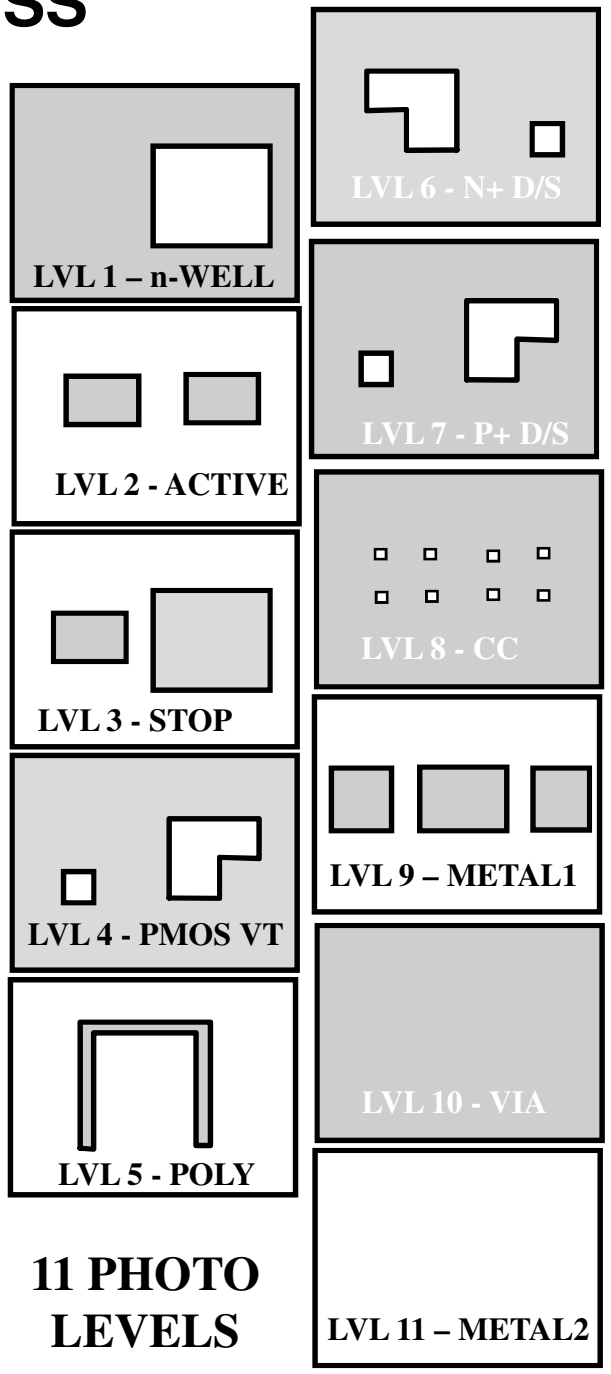
NINE PHOTO LEVELS



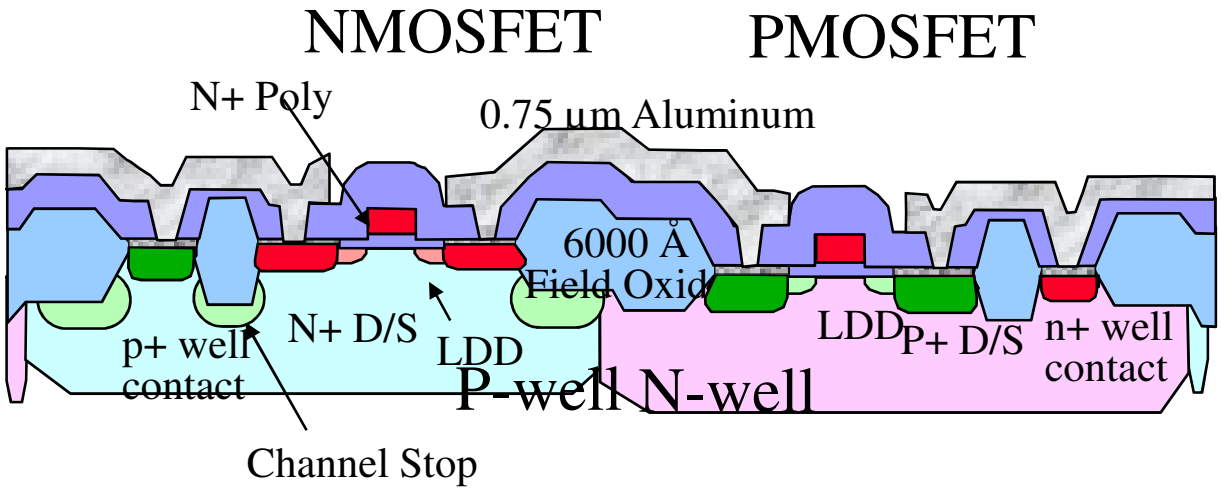
RIT SMFL-CMOS PROCESS



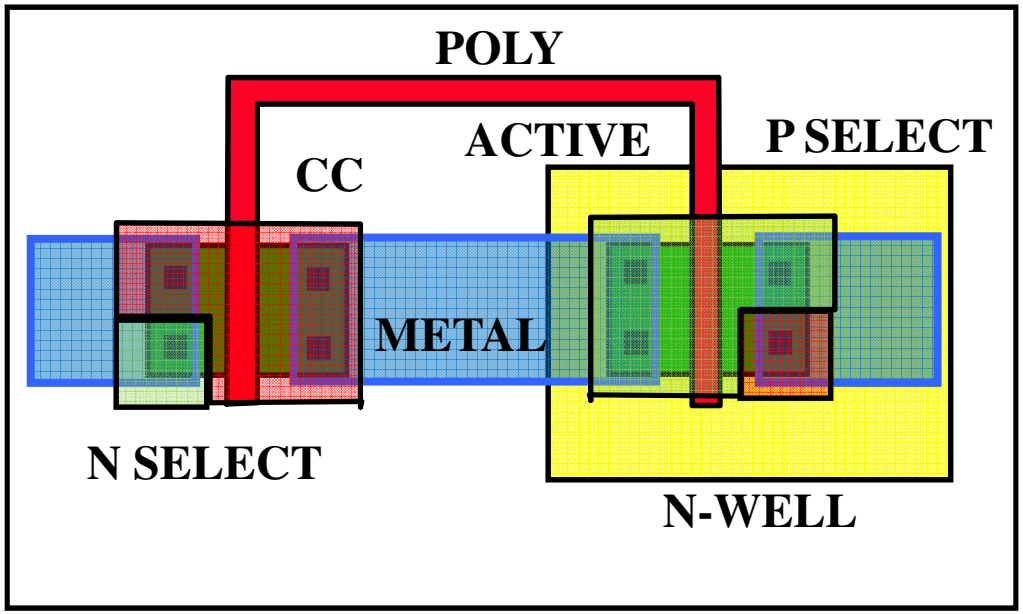


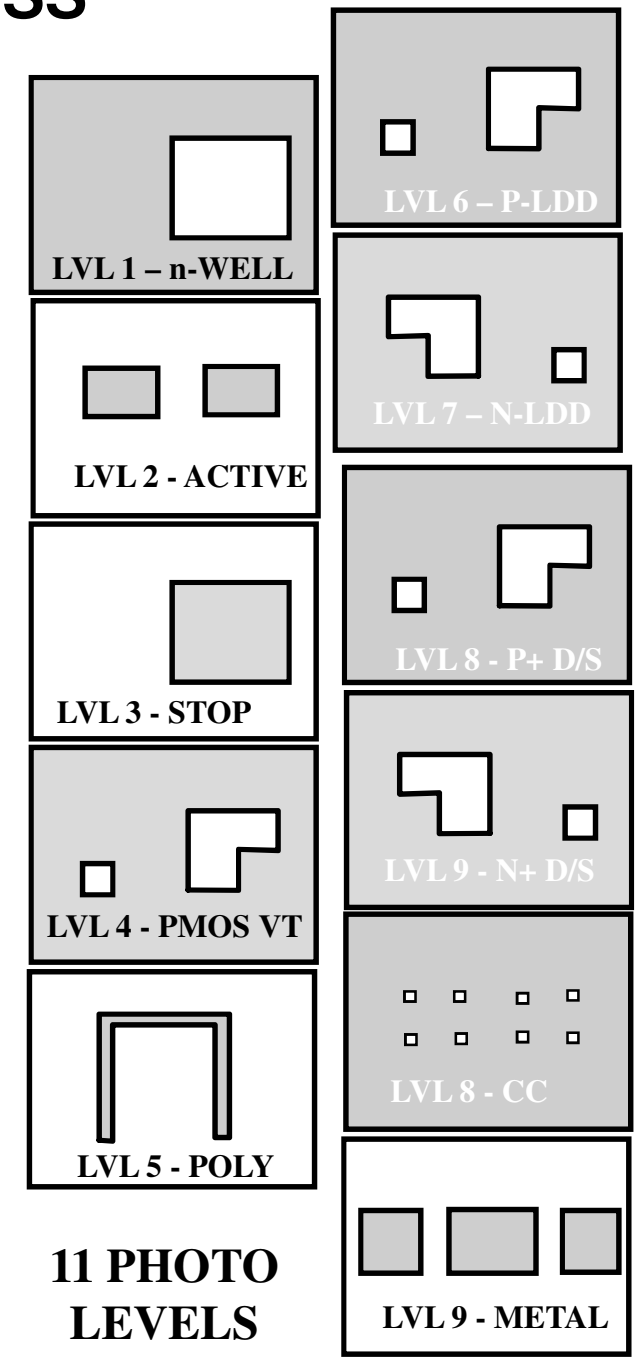


RIT SUB-CMOS PROCESS



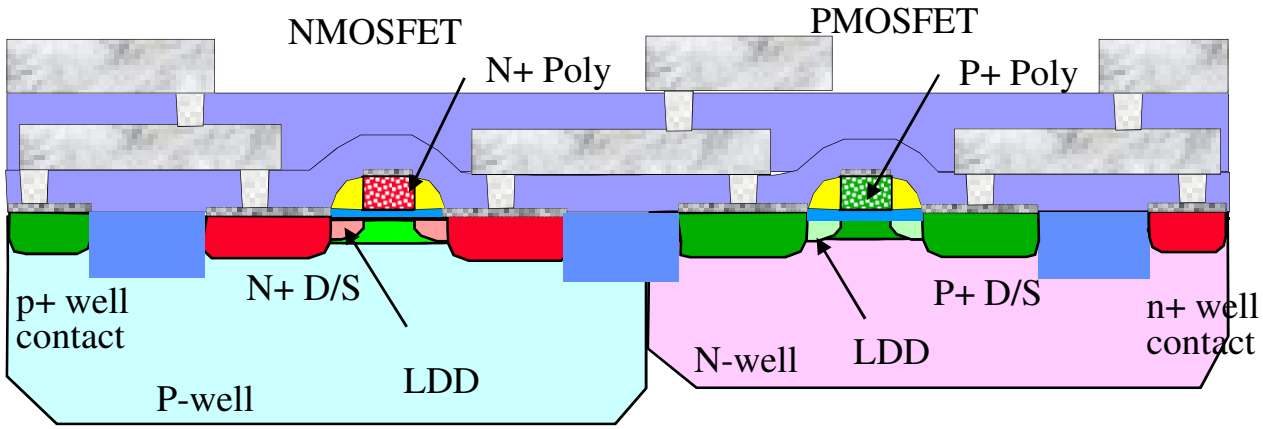
P-type Substrate 10 ohm-cm



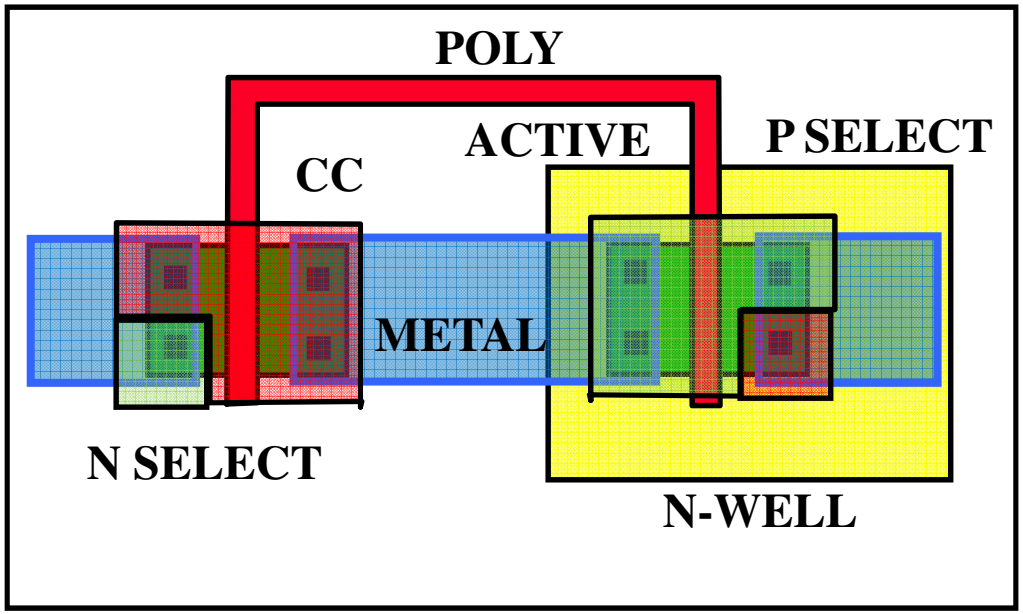


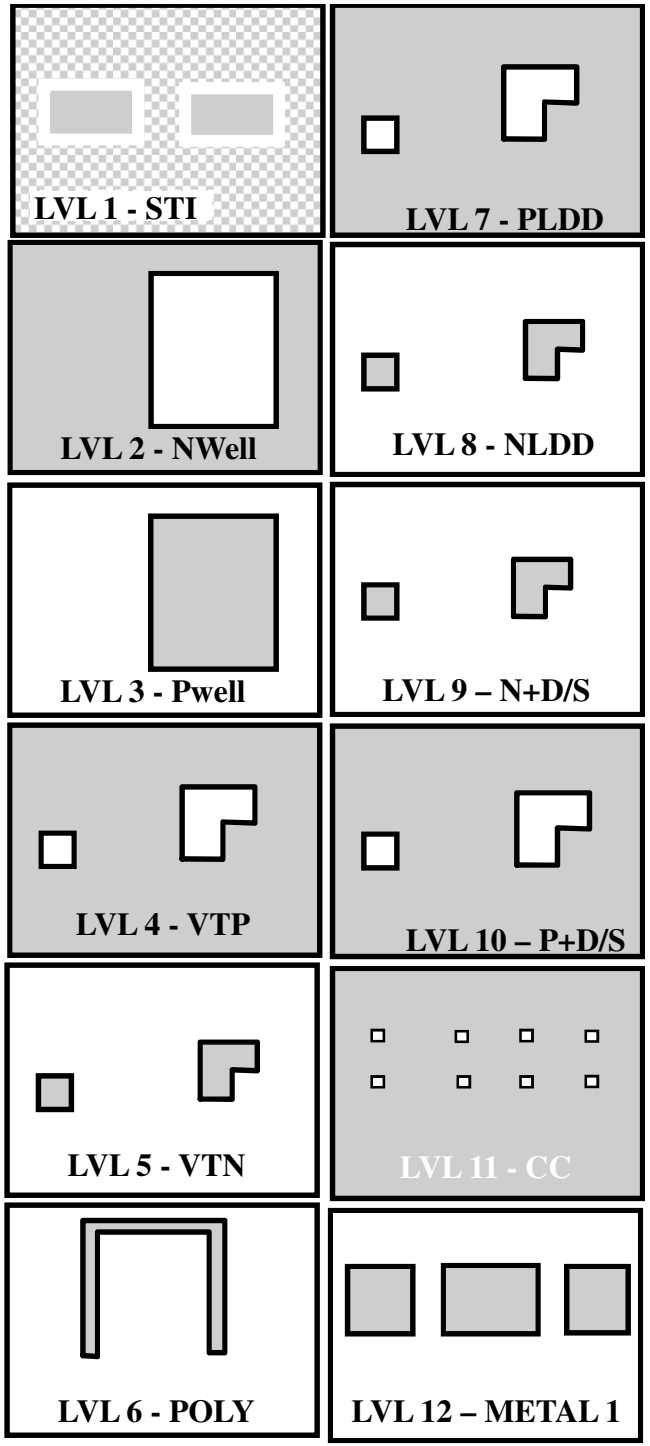
11 PHOTO LEVELS

RIT ADVANCED CMOS PROCESS



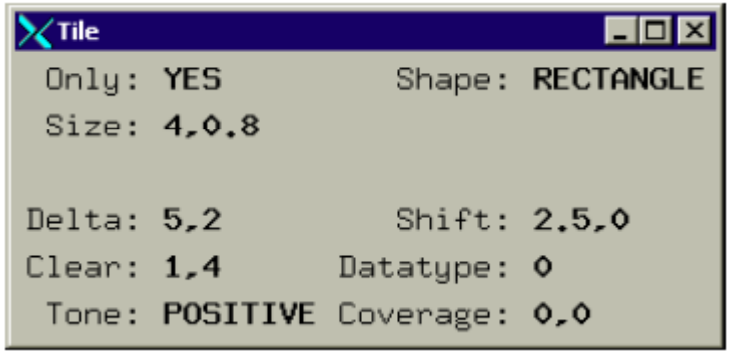
12 PHOTO LEVELS

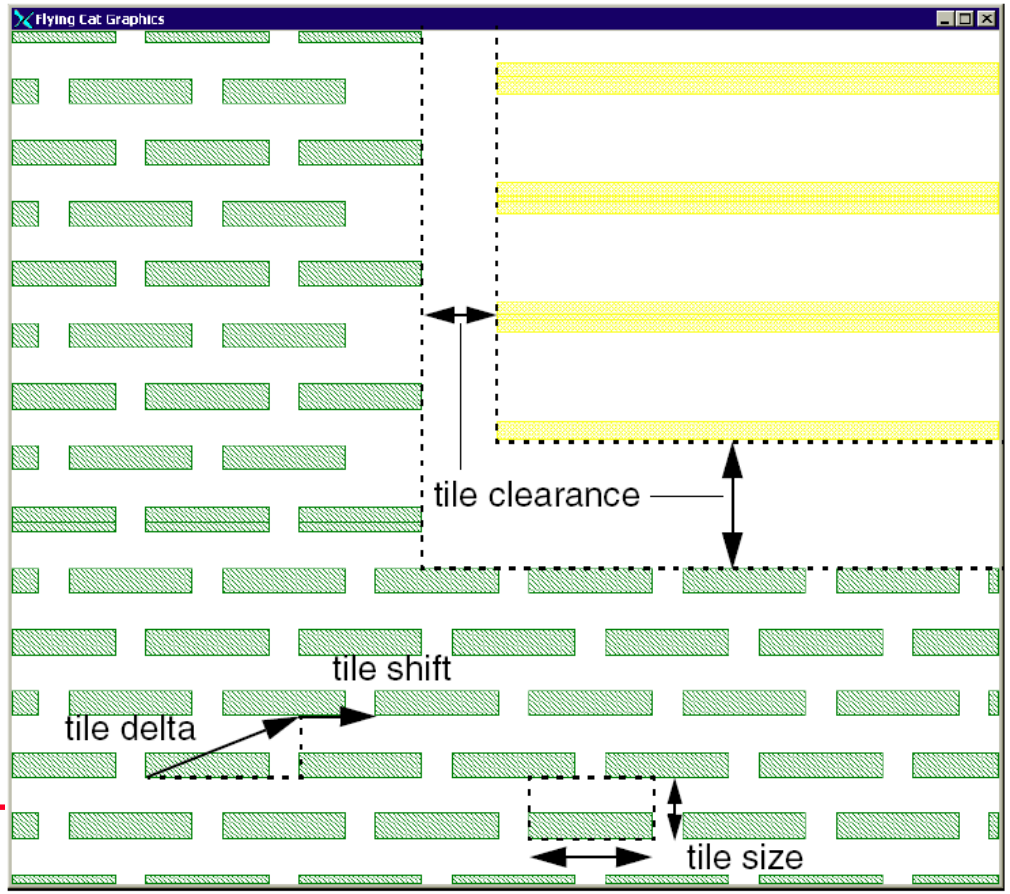




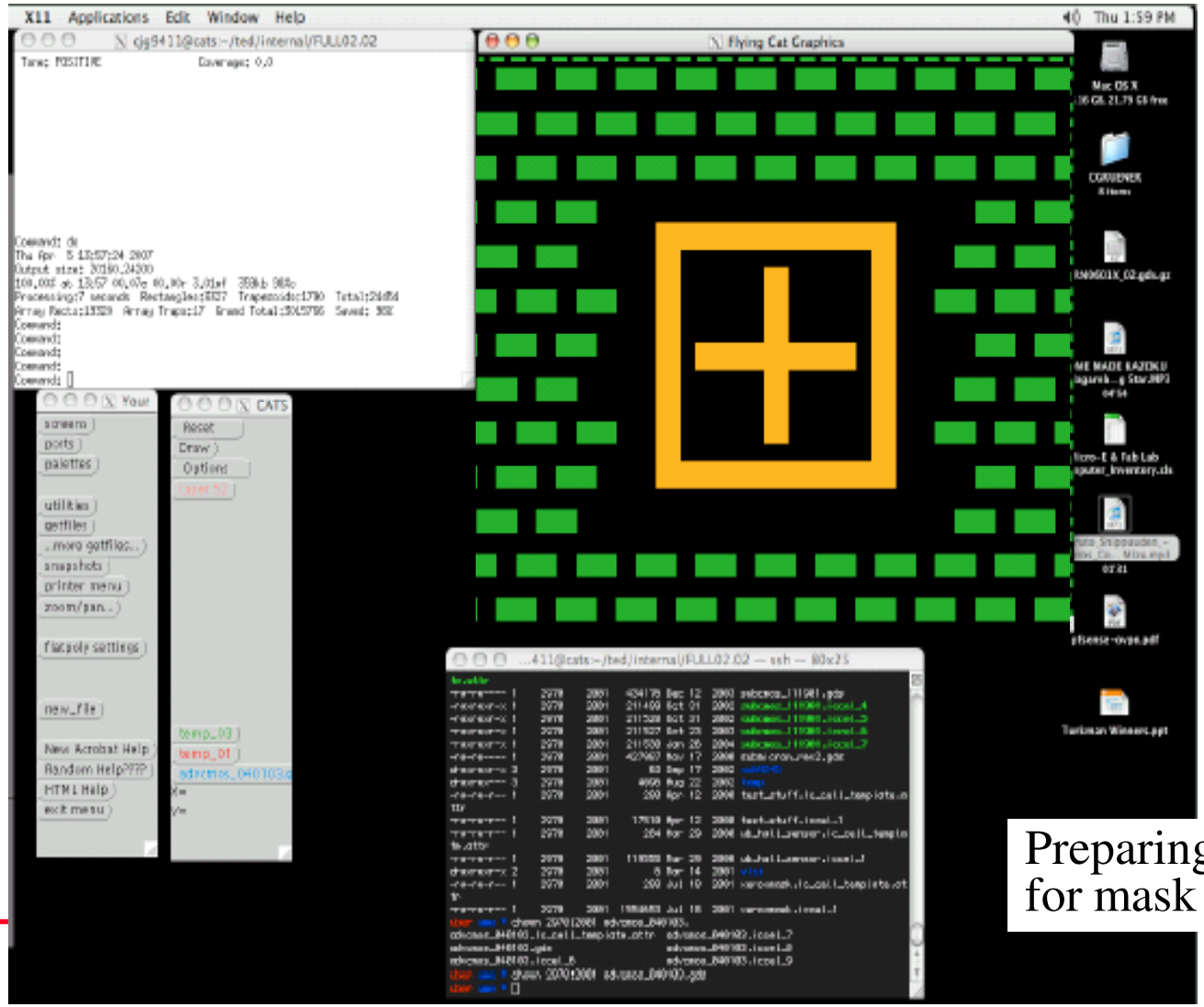
TILING FOR STI LAYER MASKMAKING

Synopsys, Inc.
CATS Software for transcription of CAD design files into readable e-beam and laser formats.





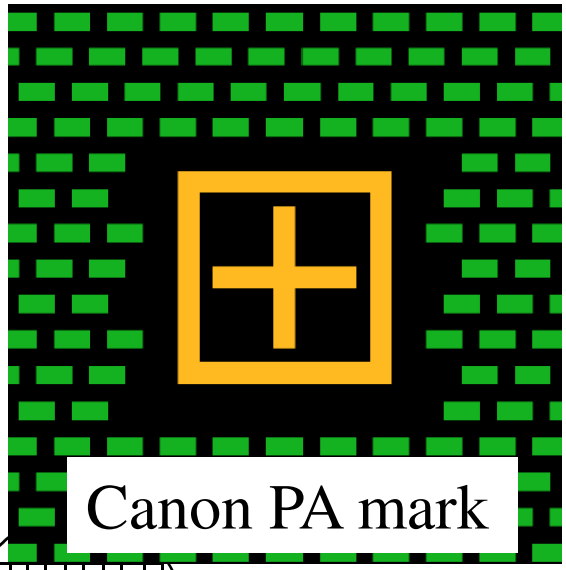
CATS



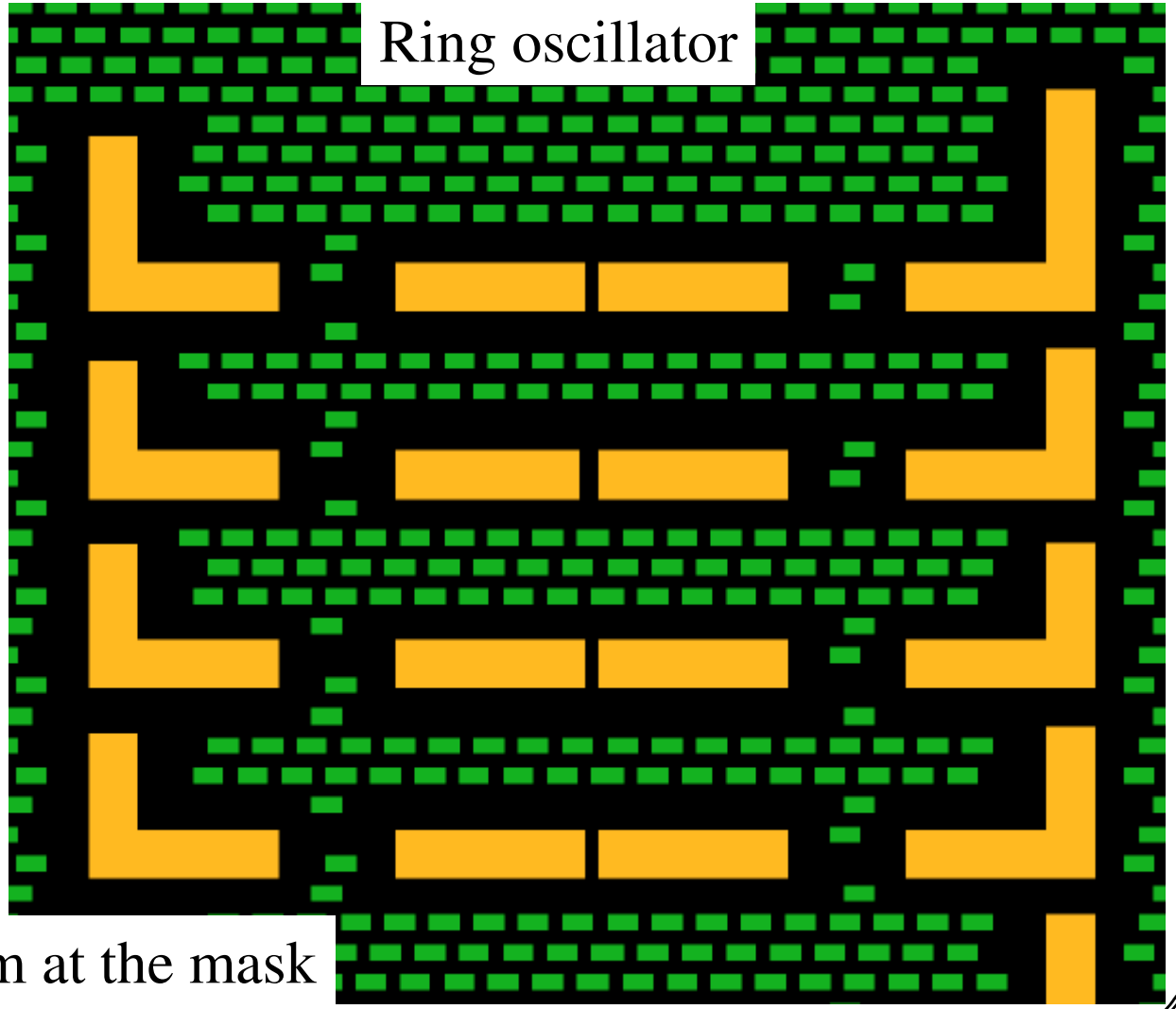
Preparing data files for mask making

TILING FOR RIT'S ADV-CMOS PROCESS STI LEVEL

COMPACT NO
TILE ONLY NO
TILE SHAPE RECTANGLE
TILE SIZE 50,25
DILE DELTA 75,50
TILE CLEAR 50,50
TILE SHIFT 25,0



Canon PA mark



Ring oscillator

Sizes are in µm at the mask

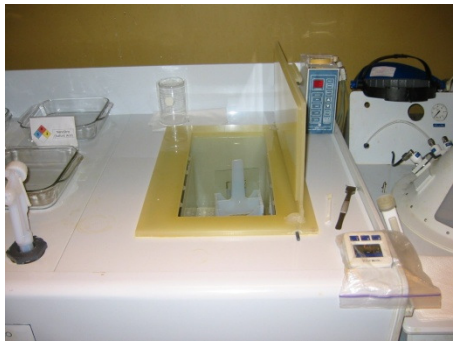
CMOS MASK SET

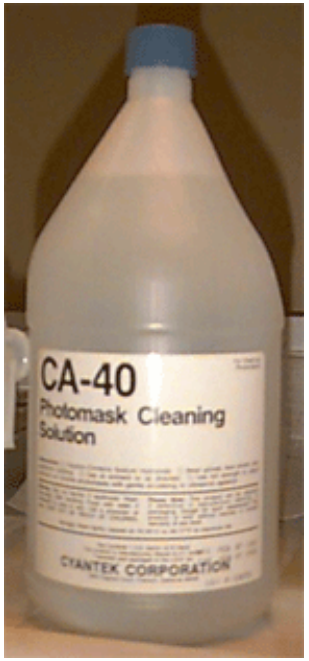
MASK CLEANING AT RIT

1. Pour CA-40 mask cleaning solution (soap) on cloth wipe and wash both sides of the photomask.

2. Rinse in Dump Rinser using the Teflon mask holder. Press RESET then START wait for 3 cycles and press RESET to silence alarm.

3. Use Spin Dryer. Close Door
   Program 6
   Spin Speed 6
   Time 40sec.
   Start

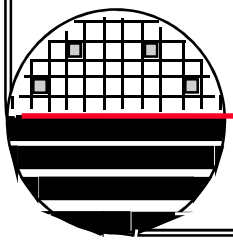




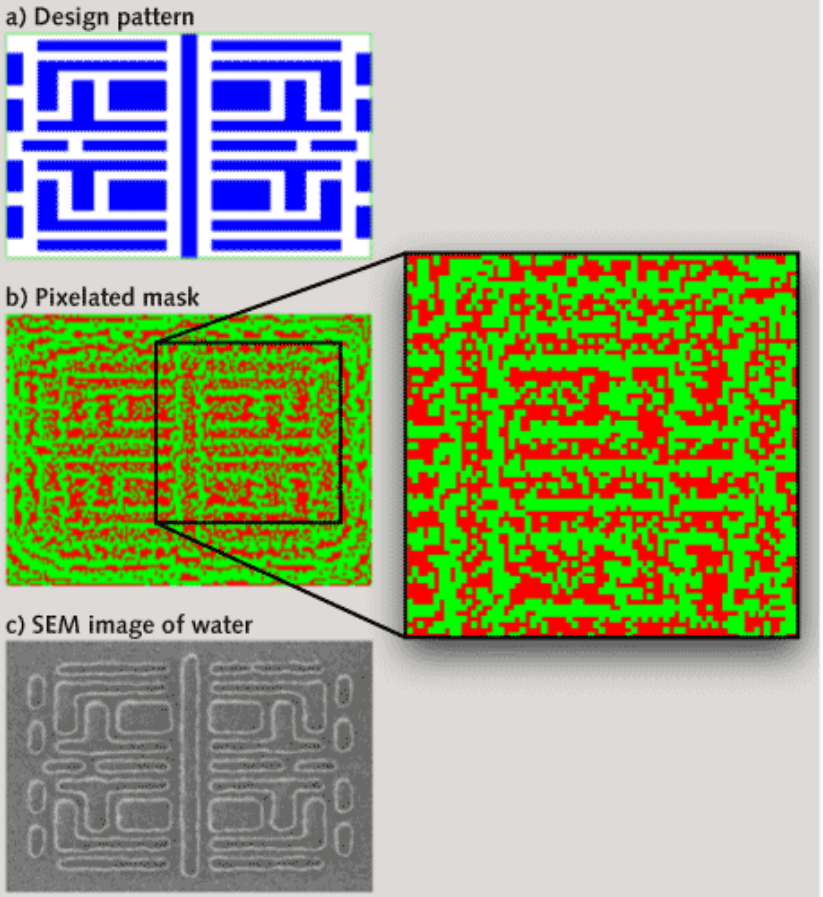
Teflon mask holder

ADVANCED MASKS

Phase Shift Masks
Optical Pattern Correction (OPC)
Tiling



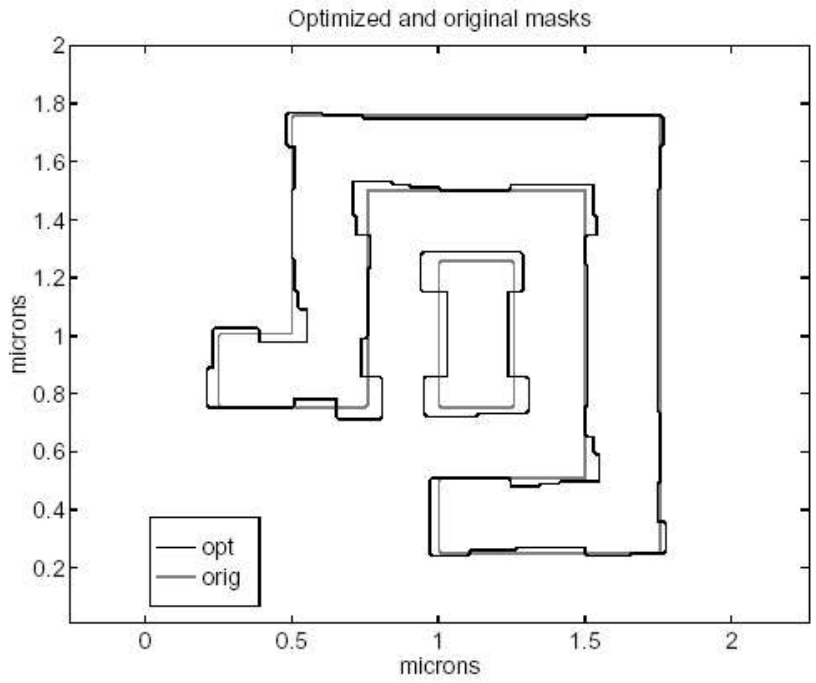
PHASE SHIFT MASKS

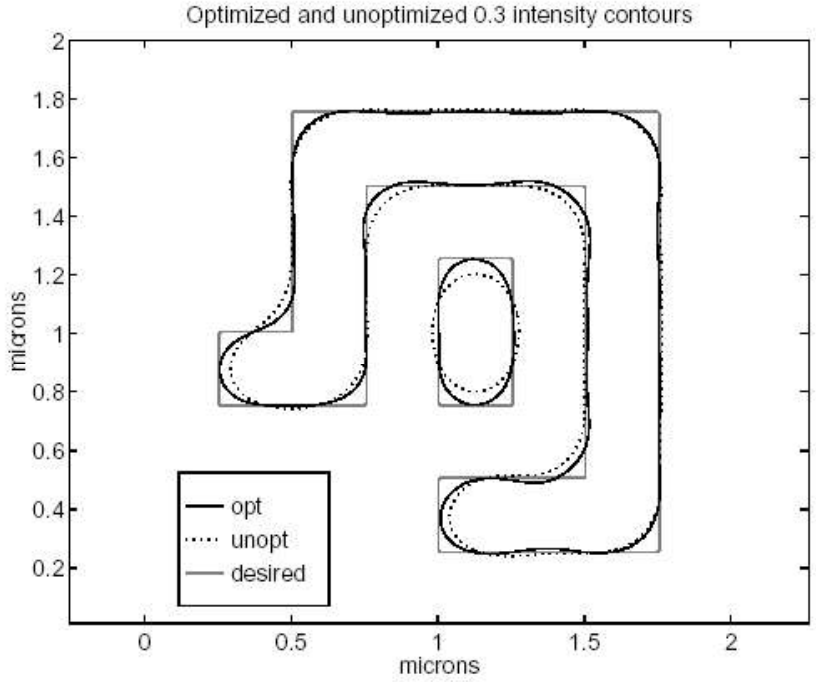


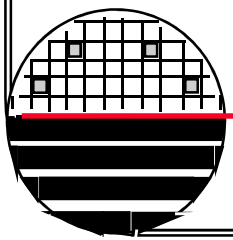
A portion of the 65nm metal 1 design (a) is converted to a pixelated phase mask design (b), where red represents 180° phase shift pits and green represents 0°, and projected by the stepper forming the resist image in (c).

WaferNews source: Intel Corp.

OPTICAL PROXIMITY CORRECTION (OPC)

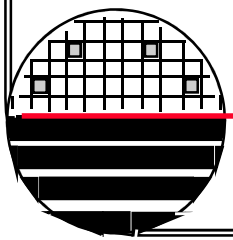






REFERENCES

1. MEBES operation manual.
2. GCA 6700 operation manual.
3. Canon operation manual.
4. "Maskmaking for Canon FPA 2000i", Suraj Bhaskaran, November 30, 1998, RIT presentation.



HOMEWORK - MASKMAKING

1. Describe what mirror 90° does.
2. Describe Boolean AND as it relates to graphical layers.
3. What is the difference between fiducial marks and alignment marks?
4. How are masks inspected?
5. How is a mask repaired?
6. How are masks cleaned at RIT.