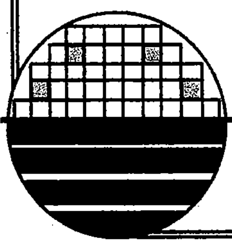
LABORATORY NOTEBOOK

EMCR650 – IC Processing Lab

Brian J. Miga

Winter 2001



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Brian J. Miga 12/4/01

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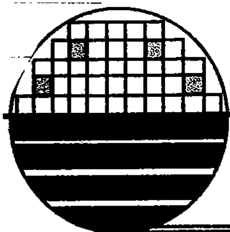

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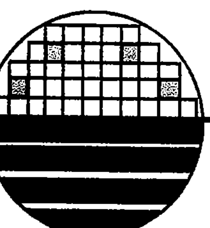
OPERATOR FLOW CHART FOR FACTORY WORK



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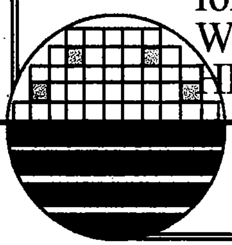
OPERATOR CERTIFICATION SIGNOFF SHEET

	Date/Initials for Initial Training	Date/Initials Certified
Stepper	L.F. 12/4/01	L.F. 1/22/02
Wafertrack	L.F. 1/24/02	
Asher	L.F. 1/12/02	L.F. 1/15/02
RCA Clean	L.F. 12/6/01	
Wet Etch	L.F. 1/22/02	
Al Etch		
Gate Oxide	L.F. 12/11/01	
Wet Oxide		
Well Drive		
Diffusion		
Poly		
Nitride	L.F. 12/12/01	
LTO		
Sputter		
Poly Etch		
Nitride Etch	L.F. 1/15/02	
4 pt Probe		
Nanospec	L.F. 1/15/02	L.F. 1/15/02
Alpha Step		
SCA		
Ion Implant	L.F. 1/15/02	L.F. 1/15/02
Wafer Probe		
HP-4145		



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Br[illegible] M[illegible] 12/4/01

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CMOS PW-3 AND PW-4 PROCESS

SDFCMOS PW-3 One level metal, p-well CMOS process used for analog devices:

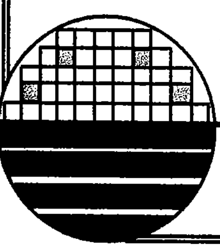
1. ID01
2. DE01
3. CL01
4. OX04--- align
5. PH03-1--well
6. ET06
7. IM01
8. ET07
9. CL01
10. OX06-well drive
11. ET06
12. OX05--- pad
13. CV02
14. PH03 -2- active
15. ET09
16. ET07
17. PH03 -3- stop
18. IM01
19. ET07
20. ET06
21. CL01
22. OX04 -- field
23. ET09
24. ET06
25. CL01
26. OX04 -- kooi
27. IM01
28. PH03 -4- nmos Vt
29. IM01
30. ET07
31. ET06
32. CL01
33. OX06 -- gate
34. CV01
35. DI04
36. ET06
37. DE01
38. PH03 -5- poly
39. ET08
40. ET07
41. PH03 -6- p+ D/S
42 IM01
43 ET07
44 PH03 -7- n+ D/S
45 IM01
46 ET07
47 CL01
48 OX08 -- anneal
49 CV03
50 PH03 -8- CC
51 ET10
52 ET07
53.DE01
54.CL01
55.ME01
56.PH03 -9- m1
57.ET05
58.ET07
59.SI01
60.TE01
61.TE02
62.TE03

SHIP

CMOS PW-4 Two level metal, p-well CMOS process used for the Gate Array (FIRST 49 STEPS SAME AS CMOS PW-3)

50. PH03 -8- CC
51. ET06
52. ET07
53. CL01
54. ME01
55. PH03 -9- metalone
56. ET05
57. ET07
58. SI02
59. TE01
60. TE02
61. TE03
62. HOLD
63. PH03 -8- CC
64. ET06
65. ET07
66. ME01
67. PH03 -9- m1
68. ET05
69. ET07
70. CV03
71. PH03 -10- Via
72. ET10
73. ET07
74. ME01
75. PH03 -11- metal 2
76. ET05
77. ET07
78.SI01
79.TE017
80.TE02
81.TE03

SHIP



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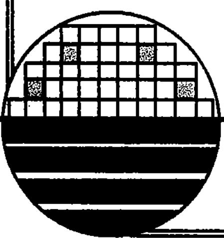
SUB-CMOS PROCESS

CMOS SC8 One level metal, SUBμ twin-well CMOS process

1. ID01
2. DE01
3. CL01
4. OX05--- pad oxide
5. CV02
6. PH03 –1- n well, open
7. ET09
8. IM01 – n-well
9. ET07
10. CL01
11. OX04 – well oxide
12. ET09
13. IM01 – p-well
14. OX06 – well drive
15. ET06
16. CL01
17. OX05 – pad oxide
18. CV02
19. PH03 – 2 - Active
20. ET09
21. ET07
22. PH03 – 3 - p-well stop
23. IM01- stop
24. ET07
25. CL01
26. OX04 - field
27. ET09
28. ET06
29. OX04 - Kooi
30. PH03 – 4 - PMOS Vt Adjust
31. IM01 - Vt
32. ET07
33. ET06
34. CL01
35. OX06 - gate
36. CV01
37. DI04 - dope poly Si
38. PH03 – 5 – poly, open
39. ET08
40. ET07
41. PH03 – 6 - n-LDD, open
42. IM01
43. ET07
44. PH03 – 7 - p-LDD
45. IM01
46. ET07
47. CL01
48. CV03
49. OX08 -- LTO Densify Anneal
50. ET10
51. PH03 – 8 - N+D/S, open
52. IM01 – N+D/S
53. ET07
54. PH03 – 9 P+ D/S
55. IM01 – P+ D/S
56. ET07
57. CL01
58. OX08 – DS Anneal
59. CV03 – LTO
60. PH03 – 10 CC, open
61. ET10
62. ET07
63. CL01
64. ME01
65. PH03 -11- metal, open
66. ET05
67. ET07
68. SI01
69. TE01
70. TE02
71. TE03
72. TE04



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12/13/01

12/13/01
10:18:59

MESA
Instruction Execution

IGEXINQ S36902
QPADEV000T RIT

Lot number . . . . . : F010606
Instruction group . : SUB-CMOS-CV02-NITRID 1.0

Type selections. Then Enter.
1=Display document 2=Execute step 5=Display detail

Opt Text
_ 1.0 Use Lower 6" LPCVD Tube (Primary)
_ 2.0 If Lower 6" LPCVD Tube is occupied, use 4" LPCVD Tube (secondary)
_ 3.0 Include D1-D3
_ 4.0 Include bare dummy wafer to measure nitride thickness
_ 5.0 Thickness desired = 3000 A (see subnit02.pps)
_ 6.0*See SPC chart for operation (nitride.pps) - execute step
_ 7.0 LPCVD Nitride at 800 C for 34 min (use SPC chart)
_ 8.0 Measure nitride thickness on dummy wafer
_ 9.0 Record 3-zone temp, dep pressure, time, thickness
_ 10.0 Record Furnace ID, complete furnace log sheet

Bottom

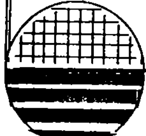
F3=Exit F5=Refresh F11=Display all F12=Cancel F24=More keys

Factory

DAILY LOT STATUS REPORT

DATE: 12/13/01 TIME: 8:00am

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
F010125	Mixed	PW3	D104		X	35	ET06	2	Done with D104
F010321	Mixed	PW3	CV01	X		34	D104	3	Poly
F010328	Subμ	1.0	D104	X		37	PH03	2	n+ Diffusion
F010604	Subμ	150	PH03		X	6	ET09	3	Waiting for Masks
F010605	Mixed	PW3	ET06	X		24	CL01	3	Etch & clean
F010606	Subμ	1.0	CV02	X		18	PH03	3	Nitride 3000Å B
F010924	Mixed	PW3	CV02	X		13	PH03	3	Nitride 1500Å
F011024	Subμ	1.0	OX04		X	11	ET09	3	Done with OX04
F011206	Mixed	PW3	ET07	X		8	CL01	3	Ash & clean
F011212	Subμ	150	OX05	X		4	CV02	3	500Å Pad Ox - Tube 4



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Shift Change Meeting (15 min. at start of lab)
Assignments for each operator are made based on the lot status, equipment status, skill level of the operator, and selection rules

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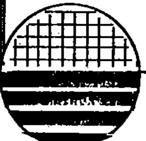
12/4/01

DAILY LOT STATUS REPORT

DATE: 12-3-2001 TIME: 2:30 Pm

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
F001205	Subμ	1.0	ET07	X		46	CL01	1	Down, use backup
F010125	Mixed	PW3	ET07	X		30	ET06	2	Down, use backup
F010321	Mixed	PW3	ET07	X		30	ET06	3	Down, use backup
F010328	Subμ	1.0	PH03	X		30	IM01	2	
F010604	Subμ	150	PH03	X		6	ET09	3	No Stepper Job
F010605	Mixed	PW3	ET07		X	19	ET06	3	Down, use backup
F010606	Subμ	1.0	OX06	X		14	ET06	3	
F010924	Mixed	PW3	ET07	X		8	CL01	3	Down, use backup
F011024	Subμ	1.0	PH03	X		6	ET09	3	



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Page 5

Assigned lot F011024 at step PH03
- Worked with Eric D.

```
12/04/01                     MESA                     IGEXINQ     S36903
10:27:39             Instruction Execution            QPADEV000M   RIT

Lot number . . . . . .   F011024
Instruction group  . :   SUB-CMOS-PH03-N-WELL 1.0

Type selections.  Then Enter.
  1=Display document   2=Execute step   3=Rework-to step

  Opt  Text
  _  > 1.0 Include D1-D3
       2.0 Locate correct masks for this project
       3.0 Record maskID used on move-in
  _    4.0 Use Trac coat program 7,3,3 (GCA1006) (see 733_722.pps)
       5.0 Coat Photoresist on D1-D3, softbake
       6.0 Expose on Stepper, level 1 maskset, NWELL
       7.0 Use correct stepper jobname (10,1)SUBCMOS.NEW\1
       8.0 Use exposure units = 0.4 integrate mode, record as time
       9.0 1 Exposure unit = 250 mj/cm**2
  _    10.0 Develop on Trac program 7,2,2 - postbake 120C (see 733_
  _    11.0 Inspect and record comments (see SUB_STP6.PPT)
                                                              More...
F3=Exit   F10=Display current step   F11=Display groups   F24=More keys
```

12/4/01

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12/4/01

12/04/01 MESA IGEXINQ S36903
10:27:39 Instruction Execution QPADEV000M RIT

Lot number . . . . . : F011024
Instruction group . : SUB-CMOS-PH03-N-WELL 1.0

Type selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt Text
12.0 Record Stepper ID, E, t, Focus, T
13.0 Measure 2um CD on Leitz microscope

Bottom

F3=Exit F10=Display current step F11=Display groups F24=More keys

Upon inspection of the instructions a major issue became apparent: There is NO more GCA Wafertrac!

Need to use handspinner and hot plates.

Used handspinner:

Used hot plates:

Step 1 - Dehydration Bake
115°C for 2 minutes

Step 2 - HMDS Primer
Dispense onto center of wafer by hand
Spin @ 4500 RPM for 60sec.

Step 3 - Apply Resist
Dispense onto center of wafer by hand (Shipley 812)
Spin @ 4500 RPM for 60sec.

[signature] 12/4/01

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12/4/01

Step 4 - Softbake
90°C for 60 sec

Step 5 - Expose
- Use GCA Stepper w/ mask "SUBCMOS1"
Exposure: .4
Focus: 250
Stepper job (10,1) SUBCMOS.NEW\1
- During run, one wafer gave a focus error. Run was continued on advice from TA.
- No other problems occured.

Step 6 - Post Exposure Bake
115°C for 45 sec

Step 7 - Develop
- Wafers were puddle developed by hand.
- First wafer was developed for 60 sec. Inspection of wafer revealed sever underdeveloping. The developer used was left over from previous processing. The developer was changed and the wafer was developed for an additional 30 sec. The other 2 wafers were developed for 60 sec in the new developer with satisfactory results.
- Wafers were rinsed in DI water and dryed with compressed air.
- A spot of PR totally developed away, destroying 1 device.

Step 8 - Hard Bake
120°C 60 sec

[signature]
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Step 9 - Measure CD

- Using the Leitz microscope, the critical dimension was verified to be ~2 μm

The lot was Moved-out to be in-que for the next step.

[signature] 12/4/01

12/6/01

Lot F010125 - 2 wafers
F010605 - 3 wafers
> Ready for RCA CLEAN (CL01

From MESA

1 - Include D1-D3
2 - RCA Clean

- Step 21 for CMOS PW-3 Fixed by Dr. Fuller
  - Removed reference to particle count
  - Added comment to use megasonics bench

DAILY LOT STATUS REPORT

DATE: 12-6-01 TIME: 8:00 am

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
F001205	Subμ	1.0	CV03	X		48	OX08	1	
→ F010125	Mixed	PW3	CL01	X		32	OX06	2	
F010321	Mixed	PW3	ET06	X		31	CL01	3	
F010328	Subμ	1.0	IM01	X		31	ET07	2	
F010604	Subμ	150	PH03		X	6	ET09	3	
→ F010605	Mixed	PW3	CL01	X		21	OX04	3	
F010606	Subμ	1.0	OX06	X		14	ET06	3	
F010924	Mixed	PW3	OX06	X		10	ET06	3	
F011024	Subμ	1.0	IM01	X		8	ET07	3	

step 30 is pmos Vt adj not nmos Vt
Mask is not correctly labeled on verniers. But the pattern is for pmos Vt

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[signature] 12/6/01

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12/6/01

RCA

APM

NH_4OH - 1part 300mL
H_2O_2 - 3parts 900mL
H_2O - 15parts 4500mL
70 °C, 15 min.

→ DI water rinse, 5 min.

→ H_20 - 50
HF - 1
60 sec.

→ DI water rinse, 5 min.

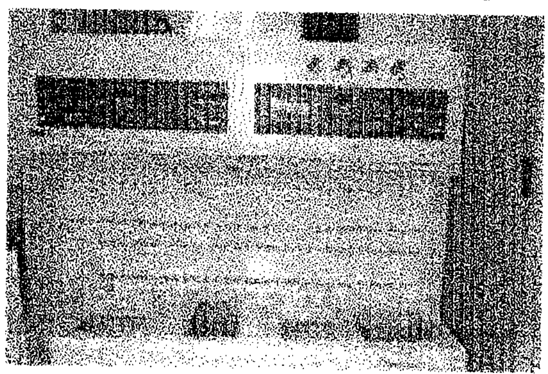
→ HPM

HCL - 1part 300mL
H_2O_2 - 3parts 900mL
H_2O - 15parts 4500mL
70 °C, 15 min.

→ DI water rinse, 5 min.

→ SPIN/RINSE DRY

What does RCA stand for?



12/6/01

12/6/01

Added chemicals as described on previous page.
Both Lots processed together.

- Drain plug issue w/ NH_4OH bath. Lost ~half of chemicals in 10 min while heating.
Lots are going to be processed as follows:
1) NH_4OH bath in old RCA Bench
2) remainder of processing on megasonics.

- Dried in SRD 9B

- 3 wafers from new lot F011206 were also cleaned @ the same time.

- lots moved out (F010605, F010125)

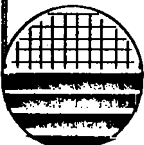
12/6/01

12/11/01

DAILY LOT STATUS REPORT

DATE: 12/11/01 TIME: 8:50 am

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
F001205	Subμ	1.0	ET10	X		50	PH03	1	
F010125	Mixed	PW3	OX06		X	33	CV01	2	
F010321	Mixed	PW3	OX06	X		33	CV01	3	
F010328	Subμ	1.0	OX06	X		35	CV01	2	PX 24
F010604	Subμ	150	PH03		X	6	ET09	3	6" Canon
F010605	Mixed	PW3	OX04	X		22	ET09	3	
F010606	Subμ	1.0	OX05	X		17	CV02	3	
F010924	Mixed	PW3	OX06		X	10	ET06	3	
F011024	Subμ	1.0	OX04	X		11	ET09	3	
F011206	Mixed	PW3	PH03	X		5	ET06	3	



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12/11/01

12/11/01 Assigned lot F010606 @ Step 0x05 (17)
~~Processing VJ's lot (F010328) 0x06 (35)~~ BJM
Dave's lot also in @ same time.
VJ will come in to unload work.
- Ran Prog #50 - Trans LC Clean (Turn Bubbler on in back)
- Started warm-up process on furnace tube 4 (to 800°C)

- VJ's lot is different. My lot and Dave's lot are being processed together.

- Dave's lot requires TCA clean during warm-up, so this will be performed prior to diffusion run (F010321)

- Target $X_{ox} = 500Å$

Recipe 250: (Tube #4)

Step	Time (min)	Temp (C)	Gas (SLPM)	Boat (In/min)
0 Boat Out	0	800	$N_2 = 5$	Out = 10
1 Push In	12	800	$N_2 = 10$	In = 15
2 Ramp Up	20	1000	$O_2 = 5$	
3 Soak O_2	43	1000	$O_2 = 10$	
4 N_2 Purge	5	25	$N_2 = 15$	
5 Ramp Down	35	25	$N_2 = 10$	
6 Pull Out	15	25	$N_2 = 5$	Out = 10

- MESA instructions were modified to reflect the TCA Clean for sub-CMOS process for this step and other 500Å dry oxides.

- Run was completed with no problems

[signature]
12/11/01

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12/11/01

```
12/11/01                               MESA                     IGEXINQ    S36902
10:14:48                      Instruction Execution             QPADEV000Q   RIT

Lot number . . . . . .   F010606
Instruction group  . :   SUB-CMOS-OX05-PAD    1.0

Type selections.  Then Enter.
  1=Display document    2=Execute step    5=Display detail

 Opt  Text
  _   1.0 Include D1-D3
  _   2.0 Use resource FURNACE04 BRUCE TUBE 04 (see subpadox.pps)
  _   3.0 Xox desired = 500A
  _   4.0*See SPC chart for operation (see*pad_ox.pps)- execute
  _   5.0 XRF warm up recipe 888, check gas supply
  _   6.0 When furnace stabilizes at 800 C abort 888
  _   7.0 XRF 500A dry O2 recipe 250, load wafers, press start
  _       P/P 800C, RU 20min, soak 43min dry O2 1000C, RD 40min
  _   8.0 When wafers complete abort 250 and XRF idle recipe 999
  _   9.0 Record 3-zone temp and soak time
  _   10.0 Record Xox at 5 test sites on D1 (see measloc.pps)
                                                                        More...
F3=Exit   F5=Refresh   F11=Display all   F12=Cancel   F24=More keys
```

```
12/11/01                               MESA                     IGEXINQ    S36903
10:15:36                      Instruction Execution             QPADEV000Q   RIT

Lot number . . . . . .   F010606
Instruction group  . :   SUB-CMOS-OX05-PAD    1.0

Type selections.  Then Enter.
  1=Display document    2=Execute step

 Opt  Text
  _   11.0 Record Furnace ID, complete furnace log sheet




                                                                        Bottom
F3=Exit   F5=Refresh   F11=Display groups   F12=Cancel   F24=More keys
```

Color was out in printer, so SPC chart would not print.

[signature] 12/11/01

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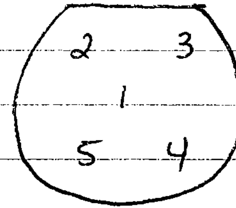
- oxide thickness measured on nanospec.
  (wafer D1)



* END OF TEST *

Ave ox: 475 Å

REFR INDEX = 1.45

Sample ID:
D1

NUMBER	THICKNESS
1	467 A
2	473 A
3	494 A
4	478 A
5	4[illegible] A

- Lot was moved on to next step in MESA.

[signature]
12/11/01

12/13/01

- Assigned lot F010606 at CV02 (step 18) → 3000Å Nitride (3 wafers)

- Tool was off. followed instructions listed in ASM 6" LPCVD Poly + Nitride instruction manual.

- According to log sheet, last 4 runs Averaged 50Å/min.
  ∴ 1:00:00 run to be performed.

- Recipe used is "RIT Standard Nitride".
  There is a new recipe for Nitride that has just been setup.
  Going to change in MESA with Dr. Fuller so future runs use "Nitride 810".

- 10 dummy wafers also included in run for Robin. Will use one of these to measure Nitride thickness.

[signature]
12/13/01

12/13/01

Si_3N_4 (1:25) RIT Standard Nitride

Step	Time	Temp °C Zone 1	Zone 2	Zone 3	Pressure (mtorr) Pump MKS	Tube MKS	Press Ck	Flows (sccm) SiH_2Cl_2	NH_3	N_2 Purge
1 Status	10s									
2 Slow_Pump_1	45min	800*	800*	810*	4000					
3 Pump_Down 1	2min	800	800	810	4000	300*				
4 Leak_Check	1min	800	800	810	4000	300	400			
5 Isolate 1										
6 N_2_Pump 1	30min	800	800	810	4000	300				150
7 Isolate 2	10sec	800	800	810	4000	300				
8 Ramp_Up1	40sec	800	800	810	4000	300*		60*	150*	
9 Set_Flow1	1hr**	800	800	810	4000	300		60	150	
10 Rf_Check										
11 Heat_up										
12 Ramp_Down 1	15sec	380	380	380	4000	300				
13 Pump_Down 2	2min	380	380	380	4000					
14 Leak_Check2										
56 Pst_Purge	1min 20sec	380	380	380	4000					150
57 Pump_Down9	1min	380	380	380	4000					
58 Isolate 9	15sec	380	380	380	4000					
59 N_2_Pump6	15min	380	380	380	4000					
60 Back_Fill	10min	380	380	380	4000					
61 End_1	1sec	380	380	380	4000	4000				

NOTES: * → Ramp

** → Calculated time

- Run time for recipe is approximately 2½ hours.

- Nitride SPC chart did not come up. Checked log file to determine if ok to run

[signature] 12/13/01

12/13/01

- Required info for MESA

Temp

Zone 1: 820.4

Zone 2: 799.9

Zone 3: 815.1

Dep Pressure: 340 mtorr

Time: 1 hr

Thickness:

Furnace ID: LPCVD02

- Log sheet on computer by Bruce furnace filled out.

- In order to speed up evacuating gas lines after run, shut off SiH_2Cl_2 w/ 3 ½ min left and NH_3 w/ 2½ min left. (According to Jeff)

- Reported bad vibration noise from load part of CVD tool to ~~Bruce~~ T.

- Run completed with no problems. Unloaded and started Gas line pumpdown. Turned over to Kevin.

- Wafers were Green. Monitor wafer measured on nanospec.
  - Monitor wafer and Robin's wafers were very spotty. Most likely they were dirty.

- Moveout completed

- Overshot target thickness of 3000Å. Noted in MESA

Objective Lens: 10X

Sample ID:
C1

NUMBER	THICKNESS
1	3622 A
2	3648 A
3	3623 A
4	3696 A

[signature] 12/13/01

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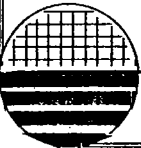
12/18/01 Lot F010125 - Ash Resist (2 wafers)

Factory

DAILY LOT STATUS REPORT

DATE: 12-17-01 TIME: 3:00pm

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
→ F010125	Mixed	PW3	ET07	X		40	PH03	2	Ash Resist
F010321	Mixed	PW3	CV01	X		34	D104	3	Poly Deposition
F010328	Subμ	1.0	ET08	X		41	ET07	2	LTO Etch
F010604	Subμ	150	PH03		X	6	ET09	3	1st level
F010605	Mixed	PW3	IM01	X		27	PH03	3	Vt
F010606	Subμ	1.0	ET09		X	20	ET07	3	1 wafer done 2 to go
F010924	Mixed	PW3	CV02	X		13	PH03	3	Nitride Dep
F011024	Subμ	1.0	OX06	X		14	ET06	3	Well Drive
F011206	Mixed	PW3	OX06		X	10	ET06	3	Well Drive
F011212	Subμ	150	CV02	X		5	PH03	3	Nitride Dep.



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- Use Branson asher
- load 4" Standard Recipe
- Forward Power 360 Watts
  Reflected Power 0 Watts
  Etch time 1.5 min
  Poly 4μm CD
  Resist Gone yes
- Dr. Fuller recommended using end-point detection next time.

[signature] 12/18/01

12/20/01

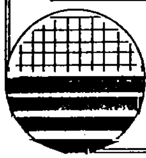
- Assigned lot F010125 at PH03 (step 41) 2 wafers

Factory

DAILY LOT STATUS REPORT

DATE: 12-20-01 **TIME:** 8:30am

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
→ F010125	Mixed	PW3	PH03	X		41	IM01	2	Photo
F010321	Mixed	PW3	CV01	X		34	D104	3	Poly dep
F010328	Subμ	1.0	ET07	X		42	PH03	2	ash
F010604	Subμ	150	ET09	X		7	IM01	3	Nitride Etch
F010605	Mixed	PW3	IM01	X		29	ET07	2	mplant
F010606	Subμ	1.0	PH03		X	22	IM01	3	Photo
F010924	Mixed	PW3	CV02	X		13	PH03	3	Nitride Dep
F011024	Subμ	1.0	OX05	X		17	CV02	3	Pad Oxide Tube D4
F011206	Mixed	PW3	CV02	X		13	PH03	3	Nitride Dep
F011212	Subμ	150	CV02	X		5	PH03	3	Nitride Dep



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```
12/20/01                    MESA                   IGEXINQ      S36903
 9:21:10           Instruction Execution           QPADEV000W    RIT

Lot number . . . . . :   F010125
Instruction group  . :   CMOS-PH03-P+-DS      3.0

Type selections.  Then Enter.
  1=Display document   2=Execute step   3=Rework-to step

  Opt  Text
   _ > 1.0 Include D1-D3 (General Instructions) (see lvl6phot.pps)
       2.0 Locate correct masks for this project
       3.0 Record device and test mask no., move-in
   _   4.0 Use Trac coat program 7,3,3 (GCA1006) (see 733_722.pps)
       5.0 Coat Photoresist on D1-D3, softbake
       6.0 Expose on Stepper, level 6 maskset, P+D/S
       7.0 Use correct stepper jobname\6T,6D
       8.0 Use integrate mode, exposure units =.4, record as time
       9.0 1 Exposure unit = 250 mW/cm**2
   _   10.0 Develop on Trac program 7,2,2 - postbake 120C (see 733_
       11.0 Inspect and record comments
                                                          More.
```

12/20/01

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12/20/01

12/20/01
9:21:10

MESA
Instruction Execution

IGEXINQ S36903
QPADEV000W RIT

Lot number . . . . . . : F010125
Instruction group . . : CMOS-PH03-P+-DS 3.0

Type selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt	Text
	12.0 Record Stepper ID, E, t, Focus, T
_	13.0 Measure X and Y overlay in 5 locations (see xyloc.pps)
_	14.0 Measure 4um CD on Leitz Microscope (see alverncd.pps)
_	15.0 Check Ring oscillator (see s42im01.pps)

- Lot moved in in MESA
- Acquired Factory Mask ID: MIXCMOS2
- Wafer trac not available. Must coat by hand.
- Step 1 - Dehydration bake
  115°C for 2 min.
- Step 2 - HMDS Primer
  Dispense onto center of wafer by hand (pipet)
  Spin on prog. 1 (4500RPM for 60 sec.)
- Step 3 - Apply Resist
  Dispense onto center of wafer by hand.
  Spin on prog 1
  ~~Step~~
- Step 4 - Soft Bake
  90°C for 60 sec

[signature] 12/20/01

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12/20/01 Step 5 - Expose
- GCA Stepper
- Level 6, MASK MIXCMOS2
- Stepper Job: EXEC [10,1] CMOSMIX16
- Exposure = .4 sec
- Dose = 250
- Process improvement: eliminate auto focus errors on GCA
- Run completed w/ no problems.

Step 6 - PEB
115°C for 45 sec

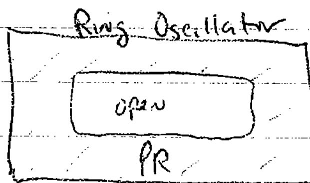
Step 7 - Develop
- Develop by hand in glass dish (~~10 sec~~) 45 sec
- Rinse w/ DI water
- Inspected under microscope: Develop was complete after 45 sec on advice from Dr. Fuller

Step 8 - Hard Bake
120°C for 60 sec

Step 9 - Measure Overlay in 5 locations:
No overlay marks available

- Also no place to measure CD.

Step 10 - Ring Oscillator checked, looked good.



[signature]
12/20/01

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12/20/01

- Level 6 is a dark field mask (all areas covered except where we want P+ implant.

- Open areas appear green

- PR appears Blue.

- Lot Looks good. Moveout completed.

B— J M— 12/20/01

1/8/02

Factory

DAILY LOT STATUS REPORT

DATE: 1-8-2002 TIME: 8:47 am

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
F010125	Mixed	PW3	IM01		X	42	ET07	2	
F010321	Mixed	PW3	CV01	X		34	DI04	3	
F010328	Subμ	1.0	IM01		X	44	ET07	2	
F010604	Subμ	150	ET09		X	7	IM01	3	
F010605	Mixed	PW3	CV01	X		34	DI04	2	
→ F010606	Subμ	1.0	ET09	X		27	ET06	3	Brian
F010924	Mixed	PW3	PH03	X		14	ET09	3	
F011024	Subμ	1.0	ET09	X		20	ET07	3	
F011206	Mixed	PW3	PH03	X		14	ET09	3	
F011212	Subμ	150	CV02	X		5	PH03	3	

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1/8/02

- Assigned lot F010606 at step ET09 (Nitride etch I think.)
Lot contains 3 wafers.

- Move in atempted, MESA needed to be initialized for new year. Fixed by Dr. Fuller. Lot moved-in

- Instructions only said to include all wafers

- Tool used for dry etch is Drytek Quad 482

```
1/08/02                        MESA                          IGMSINQ     S36801
10:40:14             Instruction Group Inquiry               QPADEV000V    RIT

Type information.  Then Enter.
  1=Display document, 5=Display detail

  Plant . . . . . . . . :   RIT
  Instruction group . .     SUB-CMOS-ET09-FIELD   SUB-CMOS ET09 NITRIDE FIELD
    Revision . . . . . .    1.0

  Opt Subgroup  Text
   _            1.0 Include D1-D3 (see subnoc.pps)
   _            2.0 Wet Etch 0.5 minute in Buffered HF, Rinse, Spin Dry
   _            3.0 Plasma etch Drytek Quad, SF6 flow- 60sccm,
                    Pressure=300mTorr, Power=300W, Etch Rate=600 A/min
   _                OR (if Drytek Quad is in use or tool is down)
   _            4.0 Plasma etch GEC Cell, SF6 flow= 30sccm,
   _                Pressure=300mTorr, Power=50W, Etch Rate=1500 A/min
   _            5.0 After etch, oxide should be 250-500A in active areas
   _            6.0 Record gas, flow, pressure, fwd/ref power, time
                                                                       Bottc
F3=Exit   F4=Prompt   F5=Refresh   F10=View 2   F12=Cancel
```

- Got instructions to print. Must do Wet Etch for 30 sec first

- Performed in wet Etch 2
  - 30sec in Buffered HF
  - Ran in SRD
  - ready for dry Etch

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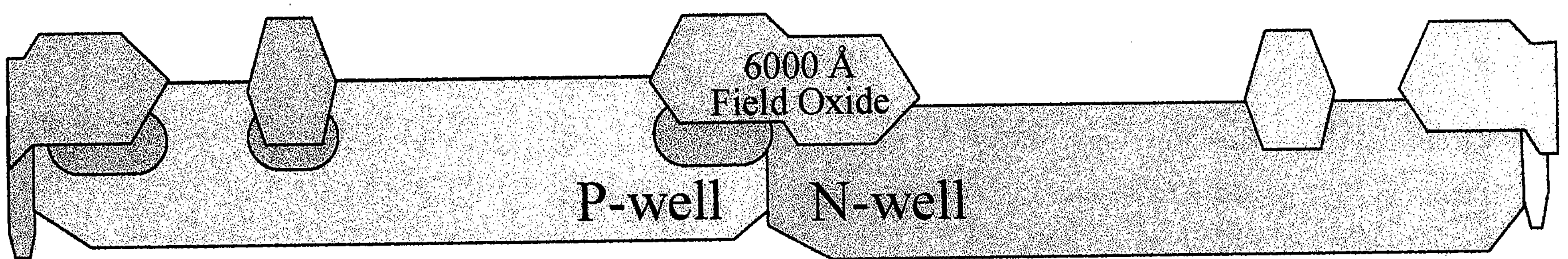
1/8/02

ETCH NITRIDE AND PAD OXIDE



N-type Substrate 10 ohm-cm

1/8/02

According to MESA - Nitride thickness should be 3000Å
I did this dep. Results were closer to 3600Å.

Etch rate according ~~EAL D.~~ MESA → 600Å

∴ Etch for 5 min and see what is up

- VJ helped teach me how to run the tool.

- Tool needed to have recipe re-written. was done by Eric D since he was on tool before me.

ogram
in Oxide on
jective Lens: 10X
mple ID:

MBER	THICKNESS
1	166 Å

- 1st 2 measurements are in the wrong area.
- The wafer had what looked like a brown water mark over 75% of it. This was remaining pad oxide. Etch was too long. reduced time to 4:30 sec. for remaining 2 wafers (D1, D3)

Gas: SF6
flow: 60sccm
Pressure: 394 mtorr
Power: 280 W
Time: 4:30

- Remaining 2 wafers looked Good. Moved-Out in MESA

[signature]
1/8/02

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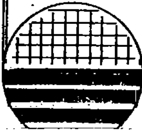
1/10/02 Assigned lot F010125 @ IM01 (step 45) - 2 wafers
Implant N+ D/S P- 4E15 - 120KeV

Factory

DAILY LOT STATUS REPORT

DATE: 1-10-02 TIME: 7:30am

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
F010125	Mixed	PW3	IM01	X		45	ET07	2	Brian
F010321	Mixed	PW3	ET06	X		36	DE01	3	
F010328	Subμ	1.0	IM01	X		47	ET07	2	
F010604	Subμ	150	ET07	X		9	CL01	3	
F010605	Mixed	PW3	CU01	X		34	DI04	2	
F010606	Subμ	1.0	PH03	X		30	IM01	3	
F010924	Mixed	PW3	ET07	X		16	PH03	3	
F011024	Subμ	1.0	PH03	X		22	IM01	3	
F011206	Mixed	PW3	ET09	X		15	ET07	2	
F011212	Subμ	150	PH03	X		6	ET09	3	



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1/10/02 MESA IGMSINQ S36801
9:25:08 Instruction Group Inquiry QPADEV000B RIT

Type information. Then Enter.
1=Display document, 5=Display detail

Plant . . . . : RIT
Instruction group . . CMOS-IM01-N+-DS CMOS IM01 N+ DS IMPLANT
Revision 3.0

Opt	Subgroup	Text
_	1.0	Include D1-D3 (see IMP01.FFT) (see impl_N+.pps)
_	2.0	Ion Implant Phosphorous, PH3, P31 (see impt_ph.pps)
_	3.0	Dose = 4e15 (about 1 hour/wafer)
_	4.0	Energy = 120 KeV
_	5.0	Do not implant with current above 30uA (damages PR)
_	6.0	Record Energy, Dose, Set-up time, Gas, Species

Botto

F3=Exit F4=Prompt F5=Refresh F10=View 2 F12=Cancel

Br 1/10/02

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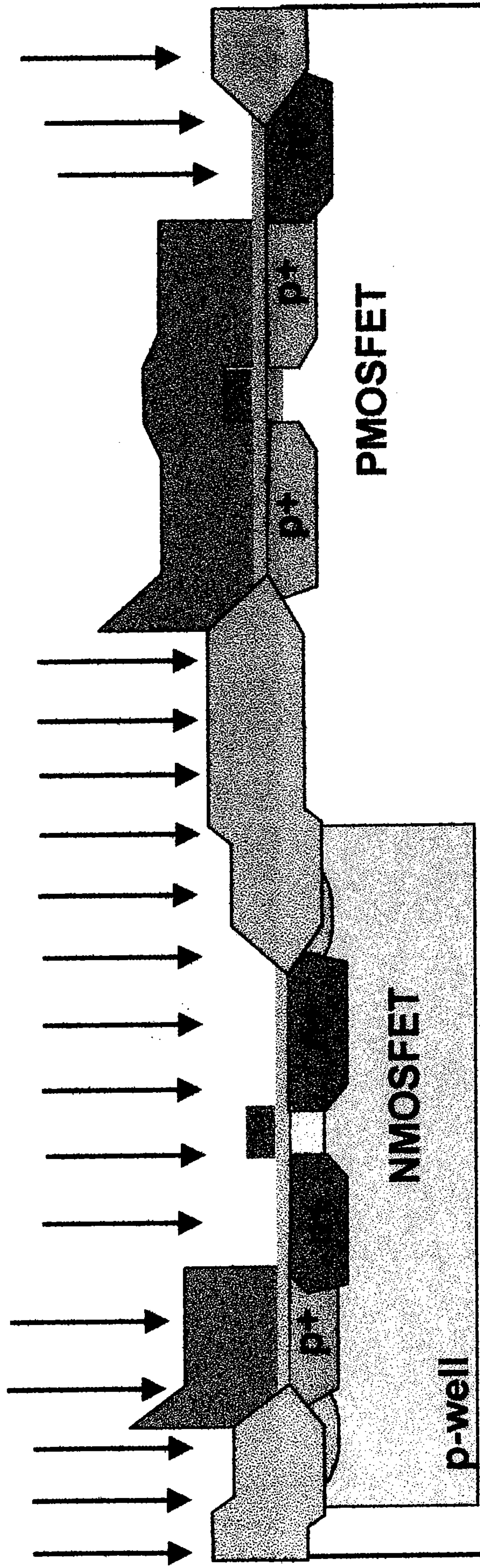
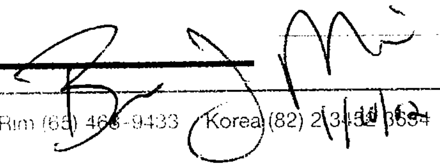
1/10/02





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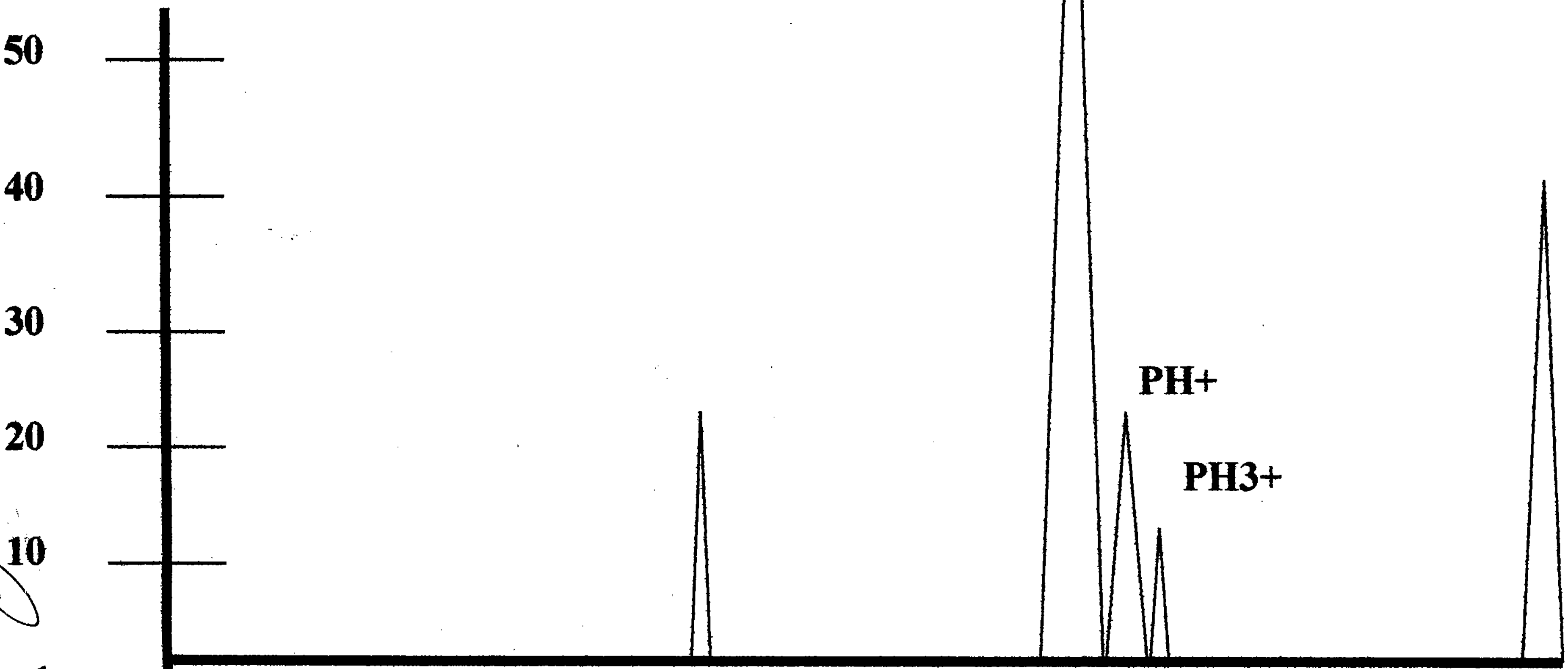
1/10/02



1/10/03

1/10/02

Followed instructions in "Varian 350D Ion Implanter Operator's instructionmanual." There was an initial set of short instructions that were wrong. Dr Fuller disposed of them. Followed the correcte instructions and machine set up great.

According to mesa, limit beam current to 30μA

Energy: 120KV

Dose: 4E15

Set-up time: 40min.

Gas: Phosphine

Species: P31

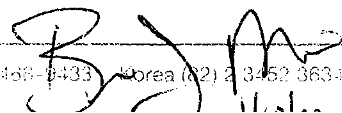
Set up beam at 28μA to stay within spec but max. throughput.

During implant, the beam current fluctuated quite a bit. It would peak around 40μA, but would drop back down. This should be ok for the PR.

30μA limit was for old Varian 400. We maxed beam current to ~ 50μA to see what it dose.

Log sheet created on PC in control rack instead of paper copies.

- Inspection of wafer that recieved higher beam current looks good under microscope. Need to change limits in MESA



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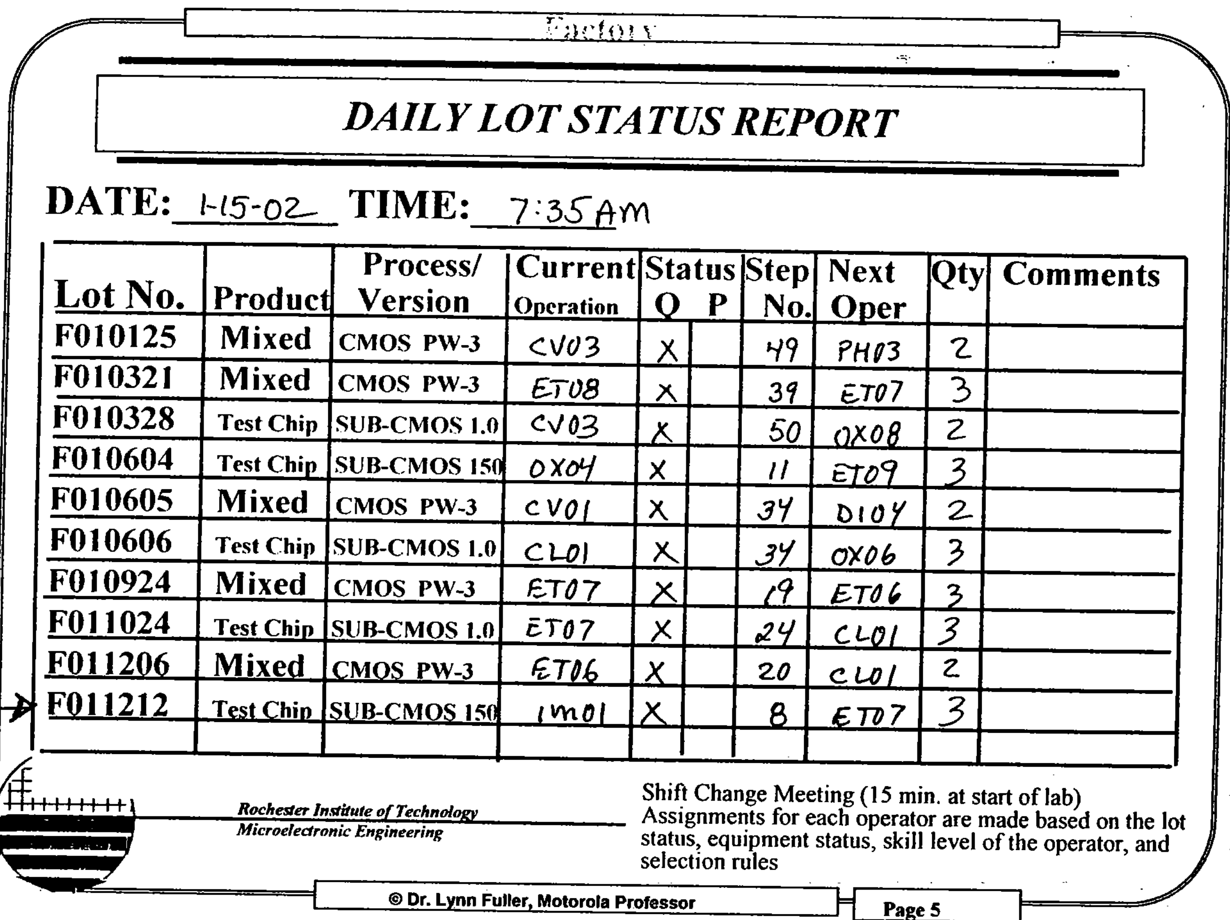
1/10/02

- Turned implanter over to James Tan after run completed.

- Both wafers looked good. Lot moved out in MESA

[signature] 1/10/02

1/15/02



Factory

DAILY LOT STATUS REPORT

DATE: 1-15-02 **TIME:** 7:35AM

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	CV03	X		49	PH03	2	
F010321	Mixed	CMOS PW-3	ET08	X		39	ET07	3	
F010328	Test Chip	SUB-CMOS 1.0	CV03	X		50	OX08	2	
F010604	Test Chip	SUB-CMOS 150	OX04	X		11	ET09	3	
F010605	Mixed	CMOS PW-3	CV01	X		34	DI04	2	
F010606	Test Chip	SUB-CMOS 1.0	CL01	X		34	OX06	3	
F010924	Mixed	CMOS PW-3	ET07	X		19	ET06	3	
F011024	Test Chip	SUB-CMOS 1.0	ET07	X		24	CL01	3	
F011206	Mixed	CMOS PW-3	ET06	X		20	CL01	2	
→ F011212	Test Chip	SUB-CMOS 150	IM01	X		8	ET07	3	

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Assigned lot F011212 @ IM01 (3 6" wafers)
P - 9.5E12 - 150keV

[signature] 1/15/02

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1/15/02

PHOSPHOROUS IMPLANT

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1/15/02 1/15/02
9:34:25

MESA
Instruction Execution

IGEXINQ S36903
QPADEV000B RIT

Lot number F011212
Instruction group . : SUB-CMOS-IM01-N-WELL 150

Type selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt Text
_ > 1.0 Include D1-D3 (see SUBNWELL.PPS)
_ 2.0 Ion Implant Phosphorous (see impt_ph.pps)
3.0 Dose = 9.5E12, Species = P31
4.0 Energy = 150 KeV
5.0 Record Energy, Dose, Set-up time, Species

- Beam set up w/ no problems. Had 70 µA of Beam current. Dialed back to 15 µA for uniformity reasons.

Energy - 150 keV
Dose - 9.5E12
Set-up time - 30 min
Species - P31

- Next step is ET07 (PR Ash)
Ashed wafers in Branson Asher
Program "EPD 6" Ash"
Provides end point detection for Ashing the resist.
- All 3 product + 4 dummy wafers ashed.
- Looked good. Moved out in ~~[illegible]~~ MESA

- Forward Power - 500W
- Reflected Power - 1W
- Time - End pt. detection
- Pressure 4472 mtorr
- O_2 4025 sccm

[signature]
1/15/02

1/17/02

- Assigned lot FD11206 @ OX04 (step 22) 2 wafers

```
1/17/02                          MESA                    IGMSINQ    S36801
9:24:33              Instruction Group Inquiry           QPADEV000R   RIT

Type information.  Then Enter.
  1=Display document, 5=Display detail

  Plant . . . . . . . . :   RIT
  Instruction group . .     CMOS-OX04-FIELD         CMOS OX04 GROW FIELD OXIDE
    Revision . . . . . .    3.0

  Opt Subgroup   Text
                  1.0 Include D1-D3
   _              2.0 Use resource FURNACE01 BRUCE TUBE 01 (SEE fieldox.pps)
   _              3.0 Xox desired = 1um
   _              4.0 See SPC chart for operation (field_ox.pps)-execute step
   _              5.0 XRF warm up recipe 888, check gas & hydrogen supply
   _              6.0 When furnace stabilizes at 800 C abort 888
   _              7.0 XRF 10,000 A wet O2 recipe 410, load wafers, press start
   _                  P/P 800C, RU 30min, 210 min soak wet O2 1100C, RD 60 min
   _              8.0 When wafers complete, abort 410 and XRF idle recipe 999
   _              9.0 Total time is approx. 5 hrs, be available at end
   _                                                                    More...
F3=Exit   F4=Prompt   F5=Refresh   F10=View 2   F12=Cancel
```

```
1/17/02                          MESA                    IGMSINQ    S36801
9:30:07              Instruction Group Inquiry           QPADEV000K   RIT

Type information.  Then Enter.
  1=Display document, 5=Display detail

  Plant . . . . . . . . :   RIT
  Instruction group . .     CMOS-OX04-FIELD         CMOS OX04 GROW FIELD OXIDE
    Revision . . . . . .    3.0

  Opt Subgroup   Text
                 10.0 Measure actual Xox on D2 in test sites
   _             11.0 Record 3-zone temp, soak time, thickness
   _
```

Power point sheets would not come up in MESA
others had same problem

[signature] 1/17/02

1/15/02

1/15/02 10:27:25	**MESA** Instruction Group Inquiry	IGMSINQ S36801 QPADEV000B RIT

Type information. Then Enter.
1=Display document, 5=Display detail

Plant . . . . : **RIT**
Instruction group . . **SUB-CMOS-ET07-N-WELL** SUB-CMOS ET07 STRIP RESIST
Revision 150

Opt	Subgroup	Text
_		1.0 Include D1-D3
_		2.0 Strip Photoresist in BRANSON Asher,(see asher.pps)
_		3.0 USE RECIPE 6" NORMAL ASH
_		4.0 Record Forward/Reflected Power, Time
_		5.0 Inspect wafers and record comments (see sub_stp9.ppt)

Instructions for Ash step

1/15/02

1/17/02

Factory

DAILY LOT STATUS REPORT

DATE: 1-17-02 **TIME:** 7:30am

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	ET10	X		51	ET07	2	
F010321	Mixed	CMOS PW-3	IM01	X		42	ET07	3	
F010328	Test Chip	SUB-CMOS 1.0	CV03	X		50	OX08	2	
F010604	Test Chip	SUB-CMOS 150	ET09	X		12	IM01	3	
F010605	Mixed	CMOS PW-3	CV01	X		34	DI04	2	
F010606	Test Chip	SUB-CMOS 1.0	CV01	X		36	DI04	3	
F010924	Mixed	CMOS PW-3	OX04		X	22	ET09	3	
F011024	Test Chip	SUB-CMOS 1.0	OX04	X		26	ET09	3	
F011206	Mixed	CMOS PW-3	OX04	X		22	ET09	2	Brian
F011212	Test Chip	SUB-CMOS 150	OX04	X		11	ET09	3	

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1/17/02

1/17/02

Recipe 410 → 10,000 Å Wet Field Oxide

	Step	Time (min)	Temp (C)	Gas (SLPM)	Boat (inch/min)
0	Boat Out	0	800	$N_2 = 5$	Out = 10
1	Push In	12	800	$N_2 = 10$	In = 15
2	Ramp Up	30	1100	$N_2 = 5$	
3	O_2 Flood	5	1100	$O_2 = 5$	
4	O_2 Soak	3hr 30min	1100	$O_2 = 2$, $H_2 = 3.6$	
5	N_2 Purge	5	1100	$N_2 = 15$	
6	Ramp Down	55	25	$N_2 = 5$	
7	Pull Out	15	25	$N_2 = 10$	Out = 10

- Wafers run in tube 1. Will be done @ ~ 4pm. Will come back after class.

- Process improvement → Auto Focus errors on GCA stepper

~~EXEC~~ To Login [10, 1]

password secret

ListF → List files

EXEC[10,1]CMOSMIX\1

EDIT CMOSMIX

Return down to pass desired

CMOSMIX\1 Good

CMOSMIX\2 1 ~~2L~~, 2nd, 3rd

~~2L~~ 3L

~~3L~~

[signature] 1/17/02

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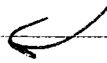
1/17/02

* END OF TEST *

REFR INDEX = 1.45
Sample ID:

NUMBER	THICKNESS
1	12119 A
2	12117 A
3	12149 A

Field oxide thickness



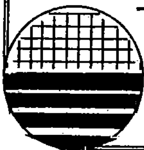
B. J. Miga 1/17/02

1/22/02

EMCR 650 Introduction

IMPROVEMENT PROJECTS

Nitride Etch Endpoint Detection - Robin
Poly Etch Endpoint Detection - Frank
Oxide Etch Endpoint – Erik D.
150 A gate Oxide Measurements – Matt Shepard
How to Measure Poly, Nitride, LTO, Oxide, Thickness - Ricky
Canon Stepper Job for Factory - Vim
NEW MESA SPC Charts for Sub-CMOS - Samantha
MESA Pictures of Sub-CMOS die at selected steps - Eric
Make all factory processes fit in 2.5 hour lab time if possible – David
Remove all auto focus failures – Brian Miga
- Luc
- James
- Chris
- Sean
- Neal
- Brian
- James
- VJ



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Microelectronic Engineering

12-13-01

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Page 13

B. J. Miga 1/22/02

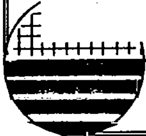
1/22/02

Factory

DAILY LOT STATUS REPORT

DATE: 1-22-02 **TIME:** 8:00am

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
→F010125	Mixed	CMOS PW-3	PH03	X		56	ET05	2	Brian
F010321	Mixed	CMOS PW-3	IM01	X		45	ET07	3	
F010328	Test Chip	SUB-CMOS 1.0	OX08	X		51	ET00	2	
F010604	Test Chip	SUB-CMOS 150	ET06	X		15	CL01	2	
F010605	Mixed	CMOS PW-3	ET06	X		36	DE01	2	
F010606	Test Chip	SUB-CMOS 1.0	ET06	X		38	DE01	3	
F010924	Mixed	CMOS PW-3	OX04	X		26	IM01	3	
F011024	Test Chip	SUB-CMOS 1.0	OX04	X		29	PH03	3	
F011206	Mixed	CMOS PW-3	CL01	X		25	OX04	2	
F011212	Test Chip	SUB-CMOS 150	IM01	X		13	OX06	3	



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– Assigned lot
F010125 @ PH03 Step 56 (Metal Lith.)

```
1/22/02                    MESA                 IGEXINQ     S36903
9:27:54             Instruction Execution       QPADEV000N     RIT

Lot number . . . . . .    F010125
Instruction group  . :    CMOS-PH03-METAL       3.0

 ype selections.  Then Enter.
  1=Display document    2=Execute step    3=Rework-to step

  Opt   Text
   _ >  1.0 Include D1-D3 (General Instructions) (see lvl9phot.pps)
        2.0 Locate correct masks for this project
        3.0 Record device and test mask no., move-in
   _    4.0 Use Trac coat program 7,3,3 (GCA1006) (see 733_722.pps)
        5.0 Coat Photoresist on D1-D3, softbake
        6.0 Expose on Stepper, level 9 maskset, METAL ONE
        7.0 Use correct stepper jobname\9T,9D,OPEN
        8.0 Use integrate mode, exposure units =.4, record as time
        9.0 1 Exposure unit = 250 mW/cm**2
   _    10.0 Develop on Trac program 7,2,2 - postbake 120C (see 733
        11.0 Inspect and record comments
```

1/22/02

1/22/02
9:27:54

MESA
Instruction Execution

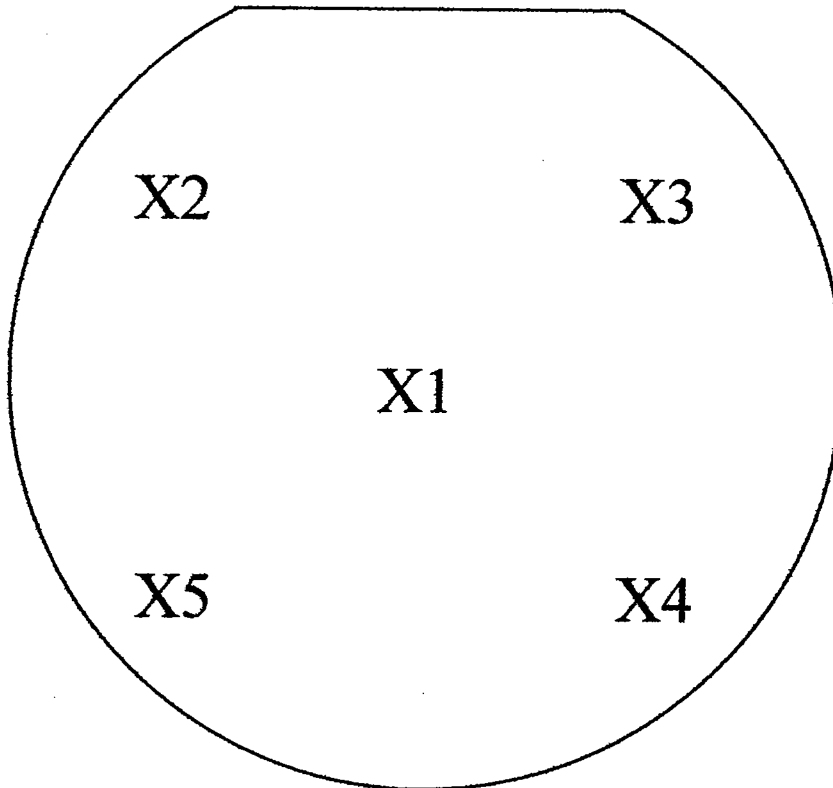
IGEXINQ S36903
QPADEV000N RIT

Lot number F010125
Instruction group . : CMOS-PH03-METAL 3.0

Type selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt	Text
	12.0 Record Stepper ID, E, t, Focus, T
_	13.0 Measure X and Y overlays in 5 locations (see xyloc.pps)
_	14.0 Measure 4um CD on Leitz microscope (see alverncd.pps)
_	15.0 Check Ring oscillator area (see s57et05.pps)

FACTORY X AND Y OVERLAY MEASUREMENT LOCATIONS

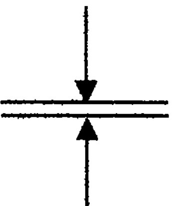


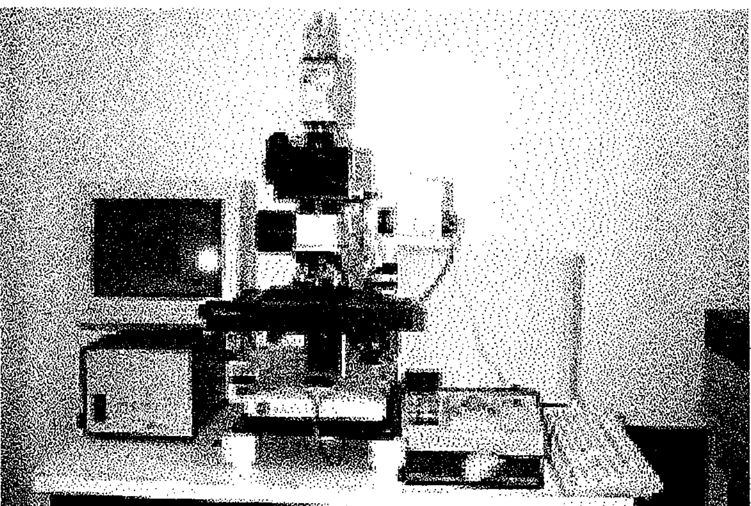
1/22/02

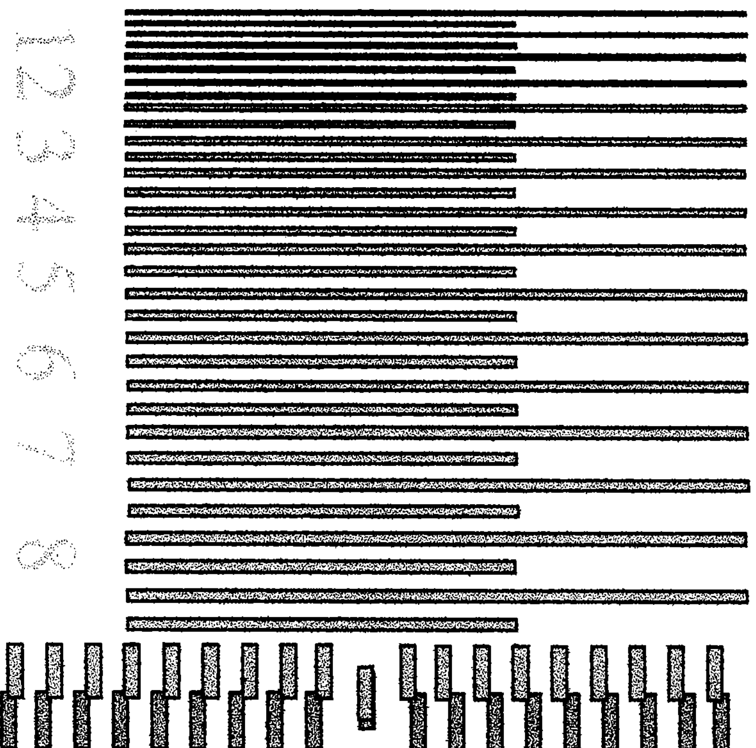
1/22/02

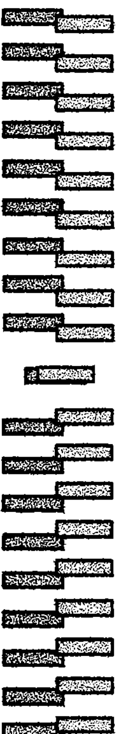
ALIGNMENT VERNIERS AND CRITICAL DIMENSION (CD) STRUCTURES

4 µm CD









[signature] 1/22/02

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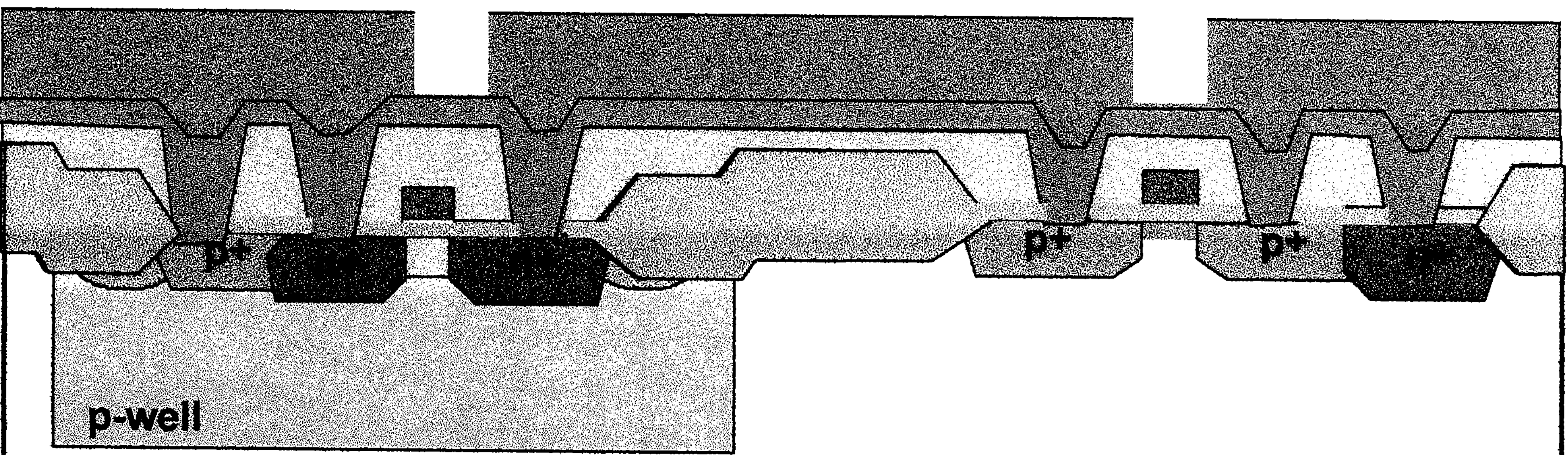
Made in USA

1/22/02

LEVEL 9 PHOTO - METAL

NMOSFET

PMOSFET



1/22/02

According to MESA, Al thickness is 4300Å

Factory MASK : MIXCMOS3

+ NO GCA wafertrac
Coat by hand.

Step 1 - Dehydration Bake
115°C for 2 min

Step 2 - HMDS Prime
Dispense small amount w/ pipet
Spin 4500 RPM for 60 sec

Step 3 - Apply Resist
Dispense Shipley 812
Spin 4500 RPM for 60 sec.

Step 4 - Soft Bake
90°C for 60 sec

Step 5 - Expose
- GCA Stepper
- Level 9, MASK MIXCMOS3
- Stepper Job : EXEC [10,1] CMOSMIX\9,OPEN
- Exposure
- Dose

- Must also load a blank mask for 5 test locations
E =
t = .2 sec
Focus = 250
T =

[signature] 1/22/02

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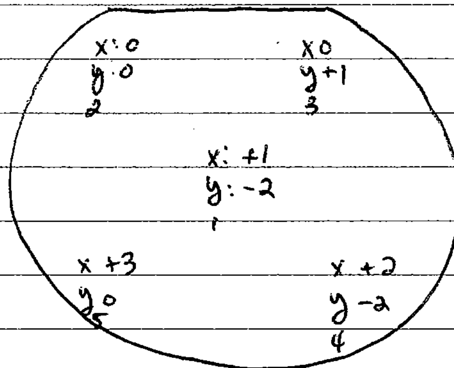
1/22/02 Step 6 - PEB
115°C for 45 sec

Step 7 - Develop
Develop for 45 sec. by hand
Rinse w/ DI water
Inspect.
- 45 sec develop looks Good.
- very minimal overlay error

- Step 8 - Hard Bake
120°C for 60 sec.

- Measure Overlay in 5 locations (Diag. on page 40)



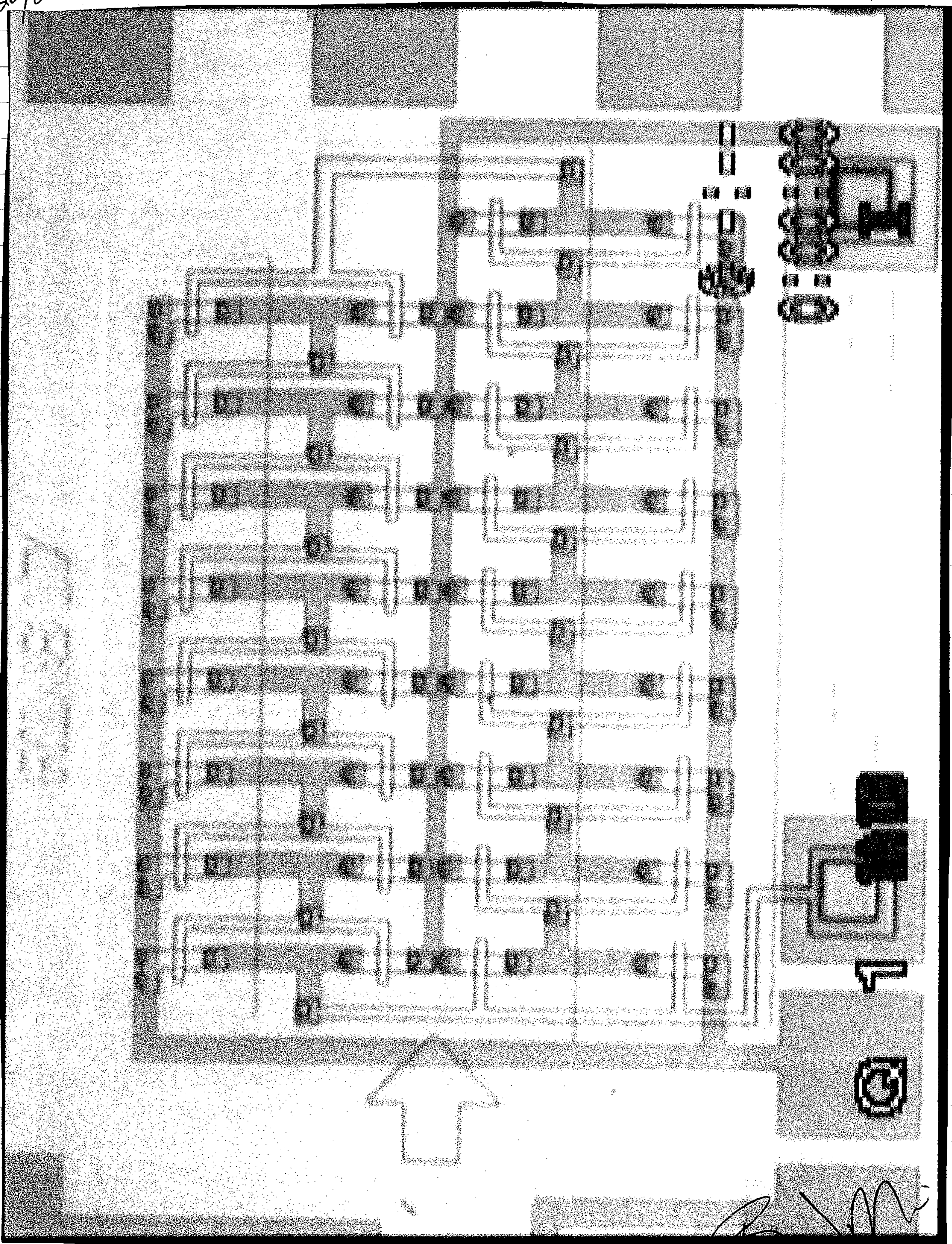
- Measure 4μm CD
Measurement on Leitz shows ~ 4μm for the Lines on interest.

- Ring oscillator checked Looks Good. Example printout on next page.

- Lot moved on to Etch.

[signature]
1/22/02

1/20/02



1/24/02

Assigned lot F010606 @ Step 40 (PH03) 3 wafers

Get to use new Photo Trac!!

Factory

DAILY LOT STATUS REPORT

DATE: 1-24-02 **TIME:** 8:18am

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	ET07	X		58	SI01	2	was done
F010321	Mixed	CMOS PW-3	OX08	X		48	CV03	3	
F010328	Test Chip	SUB-CMOS 1.0	ET10	X		52	PH03	2	
F010604	Test Chip	SUB-CMOS 150	CV02	X		18	PH03	2	
F010605	Mixed	CMOS PW-3	ET08	X		39	ET07	2	
→ F010606	Test Chip	SUB-CMOS 1.0	PH03	X		40	ET08	3	Brian
F010924	Mixed	CMOS PW-3	PH03	X		28	IM01	3	
F011024	Test Chip	SUB-CMOS 1.0	PH03	X		30	IM01	3	
F011206	Mixed	CMOS PW-3	IM01	X		27	PH03	2	
F011212	Test Chip	SUB-CMOS 150	OX06	X		14	ET06	3	

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```
1/24/02                        MESA                      IGEXINQ
9:21:38                 Instruction Execution           QPADEV000B

Lot number . . . . . .   F010606
Instruction group  . :   SUB-CMOS-PH03-POLY   1.0

'pe selections.  Then Enter.
 1=Display document    2=Execute step    5=Display detail

 Opt  Text
  _   1.0 Include D1-D3 (see sub_pho5.pps)
  _   2.0 Locate correct mask for this project
  _   3.0 Record device and test mask no., move-in
  _   4.0 Use Trac coat program 7,3,3 on Wafertrac
  _   5.0 Coat Photoresist on D1-D3, softbake
  _   6.0 Expose on Stepper, level 5 maskset, POLY
  _   7.0 Use correct stepper jobname (10,1)SUBCMOS.NEW\5
  _   8.0 Use integrate mode, exposure units =0.4, record as time
  _   9.0 One Exposure unit = 250 mj/cm**2
  _   10.0 PEB, develop by hand, 30 second develop CD26, hardbake
  _   11.0 Inspect and record comments (*place picture here)
```

1/24/02

1/24/02

1/24/02
9:21:38

MESA
Instruction Execution

IGEXINQ S36902
QPADEV000B RIT

Lot number . . . . . . : F010606
Instruction group . : SUB-CMOS-PH03-POLY 1.0

pe selections. Then Enter.
1=Display document 2=Execute step 5=Display detail

Opt	Text
_	12.0 Record Stepper ID, E, t, Focus, T, X and Y-overlays
_	13.0 Measure 2um CD on Leitz microscope

New SVG Track is very nice:

- Run program 1 on both controlers for the coat trac.
- Recieve cassette must be placed on tool first
- Hit Start.
- Process is:
  - 30 second Bake 140°C
  - HMDS Vapor Prime (20 sec)
  - Short bake
  - Cool plate for 30s
  - Spin on Resist.
  - Soft bake 90°C 60 sec

- Wafers Coated w/no problem

- Exposed on GCA
  "EXEC [10,1]SUBCMOS.NEW\5, open"

ID: Stepper 01
E: 250
t: .4
Focus: 250
MASK ID = SUBCMOS2

[signature] 1/24/02

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VP8480 Rev. 11-6-98 Made in USA

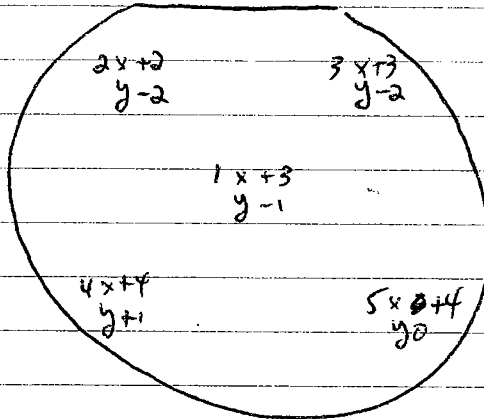
1/24/02

- Develop:

Run Program 1 on SVG Track

- Ran w/ no problems

X-y overlay



CD measure ~ 2μm on leits

- Everything looks good move out lot.

1/29/02

- Assigned Lot F010328 at ET07 (Step 55)

1/29/02
9:19:19

MESA
Instruction Execution

IGEXINQ S36903
QPADEV000B RIT

Lot number F010328
Instruction group . : SUB-CMOS-ET07-N+-DS 1.0

ype selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt Text
_ > 1.0 Include D1-D3
_ 2.0 Strip Photoresist in BRANSON Asher, (see BRANSON.pps)
3.0 USE RECIPE 4" HARD ASH
4.0 Record Forward/Reflected Power, Time

1/29/02

1/29/02

Factory

DAILY LOT STATUS REPORT

DATE: 1-29-02 **TIME:** 8:00am

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	TE01	X		60	TE02	2	
F010321	Mixed	CMOS PW-3	CV03	X		49	PH03	3	
F010328	Test Chip	SUB-CMOS 1.0	ET07	X		55	PH03	2	Brian
F010604	Test Chip	SUB-CMOS 150	PH03	X		19	ET09	2	
F010605	Mixed	CMOS PW-3	IM01	X		42	ET07	1	
F010606	Test Chip	SUB-CMOS 1.0	PH03	X		43	IM01	3	
F010924	Mixed	CMOS PW-3	CL01	X		32	OX06	3	
F011024	Test Chip	SUB-CMOS 1.0	CL01	X		34	OX06	3	
F011206	Mixed	CMOS PW-3	ET07	X		30	ET06	2	
F011212	Test Chip	SUB-CMOS 150	CL01	X		16	OX05	3	

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- Used 4" Hard Ash recipe.
- 2 wafers in lot
- RF FWD 500
  RF Refl 1
  Time 2min
- Lot moved out
  NOTE: wafers looked really bad. Looks like someone licked their fingers and touched the wafers

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1/29/02

Branson Plasma Resist Stripper

4" wafers and 6" wafers

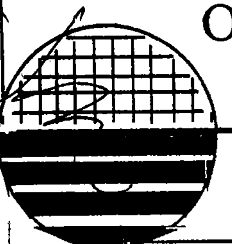
Recipes Include

- 4" normal ash
- 4" hard ash
- 6" normal ash
- 6" hard ash

Hard ash is used after ion implant

IMPROVEMENT PROJECTS

Nitride Etch Endpoint Detection - Robin
Poly Etch Endpoint Detection - Frank
Oxide Etch Endpoint – Erik D.
150 A gate Oxide Measurements – Matt Shepard
How to Measure Poly, Nitride, LTO, Oxide, Thickness - Ricky
Canon Stepper Job for Factory - Vim
NEW MESA SPC Charts for Sub-CMOS - Samantha
MESA Pictures of Sub-CMOS die at selected steps - Eric
Make all factory processes fit in 2.5 hour lab time if possible – David
Remove all auto focus failures – Brian Miga
MESA Corrections for CMOS PW-3 Process- Luc
Ion Implant for Poly Doping instead of Spin-on Dopant- James T.
Hot Phosphoric Acid Removal of Nitride- Chris
Cpk Improvement for 4 um CD and Kooi Oxide Thickness- Sean
MESA Corrections for SUB-CMOS 1.0 Process- Neal
MESA Corrections for SUB-CMOS 150 Process- Brian
- James G.
Out of Control Action Plans - VJ



1/29/02

Doing Next Step for lot F010328 (PH03)

```
     1/29/02                            MESA                       IGEXINQ    S36903
     9:54:05                    Instruction Execution             QPADEV000R   RIT

 Lot number . . . . . .   F010328
 Instruction group  . :   SUB-CMOS-PH03-P+-DS  1.0

 Type selections.  Then Enter.
   1=Display document   2=Execute step   3=Rework-to step

   Opt  Text
    _ > 1.0 Include D1-D3 (see sub_pho9.pps)
        2.0 Locate correct masks for this project (SUBCMOS3)
        3.0 Record device and test mask no., move-in
        4.0 Use Trac coat program 7,3,3 on Wafertrac
        5.0 Coat Photoresist on D1-D3, softbake
        6.0 Expose on Stepper, level 9 maskset, P+D/S
        7.0 Use correct stepper jobname (10,1)SUBCMOS.NEW\9
        8.0 Use integrate mode, exposure units = 0.4 record as time
        9.0 1 Exposure unit = 250 mW/cm**2
        10.0 Develop on Trac program 7,2,2 - postbake 120C
        11.0 Inspect and record comments (*place picture here)
                                                                              More.
 F3=Exit   F10=Display current step   F11=Display groups   F24=More keys
```

```
     1/29/02                            MESA                       IGEXINQ    S36903
     9:54:05                    Instruction Execution             QPADEV000R   RIT

 Lot number . . . . . .   F010328
 Instruction group  . :   SUB-CMOS-PH03-P+-DS  1.0

 Type selections.  Then Enter.
   1=Display document   2=Execute step   3=Rework-to step

   Opt  Text
        12.0 Record Stepper ID, E, t, Focus, T, X and Y-overlays
        13.0 Measure 2um CD on Leitz Microscope
```

- Coat on trac using same recipe as normal (#1)
- Expose on Stepper as normal
  ID - Stepper 01
  E - 250
  t - .4s
  Focus - 250
  T -

1/29/02

- Exposed ok
- Developed on SVG Track using process described before.

- Inspection revealed an error with the Stepper Job. This was level 9, but coordinates were set up for level 5. Mask is like:

5	6
9	7

- PR Ashed and the 2 wafers were reworked

- Everything went smooth
- Correct mask part used (corrected stepper job)
- x : +2
  y : 0

- Move out.

[signature] 1/29/02

1/31/02

- Originally assigned Lot F010604
  - Lot is to be scrapped due to previous mis-processing
  - Will use time to work on process improvement project

[signature] 1/31/02

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VP5840 Rev. 01-6/98 Made in USA

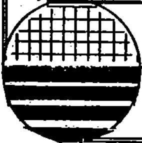
1/31/02

Factory

DAILY LOT STATUS REPORT

DATE: 1-31-02 **TIME:** 8:00am

	Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
✓	F010125	Mixed	CMOS PW-3	TE01	X		60	TE02	2	
✓	F010321	Mixed	CMOS PW-3	ET10	X		51	ET07	3	
✓	F010328	Test Chip	SUB-CMOS 1.0	IM01	X		57	ET07	2	
✓	F010604	Test Chip	SUB-CMOS 150	ET09	X		20	ET07	2	~~Brian~~
✓	F010605	Mixed	CMOS PW-3	IM01	X		42	ET07	1	
✓	F010924	Mixed	CMOS PW-3	CV01	X		34	DI04	3	
✓	F011024	Test Chip	SUB-CMOS 1.0	CV01	X		36	DI04	3	
✓	F011206	Mixed	CMOS PW-3	OX06	X		33	CV01	2	
✓	F011212	Test Chip	SUB-CMOS 150	CV02	X		18	PH03	3	
	F020129	Test Chip	SUB-CMOS 1.0	OX05	X		4	CV02	3	
	F020201	Test chip	SUB-CMOS 150	ID01	X		1	DE01	3	



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GCA Stepper - Auto Focus Failures
- CMOS MIX process (9 Levels)
  - Level 1
    AFF@: Row Column
    NONE
  - Level 2
    AFF@: 1 1
    1 2
    1 4
    Edited file - Try again
    NONE

[signature] 1/31/02

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1/31/02

CMOSMIX AFF — Row — Column

Level 3

Row	Column
1	3
1	5
2	1
3	1
5	1

Edit File, Run again

Row	Column
1	1st Die
2	LHS
3	LHS

Edit File, Run again

Row	Column
1	LHS

Removed all of Row 1

Worked

- Going to remove all Row 1 exposures. They are too close to the flat anyway. Will do for all levels

Level 4 — Row — Column

Worked Good

Level 5 - worked

Level 6

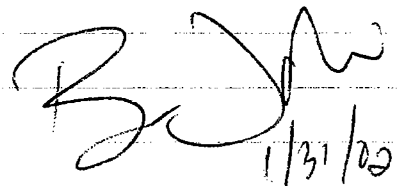
Row	Column
2	LHS
3	LHS

worked after edit

Level 7

Row	Column
2	LHS
3	LHS
*5	LHS

worked after edit



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1/31/02

Level 8: Row 2 Lits

Worked after edit

Level 9: Worked w/ no problems

CMOSMIX is Done!

Auto-Focus Failures should be gone on Mixed cmos now.
- Very bad wafers may still error on the edges
- tests were done w/ dummy wafer (clean) and blank mask.

[signature] 1/31/02

2/5/02

DAILY LOT STATUS REPORT

DATE: 2-5-02 TIME: 8:30 AM

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	TE01	X		60	TE02	2	
F010321	Mixed	CMOS PW-3	ME01	X		55	PH03	3	
F010328	Test Chip	SUB-CMOS 1.0	OX08	X		60	CV03	2	
→ F010605	Mixed	CMOS PW-3	PH03	X		44	IM01	1	
F010924	Mixed	CMOS PW-3	ET06	X		36	DE01	3	
F011024	Test Chip	SUB-CMOS 1.0	D104	X		37	ET06	3	
F011206	Mixed	CMOS PW-3	CV01	X		34	D104	2	
F011212	Test Chip	SUB-CMOS 150	CV02	X		18	PH03	3	
F020129	Test Chip	SUB-CMOS 1.0	ET09	X		7	IM01	3	
F020202	Test Chip	SUB-CMOS 150	CV02	X		5	PH03	3	
F020204	Mixed	CMOS PW-3	OX04	X		4	PH03	3	

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2/5/02
- Assigned lot F 010605 at step 44 (PH03) 1 wafer
(N+ D/S)

- SVG track was off when I came into lab. Turned on and waiting for hot plates to get up to temp.

```
2/05/02                    MESA                 IGEXINQ     S36903
9:21:03            Instruction Execution        QPADEV000F   RIT

Lot number . . . . . .   F010605
Instruction group  . :   CMOS-PH03-N+-DS      3.0

Type selections.  Then Enter.
  1=Display document    2=Execute step    3=Rework-to step

  Opt  Text
   _ > 1.0 Include D1-D3 (General Instructions) (see lvl7phot.pps)
       2.0 Locate correct masks for this project
       3.0 Record device and test mask no., move-in
       4.0 Use Trac coat program 7,3,3 (GCA1006) (see 733_722.pps)
   _   5.0 Coat Photoresist on D1-D3, softbake
       6.0 Expose on Stepper, level 7 maskset, N+D/S
       7.0 Use correct stepper jobname\7T,7D,OPEN
       8.0 Use integrate mode, exposure units =.4, record as time
       9.0 1 Exposure unit = 250 mW/cm**2
       10.0 Develop on Trac program 7,2,2 - postbake 120C (see 733_
   _   11.0 Inspect and record comments
                                                                More..
F3=Exit   F10=Display current step   F11=Display groups   F24=More keys
```


```
2/05/02                    MESA                 IGEXINQ     S36903
9:21:03            Instruction Execution        QPADEV000F   RIT

Lot number . . . . . .   F010605
Instruction group  . :   CMOS-PH03-N+-DS      3.0

Type selections.  Then Enter.
  1=Display document    2=Execute step    3=Rework-to step
```


```
  Opt  Text
       12.0 Record Stepper ID, E, t, Focus, T
   _   13.0 Measure X and Y overlay in 5 locations (see xyloc.pps)
   _   14.0 Measure 4um CD on Leitz microscope (see alverncd.pps)
```

2/5/02

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2/5/02

- This lot processed same as last several photo lots I have done.

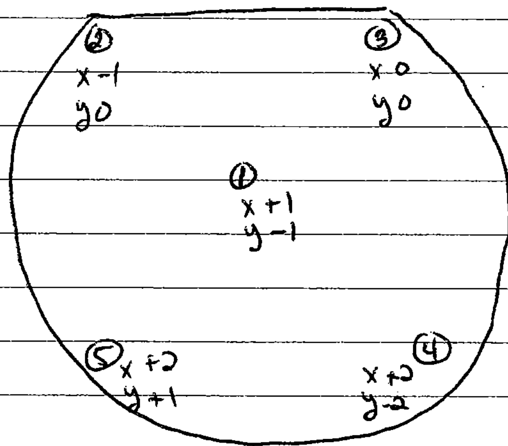
- Wafer was stuck in HMDS Vapor prime chamber. Removed wafer and track worked fine.

- Exposed with MASK MIXCMOS2 Level 7

- ID Stepper01
- E - 250
- t - .4s
- Focus: 250

- Wafer looked horrible under microscope. Appeared to be overdeveloped. Most likely not enough resist on wafer since dummies looked bad from track. Wafer reworked, Looked much better

x-y overlay



CD ~ 3.8μm for 4μm CD

Lot moved out

[signature]
2/5/02

2/5/02

More Process Improvement

Subju CMOS on GCA
- Remove all Row 7

	Row	Column
Level 1	none	
Level 2	none	
Level 3	2	2
	3	1
	Fixed	
~~Level 4~~	~~Fixed~~	
Label 5	Fixed	
Level 6	Fixed	
Level 7	2	LHS
	3	LHS
	Fixed	

[signature] 2/5/02

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Factory

DAILY LOT STATUS REPORT

DATE: 2-7-02 TIME: 8:00 am

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	TE01	X		60	TE02	2	
F010321	Mixed	CMOS PW-3	PH03	X		56	ET05	3	
F010328	Test Chip	SUB-CMOS 1.0	CV03	X		61	PH03	2	
F010605	Mixed	CMOS PW-3	IM01	X		45	ET07	1	
F010924	Mixed	CMOS PW-3	PH03	X		38	ET08	3	
F011024	Test Chip	SUB-CMOS 1.0	ET06	X		38	DE01	3	
F011206	Mixed	CMOS PW-3	CV01	X		34	DI04	2	
F011212	Test Chip	SUB-CMOS 150	CV02		X	18	PH03	3	measure results
F020129	Test Chip	SUB-CMOS 1.0	IM01	X		8	ET07	3	
F020202	Test Chip	SUB-CMOS 150	CV02		X	5	PH03	3	not done
F020204	Mixed	CMOS PW-3	PH03	X			ET06	3	

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2/7/02

60

2/7/02

- Assigned F010321 at step 56 (PH03)

2/07/02 9:20:28

MESA
Instruction Execution

IGEXINQ S36903
QPADEV000B RIT

Lot number F010321
Instruction group . : CMOS-PH03-METAL 3.0

ype selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt Text
> 1.0 Include D1-D3 (General Instructions) (see lvl9phot.pps)
2.0 Locate correct masks for this project
3.0 Record device and test mask no., move-in
4.0 Use Trac coat program 7,3,3 (GCA1006) (see 733_722.pps)
5.0 Coat Photoresist on D1-D3, softbake
6.0 Expose on Stepper, level 9 maskset, METAL ONE
7.0 Use correct stepper jobname\9T,9D,OPEN
8.0 Use integrate mode, exposure units =.4, record as time
9.0 1 Exposure unit = 250 mW/cm**2
10.0 Develop on Trac program 7,2,2 - postbake 120C (see 733_
11.0 Inspect and record comments

More..

F3=Exit F10=Display current step F11=Display groups F24=More keys

2/07/02 9:20:28

MESA
Instruction Execution

IGEXINQ S36903
QPADEV000B RIT

Lot number F010321
Instruction group . : CMOS-PH03-METAL 3.0

ype selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt Text
12.0 Record Stepper ID, E, t, Focus, T
13.0 Measure X and Y overlays in 5 locations (see xyloc.pps)
14.0 Measure 4um CD on Leitz microscope (see alverncd.pps)
15.0 Check Ring oscillator area (see s57et05.pps)

- Coated on SVG Track as normal. No problems
- Exposed on GCA. No problems

[signature]
2/7/02

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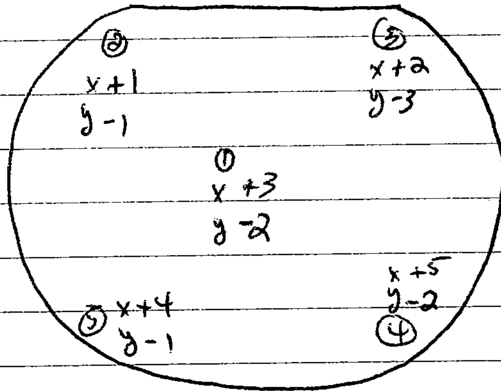
2/7/02

Developed w/ no problem

Overlay:



Lot moved to Al Etch.

Finishing Process Improvement

Sub Cmos

Level 8 - worked

Level 9 - worked

Level 10 - worked

Level 11 = row 2 LHS
row 3 LHS
Fixed

DONE!

2/7/02

2/14/02

2/14/02
9:16:51

MESA
Instruction Execution

IGEXINQ S36903
QPADEV000F RIT

Lot number F010328
Instruction group . : SUB-CMOS-PH03-CC 1.0

ype selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt Text
_ > 1.0 Include D1-D3 (see sub_pcc)
2.0 Locate correct masks for this project (SUBCMOS3)
3.0 Record device and test mask no., move-in
4.0 Use Trac coat program 7,3,3 on Wafertrac
5.0 Coat Photoresist on D1-D3, softbake
6.0 Expose on Stepper, level 10 maskset, CONTACTS
7.0 Use correct stepper jobname (10,1)SUBCMOS.NEW\10
8.0 Use integrate mode, exposure units =0.4 record as time
9.0 1 Exposure unit = 250 mJ/cm**2
10.0 Develop on Trac program 7,2,2 - postbake 120C
11.0 Inspect and record comments (*place picture here)

2/14/02
9:16:51

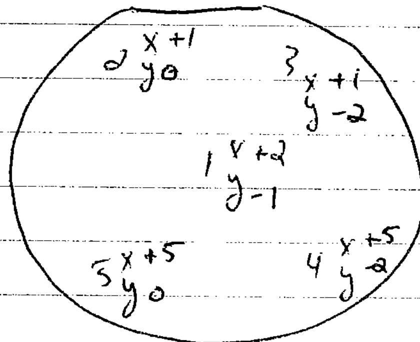
MESA
Instruction Execution

IGEXINQ S36903
QPADEV000F RIT

Lot number F010328
Instruction group . : SUB-CMOS-PH03-CC 1.0

ype selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt Text
12.0 Record Stepper ID, E, t, Focus, T, X and Y-overlays
13.0 Measure 2um CD on Leitz microscope



CD on Leitz ~ 2.3um

2/14/02

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2/14/02

Assigned lot F010328 Step 62 (PH03 - Level 10 Photo)

- Contact cut (2 wafers)

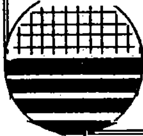
- the wafers look horrible! bad non-uniformities and evidence of mishandling.

Factory

DAILY LOT STATUS REPORT

DATE:________ TIME:________

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	TE01	X		60	TE02	2	
F010321	Mixed	CMOS PW-3	TE01	X		60	TE02	3	
→ F010328	Test Chip	SUB-CMOS 1.0	PH03	X		62	ET10	2	
F010605	Mixed	CMOS PW-3	OX08		X	48	CV03	1	
F011024	Test Chip	SUB-CMOS 1.0	ET08		X	41	ET07	3	
F011206	Mixed	CMOS PW-3	PH03	X		38	ET08	2	
F011212	Test Chip	SUB-CMOS 150	PH03		X	19	ET09	3	
F020129	Test Chip	SUB-CMOS 1.0	OX04	X		12	IM01	3	
F020202	Test Chip	SUB-CMOS 150	CV02	X		5	PH03	3	
F020204	Mixed	CMOS PW-3	ET06	X		6	IM01	3	
F020213	Mixed	CMOS PW-3	CL01	X		3	OX04	3	



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Page 5

- Coated on track, no problems

- Exposed on GCA Stepper. (.2 sec exp.)
  Reticle fork 'B' having problems w/ vac. sense.
  told tech. about problem
  Exposure went ok otherwise.

- Developed on SVG Track

[signature] 2/14/02

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ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

EMCR 631
Microelectronics Manufacturing I

Priya Rampersaud

Professor: Dr. Lynn Fuller

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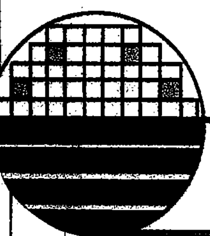
Student Run IC Factory at RIT

SUB-CMOS PROCESS

CMOS SC8 One level metal, SUBμ twin-well CMOS process

1. ID01
2. DE01
3. CL01
4. OX05--- pad oxide
5. CV02
6. PH03 –1- n well, open
7. ET09
8. IM01 – n-well
9. ET07
10. CL01
11. OX04 – well oxide
12. ET09
13. IM01 – p-well
14. OX06 – well drive
15. ET06
16. CL01
17. OX05 – pad oxide
18. CV02
19. PH03 – 2 - Active
20. ET09
21. ET07
22. PH03 – 3 - p-well stop
23. IM01- stop
24. ET07
25. CL01
26. OX04 - field
27. ET09
28. ET06
29. OX04 - Kooi
30. PH03 – 4 - PMOS Vt Adjust
31. IM01 - Vt
32. ET07
33. ET06
34. CL01
35. OX06 - gate
36. CV01
37. DI04 - dope poly Si
38. PH03 – 5 – poly, open
39. ET08
40. ET07
41. PH03 – 6 - n-LDD, open
42. IM01
43. ET07
44. PH03 – 7 - p-LDD
45. IM01
46. ET07
47. CL01
48. CV03
49. OX08 -- LTO Densify Anneal
50. ET10
51. PH03 – 8 - N+D/S, open
52. IM01 – N+D/S
53. ET07
54. PH03 – 9 P+ D/S
55. IM01 – P+ D/S
56. ET07
57. CL01
58. OX08 – DS Anneal
59. CV03 – LTO
60. PH03 – 10 CC, open
61. ET10
62. ET07
63. CL01
64. ME01
65. PH03 -11- metal, open
66. ET05
67. ET07
68. SI01
69. TE01
70. TE02
71. TE03
72. TE04



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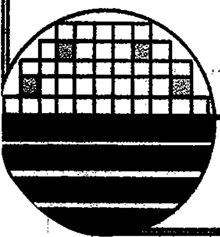
CMOS PW-3 AND PW-4 PROCESS

SDFCMOS PW-3 One level metal, p-well CMOS process used for analog devices:

1. ID01	14. PH03 -2- active	27. IM01	40. ET07	53.DE01
2. DE01	15. ET09	28. PH03 -4- nmos Vt	41. PH03 -6- p+ D/S	54.CL01
3. CL01	16. ET07	29. IM01	42 IM01	55.ME01
4. OX04--- align	17. PH03 -3- stop	30. ET07	43 ET07	56.PH03 -9- ml
5. PH03-1--well	18. IM01	31. ET06	44 PH03 -7- n+ D/S	57.ET05
6. ET06	19. ET07	32. CL01	45 IM01	58.ET07
7. IM01	20. ET06	33. OX06 -- gate	46 ET07	59.SI01
8. ET07	21. CL01	34. CV01	47 CL01	60.TE01
9. CL01	22. OX04 -- field	35. DI04	48 OX08 -- anneal	61.TE02
10. OX06-well drive	23. ET09	36. ET06	49 CV03	62.TE03
11. ET06	24. ET06	37. DE01	50 PH03 -8- CC	SHIP
12. OX05--- pad	25. CL01	38. PH03 -5- poly	51 ET10	
13. CV02	26. OX04 -- kooi	39. ET08	52 ET07	

CMOS PW-4 Two level metal, p-well CMOS process used for the Gate Array (FIRST 49 STEPS SAME AS CMOS PW-3)

50. PH03 -8- CC	57. ET07	63. PH03 -8- CC	70. CV03	77. ET07
51. ET06	58. SI02	64. ET06	71. PH03 -10- Via	78.SI01
52. ET07	59. TE01	65. ET07	72. ET10	79.TE017
53. CL01	60. TE02	66. ME01	73. ET07	80.TE02
54. ME01	61. TE03	67. PH03 -9- ml	74. ME01	81.TE03
55. PH03 -9- metalone	62. HOLD	68. ET05	75. PH03 -11- metal 2	SHIP
56. ET05		69. ET07	76. ET05	



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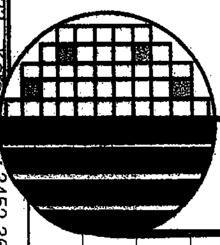
N-WELL CMOS PROCESS

CMOS NW-2 One level metal, n-well CMOS process

1. ID01
2. DE01
3. CL01
4. OX04--- align
5. PH03-1-- well
6. ET06
7. IM01
8. ET07
9. CL01
10. OX06--- well drive
11. ET06
12. OX05 -- pad
13. CV02
14. PH03 -2- active
15. ET09
16. PH03 -3-- stop
17. IM01
18. ET07
19. CL01
20. OX04
21. ET09
22. ET06
23. CL01
24. OX04
25. IM01
26. ET06
27. CL01
28. OX06
29. DE01
30. CV01
31. DI04
32. ET06
33. DE01
34. PH03 -4- poly
35. ET08
36. ET07
37. PH03 -5- p+ D/S
38. IM01
39. ET07
40. PH03 -6 n+ D/S
41. IM01
42. ET07
43. OX04
44. CV03
45. DE01
46. PH03 -7- CC
47. ET01
48. ET07
49. CL01
50. ME01
51. PH03 -8- metal
52. ET05
53. ET07
54. SI01
55. TE01
56. TE02
57. TE03

SHIP



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P. Ramperssaud

OPERATOR FLOW CHART FOR FACTORY WORK

START → Access MESA Lot Status

Find Queue Status
Step Number
Current Operation
Next Operation
Quantity

In Queue? — No → On Hold? — No → Mesa History Who Did Move-In → Contact Person Determine What To Do Next → Check Equipment Status

On Hold? — Yes → See Lab Instructor

In Queue? — Yes → On Hold? — Yes → See Lab Instructor

On Hold? — No → Check Equipment Status → Apply Lot Selection Rules → Continue A

LOT SELECTION RULES

Do Photo first
Do Oldest Lot Next
Separate Lots Current Step
Match Skill Level
Use Equipment that is Up

Continue A → Find Wafers → Prelininary Quality Check → Pass ? — No → See Lab Instructor

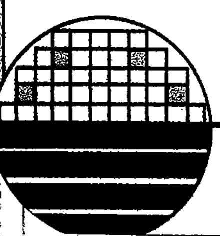
Pass ? — Yes → Do Move-In Start Run Timer → Do Work Follow MESA Instructions Exactly → Final Quality Check → Pass ? — No → See Lab Instructor

Pass ? — Yes → Stop Run Timer Move Out Record Data → Clean Up Return Wafers Return Masks → END

INITIAL QUALITY CHECK
Count Wafers
Check Picture Log Book
Think
Refer to Previous Process Step
Check MESA Move-Out Comments

BACK

FINAL QUALITY CHECK
Count Wafers
Check Picture Log Book
Think
Do Results Make Sense?



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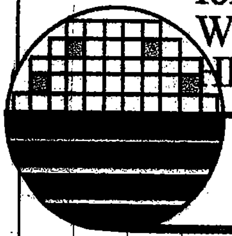
Student Run IC Factory at RIT

OPERATOR CERTIFICATION SIGNOFF SHEET

	Date/Initials for Initial Training	Date/Initials Certified
Stepper		
Wafertrack		
Asher	P.F. 12/7/01	
RCA Clean	P.F. 12/7/01	
Wet Etch		
Al Etch		
Gate Oxide		
Wet Oxide		
Well Drive		
Diffusion		
Poly		
Nitride		
LTO		
Sputter		
Poly Etch		
Nitride Etch		
4 pt Probe		
Nanospec		
Alpha Step		
SCA		
Ion Implant		
Wafer Probe		
HP-4145		



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© 6 December 2001 Dr. Lynn Fuller

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VP5840 Rev. 01-6/98 Made in USA

12/7/2001

To access MESA:

Ueserver.rit.edu → MESA BETA

username: operator

password: operator

username: student

password: nightshift

plant RIT MESA User Sign ON.

User id: operator

password: operator

@ menue choose 4

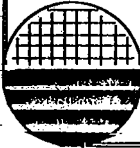
Factory Lot:

Factory

DAILY LOT STATUS REPORT

DATE: 12-7-2001 TIME: 7:30 am

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
F001205	Subμ	1.0	OX08	X		49	ET10	1	#106 Anneal
F010125	Mixed	PW3	OX06	X		33	CV01	2	#250 Gate Ox
F010321	Mixed	PW3	OX06	X		33	CV01	3	hold #250
F010328	Subμ	1.0	CL01	X		34	OX06	2	
F010604	Subμ	150	PH03		X	6	ET09	3	hold
F010605	Mixed	PW3	OX04	X		22	ET09	3	field ox #410
F010606	Subμ	1.0	ET06	X		15	CL01	3	
F010924	Mixed	PW3	OX06	X		10	ET06	3	#180 36hr well d
F011024	Subμ	1.0	ET07	X		9	CL01	3	
F011206	Mixed	PW3	OX04	X		4	PH03	3	#350 5000Å



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Shift Change Meeting (15 min. at start of lab)
Assignments for each operator are made based on the lot status, equipment status, skill level of the operator, and selection rules

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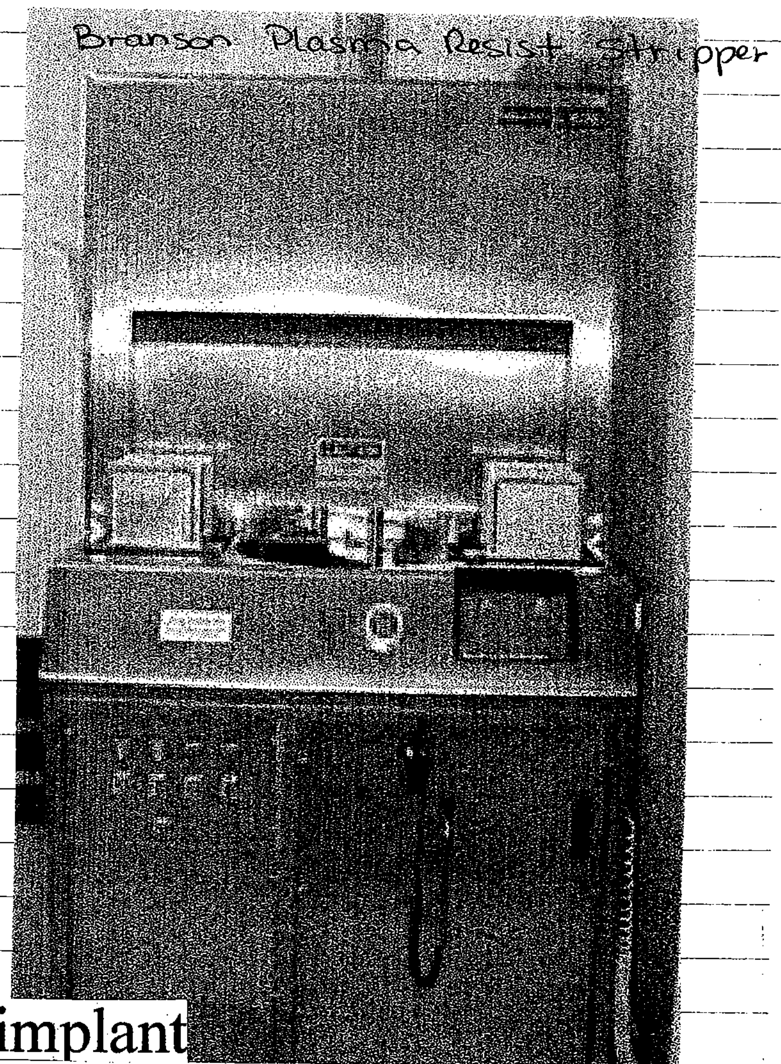
12/7/01

Factory Lot: F011024 Sub Micron CMOS

Tool: Plasmaline 415

Process: ET07

Step #: 9



Results:

Base pressure: 0.074

Forward power: 225W

Reflected power: ½ - 1 W

Ash Time: 45 min.

4" wafers and 6" wafers

Recipes Include

4" normal ash

4" hard ash

6" normal ash

6" hard ash

Hard ash is used after ion implant

12/7/01 P. [signature] 9

12/7/01

Factory Lot: F010328 Sub micron CMOS

Tool: RCA Clean

Process CL01

Step #: 34

Recipe:

Bath 1: APM (NH_4OH | H_2O_2 | H_2O in a 1:3:15 ratio)

Note: Bath will not heat until 4500 mL of Liquid is add

First add 4500 ml H_2O

Then add 900 ml H_2O_2

Finally add 300 mL NH_4OH

Bath 2: APM (HCL | H_2O_2 | H_2O in 1:3:15 ratio)

Note: Bath will heat until all 5600 ml of liquid is added

First add 4500 mL H_2O

then add 900 mL H_2O_2

Finally add 300 mL HCL

time = 10 min

↳ Bath 1

- Rinse for 4 cycle in the dump rinser
- Dip in HF | H_2O (1:50) → 60 seconds
- DI rinse 5 minutes

Bath 2 → 10 min

- DI rinse 2 min (right tank)
- DI rinse 5 min (left tank)
- Spin dry
- Inspect using Tencore Surface scan.

[signature] 12/7/01

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VP5840 Rev. 01-6-98 Made in USA

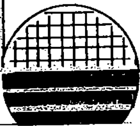
12/14/01

Factory

DAILY LOT STATUS REPORT

DATE: 12-14-01 TIME: 7:14 AM

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
F010125	Mixed	PW3	PH03	X		38	ET08	3	Poly layer 5
F010321	Mixed	PW3	CV01	X		34	DI04	3	Poly LPCVD
F010328	Subμ	1.0	ET06	X		38	DE01	2	Etch & 4pt Probe
F010604	Subμ	150	PH03		X	6	ET09	3	Canon Stepper
F010605	Mixed	PW3	OX04	X		26	IM01	3	Kooi Oxide
F010606	Subμ	1.0	PH03	X		19	ET09	3	Active layer 2
F010924	Mixed	PW3	CV02	X		13	PH03	3	Deposit Nitride
F011024	Subμ	1.0	IM01	X		13	OX06	3	P-well
F011206	Mixed	PW3	OX06	X		10	ET06	3	Well Drive
F011212	Subμ	150	CV02	X		5	PH03	3	Measure Oxide



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```
12/14/01                    MESA                     IGEXINQ      S36902
 9:11:55            Instruction Execution            QPADEV000W    RIT

Lot number . . . . . .    F010125
Instruction group   . :   CMOS-PH03-POLY          3.0

Type selections.  Then Enter.
  1=Display document     2=Execute step     5=Display detail

 Opt   Text
  _    1.0 Include D1-D3 (General Instructions) (see lvl5phot.pps)
  _    2.0 Locate correct masks for this project
  _    3.0 Record device and test mask no., move-in
  _    4.0 Use Trac coat program 7,3,3 (GCA1006) (see 733 722.pps)
  _    5.0 Coat Photoresist on D1-D3, softbake
  _    6.0 Expose on Stepper, level 5 maskset, POLY (NPH3L113.FFT)
  _    7.0 Use correct stepper jobname\5T,5D,OPEN
  _    8.0 Use integrate mode, exposure units =.4, record as time
  _    9.0 1 Exposure unit = 250 mW/cm**2
  _   10.0 Develop on Trac program 7,2,2 - postbake 120C (see 733
  _   11.0 Inspect and record comments
                                                              More

 Opt   Text
  _   12.0 Record Stepper ID, E, t, Focus, T
  _   13.0 Measure X and Y overlay in 5 locations (see xyloc.pps)
  _   14.0 Measure 4um CD on Leitz microscope (see alvernod.pps)
```

P. [signature] 12/14/01

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RCA Clean Process 12/7/01

NH_4OH - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

→ DI water rinse, 5 min.

→ H_20 - 50
HF - 1
60 sec.

→ DI water rinse, 5 min.

→ HCL - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

→ DI water rinse, 5 min.

→ SPIN/RINSE DRY

What does RCA stand for?

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P. [signature] 12/7/01

6700 DSW Wafer Stepper 12/14/01

GCA 8000 Stepper 01

After setting up the 2 masks ~~&~~ insert the wafers the stepper was align and correct data was inputted.

1 w = 1 J/s

250 mw / cm²

Energy → 100 mJ / cm²

Focus: 250

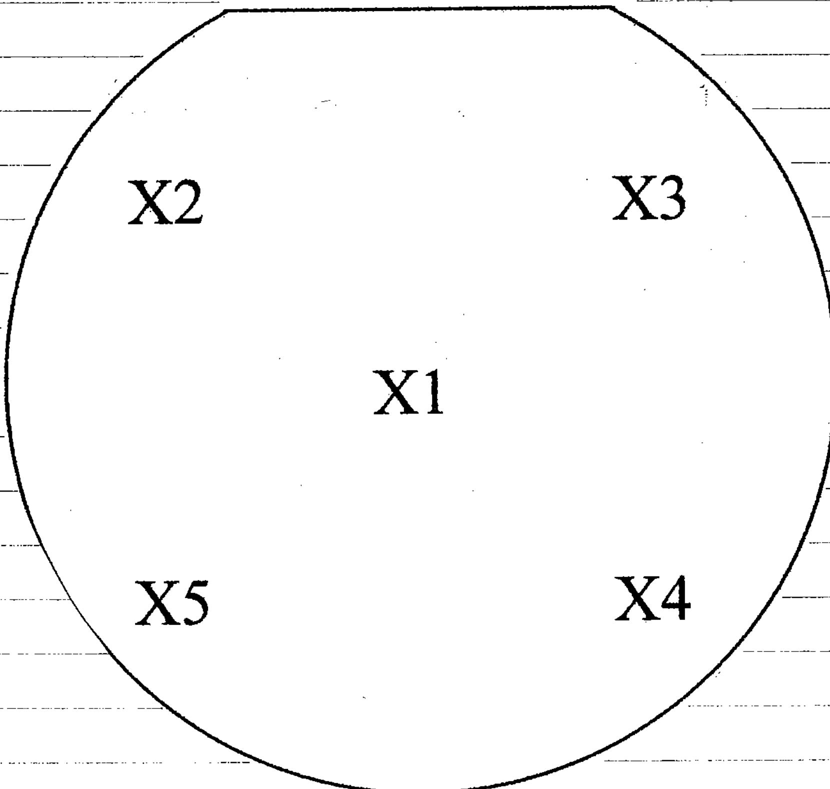
Develop on Trac program 7, 2, 2 Develop.

Post Exposure Bake → **Develop** → **Hard Bake**

Post Exposure Bake	Develop	Hard Bake
115°C, 60 sec	DI Wet CD-26 Developer 50 sec. Puddle Rinse Spin Dry	120°C, 60 sec

Factory X and Y overlay measurement Locations.

X	X	Y (um)
1	2	-3.5
2	4	-3
3	2	-1
4	1	-1
5	1	-1



[signature] 12/14/01

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VP5840 Rev 01-6/98 Made in USA

12/14/01

Factory Lot : F010125 cmos-pmo3-POLY

Tool 1

Process : Poly Layer 5 - PH03

Step Number : 38

Mask Information:

Mask 1: Bare glass

Mask 2: Factory mask Mixed cmos ver. 20003

Mask	Level	Stepper Job Name
Poly	5	Exec [10,1] cmosmix\5, Open

Mask type - negative

Alignment key x = 2.432 mm y = 2.933 mm

Step Size x = 2.62 mm y = 7.62 mm

IC Graph Filename: mixed cmos 031301

IC Graph File Location: /user/faculty/ume/

Mask ID : mixcmos 2

Testchip ID : None

Alignment correction (microns/100)

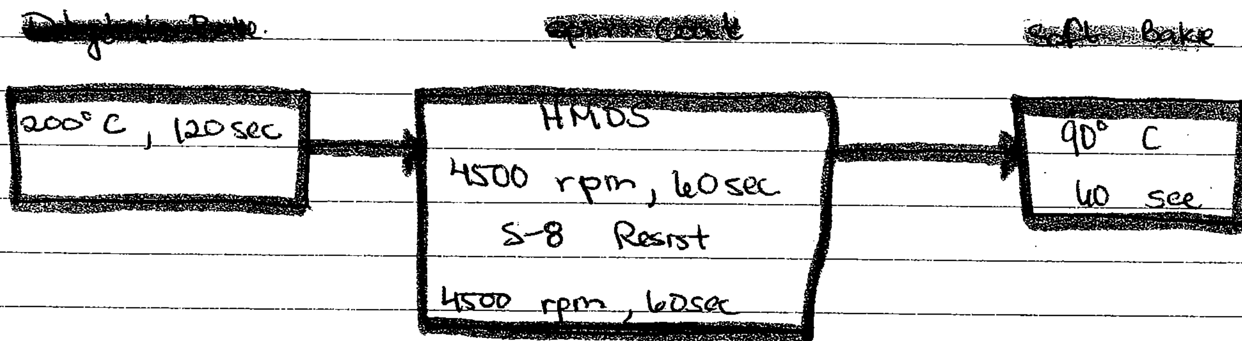
x = 3371

y = -10533

Spincoater Model P6700 Series → Trac coat program 7,33 (step 4.0)

Had to ~~pre~~ prepare this task by hand ~~skin~~ since machine was broken. the steps still remain the same.

733 coat



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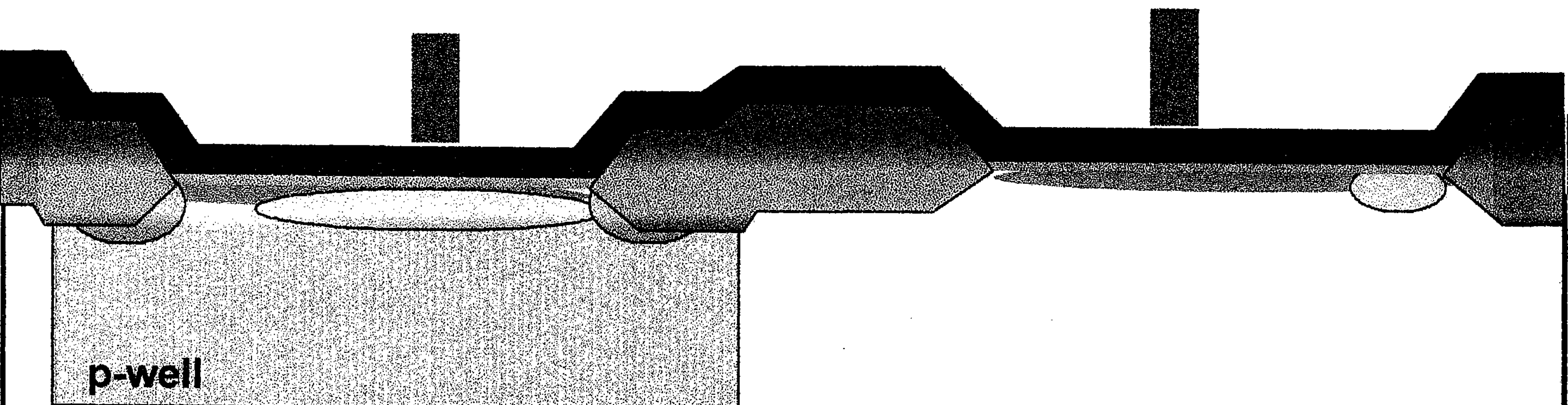
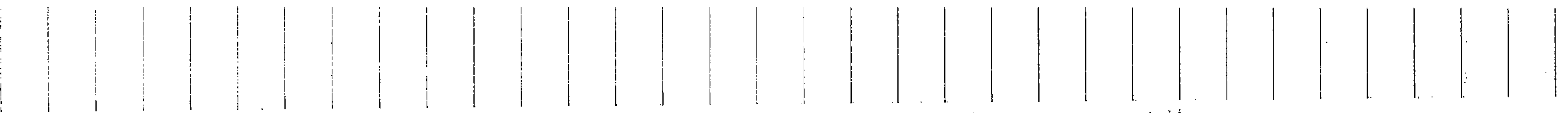
P. Ringersaud

LEVEL 5 PHOTO POLYSILICON





12/14/01

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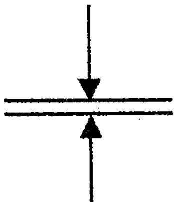
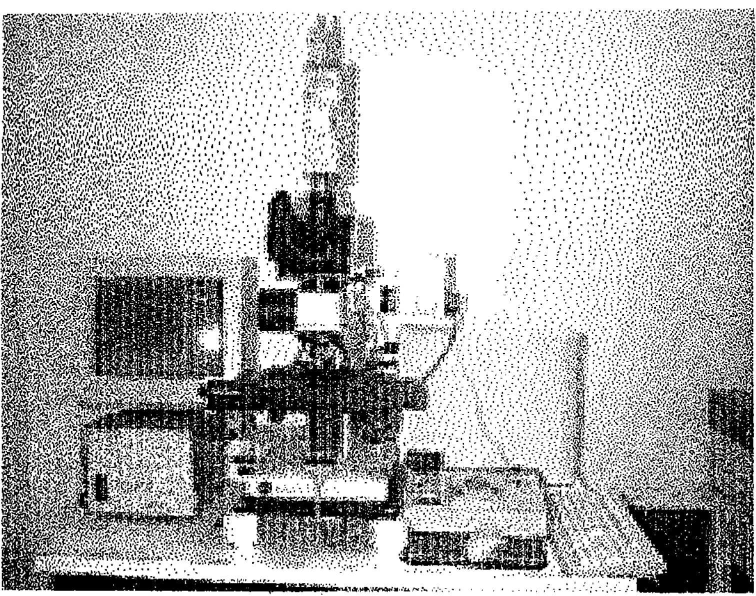
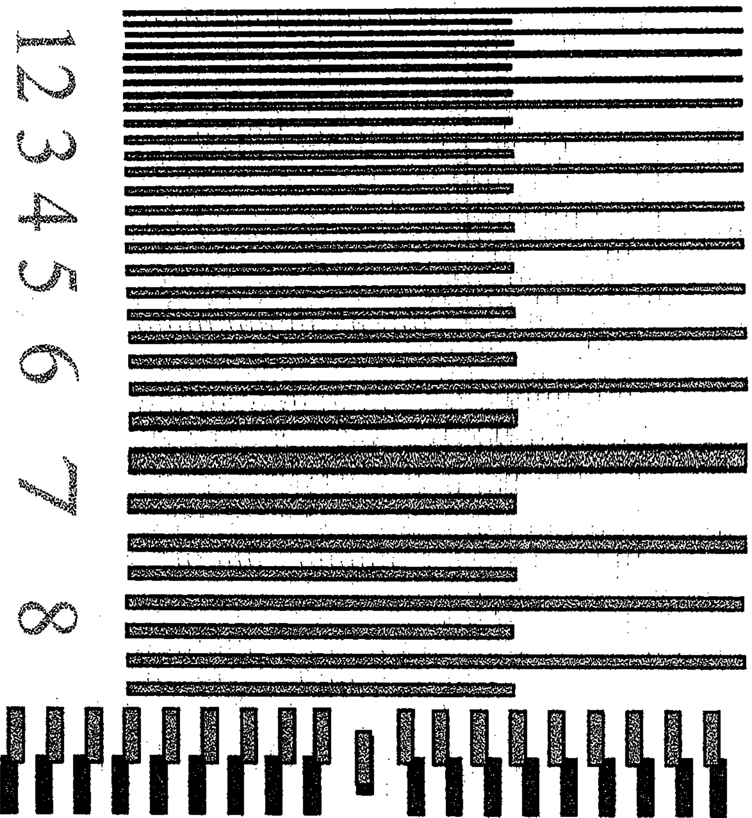
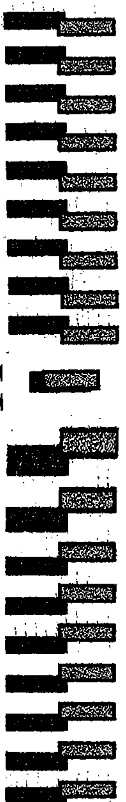
ALIGNMENT VERNIERS AND CRITICAL DIMENSION (CD) STRUCTURES

4 µm CD









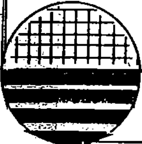
25, 23 - me 1/11/02

Factory

DAILY LOT STATUS REPORT

DATE: 1-11-02 **TIME:** 7:50 am

Lot No.	Product	version	Current Operation	Status InQ	Status InP	Step No.	Next Operation	Qty	Comments
F010125	Mixed	PW3	ET07	X		46	CL01	2	PRIYA
F010321	Mixed	PW3	PH03	X		38	ET08	3	
F010328	Subμ	1.0	ET07	X		48	CL01	2	
F010604	Subμ	150	ET07	X		9	CL01	3	
F010605	Mixed	PW3	CV01	X		34	D104	2	
F010606	Subμ	1.0	IM01	X		31	ET07	3	
F010924	Mixed	PW3	IM01	X		18	ET07	3	
F011024	Subμ	1.0	IM01	X		23	ET07	3	
F011206	Mixed	PW3	ET07	X		16	PH03	2	
F011212	Subμ	150	ET09	X		7	IM01	3	



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1/11/02 **MESA** IGEXINQ S36903
9:15:15 **Instruction Execution** QPADEV000N RIT

Lot number . . . . : F010125
Instruction group . . : CMOS-ET07-N+ 3.0

Type selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt Text
\> 1.0 Include D1-D3 (see ETC07.FFT)
2.0 Strip Photoresist in BRANSON Asher, (see BRANSON.pps)
3.0 USE RECIPE 4" HARD ASH
4.0 Record Forward/Reflected Power, Time

Factory Lot: F010125
Tool : Branson Plasma Resist Stripper
Process : ET07 - Etch
Step # : 46

[signature] 1/11/02

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VP5840 Rev. 01-5'98 Made in USA

12/14/01

1/11/02

Light on
n vaccum on
it home position
2 4 µm Line (first try)
(second try)

Actual 1/11/02
→ 4496
n → 4031
n

} Power

500 mtorr
1000 Sccm
0 Sccm

r: 500W
: 1 W
: 0 W
: 2:19 min

= 1800 W (heats surface of wafer)

→ type SOB-CMOS
or CMOS PW-3
print (VI)

1/11/02

Factory Lot: F010125

Tool : RCA TOOL

Process : CMOS-CL01-Well Drive

Step # : 47

1/11/02
10:04:10

MESA
Instruction Group Inquiry

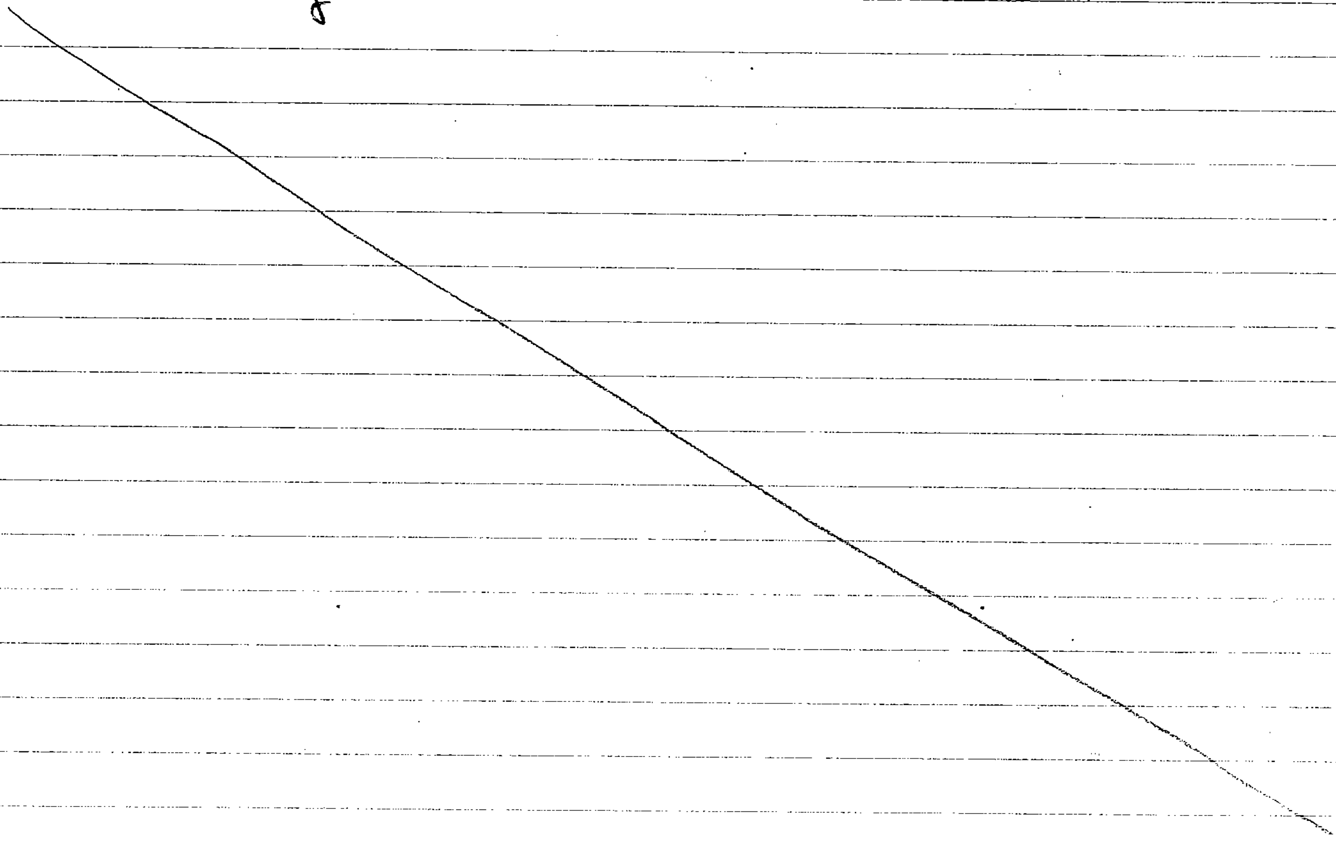
IGMSINQ S36801
QPADEV000B RIT

Type information. Then Enter.
1=Display document, 5=Display detail

Plant . . . . : **RIT**
Instruction group . . **CMOS-CL01-WELL-DRIVE** CMOS CL01 RCA CLEAN WELL DR.
Revision 3.0

Opt	Subgroup	Text
_		1.0 Include D1-D3
_		2.0 RCA Clean (see RCAClean.pps)

It was necessary to start a new batch of clean.



[signature] 1/11/02

RCA

APM
NH_4OH - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 10 min.

→

DI water
rinse, 5 min.
2.5 min down stream (R)
2.5 min up stream (L. tank)

→

H_20 - 50
HF - 1
60 sec.

→

DI water
rinse, 5 min.

→

HPM
HCL - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

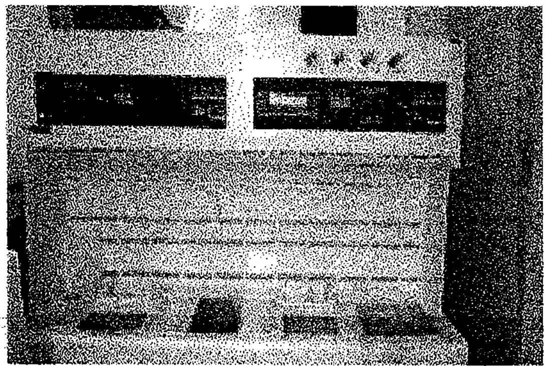
→

DI water
rinse, 5 min.

→

SPIN/RINSE
DRY

What does RCA stand for?



1/11/02

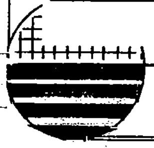
1/18/02

Factory

DAILY LOT STATUS REPORT

DATE: 1/18/02 **TIME:** 7:35 am

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	ET07	X		52	DE01	2	
F010321	Mixed	CMOS PW-3	PH03	X		44	IM01	3	
F010328	Test Chip	SUB-CMOS 1.0	CV03	X		50	OX08	2	
F010604	Test Chip	SUB-CMOS 150	IM01	X		13	OX06	2	Priya
F010605	Mixed	CMOS PW-3	DI04	X		35	ET06	2	
F010606	Test Chip	SUB-CMOS 1.0	CV01	X		36	DI04	3	
F010924	Mixed	CMOS PW-3	ET06	X		24	CV01	3	
F011024	Test Chip	SUB-CMOS 1.0	OX04		X	26	ET09	3	measure again
F011206	Mixed	CMOS PW-3	ET09	X		23	ET06	2	
F011212	Test Chip	SUB-CMOS 150	OX04		X	11	ET09	3	



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```
1/18/02                         MESA                    IGEXINQ      S36903
9:14:59                 Instruction Execution           QPADEV000B   RIT

Lot number . . . . . .    F010604
Instruction group  . :    SUB-CMOS-IM01-P-WELL 150

ype selections.  Then Enter.
 1=Display document   2=Execute step   3=Rework-to step

 Opt  Text
  _ > 1.0 Include D1-D3 (General Instructions)
  _   2.0 Ion Implant Boron (see IMPTB11.pps)
  _   3.0 Dose = 2E13, Species = B11
      4.0 Energy = 50 keV
      5.0 Record Energy, Dose, Set-up time, Species
```

Factory Lot: F010604
Tool : Ion implanter [Varian 350D]
Process : Sub-Cmos-IM01-P-Well
Step # : 13

22 [signature] 1/18/02

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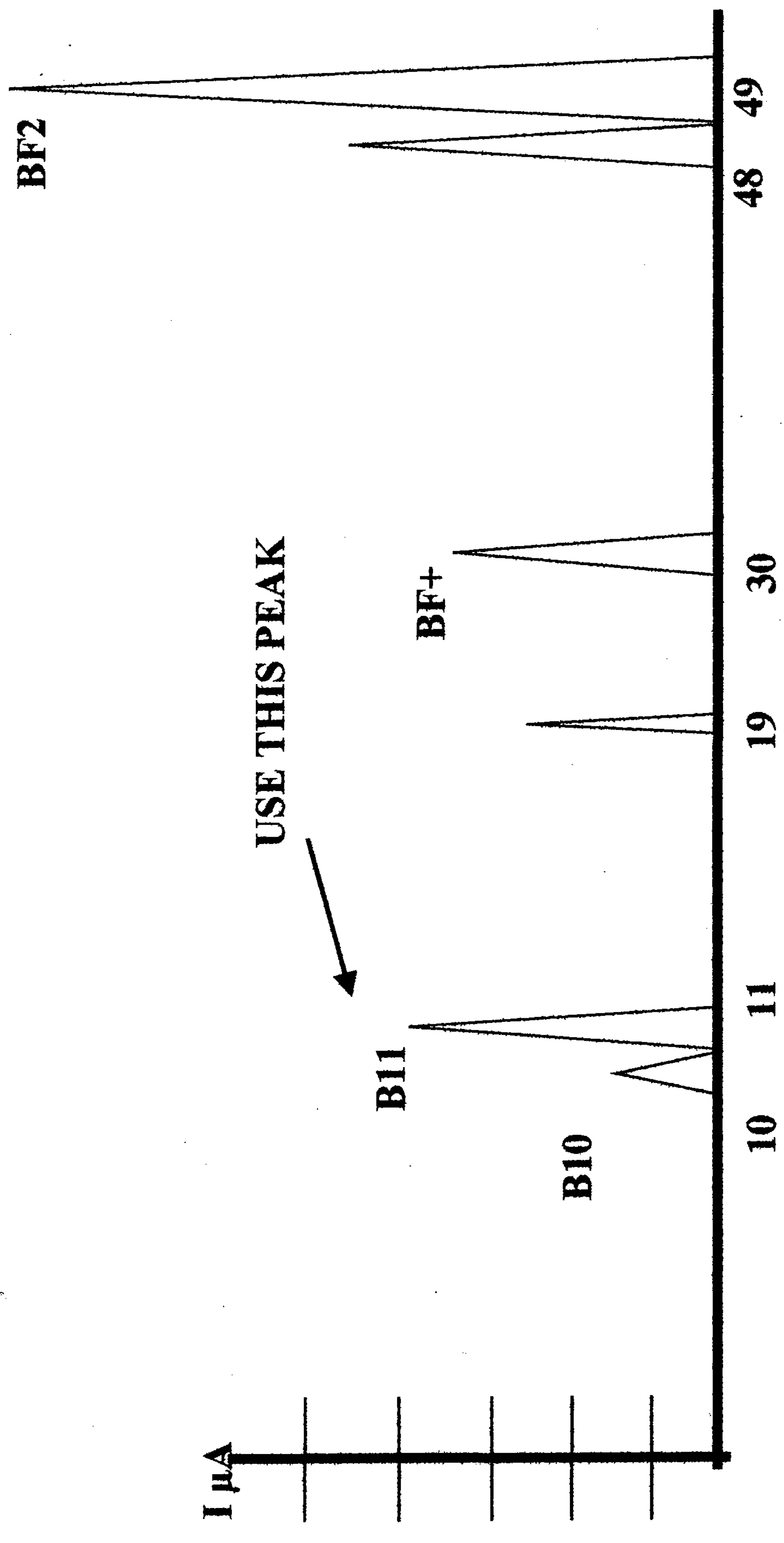
1/18/02



1/18/02

After adjusting I_x I_y my beam current = 10 uA 1/18/02

$$Time = \frac{dose \times area \times q}{I} = \frac{(2 \times 10^{13})(1.96 \times 10^{+2})(1.6 \times 10^{-19})}{10 \times 10^{-5}} = 6.272 \times 10$$

Time = 62.72 sec / wafer

Time = 62 sec/wafer

Actual Dose time = 65.2 (wafer 1)
= 64.7 (wafer 2)

End Station Controller Pressure (torr) = 1.00 E-06
Beam Line Vacuum (torr) = 8.00 E-07
Source Control Pressure gas (torr) = 0
Gas ~~BF3~~ = BF3
Species = B11
Source control pressure (w/ gas on) = 3.20 E-5
Dose 1/cm2 = 2 e13
Energy KeV = 50
Implant Area Select (cm2) = 196
Beam Current (uA) = 10
Extraction Current mA = 0.7
Source Filament Current (Amps) = 126
S magnet Current (A) = 0.9
Arc Current (A) = 0.1
Analyzer Digitial Display = 196

WBOB Wafer broken by operator

24 1/18/02

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VP5840 Rev. 01-6-98 Made in USA

1/25/02

Factory

DAILY LOT STATUS REPORT

DATE: 1-25-02 TIME: 8:00 am

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	SEM1	X		59.1	TE01	2	
F010321	Mixed	CMOS PW-3	CV03	X		49	PH03	3	
F010328	Test Chip	SUB-CMOS 1.0	PH03	X		53	IM01	2	
F010604	Test Chip	SUB-CMOS 150	CV02	X		18	PH03	2	
F010605	Mixed	CMOS PW-3	ET08	X		39	ET07	2	
F010606	Test Chip	SUB-CMOS 1.0	ET08	X		41	ET07	3	
F010924	Mixed	CMOS PW-3	IM01	X		29	ET07	3	
F011024	Test Chip	SUB-CMOS 1.0	IM01	X		31	ET07	3	
F011206	Mixed	CMOS PW-3	PH03	X		28	IM01	2	
F011212	Test Chip	SUB-CMOS 150	CV01	X		16	OX05	3	

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```
1/25/02                        MESA                    IGEXINQ      S36903
9:18:09                Instruction Execution           QPADEV000N     RIT

Lot number . . . . . .  F010605
Instruction group  . :  CMOS-ET08-POLY        3.0

Type selections.  Then Enter.
  1=Display document   2=Execute step

 Opt  Text
      1.0 Include D1-D3
  _   2.0 Reactive ion etch on Drytek Quad tool (Recipe: FACPOLY)
  _          SF6 flow = 30 SCCM  CHF3 flow = 30 SCCM
  _          Pressure = 40 mTorr   Power = 200 Watts
  _          Etch Rate = 1900 A/min
  _   3.0 Etch D1 for 3 min. and 20 sec., inspect by measuring
  _       remaining oxide thickness on Nanospec (should
  _       be < 500 A) in the 5 test sites and record
  _       (DO NOT ETCH FOR MORE THAN 3:20 MIN)
  _   4.0 Etch remaining device wafers for the same time
  _   5.0 Record gas, flow, pressure, power, time
  _                                                              Bott
F3=Exit   F5=Refresh   F11=Display groups   F12=Cancel   F24=More keys
```

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1/25/02

ITER FILM TYPE

TER OBJ LENS
10X 2=40X 3=100X

[illegible] OX,OE ON SI
EX OBJECTIVE
W REF WAFER?

CUS ON REF WAFER
EN PUSH MEASURE
TER SAMPLE #

TER REFR INDE
FR INDEX = 1 45

S FOCUS SAMPLE
EN PUSH MEASURE

D.# THICKNESS
LESS THAN 20

566 A
514 A

498 A
399 A
[illegible] A
[illegible] A
7
8 397 A

Scrap wafer after Drytek Quad.
There are no poly lines.

New Lot Started: F020204 -MIX ID01 2/1/02

Diameter (mm)	100
Orientation	1-0-0
thickness	525 +/- 25 um
Resistivity	7.5 - 12.5 Ω cm.
Crystal type	CZ
Type	N
Dopant	ph

} Data from new wafer box

DE01

DI - 1.424 V 28.0 mA } data from 4-point probe.

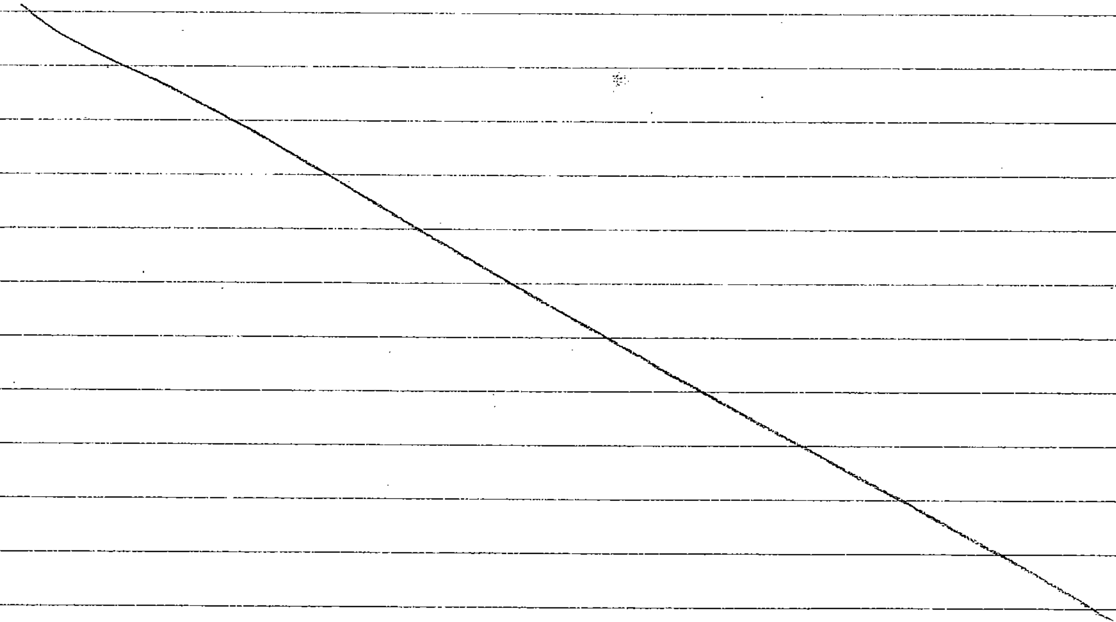
$$Rho = \pi / \ln 2 \times W \times F \times \frac{V}{I}$$

$$Rho = \frac{\pi}{\ln 2} \times 525\,\mu m \times 1 \times \frac{1.424}{28\,mA} = \frac{0.0838}{\ln 2}$$

× ~~$\pi/2$~~ → 50.85

$$Rho = 0.121\ \Omega\,m \rightarrow \boxed{12.10\ \Omega \cdot cm}$$

$$\boxed{Rho = 12.10\ \Omega \cdot cm}$$



2/1/02

2/1/02

Factory

DAILY LOT STATUS REPORT

DATE: 2-1-02 **TIME:** 9:29

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	TE01	X		60	TE02	2	
F010321	Mixed	CMOS PW-3	ET07		X	52	DE01	3	
F010328	Test Chip	SUB-CMOS 1.0	IM01	X		57	ET07	2	
F010604	Test Chip	SUB-CMOS 1.0	ET09	X		20	ET07	2	
F010605	Mixed	CMOS PW-3	IM01	X		42	ET07	1	
F010924	Mixed	CMOS PW-3	DI04	X		35	ET06	3	
F011024	Test Chip	SUB-CMOS 1.0	CV01	X		36	DI04	3	
F011206	Mixed	CMOS PW-3	CV01	X		34	DI04	2	
F011212	Test Chip	SUB-CMOS 150	CV02	X		18	PH03	3	
F020129	Test Chip	SUB-CMOS 1.0	CV02	'	X	5	PH03	3	
F020202	Test Chip	SUB-CMOS 150	OX05	X		4	CV02	3	

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```
2/01/02                       MESA                IGEXINQ     S36902
10:04:29              Instruction Execution       QPADEV000V    RIT

Lot number . . . . . .   F020204  - New Lot
Instruction group  . :   CMOS-ID01            3.0

Type selections.  Then Enter.
  1=Display document    2=Execute step    5=Display detail

  Opt  Text
   _   1.0 3 Device wafers (100) 5 ohm-cm,n-type 4"
   _   2.0 Scribe with lot number and D1-D3 (see Scribe.pps)
   _   3.0 Record data from the wafer box, rho, type, thickness for
   _       device wafers
```

2/1/02

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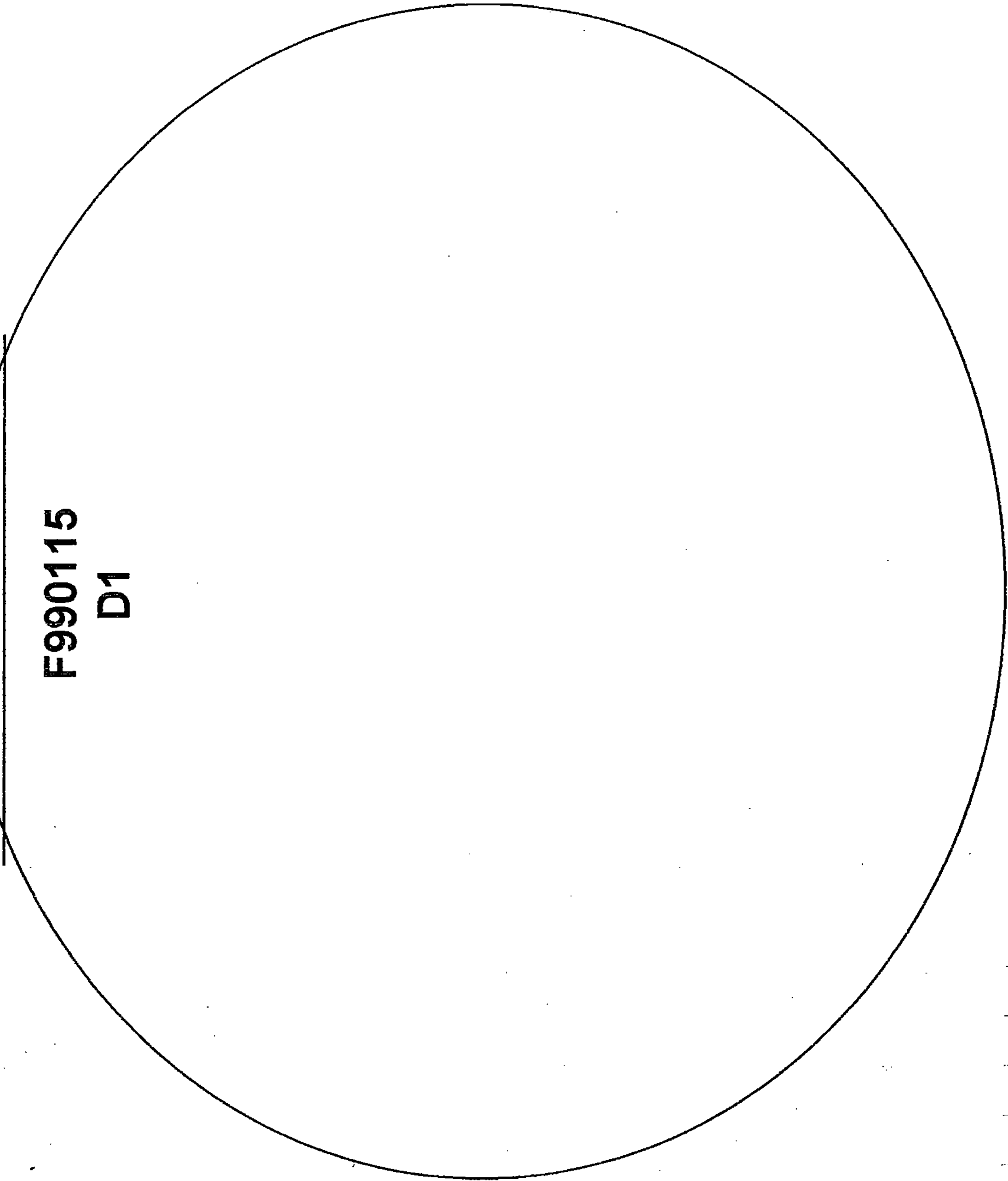
2/1/02

ID01 IDENTIFY - SCRIBE LOT NUMBER

PLAY



2/1/02

2/01/02

2/01/02
10:18:40

MESA
Instruction Execution

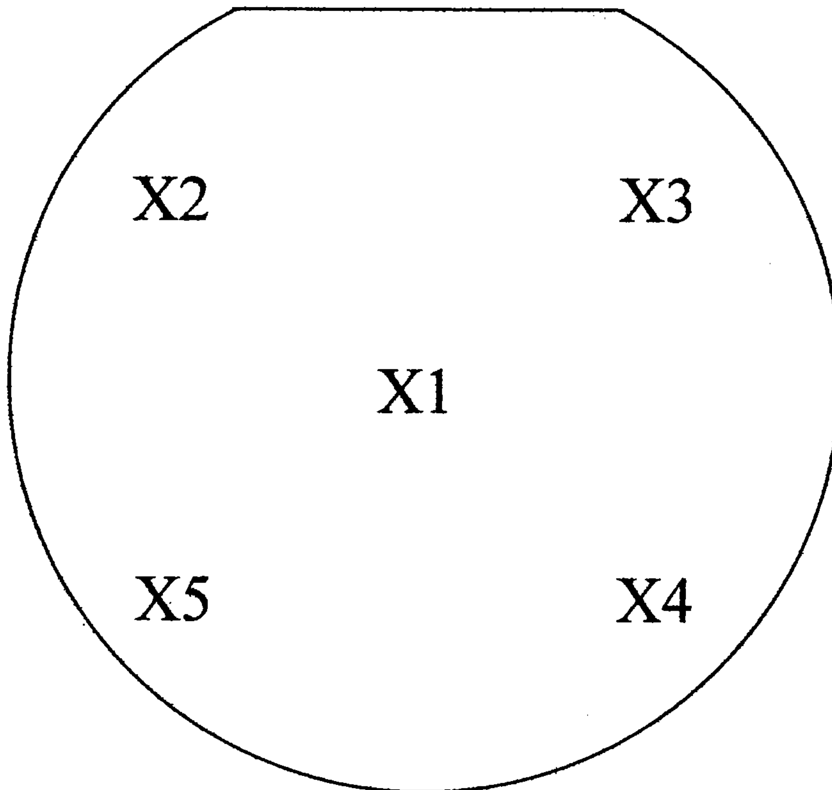
IGEXINQ S36903
QPADEV000V RIT

Lot number F020204
Instruction group . : CMOS-DE01-START 3.0

Type selections. Then Enter.
1=Display document 2=Execute step

Opt	Text
_	1.0 4pt probe D1 on front side
_	2.0 Record average voltage, current, rho (see 4ptprobe.pps)

FACTORY X AND Y OVERLAY MEASUREMENT LOCATIONS



2/1/02

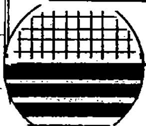
2/8/02

DAILY LOT STATUS REPORT

DATE: 2-8-02 TIME: 7:14 am

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	TE01	X		60	TE02	2	
F010321	Mixed	CMOS PW-3	ET07	X		58	S101	3	Priya
F010328	Test Chip	SUB-CMOS 1.0	CV03	X		61	PH03	2	
F010605	Mixed	CMOS PW-3	CL01	X		47	OX08	1	
F010924	Mixed	CMOS PW-3	PH03	X		38	ET08	3	
F011024	Test Chip	SUB-CMOS 1.0	PH03	X		40	ET08	3	
F011206	Mixed	CMOS PW-3	CV01	X		34	DI04	2	
F011212	Test Chip	SUB-CMOS 150	CV12		X	18	PH03	3	Done
F020129	Test Chip	SUB-CMOS 1.0	ET07	X		9	CL01	3	
F020202	Test Chip	SUB-CMOS 150	CV02	X		5	PH03	3	
F020204	Mixed	CMOS PW-3	PH03	X		5	ET06	3	

Shift Change Meeting (15 min. at start of lab)



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4" wafers and 6" wafers

Recipes Include

- 4" normal ash
- 4" hard ash
- 6" normal ash
- 6" hard ash

Hard ash is used after ion implant

RF FWD 500 W
RF REFL 0 W
Lamp W 0 W
Time/wafer: 1:02
press: 4230 m torr
O_2 4200
H_2 0

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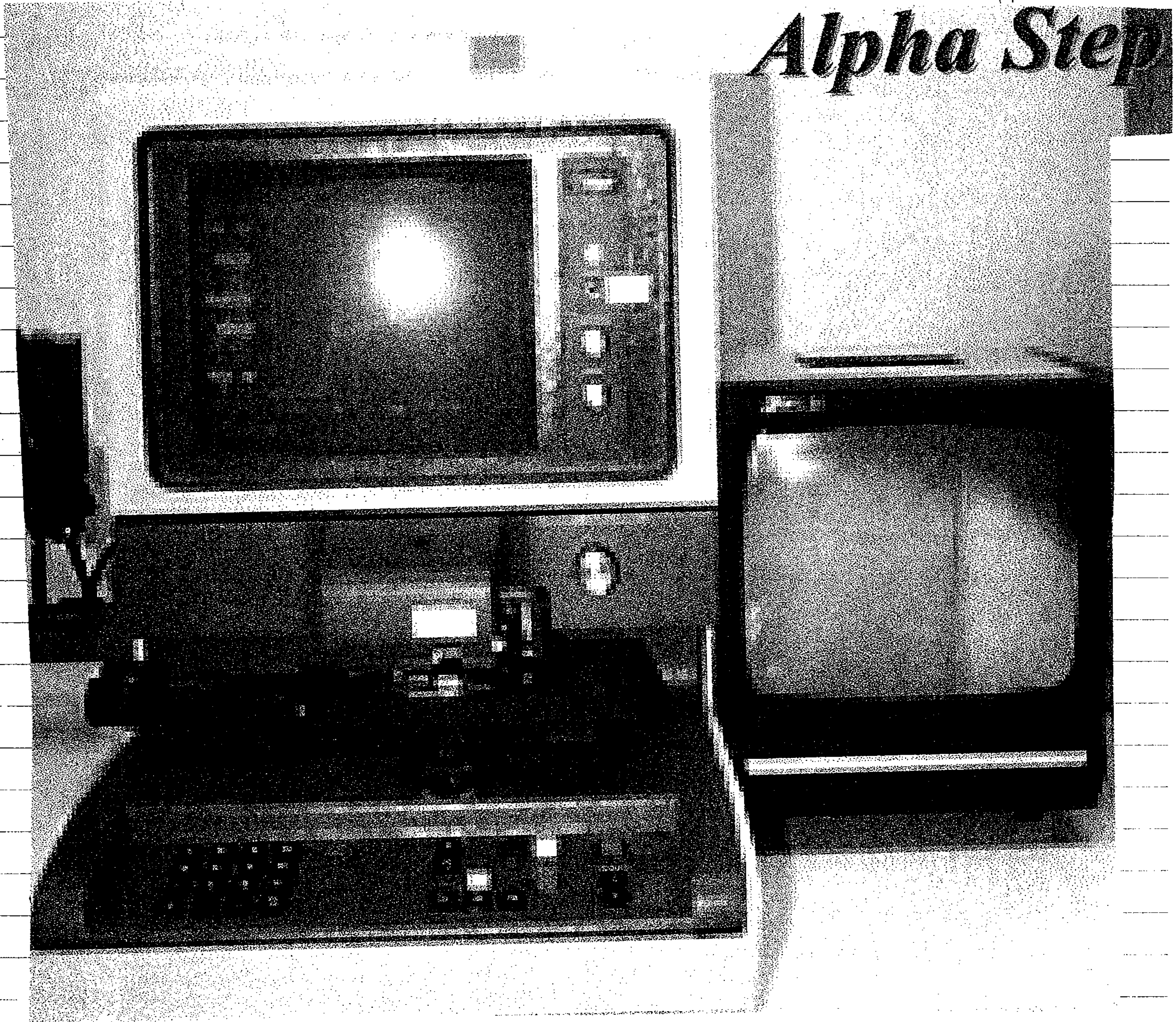
[signature] 2/8/02



2/08/02
9:04:16

MESA
Instruction Execution

IGEXINQ S36903
QPADEV000F RIT

Lot number . . . . . . : F010321
Instruction group . : CMOS-ET07-METAL 3.0

ype selections. Then Enter.
1=Display document 2=Execute step 3=Rework-to step

Opt Text

_ > 1.0 Include D1-D3
_ 2.0 Strip Photoresist in BRANSON Asher,(see BRANSON.pps)
3.0 USE RECIPE 4" NORMAL ASH
_ 4.0 Measure metal thickness on alpha step after resist strip
_ (see alphastp.pps)
5.0 Record Forward/Reflected Power, Time, Al Thickness

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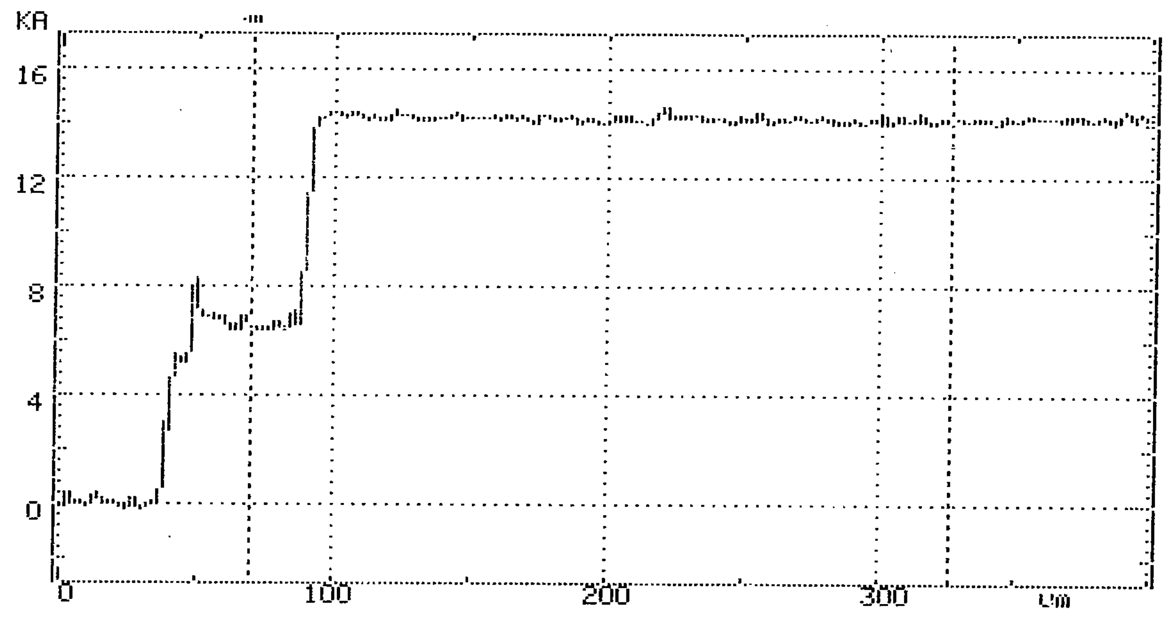
2/8/02

2/8/02

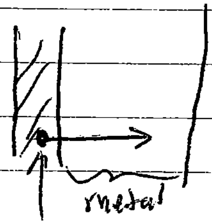
00/09 20:08
ID#
VERT. 20KA
L 6.700KA
R 14.11KA
7.415KA
Avg- 675. A
TIR 8.215KA
Ra 1.145KA
HORIZ 400um
L 70.00um
R 326.0um
256.0um
Area+81.473
SCAN MENU 1
um s/um

2000	.2	1
400	1	5
80	5	25

SCAN t=40 s
DIR. ——>
STYLUS 3mg
154 360um LEVEL



Using the alphastep.
Go to a poly line and then let it travel over to metal



place probe here.

2/15/02

poly - Silver

photo - pink

field oxide

2/15/02
9:26:27

MESA
Instruction Display

IGDPINQ S36902
QPADEV000B RIT

Lot number . . . . . . : F011024
Instruction group . . : SUB-CMOS-ET08 1.0

Type selections. Then Enter.
1=Display document 5=Display detail

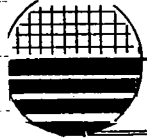
```
Opt  Text
     1.0 Include D1-D3 (see sub_pet.pps)
     2.0 Reactive ion etch in Dry-Tek Quad, SF6+CHF3
            SF6 flow = 30 SCCM  CHF3 flow = 30 SCCM
            Pressure = 40 mTORR   Power = 200 WATTS
            Etch Rate = 1900 a/min
            Do a lot history to find poly thickness and calculate
            the etch time, proper etch should leave ~1/2 gate Ox
     3.0 Inspect wafers and record comments (*place picture here)
     4.0 Record gas, flow, pressure, power, time
```

Factory

DAILY LOT STATUS REPORT

DATE: 2/15/02 **TIME:** 8:00 AM

Lot No.	Product	Process/ Version	Current Operation	Status Q	Status P	Step No.	Next Oper	Qty	Comments
F010125	Mixed	CMOS PW-3	TE01	X		60	TE02	2	
F010321	Mixed	CMOS PW-3	TE01	X		60	TE02	3	
F010328	Test Chip	SUB-CMOS 1.0	ET10	X		63	ET07	2	
F010605	Mixed	CMOS PW-3	CV13	X		49	PH03	1	
F011024	Test Chip	SUB-CMOS 1.0	ET08		X	41	ET07	3	PRIYA
F011206	Mixed	CMOS PW-3	ET08	X		39	ET07	2	
F011212	Test Chip	SUB-CMOS 150	PH03		X	19	ET09	3	
F020129	Test Chip	SUB-CMOS 1.0	ET09		X	12	IM01	3	
F020202	Test Chip	SUB-CMOS 150	CV02	X		5	PH03	3	
F020204	Mixed	CMOS PW-3	ET07	X		8	CL01	3	
F020213	Mixed	CMOS PW-3	OX04	X		4	PH03	3	



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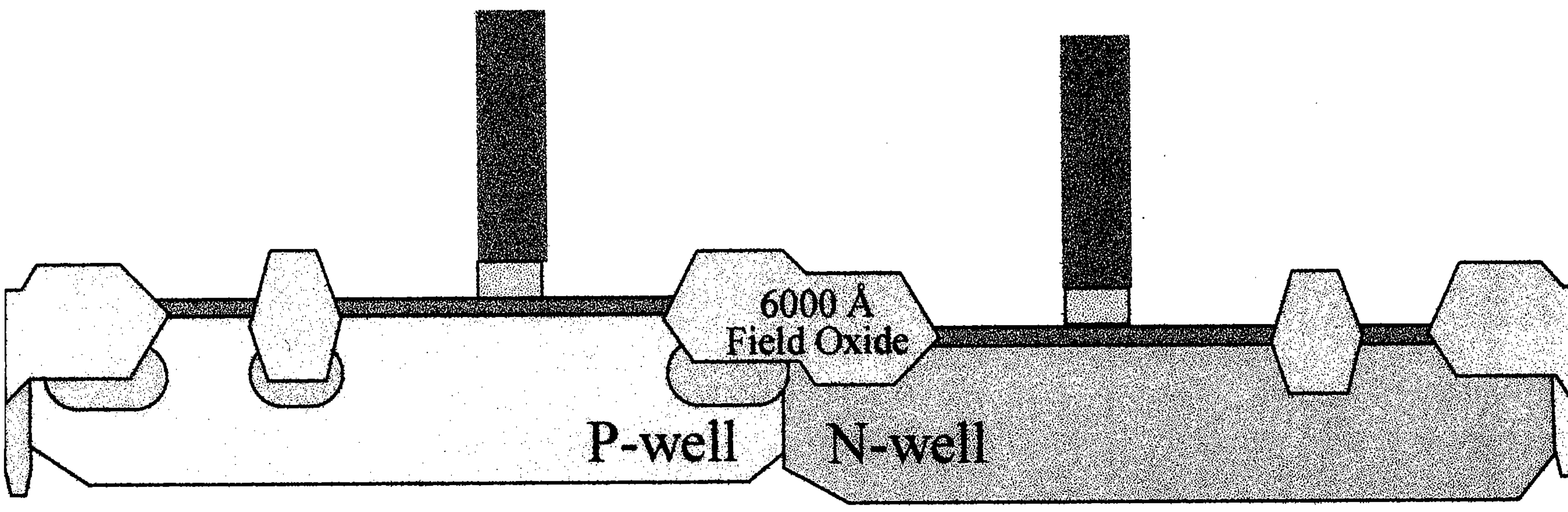
2/15/02

Wafer 2/15/02

POLY ETCH



N-type Substrate 10 ohm-cm

$SF_6 + CHF_3$
40 mTorr

2/15/02

Wafer D2 was etched for 4:30 — 2/15/02

PRINT FILM MENU? W2

* NANOSPEC/AFT *

PRINT FILM MENU?
N
ENTER FILM TYPE
1

ENTER OBJ LENS
1=10X 2=40X 3=100X
1
1 OXIDE ON SI
10X OBJECTIVE
NEW REF WAFER?
Y
FOCUS ON REF WAFER
THEN PUSH MEASURE
ENTER SAMPLE #

ENTER REFR INDEX
REFR INDEX = 1.45
PLS FOCUS SAMPLE
THEN PUSH MEASURE

SEQ. #	THICKNESS
1	1650 A
2	1711 A
3	1584 A
4	1478 A
5	1474 A
6	1468 A

Poly thickness on wafer

X center	6602
X_2	6511
X_3	6536
X_4	6496
X_5	6503

Info

Power Fwd 185

Ref 100

Flow 30 sccm (SF6 & CHF3)

Time 3:30 min

DC Bias 229

* NANOSPEC/AFT *

PRINT FILM MENU?
N
ENTER FILM TYPE
7

ENTER OBJ LENS
1=10X 2=40X 3=100X
2
7 THIN OXIDE ON SI
40X OBJECTIVE
FOCUS ON REF WAFER
THEN PUSH MEASURE
ENTER SAMPLE #

ENTER REFR INDEX
REFR INDEX = 1.45

PLS FOCUS SAMPLE
THEN PUSH MEASURE

SEQ. #	THICKNESS
1	239 A
2	LESS THAN 20 A

ENTER OBJ LENS
... 3=100X
7 ... E ON SI
... IVE
... AFER?
... REF WAFER
... SH MEASURE
ENTER SAMPLE #

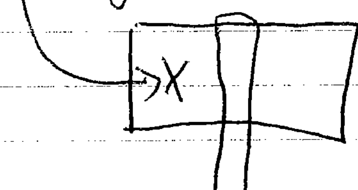
ENTER REFR INDEX
REFR INDEX = 1.45

PLS FOCUS SAMPLE
THEN PUSH MEASURE

SEQ. #	THICKNESS
1	56 A — test
2	202 A
3	201 A
4	126 A
5	192 A
6	101 A
7	89 A
8	194 A

Gate Oxide (thin oxide) ~ 250 Å → measure gate oxide

Field Oxide ~ >1000 Å



[signature] 2/15/02

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