ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

# SPICE Introduction Laboratory


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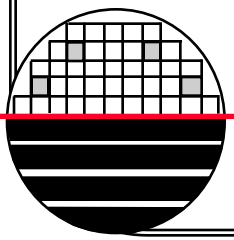
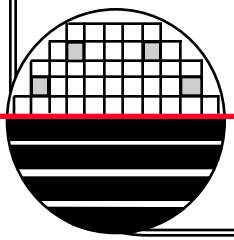


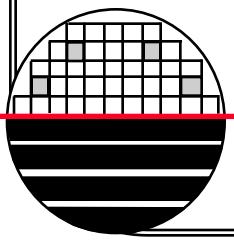
# *ADOBE PRESENTER*

This PowerPoint module has been published using Adobe Presenter. Please click on the Notes tab in the left panel to read the instructors comments for each slide. Manually advance the slide by clicking on the play arrow or pressing the page down key.



# *OUTLINE*

SPICE Introduction
PSpice Lite, OrCAD PSpice and LTSPICE
Simple Example
Resistor and Capacitor Divider Circuit
DC Analysis
AC Analysis
Transient Analysis
Diode Example
Help - Setting Initial Condition (.IC)
- Parameter Sweeps (.Param)
- Include Files (.Inc)
- Monte Carlo Analysis
References

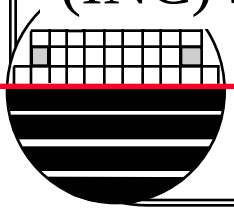


# *INTRODUCTION*

SPICE (Simulation Program for Integrated Circuit Engineering) is a general-purpose circuit simulation program for non-linear DC, non-linear transient, and linear AC analysis. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, transmission lines, switches, and several semiconductor devices: including diodes, BJTs, JFETs, MESFETs, and MOSFETs. Circuits with large numbers of all types of components can be simulated.

SPICE input files and output files are simple text files (e.g. name.txt)

Input files include a TITLE, circuit description NET LIST, analysis directives (COMMANDS), and lists of other text files to include (INC) such as model libraries (LIB) and an END command.



# *INTRODUCTION*

PSPICE Lite 9.2 is one of the OrCAD family of products, from Cadence Design Systems, Inc., offering a complete suite of electronic design tools. It is free and includes limited versions of OrCAD Capture, for schematic capture, PSPICE for analog circuit simulation and Pspice A/D for mixed analog and digital circuit simulation. PSPICE Lite 9.2 is limited to 64 nodes, 10 transistors, two operational amplifiers and 65 primitive digital devices. See page 35 (xxxv) of the PSPICE Users Guide.

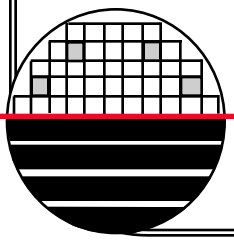
The Electrical and Microelectronic Engineering department at RIT provides a full version of Cadence Design Systems, Inc. PSPICE on the computers in the department laboratories. It uses Allegro Design Capture (also from Cadence) for schematic capture.

LT SPICE – is a free SPICE simulator with schematic capture from Linear Technology. It is quite similar to PSPICE Lite but is not limited in the number of devices or nodes. Linear Technology (LT) is one of the industry leaders in analog and digital integrated circuits. Linear Technology provides a complete set of SPICE models for LT components. (This is a good choice for your home computer.)

# *INPUT FILE GENERATION*

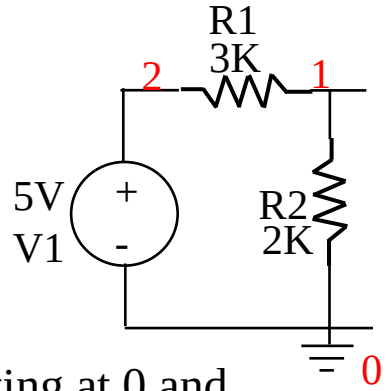
The input file for SPICE is generated automatically from the schematic capture software. In the old days the input file was created by hand as a simple text file. SPICE can still run using a simple text file as the input but today most users prefer to use schematic capture software to create the input file.

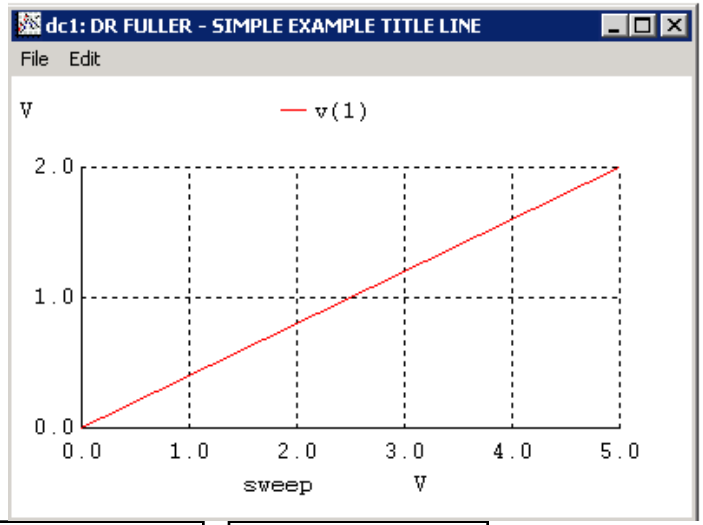
SPICE treats upper case and lower case the same (it is not case sensitive)



# EXAMPLE OF SIMPLE SPICE INPUT FILE

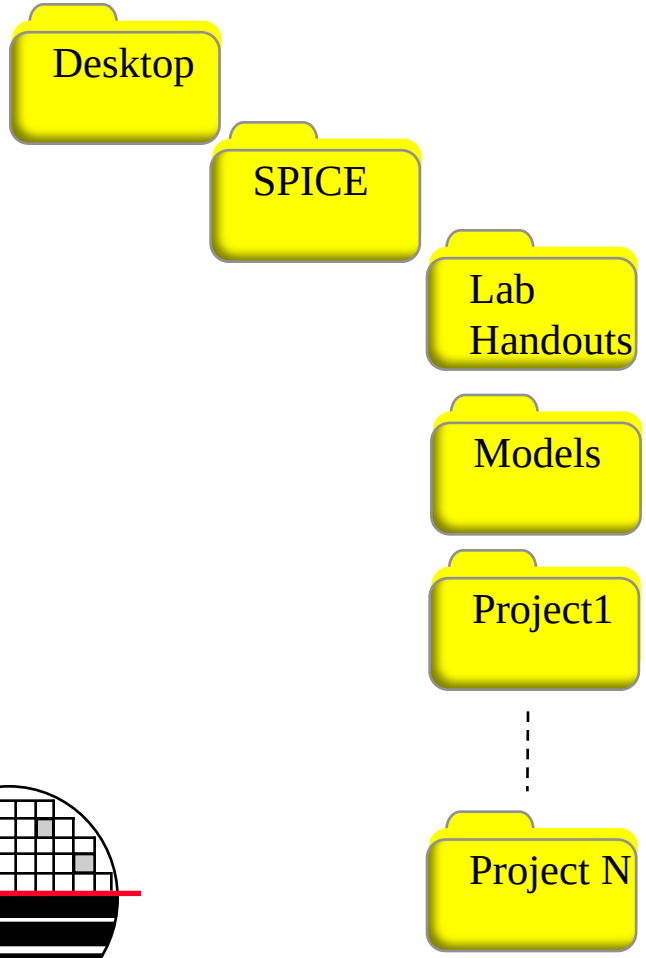
```
DR FULLER - SIMPLE EXAMPLE TITLE
* THE FIRST LINE IS THE TITLE
* LINES THAT START WITH * ARE COMMENT LINES AND DO NOTHING
* UPPER AND lower case text ARE TREATED THE SAME
* CIRCUIT IS DESCRIBED BELOW (NET LIST)
R1 1 2 3K ; resistor R1 between node 1 and node 2 has value 3K ohms
R2 1 0 2K
V1 2 0 DC 5 ; Voltage source V1 is a DC source of 5 volts
*
* REQUESTED ANALYSIS (DIRECTIVES OR COMMANDS)
.DC V1 0 5 0.1 ; find all node voltages and branch currents for V1 starting at 0 and
* incrementing by 0.1 volts ending at 5 volts
.PLOT DC V(1); plot voltage at node (1)
*
*.INCLUDE File_name.txt ;(none for this example)
* The last line is the END command
.END
```



# *BEFORE YOU START*

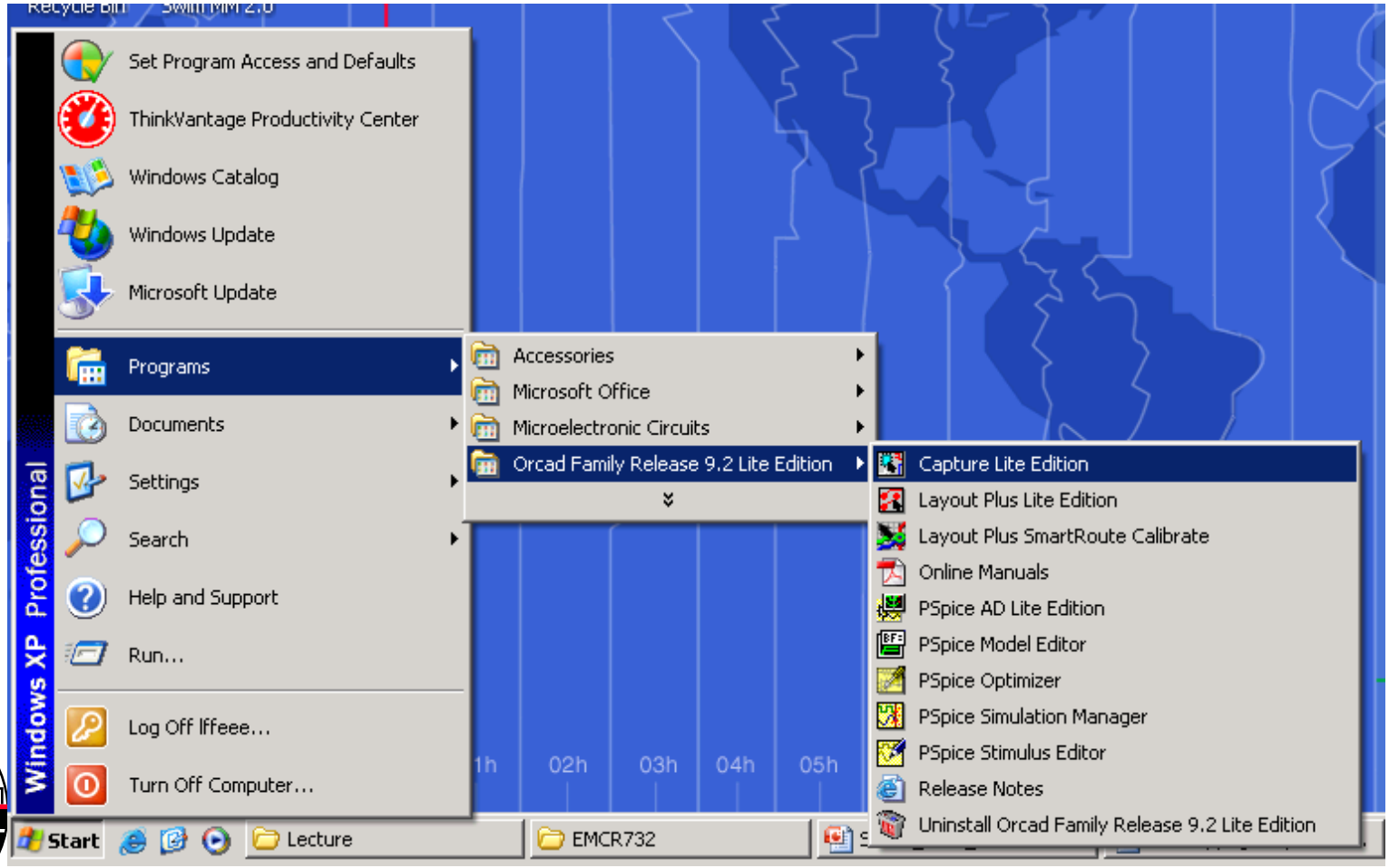
It might be good to set up some folders for your SPICE projects




I put a SPICE folder on my desktop and created sub folders for each project, models and other files, lab handouts, etc.

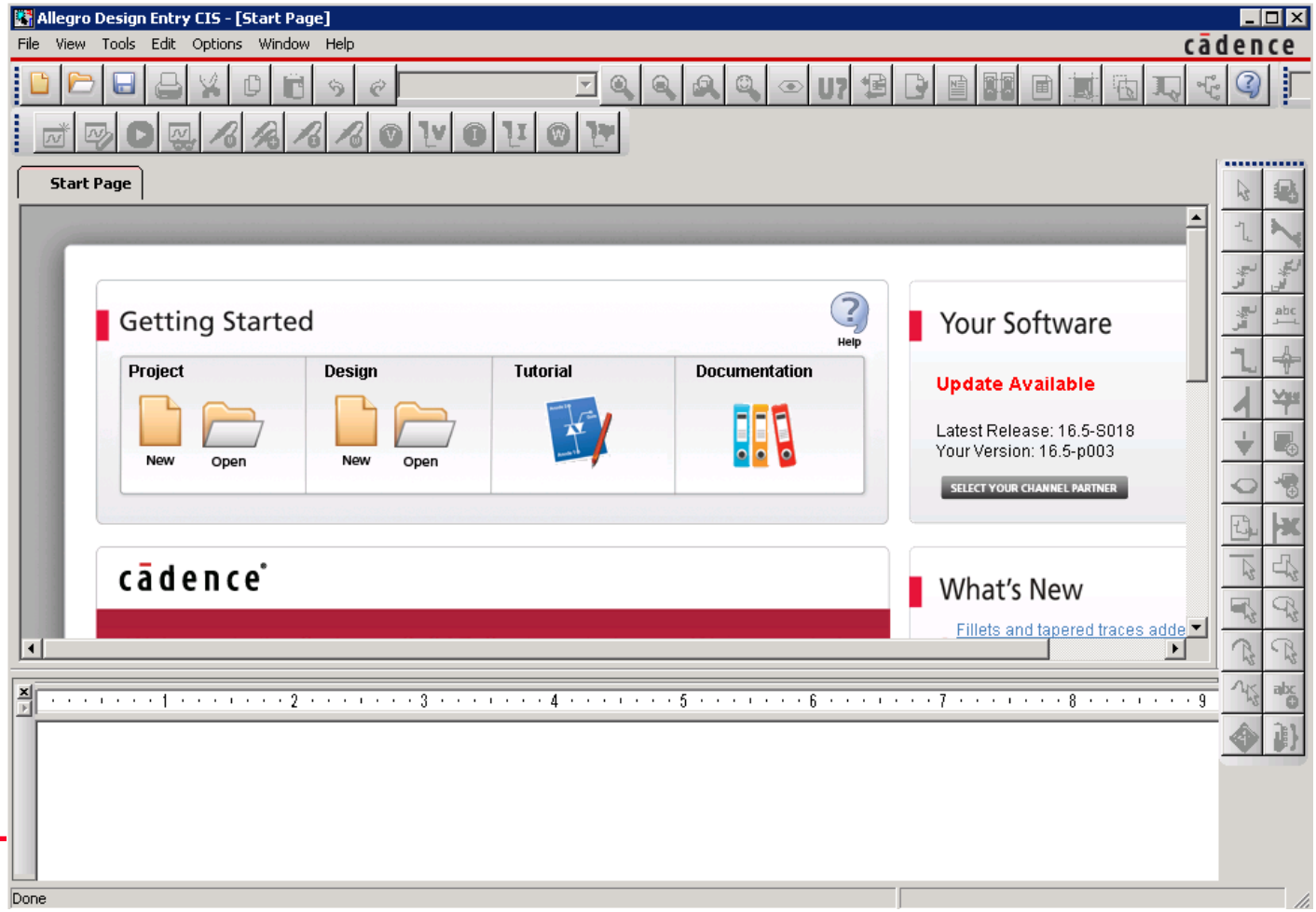
# START SCHEMATIC CAPTURE FOR PSPICE LITE

Start >Programs>Orcad Family Release 9.2 Lite Edition>Capture Lite Edition



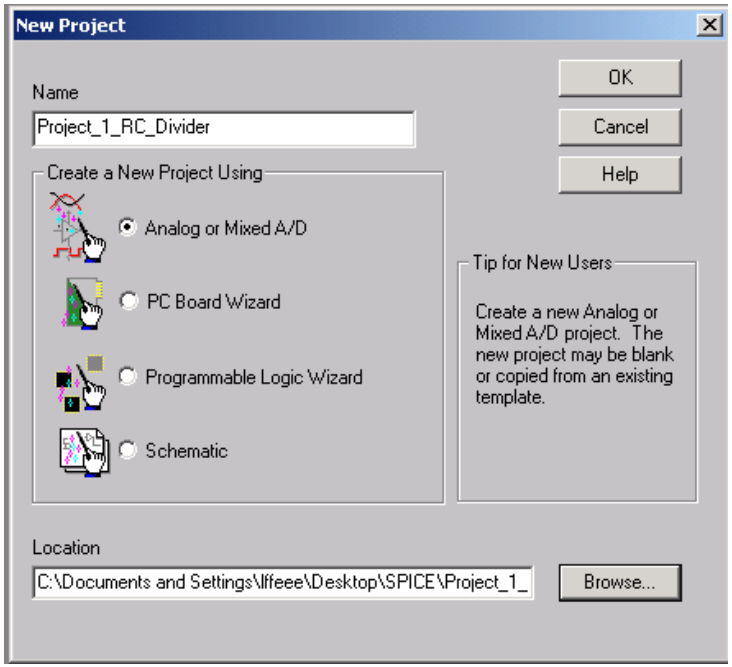
# *Cadence – Allegro DESIGN ENTRY [Start Page]*

Start >All Programs>Cadence>Release 16.6>Design Entry CIS



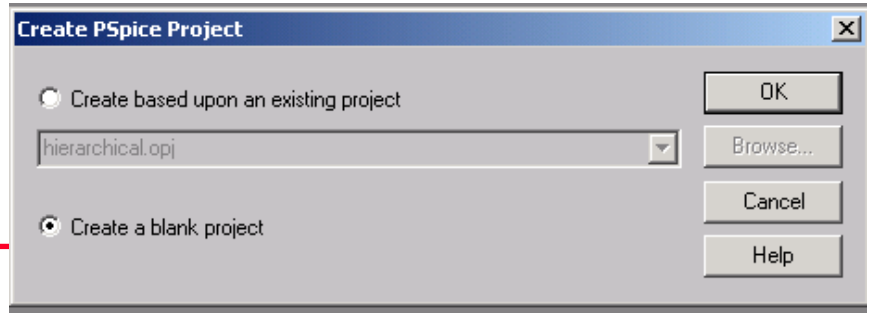
# *OPEN A NEW BLANK PROJECT*

Select File>New>Project



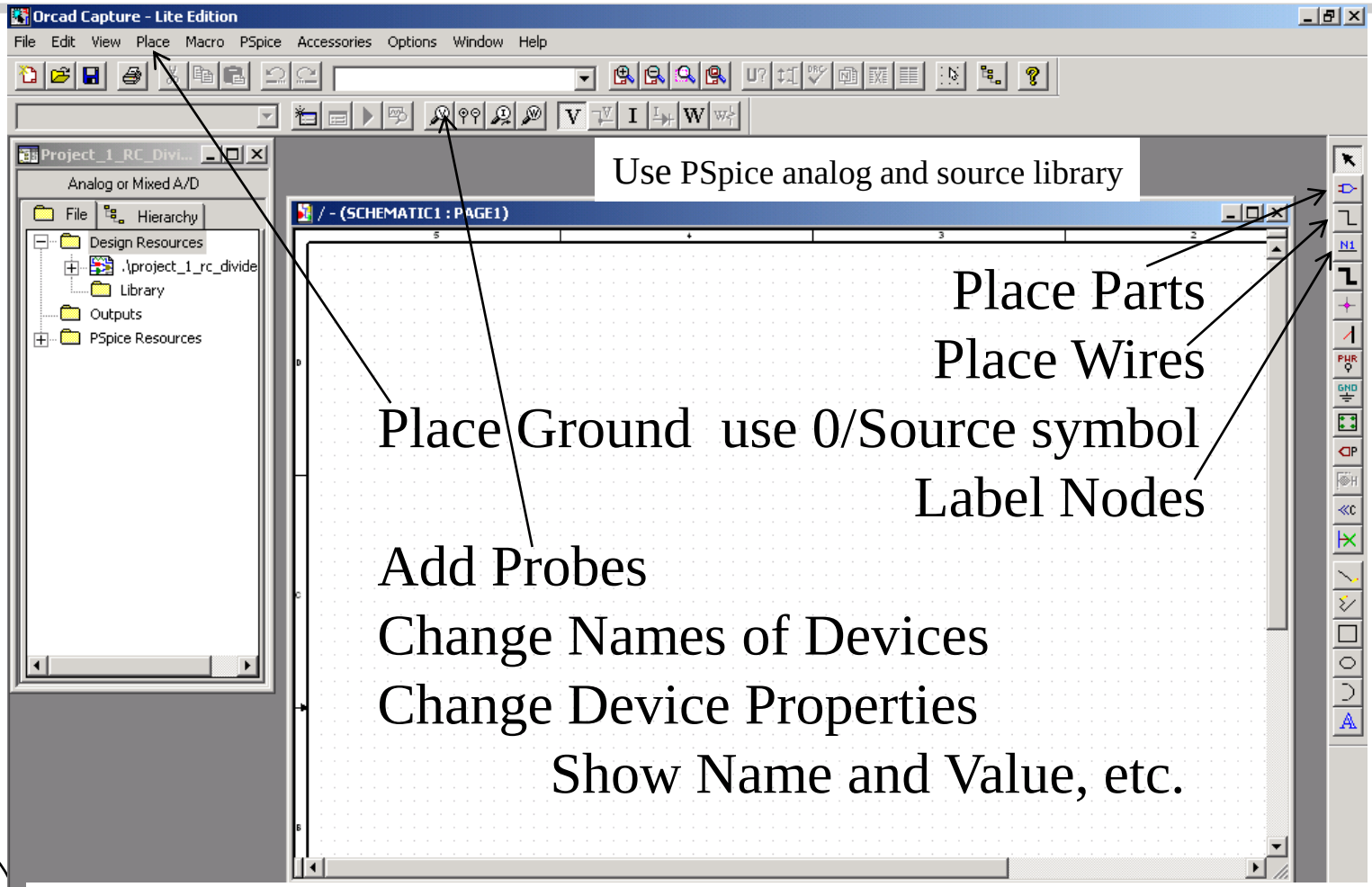

Give it a name
Select Analog or Mixed A/D

Browse to the folder location you set up



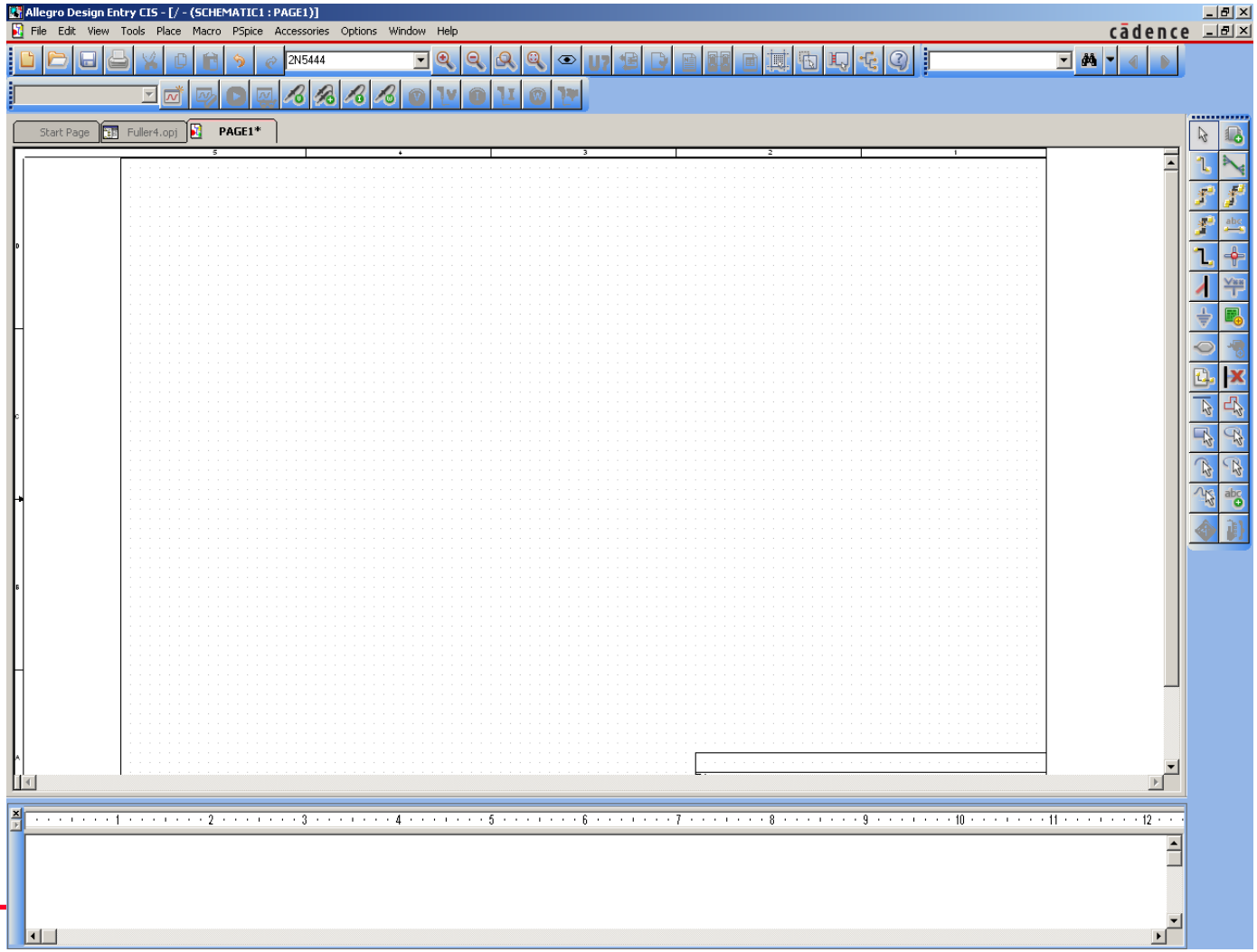

Select create a blank project

# PSPICE LITE SCHEMATIC CAPTURE WORKSPACE



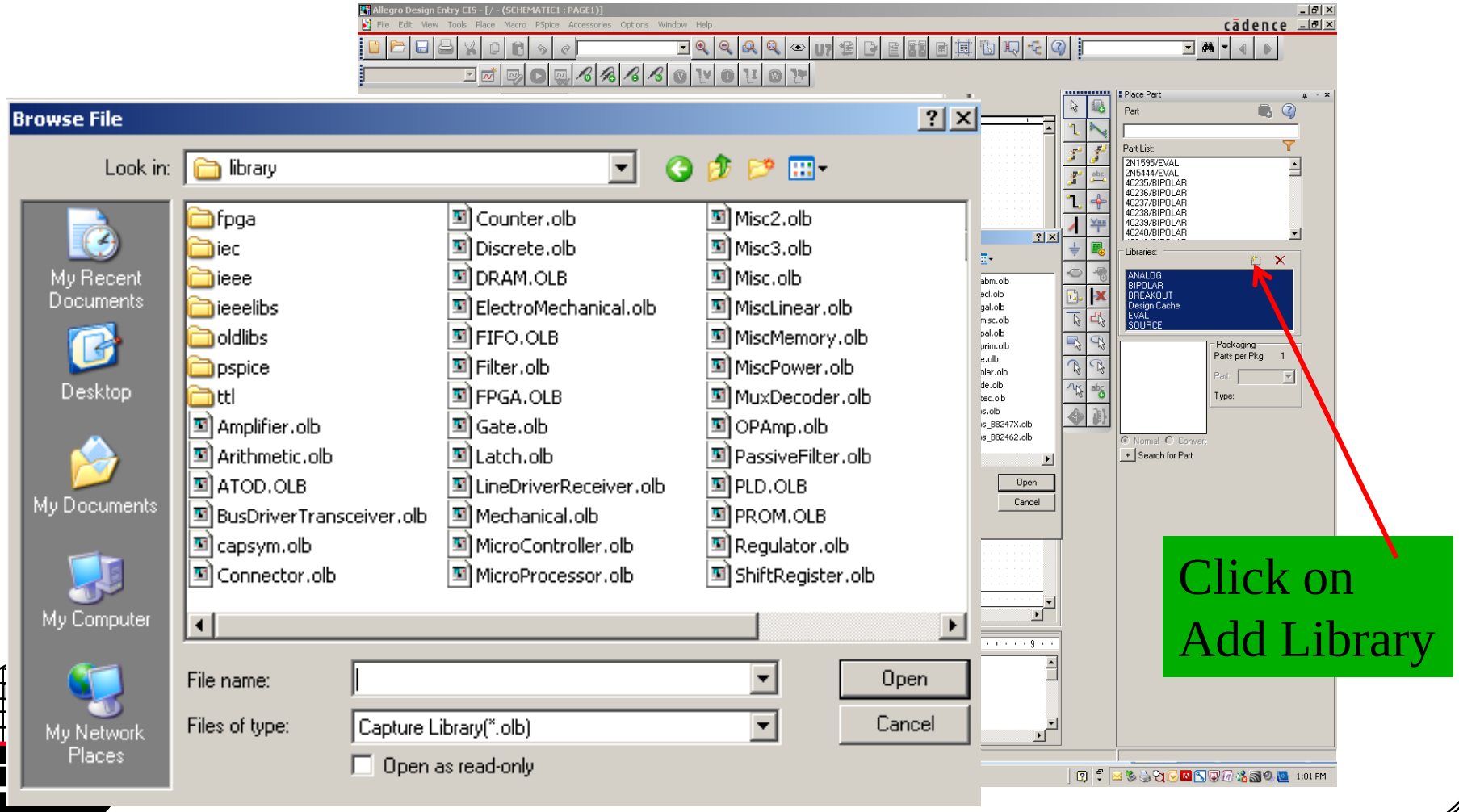

Note: SPICE requires one node to be labeled zero, either place a ground symbol labeled zero or use node label N1 icon alias = 0 (then you do not need a ground symbol)

# *Cadence – Allegro DESIGN ENTRY WORKSPACE*



# SELECT COMPONENT LIBRARIES

Place > Part (Opens component library banner on right side of space)



# *COMPONENT LIBRARY*

To place parts the project needs to be linked to some component libraries. In the PSPICE folder select

ANALOG – resistors, capacitors, inductors, switches, other

BREAKOUT – Many components but most use default SPICE models

EVAL – BJT's, FET's, Digital Logic, etc., with commercial SPICE models

SOURCE – Voltage Sources, Current Sources, etc.

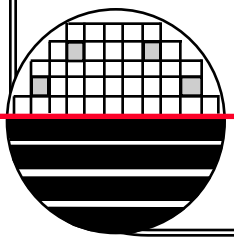
SPECIAL – Directives .IC, .INC, .PARAM, etc.

Design Cache will be automatically created to hold components used in the design. (and design specific part modifications)

Click on component name
Double click on name in parts list to place on schematic
Esc to quit placement of that part

# *EDIT SPICE FILES*

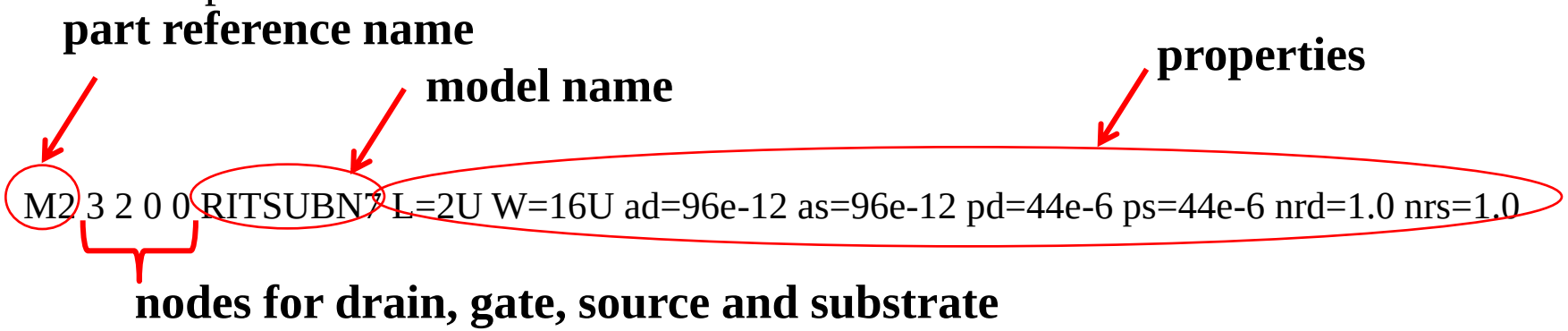
If you right click on a component in your design you can select "edit PSPICE model" . Once a part has an edited PSPICE model that model is saved in a folder linked to the project. The original model is not changed.



# MOSFET, BJT AND DIODE MODELS

Most versions of SPICE have model libraries that can be included with a SPICE input file. You could also create your own models as a simple text file and include that file with a SPICE input file for Orcad PSpice, LTSpice, or Cadence PSpice. Edit the simulation profile under the PSpice Pull down menu, the configure files tab allows text files to be added to the input file. (extension .txt or .inc)

In SPICE a transistor is defined by its **model name** and associated **properties** and its **model**. Its name and associated properties is given in the input file net list. Its model is given in the included library model file or included with the input file as a text file. For example:



# RIT MOSFET, BJT AND DIODE MODELS

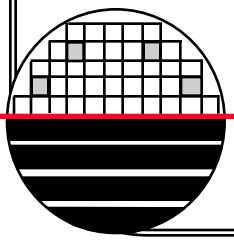
```
* The Included Model File
*2-15-2009
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8 NSS=3E11
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
.model RITMEMDIODE D IS=3.02E-9 N=1 RS=207
+VJ=0.6 CJO=200e-12 M=0.5 BV=400
*
.MODEL QRITNPN NPN (BF=416 IKF=.06678 ISE=6.734E-15 IS=6.734E-15 NE=1.259
+RC=1 RB=10 VA=109)
```

**More models for RIT components can be found on Dr. Fullers webpage http://people.rit.edu/lffeee/cmos.htm**

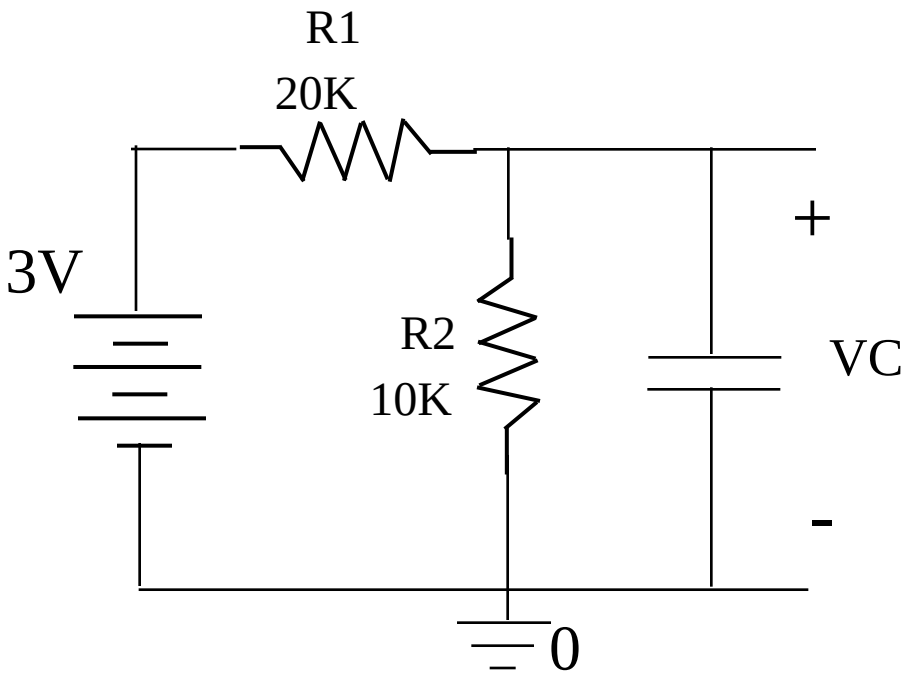
# *LABORATORY ASSIGNMENT*

Use SPICE for the following examples:

- DC analysis of RC divider circuit shown below
- Transient analysis of RC divider circuit shown below
- AC analysis of RC divider circuit shown below
- Large signal AC analysis of diode/rectifier circuit shown below



# RC DIVIDER CIRCUIT

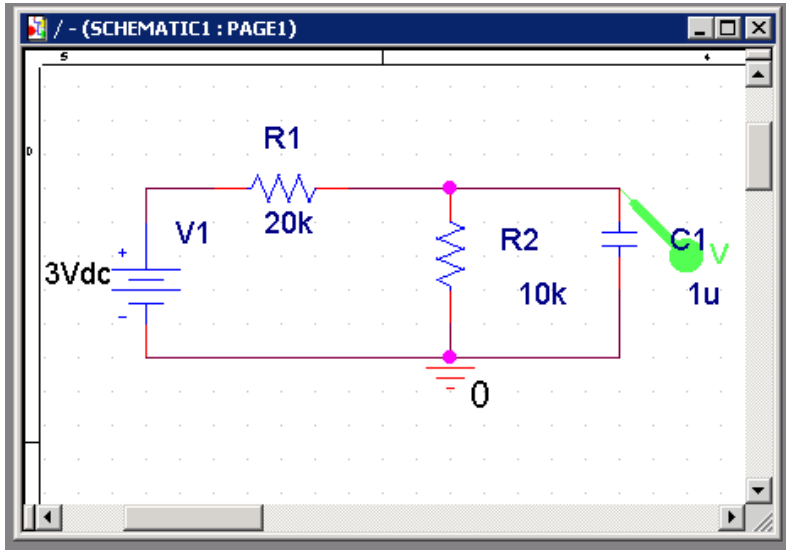


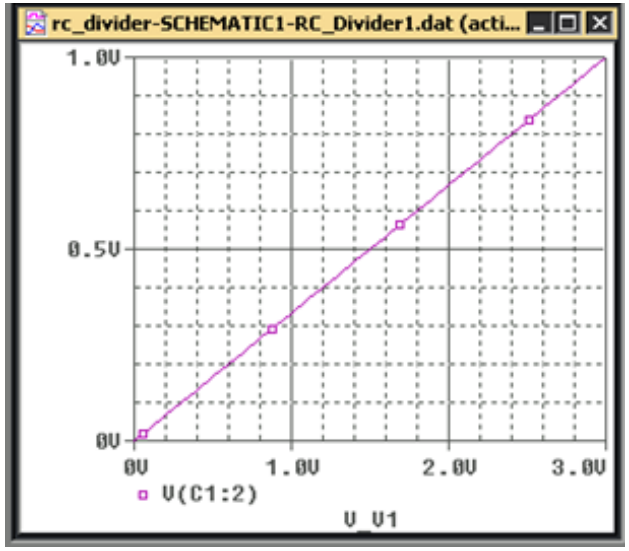

Calculate VC

Change the battery to a 3 volt step function and plot VC versus time.

Change the battery to a sinusoidal voltage source and sketch VC versus frequency

# DC SPICE ANALYSIS

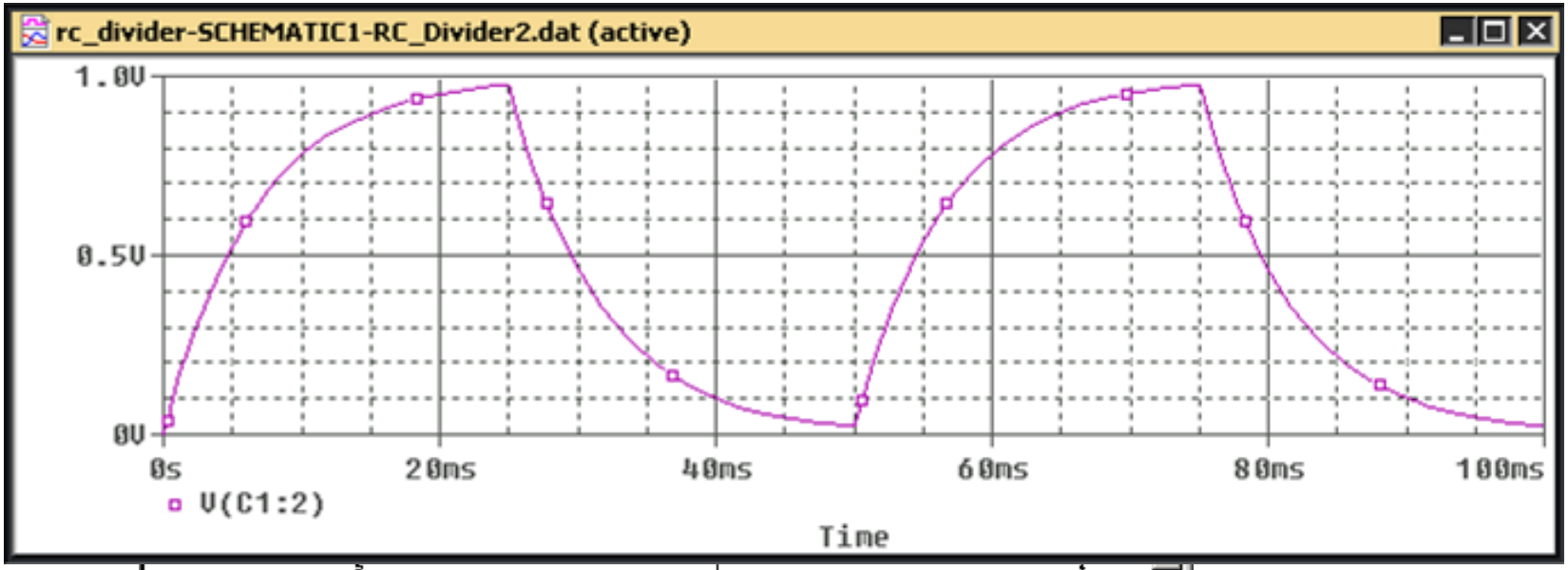


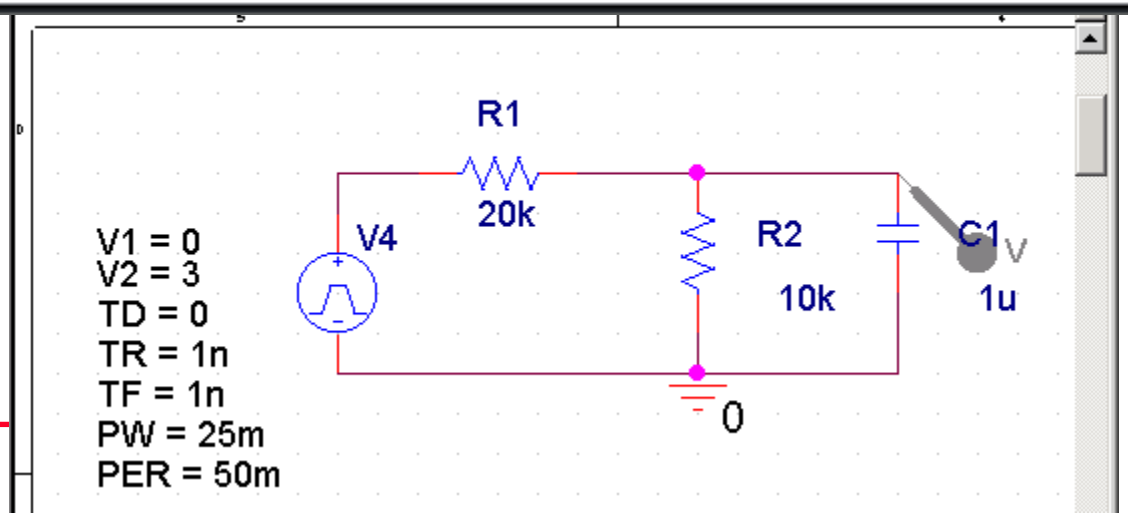




rc_divider-SCHEMATIC1-RC_Divider1.out.1

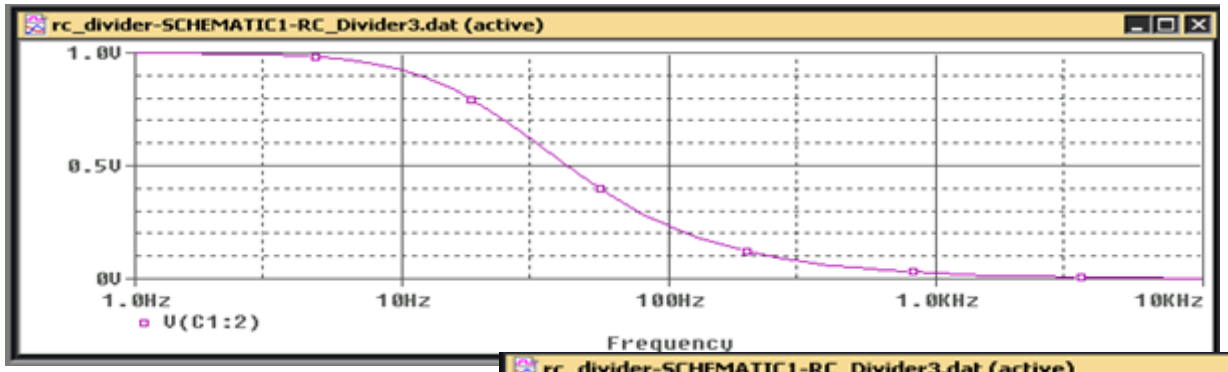
```
* From [PSPICE NETLIST] section of C:\Program Files\OrcadLite\PSpice\PSpice.ini file:
.lib "C:\Program Files\OrcadLite\Capture\Library\PSpice\nom.lib"
.lib "nom.lib"

*Analysis directives:
.DC LIN V_V1 0 3 .1
.PROBE V(*) I(*)
.INC ".\rc_divider-SCHEMATIC1.net"



**** INCLUDING rc_divider-SCHEMATIC1.net ****
* source RC_DIVIDER
C_C1          0 N00213  1u
R_R1          N00331 N00213  20k
R_R2          0 N00213  10k
V_V1          N00331 0 3Vdc

**** RESUMING rc_divider-SCHEMATIC1-RC_Divider1.sim.cir ****
.END
```

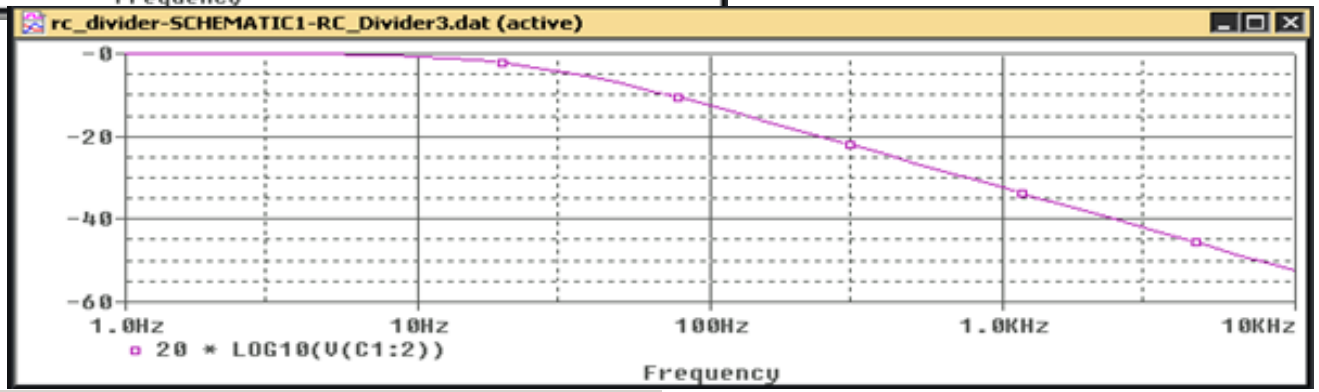
# TRANSIENT ANALYSIS

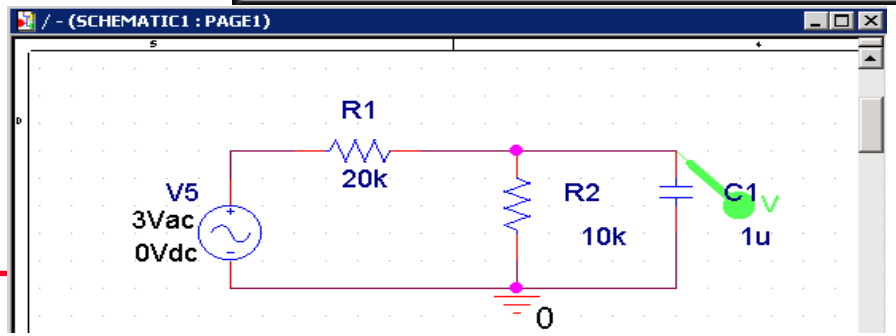


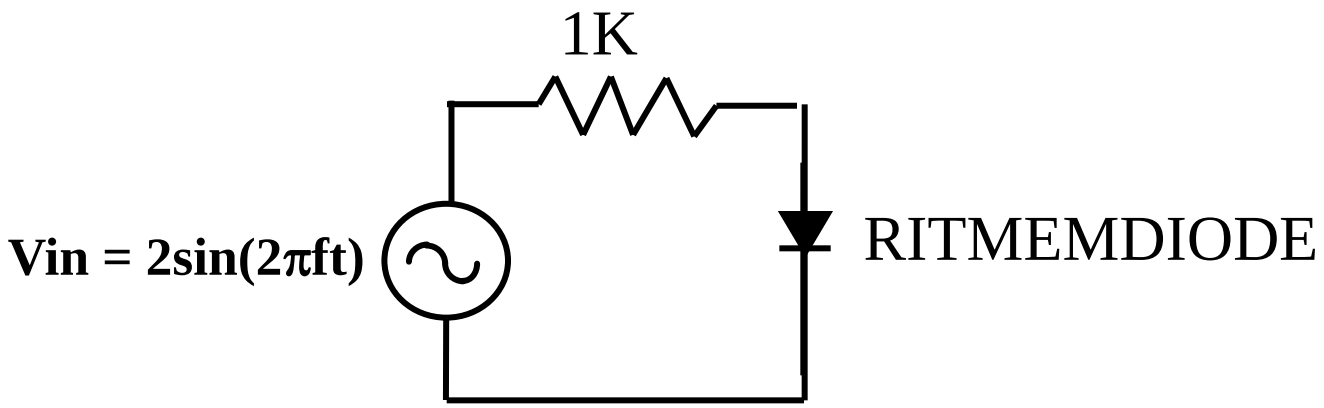
# AC ANALYSIS



# TRANSIENT ANALYSIS OF DIODE/RECTIFIER

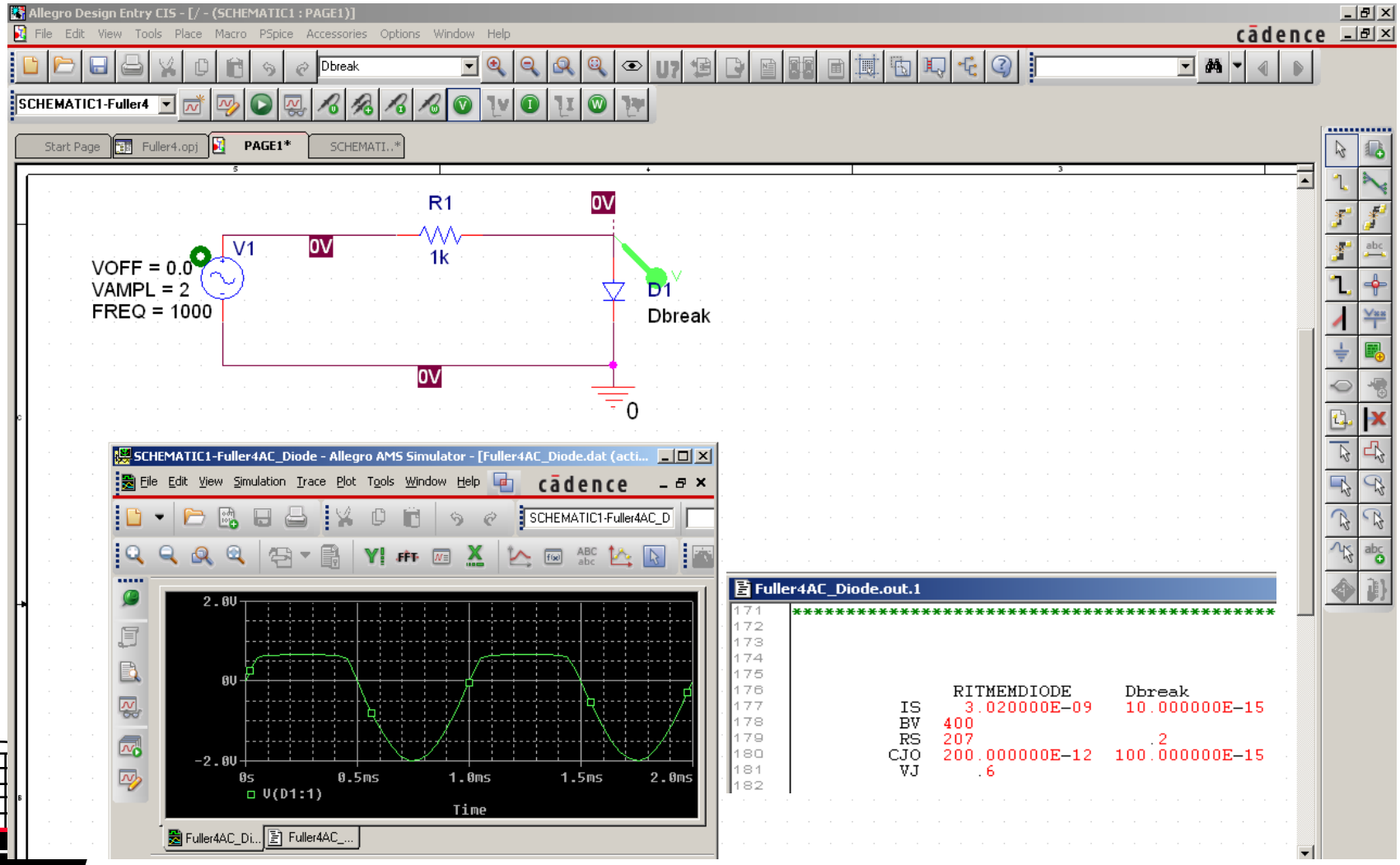



Right click on the diode and select Edit Properties, change implementation from Dbreak (or other) to RITMEMDIODE.

Edit the simulation profile under the PSpice Pull down menu, the configure files tab allows text files to be added to the input file. (extension .txt or .inc) Include the model file shown on pages below or from Dr. Fullers webpage.

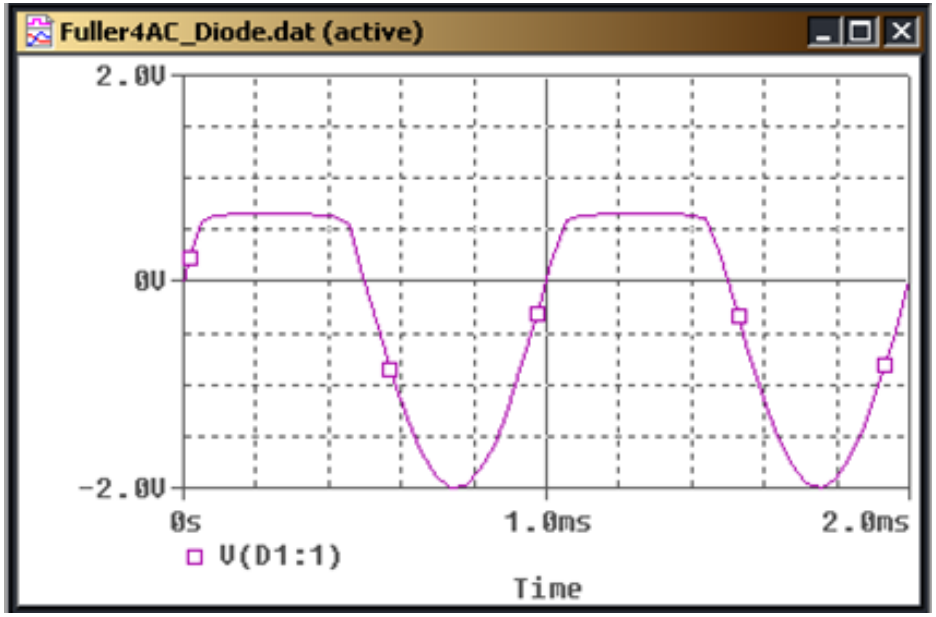
**More models for RIT components can be found on Dr. Fullers webpage http://people.rit.edu/lffeee**

# OUTPUT FILE USING Dbreak DIODE MODEL

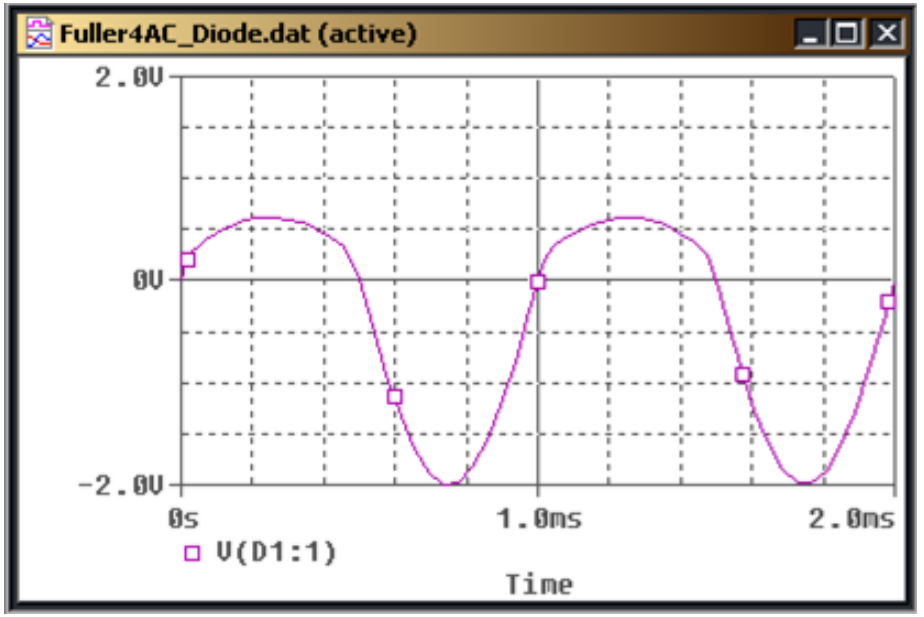


# OUTPUT USING TWO DIFFERENT DIODE MODELS

Using Dbreak Library Diode Model




Using RITMEMDIODE Diode Model



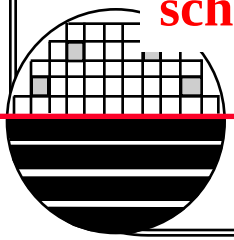

Why is there a difference in these two results?

# SPICE MODEL FOR Dbreak AND RITMEMDIODE

```
*The Library Model File for Dbreak
.model Dbreak D IS=1E-14 RS=0.2 CJO=0.1e-12
*

*The Included Model File for RITMEMDIODE
.model RITMEMDIODE D IS=3.02E-9 N=1 RS=207
+VJ=0.6 CJO=200e-12 M=0.5 BV=400
*
```

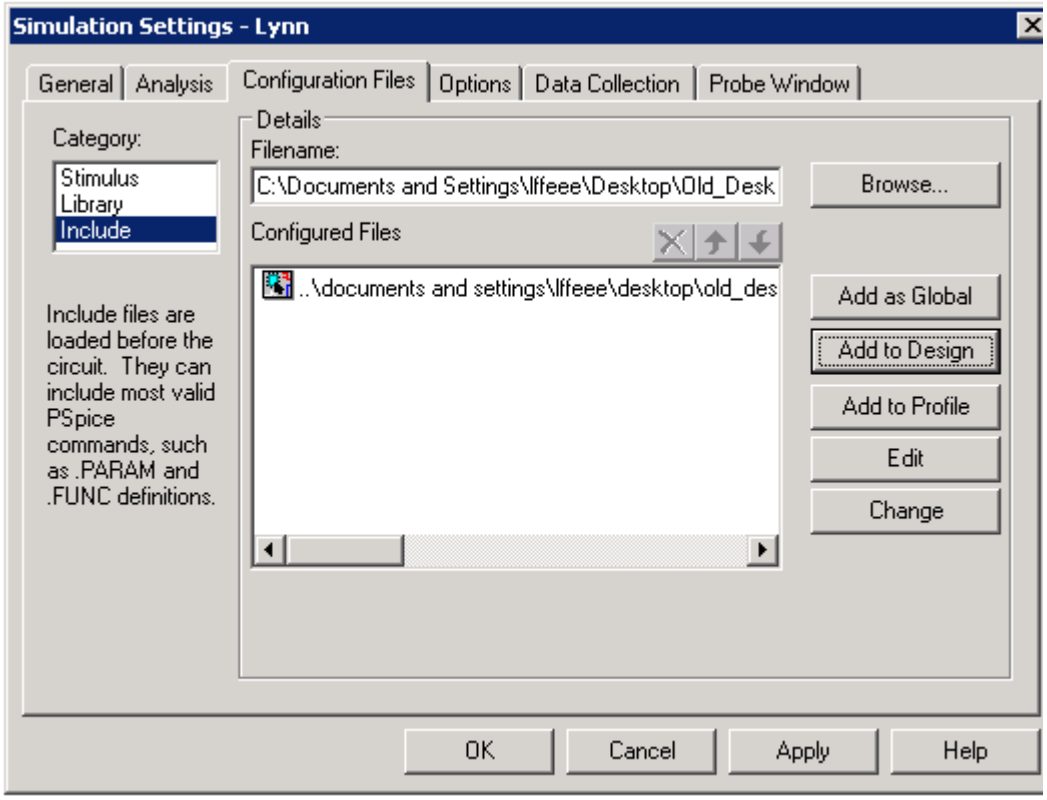
**If the model is already in a library linked to the schematic then SPICE will know where to find the model.**

**If the model is in a text file located some place on your computer then you will need to identify the path to the file. You can include files in the PSPICE simulation settings (under configuration files) or Select .Inc command from the PSPICE special library, place the icon on the schematic, double click and provide the path to the file.**



# IMPORTING THE INCLUDE FILES INTO CADENCE PSPICE

Text files can be attached to the input file in the SPICE simulation settings, configuration files, or through the .INC directive available in the PSPICE special library.

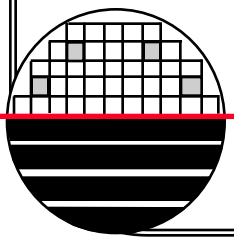


# CADENCE INITIAL CONDITION SPICE DIRECTIVE

Cadence introduces SPICE directives through its “Special” Library

.IC  V((Vin)=5) ; sets node labeled Vin to 5 volts initially.

Initial condition sets the voltage at a node to a value for DC operating point calculations.  Then removes that voltage for subsequent transient or ac analysis.  This is useful for circuits such as oscillators to help with start up.

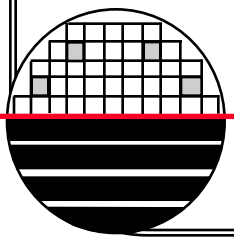


# CADENCE PARAMETER SWEEPS

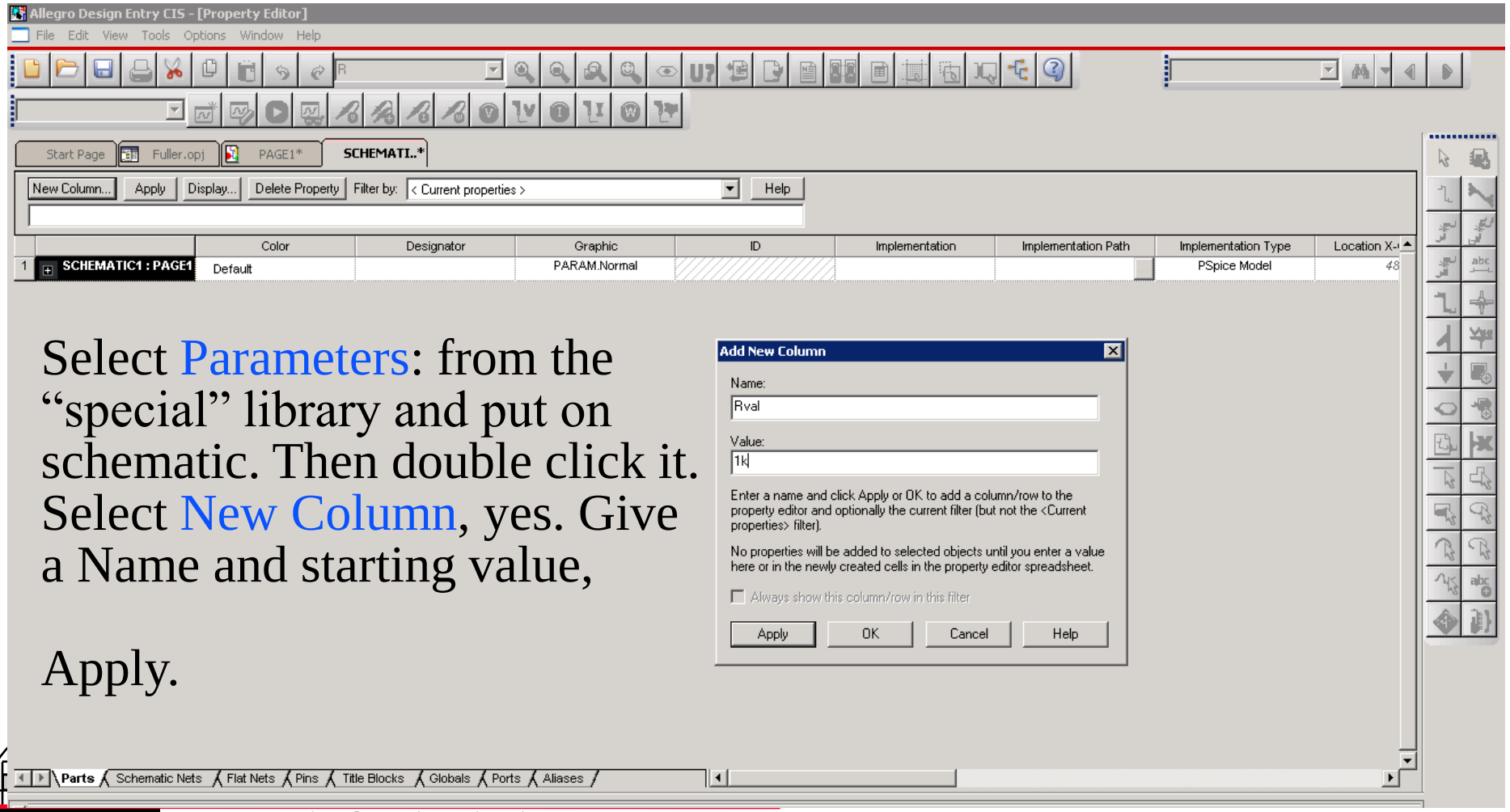
Parameter sweeps allow you to investigate the performance of your circuit for changes in some component parameter such as the value of a resistor or the width of a transistor.

Voltage sources (and other components) are automatically set up such that the voltage is a parameter that can be swept. Resistors (and other components) need to be set up so that their value can be swept.

Cadence PSPICE does this with the parameter directive in the special library.



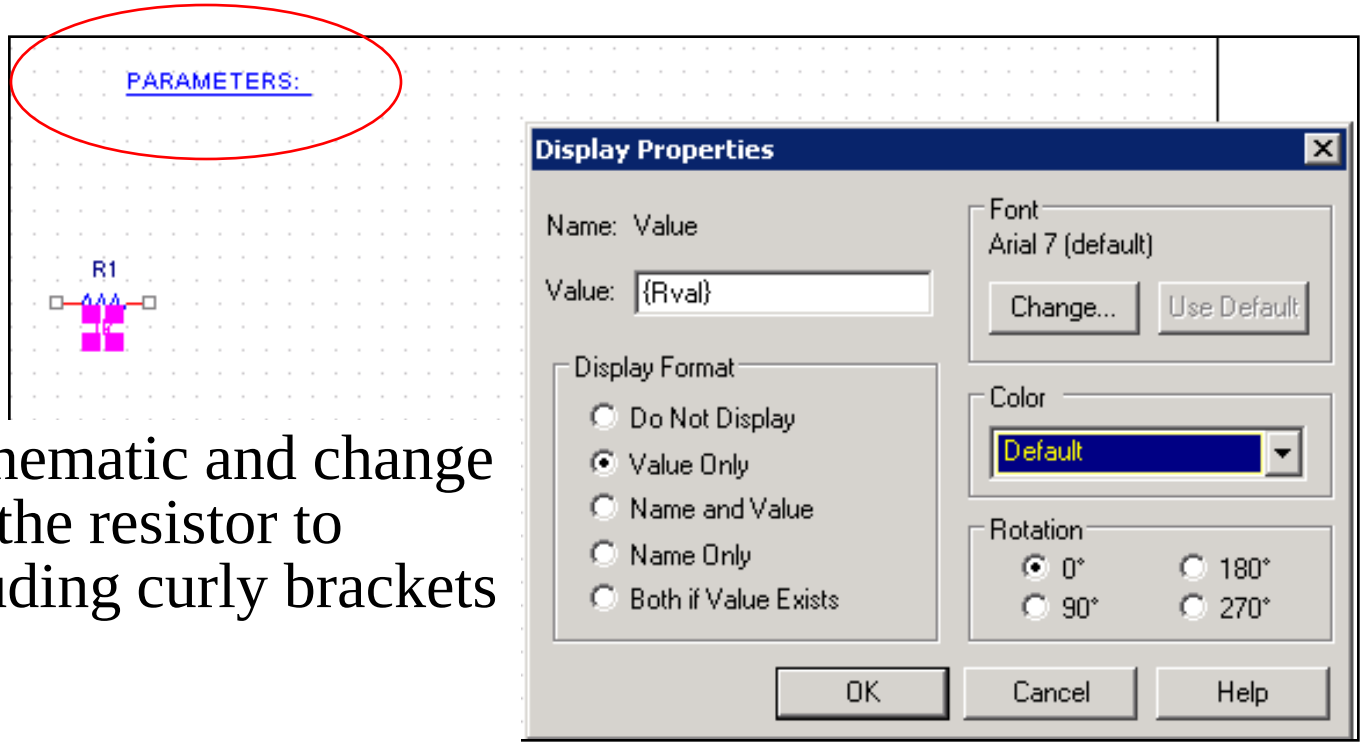
# CADENCE PARAMETER SWEEPS




Select Parameters: from the "special" library and put on schematic. Then double click it. Select New Column, yes. Give a Name and starting value,

Apply.

# CADENCE PARAMETER SWEEPS

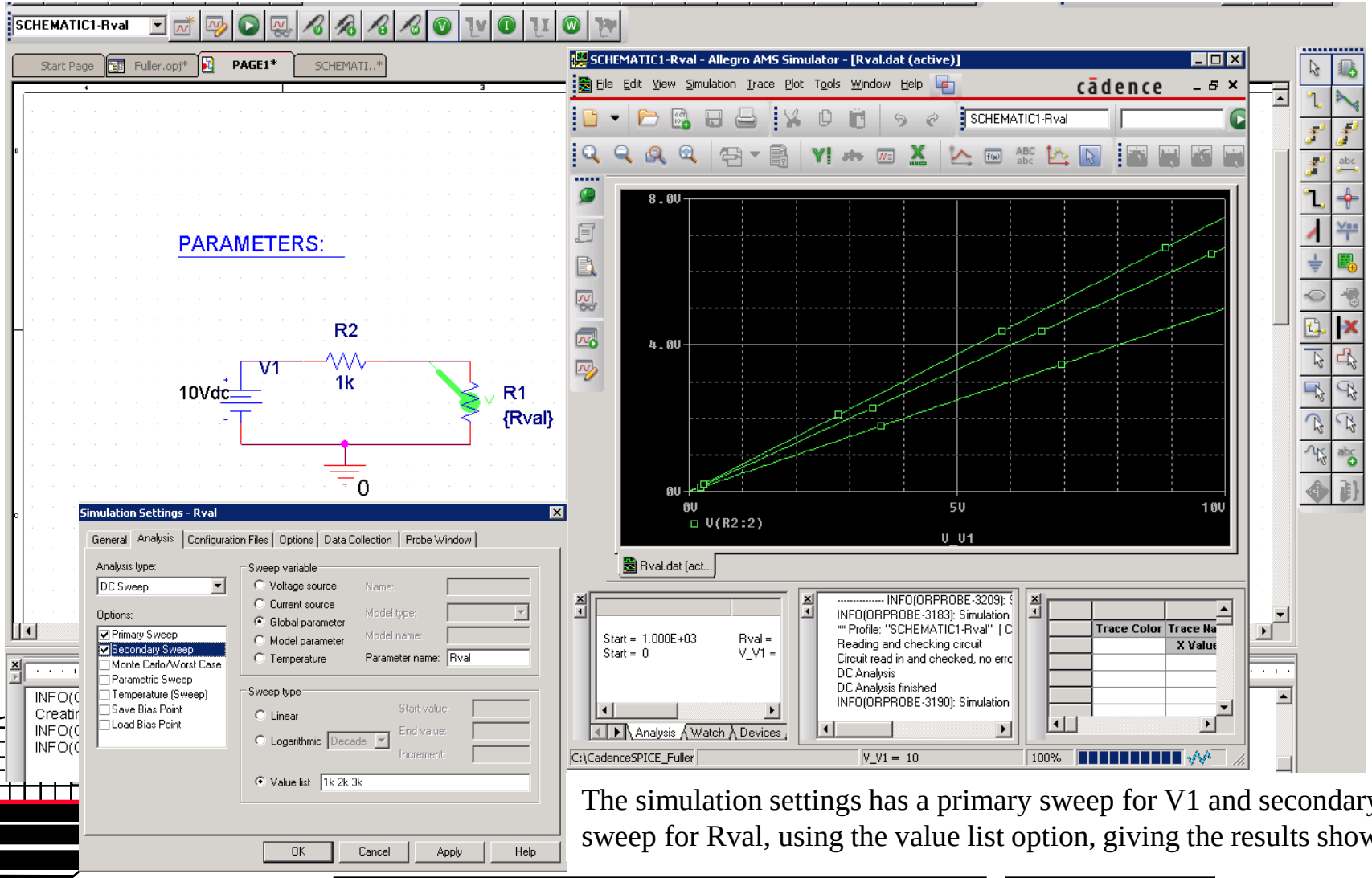



Return to schematic and change the value of the resistor to {Rval} Including curly brackets

OK

Where this is the new column name given in the attribute editor

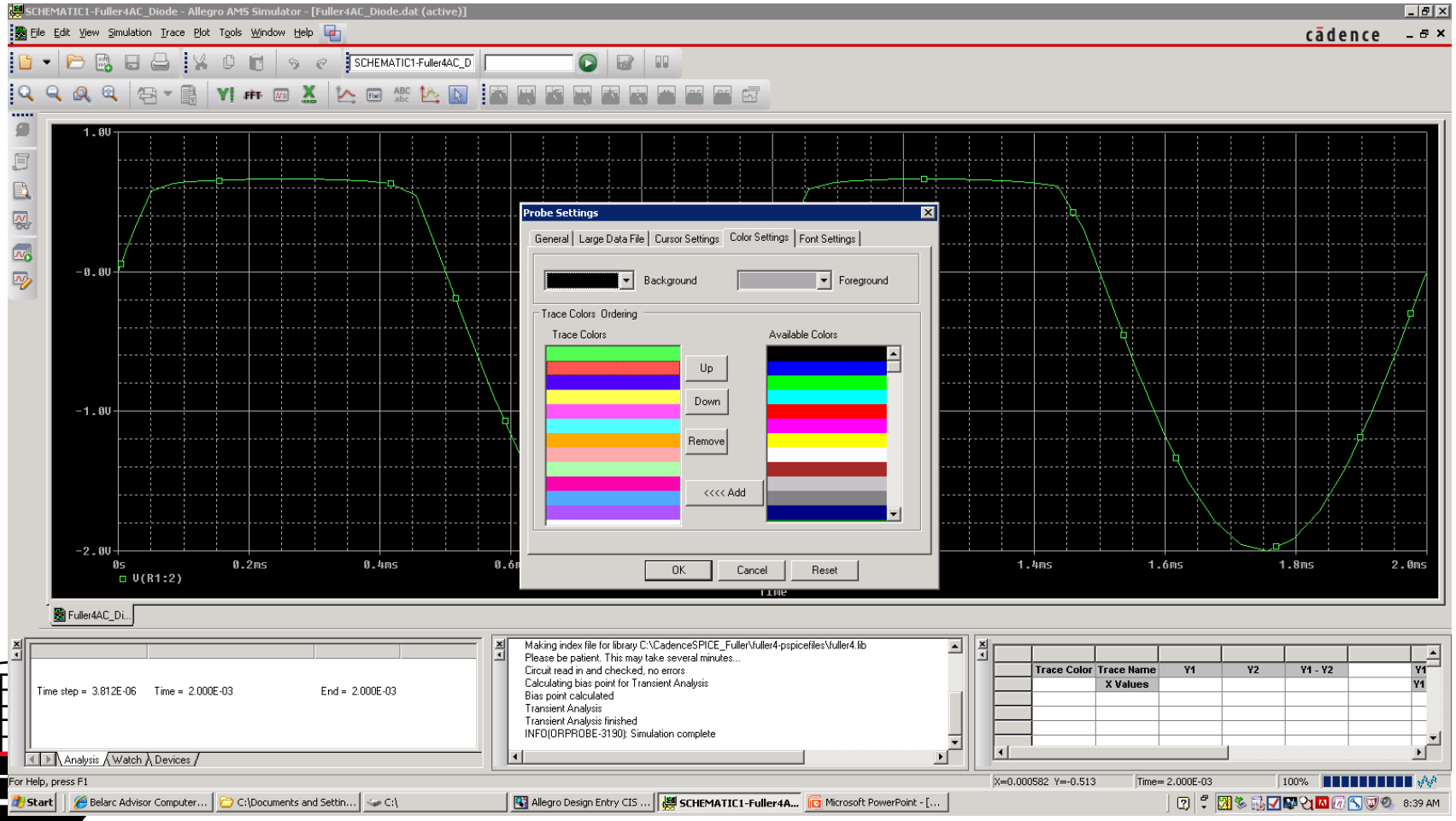
# CADENCE PARAMETER SWEEPS




The simulation settings has a primary sweep for V1 and secondary sweep for Rval, using the value list option, giving the results shown.

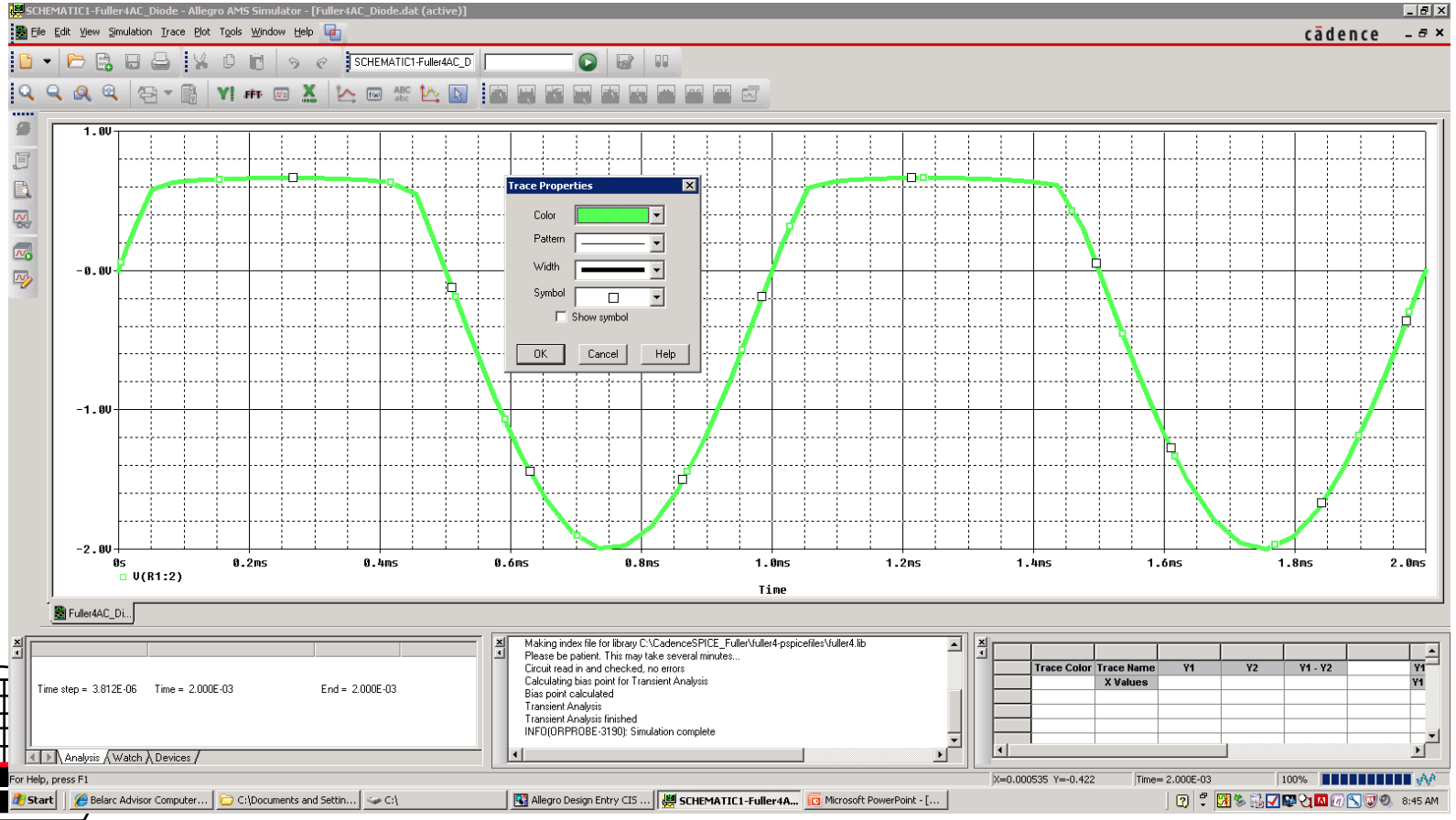
# SETTING COLORS FOR PSPICE WAVEFORM

## Tools > Options > Color Settings



# CHANGING TRACE WIDTH

After changing Background color to white and fore ground to black Trace>Trace Property>Width

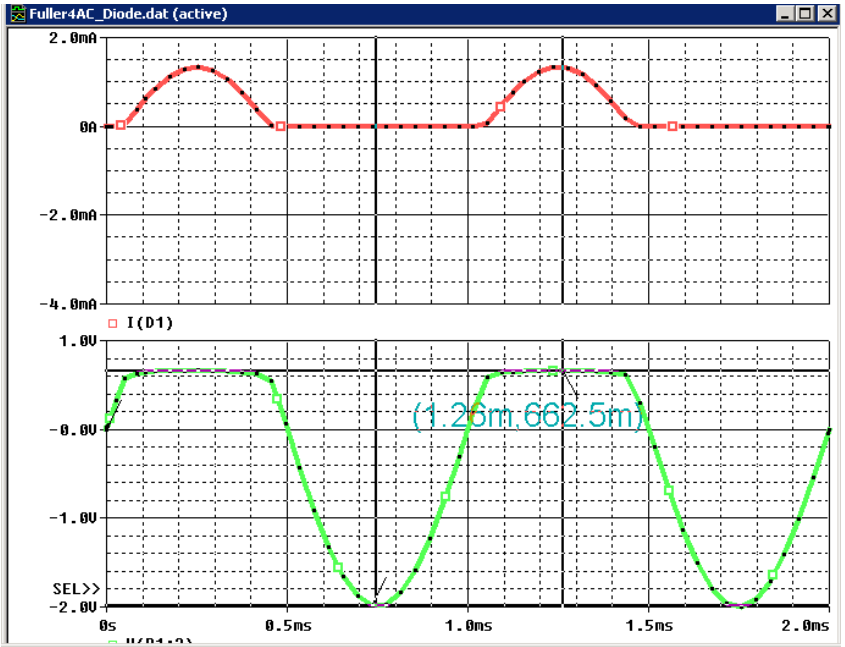


# *ADD PLOT PLANE, CURSORS, LABELS, ETC.*

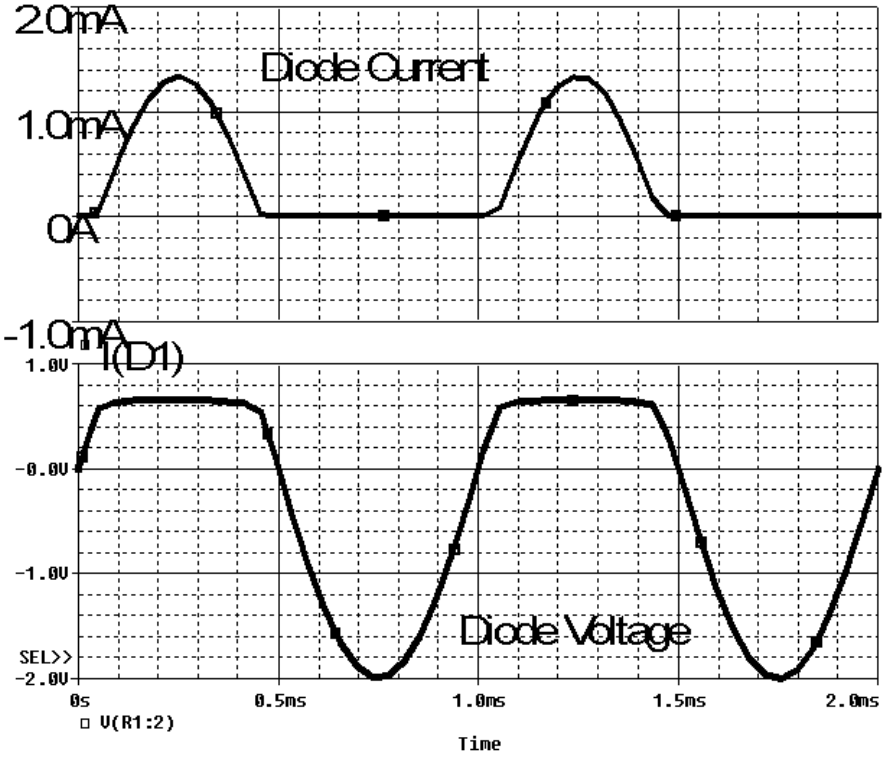
Add Plot Plane, Add Trace
Add Cursors, Then Freeze
Add Labels

Right click on trace > trace property (change line width, color, etc)

Window>Copy to clipboard > change all colors to black

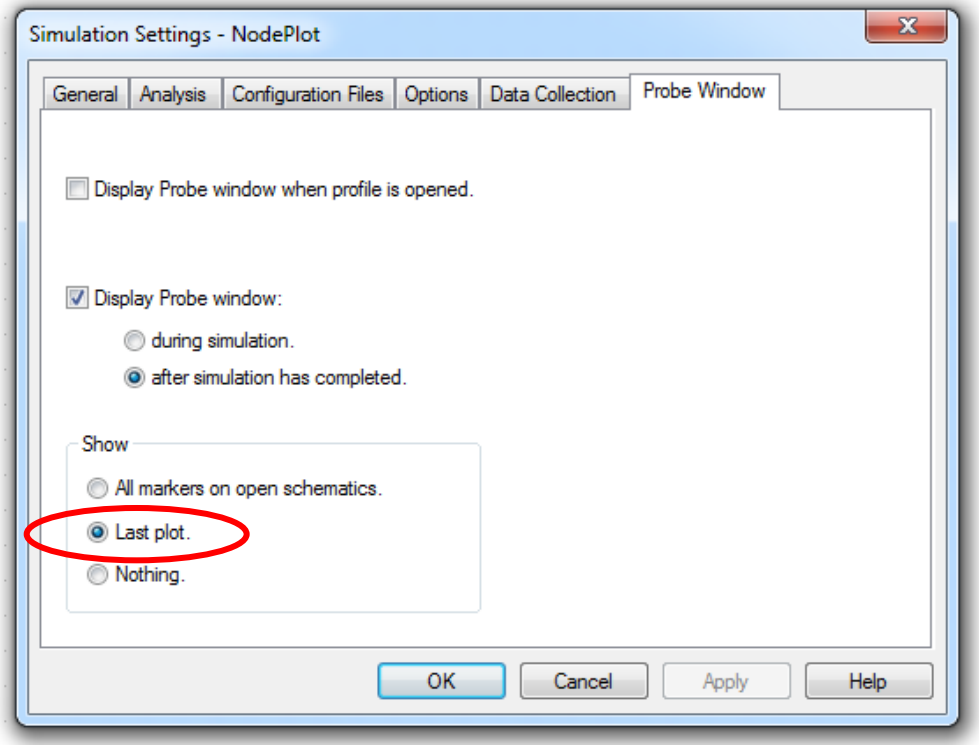



| | Trace Color | Trace Name | Y1 | Y2 | Y1 - Y2 | | Y1(Cursor1) - Y2(Cursor2) | | -2.65 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | X Values | 746.2u | 1.26m | -513.8u | | Y1 - Y1(Cursor1) | Y2 - Y2(Cursor2) | Max Y | Min Y | Avg Y |
| | CURSOR 1,2 | V(R1:2) | -1.99 | 662.5m | -2.65 | | 0 | 0 | 662.5m | -1.99 | -663.8m |
| | | I(D1) | -19.5p | 1.32m | -1.32m | | 1.99 | -661.2m | 1.32m | -19.5p | 660.0u |



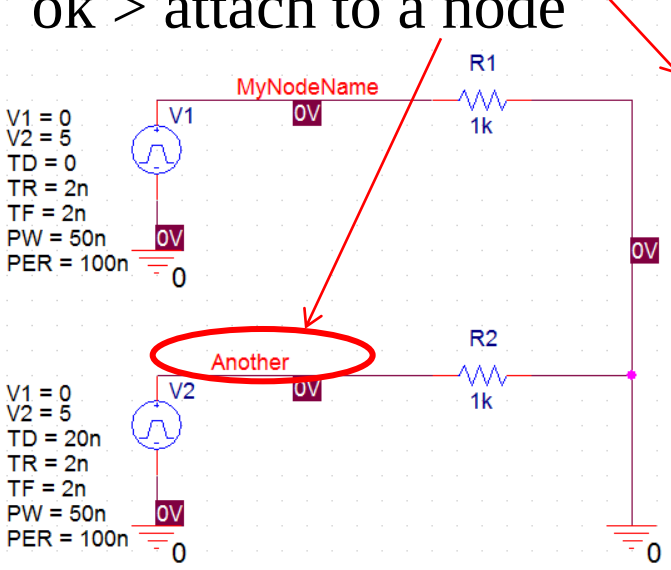
# SAVE PLOT SETTINGS

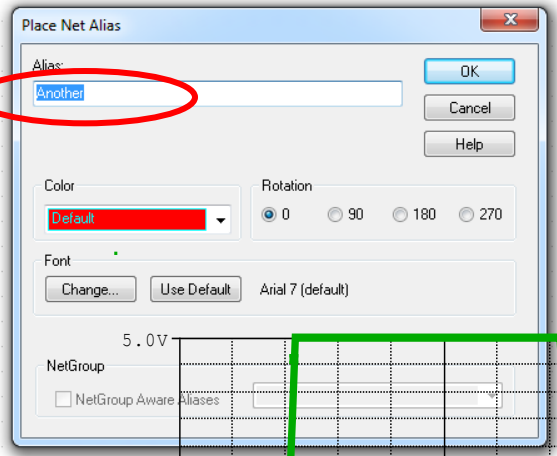
To save the plot set up, edit simulation command, select probe window and Last plot



# ADD NODE NAMES

Place > Net Alias (type in a name) > ok > attach to a node




Plot the node voltage V(another)

# *MONTE CARLO ANALYSIS*

Monte Carlo analysis allows evaluation of the impact of component variation on circuit performance. An example where resistor values are varied over their tolerance range is shown below.

**Adding Tolerances to Resistors**

Double-click the resistor symbol to which you wish to add tolerance. In the "Filter by" pull-down menu select "Orcad-Pspice". At the far right end of the table, under the tolerance label, enter the desired tolerance value in percentage format (*i.e.*, 10%). Click "Apply" in the upper left-hand corner to activate the value entered. Close the properties window.

**Setup Simulation Profile**

For a new simulation:Hit "New Simulation Profile". Input a profile, leave the "Inherited from" empty. Follow "For existing profile" steps from here on.
For existing profile: Hit "Edit Simulation Settings". Simulation Settings window will pop up. Choose "Time domain (transient)" under Analysis type. Input proper time interval for "Run to time" (*i.e.*, about 1 period). Select "Monte Carlo/Worst Case" in Options. Type in the name for "Output variable" (*i.e.*, V(RL:2)). Input "Number of runs" (usually given).

(Continued)

# *MONTE CARLO ANALYSIS (cont'd)*

Type any number between 1 and 32767 into the "Random number seed" box. Click "More Settings" button on the lower right-hand corner. Choose "the maximum value (MAX)" from the pull-down menu. Click Apply. Hit OK, then OK again.

**Running Capture CIS**

Hit the blue "Run Pspice" button on the tool bar . [Pspice window will pop up and simulation should be running at this time] Hit OK to close the window that pops up. The graph will then pop up with the voltage you wanted, provided you placed a voltage probe in the circuit. If it's blank it is because you did not place a probe in the circuit. You can do so at this time and the corresponding voltage curve should appear immediately on the graph.

**How to Get a Performance Analysis Layout (Histogram)**

In the top menu, click on "Trace" and then "Performance Analysis".
In the window that pops up, click on the "Wizard" button at the bottom.
Click NEXT. Select "Max" from the list and click NEXT.
In the text box, type in the same thing you put in the "Output Variable" for the Monte Carlo profile (*i.e.*, V(RL:2)).

# *REFERENCES*


1. MOSFET Modeling with SPICE, Daniel Foty, 1997, Prentice Hall, ISBN-0-13-227935-5
2. Operation and Modeling of the MOS Transistor, 2nd Edition, Yannis Tsividis, 1999, McGraw-Hill, ISBN-0-07-065523-5
3. UTMOST III Modeling Manual-Vol.1. Ch. 5. From Silvaco International.
4. ATHENA USERS Manual, From Silvaco International.
5. ATLAS USERS Manual, From Silvaco International.
6. Device Electronics for Integrated Circuits, Richard Muller and Theodore Kamins, with Mansun Chan, 3rd Edition, John Wiley, 2003, ISBN 0-471-59398-2
7. ICCAP Manual, Hewlet Packard
8. PSpice Users Guide.