ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Introduction to Computer Aided Design (CAD)

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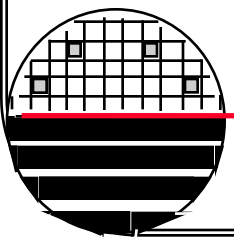
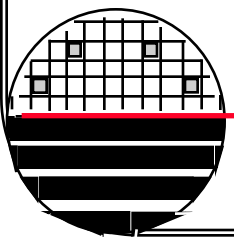


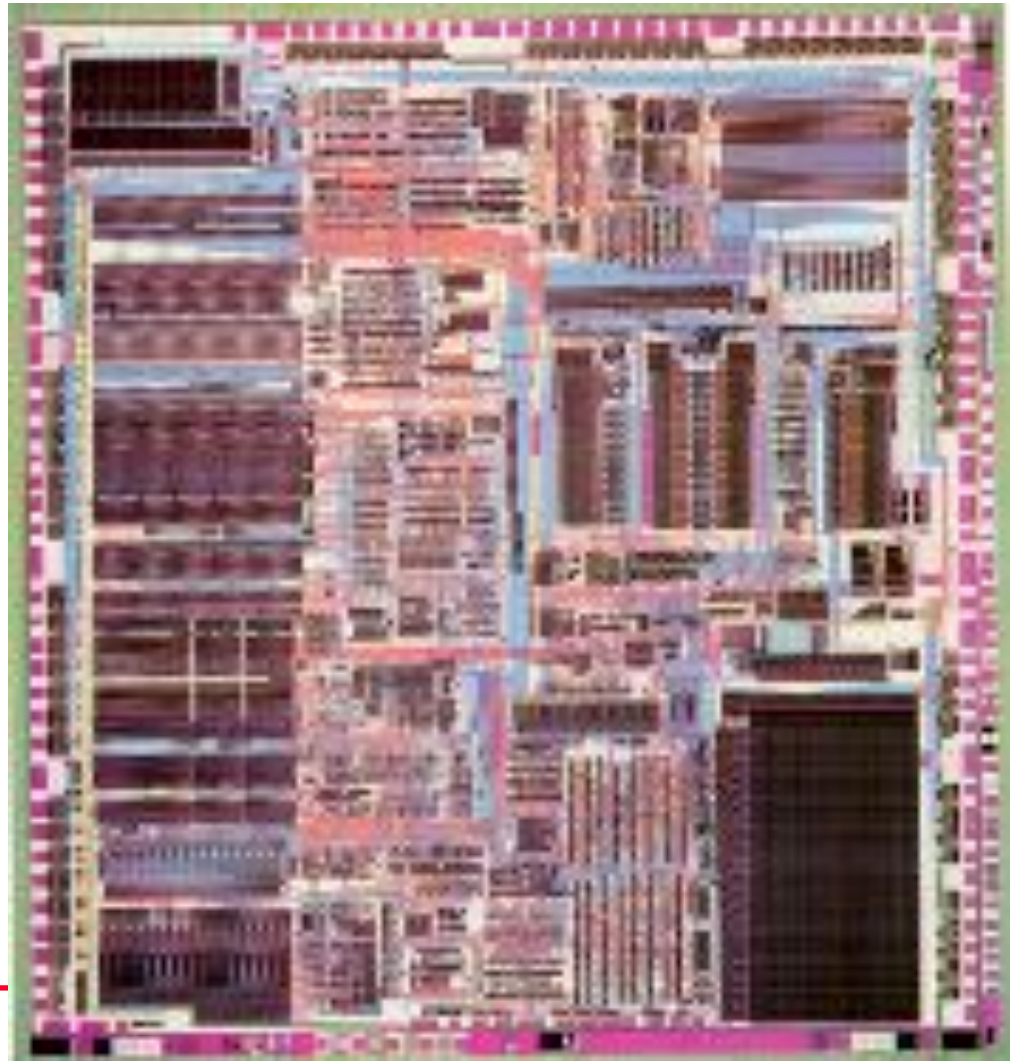
OUTLINE

The need for Computer Aided Design
The CAD Process
Levels of Abstraction
RIT's Metal Gate PMOS Process
Layout Design Rules
Layout Vs Schematic Checking
Resistor Design
Inverter, NOR, NAND Design
RS FF Design
Ring Oscillator
Maskmaking
Design Project
References
Review Questions



THE NEED FOR CAD

With millions of transistors per chip it is impossible to design with no errors without computers to check layout, circuit, process, etc.



COMPARISON OF DESIGN METHODOLOGIES

Full Custom Design

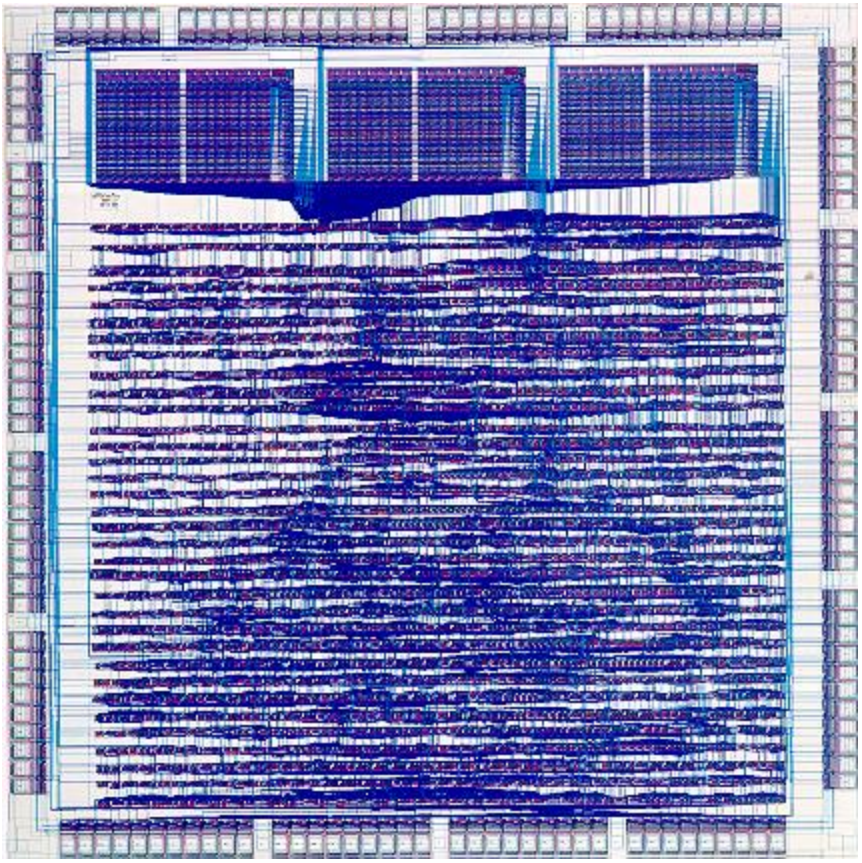
Direct control of layout and device parameters
Longer design time
but faster operation
more dense

Standard Cell Design

Easier to implement
Limited cell library selections

Gate Array or
Programmable Logic Array Design

Fastest design turn around
Reduced Performance



STAGES IN THE CAD PROCESS

Problem Specification

Behavioral Design

Functional and Logic Design

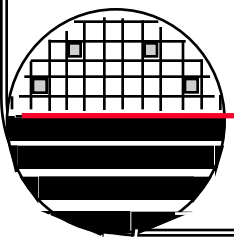
Circuit Design

Physical Design (Layout)

Fabrication Technology CAD (TCAD)

Packaging

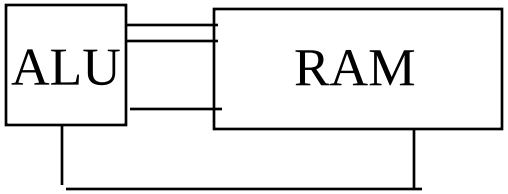
Testing



DESIGN HEIRARCHY - LEVELS OF ABSTRACTION

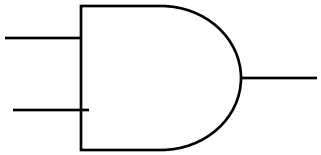
A = B + C
if (A) then X: = Y

Behavioral Model

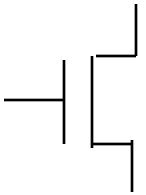


Block-Functional Model

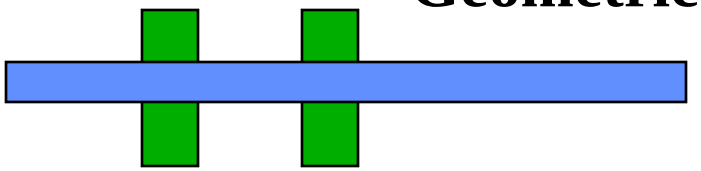
Gate-Level Model

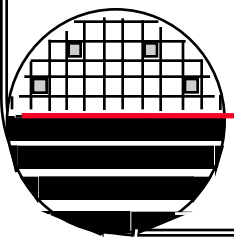


Electrical Model
(Transistor level Model)



Geometric Model





RIT METAL GATE PMOS PROCESS

PMOSFET

P channel, Metal Oxide Semiconductor Field Effect Transistor

The basic unit of distance in a scalable set of design rules is called

Lambda, λ

For the current Metal Gate PMOS process λ is ten microns (10 µm)

The process has four mask layers, they are:

Diffusion 

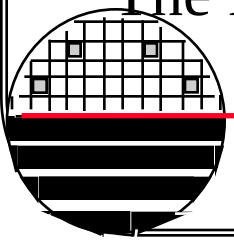
Thin Oxide 

Contact Cuts 

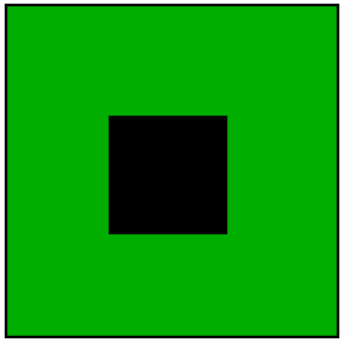
Metal 

The following rules are shown as top views

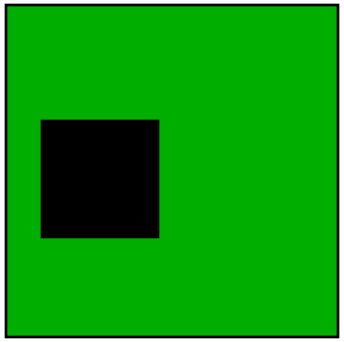
(looking down on the mask layers)



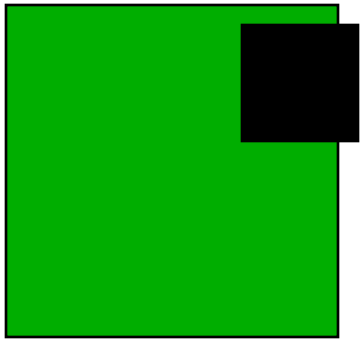
LAYOUT RULES



Perfect Overlay



Slight Overlay
Not Fatal



Misalignment
Fatal

Layout rules prevent slight misalignment from being fatal. Also, rules help make device performance consistent (minimum width for resistor will make values more consistent)

RULES FOR THE DIFFUSION LEVEL

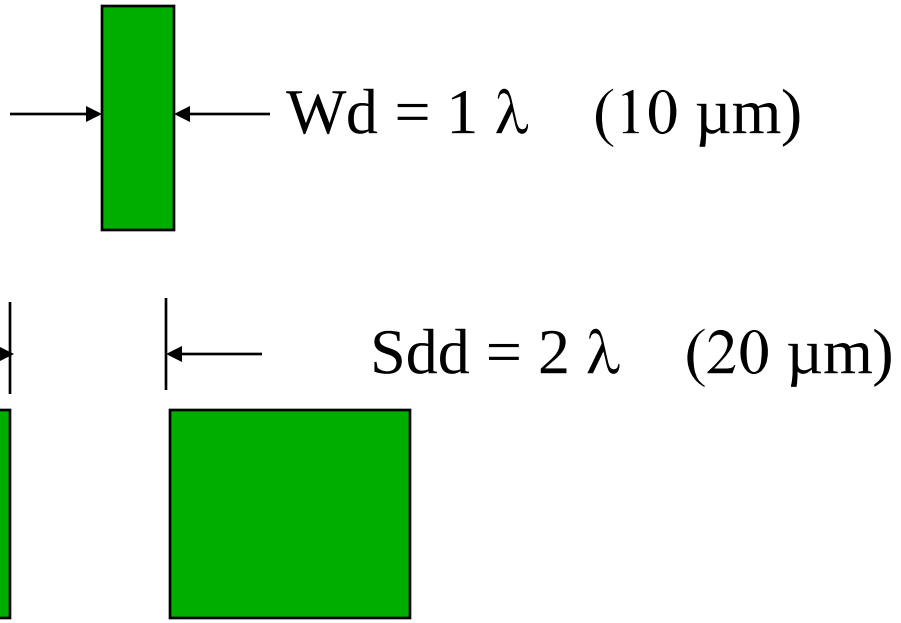
Layer 1 - diffusion (green)

Rule 1.1 Minimum Width

Wd = 1 λ

Rule 1.2 Minimum Spacing

Sdd = 2 λ



10 by 10 µm

RULES FOR THE THIN OXIDE LEVEL

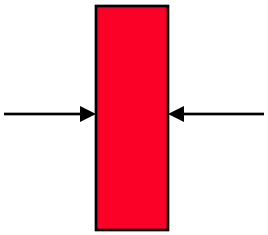
Layer 2 - Thin Oxide(red)

Rule 2.1 Minimum Width

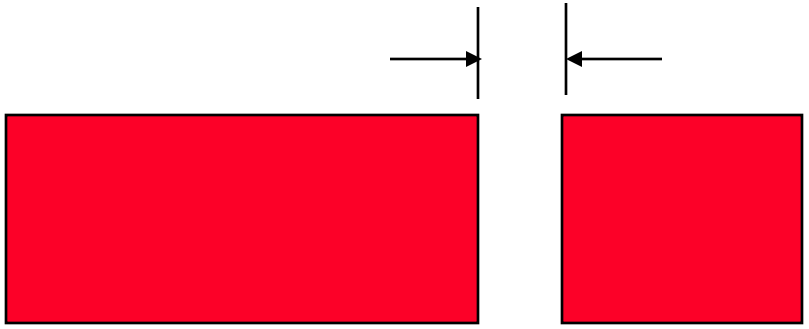
Wo = 1 λ

Rule 2.2 Minimum Spacing

Soo = 1λ



Wo = 1 λ (10 µm)



Soo = 1λ (10 µm)

10 by 10 µm

RULES FOR THE CONTACT CUT LEVEL

Layer 3 - Contact Cut (black)

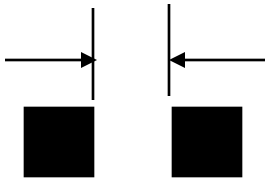
Rule 3.1 Minimum Width

Wc = 1 λ

Wmin = 1 λ (10 µm)

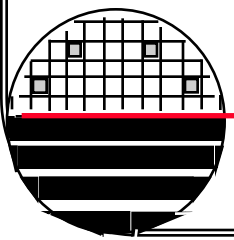
Rule 3.2 Minimum Spacing

Scc = 1 λ



Smin = 1 λ (10 µm)

10 by 10 µm



RULES FOR THE METAL LEVEL

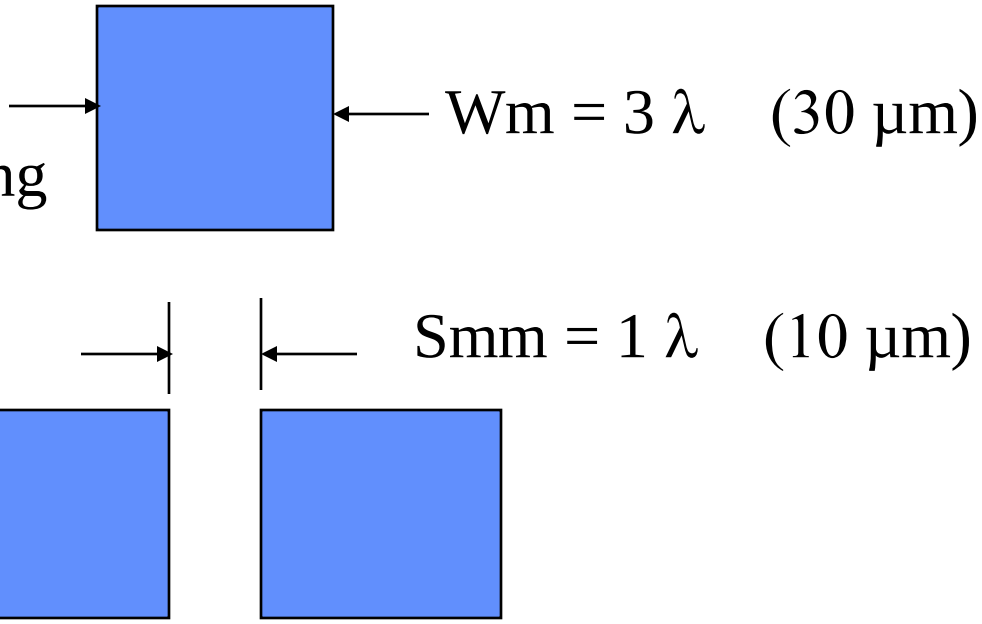
Layer 4 - metal (blue)

Rule 4.1 Minimum Width

Wm = 3 λ

Rule 4.2 Minimum Spacing

Smm = 1 λ



10 by 10 µm

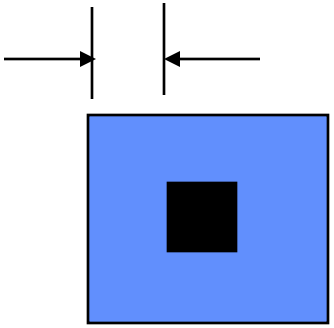
RULES FOR THE DIFFUSION, CONTACTS AND METAL LEVELS TOGETHER

Layer 1,2,3 Overlay (Extension)

Rule 3.3 Minimum Extension of metal beyond contact cut

Emc = 1 λ

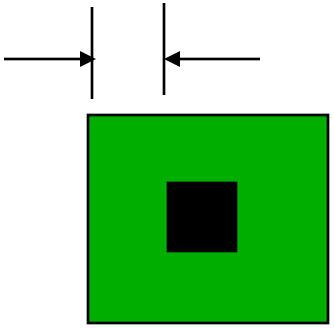
Emc= 1 λ (10 µm)



Rule 1.3 Minimum Extension of diffusion beyond contact cut

Edc = 1 λ

Edc= 1 λ (10 µm)



10 by 10 µm

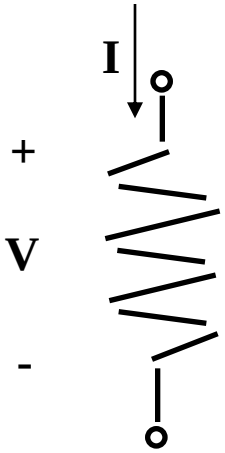
RESISTOR DESIGN

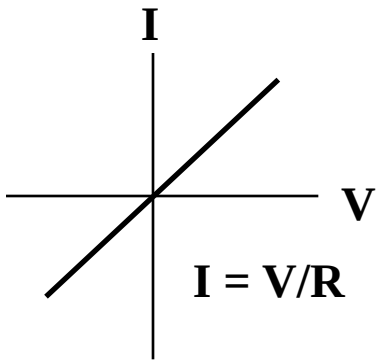
A resistor is a device with a linear relationship between current through and voltage across a device. (Also goes through the origin, that is if I=0 then V=0) The value of the resistance for a thin sheet of a material is given by:

$$R = \rho_s L/W$$

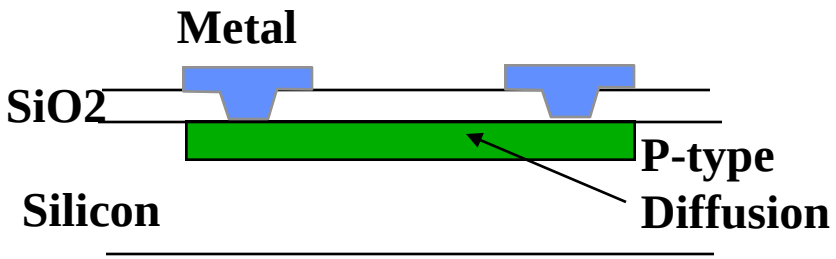
where ρ_s is the sheet resistance given by the process (for us ~100 ohms)

Schematic symbol

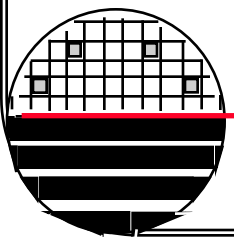




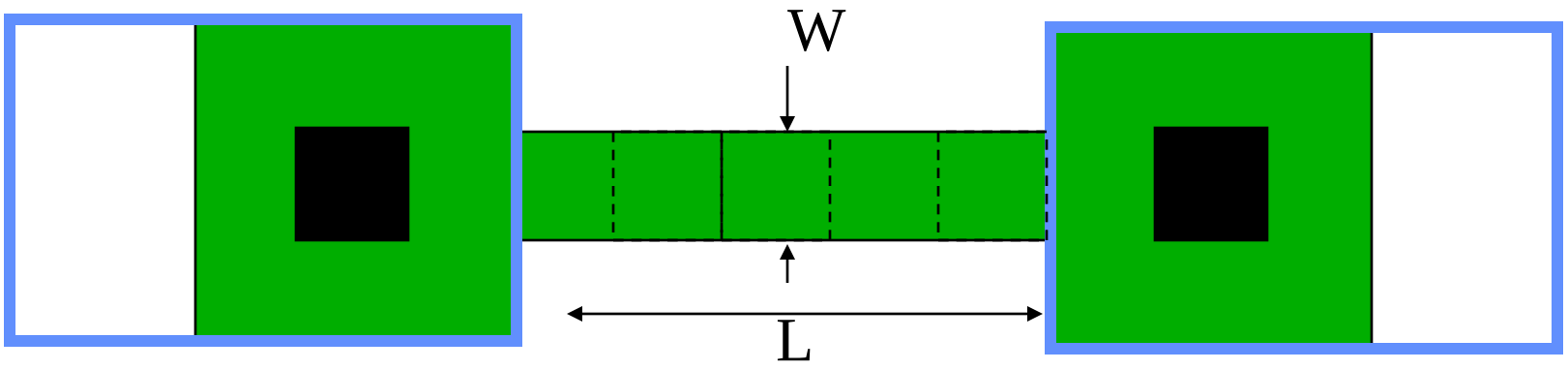
I-V characteristics



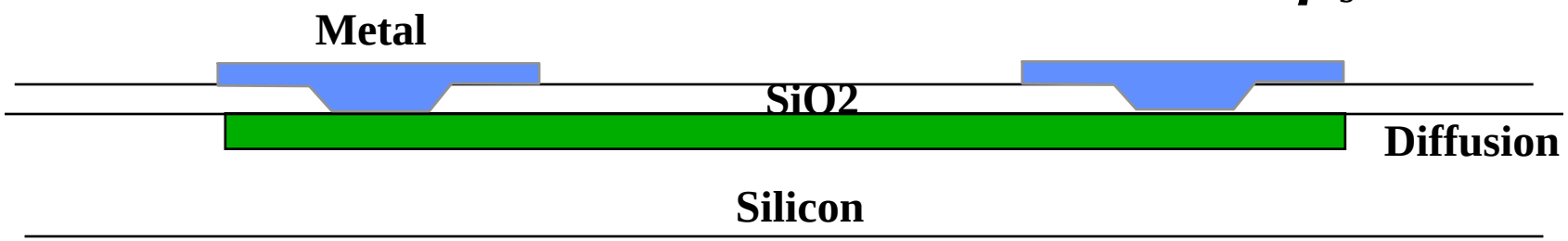
Cross section



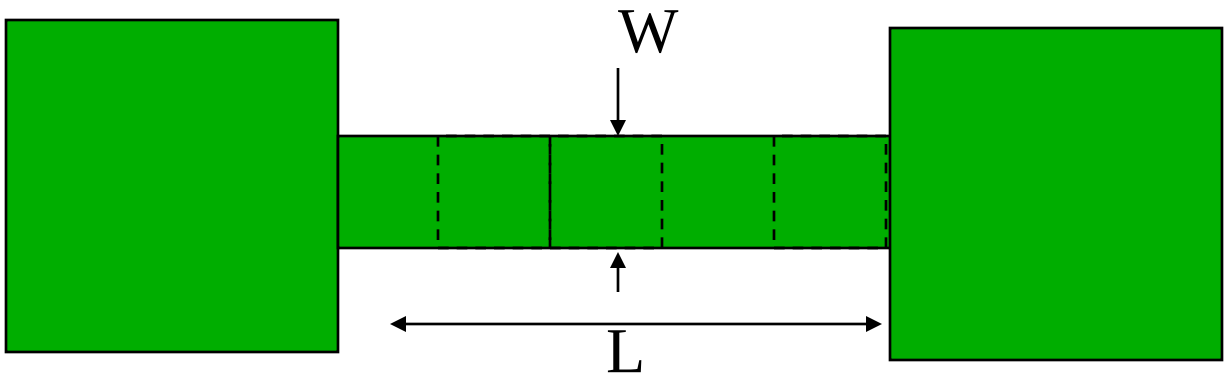
DIFFUSED RESISTOR EXAMPLE ALL LAYERS



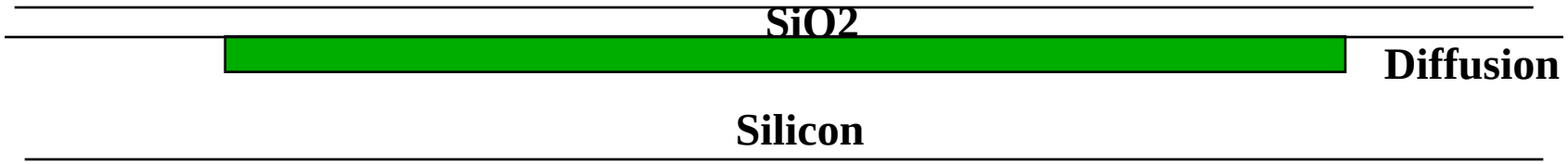
$$R = \rho_s \, L/W$$



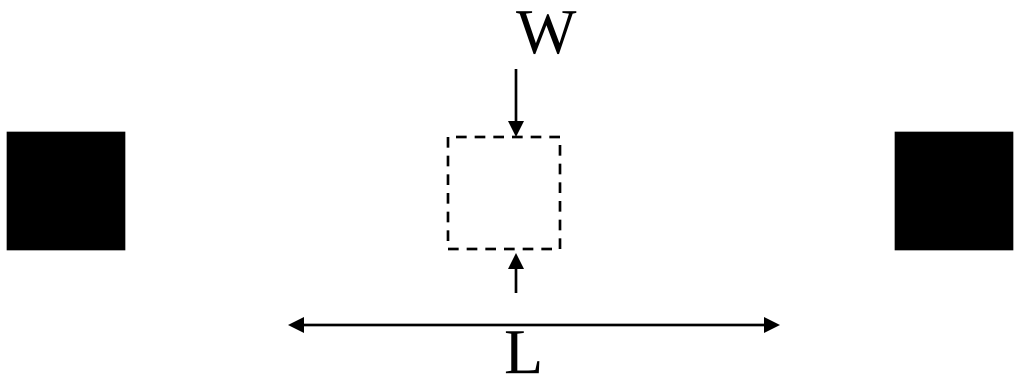
DIFFUSED RESISTOR EXAMPLE
DIFFUSED LAYER



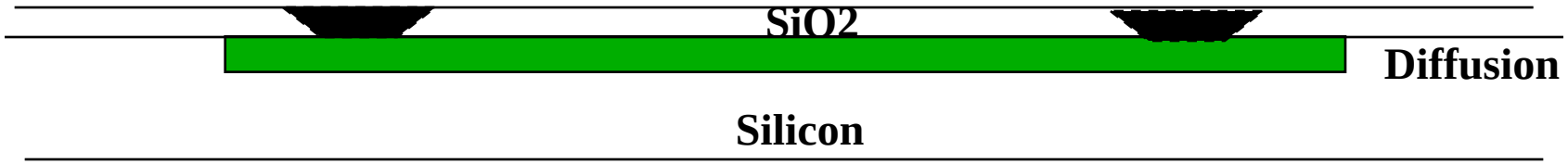
$$R = \rho_s \, L/W$$



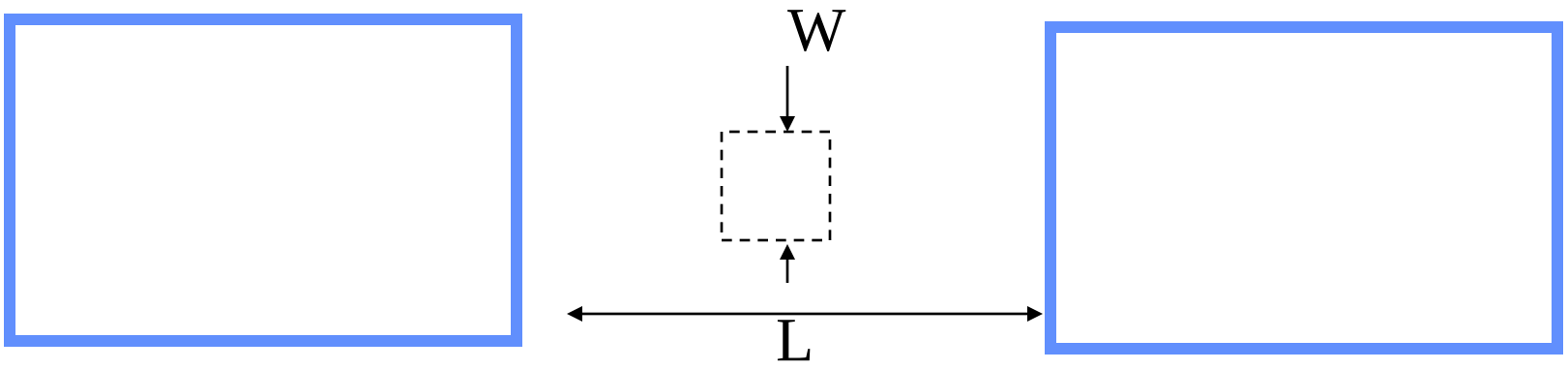
DIFFUSED RESISTOR EXAMPLE
CONTACT CUT LAYER



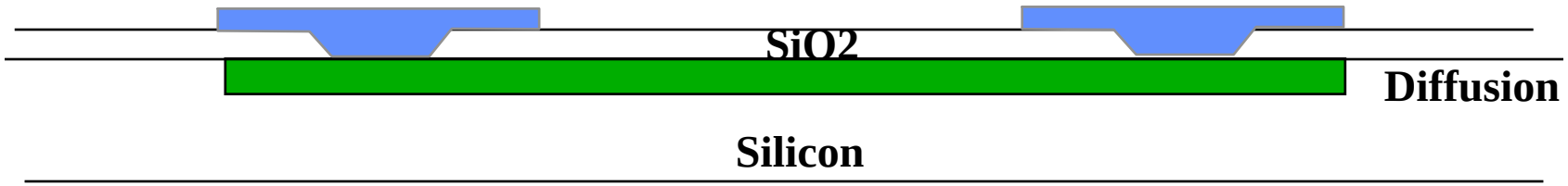
$$R = \rho_s \, L/W$$

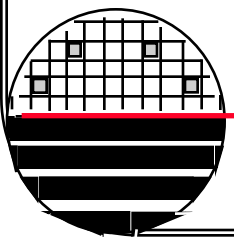


DIFFUSED RESISTOR EXAMPLE
METAL LAYER



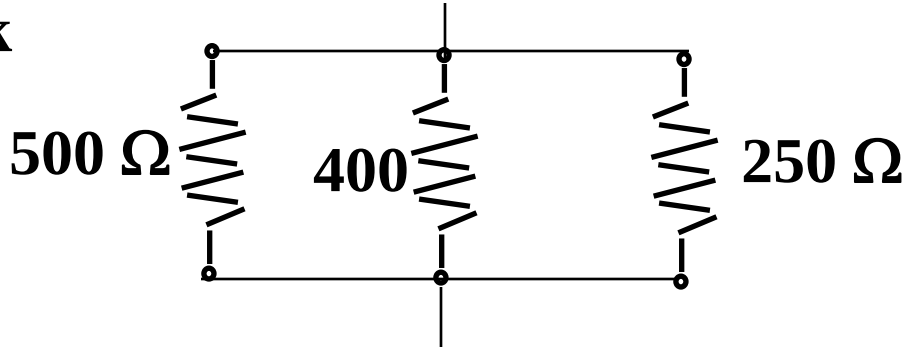
$$R = \rho_s L/W$$



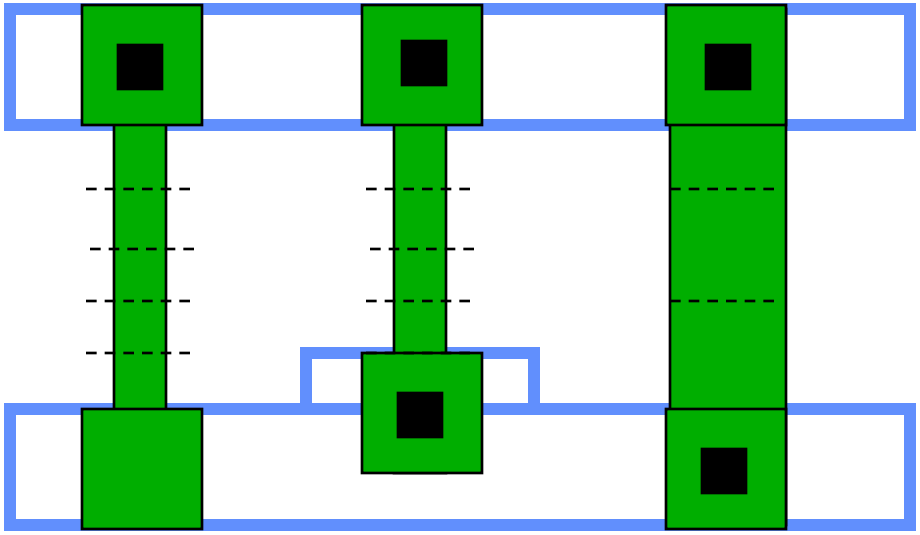


LAYOUT VERSUS SCHEMATIC (LVS) CHECKING

Desired resistor network

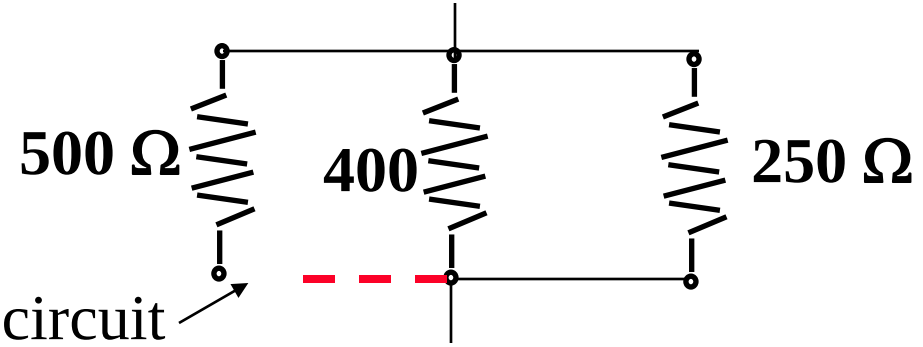


Layout

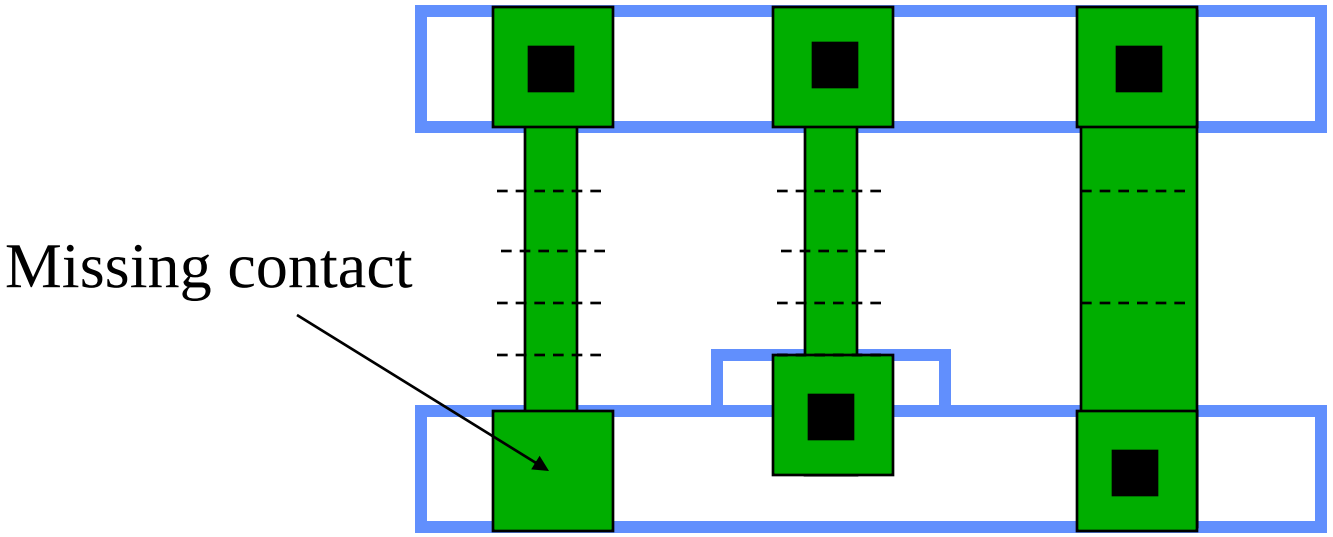


LVS RESULTS

Circuit Extracted from the Layout

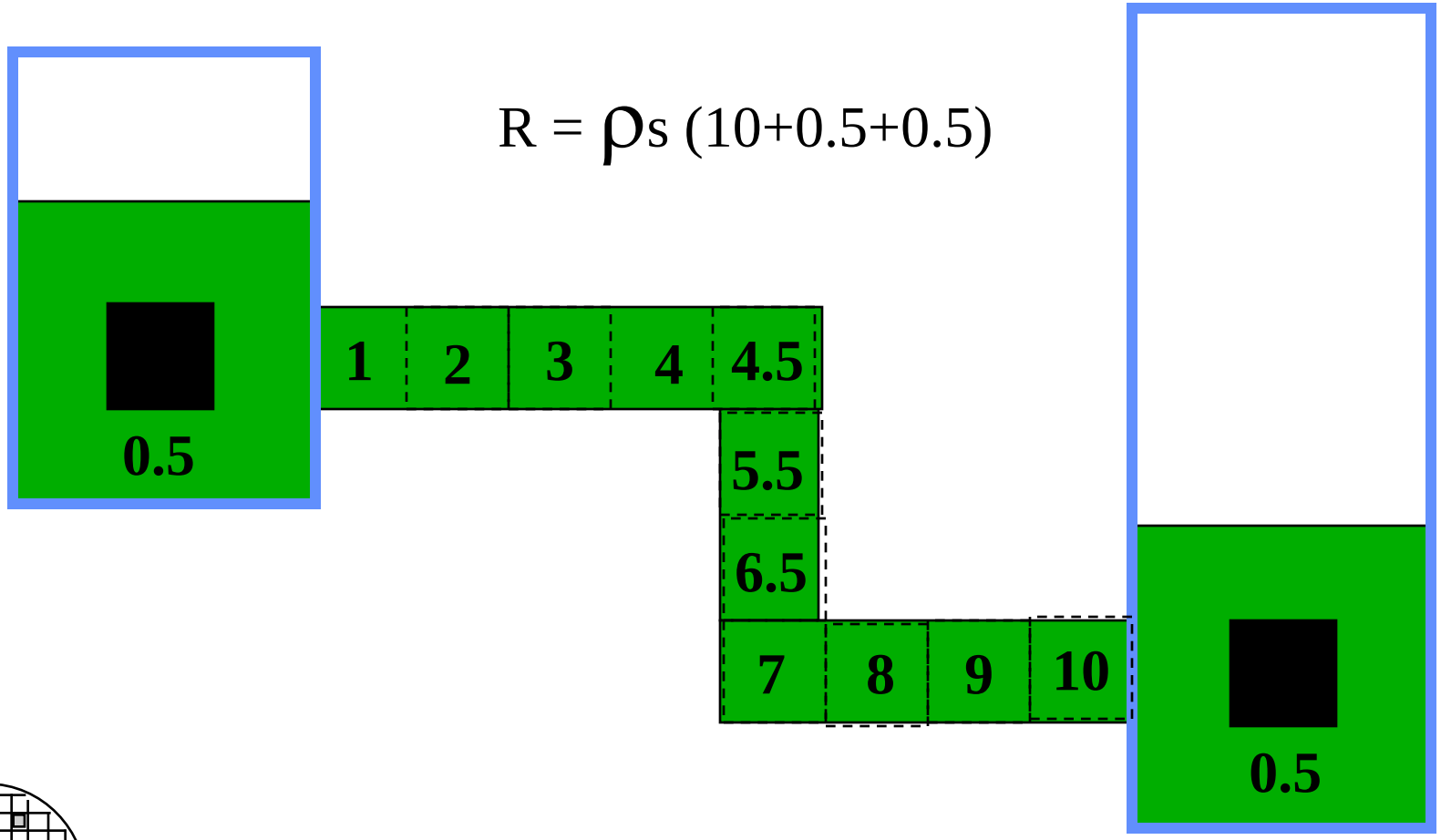


Layout



VARIATIONS ON THE BASIC RESISTOR LAYOUT

$$R = \rho s\ (10+0.5+0.5)$$

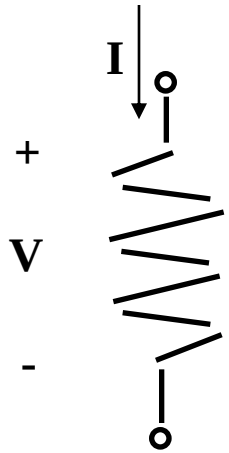


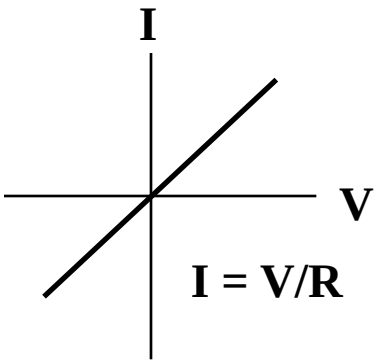
RESISTOR DESIGN DETAILS

Target Value
- Sheet resistance of layers used
  - variation
- L/W ratio
  - variation

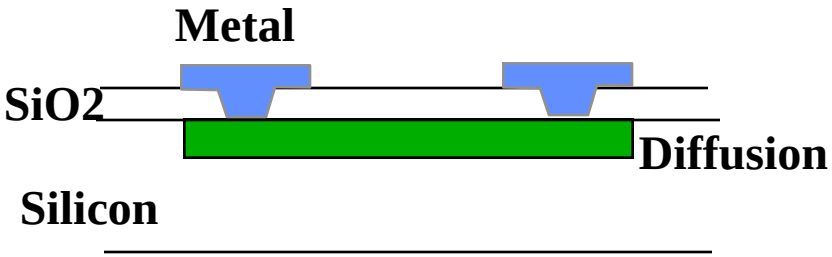
Power Dissipation
- designed L and W values

Other Physical Dimensions
- Terminal shape
- Bends

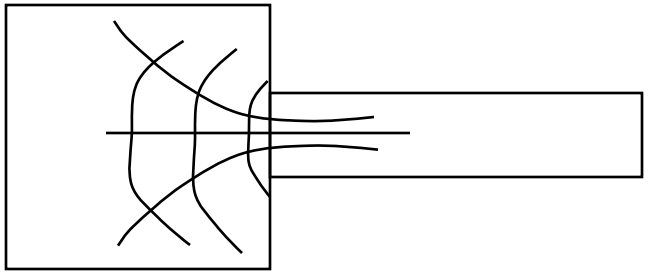




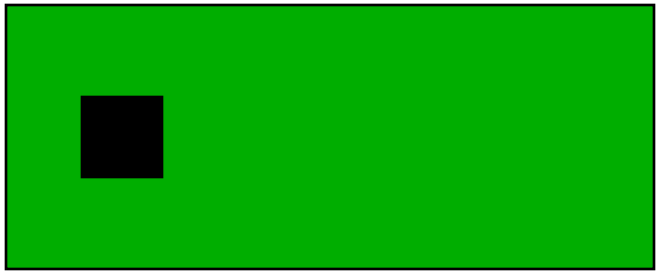
$R = \rho_s L/W$



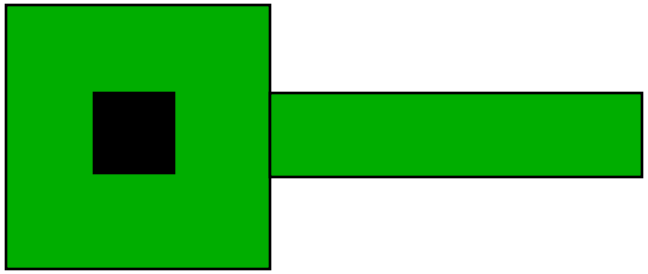
RESISTOR TERMINATION DETAILS



Field Mapping

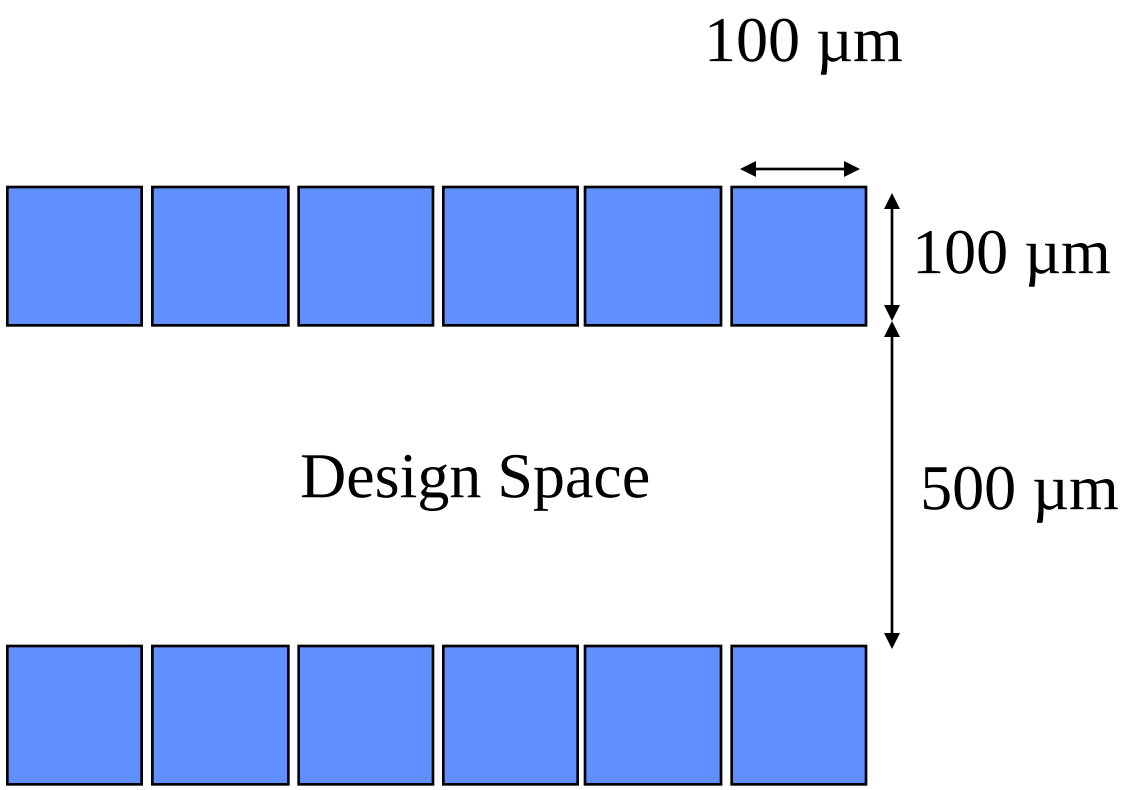


~ 0 squares



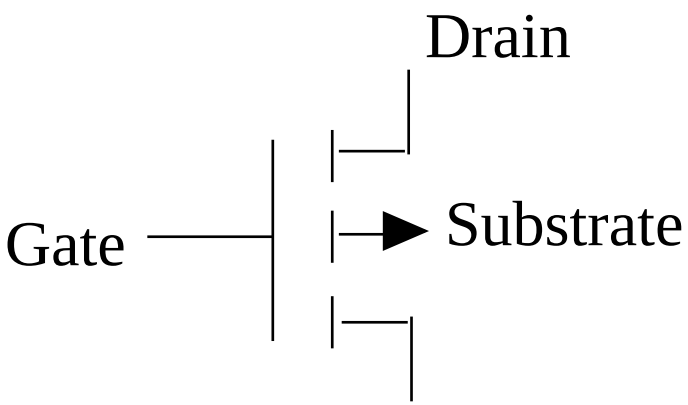
~ 0.5 squares

METAL PROBE PAD LOCATIONS



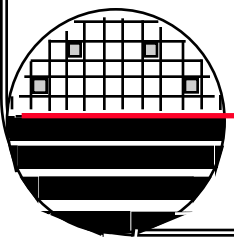
PMOS FIELD EFFECT TRANSISTORS

SYMBOL

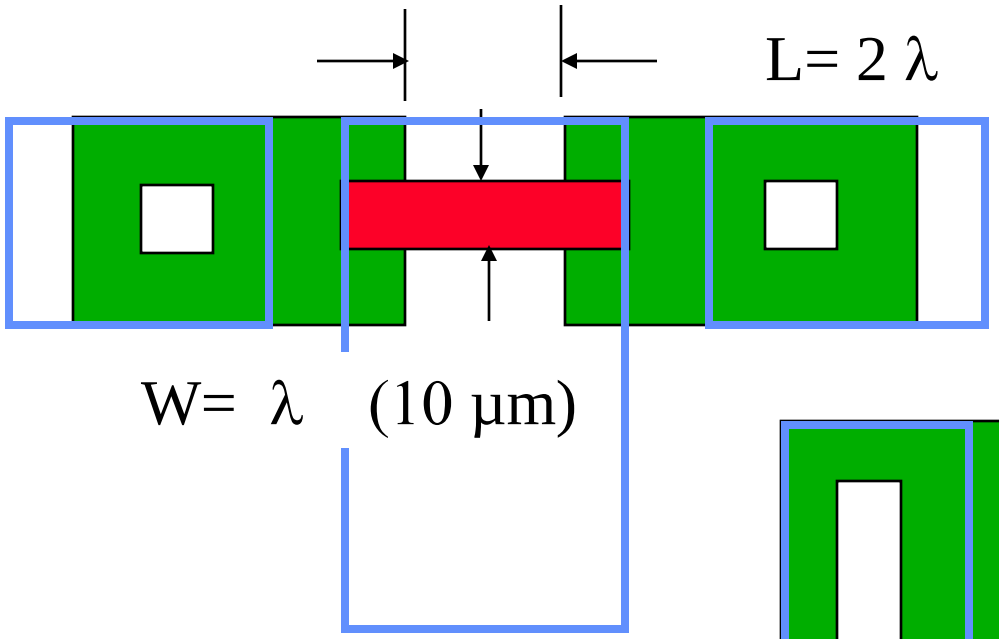


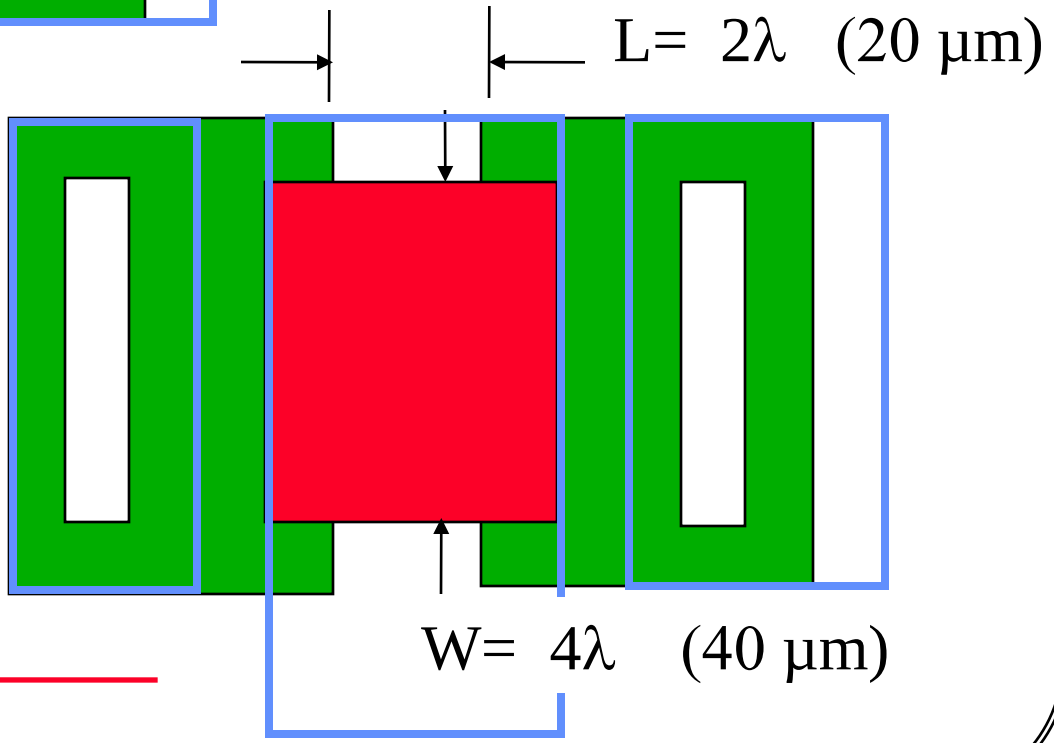
PMOS FET

The current the flows from the source to the drain is controlled by the gate voltage. Source and Drain are interchangeable. PMOS describes the structure as Metal Oxide Silicon with P-type drain and source. The width and length determine the gain of the transistor. Wider transistors give more gain (current flow). Longer transistors give more resistance (less current flow).



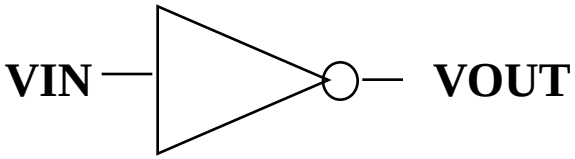
TRANSISTOR DESIGN





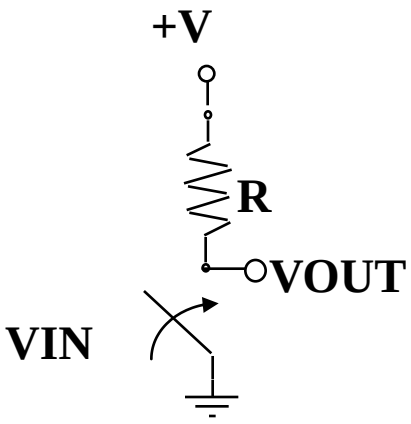
INVERTERS

SYMBOL

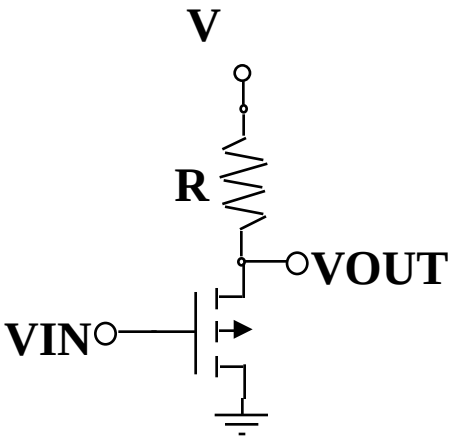


TRUTH TABLE

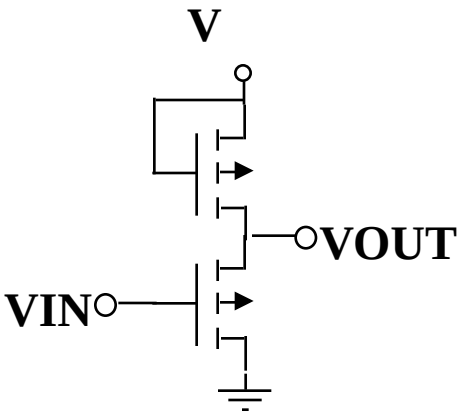
VIN	VOUT
0	1
1	0



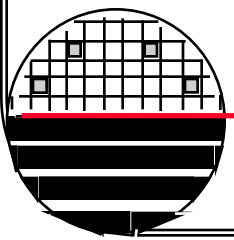
SWITCH



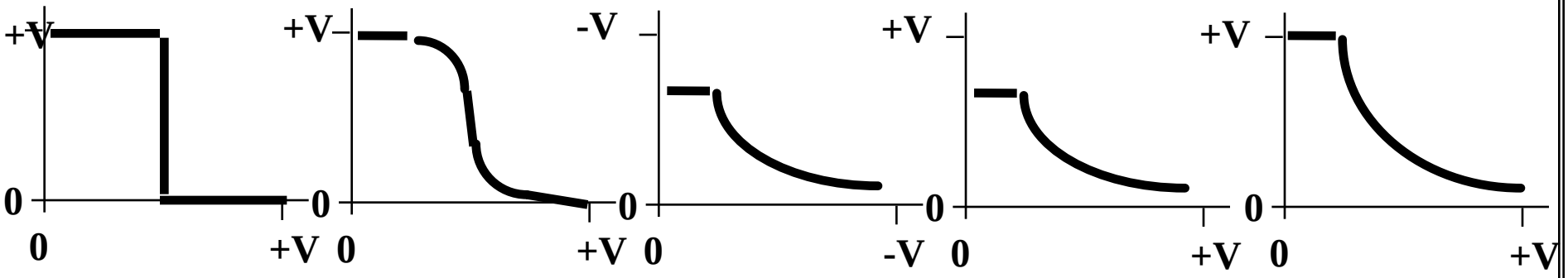
RESISTOR LOAD

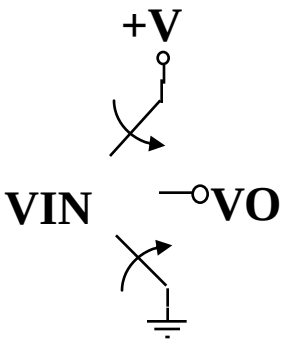


PMOSFET ENHANCEMENT LOAD

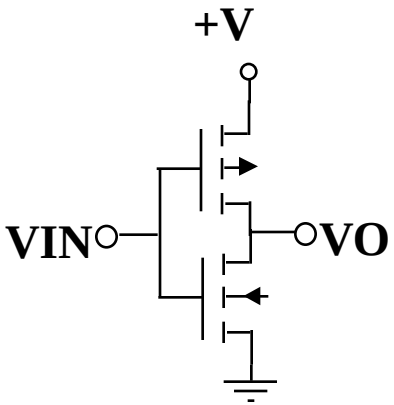


OTHER INVERTER TYPES - VOUT VS VIN

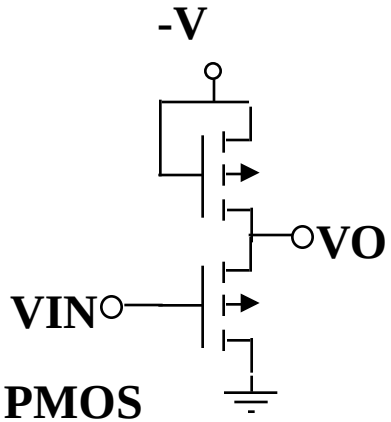




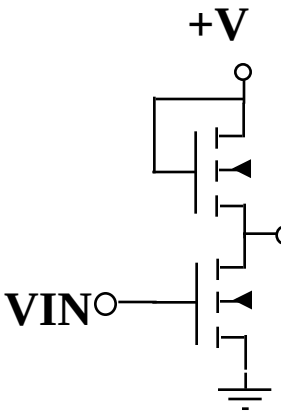
SWITCH



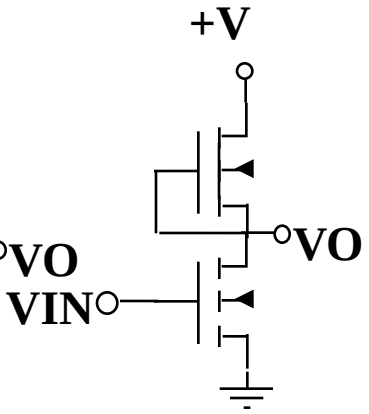
CMOS



PMOS ENHANCEMENT LOAD



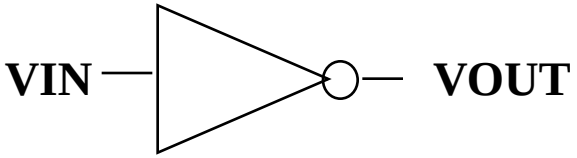
NMOS ENHANCEMENT LOAD



NMOS DEPLETION LOAD

PMOS ENHANCEMENT INVERTER GAIN

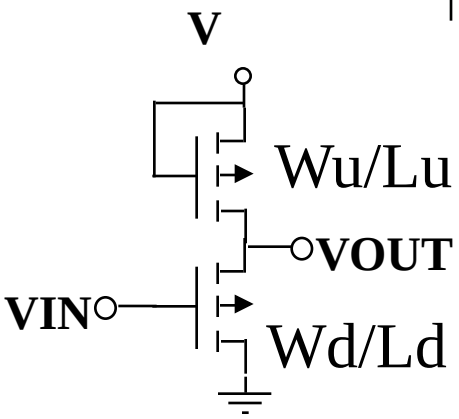
SYMBOL



TRUTH TABLE

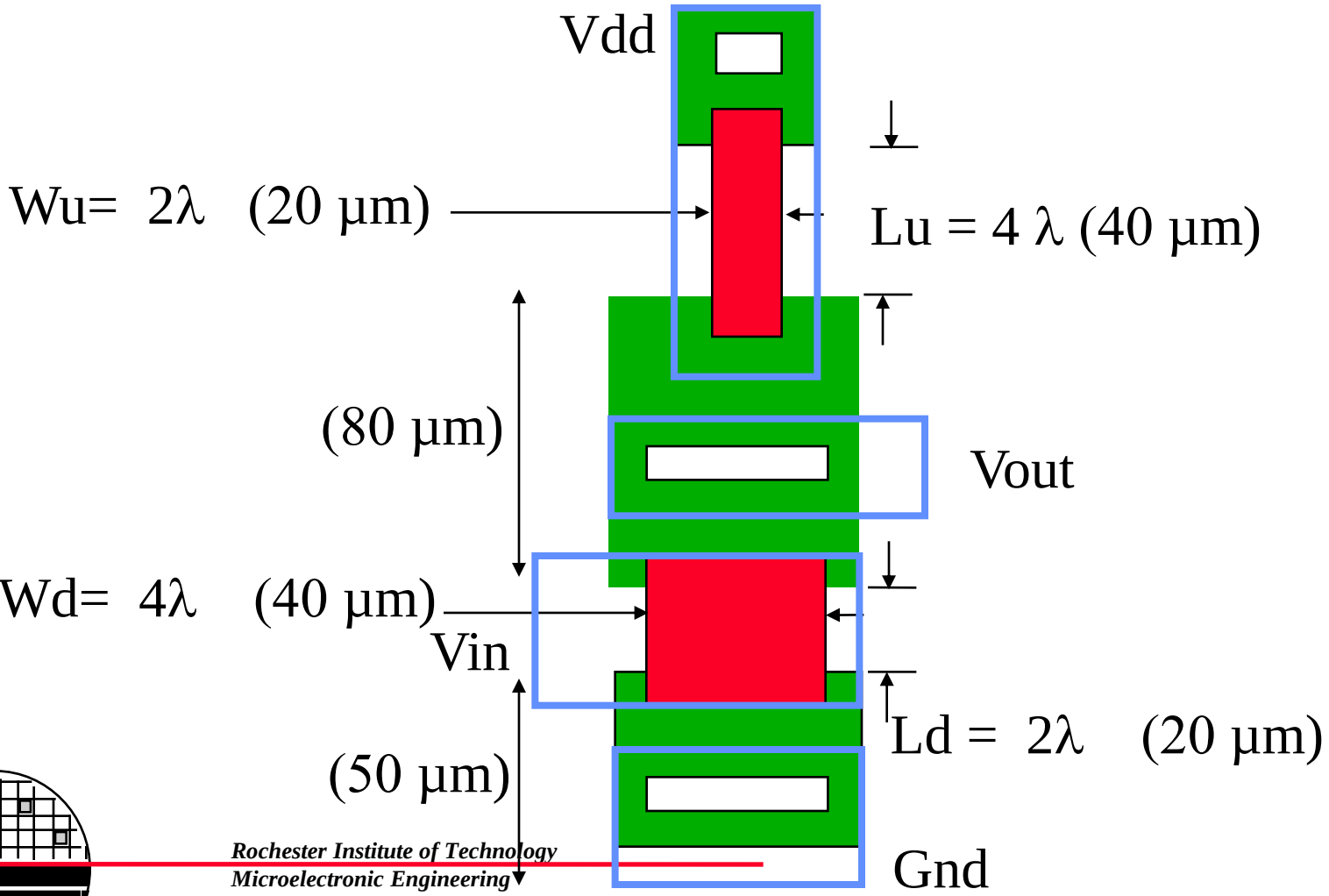
VIN	VOUT
0	1
1	0

$$\text{Inverter Gain} = \sqrt{\frac{Wd/Ld}{Wu/Lu}}$$



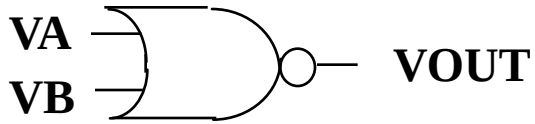
PMOSFET ENHANCEMENT LOAD

GAIN OF 2 INVERTER



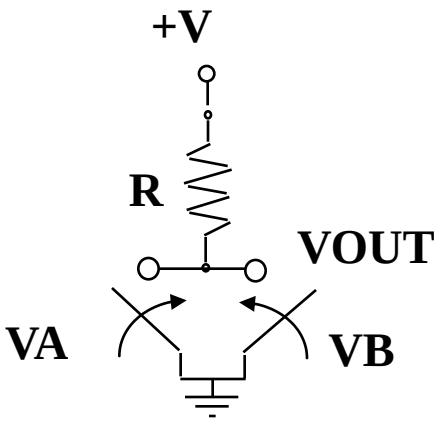
NOR GATES

SYMBOL

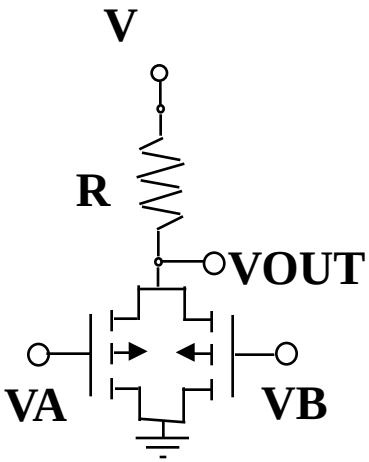


TRUTH TABLE

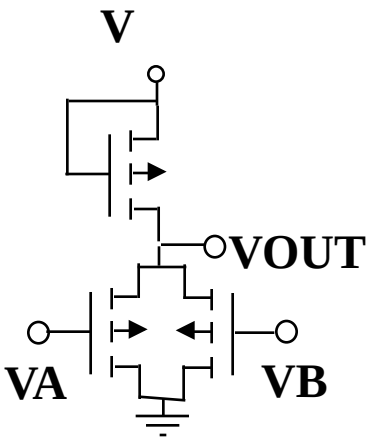
VA	VB	VOUT
0	0	1
0	1	0
1	0	0
1	1	0



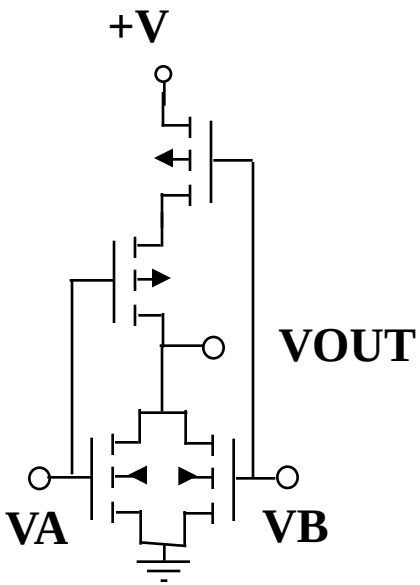
SWITCH



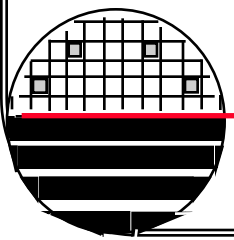
RESISTOR LOAD



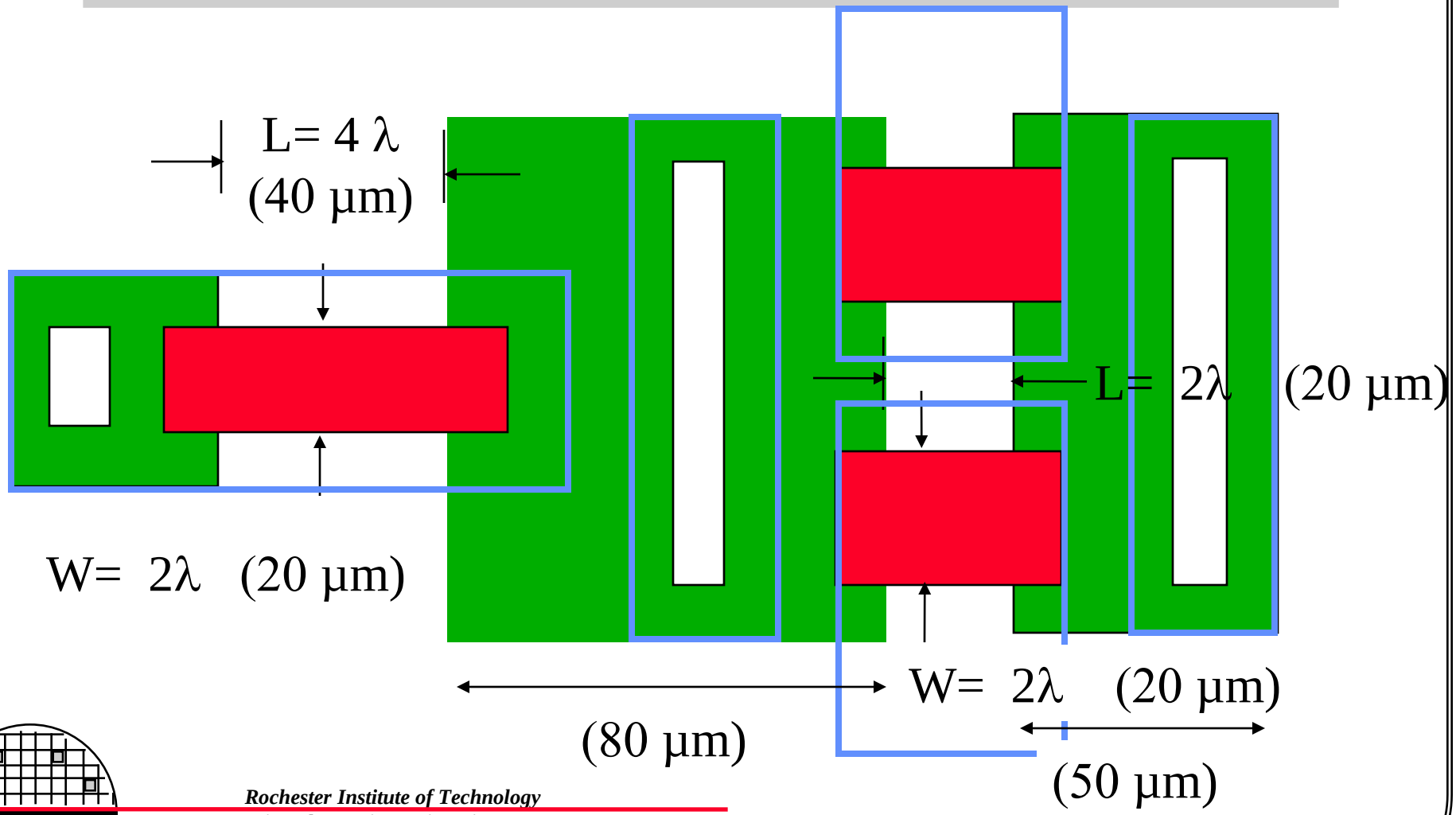
PMOS LOAD



CMOS

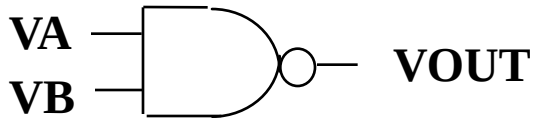


NOR GATE LAYOUT



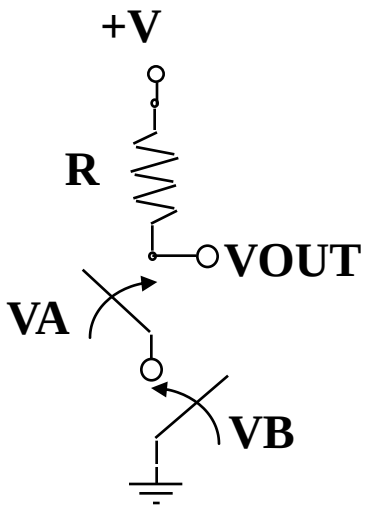
NAND GATES

SYMBOL

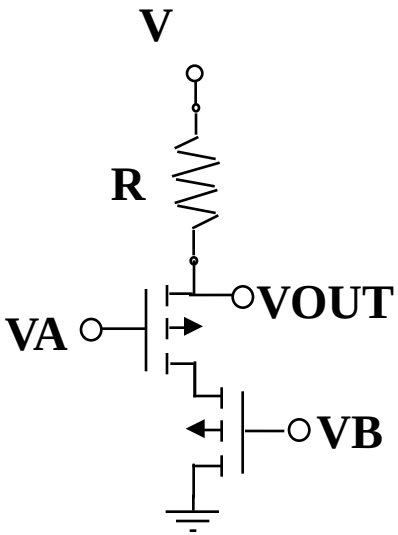


TRUTH TABLE

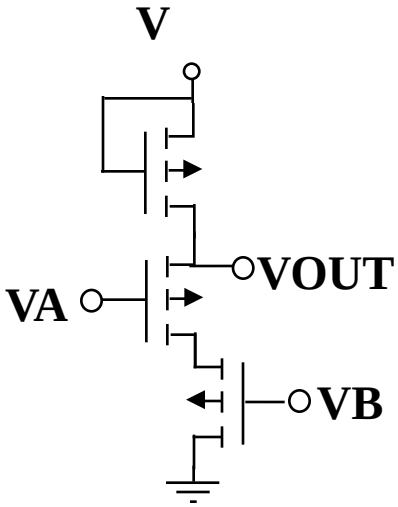
VA	VB	VOUT
0	0	1
0	1	1
1	0	1
1	1	0



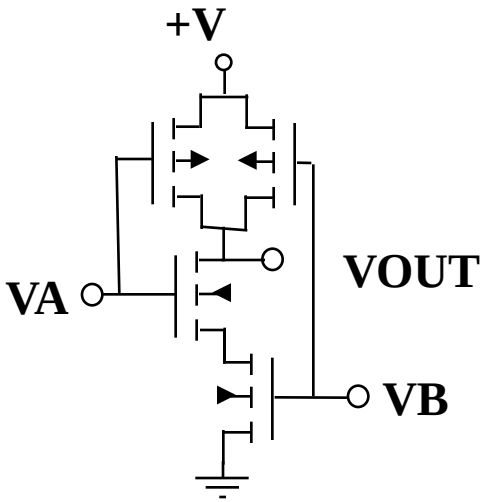
SWITCH



RESISTOR LOAD

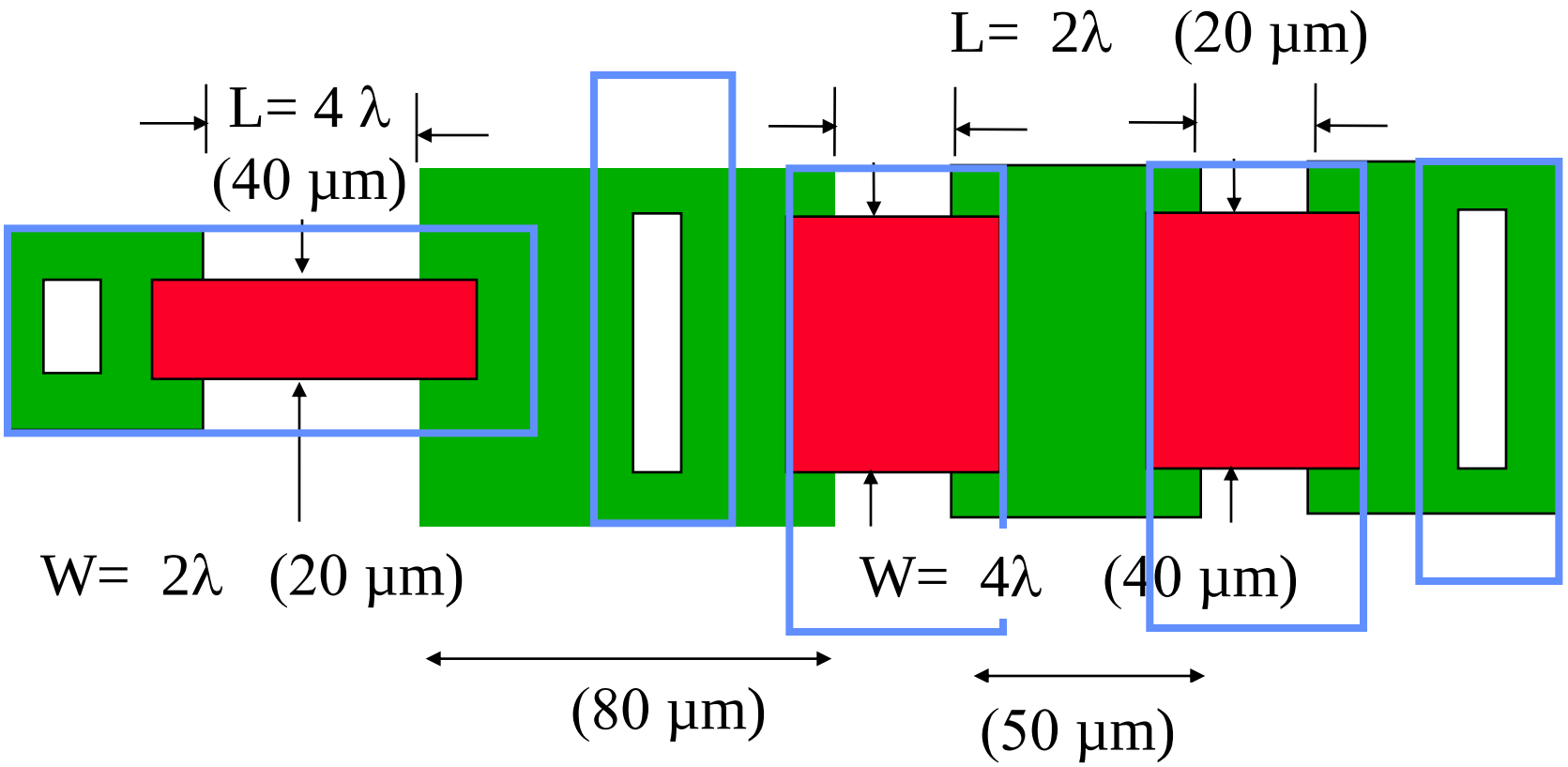


PMOS LOAD



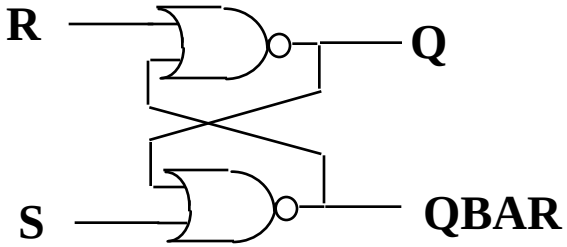
CMOS

NAND GATE LAYOUT



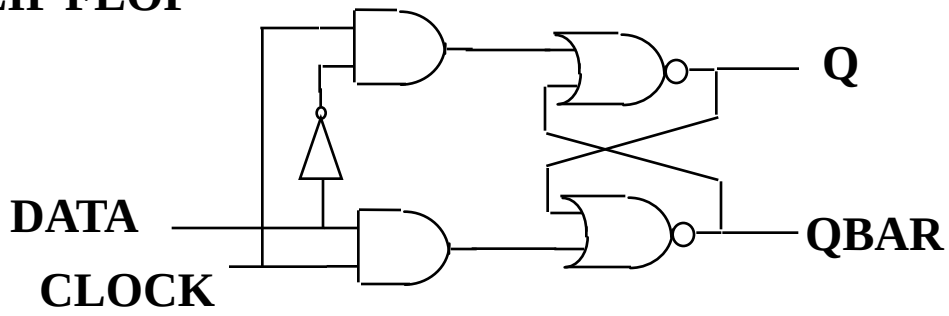
RS FLIP FLOP

RS FLIP FLOP



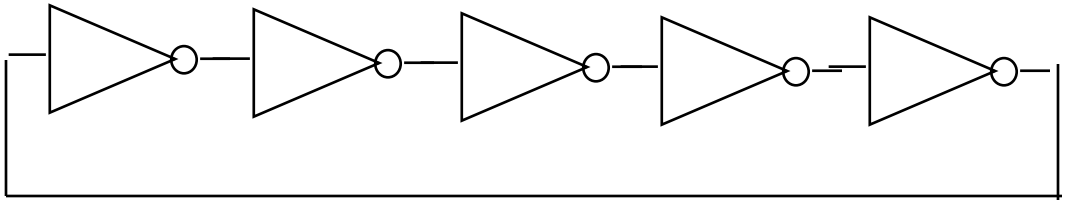
R	S	Q
0	0	Qn-1
0	1	1
1	0	0
1	1	INDETERMINATE

D FLIP FLOP



Q=DATA IF CLOCK IS HIGH
IF CLOCK IS LOW Q=PREVIOUS DATA VALUE

RING OSCILLATOR

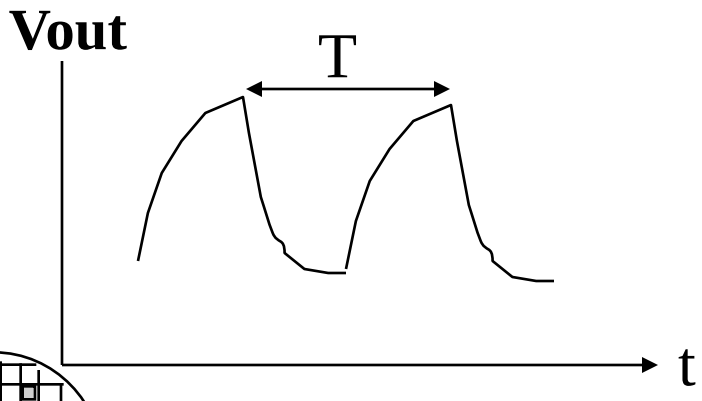


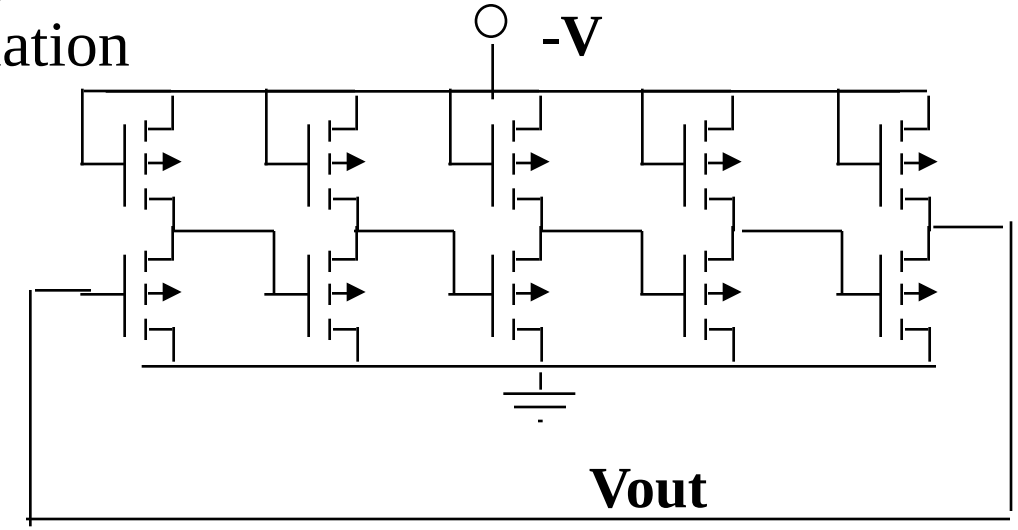
T = 2 td N

td is inverter gate delay

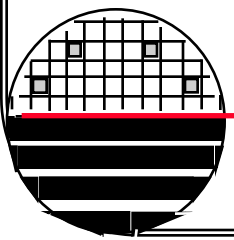
N is number of stages

T is period of oscillation





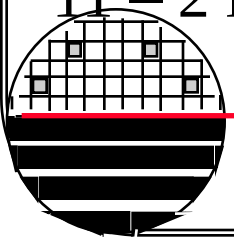
MEBES - Manufacturing Electron Beam Exposure System



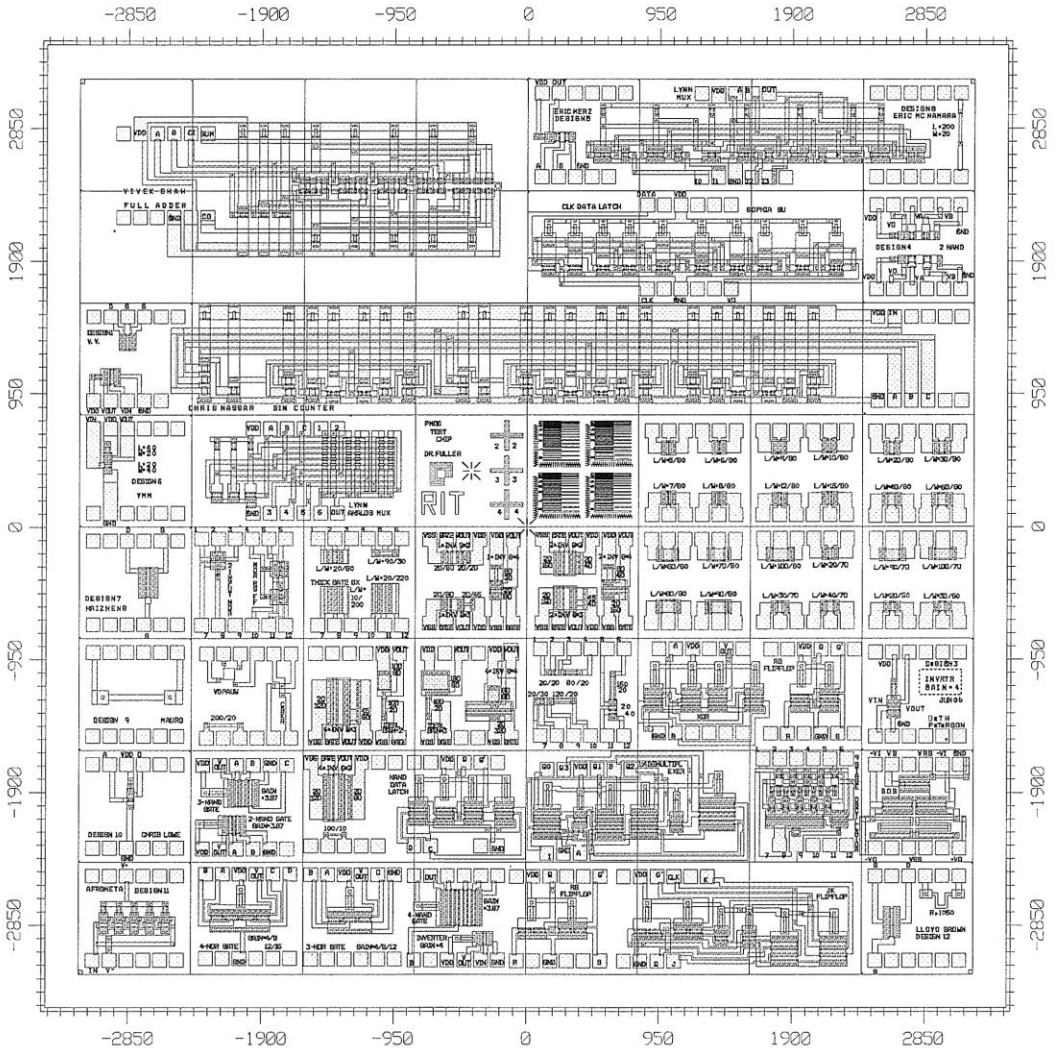
PHOTOMASK

LABORATORY DESIGN PROJECTS

1- Resistor, L=200 µm, W=20 µm
2- Resistor, L=400 µm, W=40 µm
3- PMOS Transistor L=20 µm, W=100 µm
4- PMOS Transistor L=20 µm, W=200 µm
5- Inverter Gain of 2
6- Inverter Gain of 3
7- Inverter Gain of 4
8- Nine stage ring oscillator
(using gain of 3 inverters)
9- RS Flip flop
10 – 2 input NAND
11 – 2 input NOR



EXAMPLE FROM PREVIOUS SHORTCOURSE



Roch
Micr

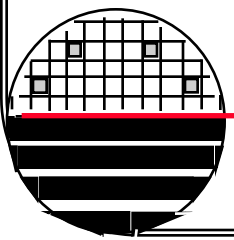
GETTING STARTED WITH LAYOUT EDITOR IC

Usually the workstation screen will be blank, move the mouse to view a login window.

Login: **guest-name**
Password: ********

The screen background will change and your desktop will appear. On the top of the screen click on **Applications** then **System Tools** then **Terminal**. A window will appear that has a Unix prompt inside. Type the command **ls** at the prompt to see a list of directories and files, the account should be empty.

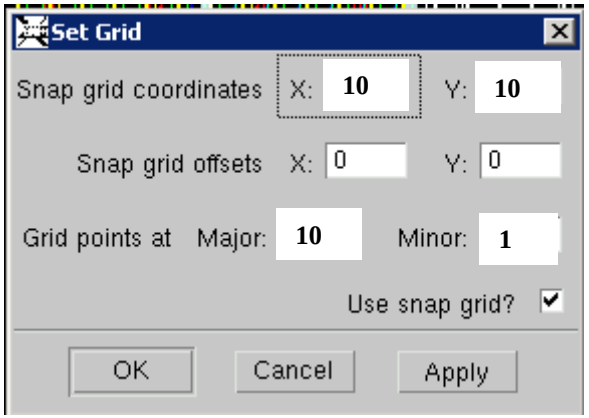
Type **ic <ENTER>,** it will take a few seconds, then maximize the IC Station window by clicking the left mouse button on the large square in the upper right corner of the IC Station window.



STARTING A CELL DESIGN

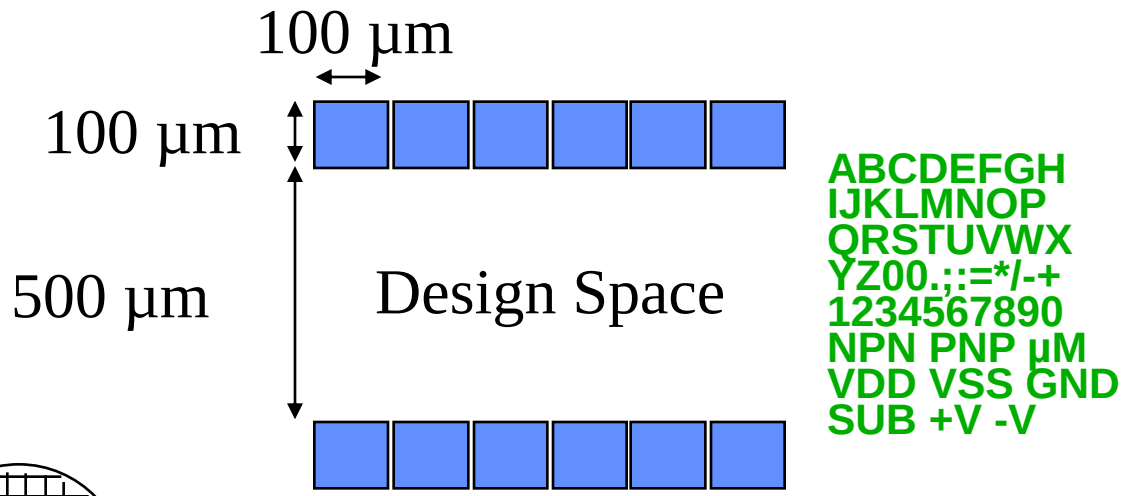
On the right hand panel of the IC Station window **Layout** then click on **New** to open the create Cell window. Fill in a **cell name that was assigned** to you. (so I can identify your cells from other students cells). For process browse to or type **/tools/ritpub/process/ritpmos** . This will select the correct level names, level numbers and colors for the PMOS process. The workspace should change to a black screen with dots. If you move the cursor around you can find different xy cursor locations as displayed at the top-center.

On top banner select **Setup>Preferences>Display>Rulers/Grid** Set the grid as shown…



ADDING PAD CELL AND LETTERS

From the banner at the top of the page choose **Add>Instance**. A tan pop-up window will appear at the bottom of the page. Type in the following cell name, all lower case, **/tools/ritpub/padframes/ritpmos/ritpmos_12_pads** and click the left mouse button on the location button. Then position the cursor at the origin 0,0 and click the left mouse button. Click the left mouse button on the cancel button on the tan pop-up box. Press SHIFT and F8 to View All. You should see a white box with ritpmos_12_pads written inside it. Hit space bar and type flatten and select, OK. Press F2 to unselect all.



DRAWING BOXES, CIRCLES AND OBJECTS

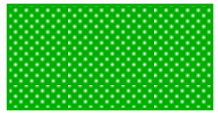
Select easy edit, right click and select Scroll Bars, see the edit commands.

DRAW BOXES by click and drag of mouse. Unselect by pressing F2 function key. The Notch command is useful to change the size of a selected box or merge rectangular shapes into more complex objects. The following command will draw a 3000 µm by 3000 µm box with layer 4 color/shading. **$add_shape([[0,0],[3000,3000]],4)**

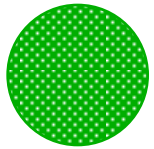
Location of lower left corner

Location of upper right corner

Box Color



DRAW CIRCLES by typing **$set_location_mode(@arc)** return. The following command will draw a 100µm radius circle centered at (0,0) using 300 straight line segments.
$add_shape($get_circle([0,0],[100,0],300),3)
To reset to rectangles type $set_location_mode(@line) return.



SELECT OBJECTS by clicking or by click and drag. Selected objects will appear to have a bright outline. Selected objects can be moved (**Move**), copied (**Copy**), deleted (**Del**) or notched (**Notc**). To **Unselect** objects press F2.

ADJUSTING VIEW

ZOOM IN OUT: pressing the + or - sign on right key pad will zoom in or out. Also pressing shift + F8 will zoom so that all objects are in the view area. Select view then area and click and drag a rectangle will zoom so that the objects in the rectangle are in the view area.

MOVING VIEW CENTER: pressing the middle mouse button will center the view around the pointer.

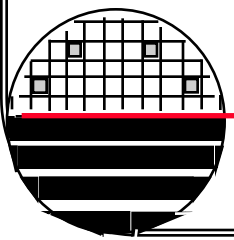
LASER PRINT OUTPUT: Select File and Print, OK. This gives a laser printer output of entire cell. Select printer **prec10**, clear width, len, pages, scale by using backspace so nothing is in those boxes. Say OK.

PRINT PART OF LAYOUT: first create a panel. Under objects, select add a panel, name it and click on rectangle symbol. Then use the left mouse button to drag a rectangle around the objects you want in the panel to be printed. Then select File and Print and enter panel name, click on print set up, printer is **prec10**, clear width, len, pages, scale by using backspace so nothing is in those boxes. Say OK.

OTHER – ADDING TEXT

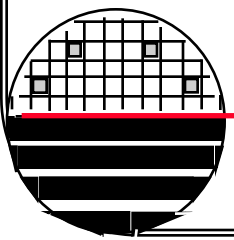
ADDING TEXT: Add > Polygon Text click on layout where you want it located. Select the text box and Edit > Change > Attributes, change pgtext, change scale to 3.0

ADDING TEXT: From the banner at the top of the page choose **Objects>add>cell**. A tan pop-up window will appear at the bottom of the page. Type in the following cell name, all lower case, **/tools/ritpub/padframes/ritpmos/ritpmos_12_pads** and click the left mouse button on the location button. Then position the cursor to the side of your layout and click the left mouse button. Click the left mouse button on the cancel button on the tan pop-up box. Press SHIFT and F8 to View All. You should see a white box with ritpmos_12_pads written inside it. Type flatten and select, OK. Press F2 to unselect all. Use select and copy to place letters you want. To change letters to a different layer use objects and **set layers**. Don't forget to delete the extra letters and numbers you don't want.



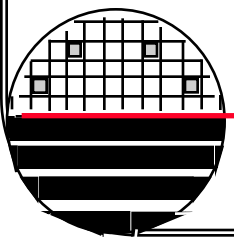
REFERENCES

1. Principles of CMOS VLSI Design, 2nd Ed., Neil H.E.Weste, Kmran Eshraghian, Addison Wesley, 1993.
2. Physical Design Automation of VLSI Systems, Bryan Preas, Michael Lorenzeti, Benjamin/Cummings, 1988.
3. VLSI Engineering, Thomas Dillinger, Prentice Hall, 1988.



HOMEWORK QUESTIONS: CAD

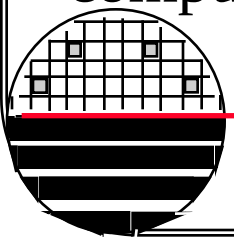
1. Why does the metal have to surround the contact opening by a certain distance?
2. What happens to the value of a resistor as its length is decreased relative to its width?
3. Give three reasons why resistors with the same value might have different layout geometry.
4. How do design rules reflect the process by which the devices are made?



VLSI DESIGN CENTER AT RIT

The VLSI Design Center (room 17-2500) consists of AMD Athlon 64 FX-51 Gentoo LINUX workstations, file servers and printers. The workstations are primarily PC's running LINIX operating system. The PC's are fast, have lots of RAM and disk space. There are two file servers for user accounts and application software. The two main print devices are a HP laser printer and a HP 36 inch color plotter. There devices are connected through an Ethernet based network. The primary application software, on this network, is the very sophisticated and tightly integrated Mentor Graphics suite of EDA (Electronic Design Automation) tools.

Accounts on the computers and access to the room are controlled by the computer engineering department. Currently Charles Gruener for computer accounts and Rick Tolleson for card swipe room access.

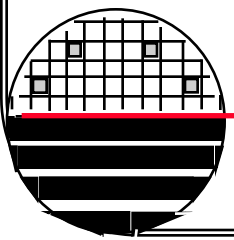


BASICS - DESKTOP

A graphical interface that provides workspaces, windows, menus, controls, and a front panel to help you organize and manage your software applications.

The **Front Panel** has a tool bar (usually at the bottom of the screen). The tool bar has a K-Gear icon which allows access to editors, graphics programs and the open office software package. The open office package has calculators, drawing programs, equation editor and word processing. You can change the settings for the look and feel of the desktop and the windows that are running. I suggest that you do not go too wild changing things , instead stick to getting the job done.

There are four “desk tops” available to run programs on. The toolbar tells you which desktop you are looking at and what is running in each window on the desktop.

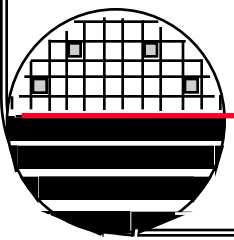


BASICS CONTINUED

The Mouse: is a three button mouse. The left mouse button is used to select or "click" on something. The right mouse button is used for popup menus. The middle mouse button is typically defined for each application and does not have a common function. For example in the layout software "IC" the middle mouse button shifts the layout so that the clicked location is centered in the workspace.

Log Out: click on K Gear icon, select Log Out…, Select End Current Session

Restore Session: If there is no activity for several minutes the screen will be locked and require the user to type his password to restore the session.



BASIC COMMANDS

Command	Description
ls	list the files and directories in the current directory
cd	change directory
cd ..	go up one directory
mv	move a file (rename a file)
rm	remove a file (delete a file)
pwd	display path of current directory
mkdir	create a new directory
rmdir	remove a directory
yppasswd	change your password

It is important to remember that since this is a UNIX operating system, the commands are case sensitive.