Development of a Deep-Submicron CMOS Process for Fabrication of High Performance 0.25 μm Transistors

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M.S. Thesis Defense

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May 19, 2006

Motivation

- Enable the Microelectronic Engineering department to continue the semiconductor industry trend of fabricating high performance transistors that have faster switching speeds and increased density and functionality
- Push the limits of the SMFL in all areas from design to fabrication to test
- Create a baseline process that can be used to integrate strained silicon, metal gates, high-*k* gate dielectrics, and replacement gate technologies at RIT

Outline

- RIT/Industry Scaling Trends
- Gate Control Fundamentals
- Short Channel Effects
- Deep-Submicron Scaling
- Test Chip Layout
- Unit Process Development & Integration
- Electrical Results
- Summary
- Questions

RIT/Industry Scaling Trends

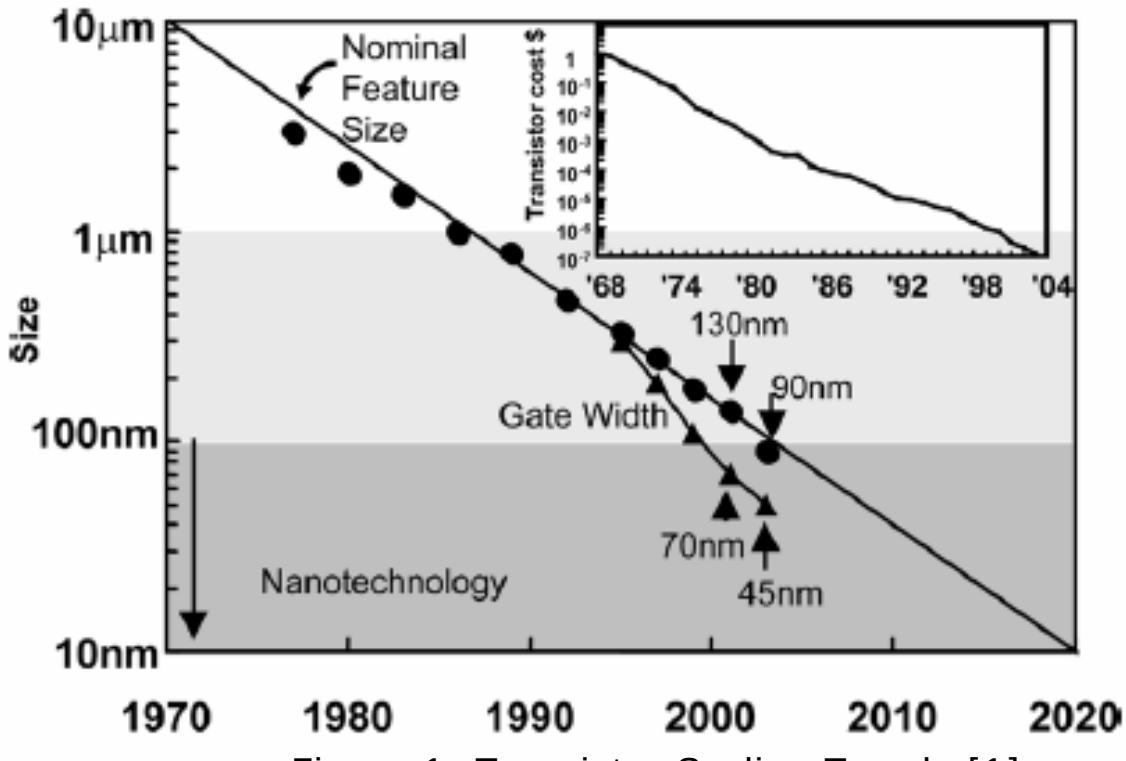


Figure 1: Transistor Scaling Trends [1]

- 0.25 µm CMOS technology was used in high volume manufacturing of the Intel Pentium III up to 600 MHz through 1999

- The gap between industry and RIT is rapidly shrinking

Gate Control Fundamentals

- NMOS Transistor
- 4 Terminal Device
  - Gate
  - Source
  - Drain
  - Body

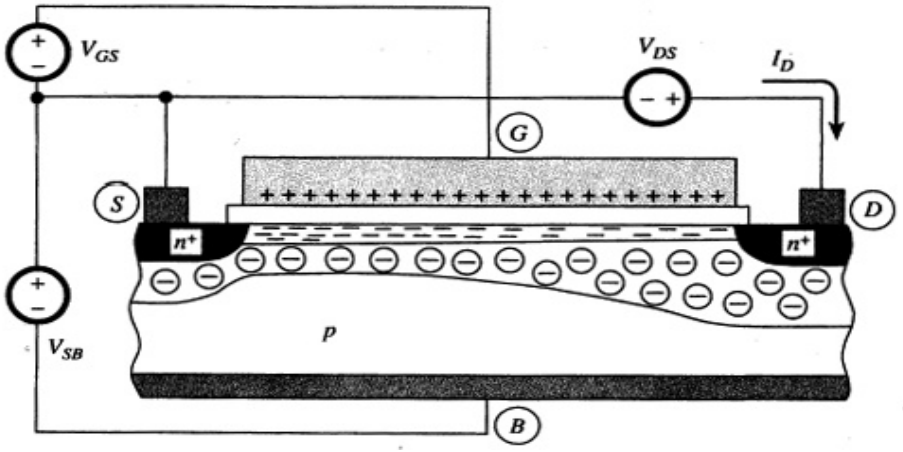


Figure 2: Schematic of NMOS Transistor [2]

To turn transistor on:

- Apply positive charge to Gate, Q_G
- A depletion region in the p-type body is created as positively charged holes are repelled by gate, exposing negatively charged acceptor ions, Q_B
- As the gate charge is further increased, electrons from the source diffuse into the channel and become inversion charge, Q_I
- $Q_G = Q_B + Q_I$

Gate Control Fundamentals

- The source and body terminals are grounded
- A positive voltage is applied to the drain, V_{DS}
- Inversion charge moves from source to drain and is the current in the device

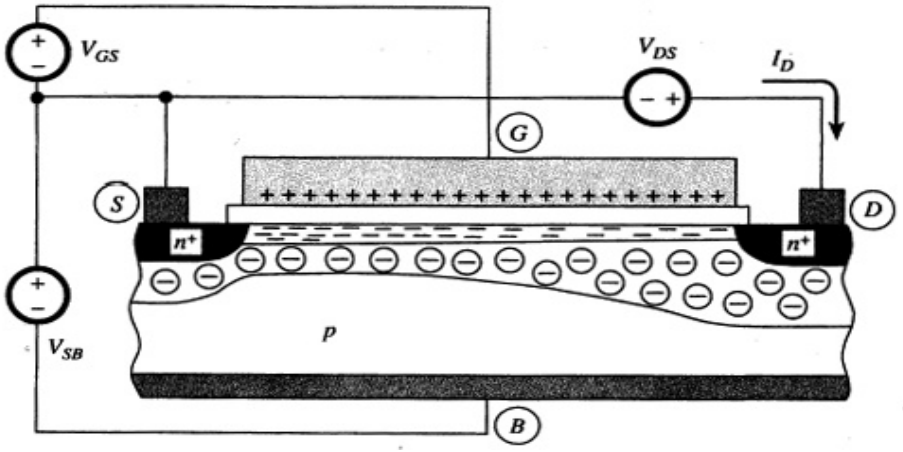


Figure 2: Schematic of NMOS Transistor [2]

- Equation 1 shows the classical derivation for drain current in a transistor by integrating the inversion charge along the channel

$$I_D = \frac{W}{L}\int_{VS}^{VD} m_n Q_n(V)\,dV \qquad \text{(Eq. 1)}$$

Gate Control Fundamentals

- A depletion region from the drain is created by the reverse biased drain - body N^+-P diode
- The positively charged donor ions in drain support some of the negative inversion charge

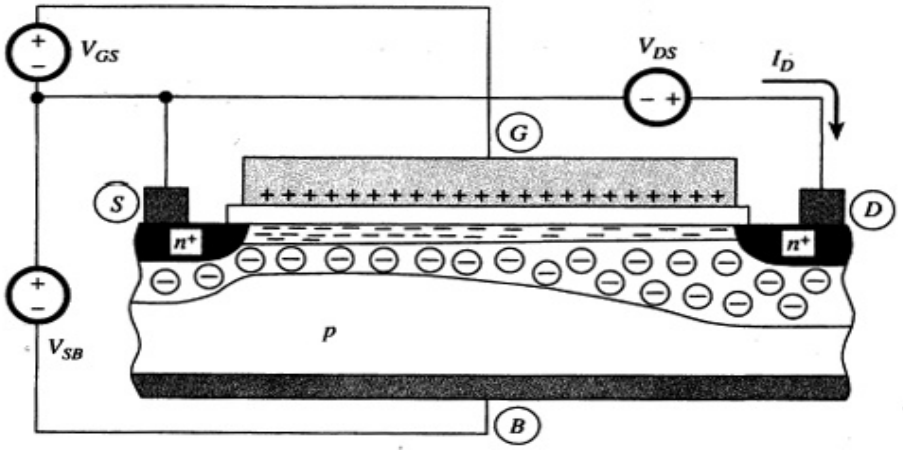


Figure 2: Schematic of NMOS Transistor [2]

- This is known as “Charge Sharing” as the gate does not have full control over the inversion channel
- For large gate lengths, the contribution of the drain in controlling the inversion layer is small compared to the gate contribution
- As transistors are scaled smaller in gate length, the drain has a larger percentage contribution in supporting inversion charge in the channel

Drain Induced Barrier Lowering

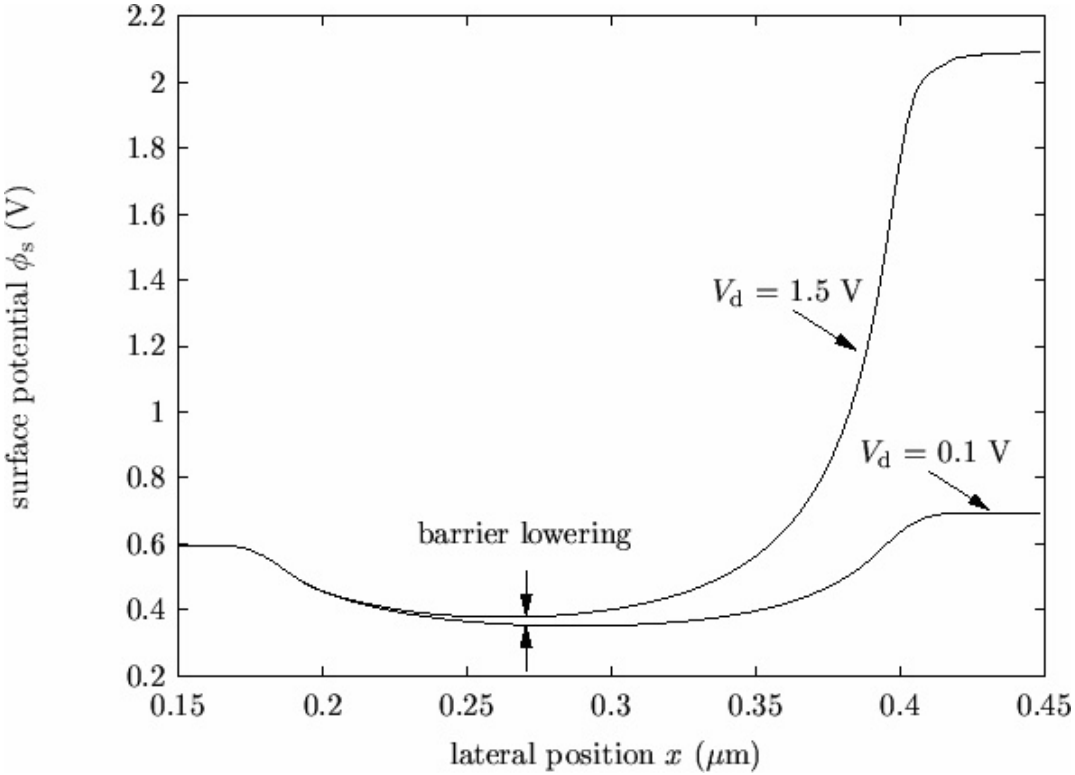


Figure 3: Surface Potential vs. Lateral Position in the Channel [3]

- As the drain bias is increased the energy barrier in the channel is lowered
- This is known as Drain Induced Barrier Lowering and is the cause of short channel effects

Short Channel Effects

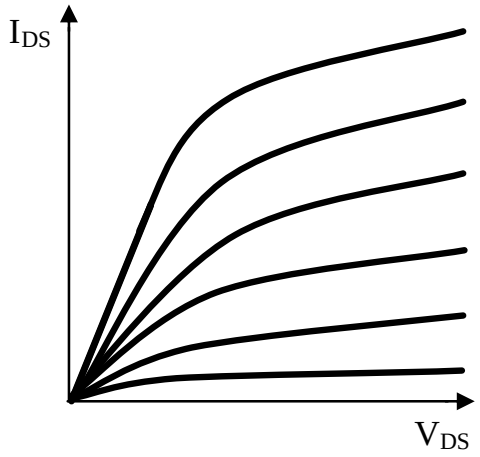
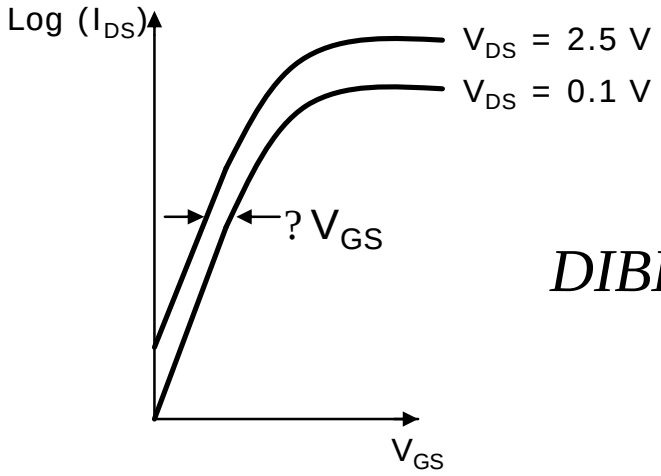


Figure 4: Channel Length Modulation



$$DIBL = \frac{\Delta V_{GS}}{\Delta V_{DS}}$$

Figure 5: Increased Sub-threshold Current

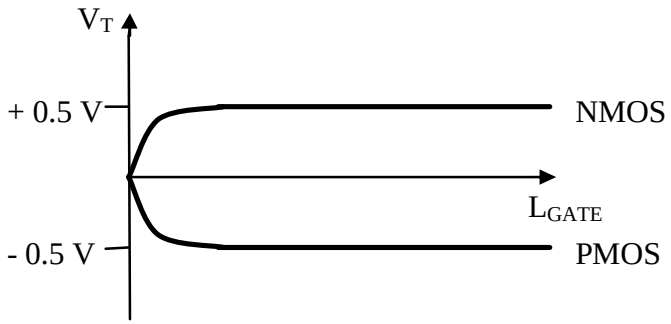


Figure 6: V_T Roll-Off

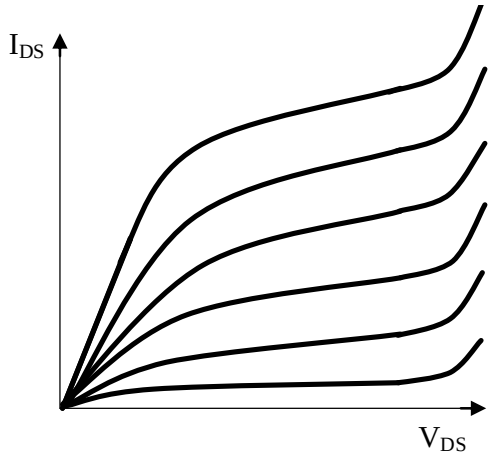


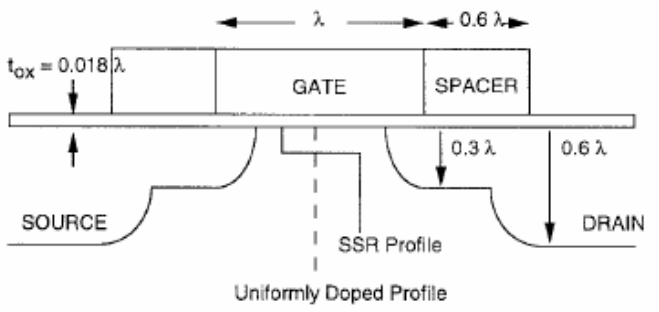
Figure 7: Source/Drain Punch through

Deep-Submicron Scaling

- The goal in deep-submicron scaling is to maximize the gate control for switching the device on and off by scaling physical and electrical parameters, therefore reducing short channel effects

Table 2: 0.25 µm Scaling Parameters from NTRS Roadmap [4]

I_{ON}	600 µA/µm	T_{ox}	40 - 50 Å
I_{OFF}	1 nA/µm	X_J (shallow LDD)	50 – 100 nm
$Log(I_{ON} / I_{OFF})$	5.75 decades	N_D (LDD)	2 - 5 x10^{18} cm^{-3}
SS	85 mV/decade	R_S (LDD)	400 – 850 Ω/sq
DIBL	< 100 mV/V	X_J (contact)	135 – 265 nm
V_{DD}	1.8 – 2.5 V	N_D (contact)	1x10^{20} cm^{-3}
$\lvert V_T \rvert$	0.5 V	X_J (SSRW channel)	50 – 100 nm



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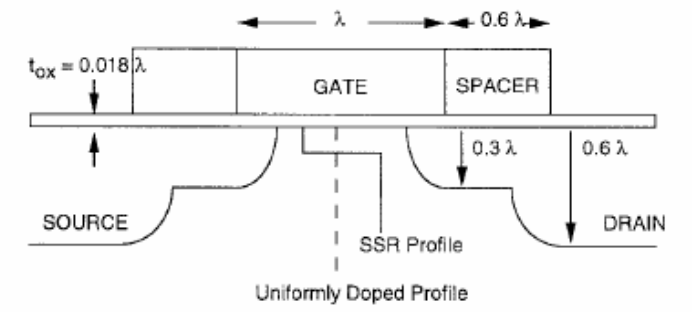
- Decrease gate oxide thickness
- Gate is closer to the channel
- More control in switching device off
- $C_{ox} \uparrow$ since $C_{ox} = \varepsilon A/t_{ox}$ or $C_{ox} = \Delta Q/\Delta V$
- I_D and $g_m \uparrow$ since $\propto C_{ox}$



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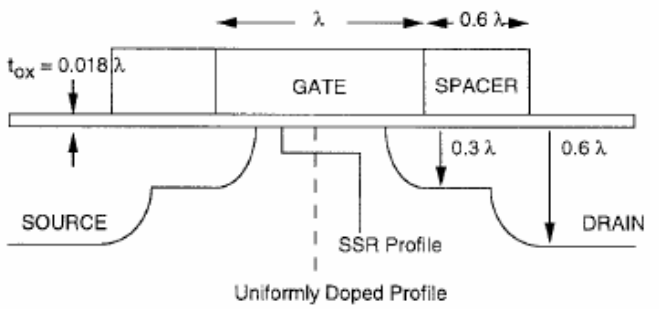
- Decrease junction depth of source/drain
- Depletion region from gate dominates depletion region from the drain
- Trade-off is sheet resistance ↑ and I_D ↓
- N_D must ↑ which will cause R_S ↓



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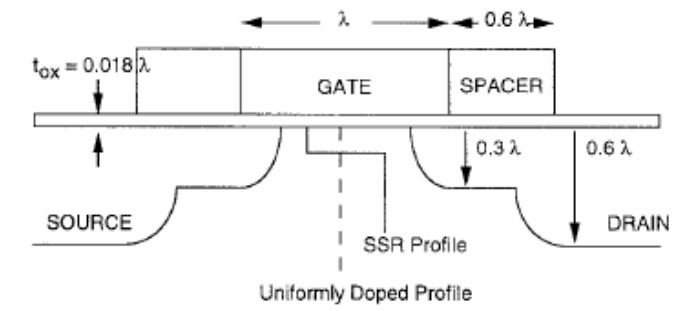
- Use sidewall spacer to create deeper source/drain junction called the contact
- Typically ~2x as deep as shallow LDD
- Doped heavily to reduce R_S



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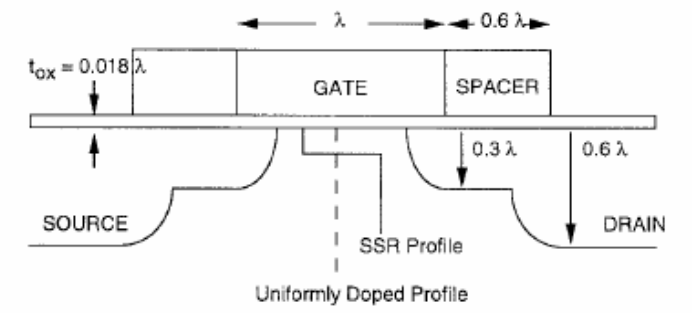
- Decrease V_{DD} to reduce depletion region from the drain and prevent lateral and vertical punch-through
- Increase doping of channel to decrease the depletion region from the source/drain
- Use a retrograde profile where doping is low at the surface and higher sub-surface
- Mobility of carriers ↑
- I_D and g_m ↑ since both are ∝ mobility



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- As T_{OX} ↓, gate leakage current ↑ as $V_{GS\text{-}MAX} = V_{DD}$
- V_{GS} must ↓ to reduce this leakage
- V_T must ↓ so (V_{GS}-V_T) ↑, this is "Gate Overdrive" and is ∝ I_D
- Want I_{ON} ↑ since gate delay ∝ I_{ON}^{-1}

$$t = \frac{CV}{I_{ON}} \quad \text{(Eq. 2)}$$

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- Want I_{OFF} to be low to reduce standby power
- The industry standard metric is 1 nA/µm of off-current
- This results in 5.75 decades between I_{ON} and I_{OFF}
- There is 500 mV swing between 0 V and V_T
- SS of 85 mV/decade is needed to turn the device off

$$SS = \frac{KT}{q} \times \ln(10) \times \left[1 + \frac{C_D}{C_{OX}}\right] \quad \text{(Eq. 3)}$$

Theoretical limit ~ 60 mV/decade @ 300K

Layout of Test Chip

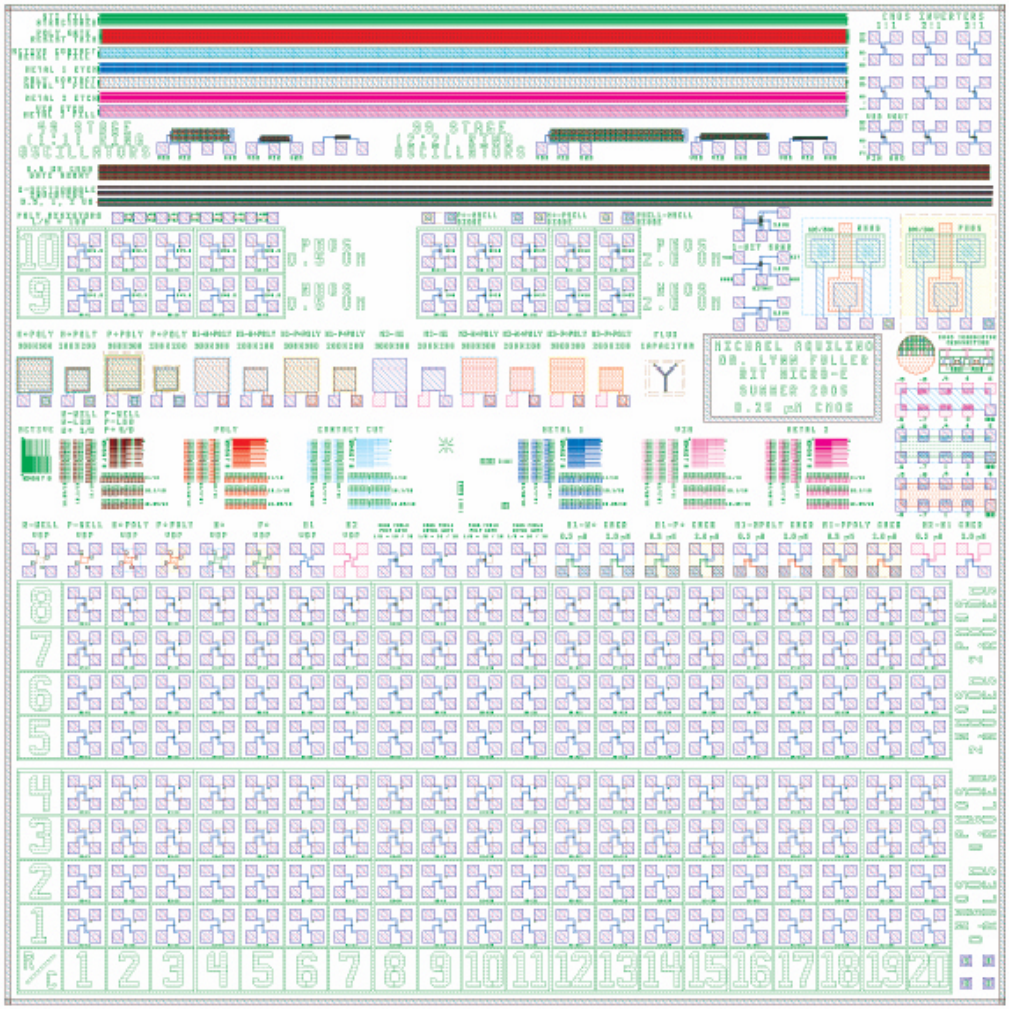
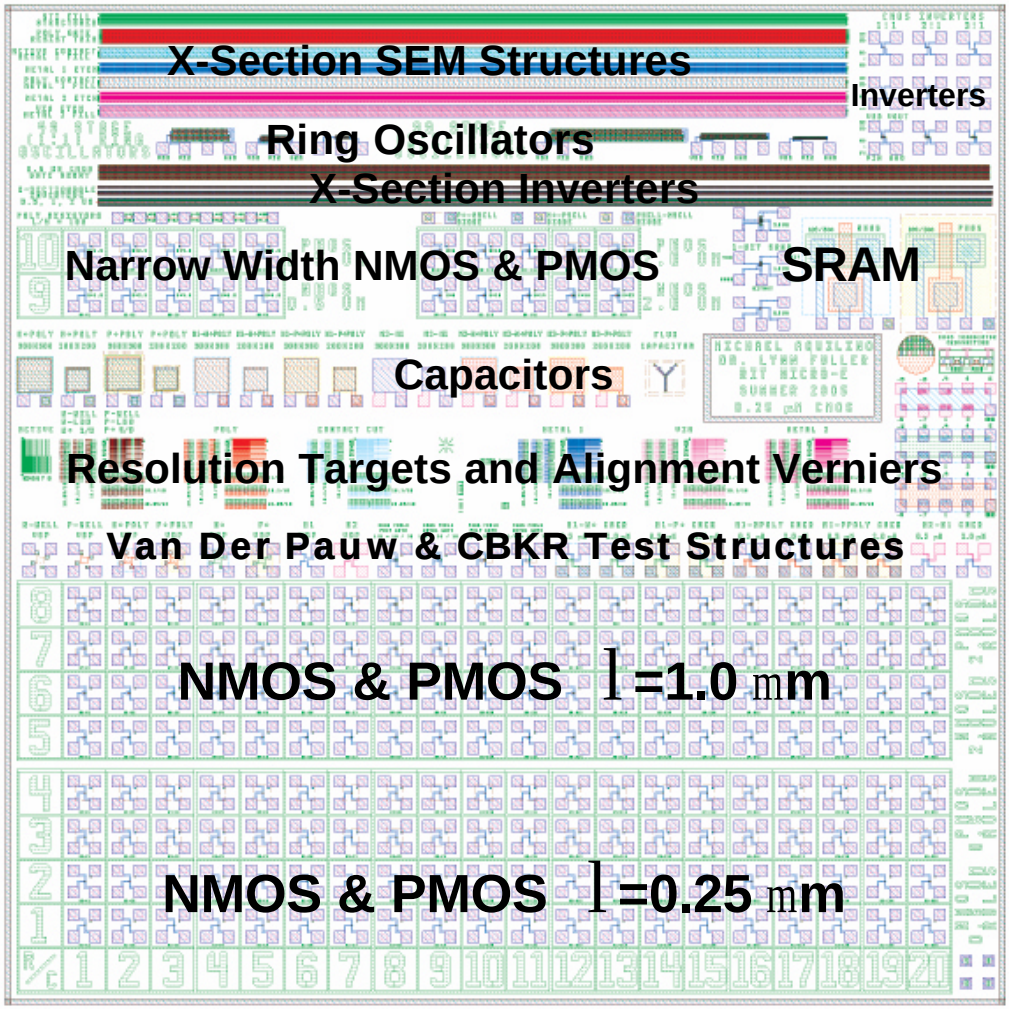


Figure 9: Test Chip Layout

- **9 Design Layers**
  - **Active**
  - **N-Well**
  - **Poly**
  - **N^+ Select**
  - **P^+ Select**
  - **Contact Cut**
  - **Metal 1**
  - **Via**
  - **Metal 2**
- **10 Masks**
- **12 Lithography Levels**

Layout of Test Chip



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0.25 µm Device Technology

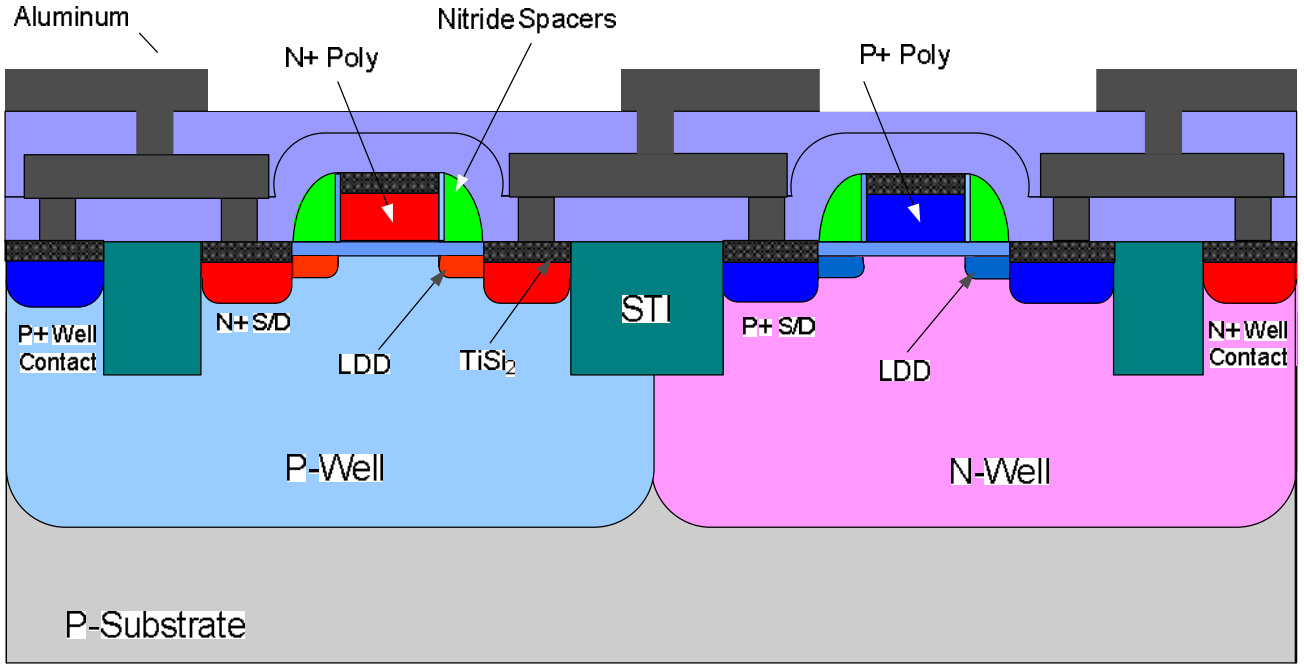


Figure 10: CMOS Inverter Cross Section showing NMOS (left) and PMOS (right) Transistors

- Shallow Trench Isolation
- 50 Å gate oxide w/ N_2O
- Polysilicon Reactive Ion Etch
- Arsenic/BF_2 Low Doped SDE
- Si_3N_4 Sidewall Spacers
- Dual Doped Poly Gates
- Rapid Thermal Dopant Activation
- Titanium Silicide
- Contact Cut Plasma Etch
- 2 Level Aluminum Metallization

RIE Trench Etch with Photoresist

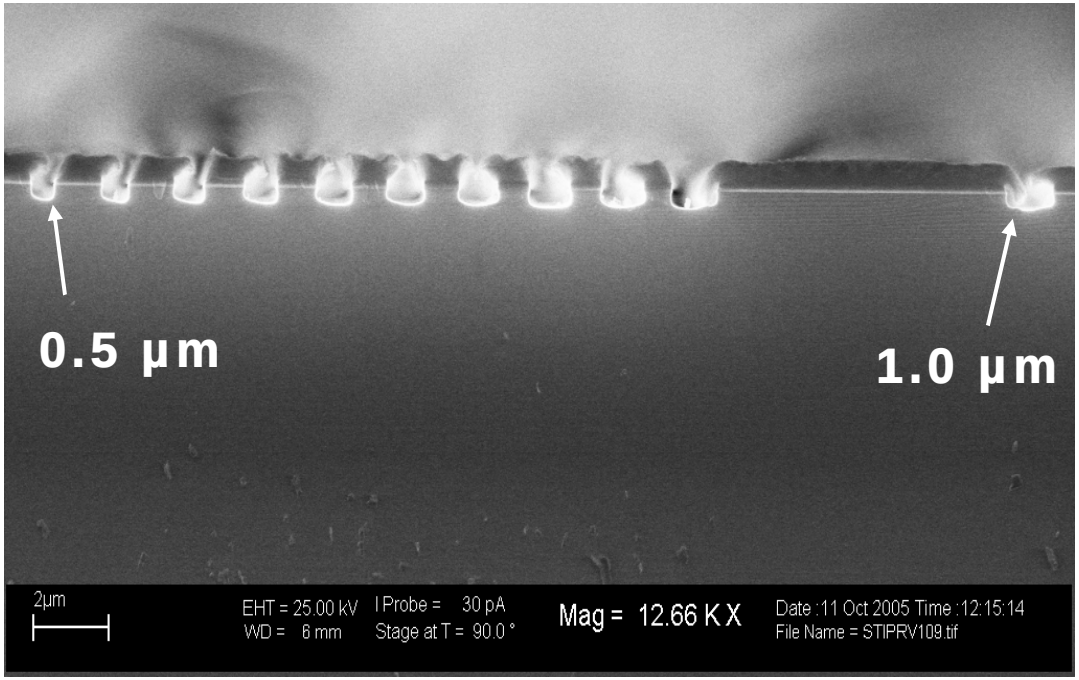


Figure 11: RIE of Silicon Trenches

Si_3N_4 Etch Rate = 1010 Å/min
SiO_2 Etch Rate = 489 Å/min
Si Etch Rate = 1175 Å/min

Recipe Parameters:
Power = 250 W
Pressure = 60 mTorr
SF_6 = 30 sccm
CHF_3 = 30 sccm
Drytek Quad - Chamber 2

- Target silicon trench depth is 4000 Å
- Photoresist is causing footing at bottom of trench towards the end of etch
- Need to increase hard bake temp to 140°C from 110°C
- Trenches as small as 0.5 µm wide can be etched
- 500 Å liner oxide thermally grown to repair damage to sidewalls of trench and round off the corners at the bottom for better TEOS filling

Uniformly Doped Twin Well

	NMOS	PMOS		NMOS Field	PMOS Field
Well Type	p	n		p	n
Gate Material	N^+ Poly	P^+ Poly		N^+ Poly	P^+ Poly
Doping Concentration (cm^{-3})	$6.5x10^{17}$	$5.5x10^{17}$		$6.5x10^{17}$	$5.5x10^{17}$
Junction Depth (µm)	3	3		3	3
Gate Oxide (Å)	50	50		4000	4000
Threshold Voltage (V)	+ 0.5 V	- 0.5 V		+ 50 V	- 50 V

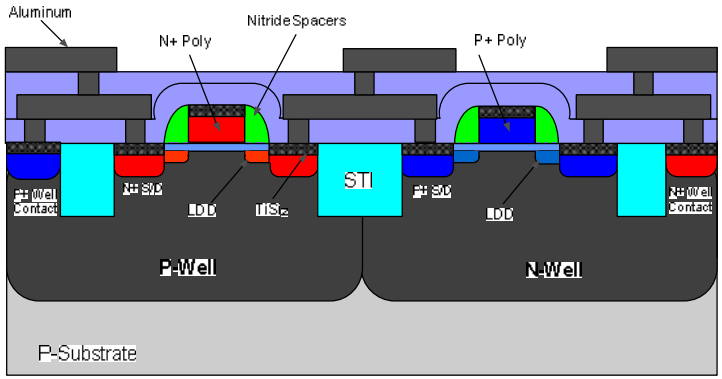


Figure 12: Twin Well Doping

- N & P Well implanted after the liner oxide before the STI TEOS fill
- Well Drive in for 6 hours @ 1100°C in N_2
- The junction depth of the wells must be large enough to prevent vertical punch-through between the reverse-biased drain of the PMOS and the starting wafer

7000 Å Trench Fill with PECVD TEOS

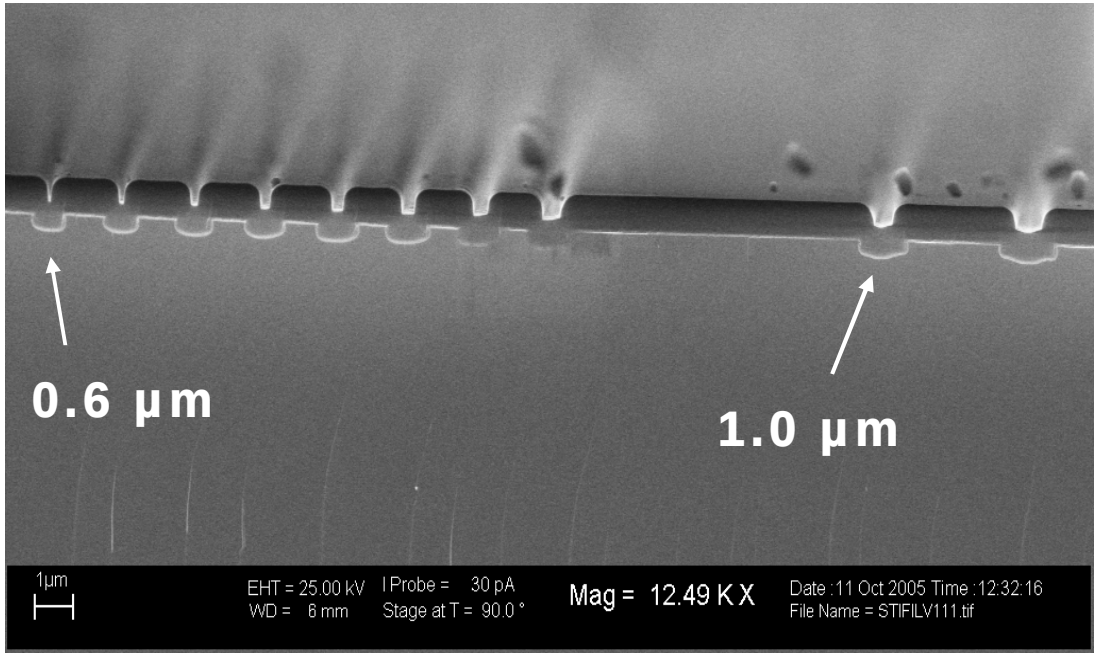


Figure 13: Shallow Trench After TEOS Deposition

Recipe Parameters:
Name = A6-7000A TEOS LS
Power = 295 W
Pressure = 9000 mTorr
TEOS = 400 sccm
O_2 = 285 sccm
Temp = 390°C

- Trenches filled with 7000 Å PECVD TEOS in Applied Materials P-5000
- 4000 Å Si + 500 Å Pad Ox + 1500 Å Nitride + 1000 Å overfill = 7000 Å
- CMP is used to polish TEOS off active areas using nitride as stop layer

Shallow Trench Isolation After CMP

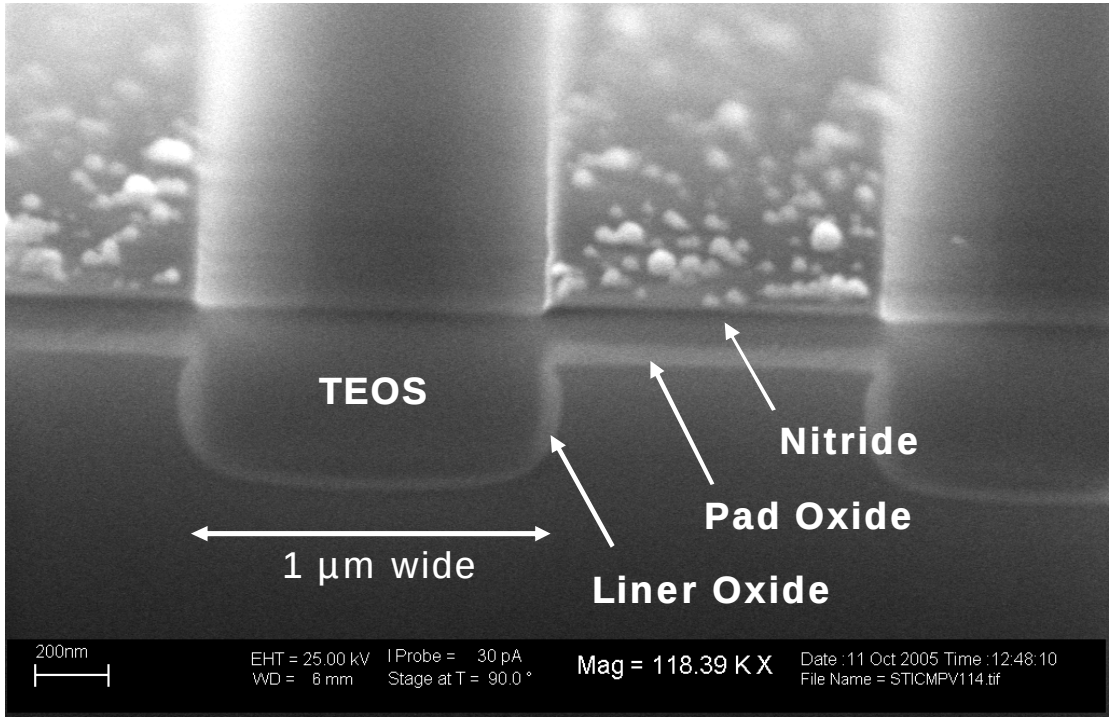


Figure 14: 1 µm Shallow Trench After CMP

TEOS Removal = 1574 Å/min
Si_3N_4 Removal = 407 Å/min

SiO_2/Si_3N_4 Selectivity = 3.87

Recipe Parameters:
Down Force = 6 PSI
Carrier = 70 RPM
Table = 50 RPM
Slurry = 60 mL/min

- Nitride protects the active areas where the transistors will be built
- After cleans, a TEOS densification is done to lower TEOS etch rate in HF
- Nitride and Pad Oxide removed so 50 Å gate oxide can be grown

C-V Analysis of P^+/N^+ Poly Capacitors

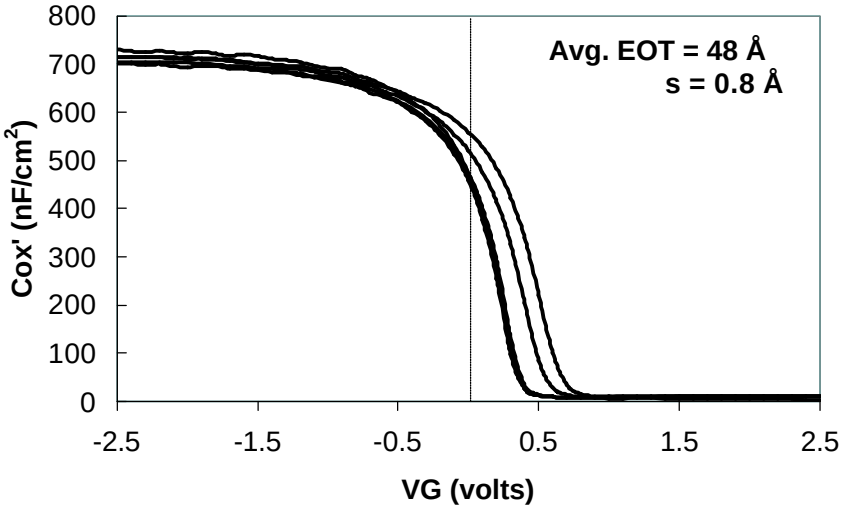


Figure 15: P^+ Poly Capacitor with 48 Å EOT

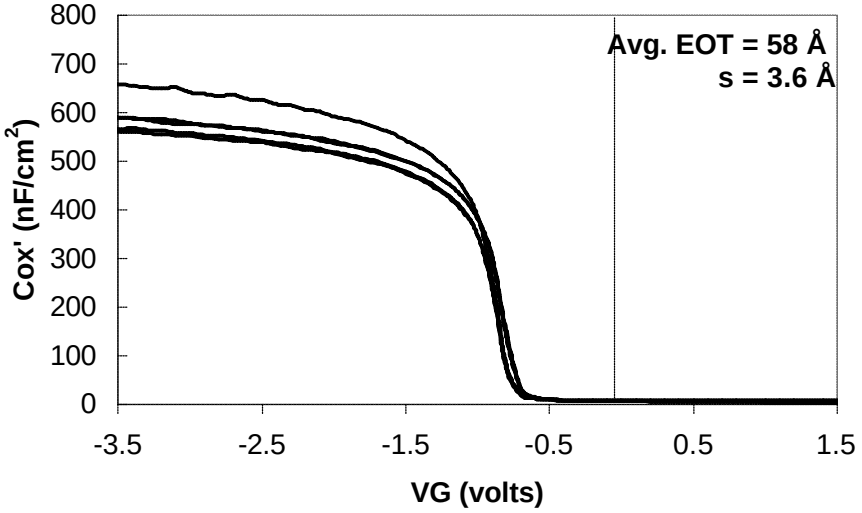


Figure 16: N^+ Poly Capacitor with 58 Å EOT

- Nitrogen is incorporated into the gate oxide from N_2O gas to prevent boron from diffusing from P^+ poly into the channel during the source/drain anneal
- 50 Å gate oxide measured with Variable Angle Spectroscopic Ellipsometer
- P^+ poly capacitors exhibit no poly depletion with average EOT = 48 Å
- N^+ poly capacitors exhibit some poly depletion with average EOT = 58 Å

Photoresist Trimming for 0.25 µm Gate Length

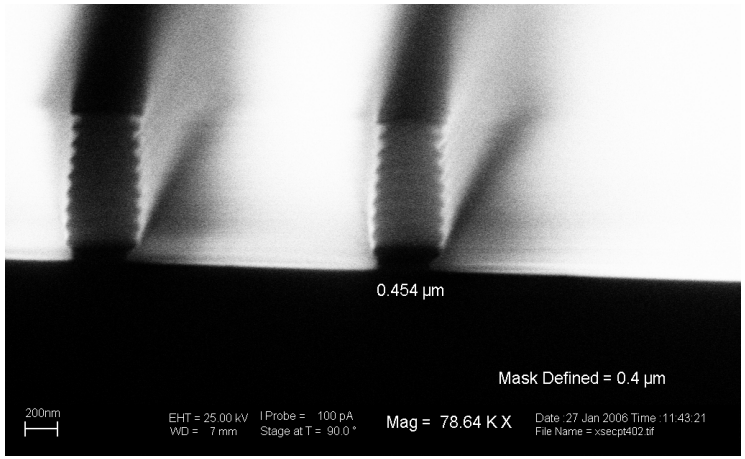


Figure 17: 0.45 µm PR Line Before Trim

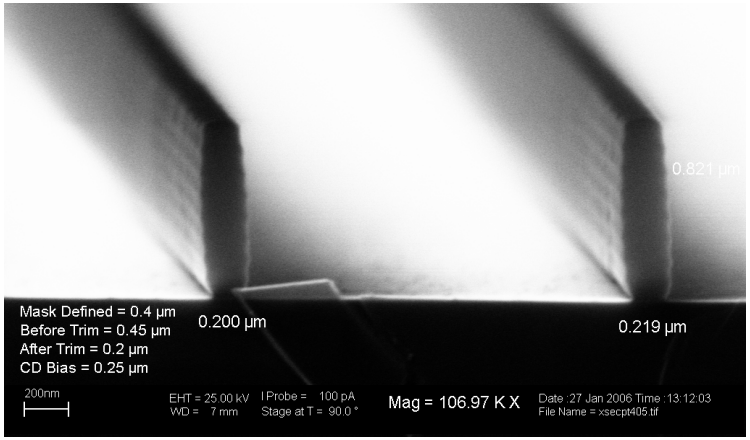


Figure 18: 0.2 µm PR Line After Trim

- Resolution limit of Canon i-line stepper ~ 0.5 µm

- 1250 Å of PR is etched off each side of 0.5 µm PR lines in O_2 plasma to make 0.25 µm lines

<u>Recipe Parameters:</u>
Power = 100 W
Pressure = 400 mTorr
O_2 = 20 sccm
Gap = 1.65 cm
Tool = LAM490

- PR Horizontal Etch Rate = 555 Å/min
- PR Vertical Etch Rate = 720 Å/min
- Anisotropy = $(1-ER_H/ER_V)$ = 0.23

Polysilicon Reactive Ion Etch

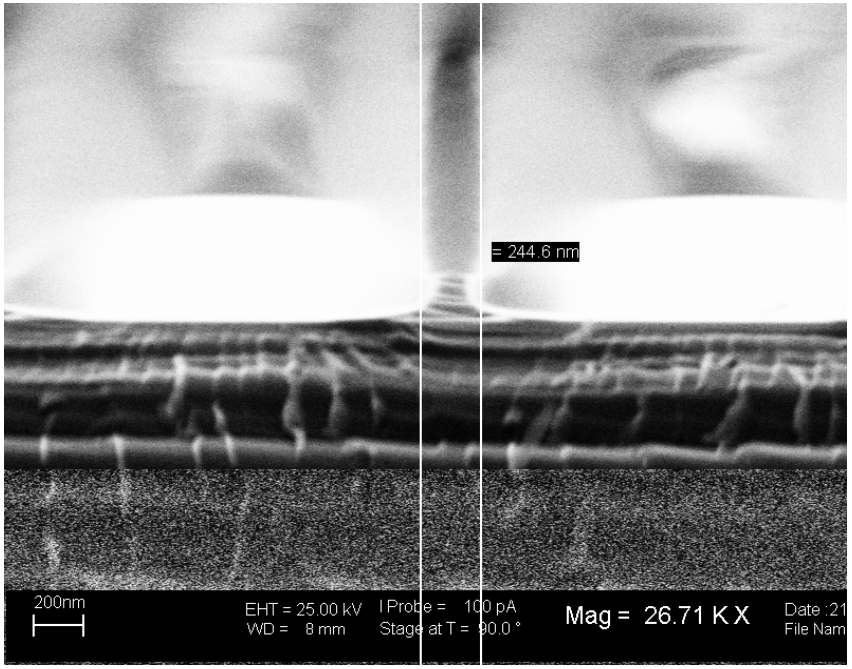


Figure 19: 0.25 µm Poly Gate Length

Poly Etch Rate = 336 Å/min
SiO_2 Etch Rate = 70 Å/min

Poly/SiO_2 Selectivity = 4.8

Recipe Parameters:
Power = 200 W
Pressure = 30 mTorr
SF_6 = 10 sccm
CHF_3 = 35 sccm
O_2 = 5 sccm
Drytek Quad - Chamber 2

- 0.25 µm PR lines are transferred into 2000 Å LPCVD polysilicon layer
- 75° sidewall angle with RIE recipe
- < 90° angle reduces crossectional area of gate: R_{Gate} -, switching speed ¯

Poly Re-Oxidation

- After plasma etch of gate there is damage to edges of gate oxide
- A 100 Å oxide is thermally grown to:
  - Repair damage to edges of gate oxide from plasma etch of the poly gate
  - Create a thicker screening oxide for source/drain extension implant
  - Make a thicker etch stop for sidewall spacer etch process
  - Form an off-set region for lateral diffusion of shallow s/d extension

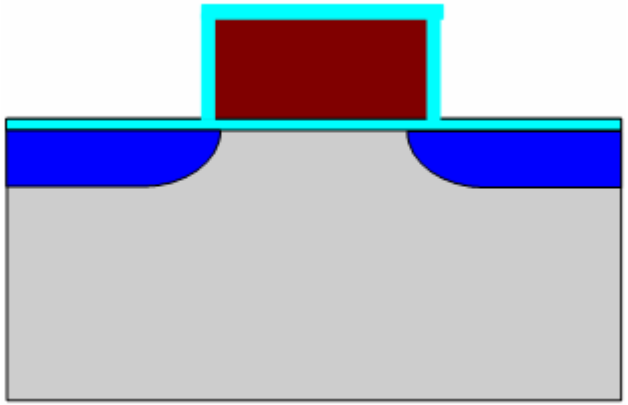


Figure 20: Poly Re-Oxidaiton

- Want to reduce gate overlap of s/d to reduce Miller Capacitance
  - This capacitance will reduce the cut-off frequency of the device
- Need 15 – 20 nm of gate overlap for proper capacitive coupling of the gate to the channel or drive current will degrade [6]

As/BF_2 Low Doped S/D Extensions

- Low energy BF_2 and Arsenic ions are implanted for shallow junctions self aligned to the poly gate

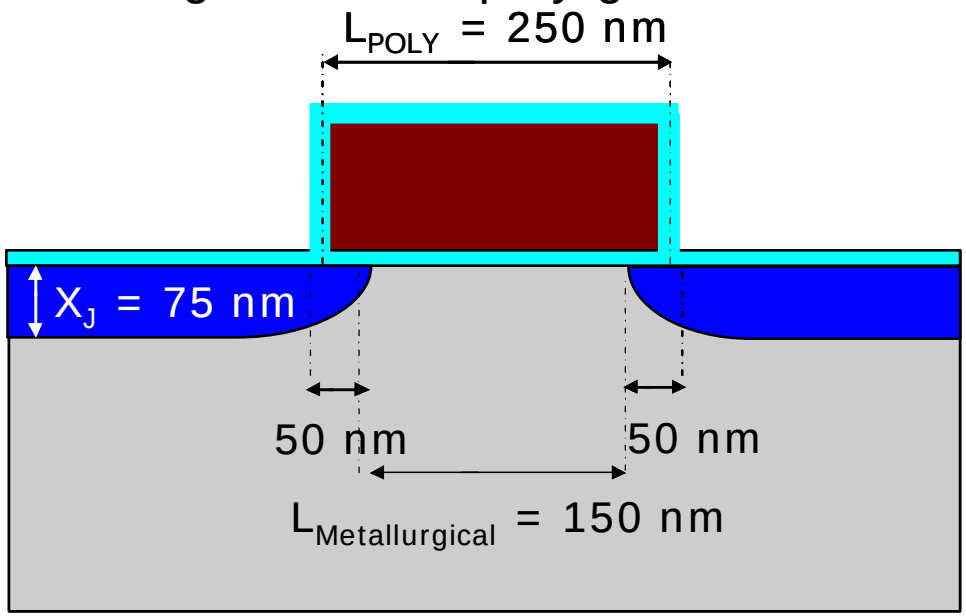
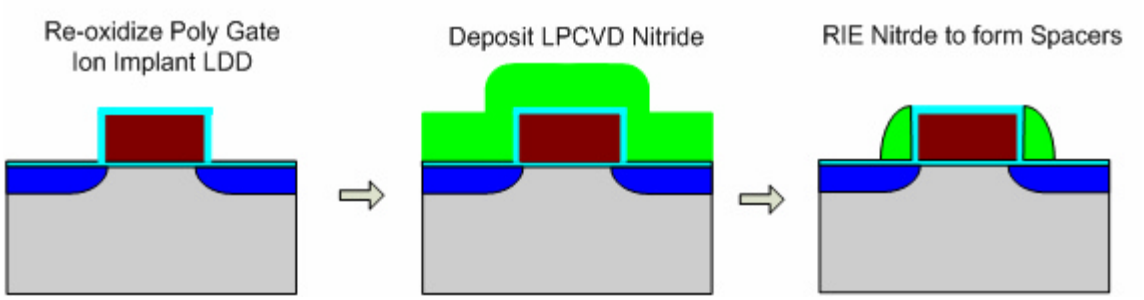


Figure 21: Effective Channel Length Estimation

- NMOS LDD
  - 25 keV, As, $2.75x10^{13}$ cm^{-2}
  - X_J = 75 nm
  - N_D = $5x10^{18}$ cm^{-3}
- PMOS LDD
  - 20 keV, BF_2, $3.5x10^{13}$ cm^{-2}
  - X_J = 75 nm
  - N_D = $5x10^{18}$ cm^{-3}

- Gate Overlap = 50 nm – 10 nm = 40 nm = 15 – 20 nm requirement
- $L_{EFFECTIVE}$ will be extracted to be between L_{POLY} and $L_{Metallurgical}$
- Process is designed for L_{POLY} = 0.25 µm and $L_{EFFECTIVE}$ = 0.20 µm

Silicon Nitride Sidewall Spacers



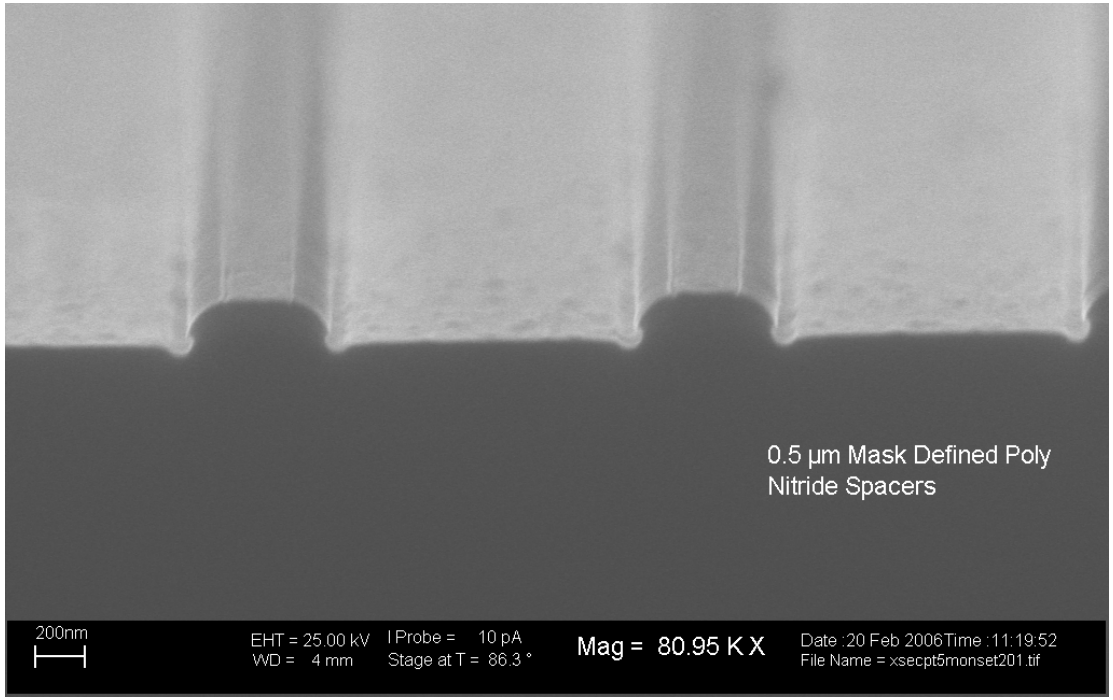


Figure 22: Nitride Sidewall Spacers

- $t_{Nitride} = t_{Poly}$
- L_{Spacer} is determined by:
  - Poly thickness
  - Nitride conformality
  - Etch anisotropy

Si_3N_4 Etch Rate = 1110 Å/min
SiO_2 Etch Rate = 555 Å/min

Si_3N_4/SiO_2 Selectivity = 2

<u>Recipe Parameters:</u>
Power = 250 W
Pressure = 60 mTorr
SF_6 = 30 sccm
CHF_3 = 30 sccm
Drytek Quad – Chamber 2

As/BF_2 Source/Drain & Poly Contact Implant

- High dose BF_2 and Arsenic ions are implanted at higher energies for the deeper source/drain contacts that are self aligned to the spacers

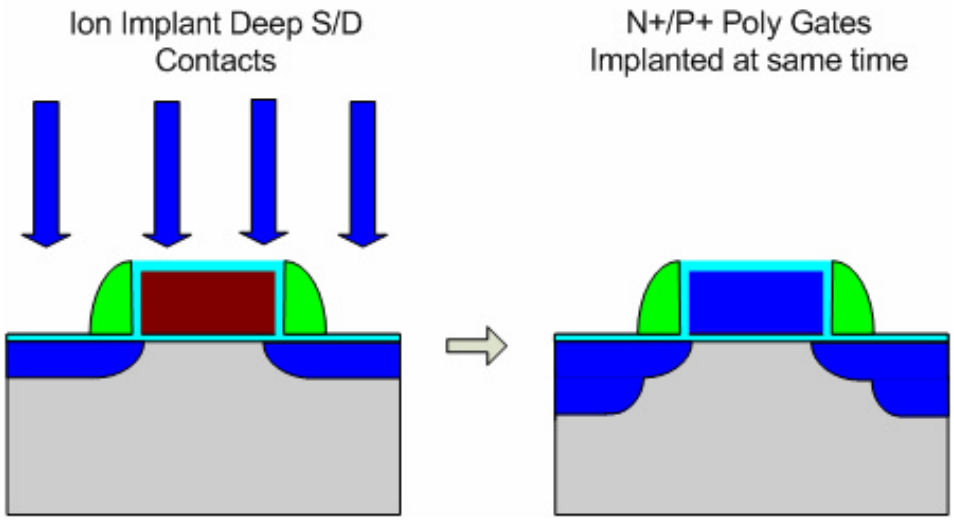


Figure 23: S/D Contact & Poly Doping

- NMOS Source/Drain Contact
  - 30 keV, As, $5x10^{15}$ cm^{-2}
  - X_J = 150 nm
  - $N_D \geq 1x10^{20}$ cm^{-3}
- PMOS Source/Drain Contact
  - 25 keV, BF_2, $5x10^{15}$ cm^{-2}
  - X_J = 150 nm
  - $N_D \geq 1x10^{20}$ cm^{-3}

- Poly Gates doped at the same time as the source/drain contact implants
- N^+ Poly for NMOS and P^+ Poly for PMOS for surface channel devices

Rapid Thermal Dopant Activation

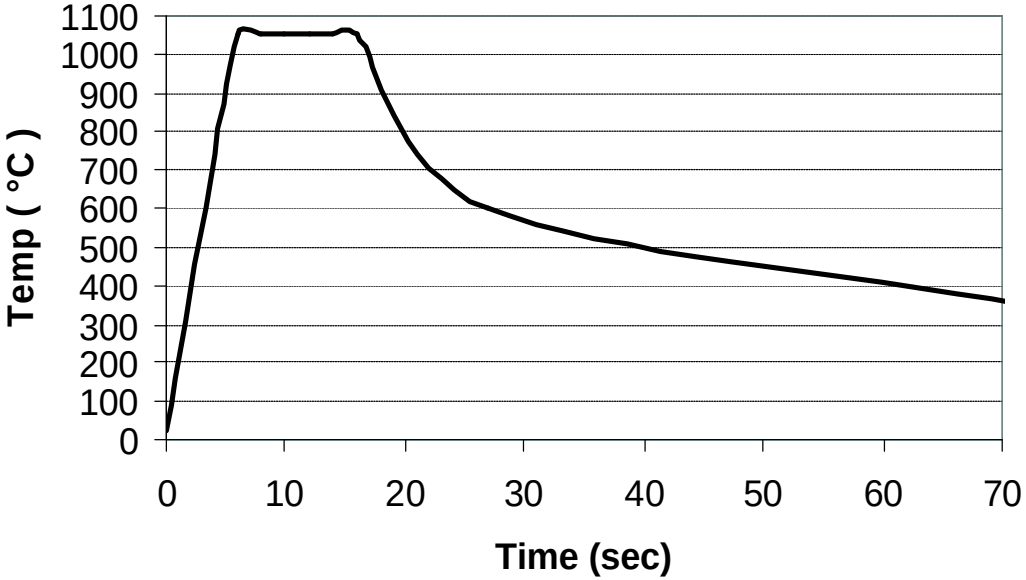


Figure 24: RTP Temperature Profile

- Tool = AG610-A RTP
- Recipe = MVA1050A.RCP
- Ramp up to 1050°C @ 200°C/sec
- Soak for 10 seconds in N_2
- Ramp down to 600°C @ 41°C/sec

- A high temperature thermal step is required for dopant activation and to repair damage to the silicon lattice caused by the high dose S/D implants
- Rapid Thermal Processor needed to avoid TED temp ranges (670–900°C) [7]
- Arsenic not as susceptible to Transient Enhanced Diffusion compared to BF_2

Self Aligned Titanium Silicide ($TiSi_2$)

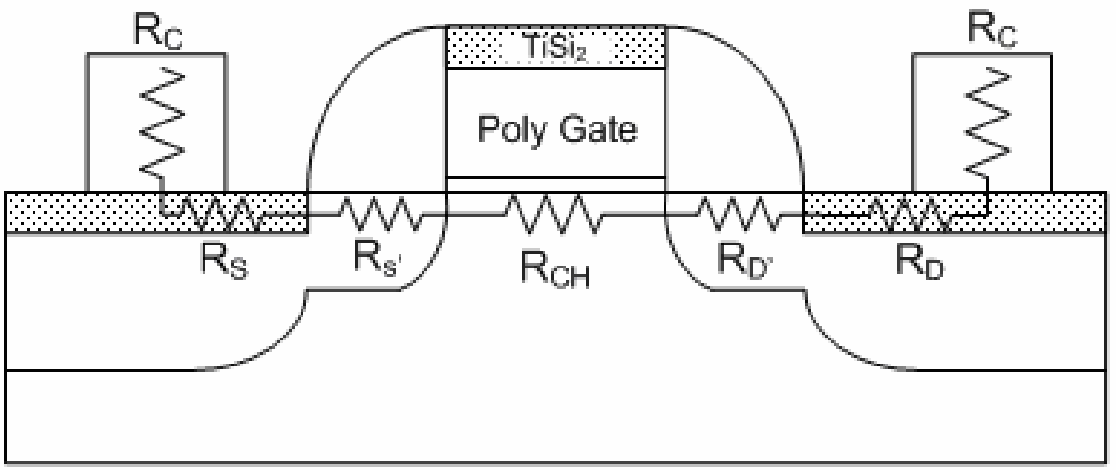


Figure 25: $TiSi_2$ for Low Contact Resistance to Source & Drain

- Two-step silicide process to reduce R_S and R_D
- Higher resistivity C49 Phase – 30 seconds @ 715°C in N_2
- Etch un-reacted Titanium in 2:1 H_2O_2:H_2SO_4
- Lower resistivity C54 Phase – 20 seconds @ 850°C in N_2

	After S/D Anneal	After RTP-1 & Ti etch	After RTP-2
Average Sheet Resistance (Ω/sq)	45	12.86	1.66

Contact Cut Reactive Ion Etch

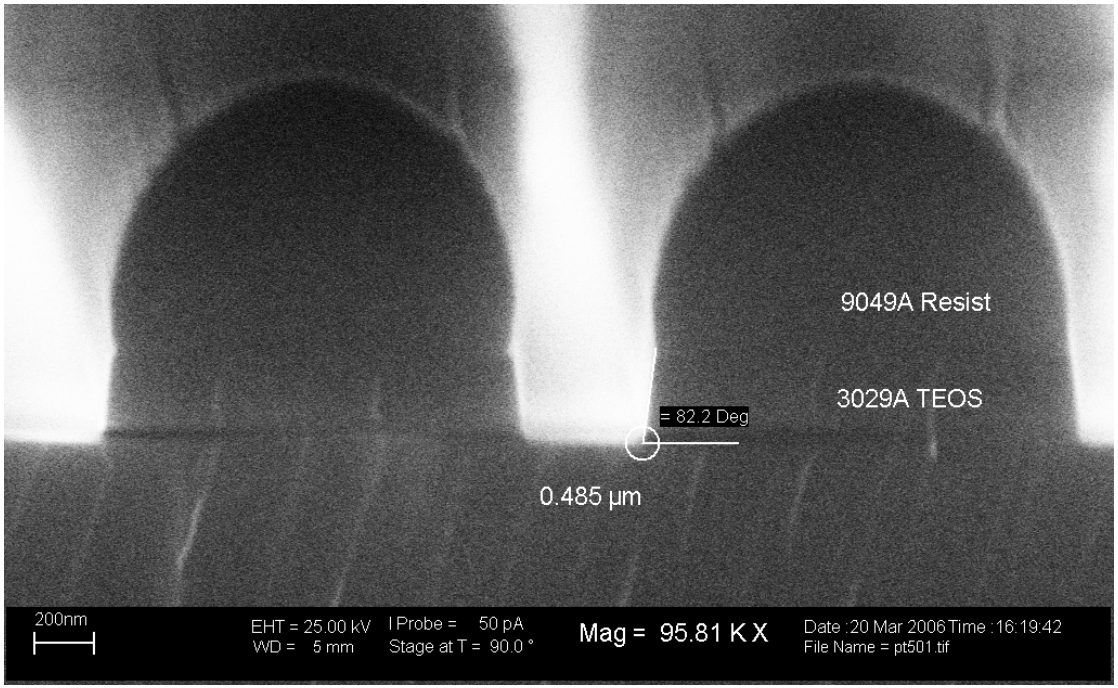


Figure 26: Contact Cut RIE

SiO_2 Etch Rate = 1850 Å/min
Si Etch Rate = 320 Å/min

SiO_2/Si Selectivity = 5.78

Recipe Parameters:
Applied Materials P-5000
Recipe = C6 – Oxide Etch
Power = 650 W
Pressure = 250 mTorr
CHF_3 = 100 sccm
CF_4 = 50 sccm
B = 40 Gauss

- 0.5 µm contact cuts etched in 3000 Å of TEOS
- 82° Sidewall Angle with RIE recipe

Aluminum Metallization

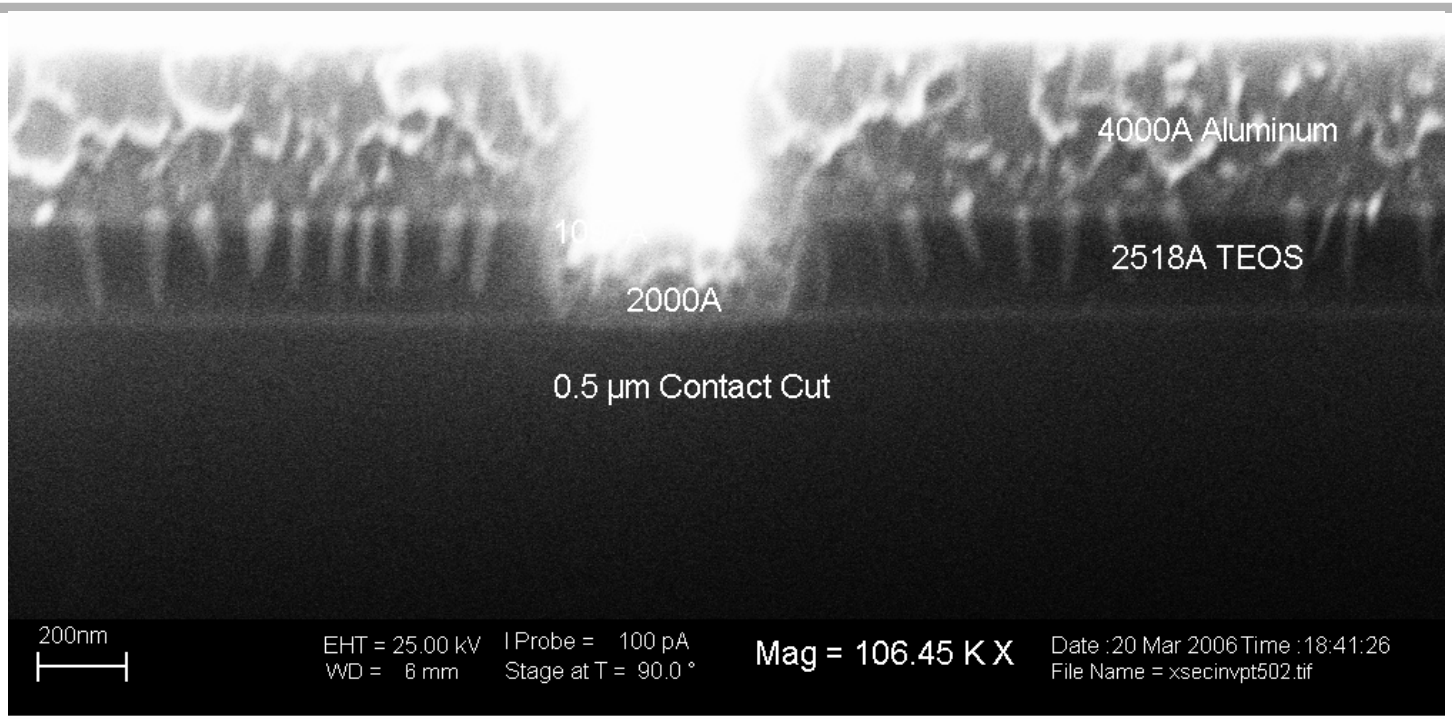


Figure 27: 0.5 µm Contact Cuts After Metal 1

- 0.5 µm contact cuts are filled with 5000 Å of Aluminum
- Smaller areas are more difficult to fill
- Back End CMP, Via and Metal 2 processes still need characterization

ID-VD for 0.25 µm NMOS Transistor

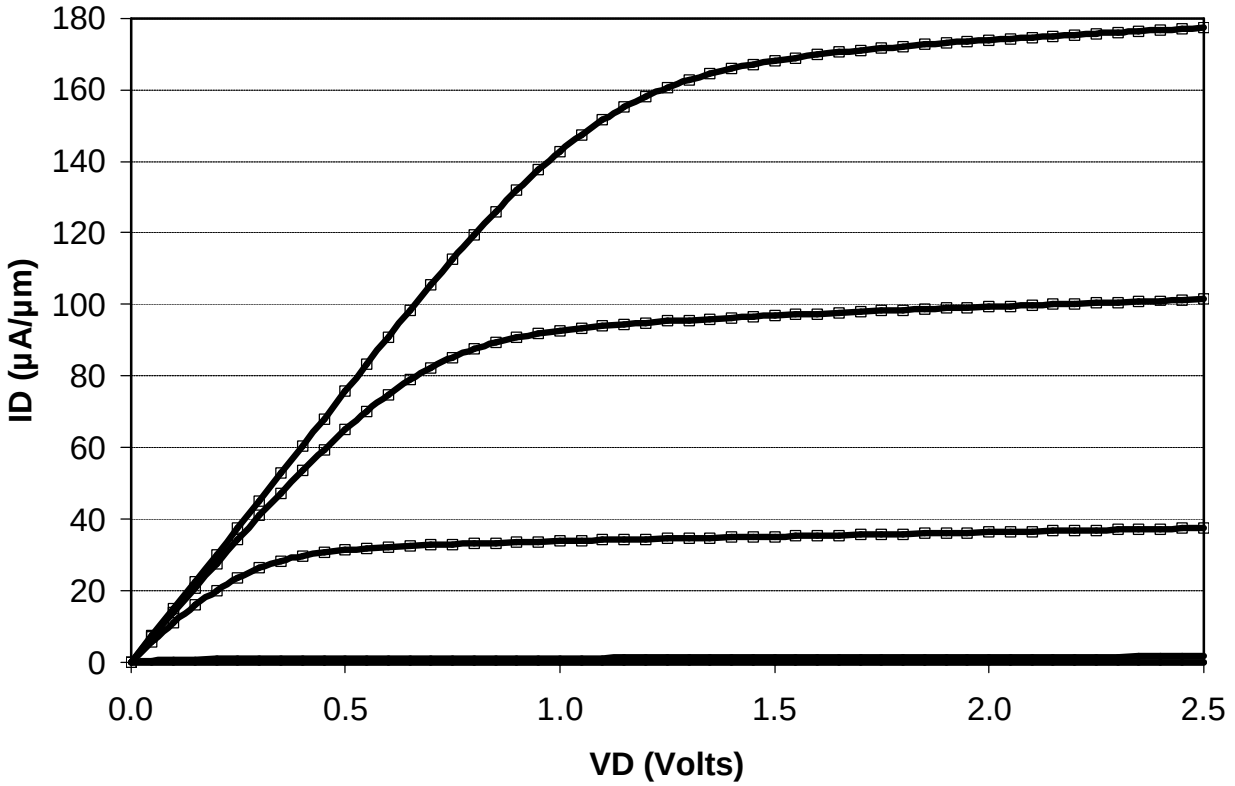


Figure 28: ID-VD for 0.25 µm NMOS Transistor

- L_{mask} = 0.5 µm
- L_{poly} = 0.25 µm
- $L_{effective}$ = 0.2 µm

- ID = 177 µA/µm @ VG=VD=2.5 V
- V_T = 1.0 V

*This is RIT's Smallest NMOS Transistor

ID-VG Sub-threshold 0.25 µm NMOS

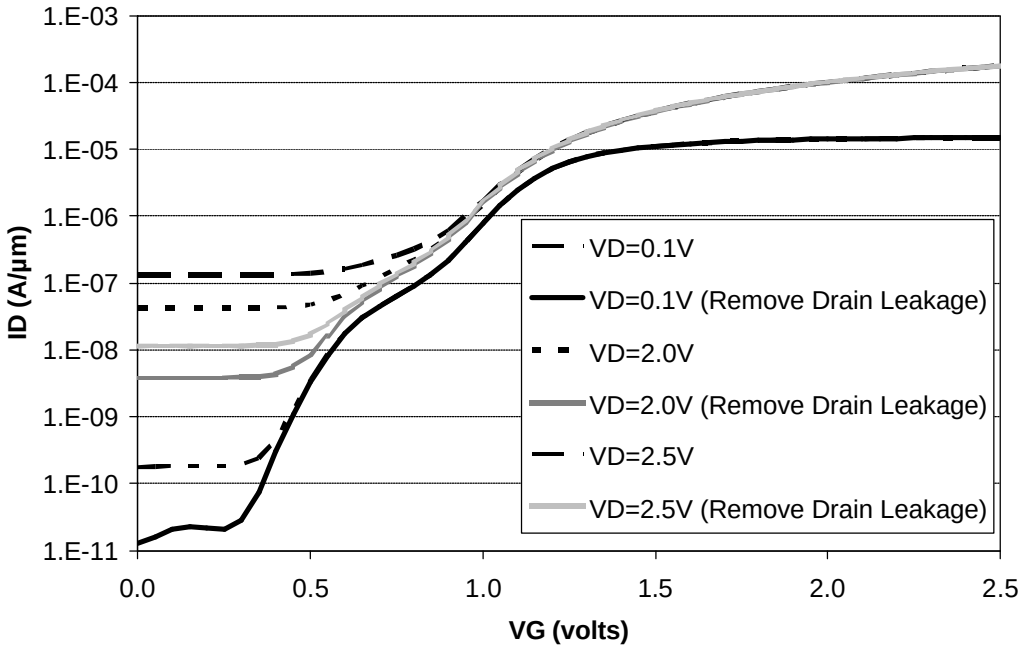


Figure 29: ID-VG for 0.25 µm NMOS Transistor

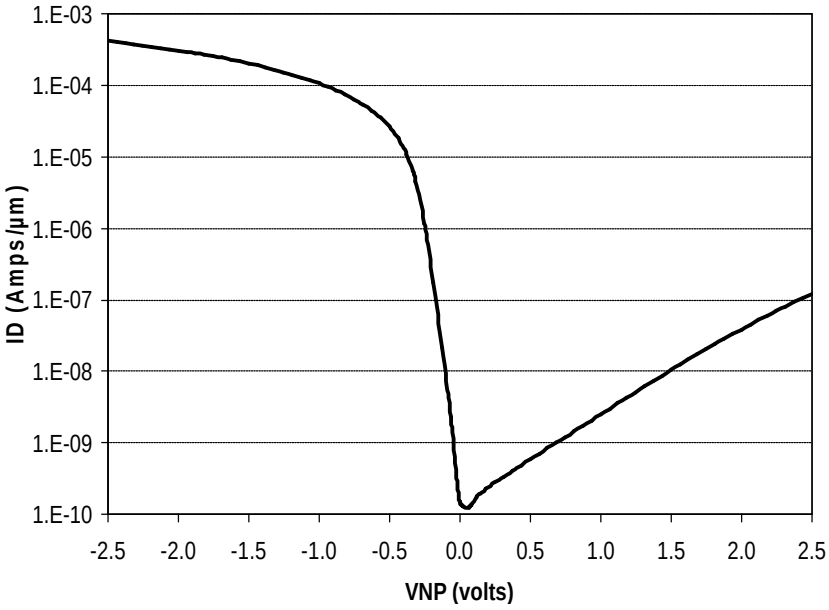


Figure 30: NMOS Drain Diode Leakage

- I_{off} = 13 pA/µm @ VD=0.1 V (with drain diode leakage removed)
- I_{off} = 11 nA/µm @ VD=2.5 V (with drain diode leakage removed)
- Log(I_{on}/I_{off}) = 4.2 decades
- SS = 119 mV/decade @ VD=0.1 V

ID-VD for 0.25 µm PMOS Transistor

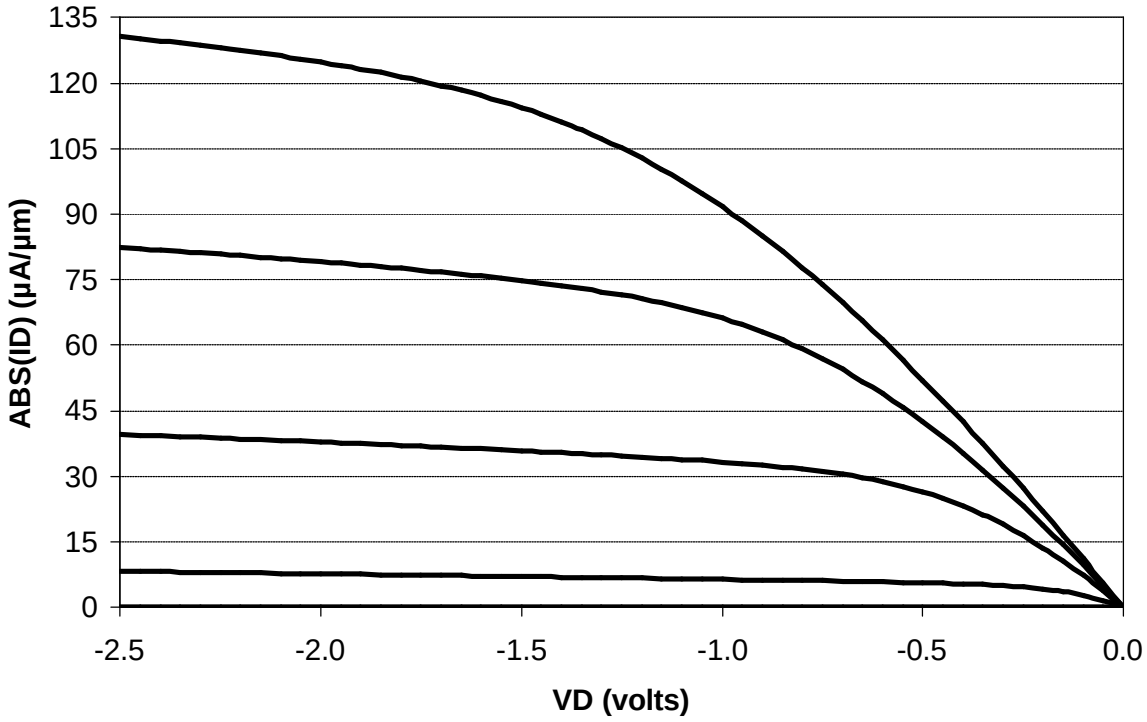


Figure 31: ID-VD for 0.25 µm PMOS Transistor

- L_{mask} = 0.6 µm
- L_{poly} = 0.25 µm
- $L_{effective}$ = 0.2 µm

- |ID| = 131 µA/µm @ VG=VD=-2.5 V
- V_T = -0.75 V

*This is RIT's Smallest PMOS Transistor

ID-VG Sub-threshold 0.25 µm PMOS

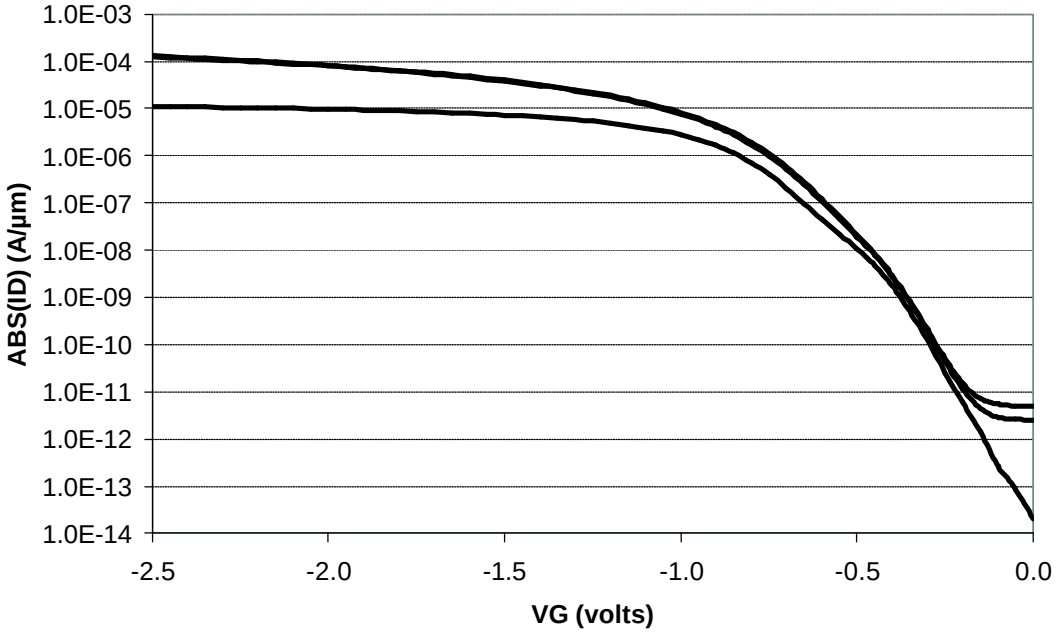


Figure 32: ID-VG for 0.25 µm PMOS Transistor

- I_{off} = -20 fA/µm @ VD=-0.1 V
- I_{off} = -4.9 pA/µm @ VD=-2.5 V
- Log(I_{on}/I_{off}) = 7.4 decades
- SS = 75 mV/decade @ VD=-0.1 V
- SS = 85 mV/decade @ VD=-2.5 V
- DIBL = 8.3 mV/V @ ID=-1 nA/µm

V_T Roll-Off

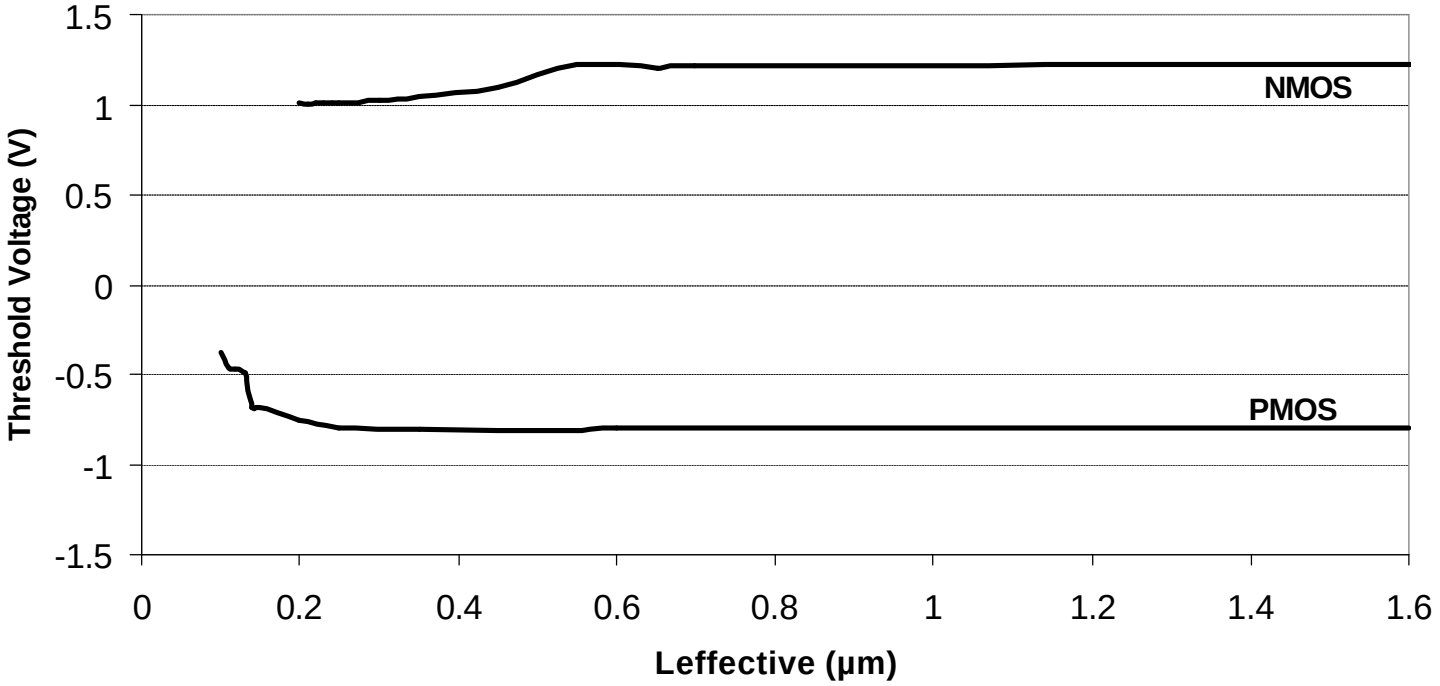
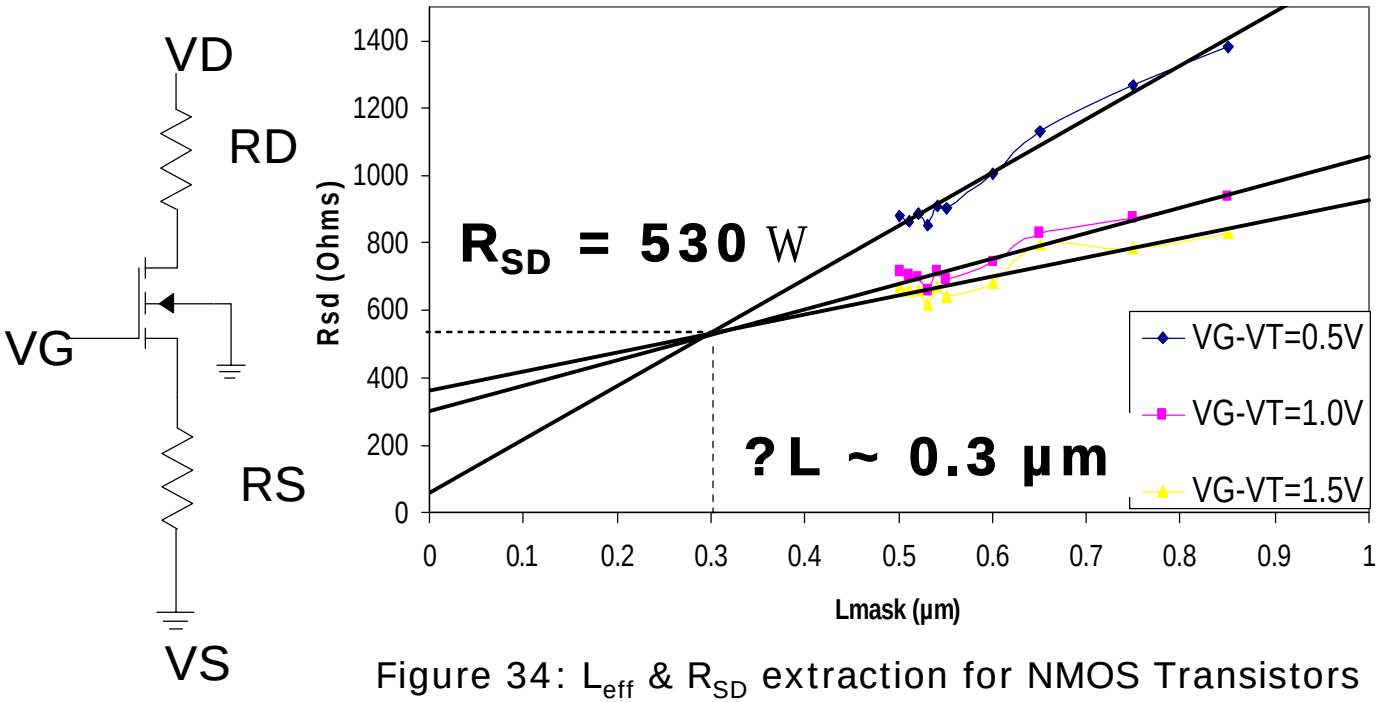


Figure 33: Threshold Voltage Roll-off Short Channel Effect

- As the gate length decreases, V_T decreases in magnitude
- For small enough $L_{effective}$, the V_T's can decrease to 0 V
- Energy barrier lowering from drain so severe, the devices are on at V_G=0 V

NMOS Terada-Muta Method for L_{eff} and R_{SD}



$L_{eff} = L_{mask} - ?L$
$L_{eff} = 0.5\ \mu m - 0.3\ \mu m$
$L_{eff} = 0.2\ \mu m$

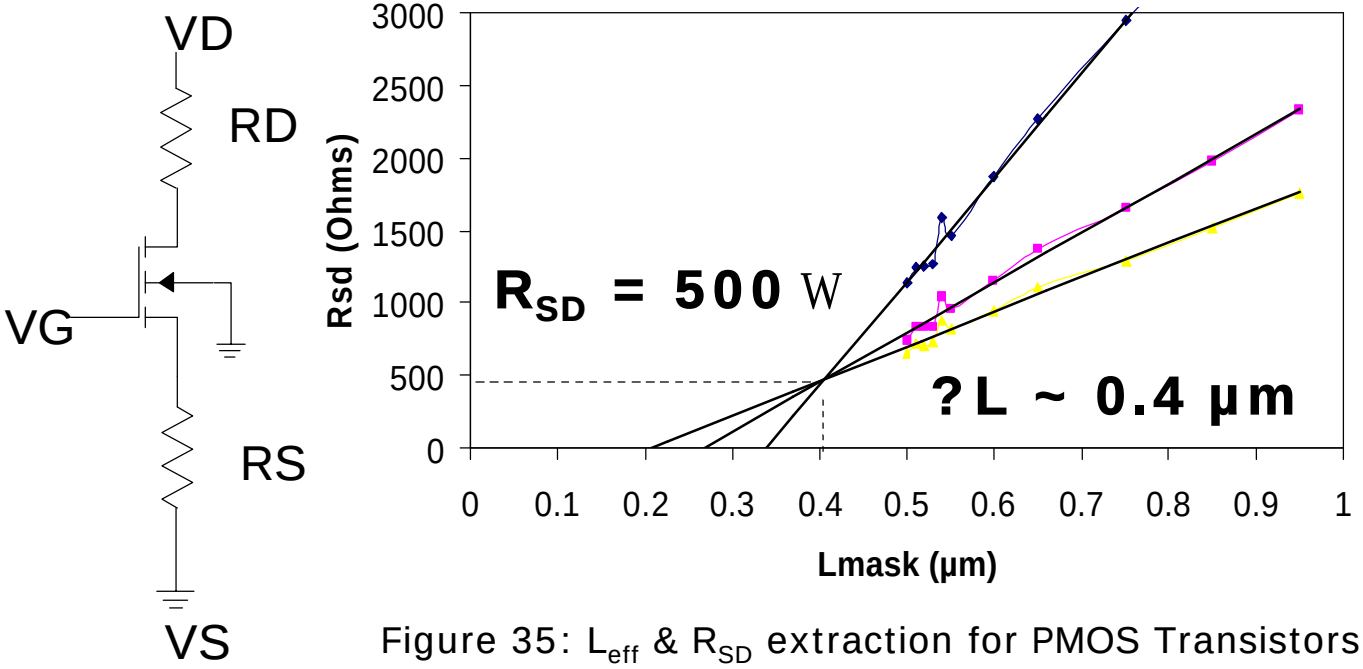
Figure 34: L_{eff} & R_{SD} extraction for NMOS Transistors

Linear Region:
$V_D = 0.1V$
$V_G - V_T >> I_D R_{SD}$
At low I_D, V_{RSD} small

$$Rm = \frac{Vd}{Id} = R_{SD} + \frac{(L_{mask} - ?L)}{\mu Cox'W(V_{GS} - V_t)}$$

Plot R_m vs. L_{mask} for different $(V_{GS} - V_t)$ [8]

PMOS Terada-Muta Method for L_{eff} and R_{SD}



$L_{eff} = L_{mask} - ?L$
$L_{eff} = 0.6\ \mu m - 0.4\ \mu m$
$L_{eff} = 0.2\ \mu m$

Figure 35: L_{eff} & R_{SD} extraction for PMOS Transistors

Linear Region:
$V_D = 0.1V$
$V_G - V_T >> I_D R_{SD}$
At low I_D, V_{RSD} small

$$Rm = \frac{Vd}{Id} = R_{SD} + \frac{(L_{mask} - ?L)}{\mu Cox'W(V_{GS} - V_t)}$$

Plot R_m vs. L_{mask} for different $(V_{GS} - V_t)$ [8]

Summary

- Unit Processes have been developed to achieve 0.25 µm CMOS Transistors
- The unit processes have been integrated into a 75-step CMOS process flow
- Fabrication has been completed and transistors characterized
- This process can be improved upon for increased transistor performance as well as integrating high-k and strained silicon technologies in the future

Acknowledgements

I would like to thank the following people for their advisement and support in this work and throughout my 6 years at RIT:

- Dr. Lynn Fuller (M.S. Thesis Advisor)
- Dr. Santosh Kurinec (Committee Member)
- Dr. Karl Hirschman (Committee Member)

- MicroE Faculty & Staff
  - Dr. Sean Rommel
  - Dr. Michael Jackson
  - Dr. Bruce Smith
  - Dr. Robert Pearson
  - Prof. Dale Ewbank
  - Sara Widlund
- SMFL Staff
  - Bruce Tolleson
  - Dave Yackoff
  - Sean O'Brien
  - Scott Blondell
  - Tom Grimsley
  - Rich Battaglia
  - John Nash
- Graduate Students
  - Dan Jaeger
  - Reinaldo Vega
  - Eric Woodard
  - Mike Latham
  - Rob Manley
  - Germain Fenger

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