Introduction to the Long and Short Channel MOSFET

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10-13-2014 MOSFET-Long-Short-Intro.ppt

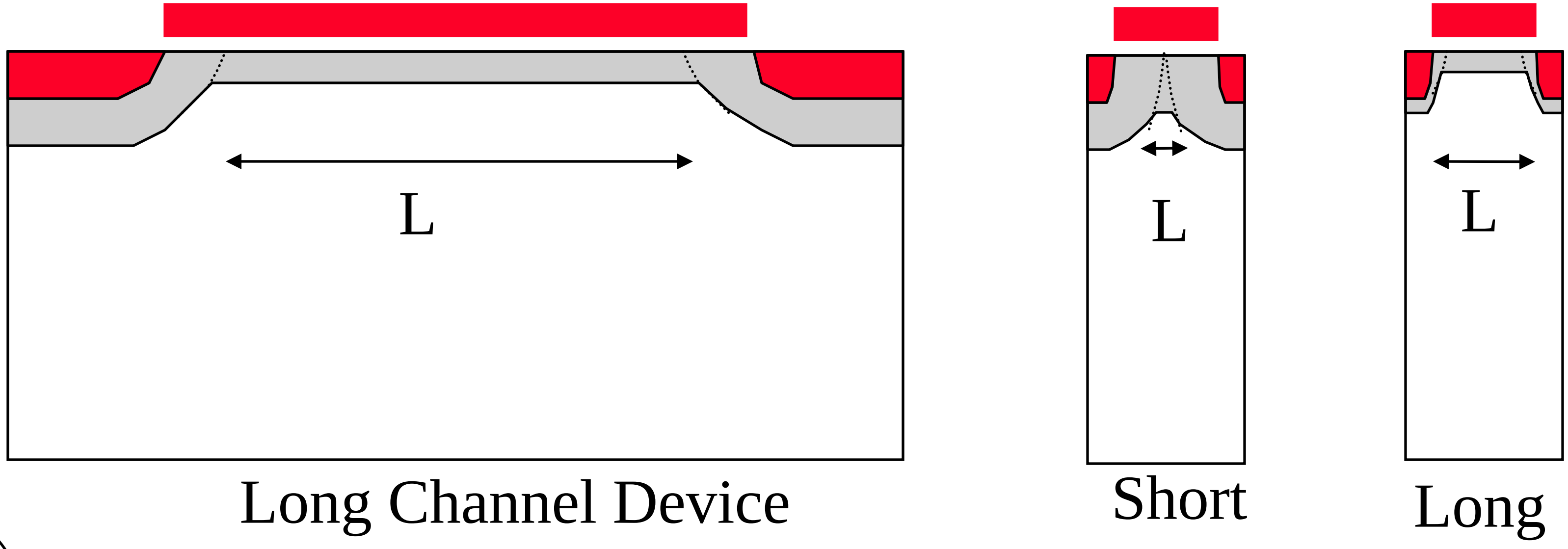
OUTLINE

Long Channel vs. Short Channel
MOSFET I-V Characteristics
MOS Threshold Voltage
Lambda, Gamma, Kappa
Leff
VT Rolloff, DIBL
Punchthrough
Mobility, Effective Mobility, Theta, Vmax, Eta
Gate Oxide Leakage
Salacide
Work Function Engineering, Surface/Buried Channel
Strained Silicon, Current Drive in MOSFETs
FIN FETS
References
Homework

THE LONG CHANNEL MOSFET

Long-channel MOSFET is defined as devices with width and length long enough so that edge effects from the four sides can be neglected

Channel length L must be much greater than the sum of the drain and source depletion widths. The goal is to make tiny long channel devices



Tiny Long Channel

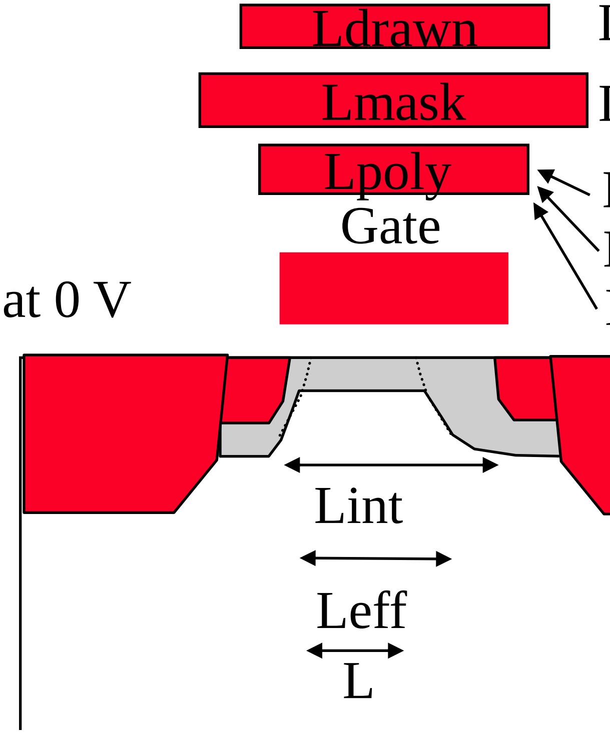
LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L

Ldrawn = what was drawn

Lambda = design rule parameter, λ, ie 0.25µm

Lmin = min drawn poly length, 2λ 0.50µm

Lmask = ? Depends on +/-bias 5X, 4X, etc.



Lresist after photo (resist trimming??) 0.40µm

Lpoly after poly etch 0.35µm

Lpoly after poly reoxidation 0.30µm

Source at 0 V

Drain at 3.3V

0.30µm

0.27µm

0.11µm

Internal Channel Length, Lint =distance between junctions, including under diffusion

Effective Channel Length, Leff = distance between space charge layers,Vd = Vs= 0

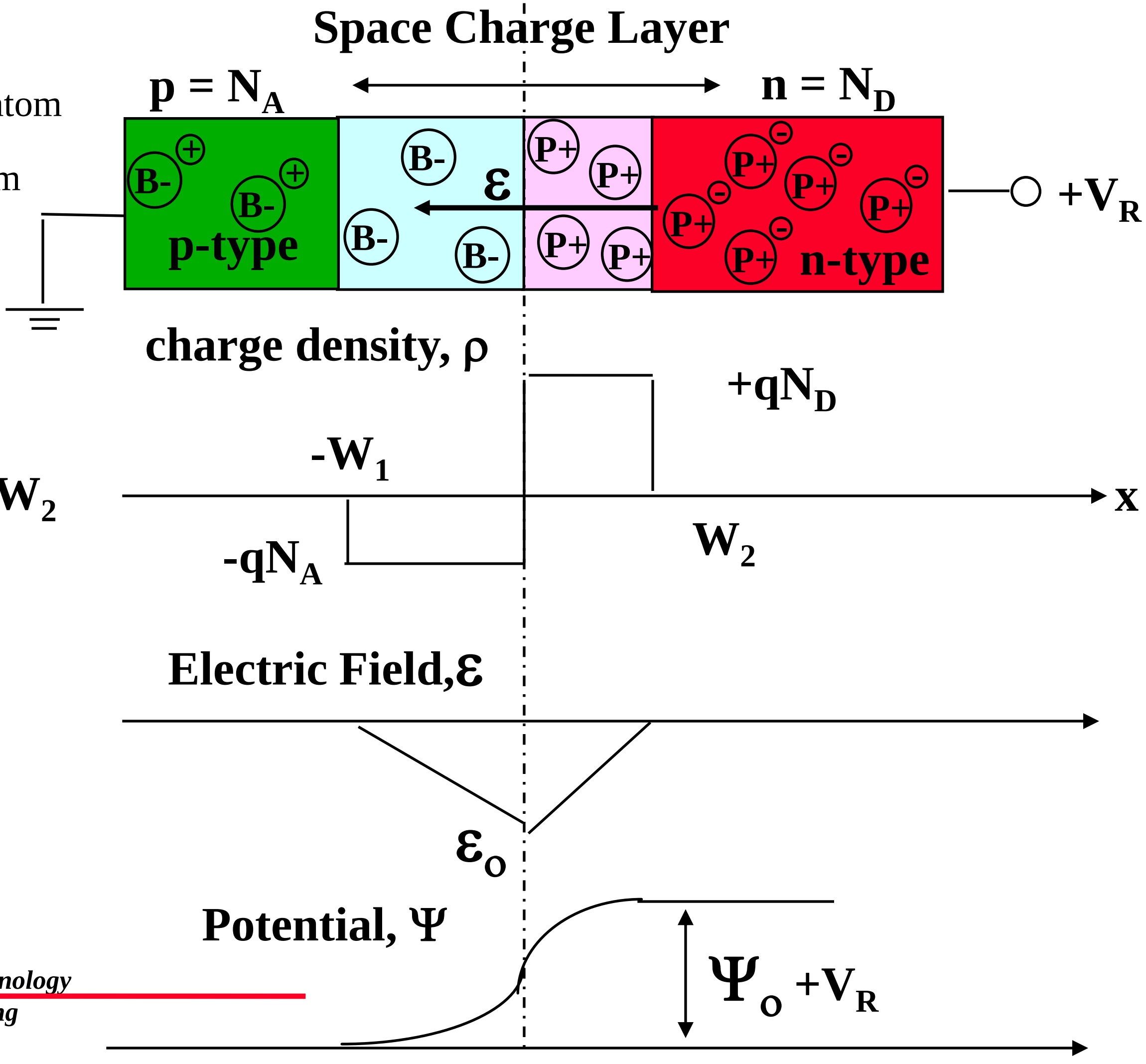
Channel Length, L, = distance between space charge layers, when Vd= what it is

Extracted Channel Length Parameters = anything that makes the fit good (not real)

UNIFORMLY DOPED PN JUNCTION

P+ ⊖	Phosphrous donor atom and electron
P+	Ionized Immobile Phosphrous donor atom
B-	Ionized Immobile Boron acceptor atom
B- ⊕	Boron acceptor atom and hole

$$qN_A W_1 = qN_D W_2$$



PROCESS CALCULATIONS

Built in Voltage: $\Psi_o = KT/q \ln (Na\ Nd/ni^2)$

Width of Space Charge Layer: $Wsc= [(2\varepsilon/q)(\Psi_o + V_R)(1/Na + 1/Nd)]^{1/2}$

$E_o = - [(2q/\varepsilon)(\Psi_o + V_R)(NaNd/(Na+Nd))]^{1/2}$

Example:

$\Psi_o = 0.026 \ln (1E17\ 1E17/1.45E10^2) = 0.82$

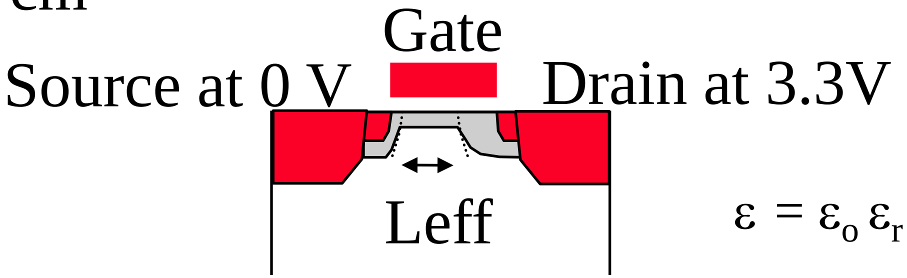
Wsc @ 0V=$[(2(11.7)(8.85E{-}14)/1.6E{-}19)(0.82)(1/1E17 + 1/1E17)]^{1/2}$

= 0.15 µm and 0.07 µm on each side of the junction

Wsc @ 3.3V=$[(2(11.7)(8.85E{-}14)/1.6E{-}19)(0.82+3.3)(1/1E17)]^{1/2}$

= 0.33 µm and 0.16 µm on each side of the junction

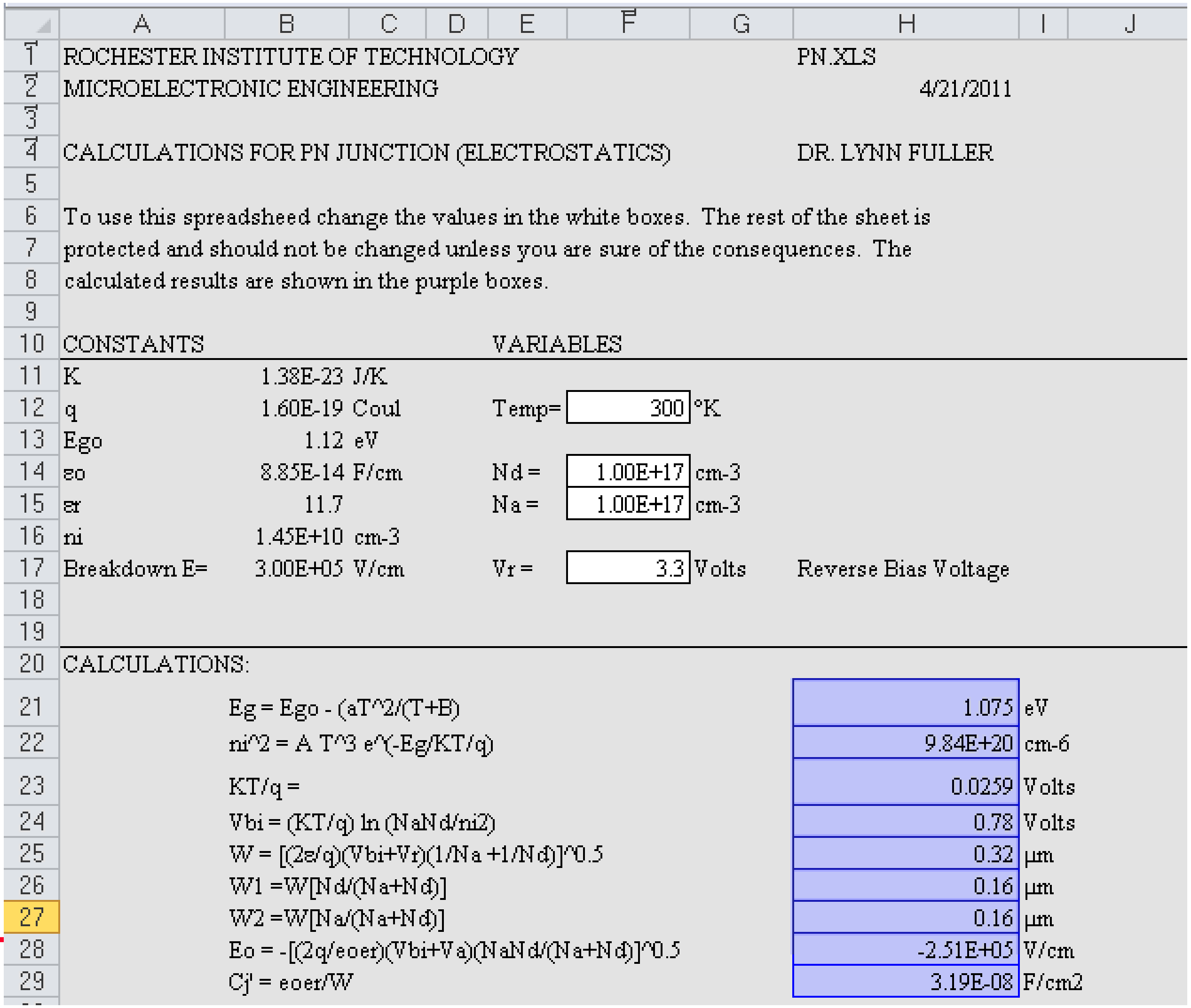
$E_o = - 2.5E5$ V/cm



$\varepsilon = \varepsilon_o\, \varepsilon_r = 8.85E{-}12\ (11.7)$ F/m

Leff = 0.5 - 0.07 - 0.16 = ~ 0.27 µm

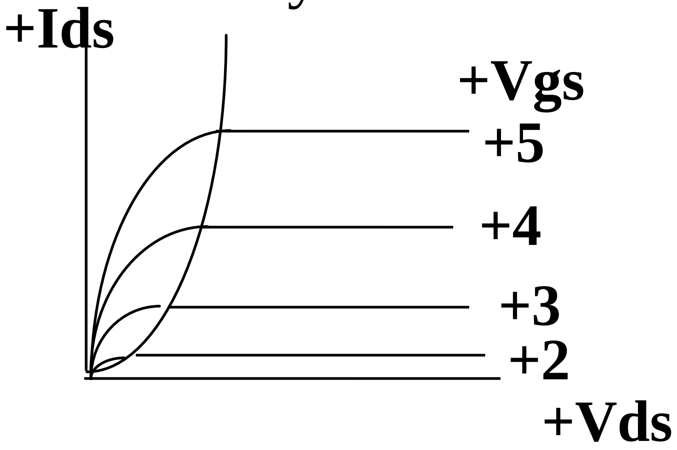
EXAMPLE CALCULATIONS

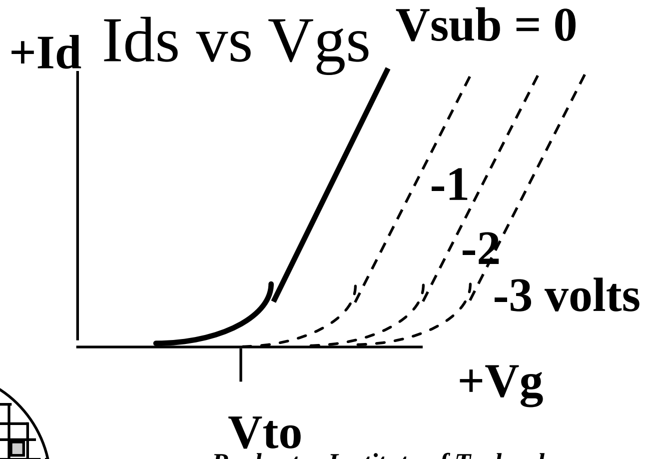


	A	B	C	D	E	F	G	H	I	J
1	ROCHESTER INSTITUTE OF TECHNOLOGY							PN.XLS		
2	MICROELECTRONIC ENGINEERING							4/21/2011		
3										
4	CALCULATIONS FOR PN JUNCTION (ELECTROSTATICS)							DR. LYNN FULLER		
5										
6	To use this spreadsheed change the values in the white boxes. The rest of the sheet is									
7	protected and should not be changed unless you are sure of the consequences. The									
8	calculated results are shown in the purple boxes.									
9										
10	CONSTANTS				VARIABLES					
11	K	1.38E-23	J/K							
12	q	1.60E-19	Coul		Temp=	300	°K			
13	Ego	1.12	eV							
14	εo	8.85E-14	F/cm		Nd =	1.00E+17	cm-3			
15	εr	11.7			Na =	1.00E+17	cm-3			
16	ni	1.45E+10	cm-3							
17	Breakdown E=	3.00E+05	V/cm		Vr =	3.3	Volts	Reverse Bias Voltage		
18										
19										
20	CALCULATIONS:									
21		Eg = Ego - (aT^2/(T+B)						1.075	eV	
22		ni^2 = A T^3 e^(-Eg/KT/q)						9.84E+20	cm-6	
23		KT/q =						0.0259	Volts	
24		Vbi = (KT/q) ln (NaNd/ni2)						0.78	Volts	
25		W = [(2ε/q)(Vbi+Vr)(1/Na +1/Nd)]^0.5						0.32	µm	
26		W1 =W[Nd/(Na+Nd)]						0.16	µm	
27		W2 =W[Na/(Na+Nd)]						0.16	µm	
28		Eo = -[(2q/eoer)(Vbi+Va)(NaNd/(Na+Nd)]^0.5						-2.51E+05	V/cm	
29		Cj' = eoer/W						3.19E-08	F/cm2	

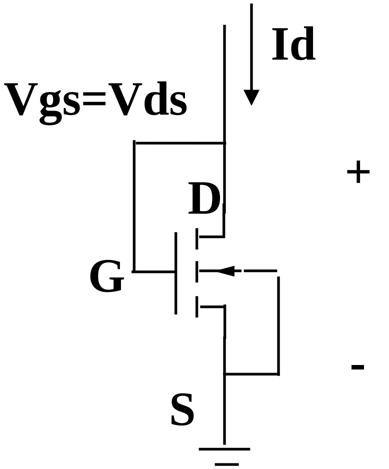
I-V CHARACTERISTICS

Family of Curves



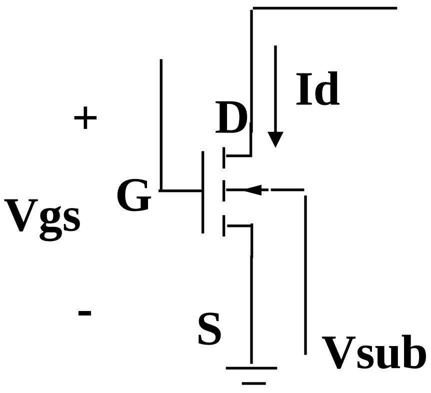


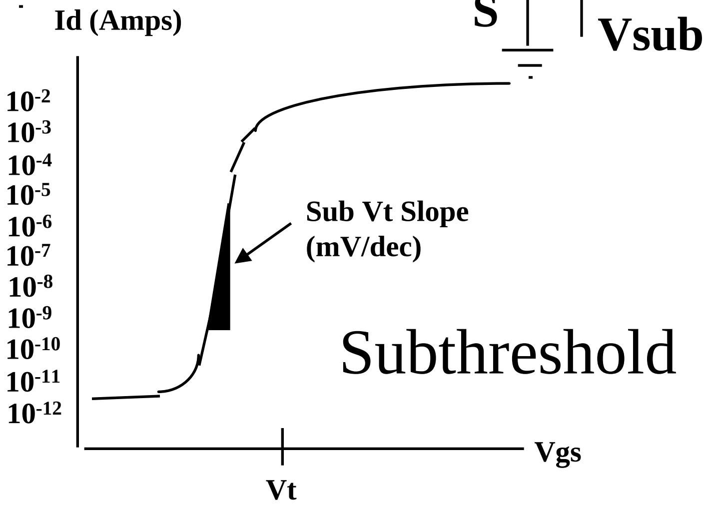
Saturation Region



Non Saturation Region

Vd = 0.1 Volt





Subthreshold

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LONG CHANNEL EQUATIONS FOR UO, VTO AND ID

Mobility:

$$\mu = \mu_{min} + \frac{(\mu_{max}-\mu_{min})}{\{1 + (N/N_{ref})^{\alpha}\}}$$

Parameter	Arsenic	Phosphorous	Boron
μ_{min}	52.2	68.5	44.9
μ_{max}	1417	1414	470.5
N_{ref}	9.68X10^16	9.20X10^16	2.23X10^17
α	0.680	0.711	0.719

Threshold Voltage:

+/-
nmos/pmos

$$VTO = \Phi ms - q\ NSS/Cox' +/- 2[\Phi F] +/- 2\ (q\varepsilon s\ NSUB\ [\Phi F])^{0.5}/Cox'$$

$[\Phi F] = (KT/q)\ \ln(NSUB/ni)$ where ni = 1.45E10 and KT/q = 0.026

Absolute value

Drain Current:

Non-Saturation

$$I_D = \frac{\mu W\ Cox'}{L}(Vg-Vt-V_d/2)V_d$$

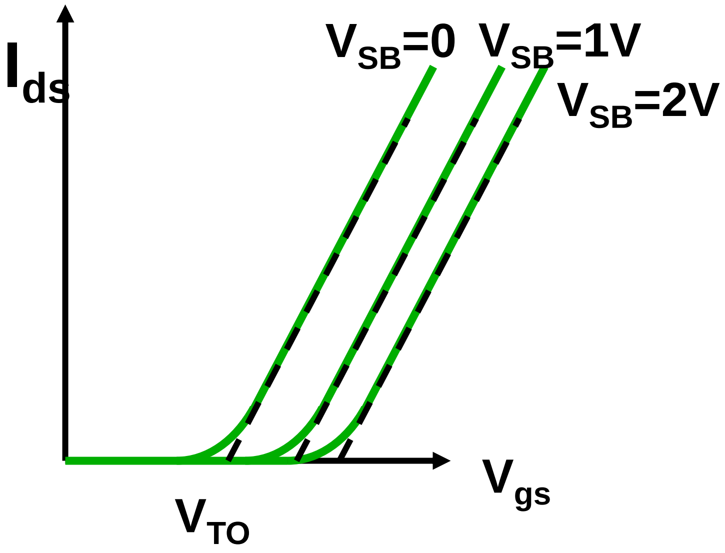
Saturation

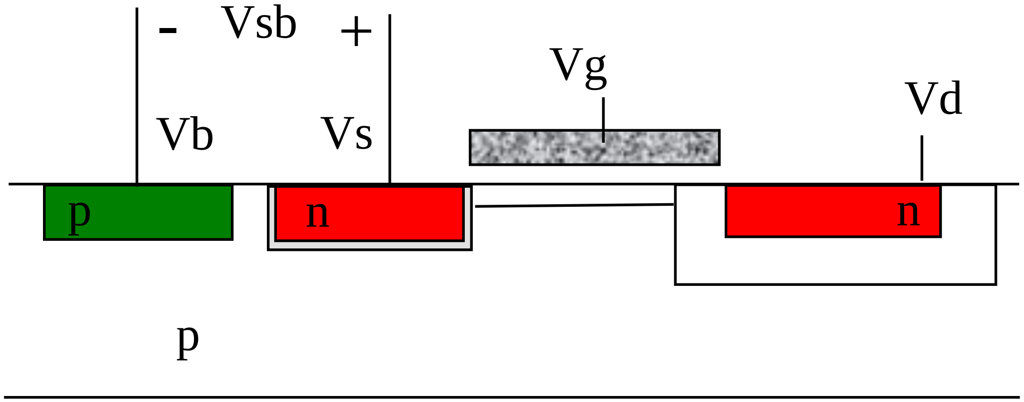
$$I_{Dsat} = \frac{\mu W\ Cox'}{2L}(Vg-Vt)^2$$

$Cox' = \varepsilon r \varepsilon o/TOX = 3.9\varepsilon o/TOX$

BACK-BIASING EFFECTS – GAMMA

Body Effect coefficient GAMMA or γ :





$$\boxed{\gamma = \frac{1}{C'_{ox}}\sqrt{2q\varepsilon_{Si}N_{sub}}}$$

$$V_T = \Phi_{MS} - \frac{Qss}{C'_{ox}} + 2\phi_F + \gamma\sqrt{2\phi_F + V_{SB}}$$

where εr si = 11.7 and εr ox = 3.9
εo = 8.8eE-14F/cm
q = 1.6E-19

LONG CHANNEL THRESHOLD VOLTAGE, VT

Flat-band Voltage $$V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C'_{ox}} - \frac{1}{C'_{ox}} \int_0^{Xox} \frac{X}{X_{ox}} \rho(x)\, dx$$

p-type substrate
(n-channel)

n-type substrate
(p-channel)

$Q_{ss} = q\, N_{ss}$

Bulk Potential : $\phi_p = -KT/q \;\; \ln (N_A / n_i)$ | $\phi_n = +KT/q \;\; \ln (N_D / n_i)$

Work Function: Difference $\phi_{M\,S} = \phi_M - (X + Eg/2q + [\phi_p])$ | $\phi_{M\,S} = \phi_M - (X + Eg/2q - [\phi_n])$

***Maximum Depletion Width**: $\sqrt{\frac{4\, \varepsilon s [\phi_p]}{qNa}}$ | $\sqrt{\frac{4\, \varepsilon s [\phi_n]}{qNd}}$

NMOS Threshold Voltage: $$VT = V_{FB} + 2\,[\phi_p] + \frac{1}{C'_{ox}} \sqrt{2\, \varepsilon s\, q\, Na\, (2[\phi_p])}$$

p-type substrate

PMOS Threshold Voltage: $$VT = V_{FB} - 2\,[\phi_n] - \frac{1}{C'_{ox}} \sqrt{2\, \varepsilon s\, q\, Nd\, (2[\phi_n])}$$

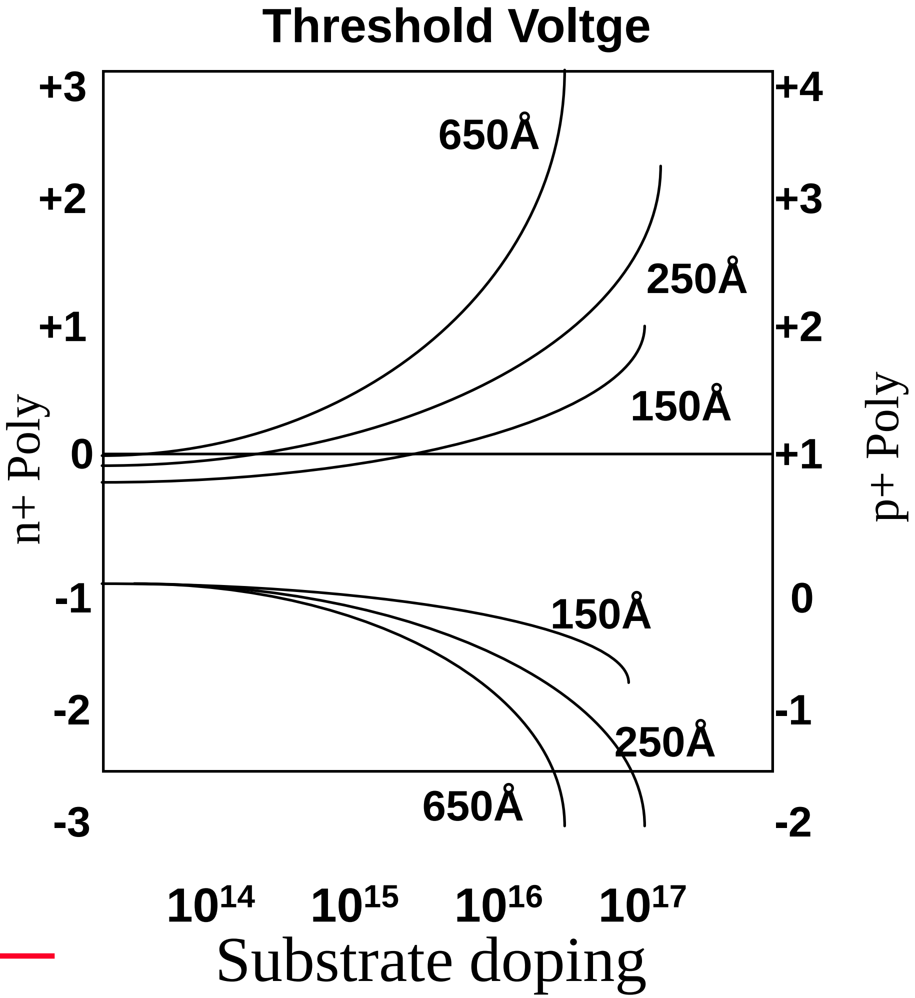
n-type substrate

MAJOR FACTORS AFFECTING VTO

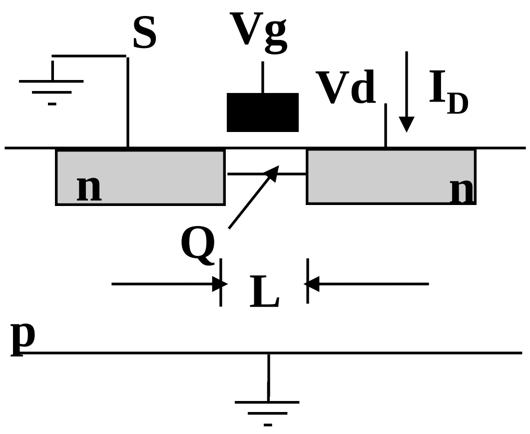
Gate work function, n+, p+, aluminum
Substrate doping, Nd or Na
Oxide thickness, Xox
Surface State Density, Nss or Qss

n+ poly gate left scale
p+ poly gate right scale
Nss= 0
Vbs = 0
implant dose = zero

Nss is never zero, typically adds 0.5 volts that is shifts both scales up 0.5 volts



APPROXIMATE EQUATION FOR ID IN NON-SATUATION REGION



$$I_D = \frac{\mu W\ Cox'}{L}(Vg-Vt-V_d/2)V_d$$

Cox' = Cox/Area = ɛoɛr/Xox

and Area = WL

and Xox is gate oxide thickness

Estimate I_D = charge in transit divided by the transit time

charge in transit Q = (Q source end + Q drain end) ave

Q = CV = [Cox(Vg-Vs-Vt)+Cox(Vg-Vd-Vt)]/2

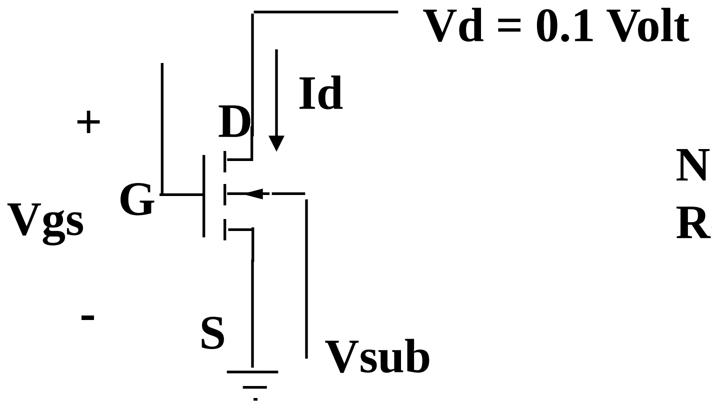
Q = Cox(Vg-Vt-Vd/2) = Cox'WL(Vg-Vt-Vd/2)

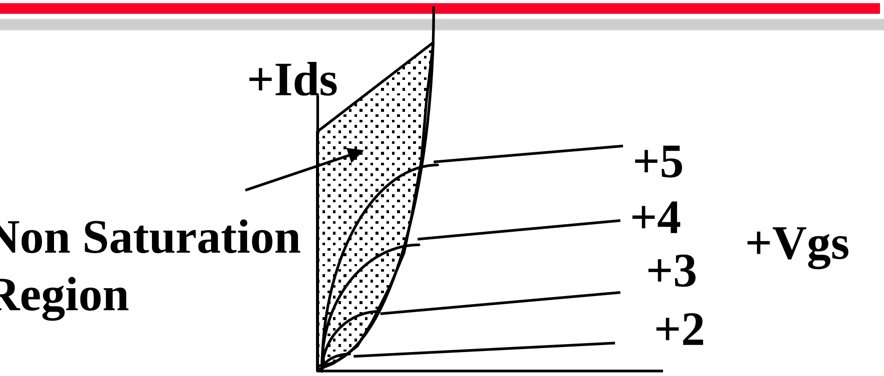
Transit time = distance/velocity = L/v = L/μE = L/μ(Vd/L) = L^2/μVd

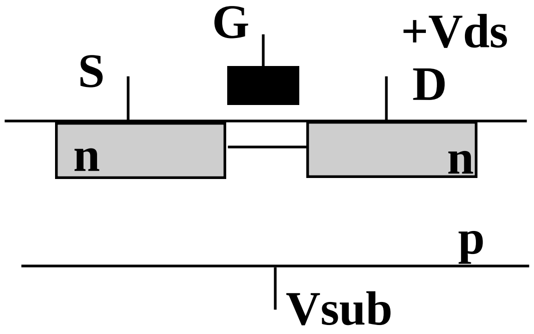
E is electric field

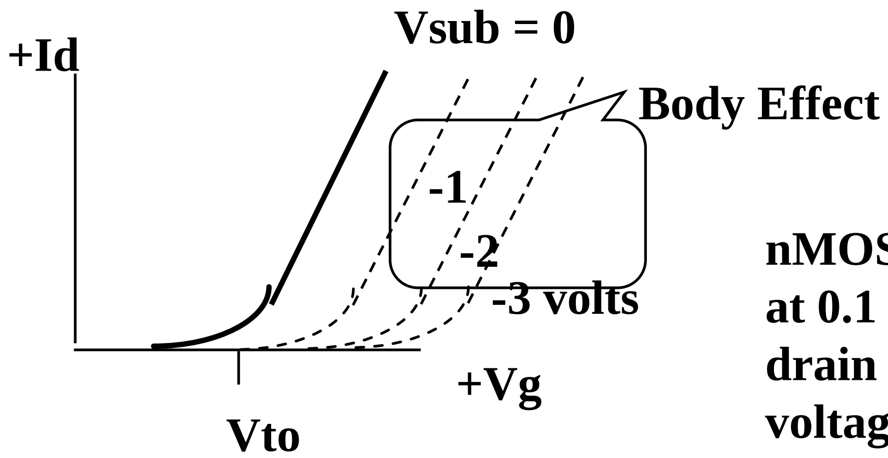
mobility

NON SATURATION REGION CHARACTERISTICS



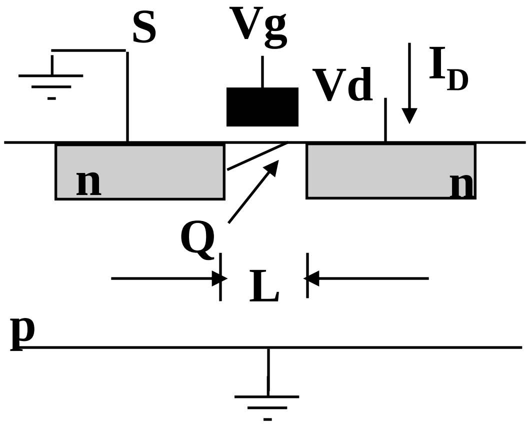






nMOSFET with Vt=1, since the Drain is at 0.1 volts and the source is at zero. Both drain and source will be on at gate voltages greater than 1.1 volt. the transistor will be in the non saturation region.

APPROXIMATE EQUATION FOR ID IN SATURATION REGION

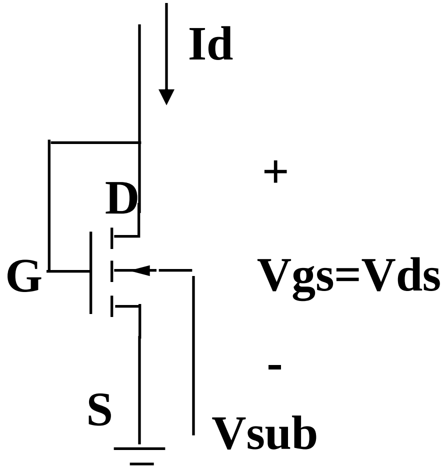


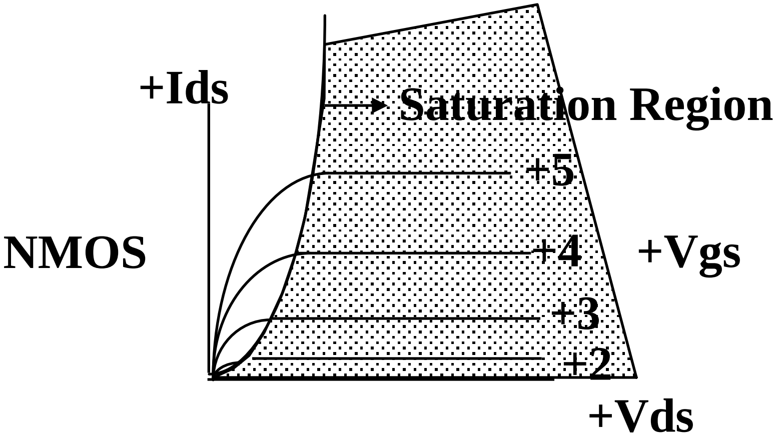
$$\boxed{I_{Dsat} = \frac{\mu W\ Cox'}{2L}(Vg-Vt)^2}$$

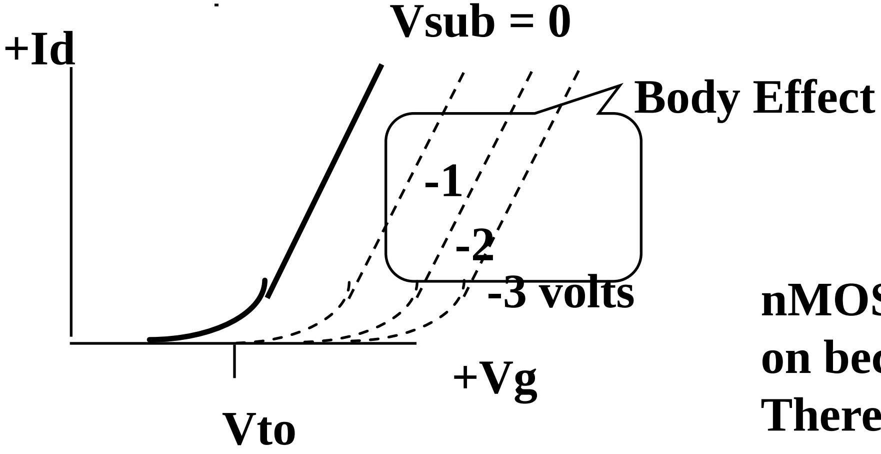
If Vd increases eventually Vg-Vd will be less than Vt and further increases in Vd will not cause increases in ID (because the additional voltage will be across the gap region at the drain end where it can not reduce the transit time)

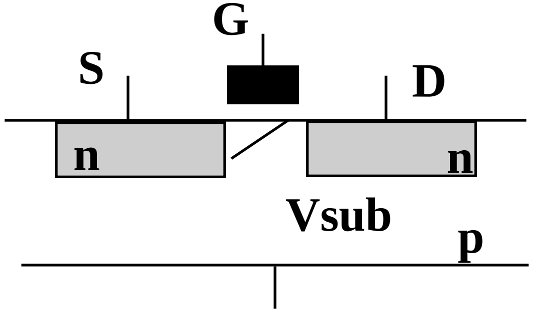
So substitute Vg-Vd = Vt or Vd = Vg-Vt into equation for non saturation region to get equation for saturation region.

SATURATION REGION CHARACTERISTICS



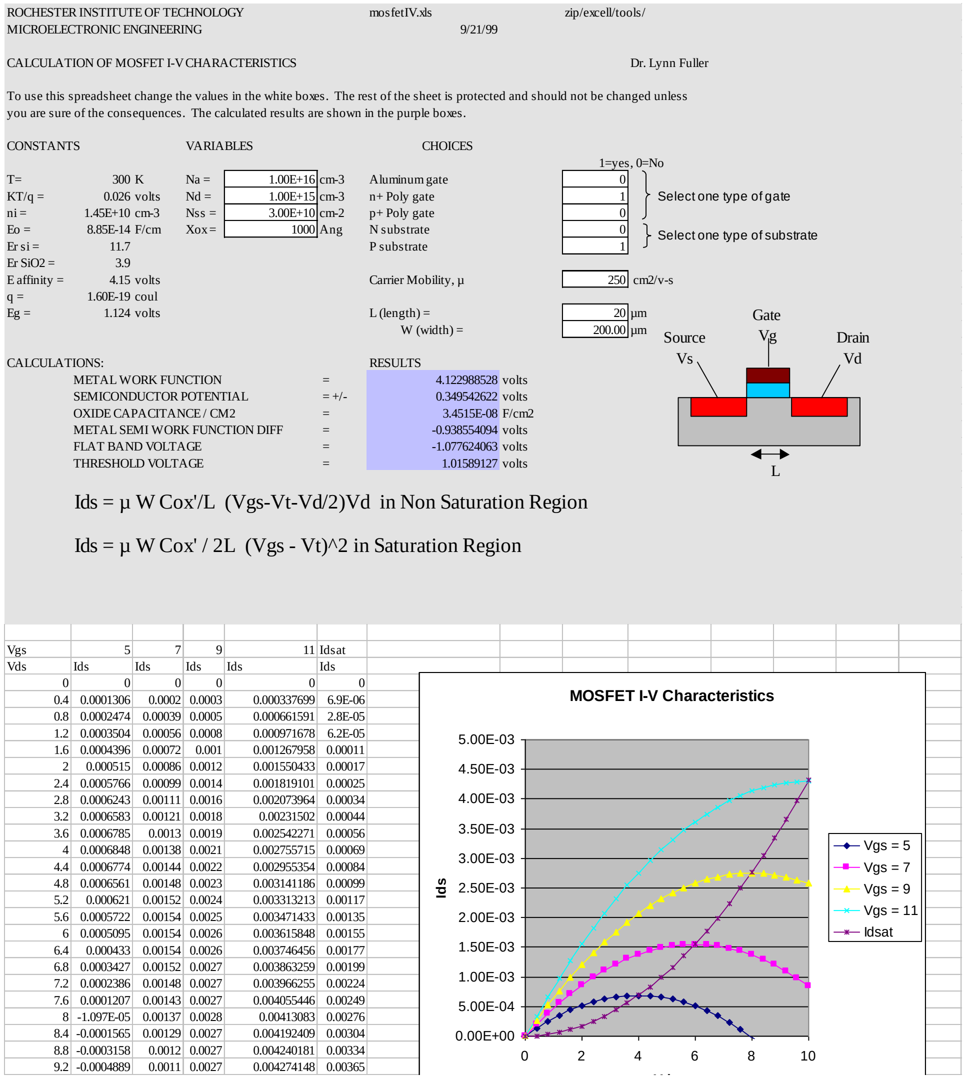






nMOSFET with Vt=1, Drain end is never on because Voltage Gate to Drain is Zero. Therefore this transistor is always in Saturation Region if the gate voltage is above the threshold voltage.

CALCULATOR FOR IDEAL I-V CHARACTERISTICS



ROCHESTER INSTITUTE OF TECHNOLOGY   mosfetIV.xls   zip/excell/tools/
MICROELECTRONIC ENGINEERING   9/21/99

CALCULATION OF MOSFET I-V CHARACTERISTICS   Dr. Lynn Fuller

To use this spreadsheet change the values in the white boxes. The rest of the sheet is protected and should not be changed unless you are sure of the consequences. The calculated results are shown in the purple boxes.

CONSTANTS

T= 300 K
KT/q = 0.026 volts
ni = 1.45E+10 cm-3
Eo = 8.85E-14 F/cm
Er si = 11.7
Er SiO2 = 3.9
E affinity = 4.15 volts
q = 1.60E-19 coul
Eg = 1.124 volts

VARIABLES

Na = 1.00E+16 cm-3
Nd = 1.00E+15 cm-3
Nss = 3.00E+10 cm-2
Xox = 1000 Ang

CHOICES

1=yes, 0=No

Aluminum gate 0
n+ Poly gate 1
p+ Poly gate 0
Select one type of gate

N substrate 0
P substrate 1
Select one type of substrate

Carrier Mobility, µ 250 cm2/v-s

L (length) = 20 µm
W (width) = 200.00 µm

CALCULATIONS:

		RESULTS	
METAL WORK FUNCTION	=	4.122988528	volts
SEMICONDUCTOR POTENTIAL	= +/-	0.349542622	volts
OXIDE CAPACITANCE / CM2	=	3.4515E-08	F/cm2
METAL SEMI WORK FUNCTION DIFF	=	-0.938554094	volts
FLAT BAND VOLTAGE	=	-1.077624063	volts
THRESHOLD VOLTAGE	=	1.01589127	volts

Ids = µ W Cox'/L (Vgs-Vt-Vd/2)Vd in Non Saturation Region

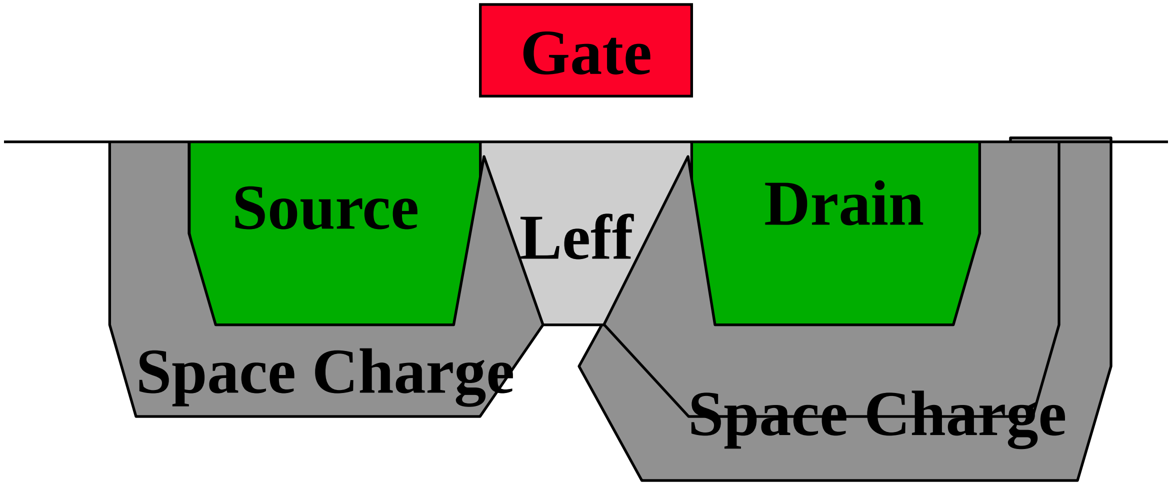
Ids = µ W Cox' / 2L (Vgs - Vt)^2 in Saturation Region

Vgs	5	7	9	11	Idsat
Vds	Ids	Ids	Ids	Ids	Ids
0	0	0	0	0	0
0.4	0.0001306	0.0002	0.0003	0.000337699	6.9E-06
0.8	0.0002474	0.00039	0.0005	0.000661591	2.8E-05
1.2	0.0003504	0.00056	0.0008	0.000971678	6.2E-05
1.6	0.0004396	0.00072	0.001	0.001267958	0.00011
2	0.000515	0.00086	0.0012	0.001550433	0.00017
2.4	0.0005766	0.00099	0.0014	0.001819101	0.00025
2.8	0.0006243	0.00111	0.0016	0.002073964	0.00034
3.2	0.0006583	0.00121	0.0018	0.00231502	0.00044
3.6	0.0006785	0.0013	0.0019	0.002542271	0.00056
4	0.0006848	0.00138	0.0021	0.002755715	0.00069
4.4	0.0006774	0.00144	0.0022	0.002955354	0.00084
4.8	0.0006561	0.00148	0.0023	0.003141186	0.00099
5.2	0.000621	0.00152	0.0024	0.003313213	0.00117
5.6	0.0005722	0.00154	0.0025	0.003471433	0.00135
6	0.0005095	0.00154	0.0026	0.003615848	0.00155
6.4	0.000433	0.00154	0.0026	0.003746456	0.00177
6.8	0.0003427	0.00152	0.0027	0.003863259	0.00199
7.2	0.0002386	0.00148	0.0027	0.003966255	0.00224
7.6	0.0001207	0.00143	0.0027	0.004055446	0.00249
8	-1.097E-05	0.00137	0.0028	0.00413083	0.00276
8.4	-0.0001565	0.00129	0.0027	0.004192409	0.00304
8.8	-0.0003158	0.0012	0.0027	0.004240181	0.00334
9.2	-0.0004889	0.0011	0.0027	0.004274148	0.00365

THE SHORT CHANNEL MOSFET

Sort channel MOSFET is defined as devices with width and length short enough such that the edge effects can not be neglected.

Channel length Leff is comparable to the depletion widths associated with the drain and source.



TERADA-MUTA METHOD FOR EXTRACTING Leff and Rds

Terada-Muta Method for Leff and Rds

In the linear region (V_D is small):

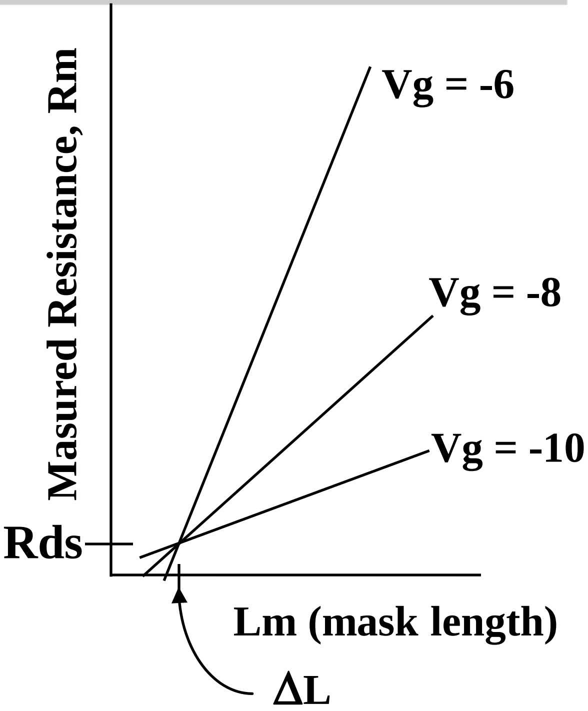
$$I_D = \underbrace{\frac{\mu W\ Cox'}{Leff}\left(Vgs-Vt-\overset{0}{V_d/2}\right)}_{1/Rm}\ V_D$$

$$\boxed{I_D = 1/R_m\ V_D}$$

Leff = Lm - ΔL

where ΔL is correction due to processing

Lm is the mask length



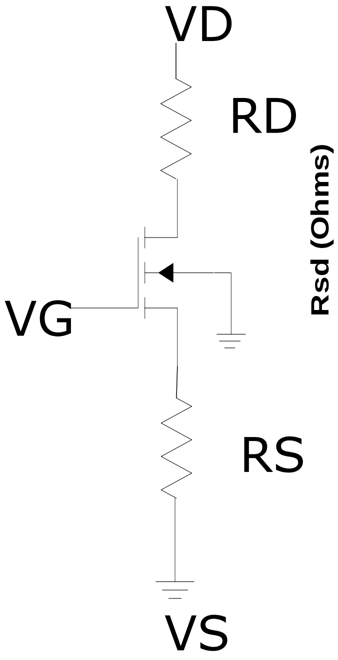
Rm = V_D/I_D = measured resistance

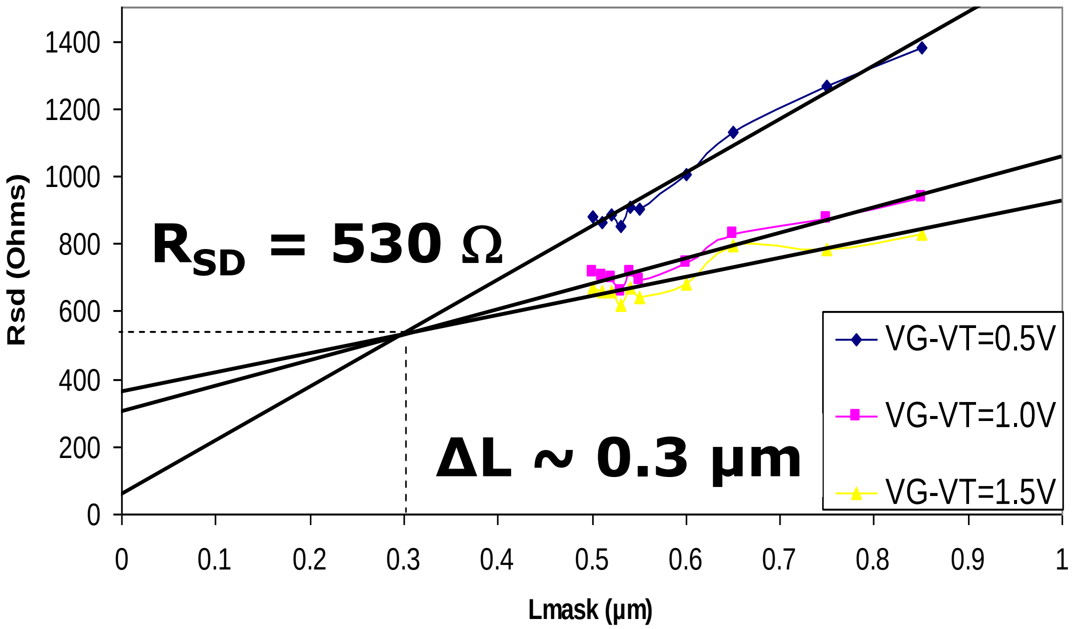
= Rds + (Lm - ΔL)/ μW Cox' (Vgs-Vt)

so measure Rm for different channel length transistors and plot Rm vs Lm where Rm = intersect find value for ΔL and Rds

Then Leff can be calculated for each different length transistor from Leff = Lm - ΔL

TERADA-MUTA METHOD FOR EXTRACTING Leff and Rds





L_{eff} & R_{SD} extraction for NMOS Transistors

$L_{eff} = L_{mask} - \Delta L$
L_{eff} = 0.5 µm – 0.3 µm
L_{eff} = 0.2 µm

Linear Region:
V_D= 0.1V
$V_G-V_T >> I_DR_{SD}$
At low I_D, V_{RSD} small

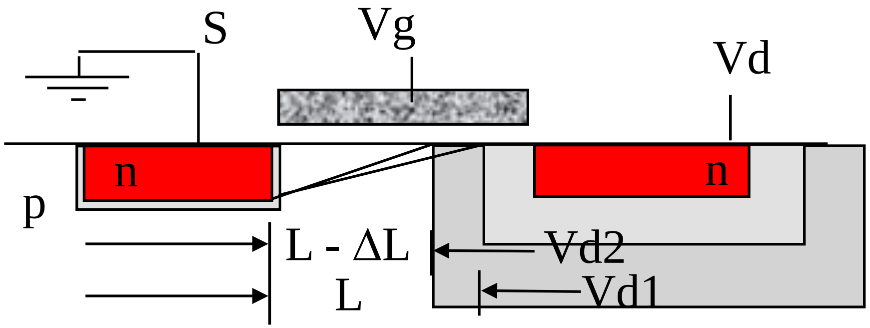
$$Rm = \frac{Vd}{Id} = R_{SD} + \frac{(L_{mask} - \Delta L)}{\mu Cox'W(V_{GS}-V_t)}$$

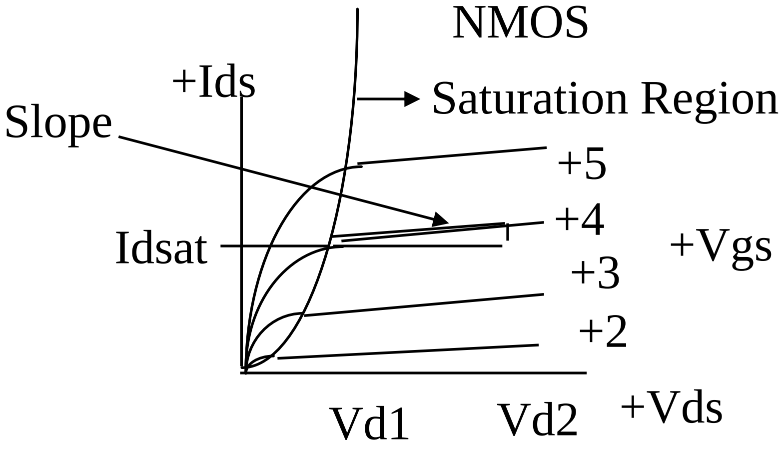
Plot R_m vs. L_{mask} for different $(V_{GS}-V_t)$

CHANNEL LENGTH MODULATION - LAMBDA

Channel Length Modulation Parameter λ

λ = Slope/ Idsat





$$I_{Dsat} = \frac{\mu W\ Cox'}{2L}(Vg-Vt)^2\,(1+\lambda Vds)$$

NMOS Transistor
DC Model, λ is the channel length modulation parameter. Typical value might be 0.02

Saturation Region

Note: λ is is different for each different channel length, L.

$$I_D = \frac{\mu W\ Cox'}{L}(Vg-Vt-V_d/2)V_d\,(1+\lambda Vds)$$

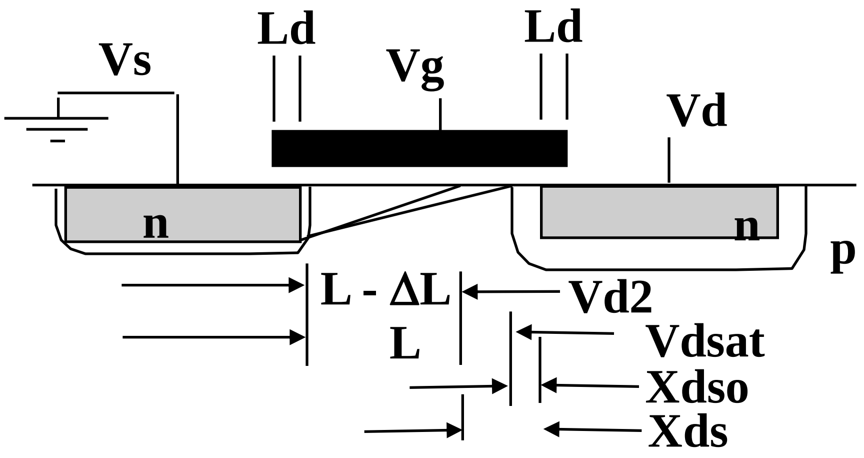
Non Saturation Region

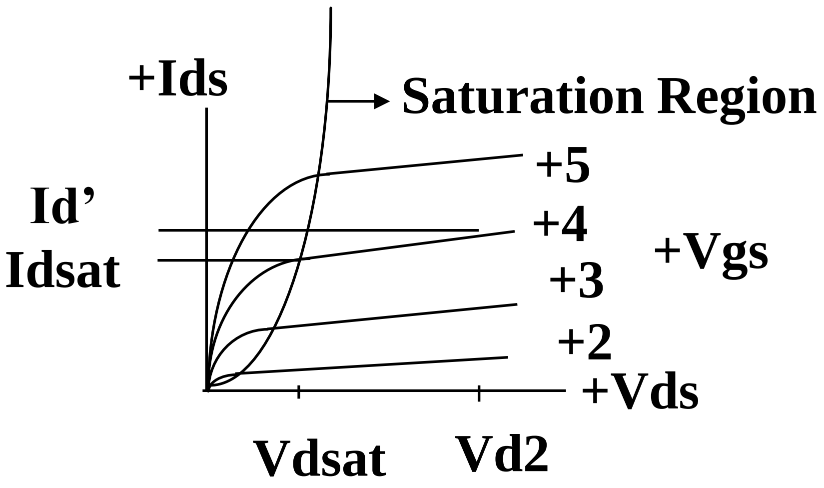
2ND GENERATION EQUATIONS FOR CHANNEL LENGTH MODULATION

KAPPA is channel length modulation parameter.

KAPPA is calculated = [(qNsub/(2εoεr))((1-Idsat/Id')(L-2LD-Xdso-Xds))^2)/(Vd2-Vdsat)]^0.5

Measure Id’ at large Vds, and Idsat at Vdsat,
Kappa has units of 1/V typical value ~0.1



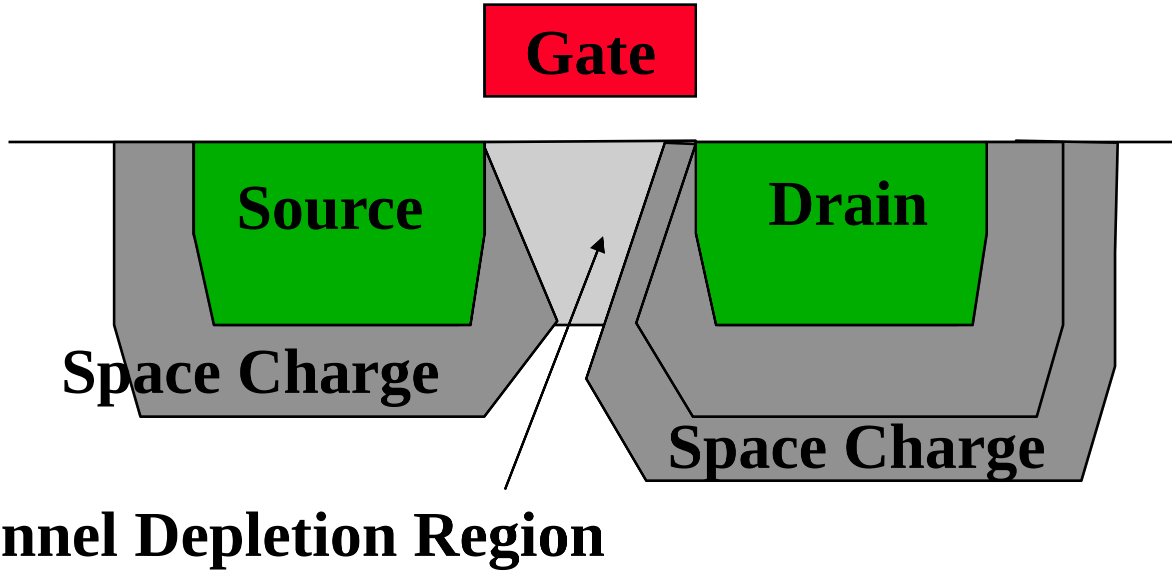


Note: Kappa is not different for each different channel length, L

SHORT CHANNEL VT ROLL OFF AND DIBL

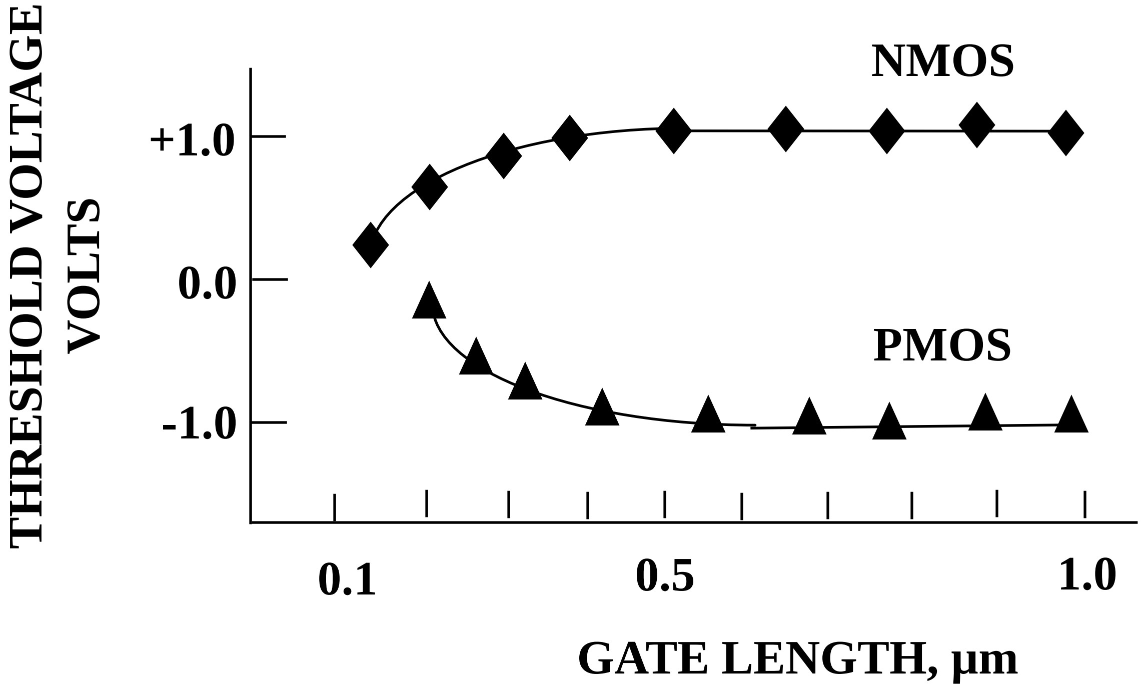
As the channel length decreases the **channel depletion region** becomes smaller and the VT needed to turn on the channel appears to decrease.

A similar effect occurs for increasing V_{DS} which causes an increase in the drain space charge layer. Called **Drain Induced Barrier Lowering or DIBL**



THRESHOLD VOLTAGE ROLL OFF

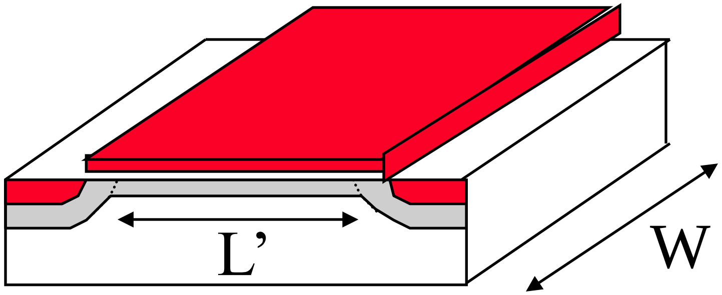
A Test Chip is used that includes nMOS and pMOS transistors of various lengths from 0.1 µm to 5.0 µm and the threshold voltage is plotted versus channel length. The threshold voltage needs to be high enough so that when the input is zero or +Vsupply the transistor current is many decades lower than when it is on. Vt and sub-Vt slope interact.

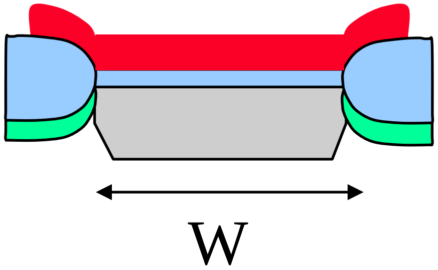


NARROW GATE WIDTH EFFECTS

Fringing field causes channel depletion region to extend beyond the gate in the width direction Thus additional gate charge is required causing an apparent increase in threshold voltage. In wide channel devices this can be neglected but as the channel becomes smaller it is more important

In NMOS devices encroachment of the channel stop impurity atoms under the gate edges causing the edges to be heavier doped requiring more charge on the gate to turn on the entire channel width. In PMOSFETs the phosphorous pile up at the surface under the field region causes a similar apparent increase in doping at the edges of the channel width

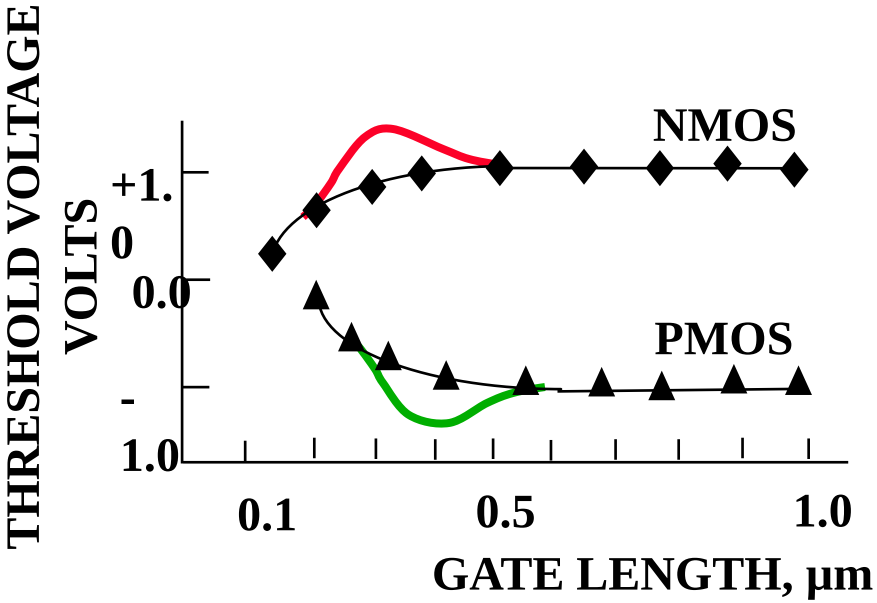




REVERSE THRESHOLD VOLTAGE ROLLOFF

Vt initially increases with decrease in channel length then decreases. This is caused by various effects that result in lateral dopant nonuniformity in the channel.

Example: Oxidation Enhanced Diffusion or enhanced diffusion due to implant damage causing the dopant concentration to be higher in the channel near the drain and source edges of the poly gate.



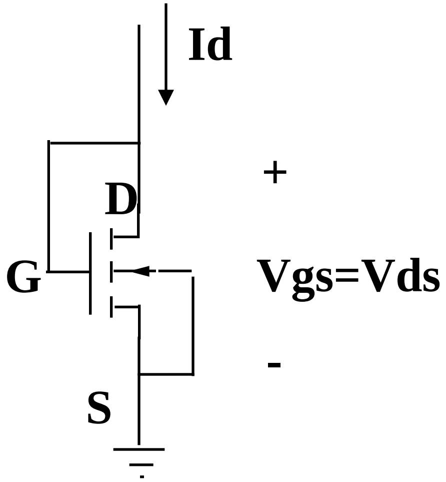
2ND GENERATION EQUATIONS FOR NARROW WIDTH

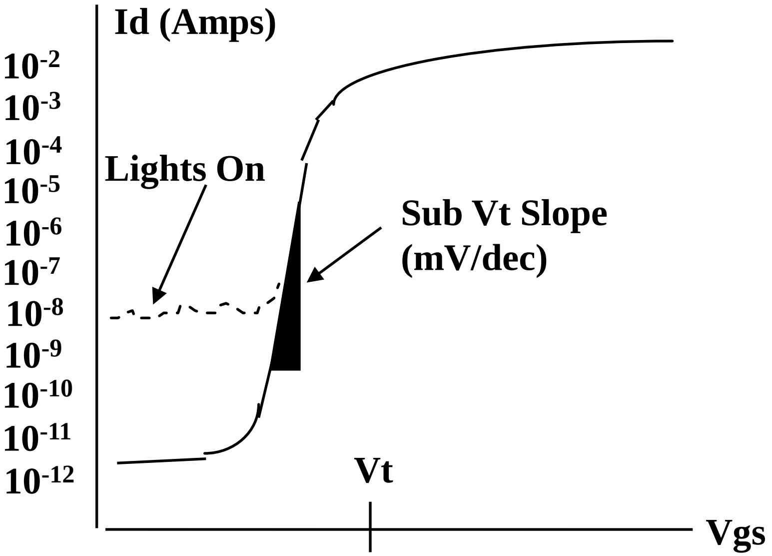
DELTA is introduced to model narrow channel effects on threshold voltage. The parameter WD (channel width reduction from drawn value) is used to calculate the effective channel width. DELTA is used in the calculation of threshold voltage.

$$\boxed{\mathrm{DELTA} = \frac{q\ \mathrm{NSUB}\ \mathrm{Xds}^2}{\varepsilon\mathrm{o}\ \varepsilon\mathrm{si}\ 2\ \mathrm{PHI}}}$$

Note: a dimensionless number typically ~3

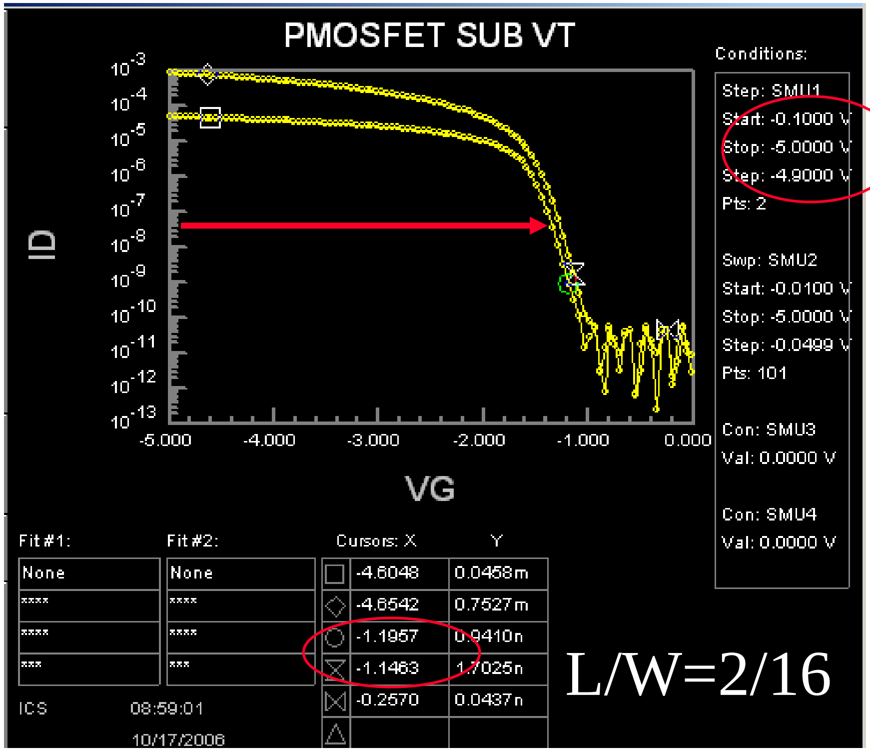
SUBTHRESHOLD CHARACTERISTIC





The subthreshold characteristics are important in VLSI circuits because when the transistors are off they should not carry much current since there are so many transistors. (subthreshold slope typical value about 100 mV/decade, theoretical maximum of 63mV/dec at room T). Thinner gate oxide makes subthreshold slope larger. Surface channel has larger slope than buried channel. Larger slope is better.

DRAIN INDUCED BARRIER LOWERING



Conditions:

Step: SMU1
Start: -0.1000 V
Stop: -5.0000 V
Step: -4.9000 V
Pts: 2

Swp: SMU2
Start: -0.0100 V
Stop: -5.0000 V
Step: -0.0499 V
Pts: 101

Con: SMU3
Val: 0.0000 V

Con: SMU4
Val: 0.0000 V

Fit #1:	Fit #2:	Cursors:	X	Y
None	None	□	-4.6048	0.0458m
****	****	◇	-4.6542	0.7527m
****	****	○	-1.1957	0.9410n
***	***	⧗	-1.1463	1.7025n
		⋈	-0.2570	0.0437n
		△		

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L/W=2/16

DIBL = change in VG /change in VD
at ID=1E-9 amps/µm
or 1.6E-8 amps for this
size transistor

= ~ (1.1957-1.1463)/(5-0.1)
= ~ 10mV/V

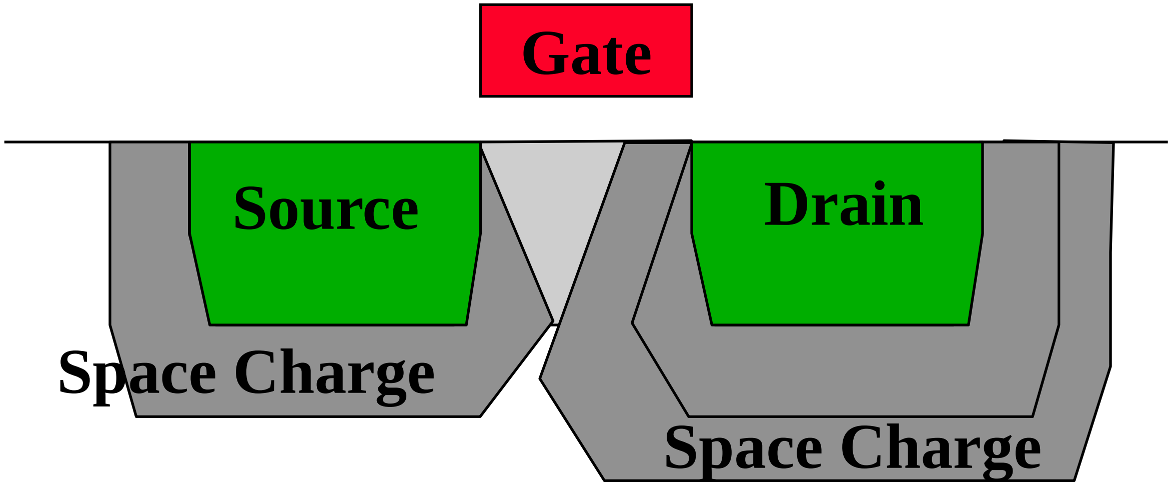
2ND GENERATION MODEL EUATIONS FOR THRESHOLD VOLTAGE

The parameter ETA is used to describe DIBL (Drain Induced Barrier Lowering) resulting in a modification to the LEVEL 1 equation for threshold voltage.

$$\mathbf{VTO = \Phi ms - \phi_{ETA} - q\ NSS/Cox' - 2\ \Phi F - 2\ (q\varepsilon s\ NSUB\ \Phi F)^{0.5}/Cox'}$$

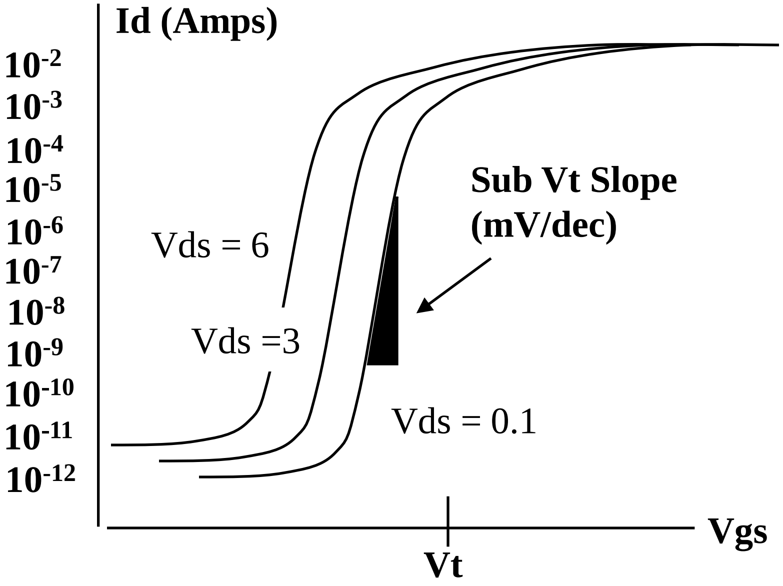
$$\phi_{ETA} = \frac{(-\ 8.14E\text{-}22)*ETA}{Cox'Leff^{\ 3}}\ Vds$$

PUNCHTHROUGH

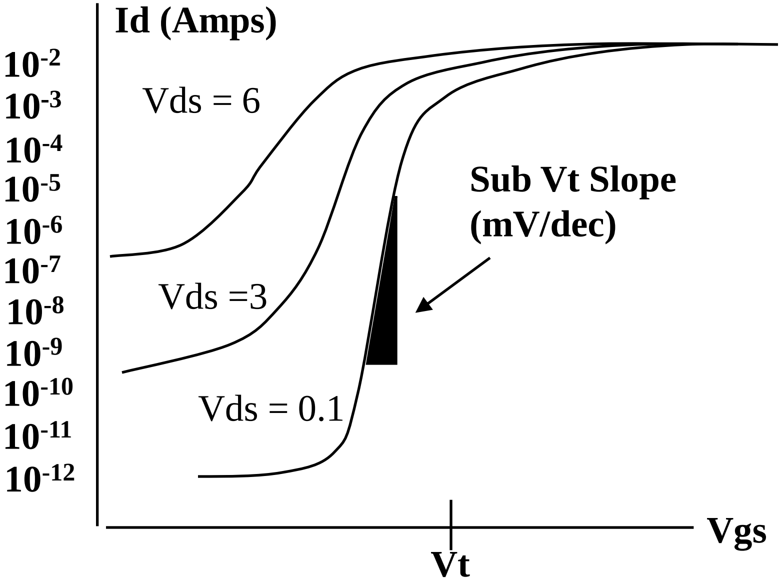


As the voltage on the drain increases the space charge associated with the drain pn junction increases. Current flow through the transistor increases as the source and drain space charge layers approach each other. This is called **punchthrough**. The first indication is an increase in the sub threshold current and a decrease in the the subthreshold slope.

PUNCHTHROUGH



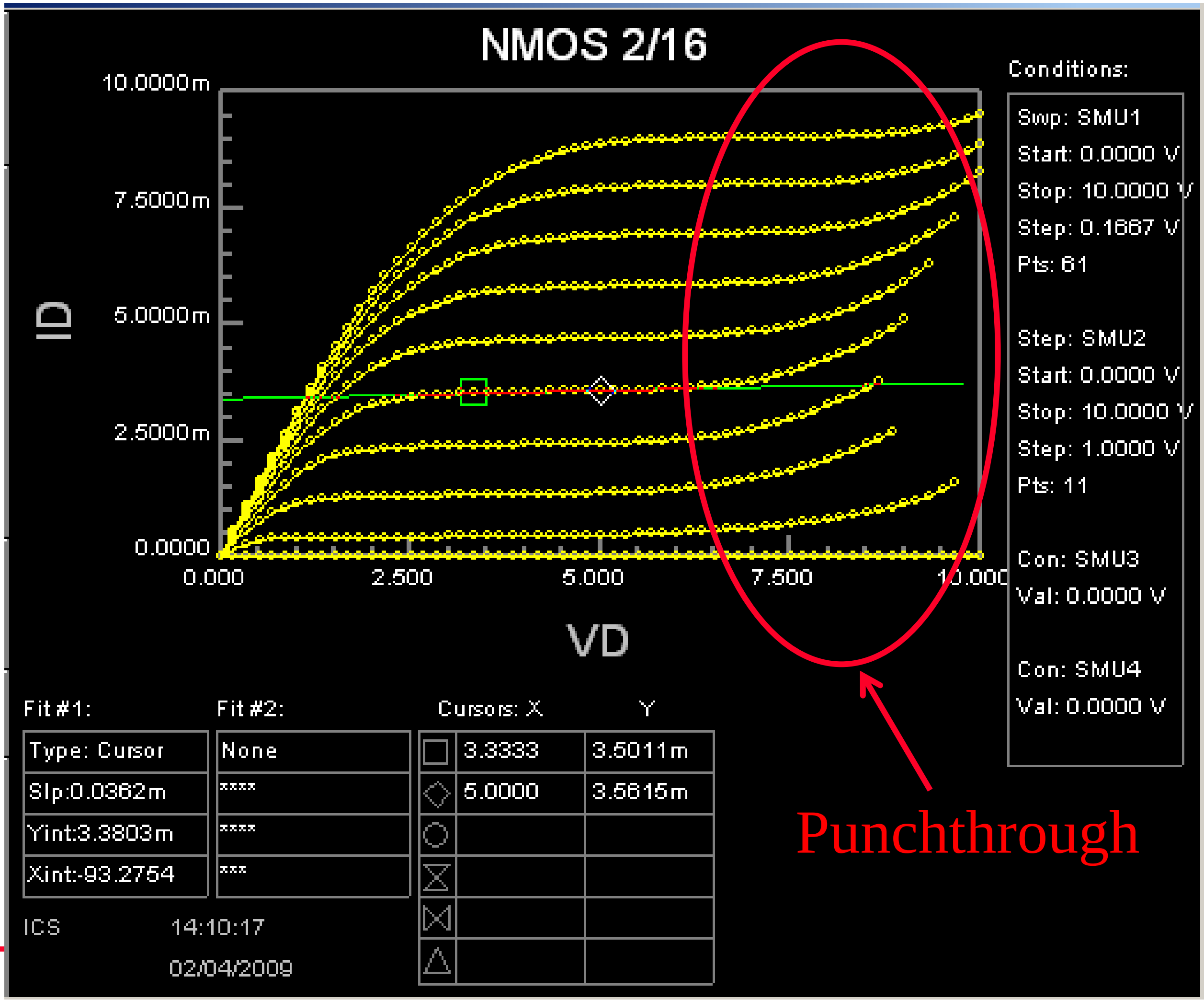
Long channel behavior



Short channel behavior

Punchthrough

MEASURED ID-VDS FAMILY



Conditions:

Swp: SMU1
Start: 0.0000 V
Stop: 10.0000 V
Step: 0.1667 V
Pts: 61

Step: SMU2
Start: 0.0000 V
Stop: 10.0000 V
Step: 1.0000 V
Pts: 11

Con: SMU3
Val: 0.0000 V

Con: SMU4
Val: 0.0000 V

Fit #1:	Fit #2:
Type: Cursor	None
Slp:0.0362m	****
Yint:3.3803m	****
Xint:-93.2754	***

Cursors:	X	Y
□	3.3333	3.5011m
◇	5.0000	3.5615m
○		
⧖		
⋈		
△		

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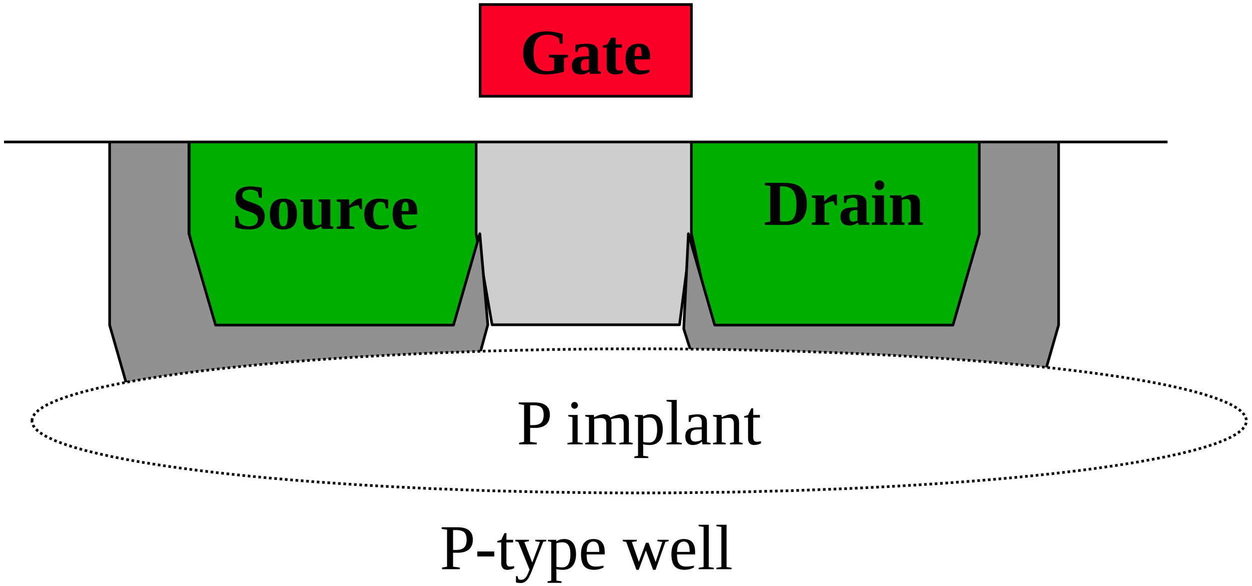
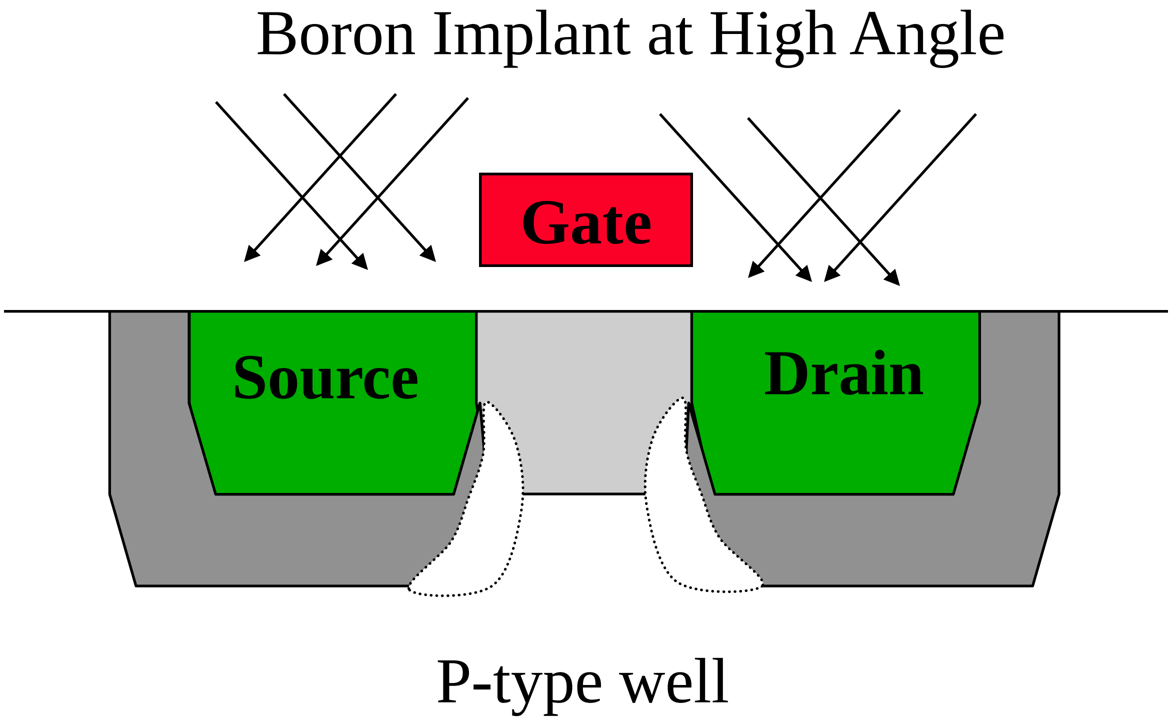
PUNCHTHROUGH IMPLANT

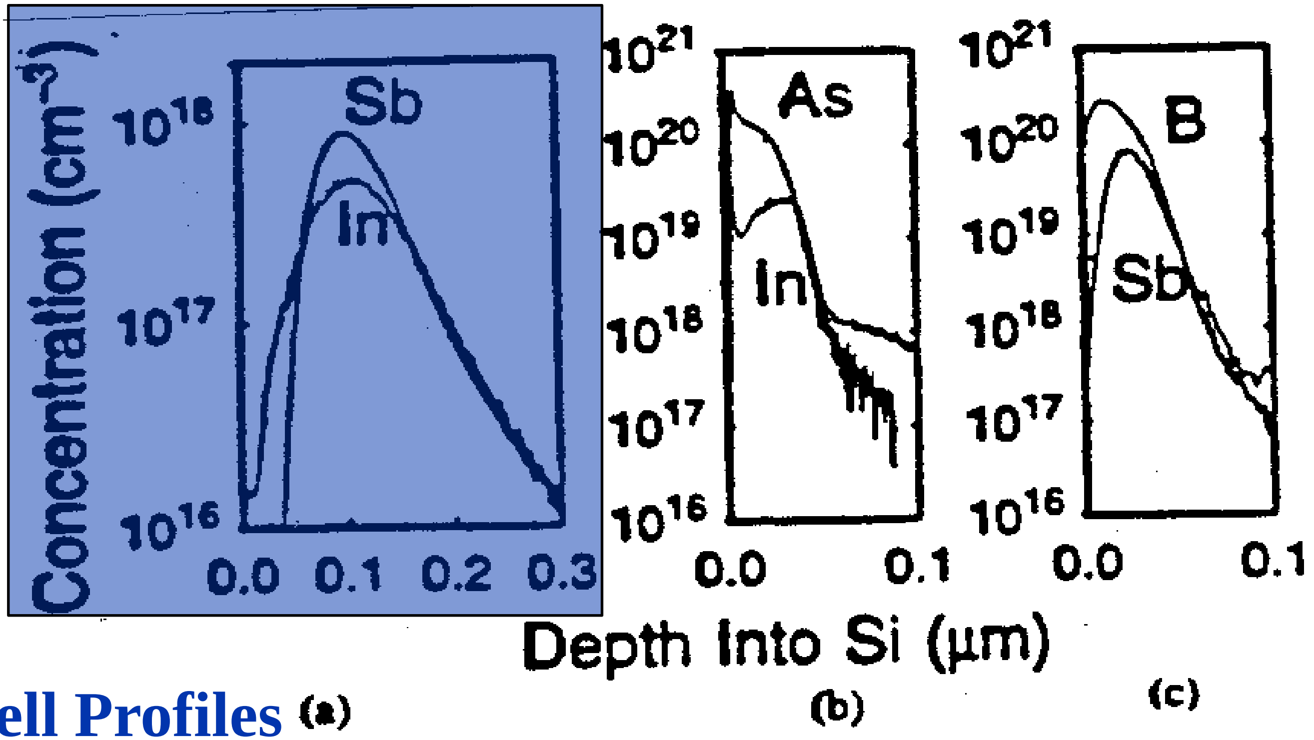


Punch through implant increases the well doping below the drain and source depth making the space charge layer smaller.

PUNCHTHROUGH HALO IMPLANT



RETROGRADE WELL TO REDUCE PUNCHTHROUGH



Well Profiles

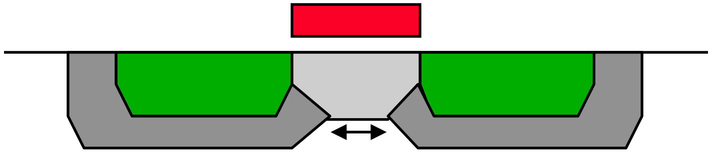
Fig. 1. SIMS measurement of the channel implant for nMOS and pMOS (a), and the source–drain extension/halo profiles for nMOS (b) and pMOS (c).

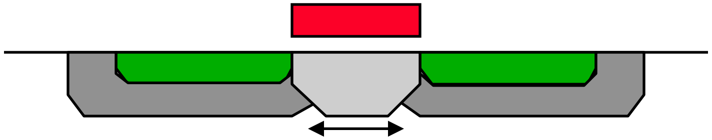
WHY THE D/S NEEDS TO BE SHALLOW

Sketch the three space charge layers

- The Channel Space Charge
- The Drain Space Charge
- The Source Space Charge

Look at Punchthrough





Punchthrough will occur at lower drain voltages in the device with deeper D/S

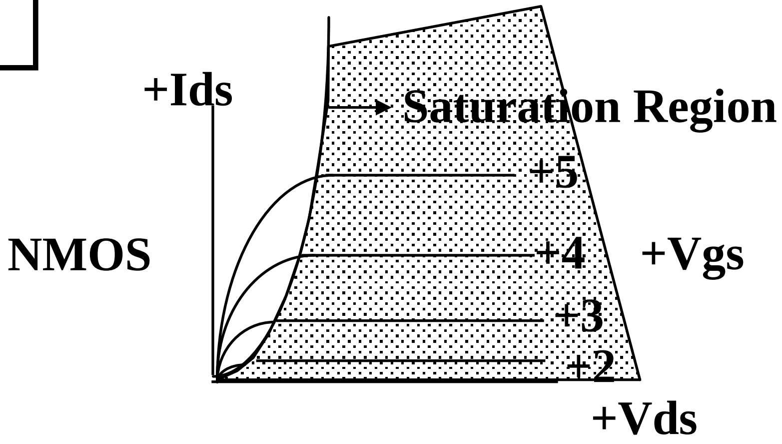
CURRENT DRIVE - MOBILITY - μ

$$I_D = \frac{\mu W\,Cox'}{L}(Vg-Vt-V_d/2)V_d$$

Non Saturation Region

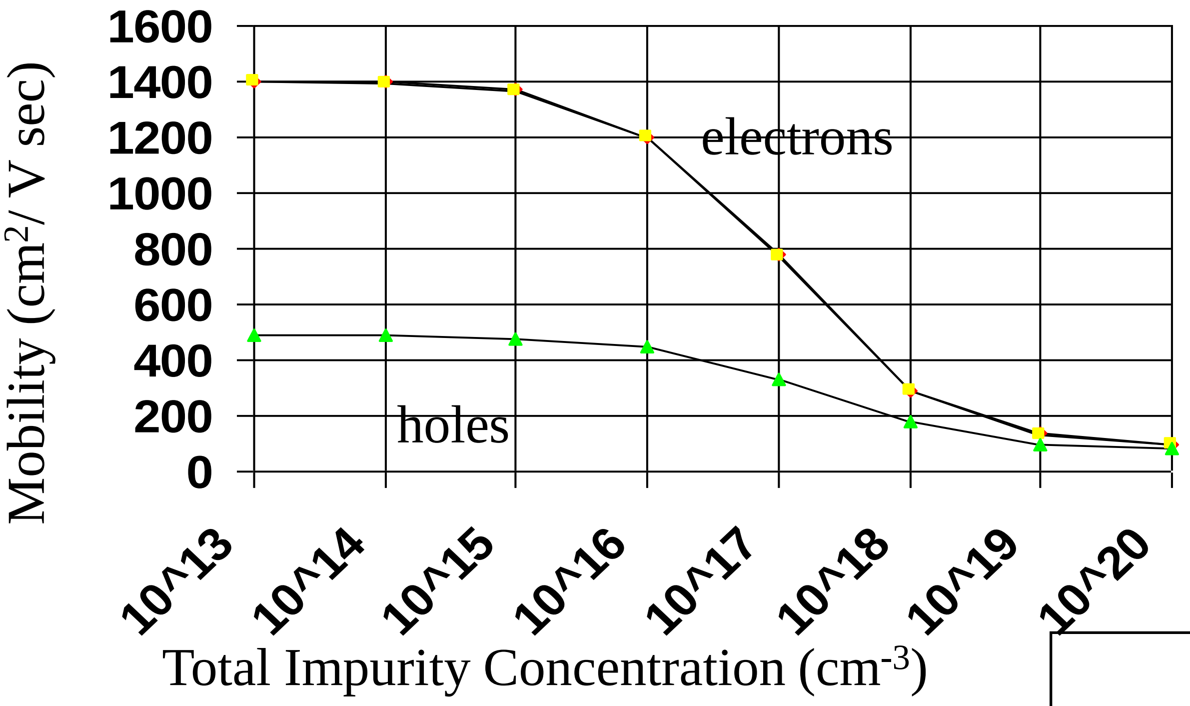
$$I_{Dsat} = \frac{\mu W\,Cox'}{2L}(Vg-Vt)^2$$

Saturation Region



Mobility (μ) decreases with increase in doping concentration

MOBILITY



Electron and hole mobilities in silicon at 300 K as functions of the total dopant concentration (N). The values plotted are the results of the curve fitting measurements from several sources. The mobility curves can be generated using the equation below with the parameters shown:

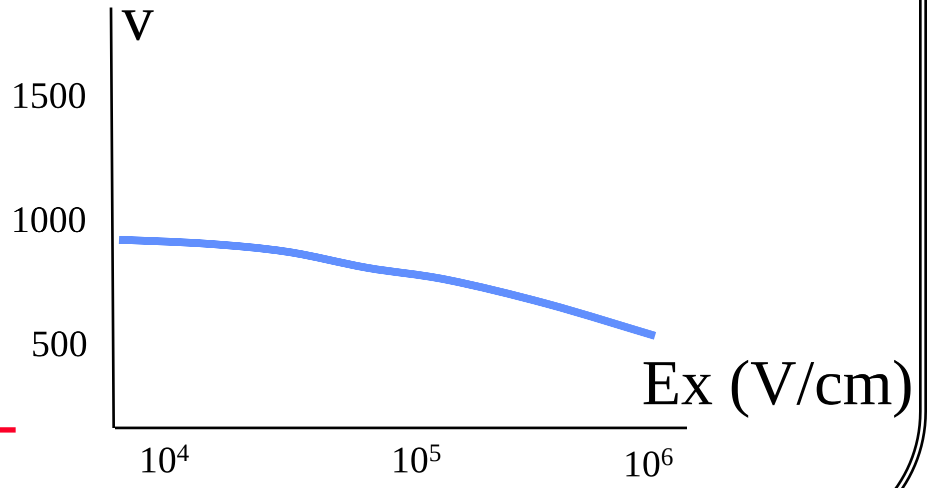
$$\mu(N) = \mu_{mi} + \frac{(\mu_{max}-\mu_{min})}{\{1 + (N/N_{ref})^{\alpha}\}}$$

From Muller and Kamins, 3rd Ed., pg 33

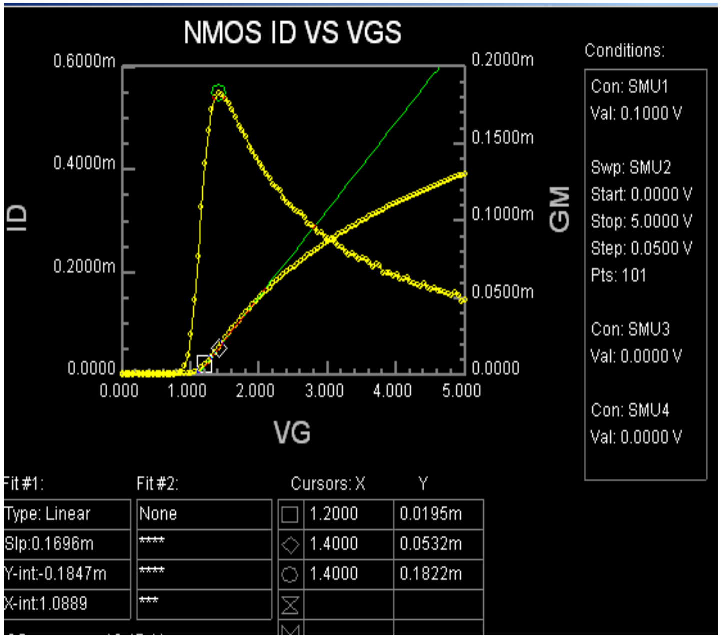
Parameter	Arsenic	Phosphorous	Boron
μ_{min}	52.2	68.5	44.9
μ_{max}	1417	1414	470.5
N_{ref}	9.68X10^16	9.20X10^16	2.23X10^17
α	0.680	0.711	0.719

MOBILITY DEGRADATION

In a MOSFET the mobility is lower than the bulk mobility because of the scattering with the Si-SiO2 interface. The vertical electric field causes the carriers to keep bumping into the interface causing the mobility to degrade. The electric fields can be 1E5 or 1E6 V/cm and at that level the collisions with the interface reduce the mobility even more. The vertical electrical field is higher for heavier doped substrates and when Vt adjust implants are used.



MOBILITY DEGRADATION



Conditions:

Con: SMU1
Val: 0.1000 V

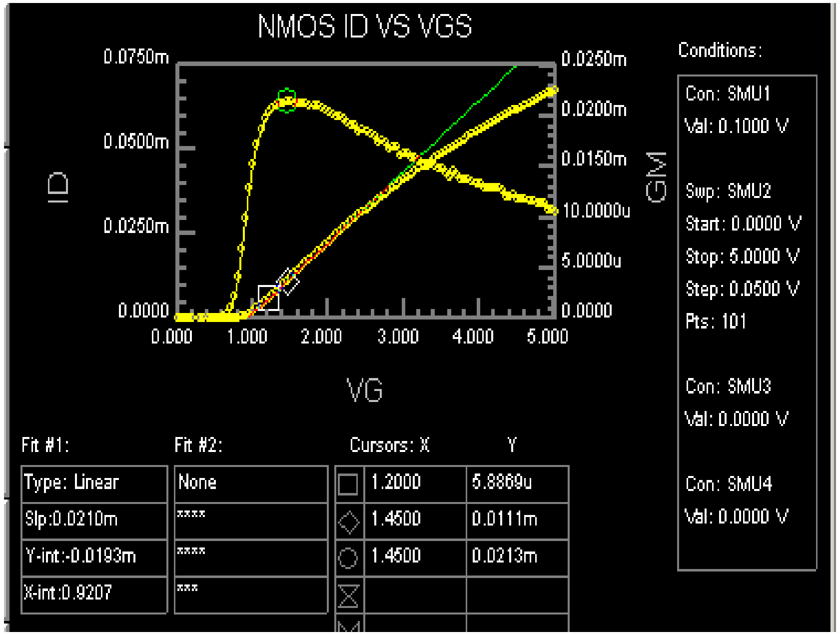
Swp: SMU2
Start: 0.0000 V
Stop: 5.0000 V
Step: 0.0500 V
Pts: 101

Con: SMU3
Val: 0.0000 V

Con: SMU4
Val: 0.0000 V

Fit #1:	Fit #2:	Cursors: X		Y
Type: Linear	None	□	1.2000	0.0195m
Slp:0.1696m	****	◇	1.4000	0.0532m
Y-int:-0.1847m	****	○	1.4000	0.1822m
X-int:1.0889	***	⧗		

short channel



Conditions:

Con: SMU1
Val: 0.1000 V

Swp: SMU2
Start: 0.0000 V
Stop: 5.0000 V
Step: 0.0500 V
Pts: 101

Con: SMU3
Val: 0.0000 V

Con: SMU4
Val: 0.0000 V

Fit #1:	Fit #2:	Cursors: X		Y
Type: Linear	None	□	1.2000	5.8869u
Slp:0.0210m	****	◇	1.4500	0.0111m
Y-int:-0.0193m	****	○	1.4500	0.0213m
X-int:0.9207	***	⧗		

long channel

Note: Id should follow green line in long channel devices

2^{nd} GENERATION MODELS EQUATIONS FOR MOBILITY

The mobility used in the equations for Ids is the effective mobility , Ueff. Starting with UO from level 1, Ueff is found. The parameter THETA is introduced to model mobility degradation due to high vertical electric fields (larger values of Vgs - VTO).

$$\boxed{\text{Ueff*} = \frac{\text{UO}}{(1+\text{THETA}\,(\text{Vgs-VTO}))}}$$

Measure Ids for a wide transistor with low value of Vds and large value of Vgs and using Leff from Terata-Muta method and LAMBDA from level 1, calculate THETA from these two equations.

$$I_{dsat} = \frac{\text{Ueff W Cox'}}{\text{2Leff}}\,(\text{Vg-Vt})^2\,(1+\lambda\text{Vds})$$

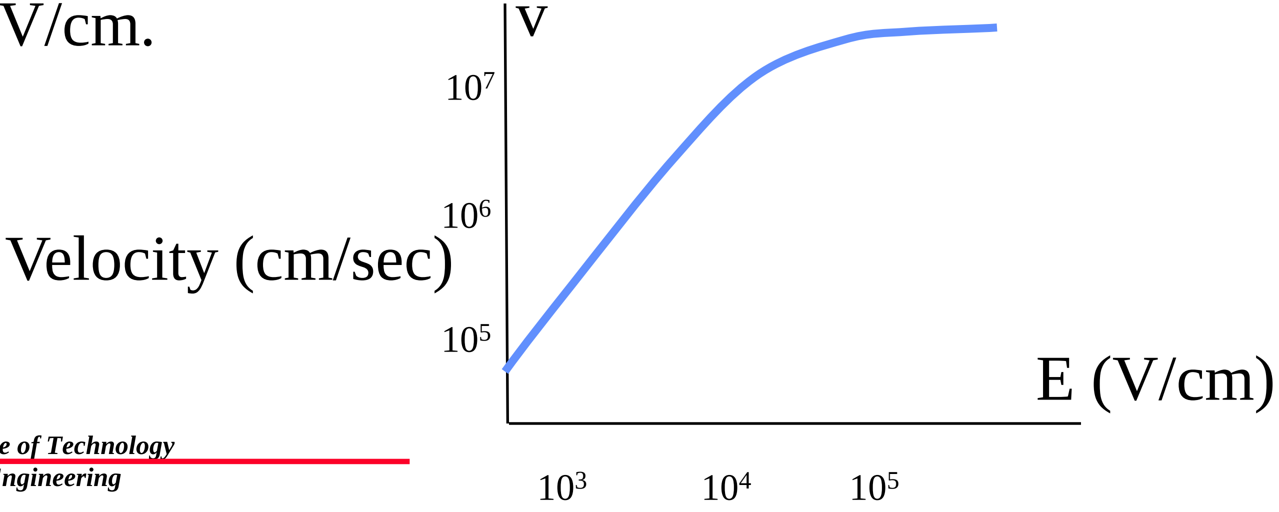
Warning: Curvature also due to R_{DS} so Vds is (Vapplied – Rds*Idsat) requires an iterative approach to find THETA

VELOCITY-SATURATION

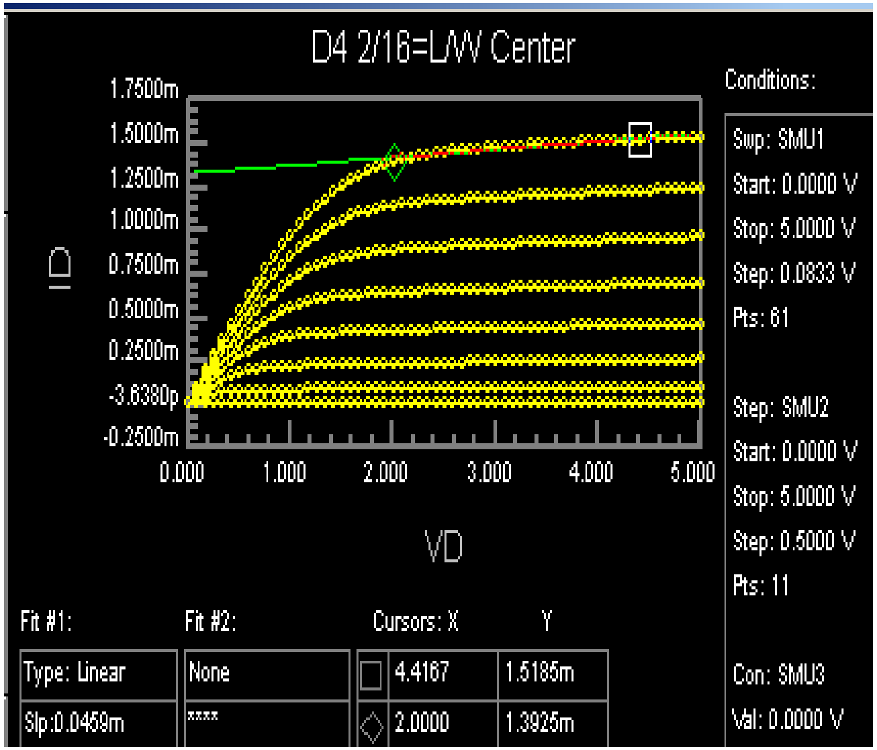
Carriers in semiconductors typically move in response to an applied electric field. The carrier velocity is proportional to the applied electric field. The proportionality constant is the mobility.

Velocity = mobility x electric field = μ E

At very high electric fields this relationship ceases to be accurate. The carrier velocity stops increasing (or we say saturates) In a one micrometer channel length device with one volt across it the electric field is 1E4 V/cm.



VELOCITY SATURATION



Conditions:

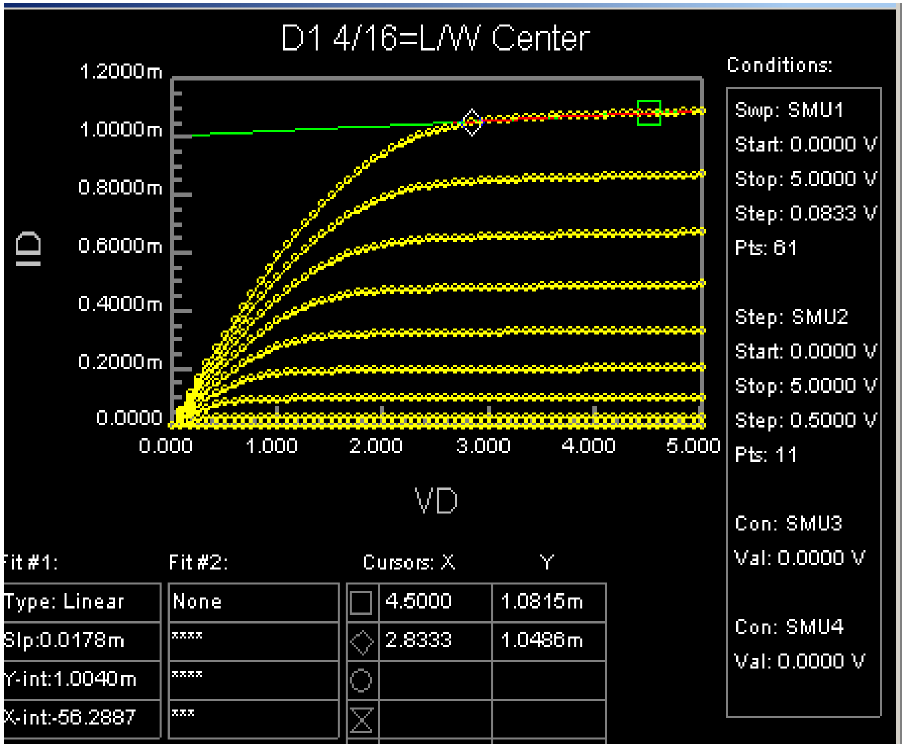
Swp: SMU1
Start: 0.0000 V
Stop: 5.0000 V
Step: 0.0833 V
Pts: 61

Step: SMU2
Start: 0.0000 V
Stop: 5.0000 V
Step: 0.5000 V
Pts: 11

Con: SMU3
Val: 0.0000 V

Fit #1:	Fit #2:	Cursors:	X	Y
Type: Linear	None	☐	4.4167	1.5185m
Slp:0.0459m	****	◇	2.0000	1.3925m

Short channel



Conditions:

Swp: SMU1
Start: 0.0000 V
Stop: 5.0000 V
Step: 0.0833 V
Pts: 61

Step: SMU2
Start: 0.0000 V
Stop: 5.0000 V
Step: 0.5000 V
Pts: 11

Con: SMU3
Val: 0.0000 V

Con: SMU4
Val: 0.0000 V

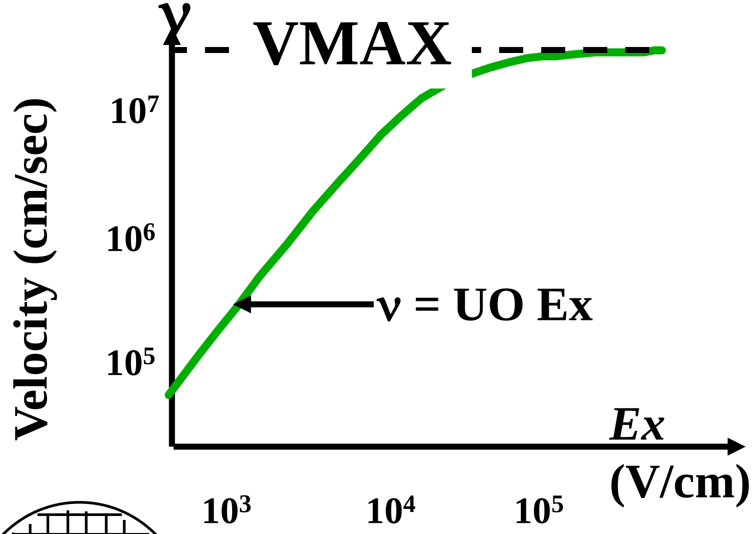
Fit #1:	Fit #2:	Cursors:	X	Y
Type: Linear	None	☐	4.5000	1.0815m
Slp:0.0178m	****	◇	2.8333	1.0486m
Y-int:1.0040m	****	○		
X-int:-56.2887	***	⧖		

long channel

Note: Id should increase with $(Vgs-Vt)^2$ in long channel devices

2ND GENERATION EQUATIONS FOR MOBILITY (cont.)

The parameter VMAX is introduced to model the decrease in mobility at higher Vds due to velocity saturation. Ideally, carrier velocity is directly proportional to the applied electric field. However, at very high lateral electric fields, Ex, this relationship ceases to be accurate - the carrier velocity saturates at VMAX.

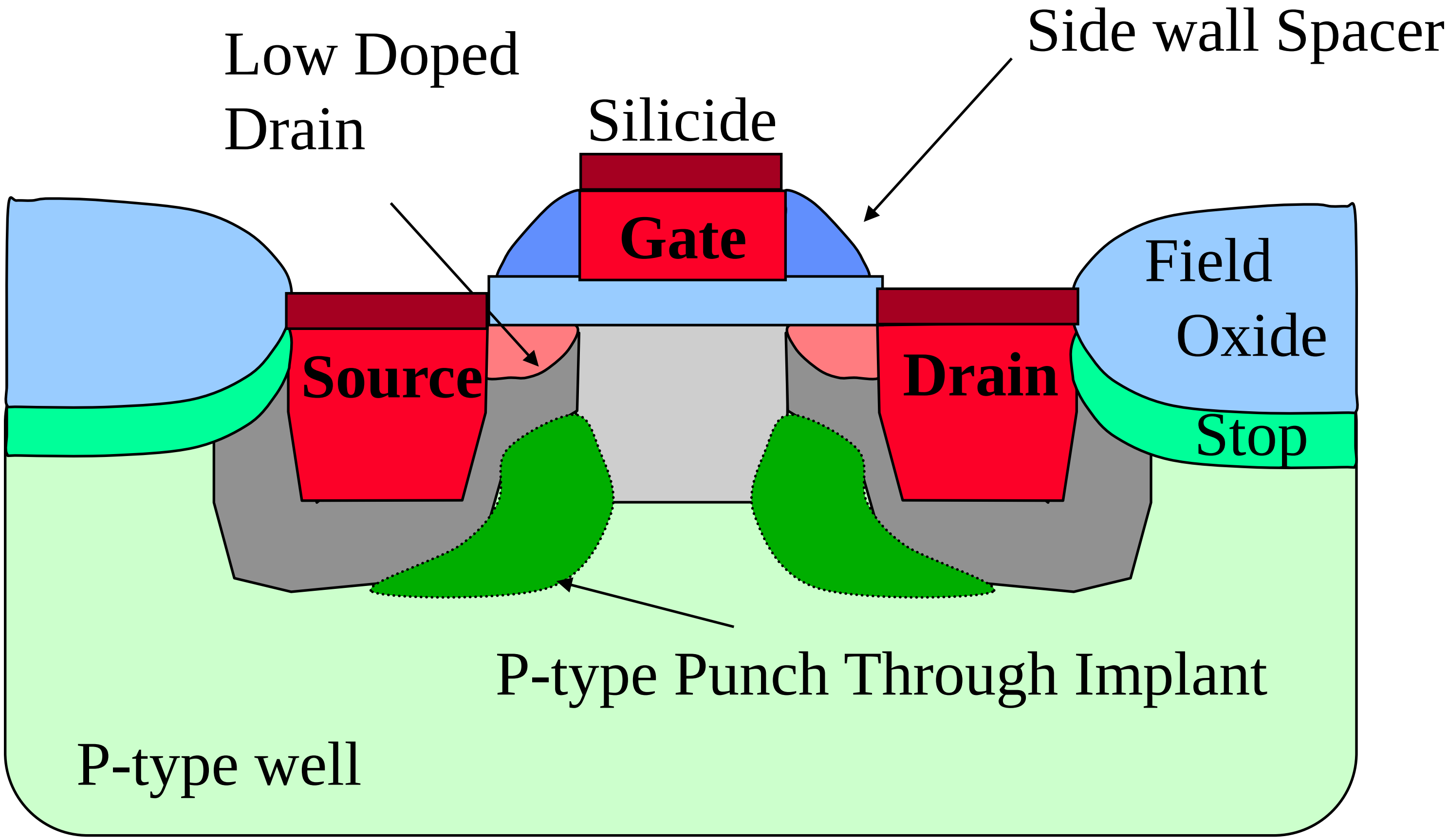


$$\text{Ueff} = \frac{\text{UO}}{\left(1+\text{THETA}\,(\text{Vgs}-\text{VTO})\right)\left(1 + \text{UO}\,\dfrac{\text{vde}}{\text{VMAX Leff}}\right)}$$

Where, Vde = min (Vds, Vdsat)

Note: other models (equations) for mobility exist and use parameters such as UCRIT, UEXP, ULTRA, ECRIT, ESAT

LOW DOPED DRAIN REDUCES LATERAL FIELD



GATE OXIDE LEAKAGE

The gate should be as thin as possible to reduce the short channel effects. In addition there is a limit imposed by considerations that affect the long term reliability of the gate oxide. This requirement imposes a maximum allowed electric field in the oxide under the long term normal operating conditions. This limit is chosen as 80% of the oxide field value at the on-set of Fowler-Nordheim (F-N) tunneling through the oxide. Since the latter is 5 MV/cm, a 4 MV/cm oxide field is considered as the maximum allowed for long term, reliable operation. For example:

For 2.5 volt operation, Xox is set at: $X_{ox} = V_{dd} / E_{max}$

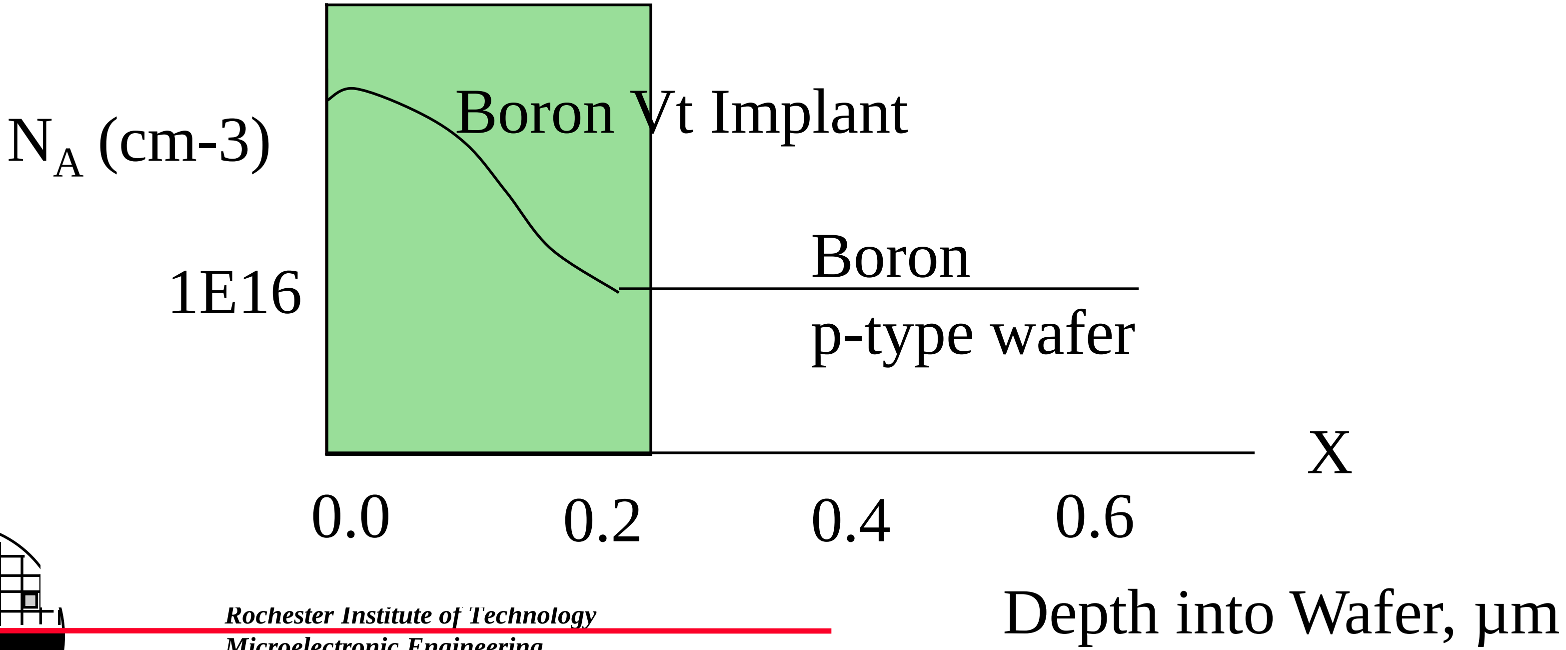
$$= 2.5\ \text{V} / 4\ \text{MV/cm} = 65\ \text{Å}$$

SALICIDE

Ti Salicide will reduce the sheet resistance of the poly and the drain and source regions. Salicide is an acronym for Self Aligned Silicide and Silicide is a material that is a combination of silicon and metal such as Ti, W or Co. These materials are formed by depositing a thin film of the metal on the wafer and then heating to form a Silicide. The Silicide forms only where the metal is in contact with the Silicon or poly. Etchants can remove the metal and leave the Silicide thus the term **S**elf **A**ligned Si**licide** or SALICIDE.

NMOS WITH N+ POLY GATE

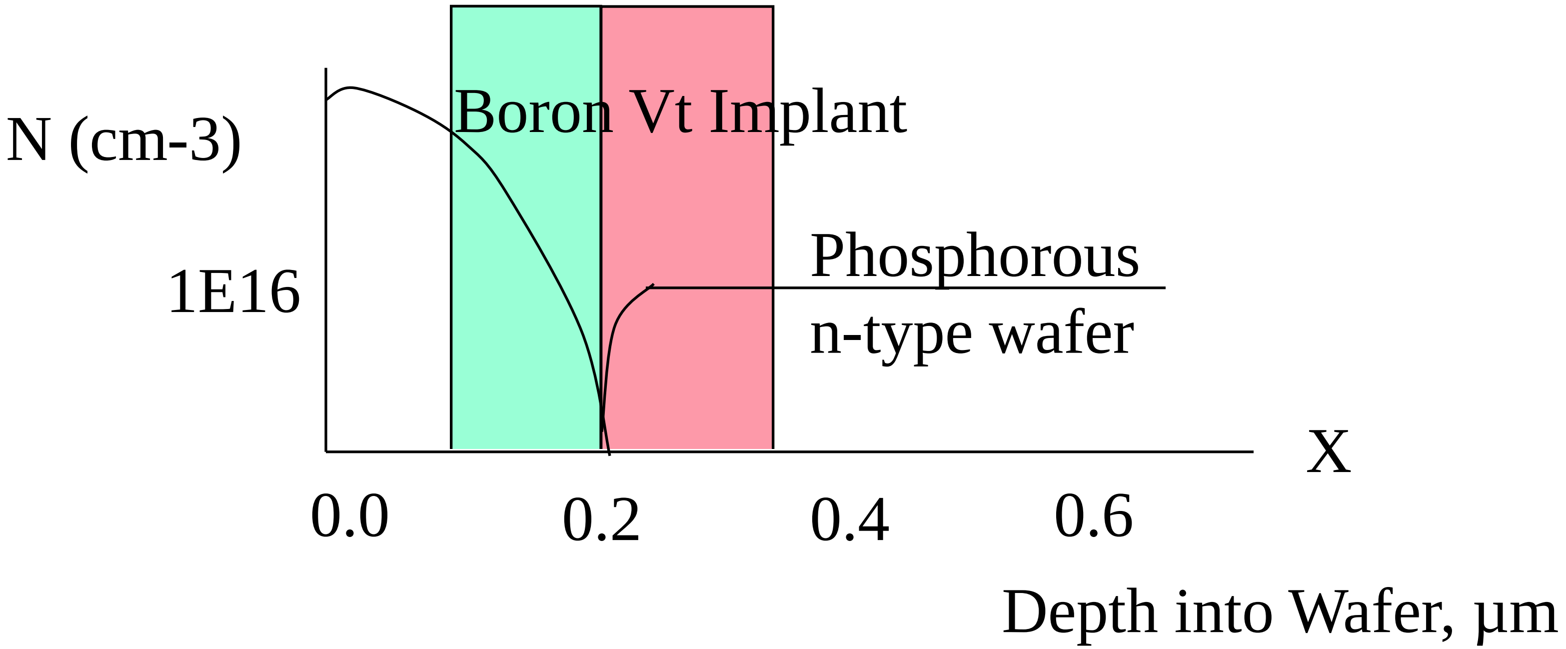
- **Vt Is Typically Negative Or If Positive Near Zero**
- **Vt Adjust Implant Is Boron In A P-type Substrate Making The Nmos Transistor A Surface Channel Device**



PMOS WITH N+ POLY GATE

- **Vt Can Not Be Positive Because All The Contributors To The Vt Are Negative. Even Making Qss=0 And Nd = Zero Does Not Make Vt Positive**
- **Vt Is Typically More Negative Than Desired Like -2 Volts**
- **Vt Adjust Implant Is Boron In An N-type Substrate Making The Pmos Transistor A Buried Channel Device (Charge Carriers Move Between Drain And Source At Some Distance Away From The Gate Oxide/Silicon Interface**

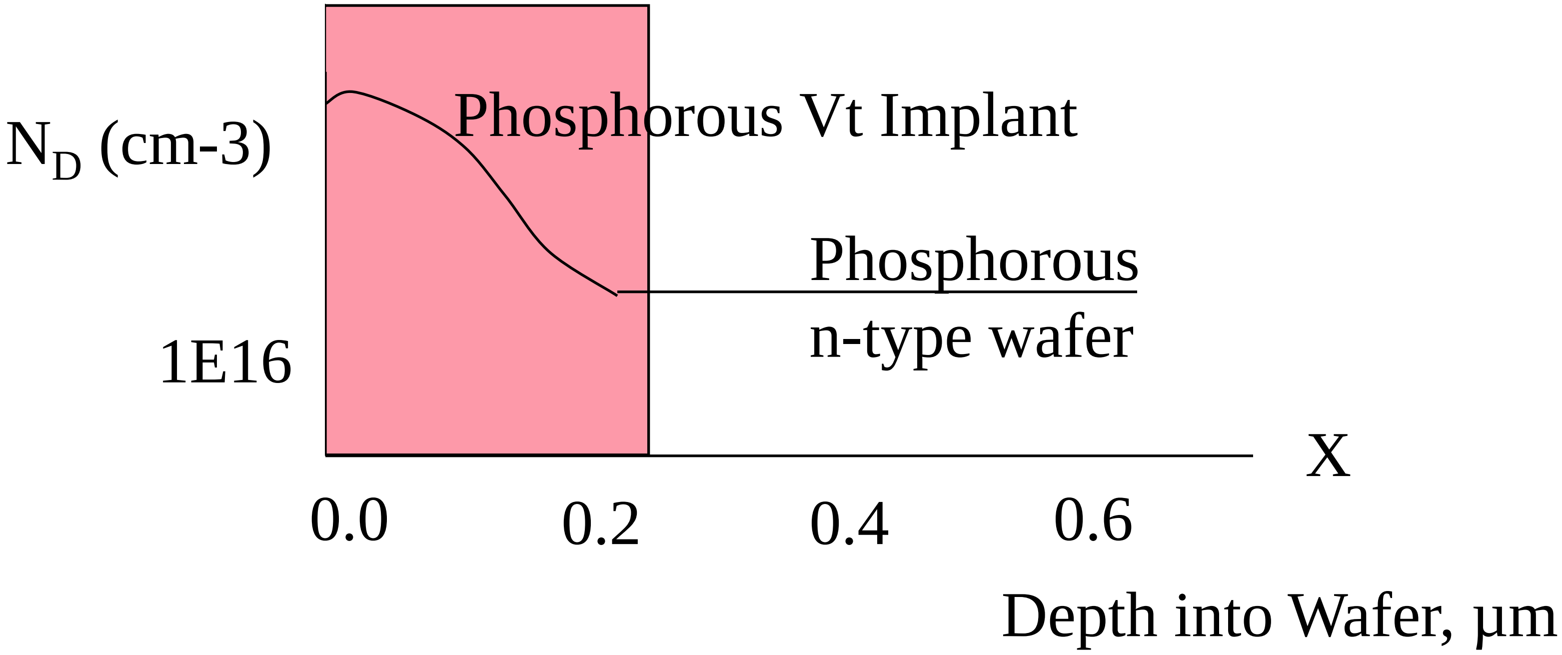
PMOS WITH N+ POLY GATE



PMOS WITH P+ POLY GATE

- **Changes Work Function Of The Metal**
- **Thus Metal-semiconductor Workfunction Differernce Becomes About +1 Volt Rather Than ~0 Volts.**
- **This Makes Vt More Positive Than Desired So An Ion Implant Of N-type Impurity Is Needed Making The Device A Surface Channel Device Rather Than A Buried Channel Device.**

PMOS WITH P+ POLY GATE

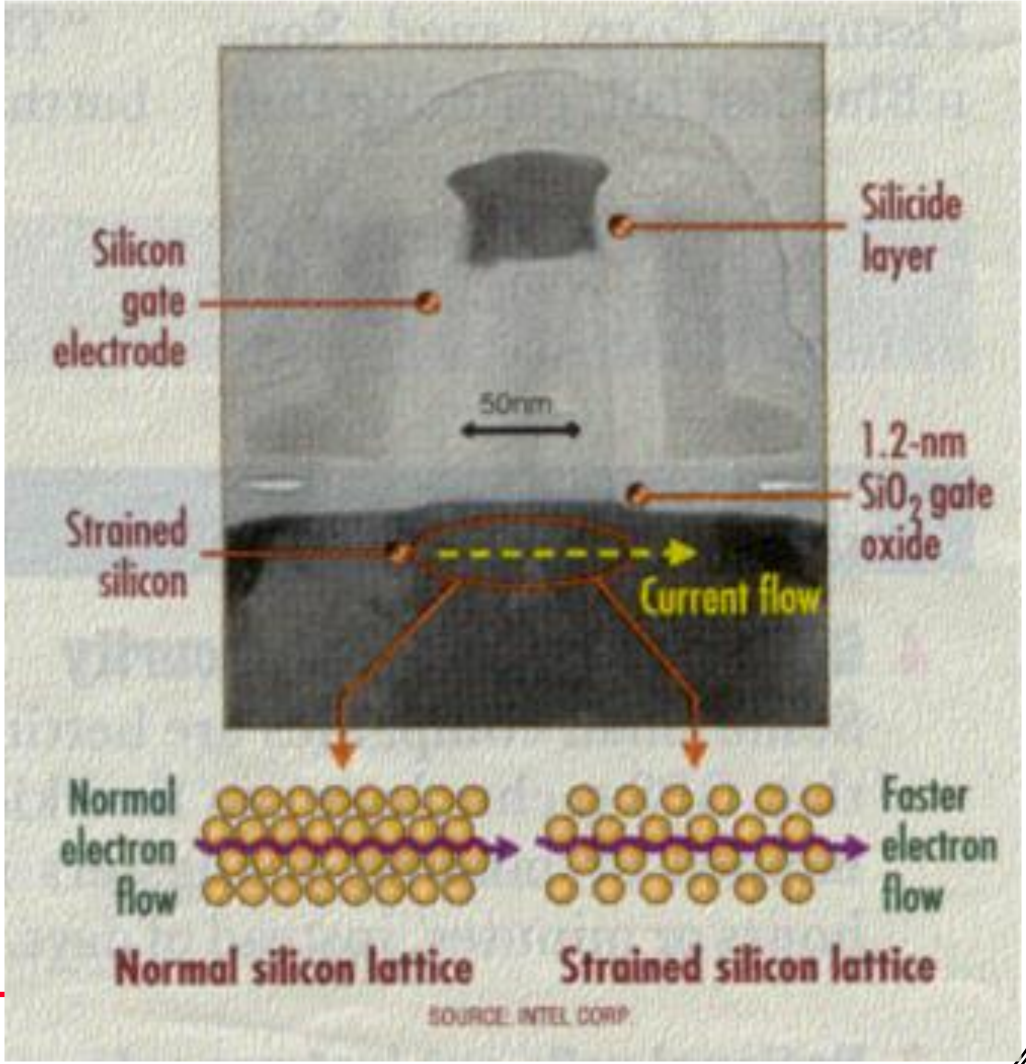


SURFACE CHANNEL VS BURIED CHANNEL

- Surface Channel Devices Exhibit Higher Subthreshold Slope
- Surface Channel Devices Are Less Sensitive To Punch Through
- Surface Channel Devices Have Less Severe Threshold Voltage Rolloff
- Surface Channel Devices Have Higher Transconductance
- Surface Channel Devices Have About 15% Lower Carrier Mobility

STRAINED SILICON

Strained silicon can increase carrier mobility



STRAINED SILICON

A simple way to think about strained silicon follows: Tensile strain causes the silicon atoms to be pulled further apart making it easier for electrons to move through the silicon. On the other hand moving the atoms further apart makes it harder for holes to move because holes require bound electrons to move from a silicon atom to a neighboring silicon atom in the opposite direction, which is more difficult if they are further apart. Thus tensile strain increases mobility in n-type silicon and compressive strain increases mobility in p-type silicon (devices).

Strain can be created globally or locally. Growing an epitaxial layer of silicon on a silicon/germanium substrate creates (global) biaxial tensile strain in the silicon. N-MOSFETS built on these wafers will have higher mobility. P-MOSFETS will have lower mobility. Local strain can be created for each transistor such that N-MOSFETS see tensile strain and P-MOSFETS see compressive strain improving both transistors mobility. Local strain techniques include capping layers and introducing Ge or C in the source/drain regions.

0.025µm STRAINED SILICON MOSFET

2007

Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon–Carbon Source/Drain and Tensile-Stress Liner

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Ming-Fu Li, Ganesh S. Samudra, and Yee-Chia Yeo

Abstract—We report the demonstration of 25-nm gate-length L_G strained nMOSFETs featuring the silicon–carbon source and drain ($Si_{1-y}C_y$S/D) regions and a thin-body thickness T_{body} of ~18 nm. This is also the smallest reported planar nMOSFET with the $Si_{1-y}C_y$S/D stressors. Strain-induced mobility enhancement due to the $Si_{1-y}C_y$S/D leads to a significant drive-current I_{Dsat} enhancement of 52% over the control transistor. Furthermore, the integration of tensile-stress SiN etch stop layer and $Si_{1-y}C_y$S/D extends the I_{Dsat} enhancement to 67%. The performance enhancement was achieved for the devices with similar subthreshold swing and drain-induced barrier lowering. The $Si_{1-y}C_y$S/D technology and its combination with the existing strained-silicon techniques are promising for the future high-performance CMOS applications.

Index Terms—Electron mobility, nMOSFET, silicon–carbon ($Si_{1-y}C_y$), silicon nitride liner, strain, stress.

I. INTRODUCTION

RECENTLY, channel-strain engineering is being actively pursued to enhance carrier mobility and drive current

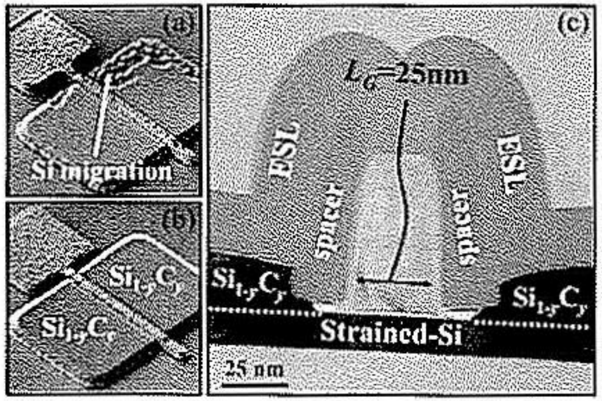

Fig. 1. (a) SEM image showing problems of silicon migration during the high temperature (800 °C) prebake step in the $Si_{1-y}C_y$ selective epitaxy process. (b) Excellent morphology of $Si_{1-y}C_y$ on the S/D regions is demonstrated when a reduced prebake temperature (700 °C) and a tightly controlled SOI body thickness are used. (c) TEM micrograph of a strained n-channel transistor with the $Si_{1-y}C_y$S/D stressors and the high stress ESL. This transistor features the physical gate length L_G of 25 nm and the body thickness T_{body} of ~15 nm. A 25-nm-thick SiN ESL with the tensile stress of 1.1 GPa was used.

0.025µm STRAINED SILICON MOSFET

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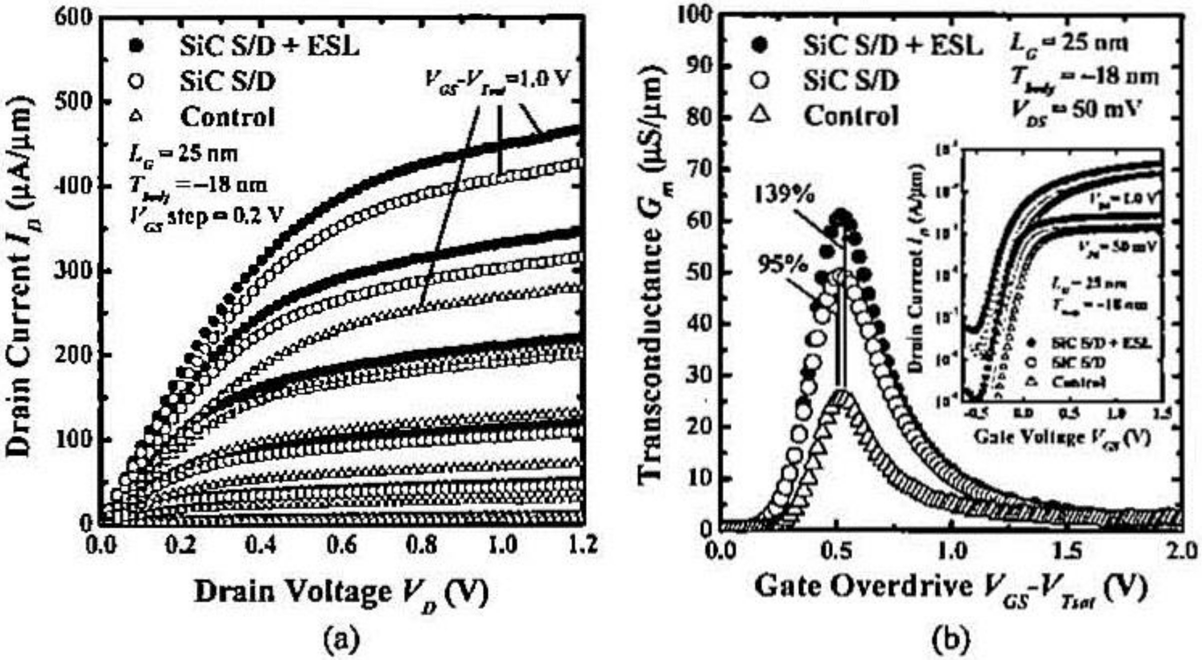
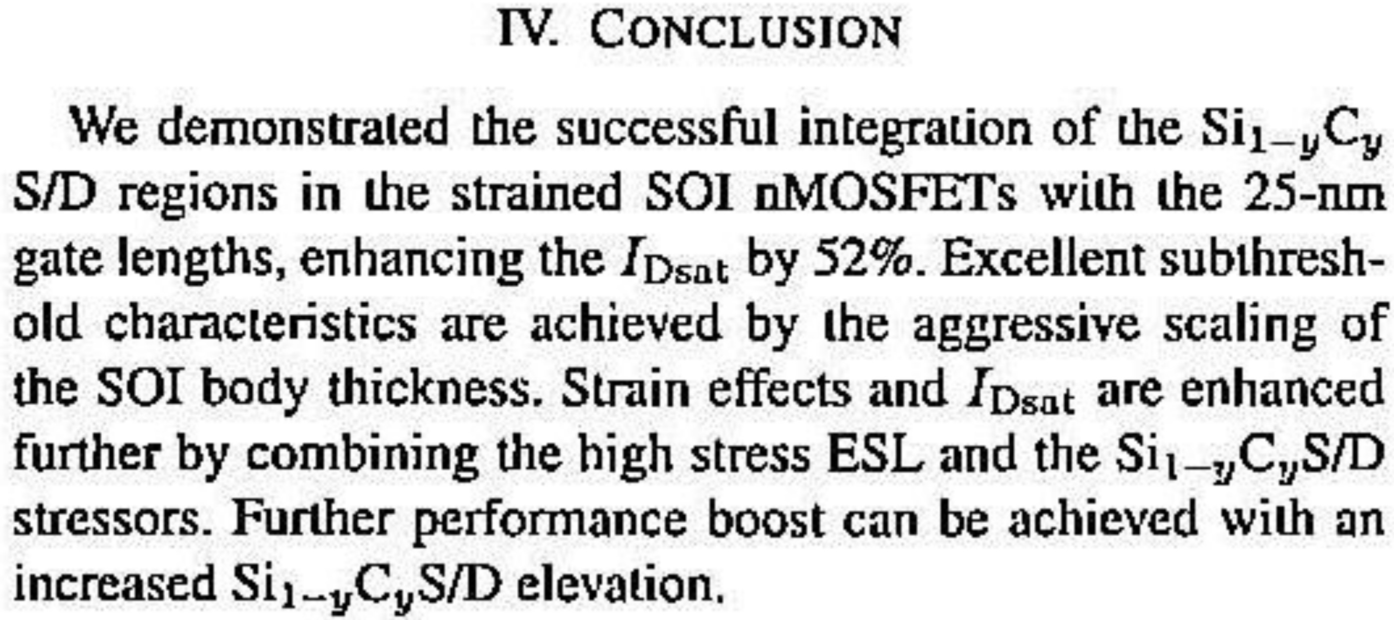


Fig. 2. (a) I_{DS}–V_{DS} characteristics of the control and strained nMOSFETs with single stressor (Si$_{1-y}$C$_y$S/D) and dual stressors (Si$_{1-y}$C$_y$S/D and tensile-stress SiN ESL). Significant I_{Dsat} enhancement of 52% is observed in the single stressor device over the control transistor. Even higher I_{Dsat} improvement of 67% is achieved with the integration of high stress ESL and Si$_{1-y}$C$_y$S/D. (b) Single and dual stressor strained devices are observed to enhance the transconductance by 95% and 139% over the control transistor, respectively.

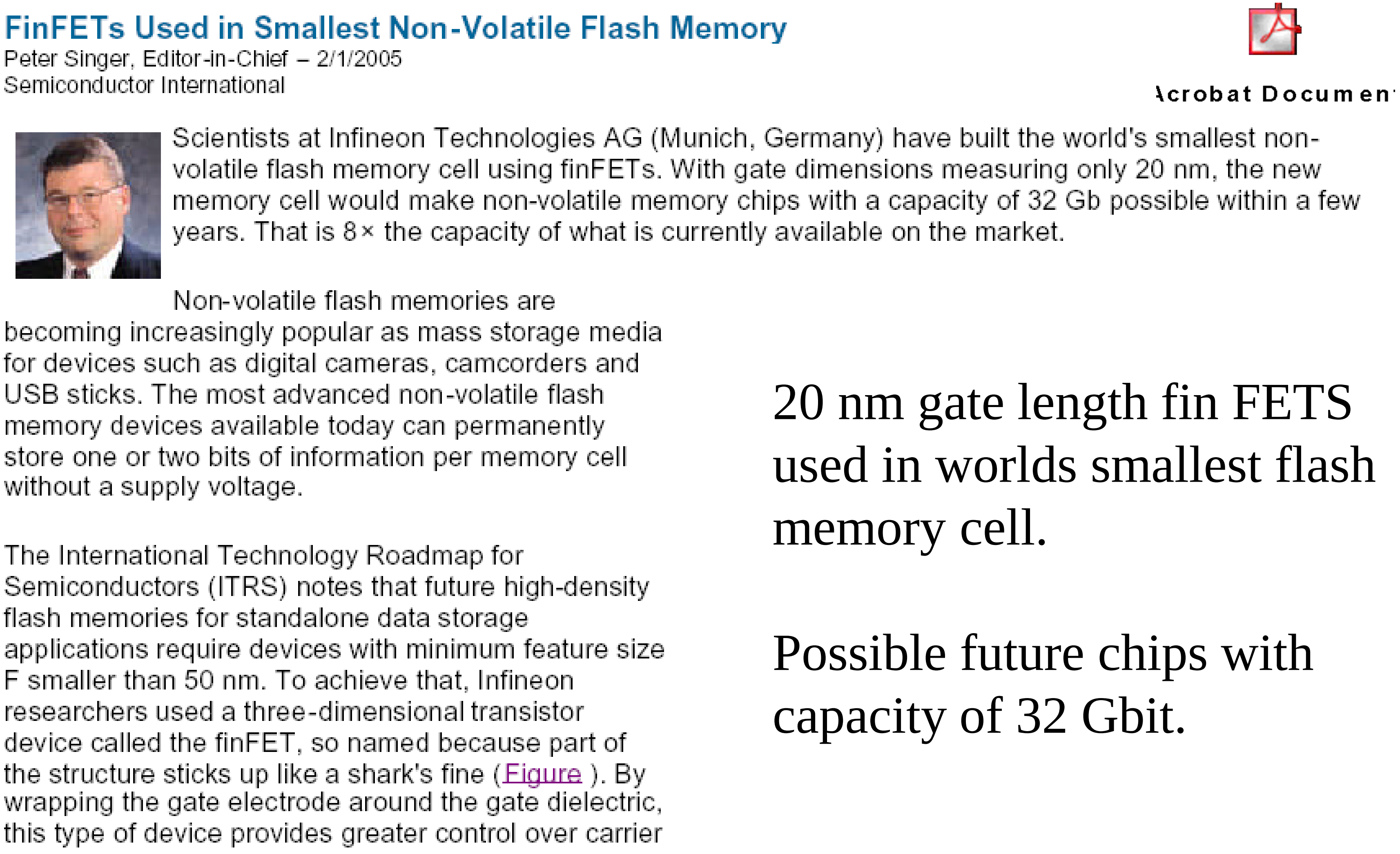
0.025µm STRAINED SILICON MOSFET



IV. CONCLUSION

We demonstrated the successful integration of the $Si_{1-y}C_y$ S/D regions in the strained SOI nMOSFETs with the 25-nm gate lengths, enhancing the I_{Dsat} by 52%. Excellent subthreshold characteristics are achieved by the aggressive scaling of the SOI body thickness. Strain effects and I_{Dsat} are enhanced further by combining the high stress ESL and the $Si_{1-y}C_y$S/D stressors. Further performance boost can be achieved with an increased $Si_{1-y}C_y$S/D elevation.

FIN FETS IN FLASH MEMORY



FinFETs Used in Smallest Non-Volatile Flash Memory

Peter Singer, Editor-in-Chief – 2/1/2005
Semiconductor International

Scientists at Infineon Technologies AG (Munich, Germany) have built the world's smallest non-volatile flash memory cell using finFETs. With gate dimensions measuring only 20 nm, the new memory cell would make non-volatile memory chips with a capacity of 32 Gb possible within a few years. That is 8× the capacity of what is currently available on the market.

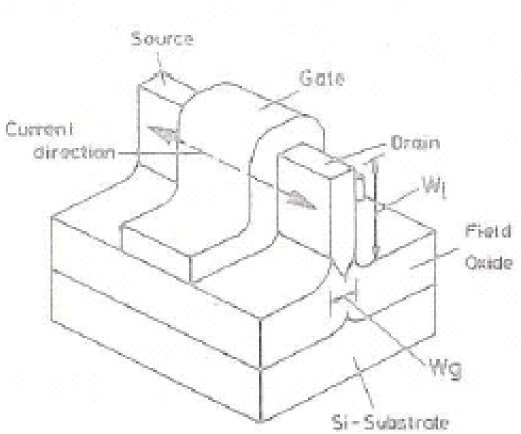
Non-volatile flash memories are becoming increasingly popular as mass storage media for devices such as digital cameras, camcorders and USB sticks. The most advanced non-volatile flash memory devices available today can permanently store one or two bits of information per memory cell without a supply voltage.

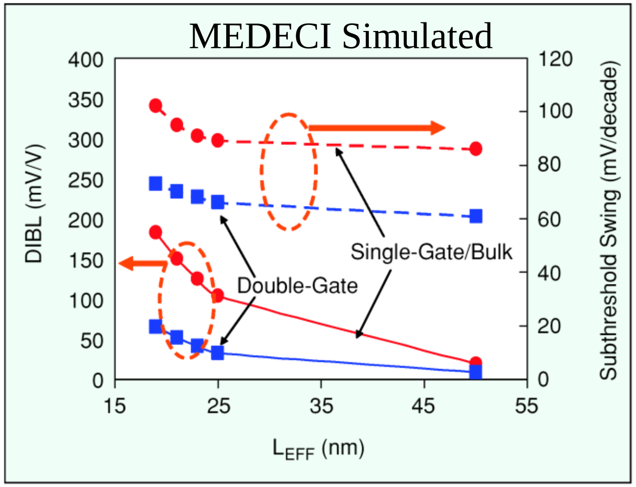
The International Technology Roadmap for Semiconductors (ITRS) notes that future high-density flash memories for standalone data storage applications require devices with minimum feature size F smaller than 50 nm. To achieve that, Infineon researchers used a three-dimensional transistor device called the finFET, so named because part of the structure sticks up like a shark's fine (Figure). By wrapping the gate electrode around the gate dielectric, this type of device provides greater control over carrier flow and leakage current. When used in memory

20 nm gate length fin FETS used in worlds smallest flash memory cell.

Possible future chips with capacity of 32 Gbit.

TRIPLE GATE TRANSISTOR





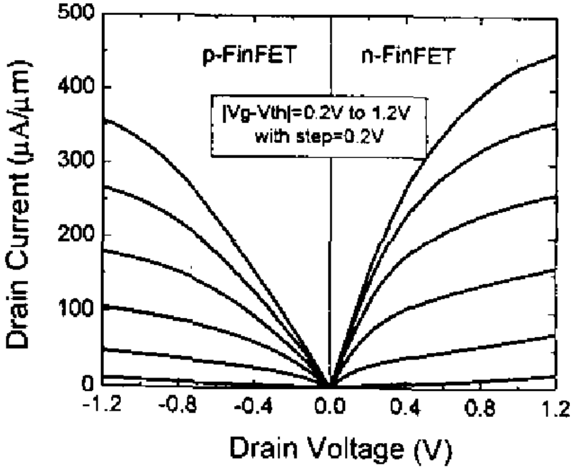


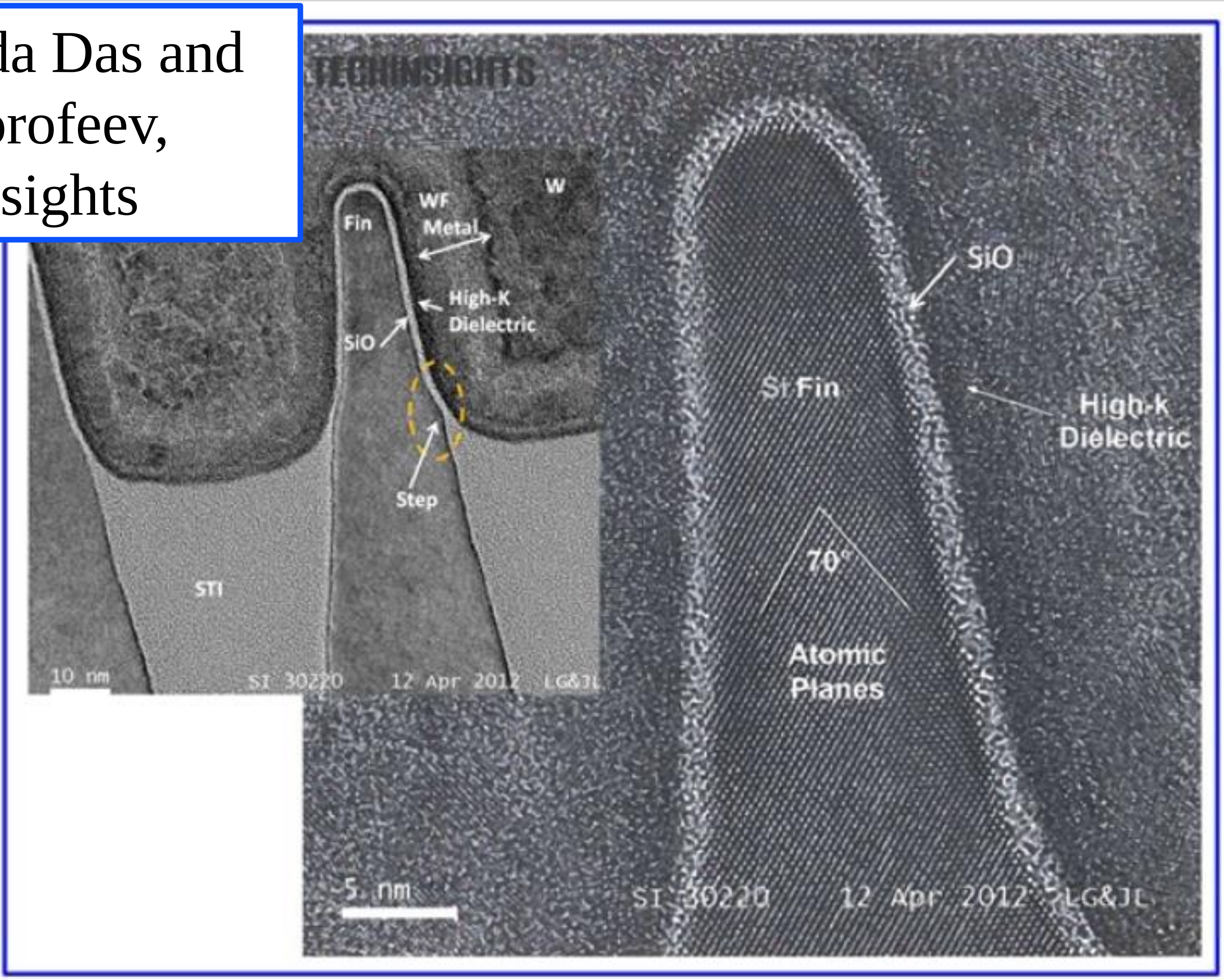
Fig.5 Id-Vd characteristics of 10nm gate length CMOS FinFET transistors.

- The drive currents are 446 uA/um for n-FinFET and 356 uA/um for p-FinFET respectively
- The peak transconductance of the p-FinFET is very high (633uS/um at 105 nm L_g), because the hole mobility in the (110) channel is enhanced
- Gate Delay is 0.34 ps for n-FET and 0.43 ps for p-FET respectively at 10 nm Lg
- The subthreshold slope is ~60 mV/dec for n-FET and 101 mV/dec for p-FET respectively
- The DIBL is 71 mV/V n-FET and 120 mV/V for p-FET respectively

Qin Zhang, 04/19/2005

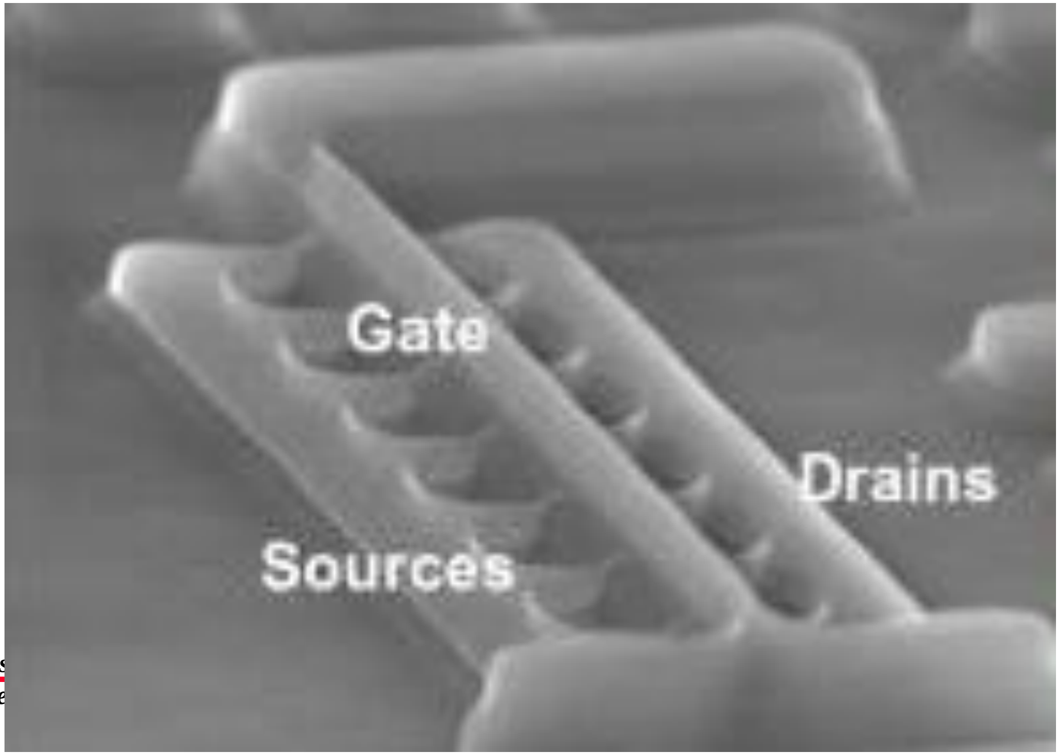
FIN FET

from: Arabinda Das and Alexandre Dorofeev, UBM Tech Insights



SUMMARY FOR FINFETS AND TRIPLE GATE FETS

1. Fin FETS have higher gm and Idrive because mobility is increased with lower doped channels.
2. Fin FETs have higher sub-threshold slope.
3. Fin FETS have lower DIBL



SUMMARY

Todays most advanced devices have gate lengths near 10nm. Although the goal is to have long channel behavior it is difficult to achieve. There are many factors to consider and no simple solution. The models for simulation (SPICE) have become very complex.

REFERENCES

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HOMEWORK – MOSFET

1. Calculate the IDS -VDS characteristics for a PMOS transistor for 0<VDS <5 built with the following parameters: substrate doping ND = 1E15 cm-3, Xox = 500 Å, N+ poly gate, Nss = 3E11, W = 32 µm, L = 16 µm

2. Use SPICE to simulate the IDS-VDS characteristics for the PMOS transistor above. Compare SPICE versus hand calculated (Excel).

3. Use SPICE to simulate the IDS-VDS characteristics for a NMOS transistor using a SPICE MOSFET model for L = 1um and for L = 0.1um. Let W be 10 times L.