ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

MOS Inverters

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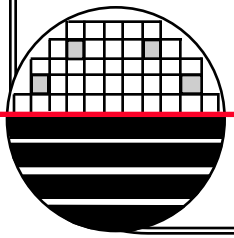
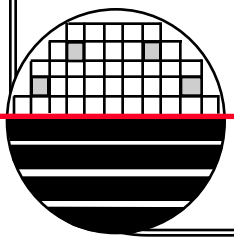


OUTLINE

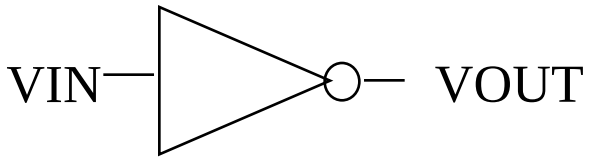
Introduction
Voltage Transfer Curve (VTC)
Noise Margin
Inverter Current vs. Vin
PMOS Inverter
NMOS Inverter
CMOS Inverter
Pseudo NMOS Inv, NAND and NOR
References
Homework



INTRODUCTION

There are many ways to make an inverter. In this document we will investigate various MOS inverters, their voltage transfer curve, current, noise margin, speed etc. The inverter is the simplest logic gate to analyze and can give useful results for the comparison of different inverter designs and fabrication technologies.

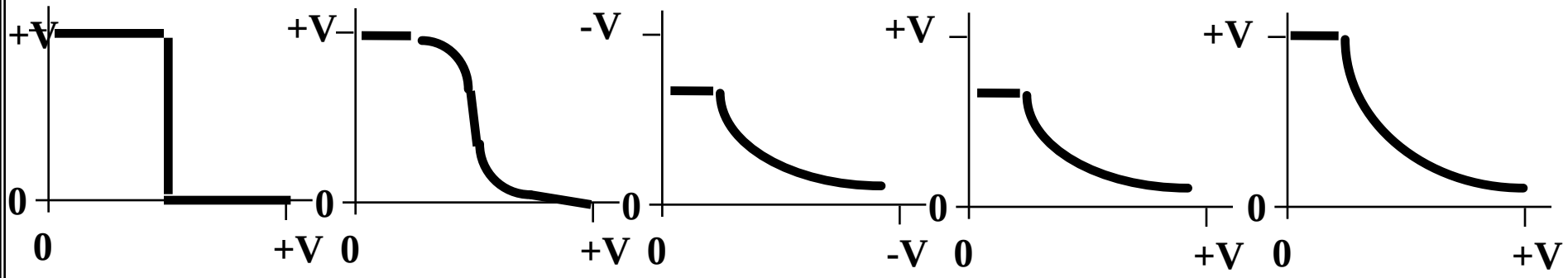
SYMBOL

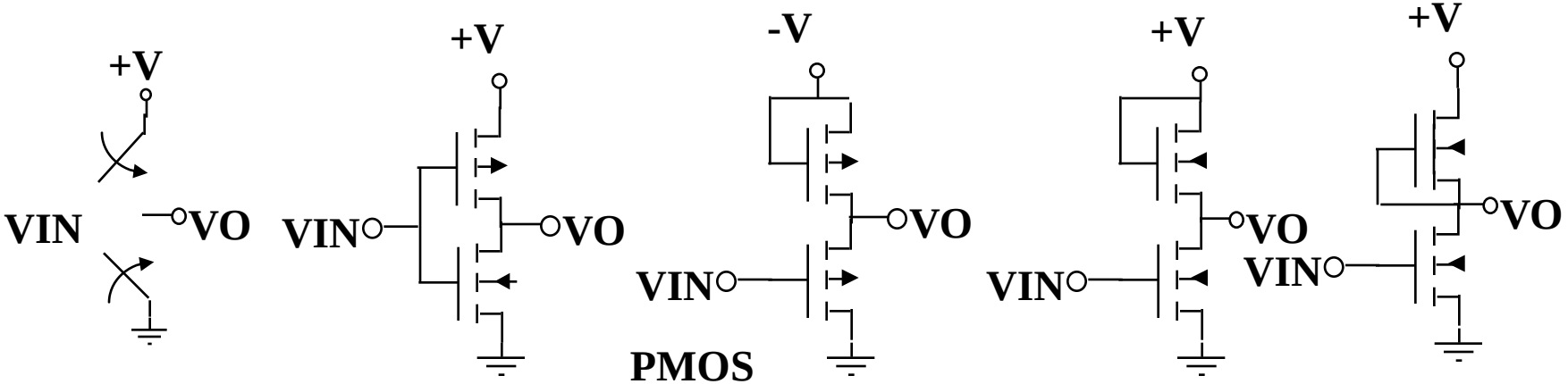


TRUTH TABLE

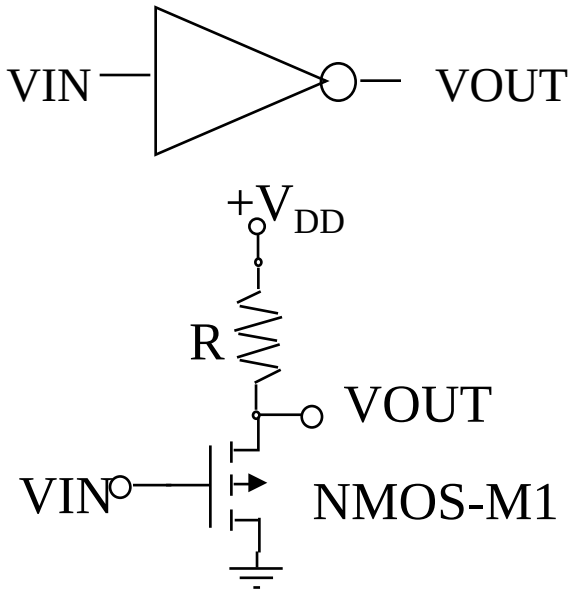
VIN	VOUT
0	1
1	0

INVERTER TYPES - VOUT VS VIN (VTC)

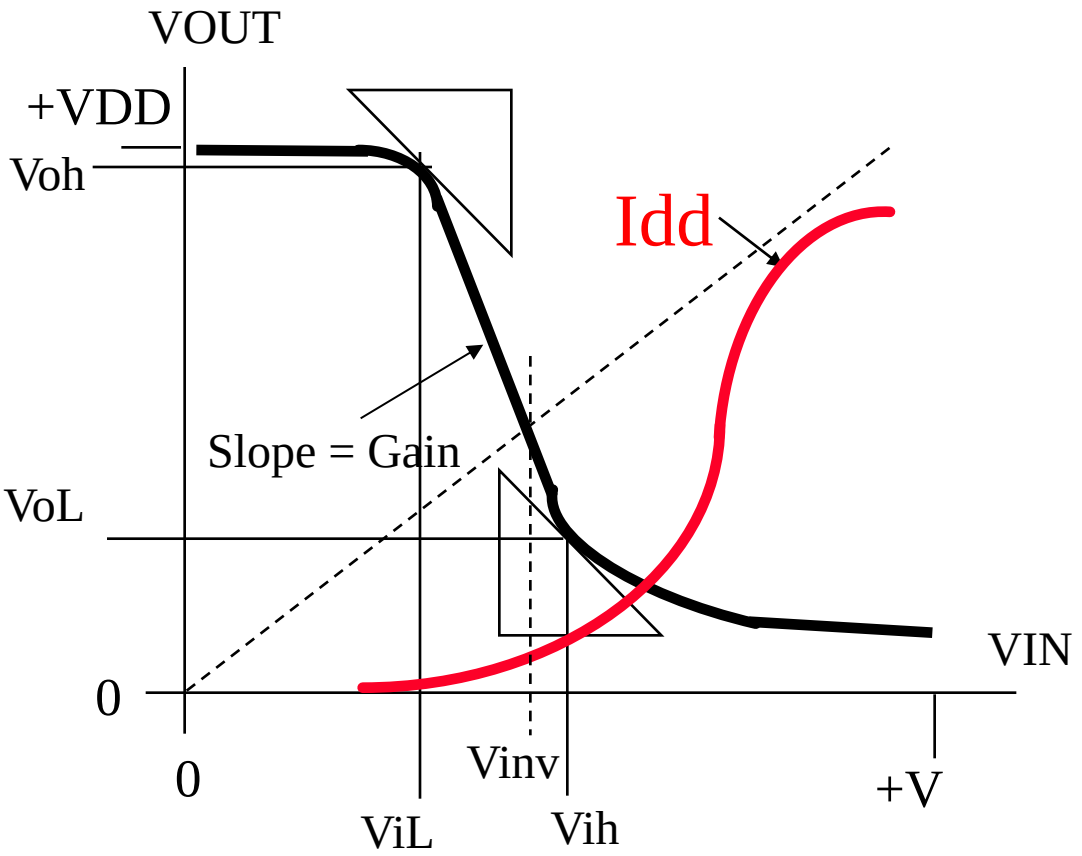




VOLTAGE TRANSFER CURVE NMOS-RESISTOR LOAD

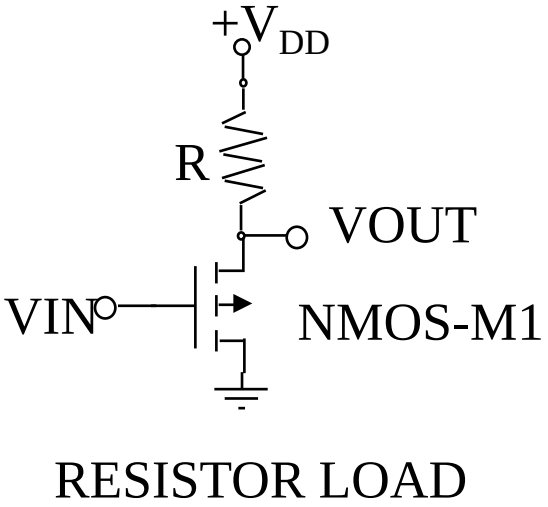


RESISTOR LOAD

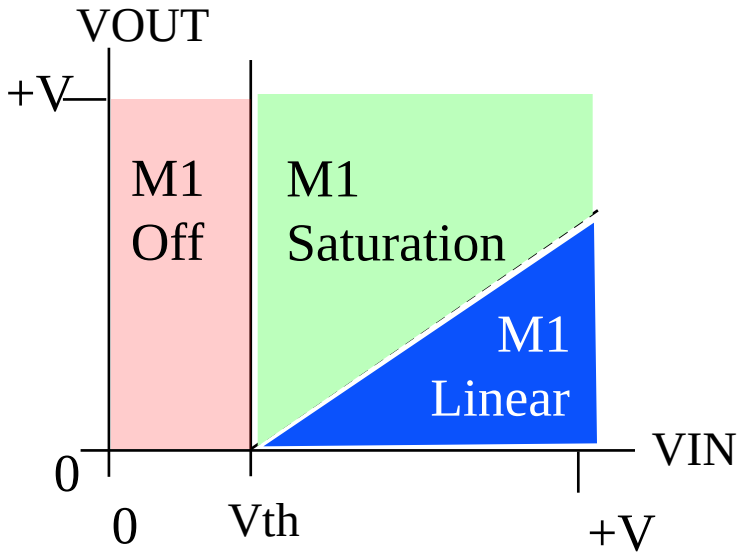


NML, noise margin low, Δ0 =ViL-VoL
NMH, noise margin high, Δ1 =VoH-ViH

CALCULATION OF VTC



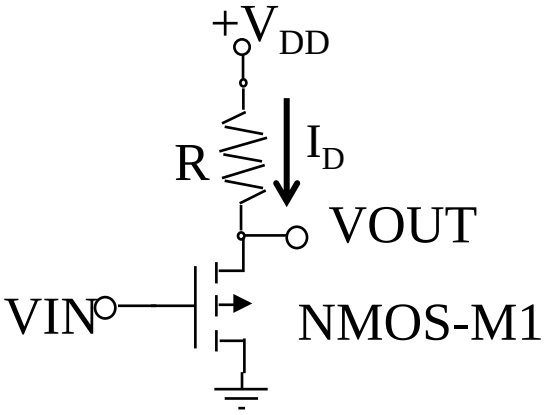
RESISTOR LOAD



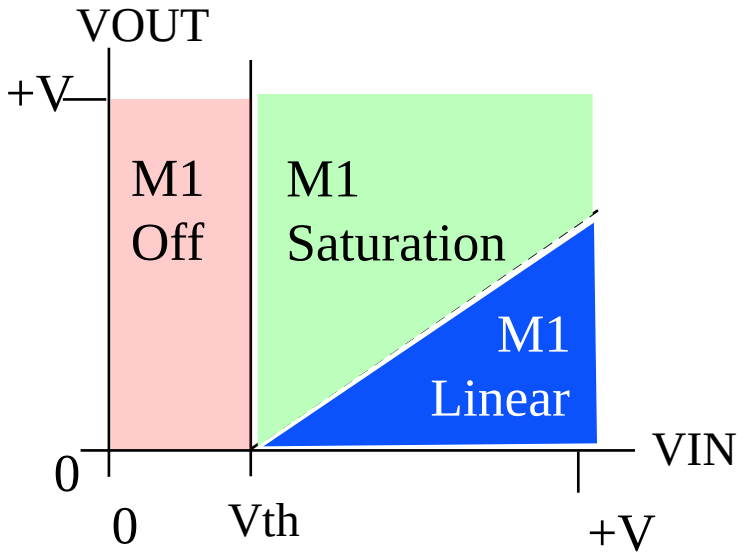
First figure out if the transistor is
sub-threshold or off, Vgs < Vth and Vgd < Vth
non-saturation, Vgs > Vth and Vgd > Vth
saturation region, Vgs > Vth and Vgd < Vth

Note: Vin = Vgs, Vout = Vds, therefore Vgd = Vin-Vout
Vth might be +1volt

CALCULATION OF VTC



RESISTOR LOAD



Next calculate Vout = $V_{DD} - I_D R$ using the correct equation for I_D for the transistor depending on region of operation

Linear (Non-Saturation)

$$I_D = \frac{\mu W \, Cox' \, (Vg - Vt - V_d/2) V_d}{L}$$

Saturation

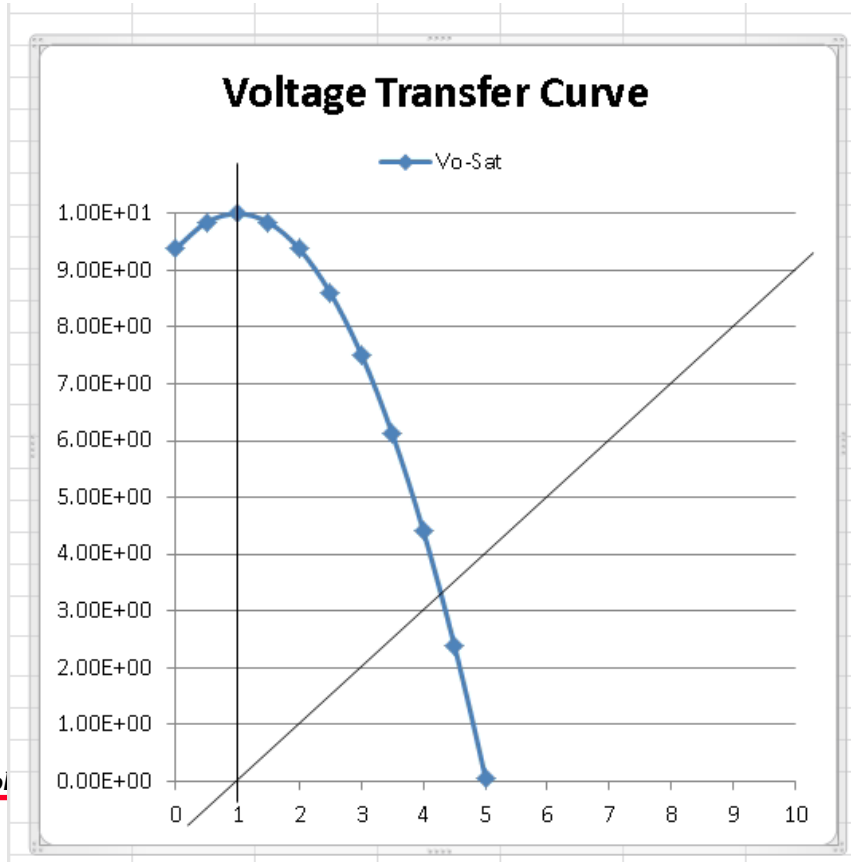
$$I_D = \frac{\mu W \, Cox' \, (Vg - Vt)^2}{2L}$$

$$Cox' = Cox/Area = \varepsilon o \varepsilon r / Xox$$

CALCULATION OF VTC

M1 in Saturation $V_{out} = V_{DD} - R I_D = V - R \frac{\mu W Cox'}{2L} (Vin-Vt)^2$

Cox' = Cox/Area = εoεr/Xox
εo = 8.85e-14 F/cm
εr=3.9 for oxide
Xox = gate oxide thickness
W= width of MOSFET
L=Length of MOSFET
Vt = Threshold Voltage



Vin	Vo-Sat
0	9.38E+00
0.5	9.84E+00
1	1.00E+01
1.5	9.84E+00
2	9.38E+00
2.5	8.60E+00
3	7.51E+00
3.5	6.12E+00
4	4.41E+00
4.5	2.39E+00
5	5.97E-02
5.5	-2.58E+00
6	-5.53E+00
6.5	-8.79E+00
7	-1.24E+01
7.5	-1.62E+01
8	-2.04E+01
8.5	-2.49E+01
9	-2.98E+01
9.5	-3.49E+01
10	-4.03E+01

CALCULATION OF VTC

M1 in Non-Saturation $V_{out} = V_{DD} - I_D R$

$$V_{out} = V_{DD} - I_D R = V_{DD} - \frac{R\,\mu W\,Cox'}{L}(V_g - V_t - V_d/2)V_d$$

$\frac{R\,\mu W\,Cox'}{L} \rightarrow Kx$

$$V_o = V_{DD} - R\,Kx(V_{in} - V_t - V_o/2)V_o$$

$$V_o = V_{DD} - R\,Kx(V_{in} - V_t)V_o - RKxV_o^2/2$$

$$0 = V_{DD} - R\,Kx(V_{in} - V_t - 1)V_o - RKxV_o^2/2$$

quadratic formula

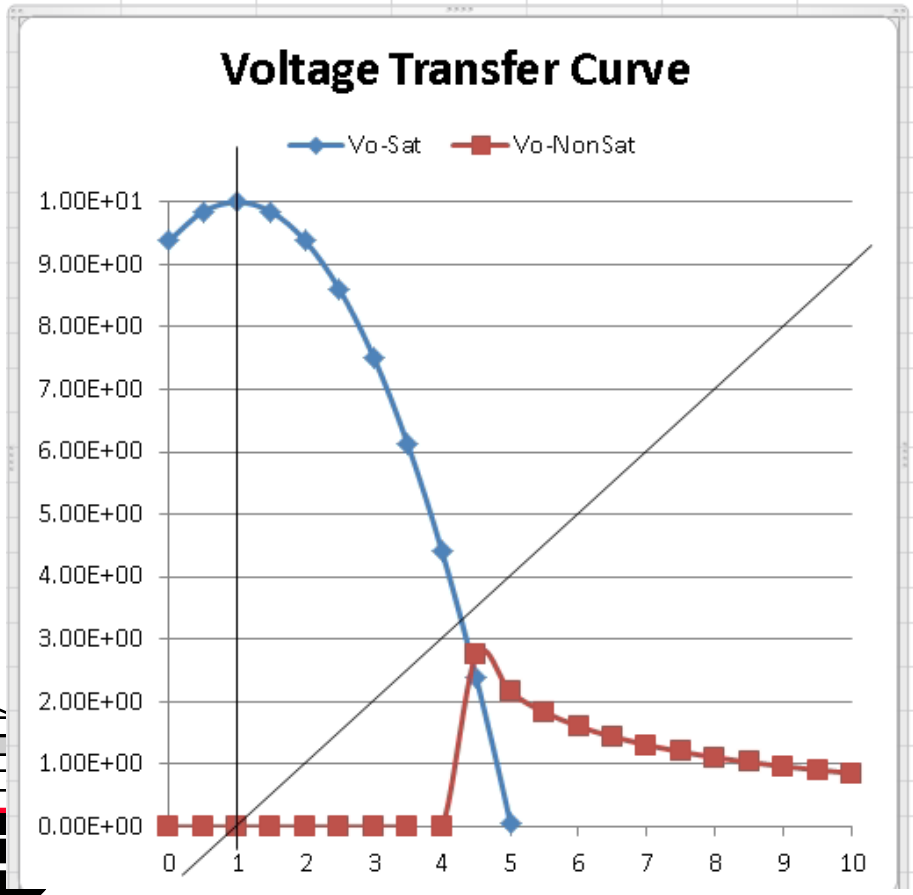
$$\mathbf{a\,x^2 + bx + c = 0}$$

$$\mathbf{x = -b \pm \sqrt{b^2 - 4ac}}$$

CALCULATION OF VTC

M1 in Non-Saturation Vout = b^2 +/- $\sqrt{b^2 - 2V_{DD}/KxR}$

b=(Vin – Vt + 1/KxR)



Vin	Vo-Sat	Vo-NonSat	b	ID - Sat
0	9.38E+00	#NUM!	-1.95E-01	6.21E-04
0.5	9.84E+00	#NUM!	3.05E-01	1.55E-04
1	1.00E+01	#NUM!	8.05E-01	0.00E+00
1.5	9.84E+00	#NUM!	1.30E+00	1.55E-04
2	9.38E+00	#NUM!	1.80E+00	6.21E-04
2.5	8.60E+00	#NUM!	2.30E+00	1.40E-03
3	7.51E+00	#NUM!	2.80E+00	2.49E-03
3.5	6.12E+00	#NUM!	3.30E+00	3.88E-03
4	4.41E+00	#NUM!	3.80E+00	5.59E-03
4.5	2.39E+00	2.74E+00	4.30E+00	7.61E-03
5	5.97E-02	2.16E+00	4.80E+00	9.94E-03
5.5	-2.58E+00	1.83E+00	5.30E+00	1.26E-02
6	-5.53E+00	1.61E+00	5.80E+00	1.55E-02
6.5	-8.79E+00	1.44E+00	6.30E+00	1.88E-02
7	-1.24E+01	1.31E+00	6.80E+00	2.24E-02
7.5	-1.62E+01	1.20E+00	7.30E+00	2.62E-02
8	-2.04E+01	1.11E+00	7.80E+00	3.04E-02
8.5	-2.49E+01	1.03E+00	8.30E+00	3.49E-02
9	-2.98E+01	9.67E-01	8.80E+00	3.98E-02
9.5	-3.49E+01	9.09E-01	9.30E+00	4.49E-02
10	-4.03E+01	8.58E-01	9.80E+00	5.03E-02

CALCULATION OF VTC

R INSTITUTE OF TECHNOLOGY — NMOS-Resistor-VTC.xls
CTRONIC ENGINEERING — 10/4/2014

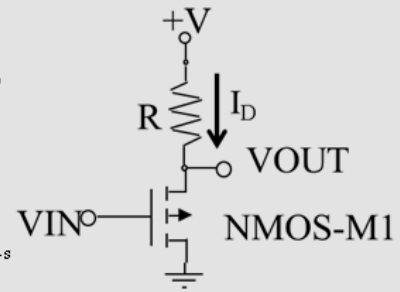
ION OF VOLTAGE TRANSFER CURVE — Dr. Lynn Fuller

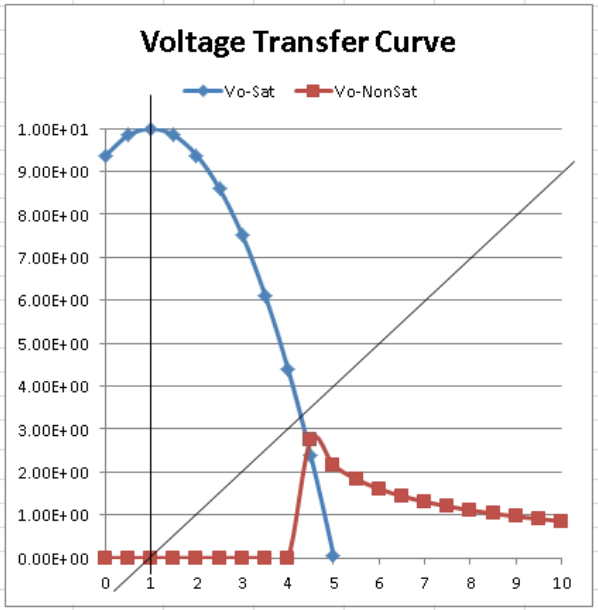
spreadsheet change the values in the white boxes. The rest of the sheet is protected and should not be changed unless
e of the consequences. The calculated results are shown in the purple boxes.

TS		VARIABLES			CHOICES	
					1=yes, 0=No	
8.85E-14	F/cm	Vt =	1.00E+00	volts	Saturation Equation	0
11.7		W =	20.00	um	Non Saturation Equation	1
3.9		L =	2.00	um		
		V=	10	volts		
		R=	1000	ohms		
		uo=	300	$cm^2/v\text{-}s$		
		Xox =	250	Å		

cm2/v-s

µm
µm





TIONS:

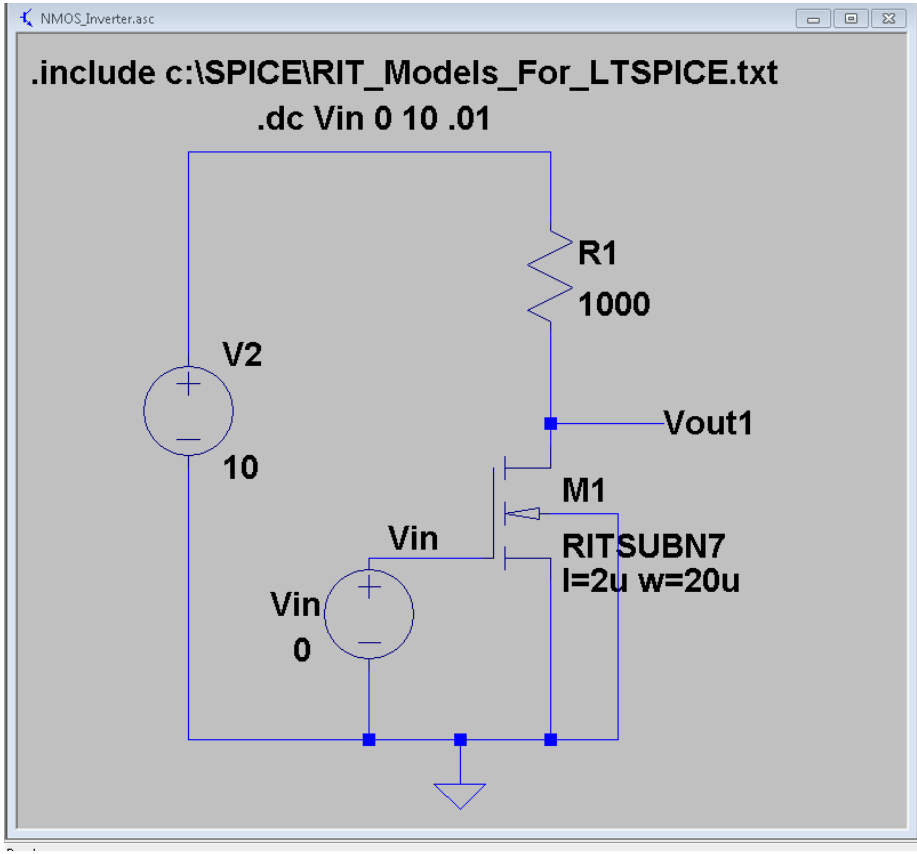
		RESULTS	
OXIDE CAPACITANCE / CM^2	=	4.14E-07	F/cm^2
Kp = u Cox'	=	1.24E-04	A/V^2
DRAIN CURRENT, ID	=	0.00012425	A
Kp W/L	=	0.00124254	A

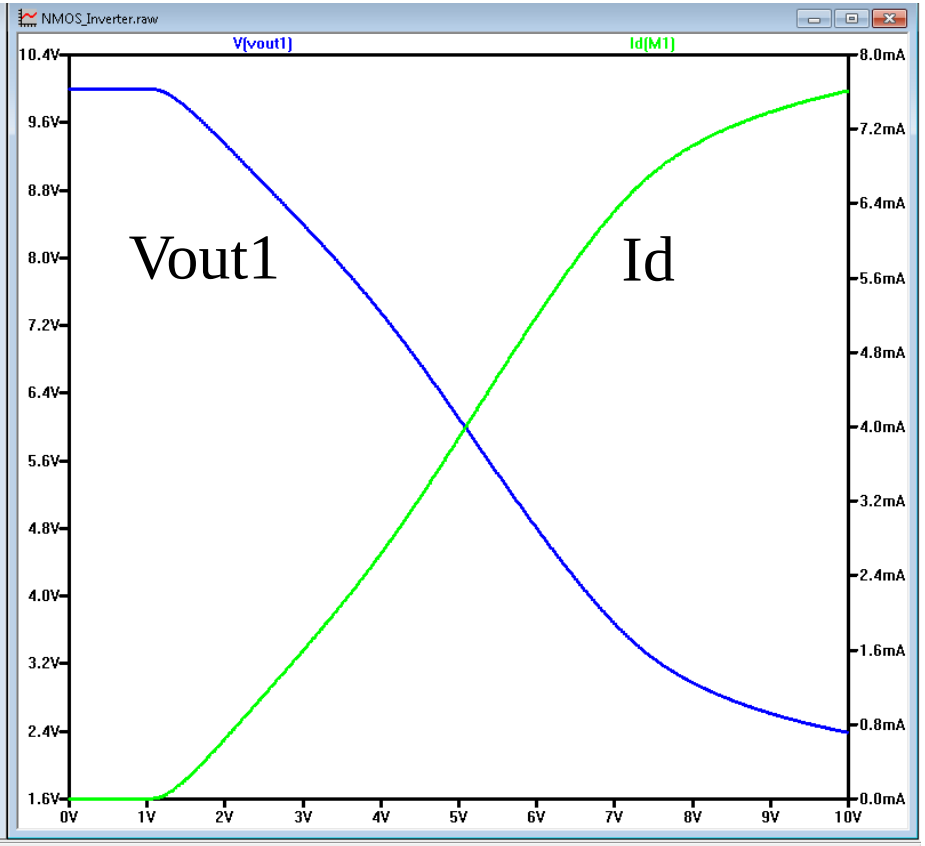
$Id = \mu W Cox'/L \ (Vgs-Vt-Vd/2)Vd$ in Non Saturation Region

$Id = \mu W Cox' / 2L \ (Vgs - Vt)^2$ in Saturation Region

Note: Equations only valid in specific regions

LTSPICE – RESISTOR LOAD INVERTER - VTC





CALCULATION OF NOISE MARGINS

Approach

Take derivative set equal to -1

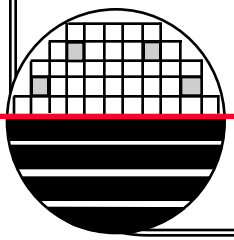
find VIL and VIH

VOH and VOL

Find point where Vin = Vout

Find I

Find Power

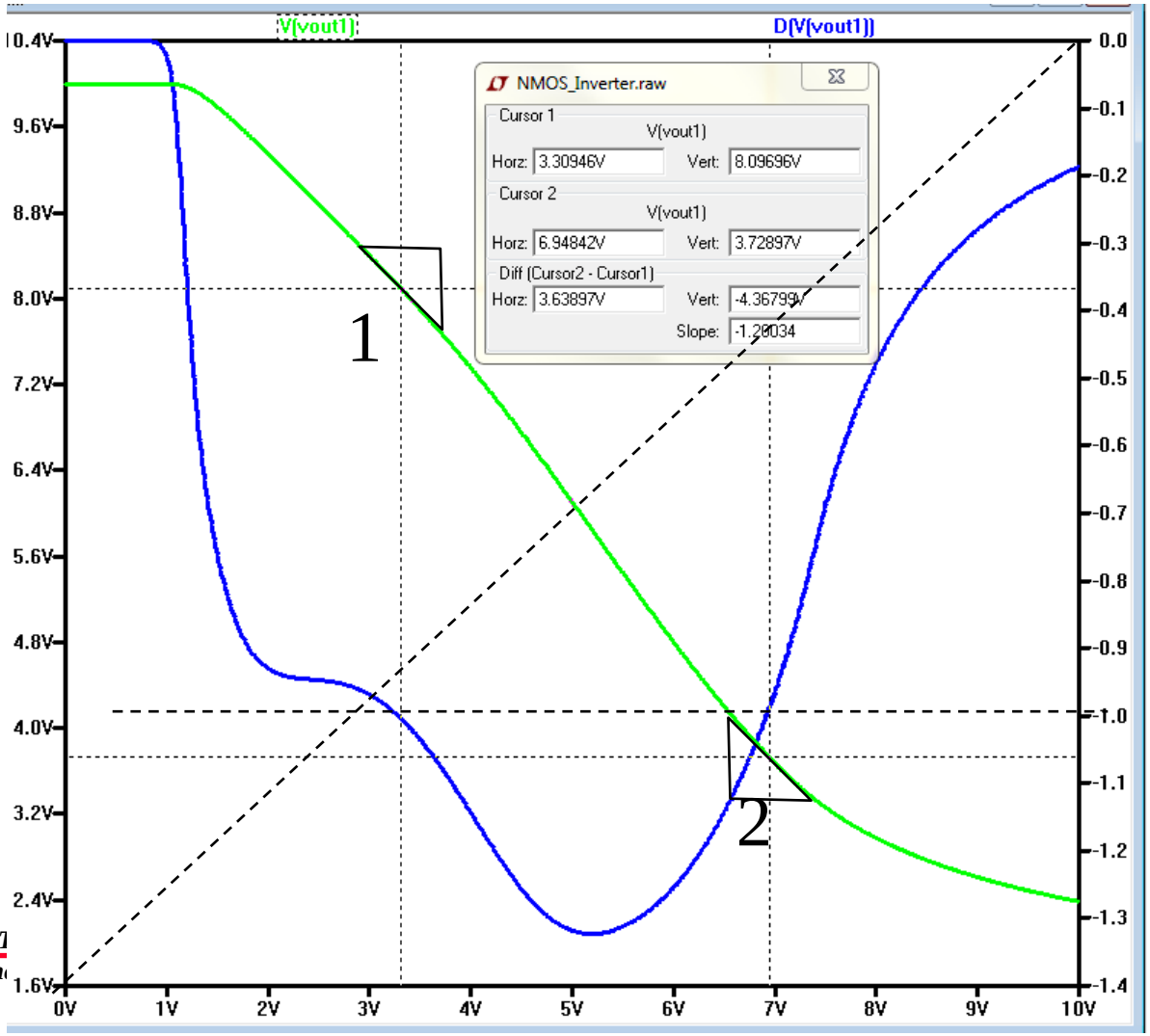


SPICE CALCULATIONS FOR NOISE MARGINS

RL = 1K

VIL = 3.31
VIH = 6.95
VOH = 8.09
VOL = 3.37
Δ0 = VIL – VOL
=3.31-3.73= -0.42
Δ1=VOH-VIH=
=8.09-6.95=1.14

Max Gain = -1.32

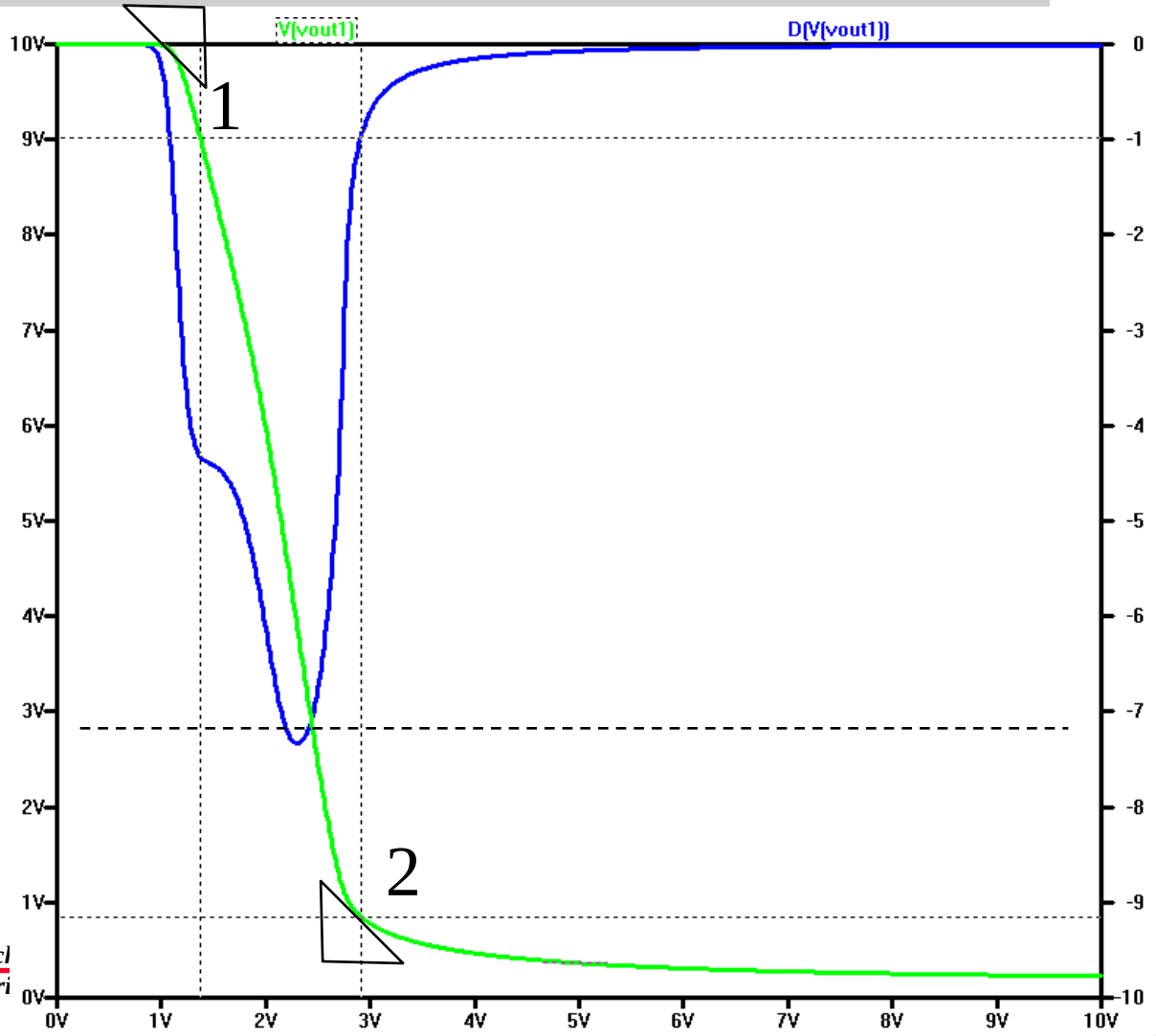


SPICE CALCULATIONS FOR NOISE MARGINS

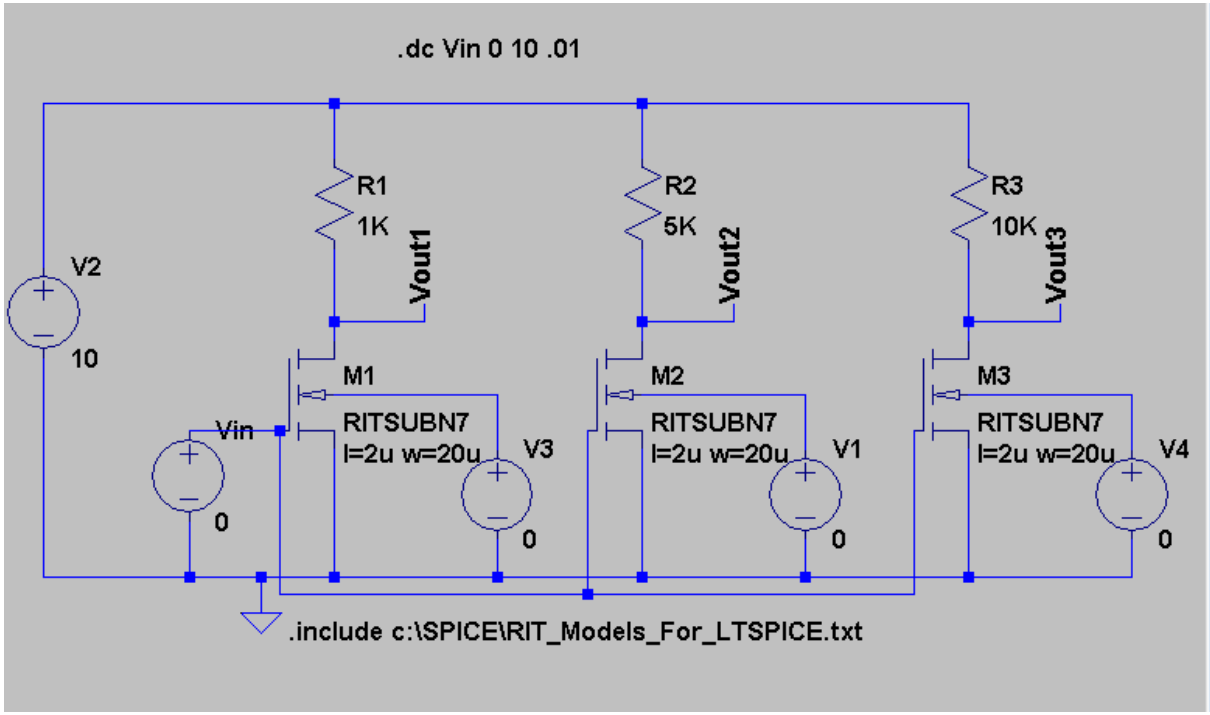
RL = 10K

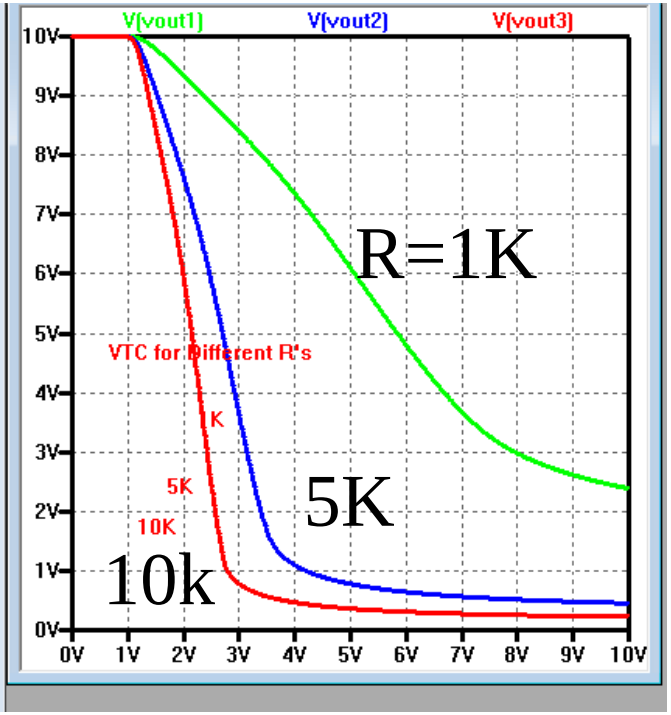
VIL = 1.0
VIH = 2.91
VOH = 10.0
VOL = 0.91
Δ0 = VIL – VOL
=1.0-0.91= 0.08
Δ1=VOH-VIH=
=10-2.91=7.09

Max Gain = -7.2

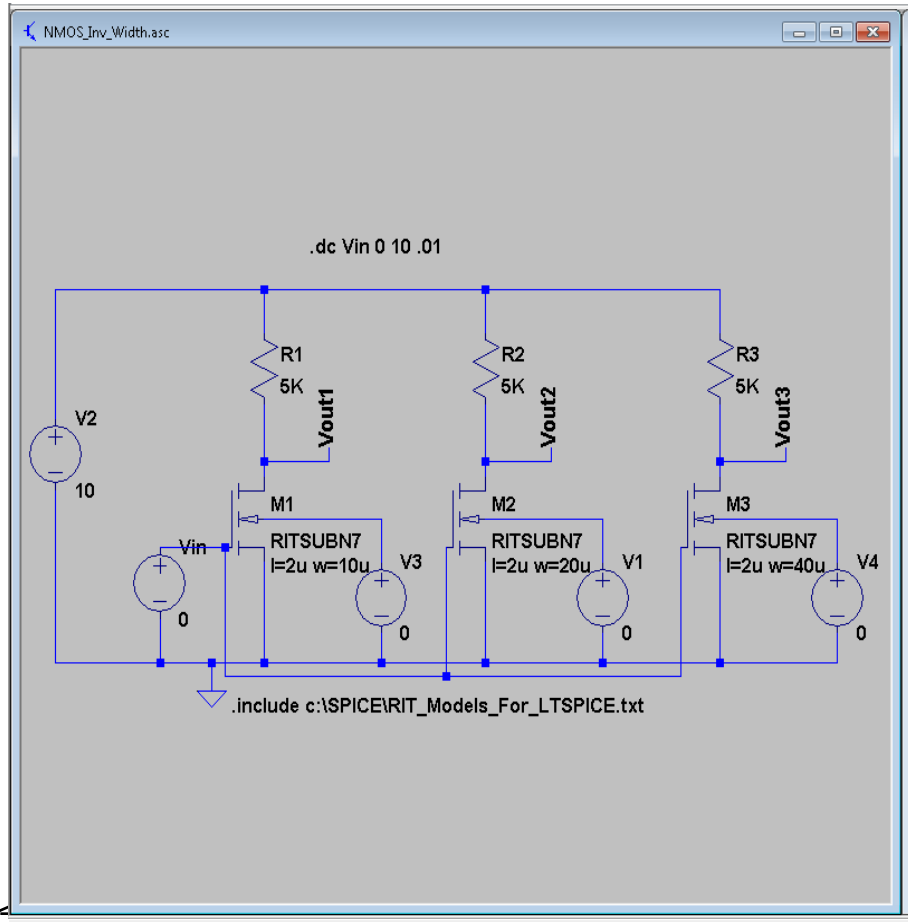


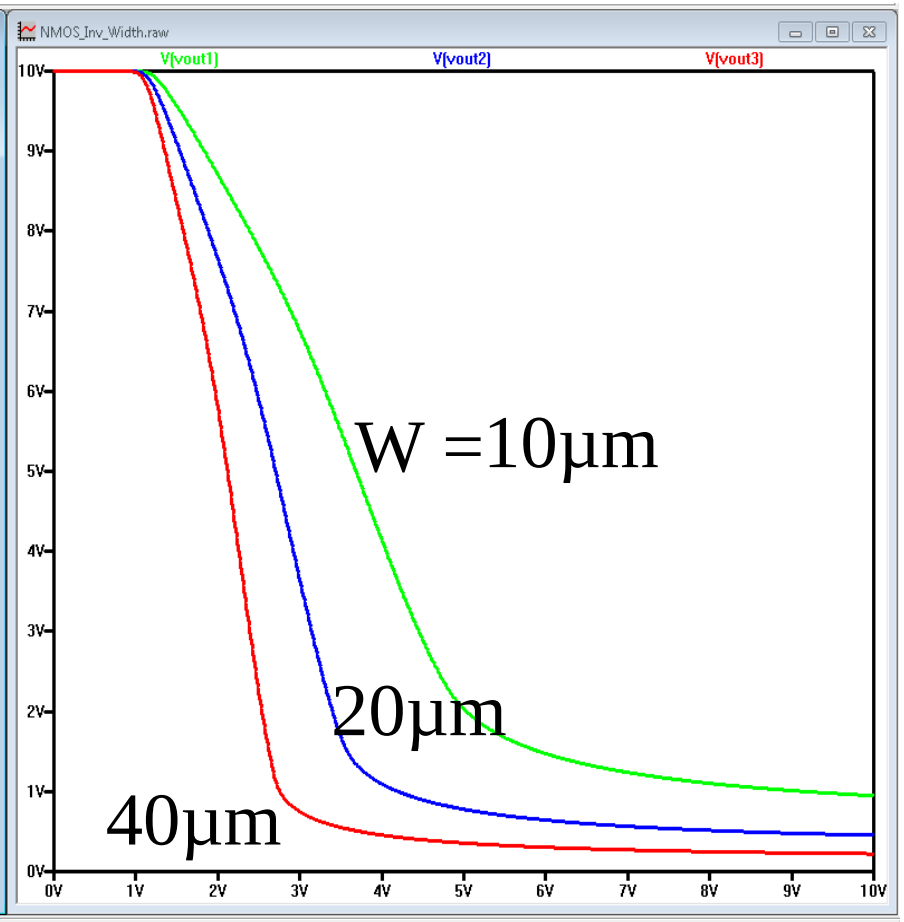
LTSPICE - INVERTER VTC – FOR DIFFERENT RL



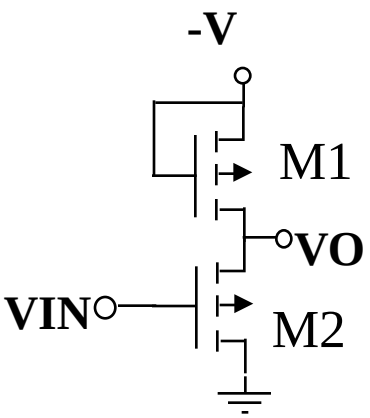


LTSPICE – INVERTER VTC FOR DIFFERENT W

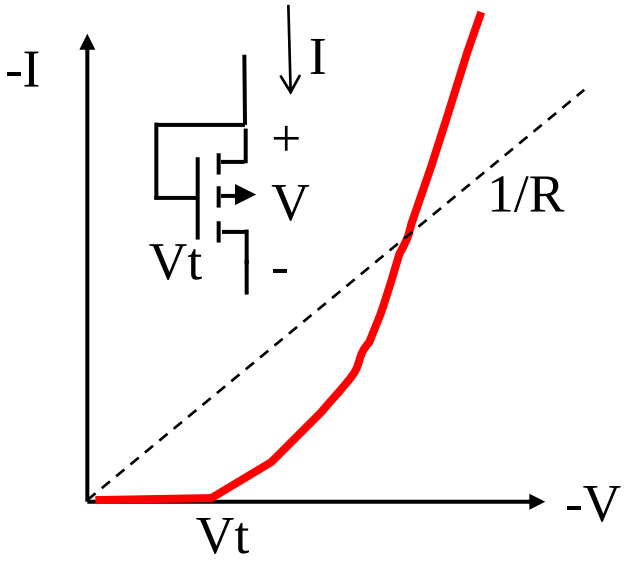




VTC PMOS INVERTER- PMOS ENHANCEMENT LOAD



PMOS ENHANCEMENT LOAD



$$\text{Gain} = \sqrt{\frac{W2/L2}{W1/L1}}$$

M2 is the switch and M1 is the load. The load limits the current when M2 is on. The load could be a resistor but a PMOS transistor with gate connected to the drain is smaller in size and also limits current. See the I-V characteristics. In the first quadrant the transistor approximates the resistor. However, Vout high is below VDD by the threshold voltage of M1

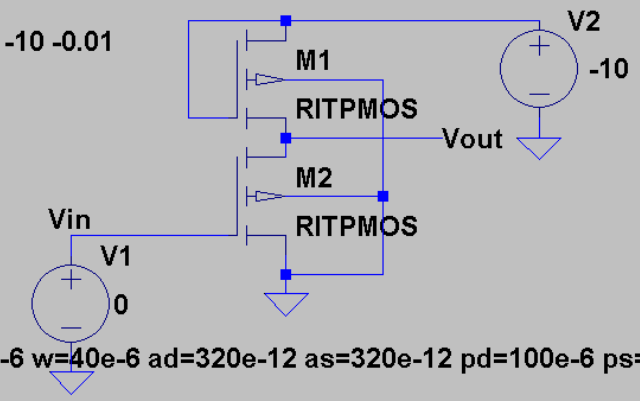
VTC PMOS INVERTER- PMOS ENHANCEMENT LOAD

PMOS-Inverter.asc

Note: Supply and input V is negative

I=40e-6 w=20e-6 ad=320e-12 as=320e-12 pd=100e-6 ps=100e-6

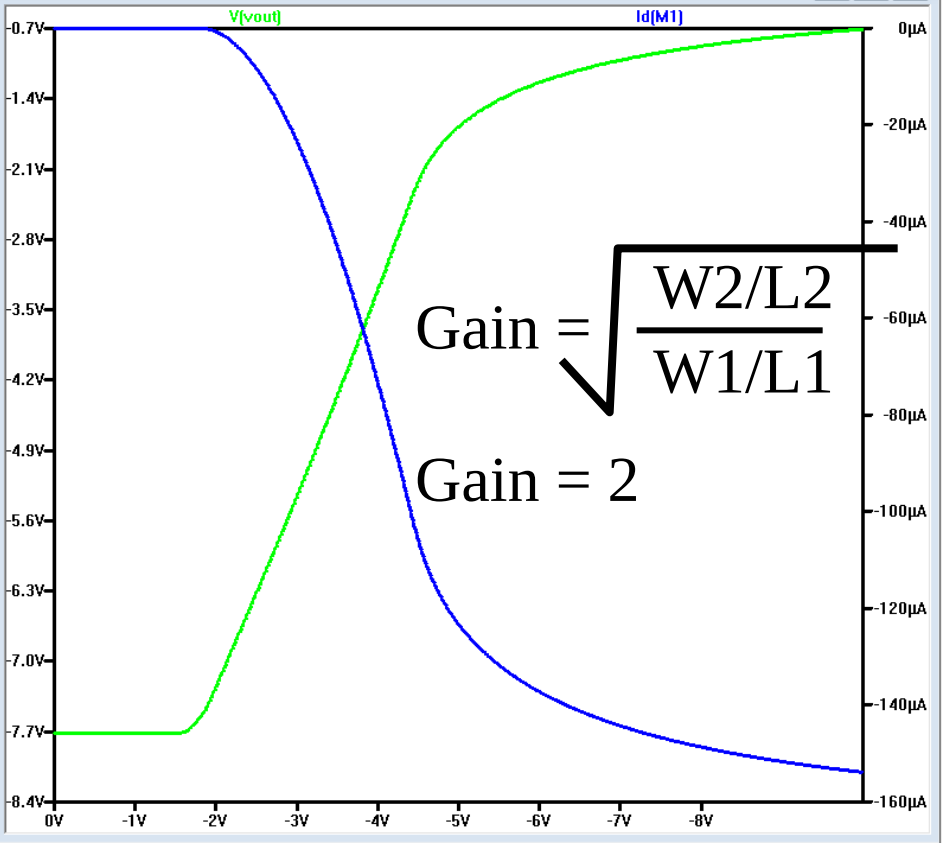
.dc V1 0 -10 -0.01



I=20e-6 w=40e-6 ad=320e-12 as=320e-12 pd=100e-6 ps=100e-6

```
.MODEL RITPMOS PMOS (LEVEL=7 VERSION=3.1 CAPMOD=2 MOBM
+TOX=5.0E-8 XJ=3E-6 NCH=1.00E15 NSUB=1.00E15 PCLM=5
+WINT=2.0E-7 LINT=2.26E-6 NGATE=5E20 VTH0=-1.77
+RSH=120 JS=3.35E-7 JSW=3.35E-7 CJ=1.8E-4 MJ=0.5 PB=0.88
+CJSW=4.97E-10 MJSW=0.5 PBSW=0.88
+CGSO=1.09E-10 CGDO=1.09E-10 CGBO=6.90E-10 )
```

PMOS-Inverter.raw



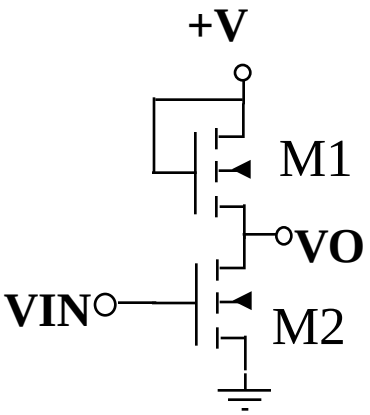
$$\text{Gain} = \sqrt{\frac{W2/L2}{W1/L1}}$$

Gain = 2

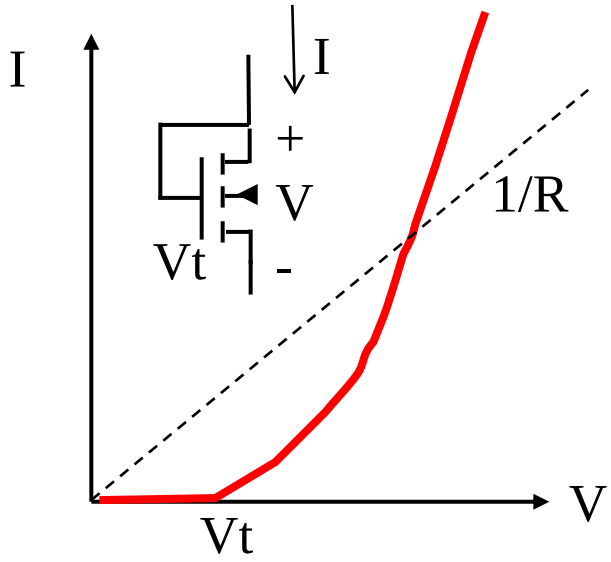
-10 Volts is Logic High

0 Volts is Logic Low

VTC NMOS INVERTER- NMOS ENHANCEMENT LOAD



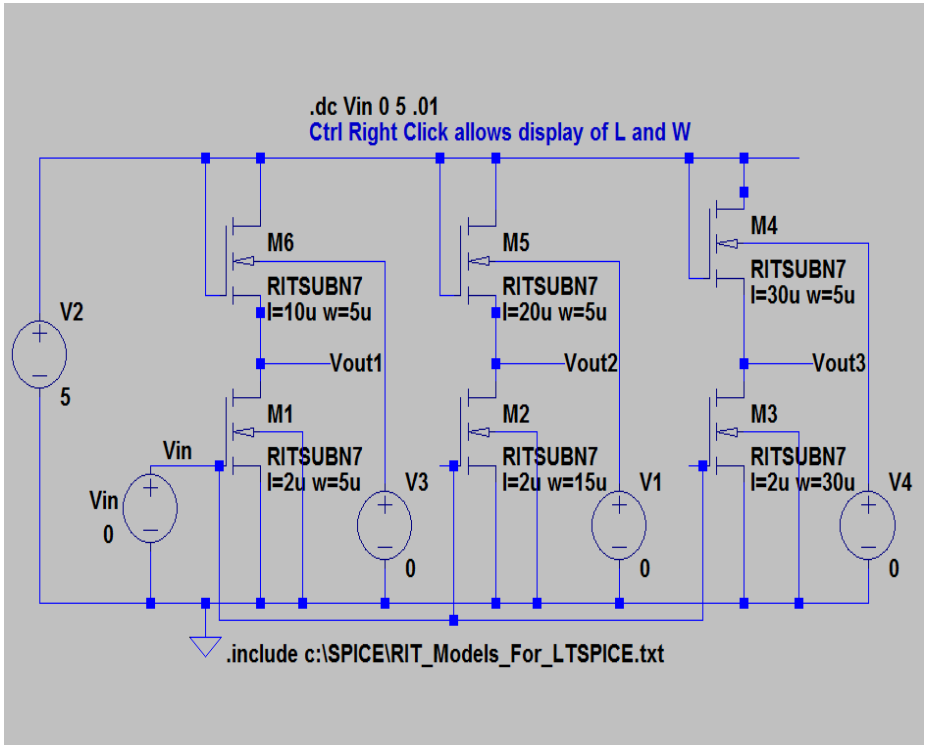
NMOS ENHANCEMENT LOAD

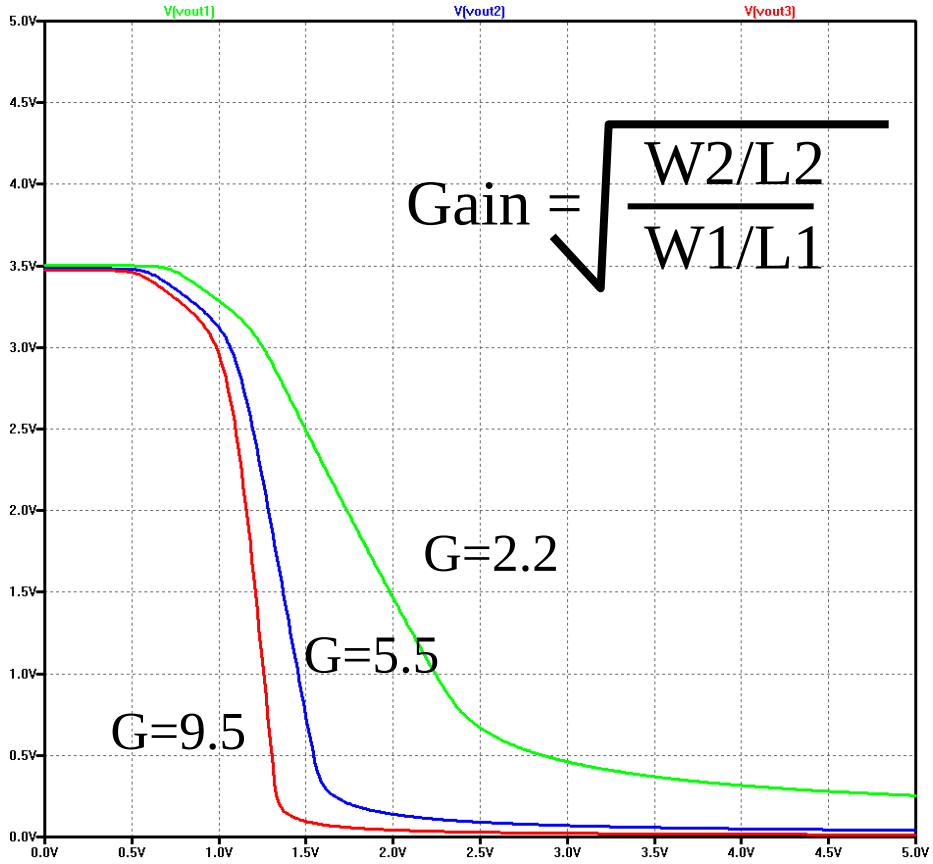


$$\text{Gain} = \sqrt{\frac{W2/L2}{W1/L1}}$$

M2 is the switch and M1 is the load. The load limits the current when M2 is on. The load could be a resistor but an NMOS transistor with gate connected to the drain is smaller in size and also limits current. See the I-V characteristics. In the first quadrant the transistor approximates the resistor. However, Vout high is below VDD by the threshold voltage of M1

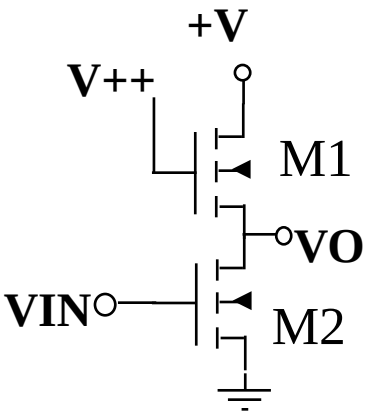
VTC NMOS INVERTER- NMOS ENHANCEMENT LOAD





Note: increasing L of the load is equivalent to increasing R of a resistor load, Vout high is Vdd – Vt_{M1} , Gain is shown.

VTC NMOS INVERTER- NMOS ENHANCEMENT LOAD AND V++ GATE BIAS

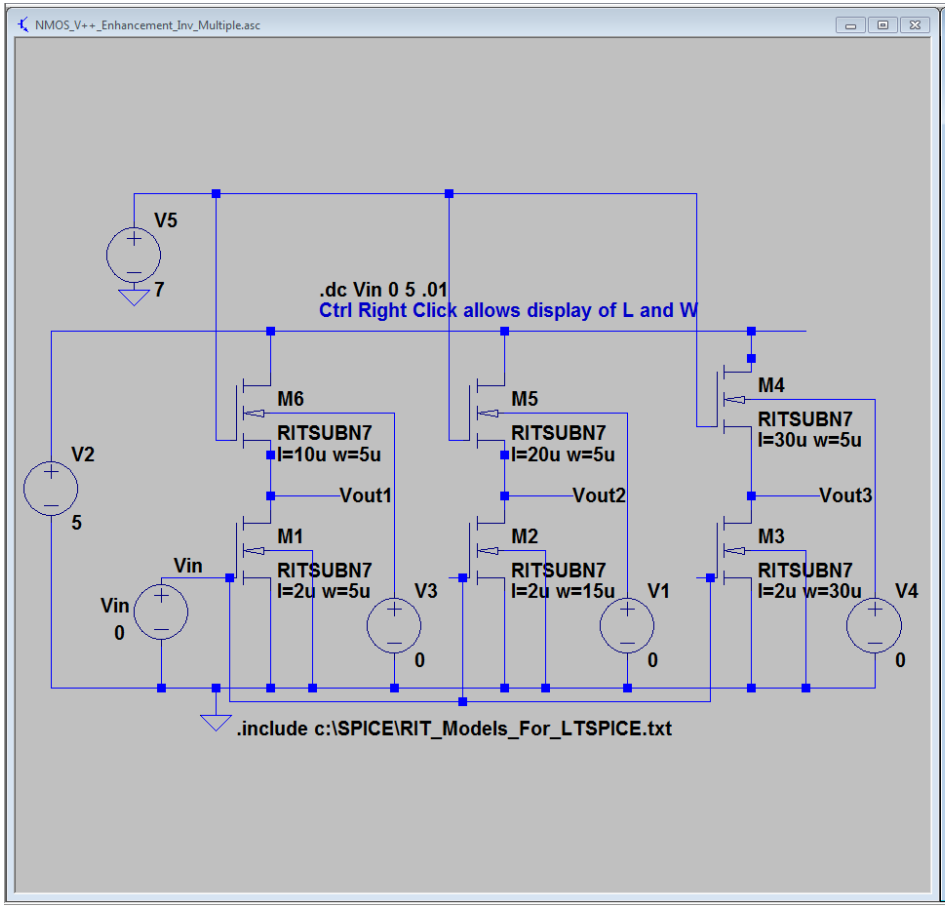


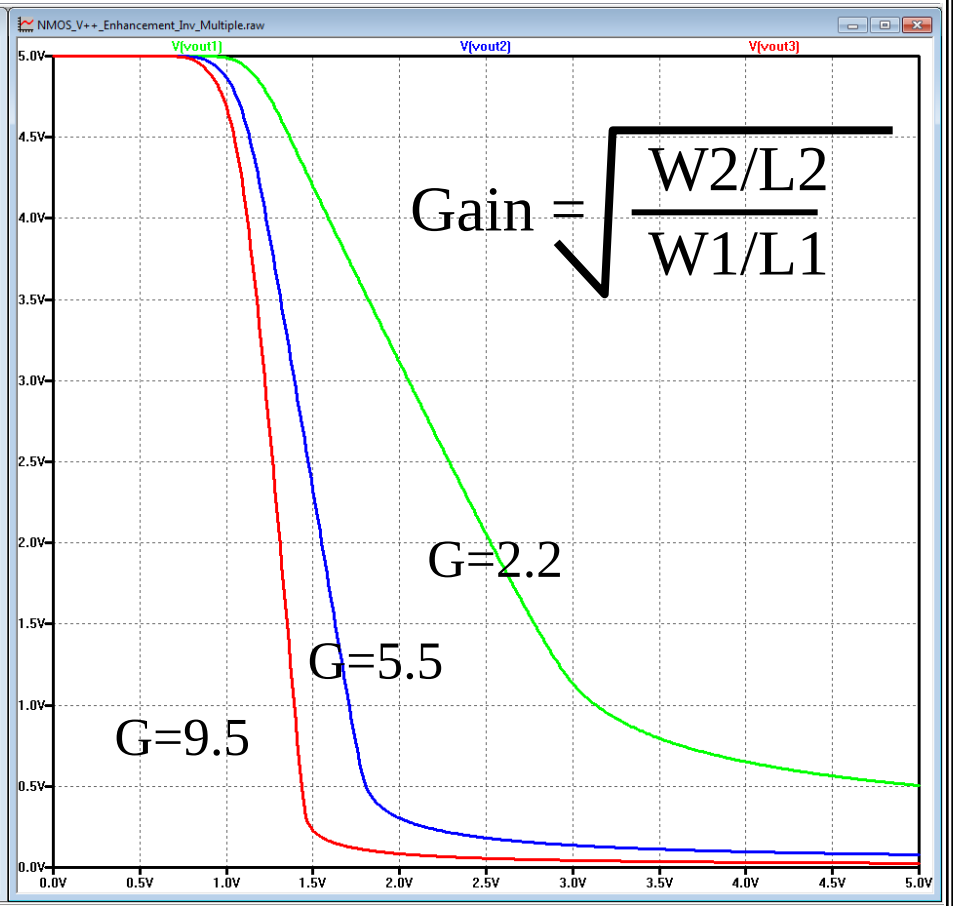
NMOS ENHANCEMENT LOAD V++ GATE BIAS

$$\text{Gain} = \sqrt{\frac{W2/L2}{W1/L1}}$$

M2 is the switch and M1 is the load. The load limits the current when M2 is on. The load could be a resistor but an NMOS transistor with gate connected to the drain is smaller in size and also limits current. See the I-V characteristics. In the first quadrant the transistor approximates the resistor. M1 is always on because the gate voltage is above the supply voltage. Vout max is the supply voltage.

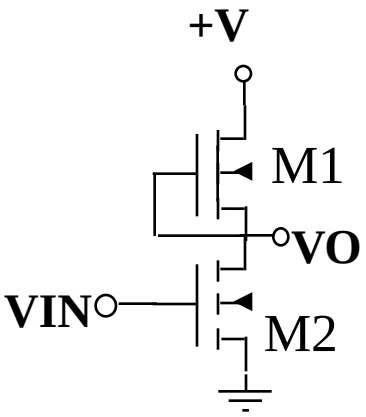
VTC NMOS INVERTER- NMOS ENHANCEMENT LOAD AND V++ GATE BIAS



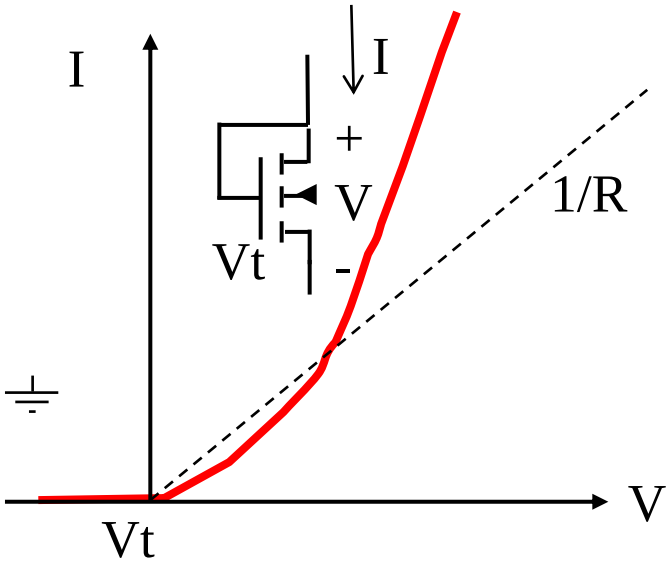


Note: increasing L of the load is equivalent to increasing R of a resistor load, Vout high is Vdd, Gain is shown.

VTC NMOS INVERTER – NMOS DEPLETION LOAD



NMOS DEPLETION LOAD



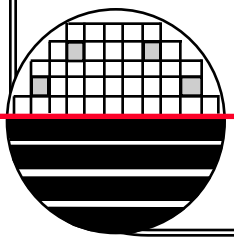
$$\text{Gain} = \sqrt{\frac{W2/L2}{W1/L1}}$$

M2 is the switch and M1 is the load. The load limits the current when M2 is on. The load could be a resistor but an NMOS transistor with gate connected to the drain is smaller in size and also limits current. See the I-V characteristics. In the first quadrant the transistor approximates the resistor. M1 is always on because its threshold voltage is set to zero or slightly negative by ion implant.

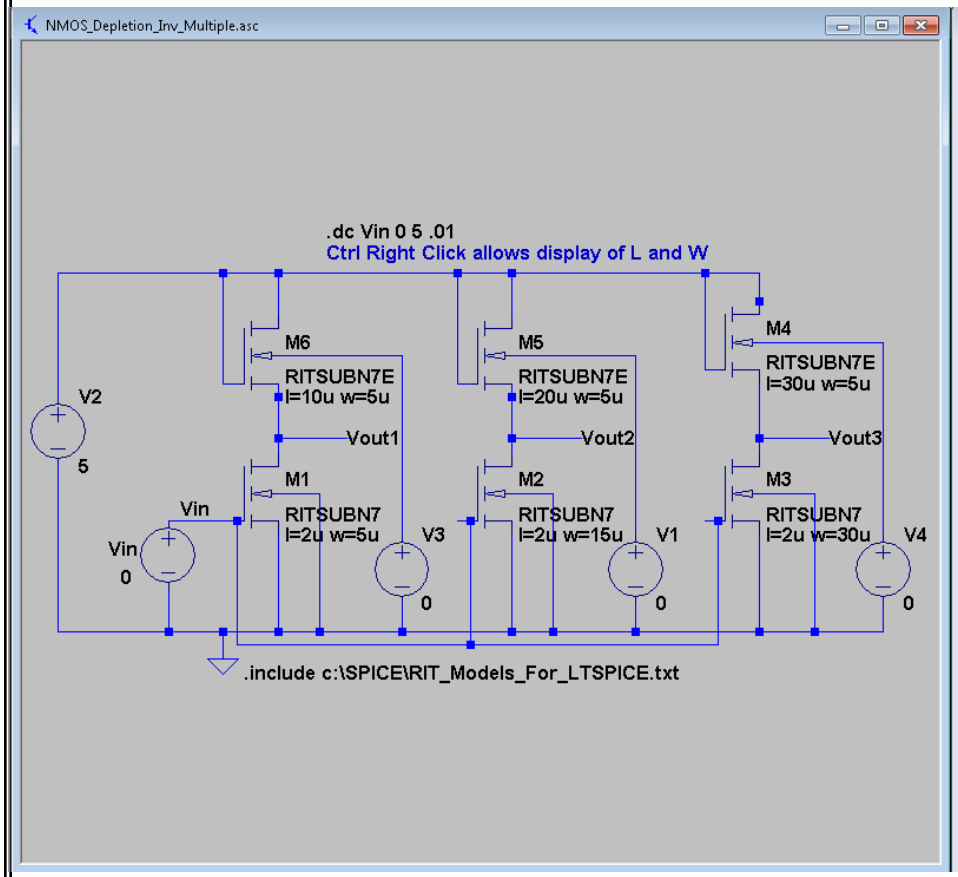
VTC NMOS INVERTER – NMOS DEPLETION LOAD

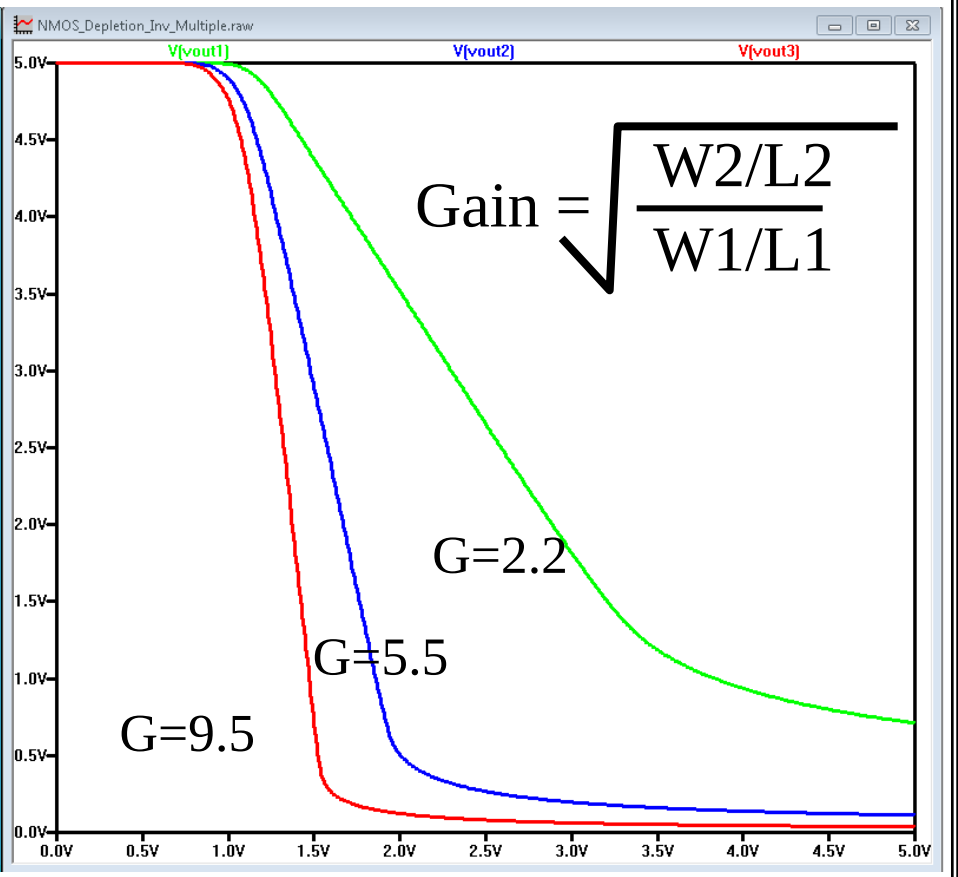
* From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL **RITSUBN7E** NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=**-1.0** U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)

Need a new SPICE model for the Enhancement mode NMOS. New model name and negative VTH0. Using ion implant the VTH0 can be made negative.



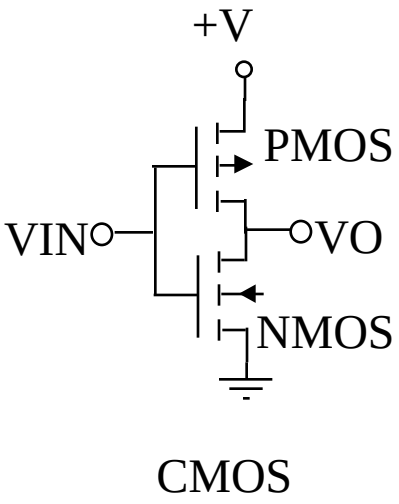
VTC NMOS INVERTER – NMOS DEPLETION LOAD



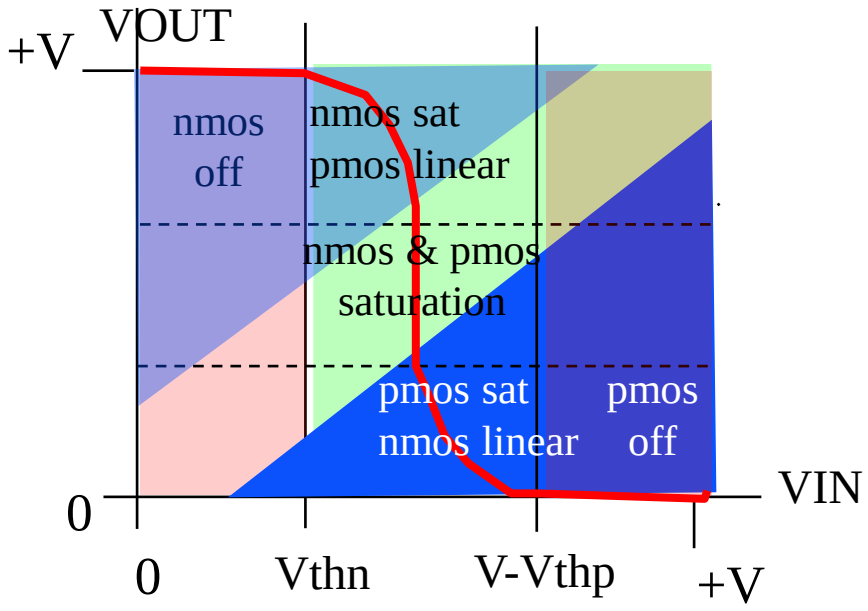


Note: increasing L of the load is equivalent to increasing R of a resistor load, Vout high is Vdd, Gain is shown.

CMOS - CALCULATION OF VTC



CMOS



First figure out if the transistor is

sub-threshold or off, Vgs < Vth and Vgd < Vth

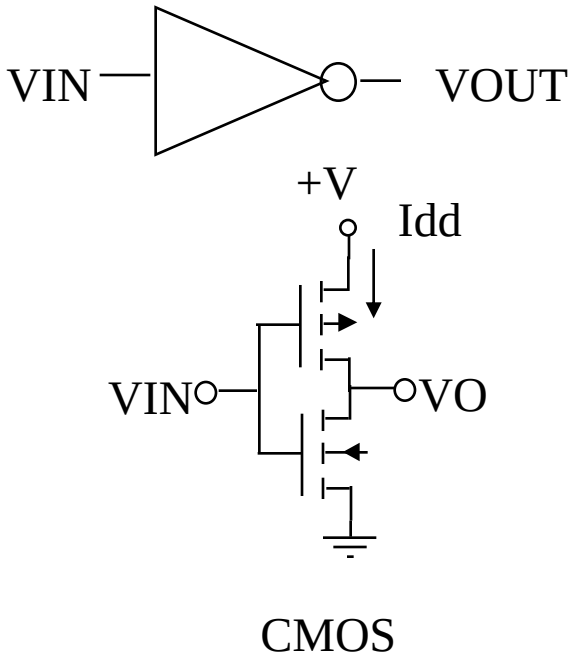
non-saturation, Vgs > Vth and Vgd > Vth

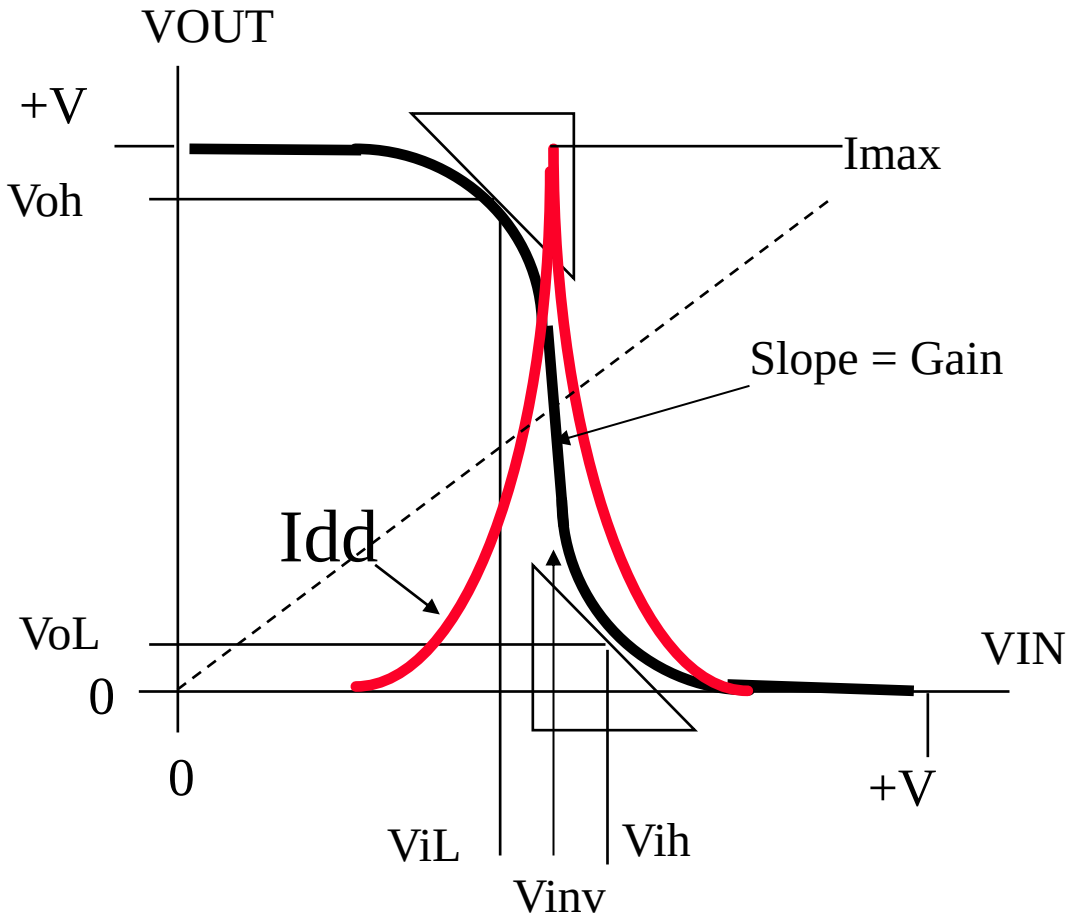
saturation region, Vgs > Vth and Vgd < Vth

Note: Vin = Vgs, Vout = Vds, therefore Vgd = Vin-Vout

Vth might be +1volt

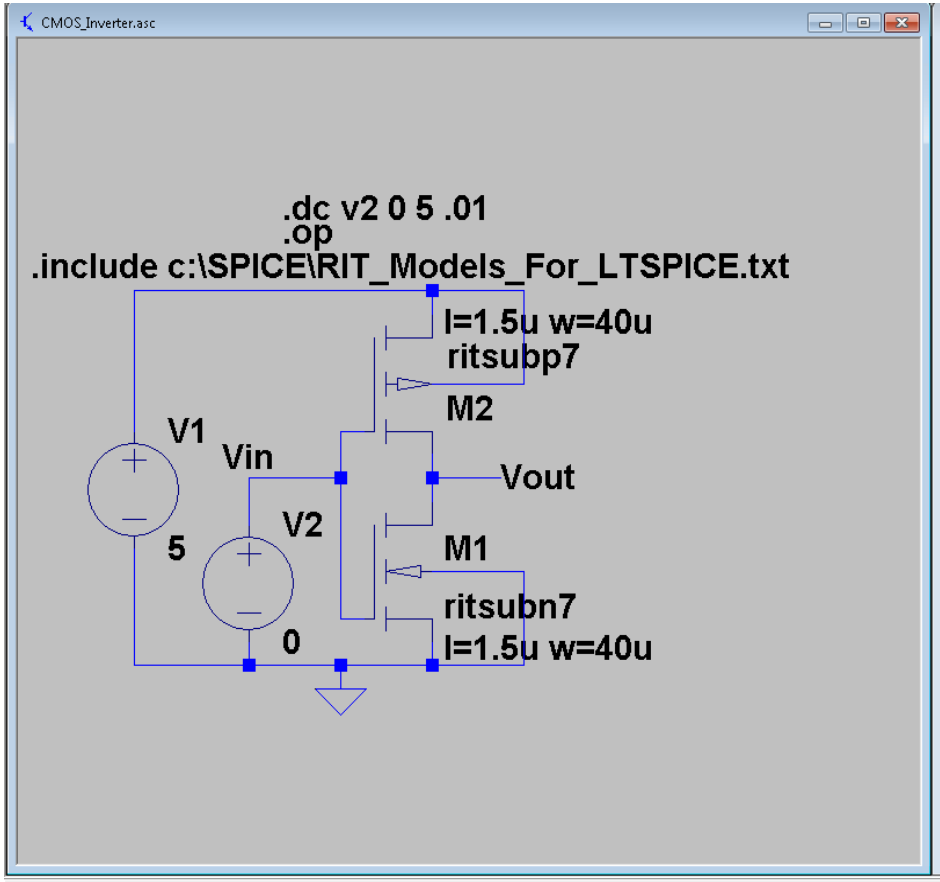
CMOS INVERTER

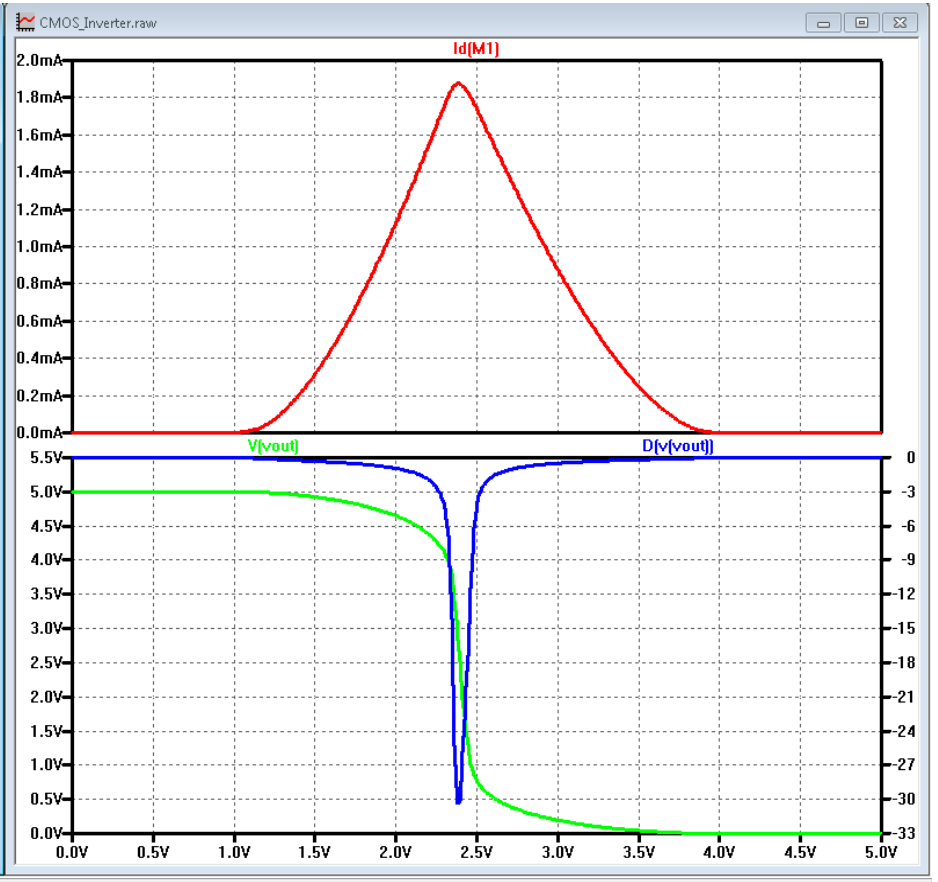




NML, noise margin low, Δ0 =ViL-VoL
NMH, noise margin high, Δ1 =VoH-ViH

LTSPICE – CMOS INVERTER



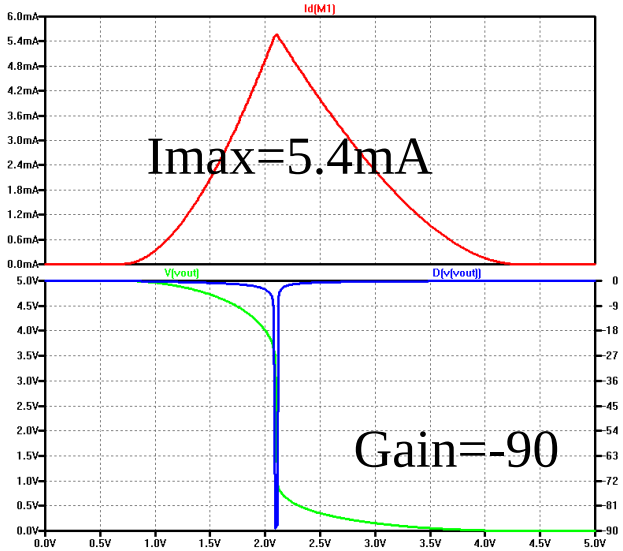


NML, noise margin low, $\Delta 0$ =ViL-VoL = 2.2-0.5 = 1.7

NMH, noise margin high, $\Delta 1$ =VoH-ViH = 4.5-2.5 = 2.0

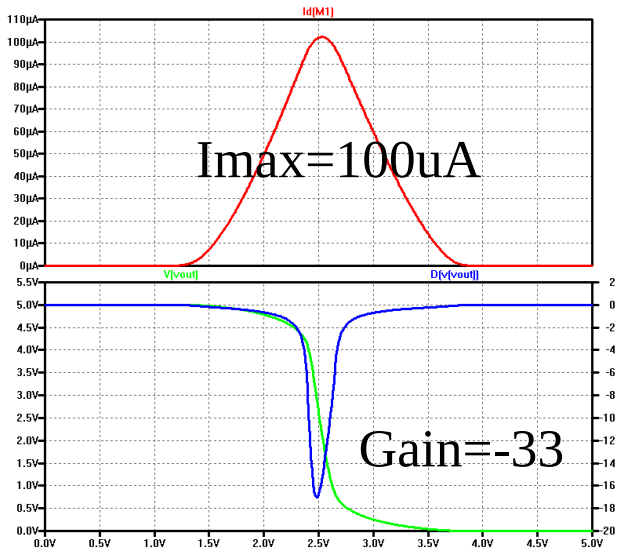
COMPARISON OF 10u, 1u AND 100n CMOS INVERTERS

VDD = 5 volts



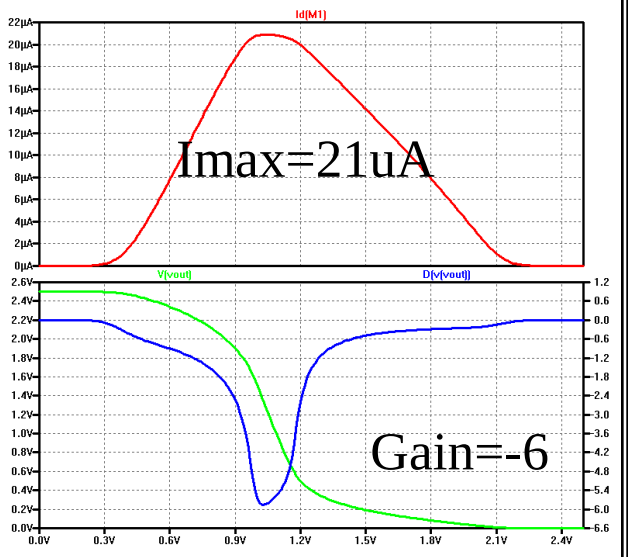
RITALDN3/RITALDP3
L=10u W=880u
L=10u W=880u

VDD = 3.3 volts



RITSUBN7/RITSUBP7
Ln=1u Wn=2u
Lp=1u Wp=2u

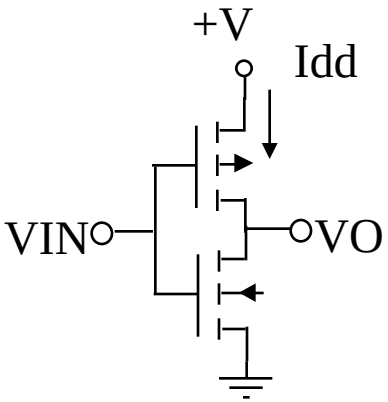
VDD = 2.5 volts



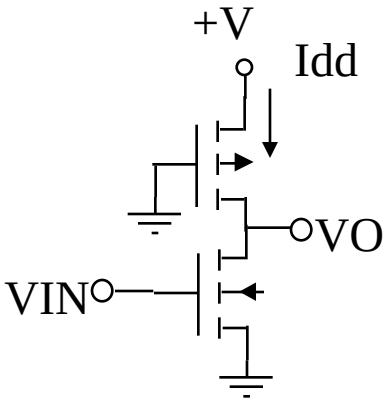
EECMOSN/EECMOSP
Ln=180n Wp=200n
Ln=180n Wp=200n

PSEUDO – CMOS

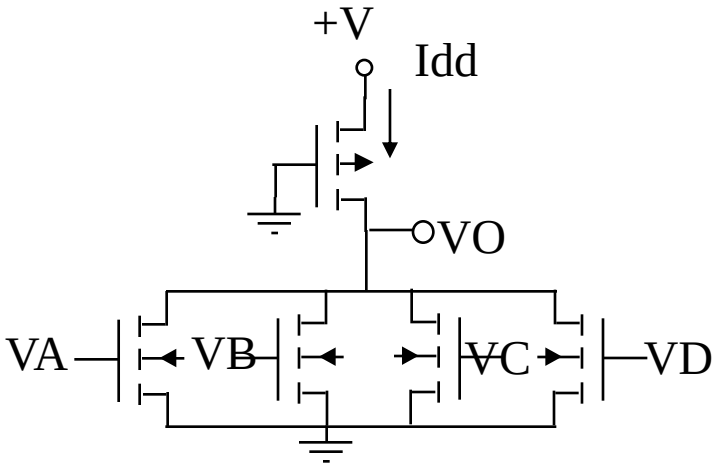
There are situations where we want a large number of inputs. Rather than have CMOS where there will be many transistors in series (which will not work) we can use a single PMOS transistor that is always on.



CMOS

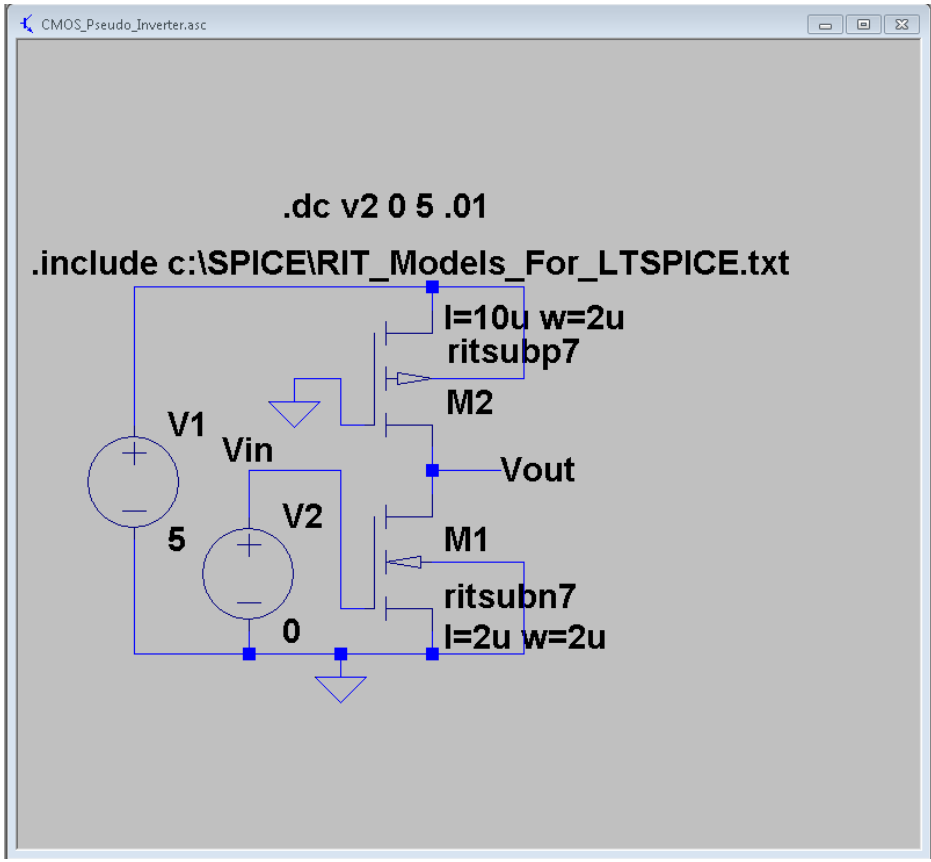


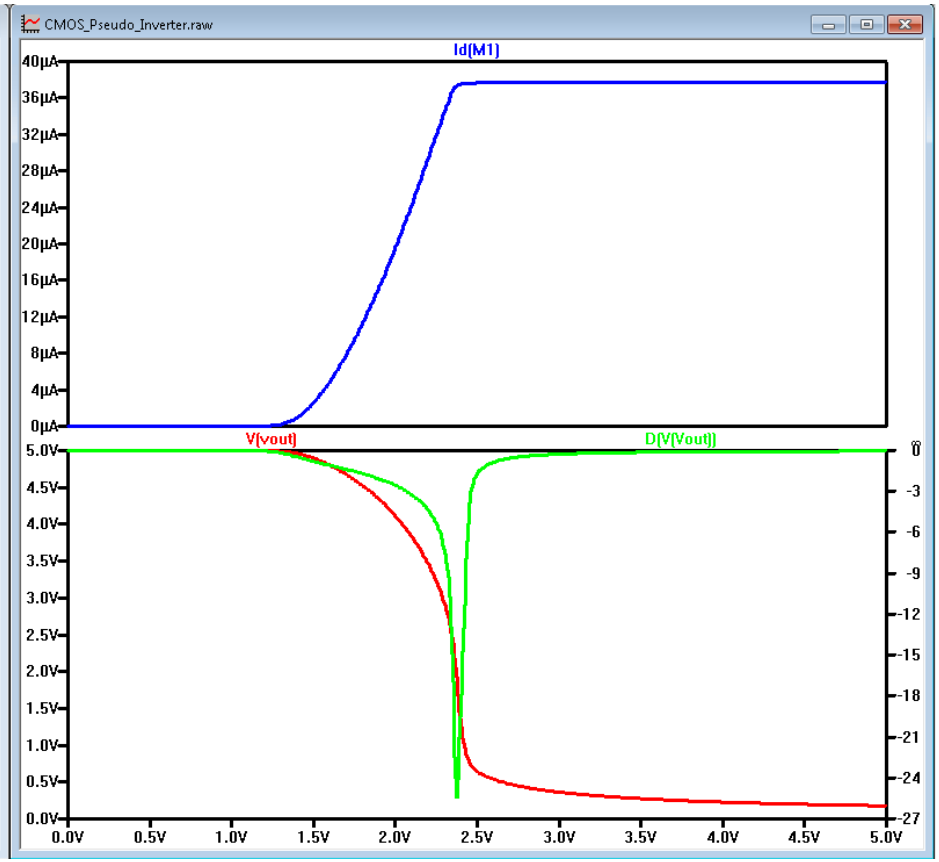
Pseudo NMOS Inverter



4 Input NOR

PSEUDO – CMOS INVERTER

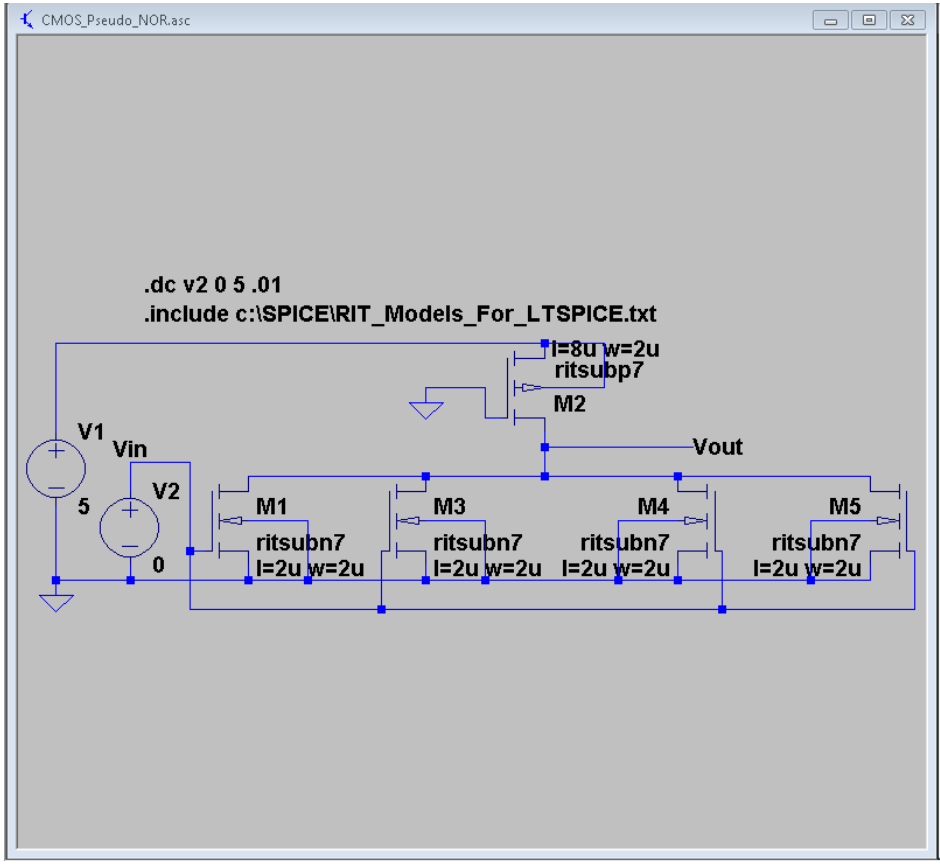


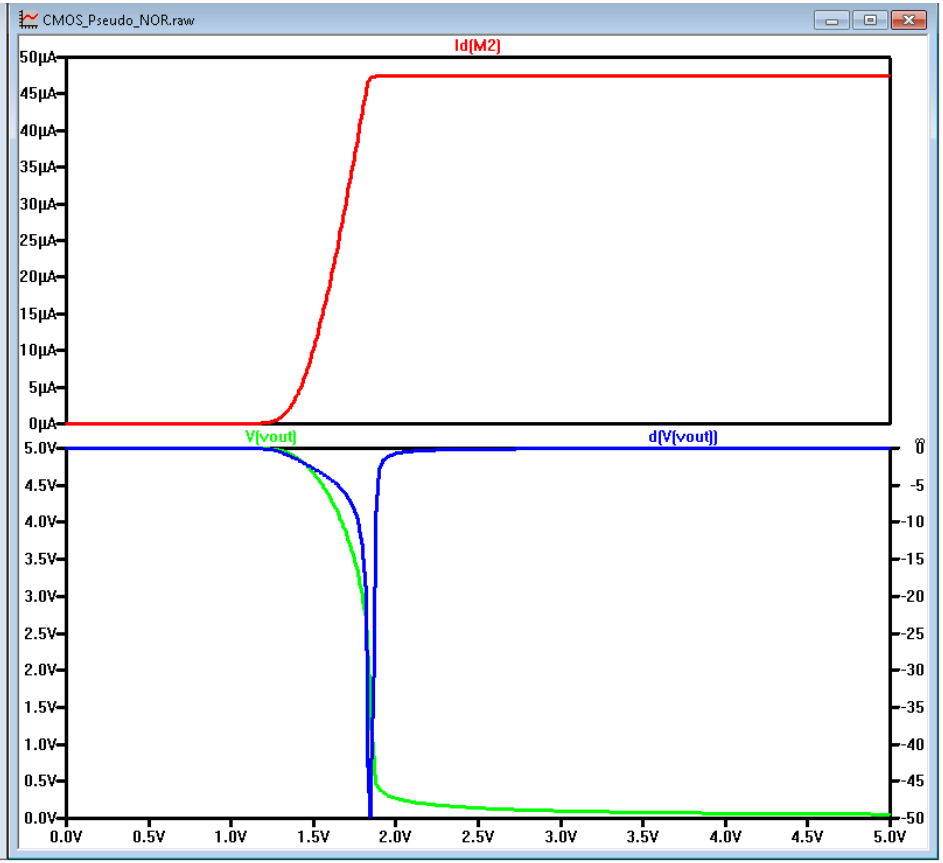


No advantages over CMOS inverter

$\Delta 0 = 1.0$, $\Delta 1 = 3.0$

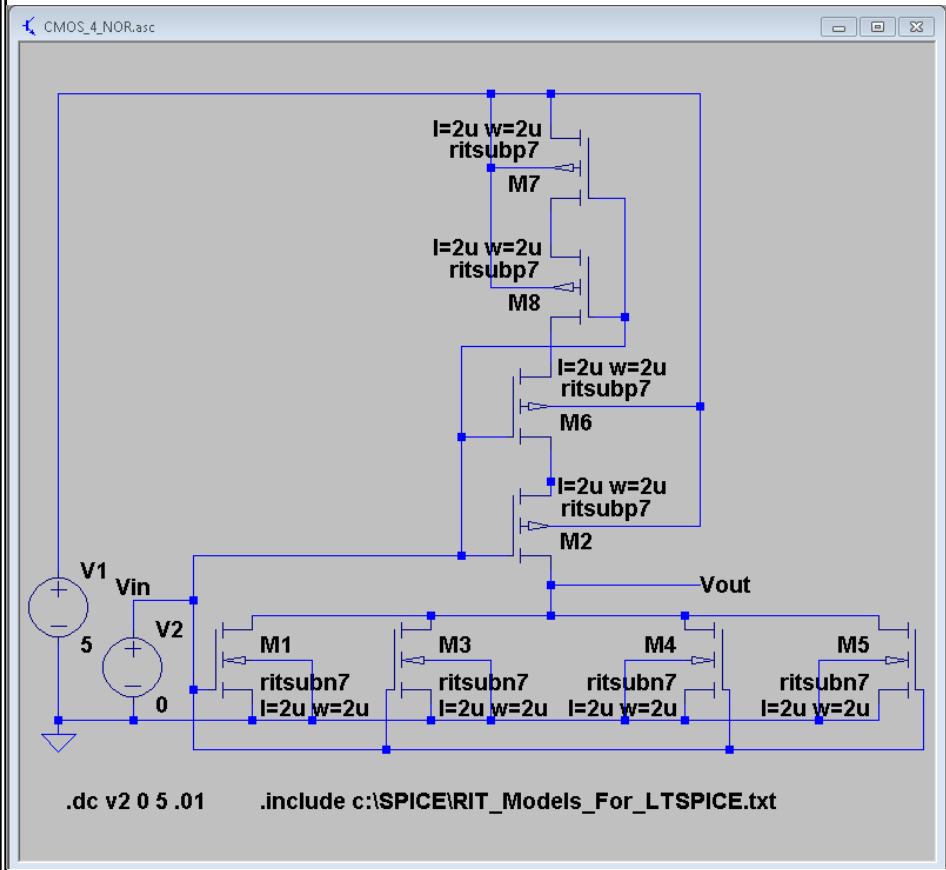
PSEUDO – CMOS NOR

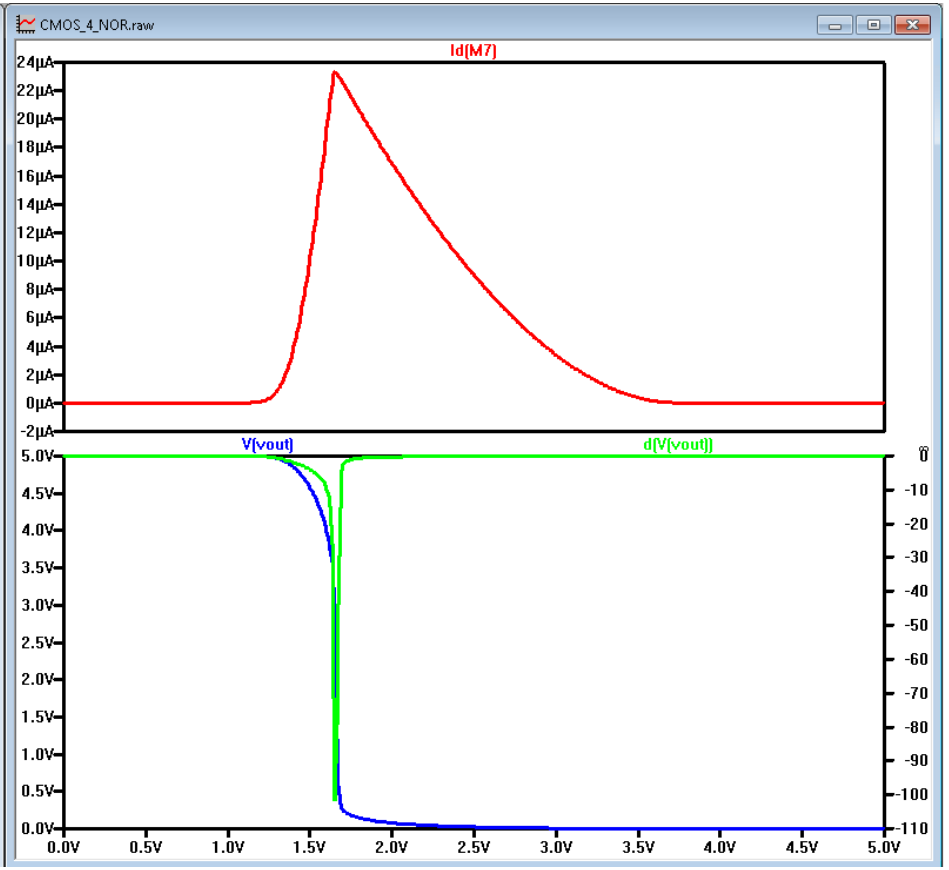




Note: noise margin ~ Δ0=1.3 , Δ1=2.8
max current drive 50uA
static current not zero for Vout=low
gate delay ?

CMOS NOR-4

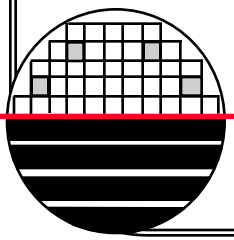




Note: noise margin ~ Δ0=1.2 , Δ1=3.2
max current drive 50uA
static current is zero
gate delay ?

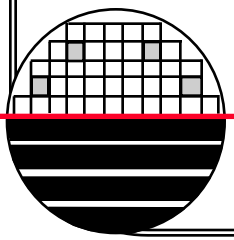
REFERNCES

1. Hodges Jackson and Saleh, Analysis and Design of Digital Integrated Circuits, Chapter 4.
2. Sedra and Smith, Microelectronic Circuits, Sixth Edition, Chapter 13.
3. Dr. Fuller's Lecture Notes, http://people.rit.edu/lffeee

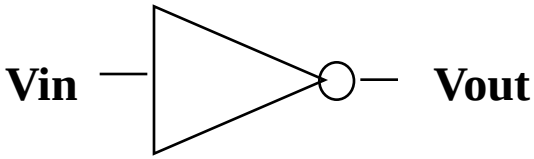


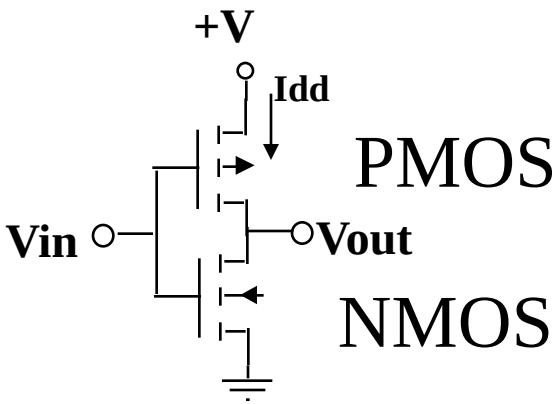
HOMEWORK – MOS INVERTERS

1. Using SPICE obtain the VTC for a CMOS inverter with gate lengths of ~1um. Let the width of both transistors be 2um Determine the noise margins. Determine the maximum current and voltage gain. (Use the SPICE models given below) Make appropriate assumptions.
2. Repeat problem 1 for gate L and W of ~200nm.
3. Given the layout shown below of a CMOS inverter find L, W, AD, AS, PD, PS.
4. The schematic below is for a tristate inverter. This device should be able to make the output high or low when the enable (EN) is high. When the enable is low the inverter is effectively disconnected from the load (high impedance, Z). Use SPICE to show that this circuit operates as intended.



INVERTER LAYOUT

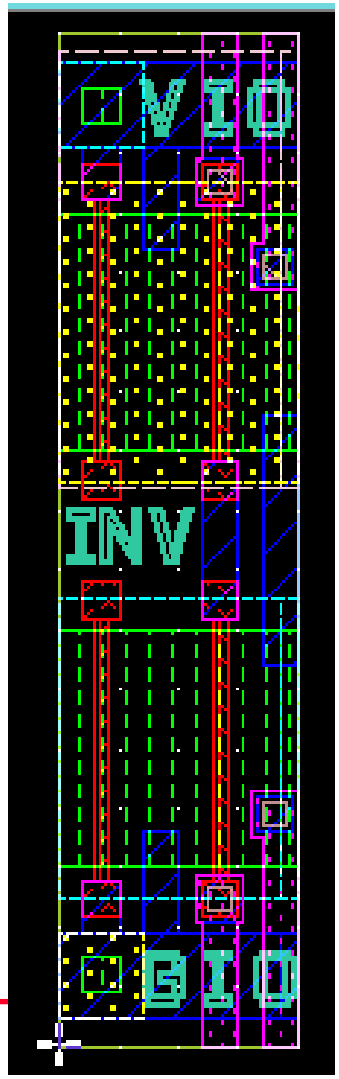


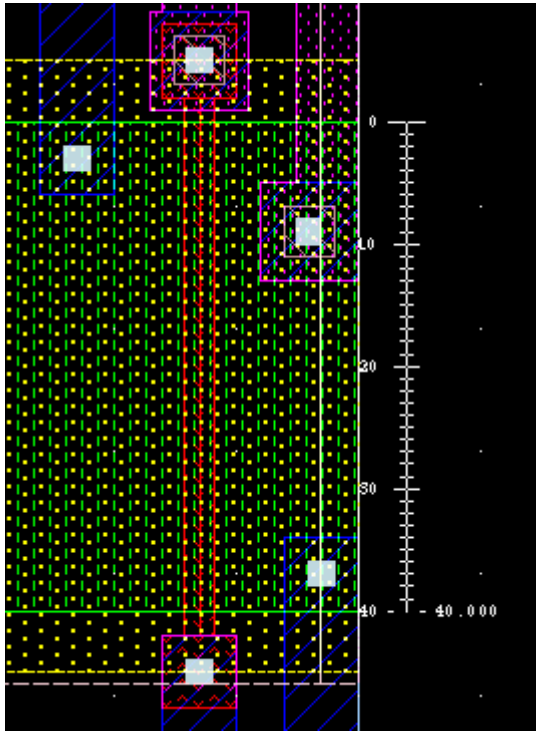


CMOS

TRUTH TABLE

VIN	VOUT
0	1
1	0

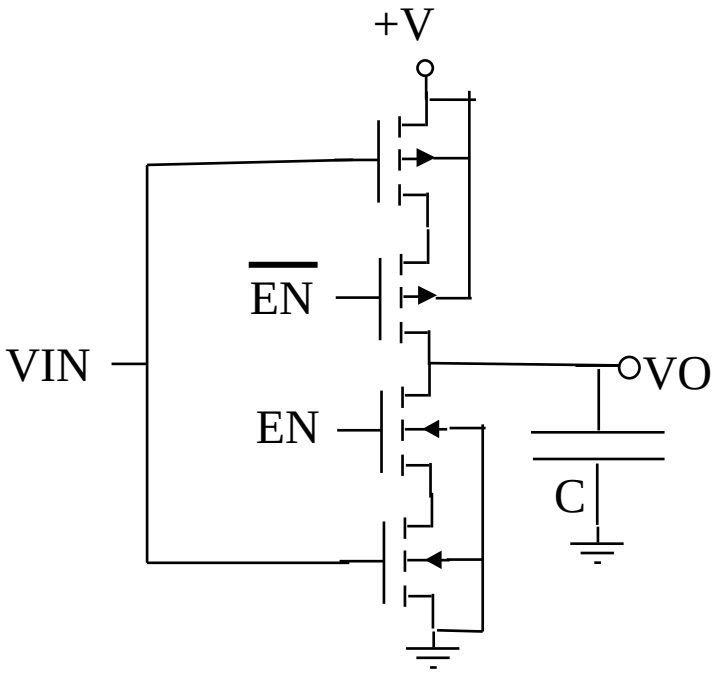




W = 40 µm

Lpoly = 2.0µm

HOMEWORK – MOS INVERTERS

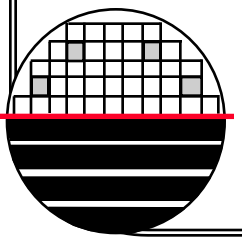


Tristate Inverter

EN	VIN	VO
0	0	High Z
0	1	High Z
1	0	1
1	1	0

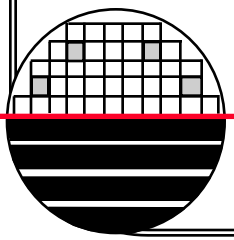
SPICE MODELS FOR MOSFETS

```
*SPICE MODELS FOR RIT DEVICES - DR. LYNN FULLER 4-10-2014
*LOCATION DR.FULLER'S WEBPAGE - http://people.rit.edu/lffeee/CMOS.htm
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=1u W=200u
.MODEL RIT4007N7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=1u W=200u
.MODEL RIT4007P7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



SPICE MODELS FOR MOSFETS

```
*Used for ALD1103 chips
*Note: Properties L=10u W=880u
.MODEL RITALDN3 NMOS (LEVEL=3
+TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0= 1215 VTO=0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5
+NSUB=1.57E16 +XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)
*
*Used for ALD1103 chips
*Note: Properties L=10u W=880u
.MODEL RITALDP3 PMOS (LEVEL=3
+TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0=550 VTO=-0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5
+NSUB=1.57E16 +XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)
```



SPICE MODELS FOR MOSFETS

```
*4-4-2013 LTSPICE uses Level=8
*For RIT Sub-CMOS 150 process with L=2u
.MODEL RITSUBN8 NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013  LTSPICE uses Level=8
*For RIT Sub-CMOS 150 process with L=2u
.MODEL RITSUBP8 PMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
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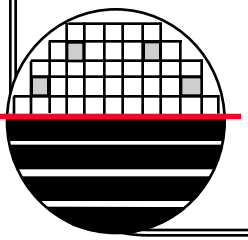
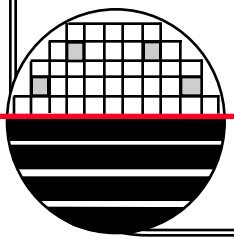


SPICE MODELS FOR MOSFETS

* From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL RITSUBP7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)



SPICE MODELS FOR MOSFETS

```
*4-4-2013  LTSPICE uses Level=8
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSN     NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013  LTSPICE uses Level=8
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSP     PMOS (LEVEL=8
+TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
```