ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Microelectromechanical Systems (MEMs) Process Integration

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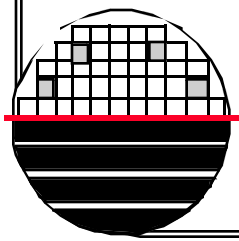
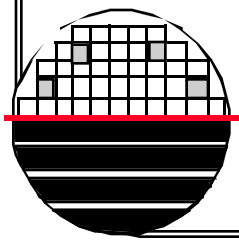


OUTLINE

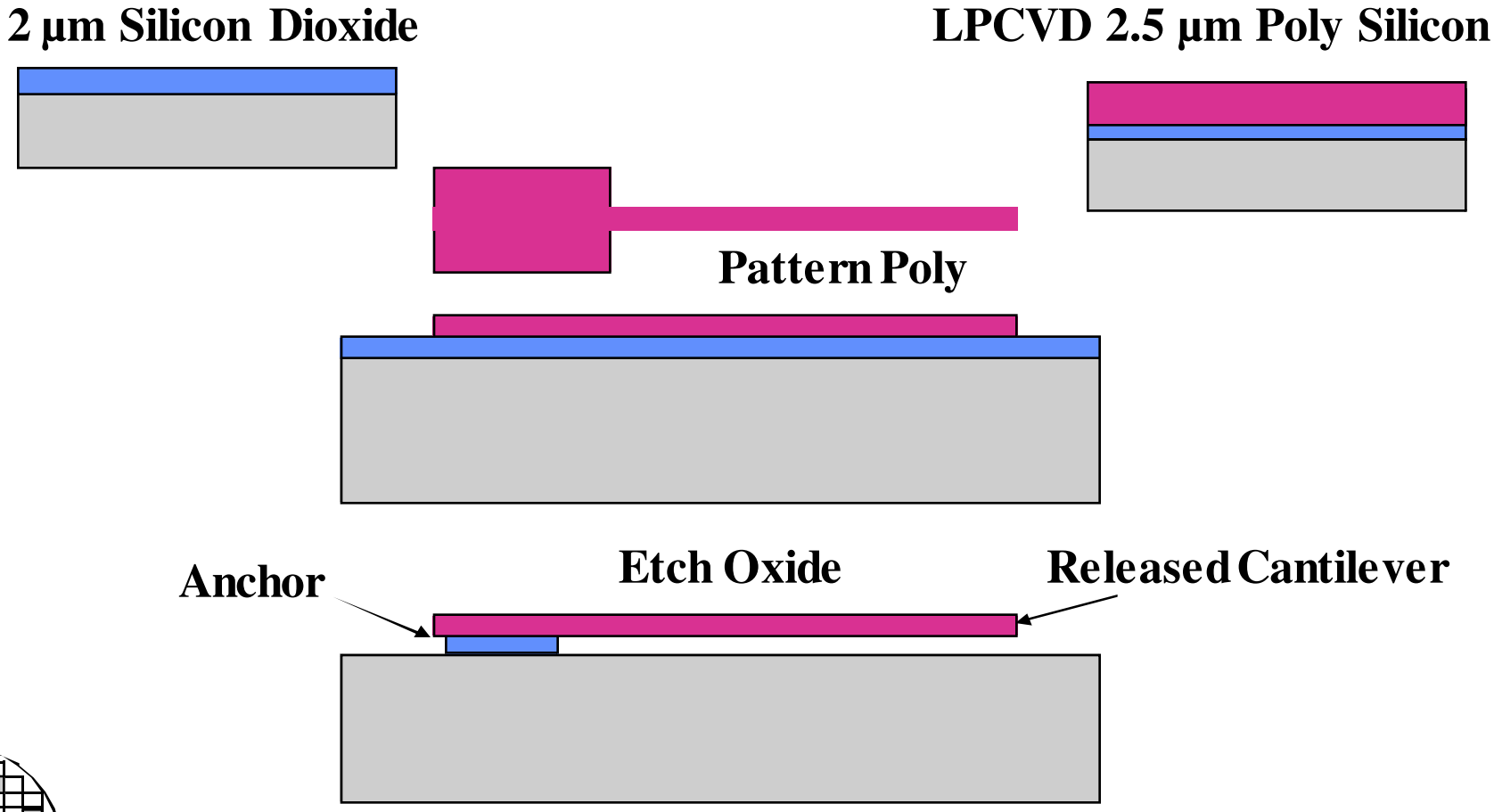
Surface Micromachine Processes
- **Single Poly Layer Processes**
  - **Simple Single Mask Process**
  - **Anchor Process**
  - **Anchor Plus Dimple Process**
  - **Substrate Isolation Process**
- **Two Poly Layer Processes**
  - **Center Pin Bearing Process**
  - **Flange Bearing Process**

Bulk Micromachine Processes
- **Silicon Diaphragm Process**
- **Advanced Silicon Diaphragm Design**
- **Surface Diaphragm Design**

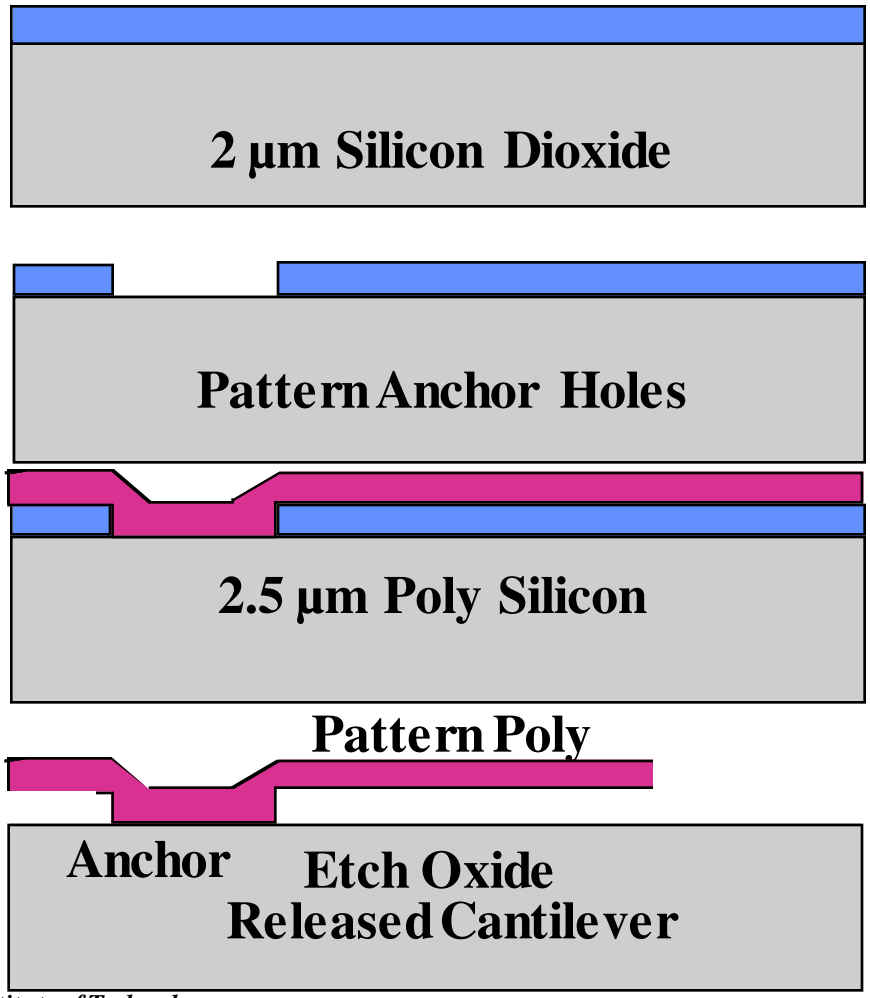
Integrating Electronics with MEMs



SIMPLE ONE MASK PROCESS

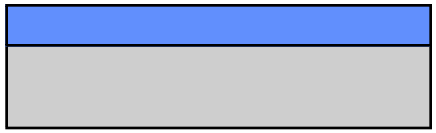


ANCHOR PROCESS

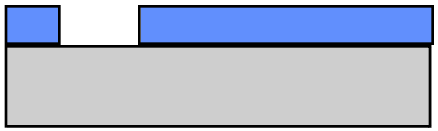


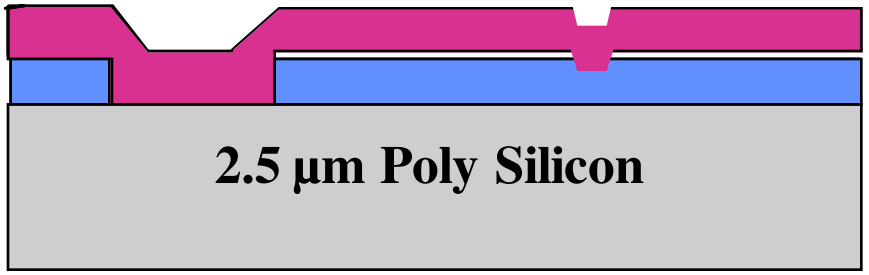
ANCHOR PLUS DIMPLE PROCESS

2 µm Silicon Dioxide

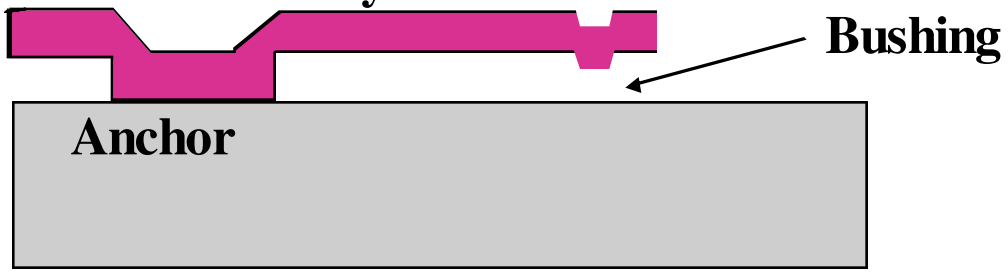


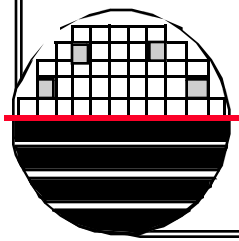
Pattern Anchor Holes





Pattern Poly and Etch Oxide



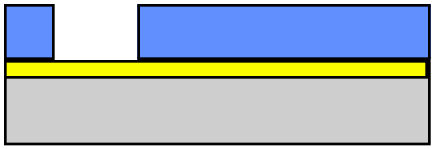


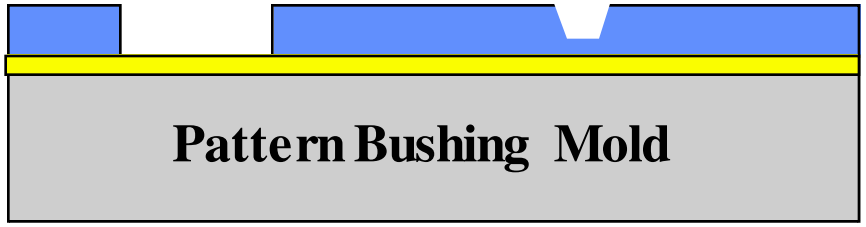
SUBSTRATE ISOLATION PROCESS

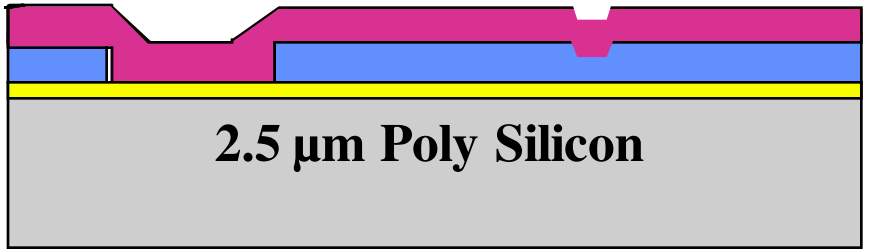
Pad Oxide and Nitride

2 µm Silicon Dioxide

Pattern Anchor Holes







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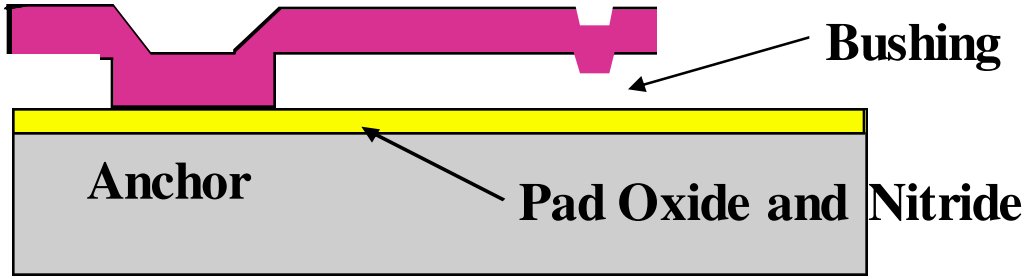
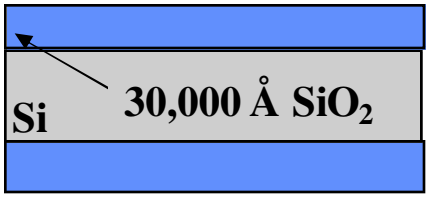
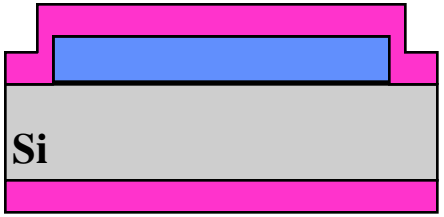
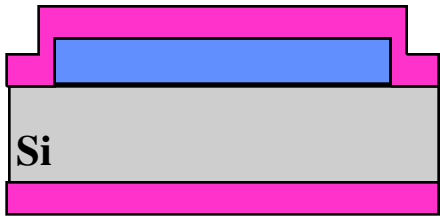


SURFACE MICROMACHINED POLY DIAPHRAGM

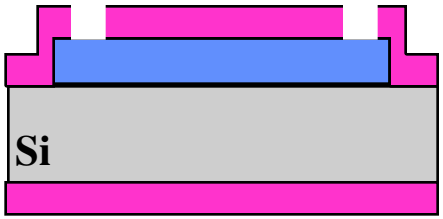




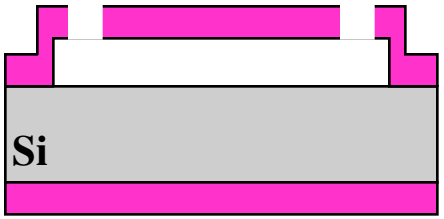
Photolithography
Etch in BHF



LPCVD 2.0 µmPoly



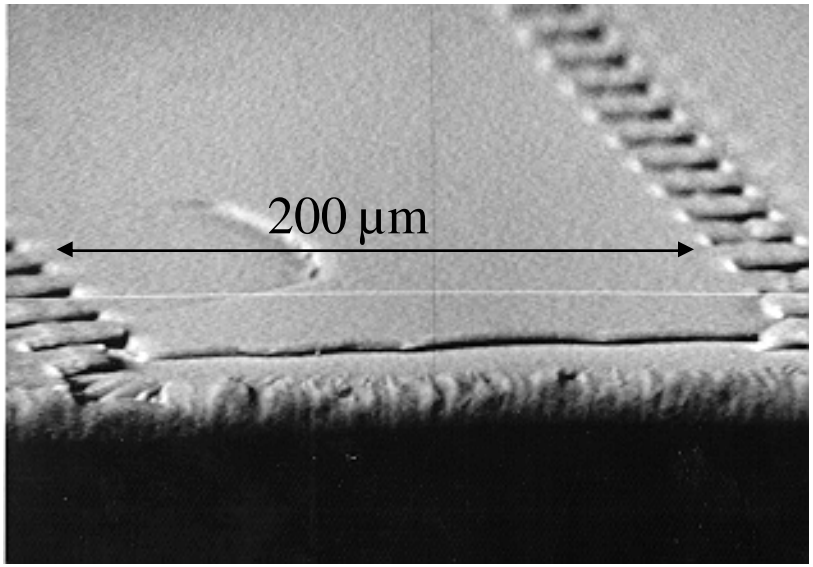
Photolithography
Etch Poly in SF6+ O2



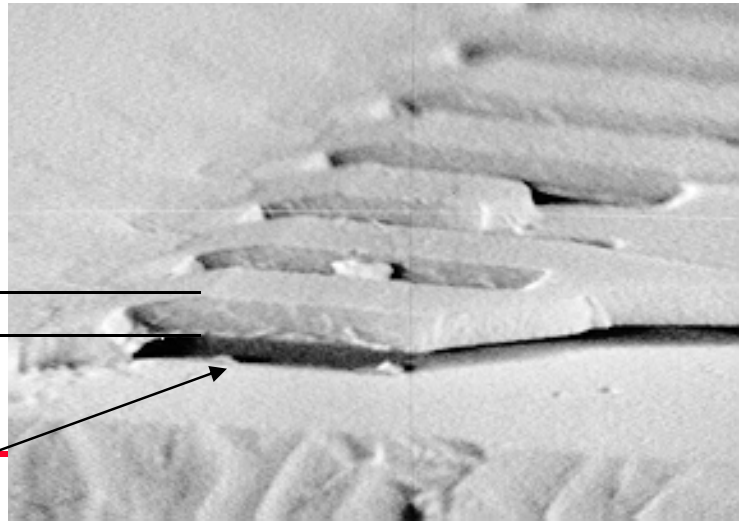
Etch SiO2 in BHF

SURFACE MICROMACHINED POLY DIAPHRAGM

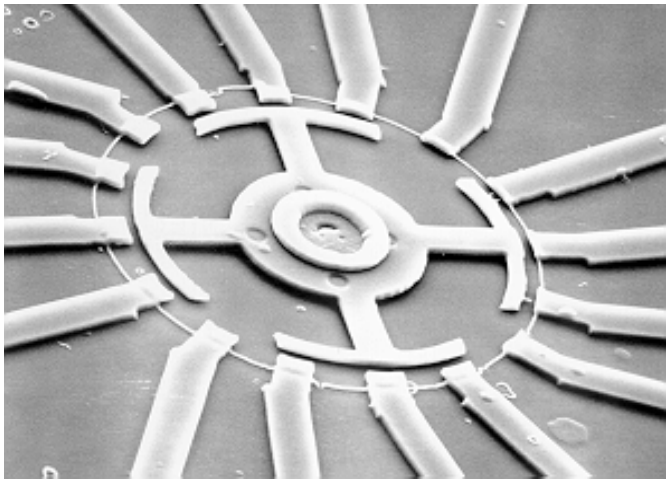
Poly Covered Trench

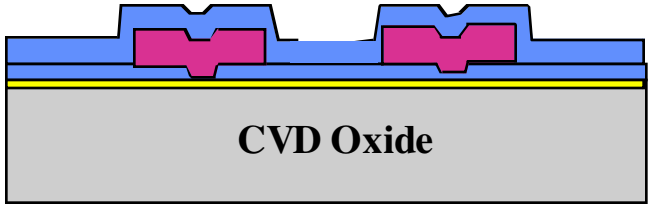


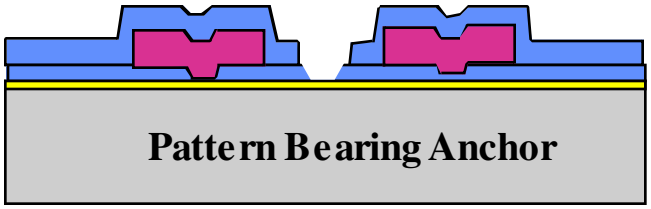
John Castellana, 1997
BSµE RIT

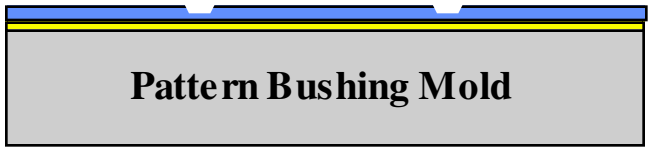


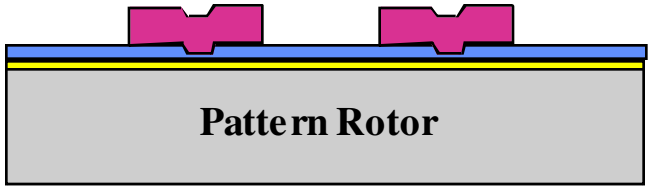
CENTER-PIN BEARING PROCESS

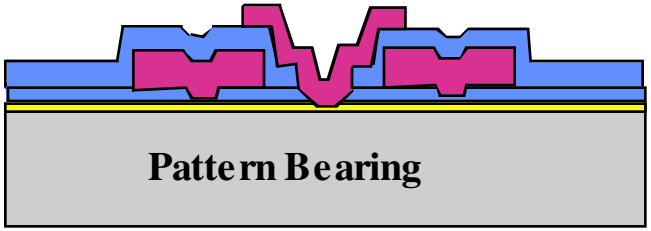


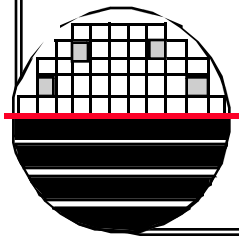




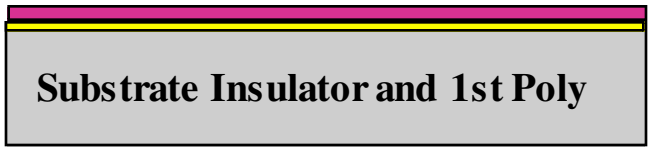


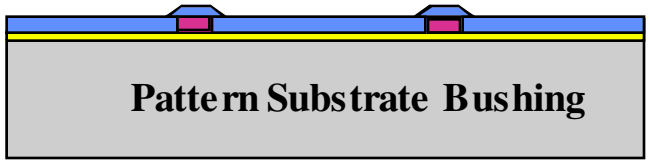


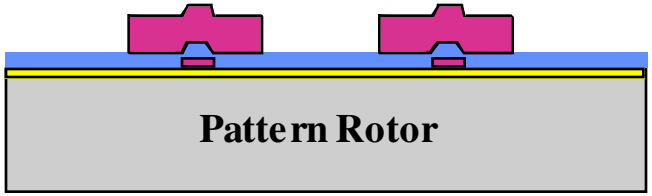


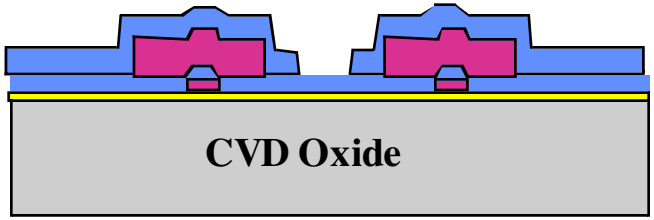


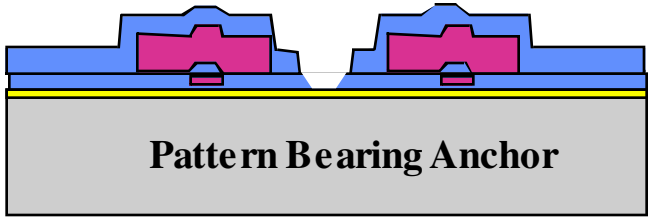
CENTER PIN AND SUBSTRATE BEARING PROCESS

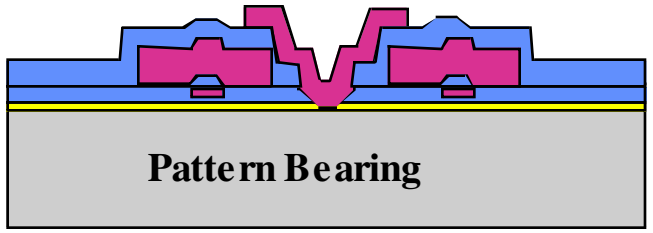


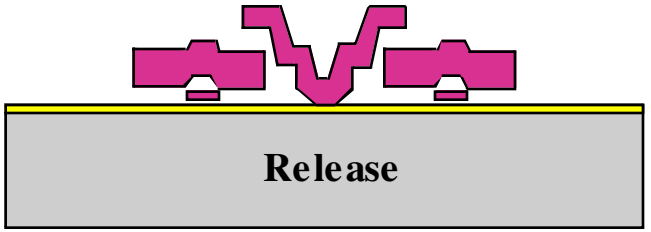


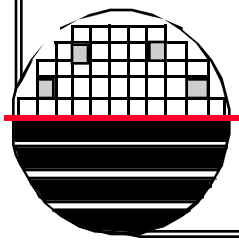




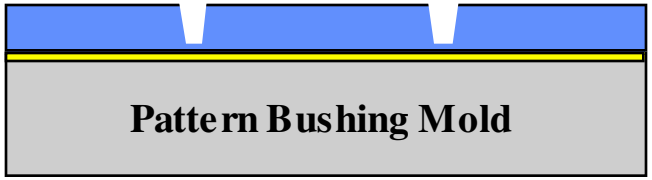


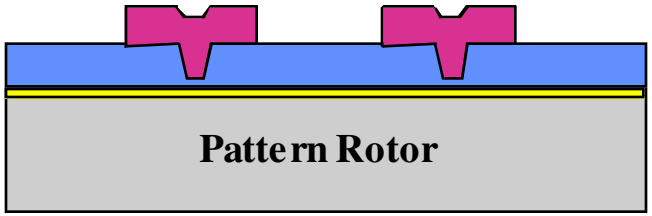


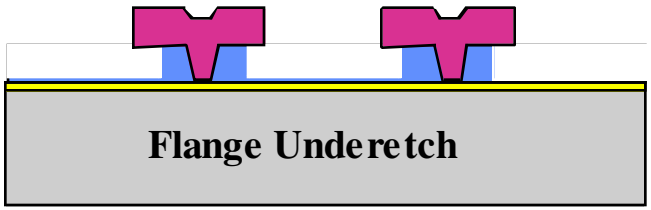


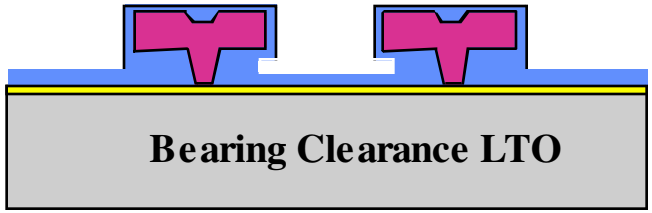


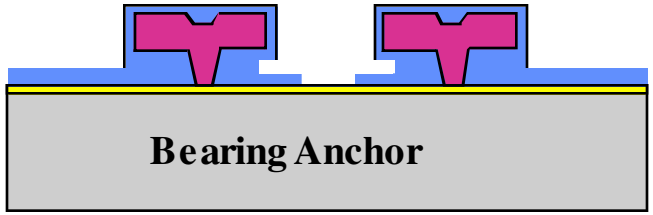
FLANGE BEARING PROCESS

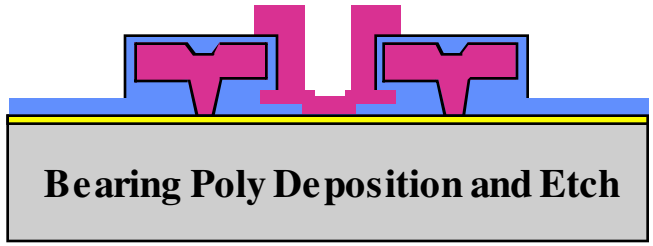


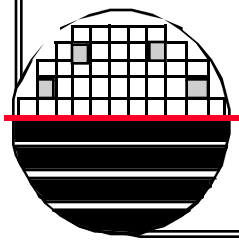






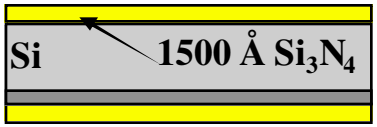




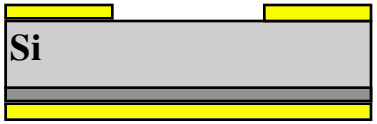


BACKSIDE ETCHED BULK MICROMACHINED P+ ETCH STOP DIAPHRAGM PROCESS

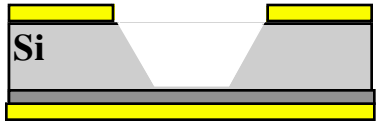
Boron Doped P+ Etch Stop
and n-type Epitaxial Layer



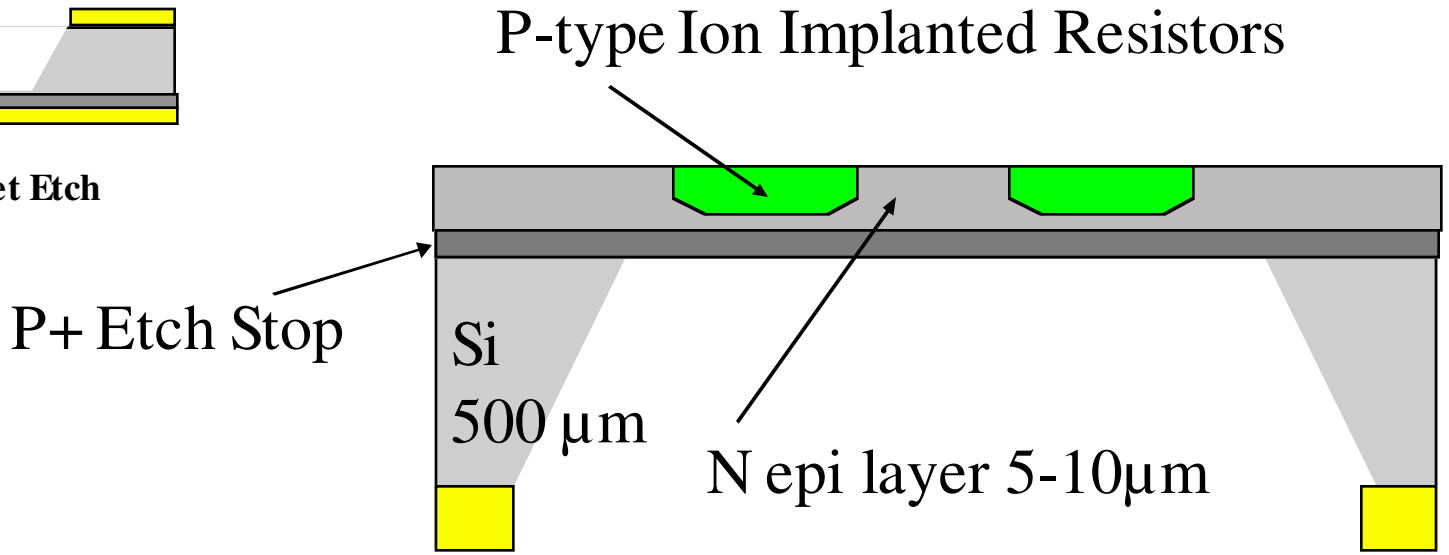
LPCVD Nitride



Photolithography
Etch Nitride inSF6



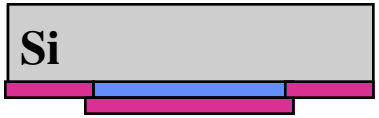
KOH Wet Etch



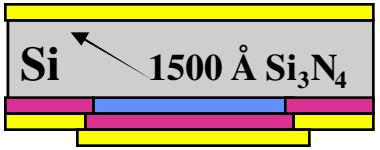
BACKSIDE ETCHED BULK MICROMACHINED POLYSILICON DIAPHRAGM PROCESSES

10,000 Å Thermal Oxide

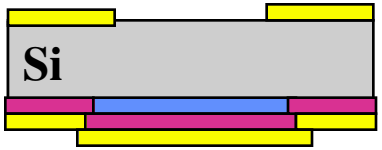
Photo define Oxide for diaphragm spacer



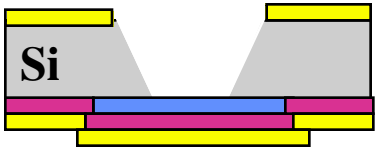
LPCVD Polysilicon diaphragm of 2 µm thickness and removed from backside of wafer



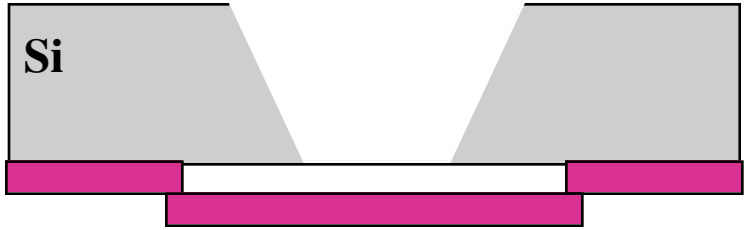
LPCVD Nitride



Photolithography Etch Nitride inSF6



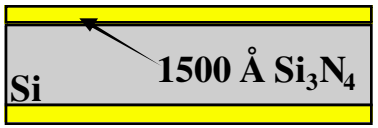
KOH Wet Etch Stop on Oxide

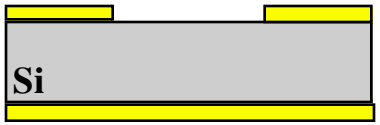


Etch Oxide and Nitride

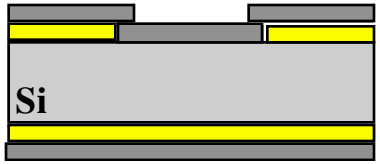
Either thin film resistor or capacitive sensor on poly diaphragm.

TOP SIDE BULK MICROMACHINED SILICON NITRIDE DIAPHRAGM

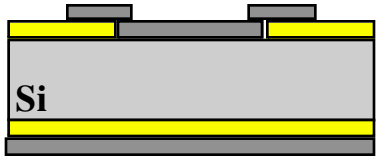




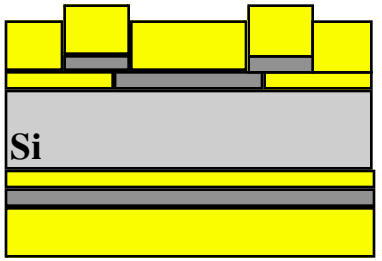
Photolithography
Etch inSF6



LPCVD 0.8µmPoly



Photolithography
Etch Poly in SF6+ O2



LPCVD 0.8µm Low
Stress Si_3N_4

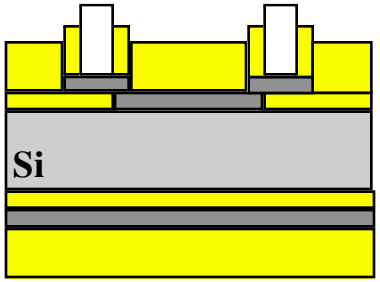
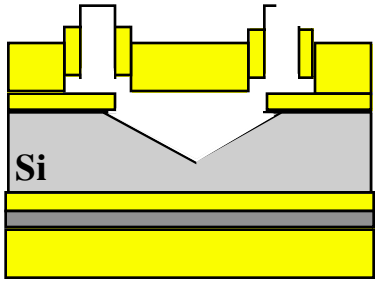
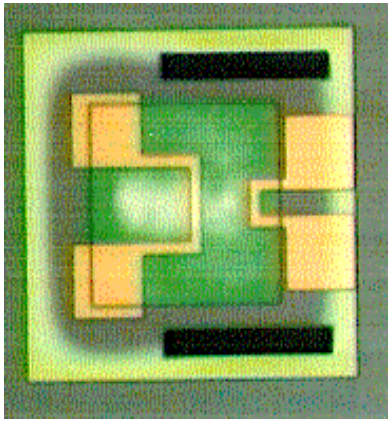
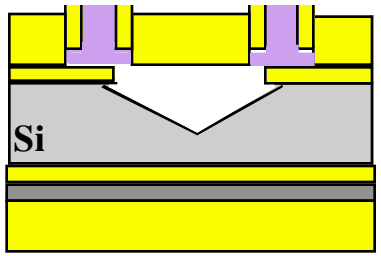


Photo Etch Holes

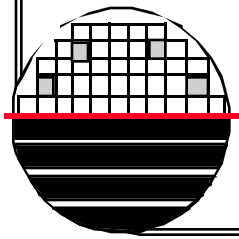


Etch in KOH





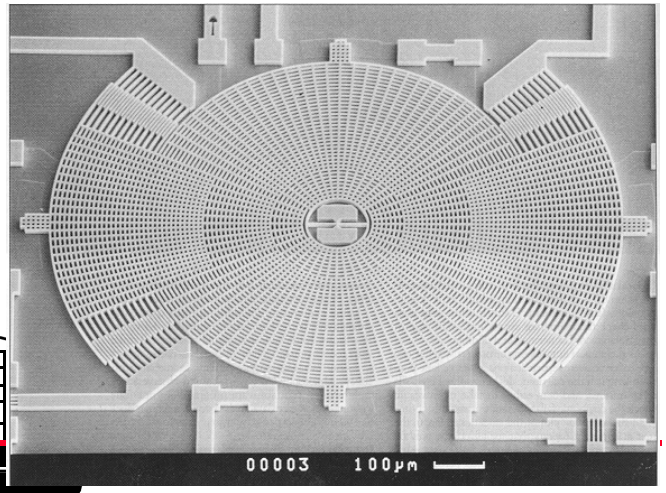
Fill Etch Holes
with LPCVD

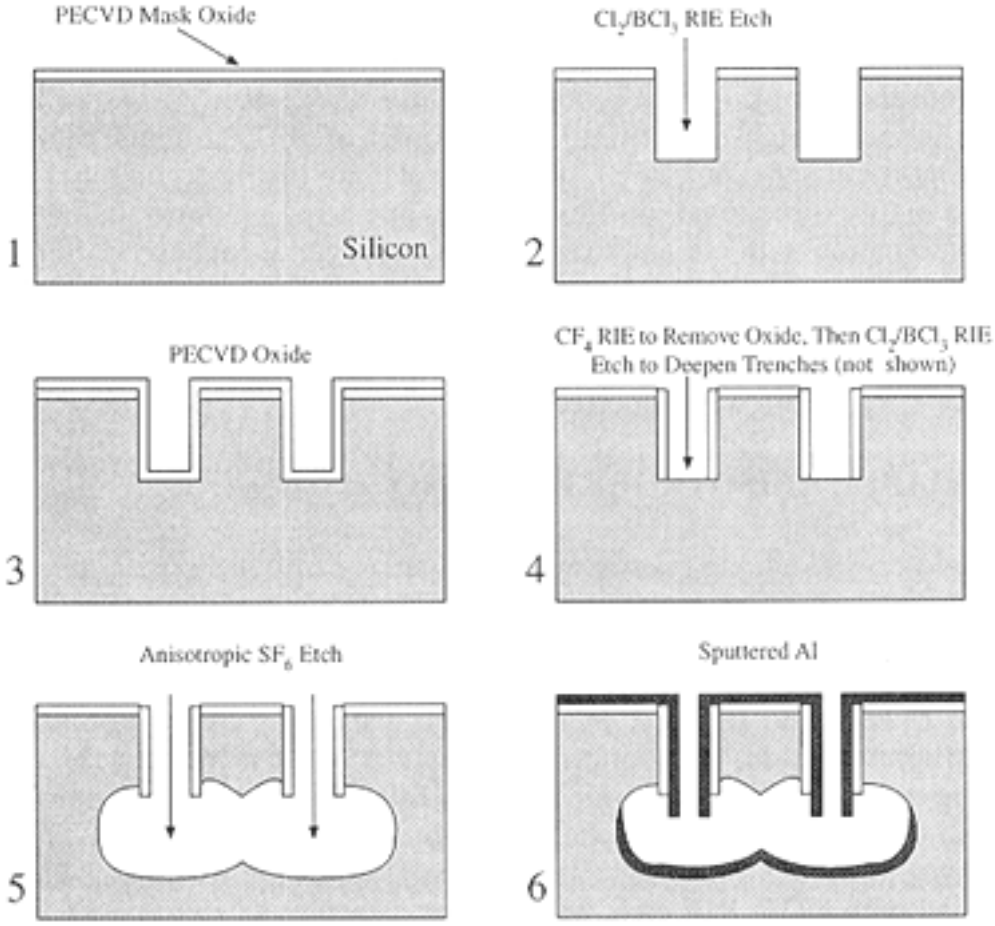


SCREAM PROCESS

Single Crystal Reactive Ion Etched Process for Microelectromechanical Structures

A process that involves anisotropic (Cl_2/BCl_3) reactive ion etch (RIE) followed by isotropic (SF_6) RIE

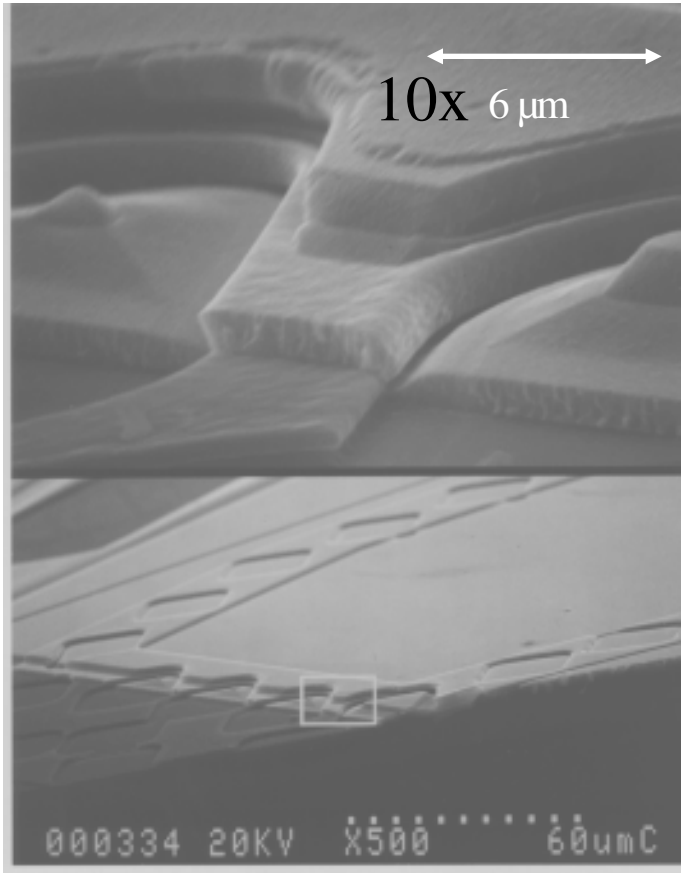


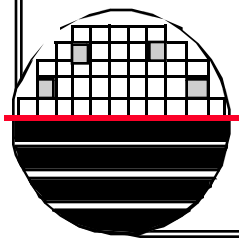


INTEGRATING ELECTRONICS WITH MEMS

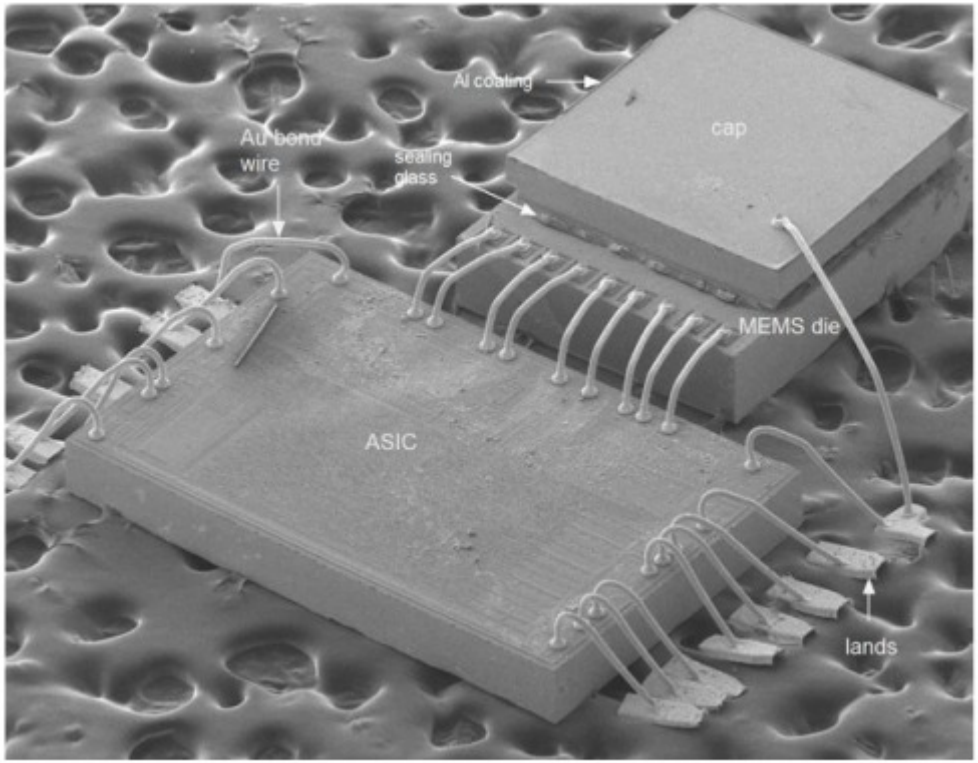
Poly Gate PMOS and MEMs at the Same Time
CMOS first MEMs After
MEMs first CMP CMOS After
CMOS and MEMs at the Same Time

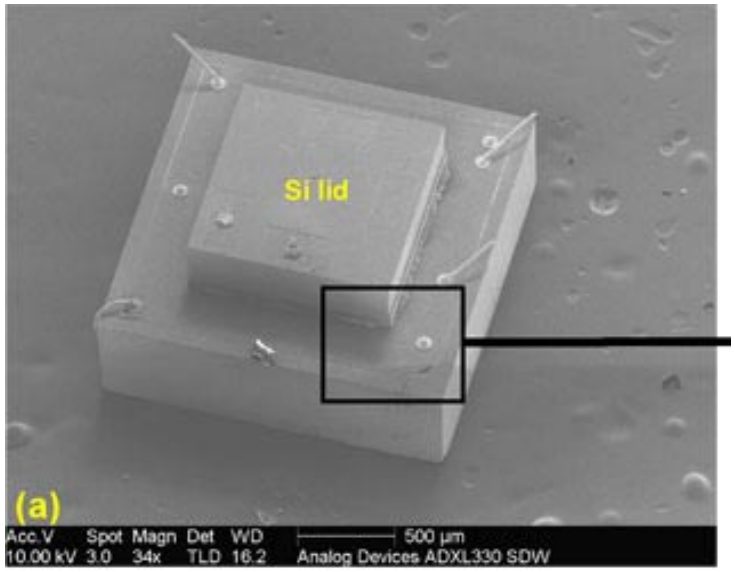
Topology is the main problem

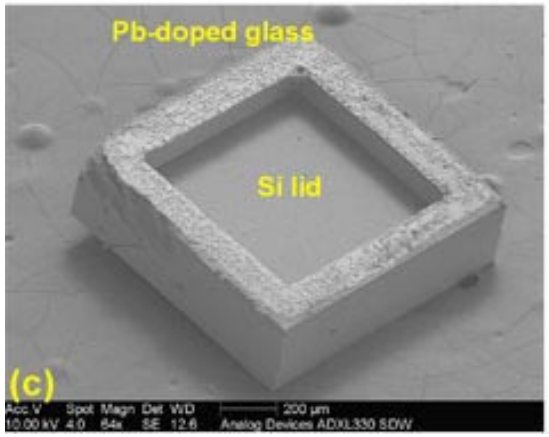




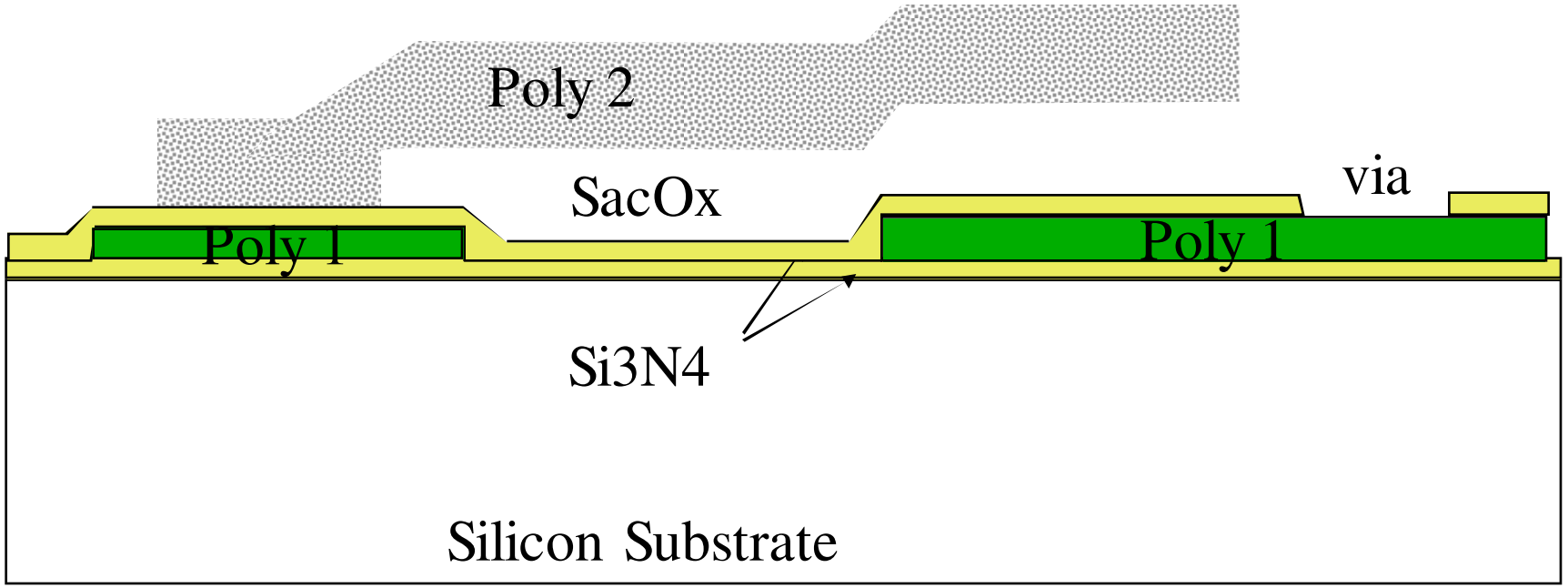
ELECTRONICS CHIP PLUS MEMS CHIP IN SAME PACKAGE







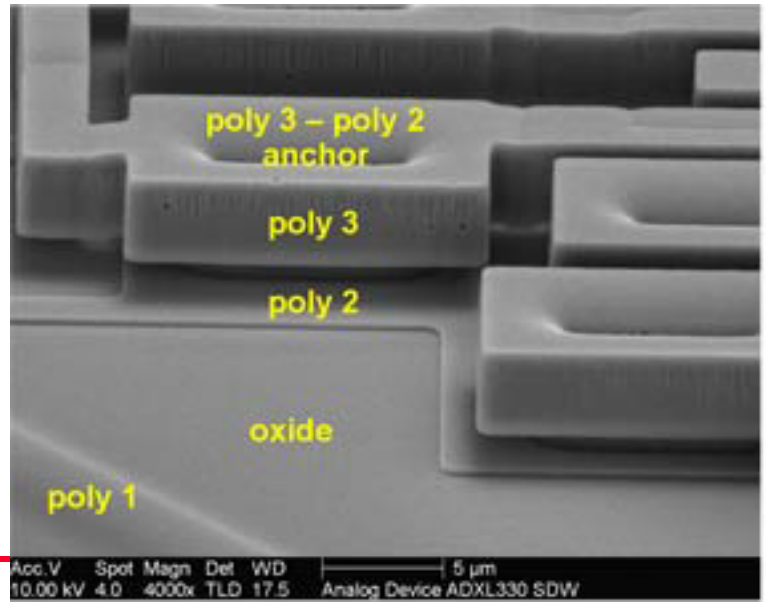
SCALED DRAWING

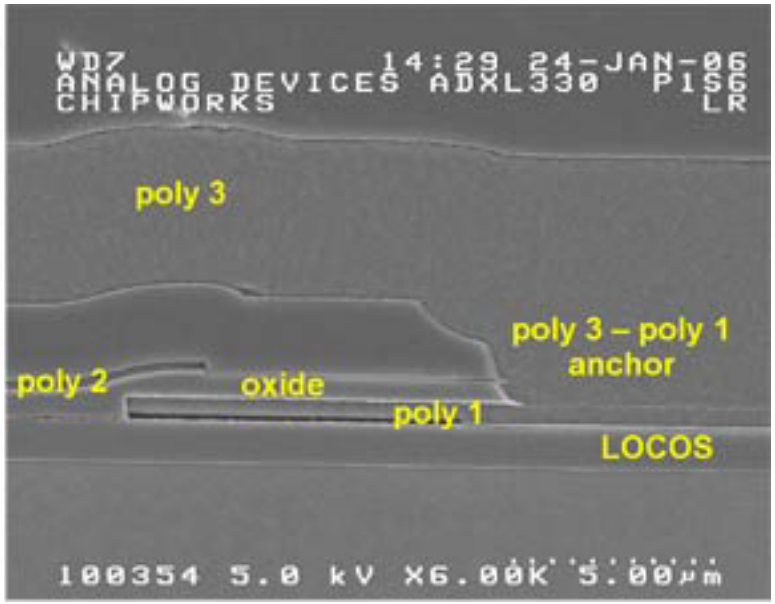


2 um

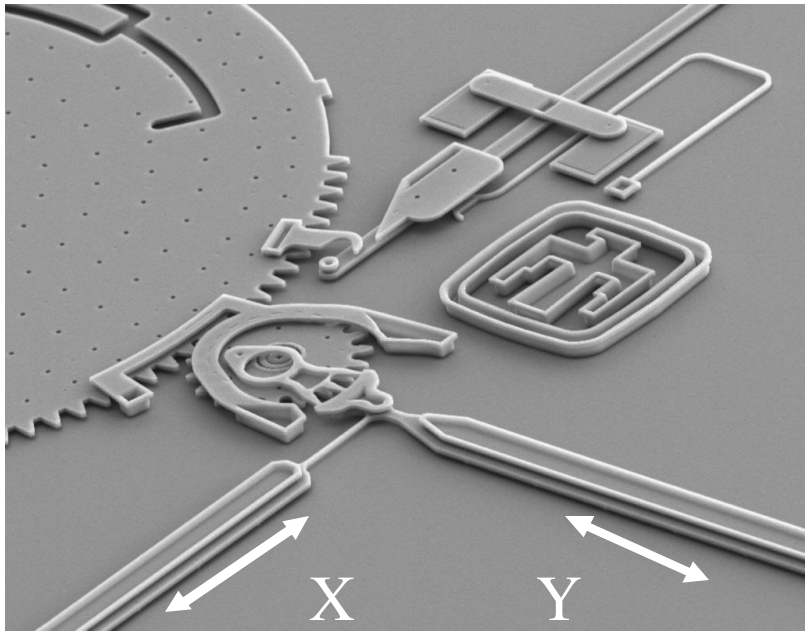
ADDRESSING TOPOLOGY

1. Use thicker layers for each subsequent layer.
2. Run interconnects in poly over topology because LPCVD is a conformal deposition process.
3. LOCOS like processes to reduce topology.
4. CMP

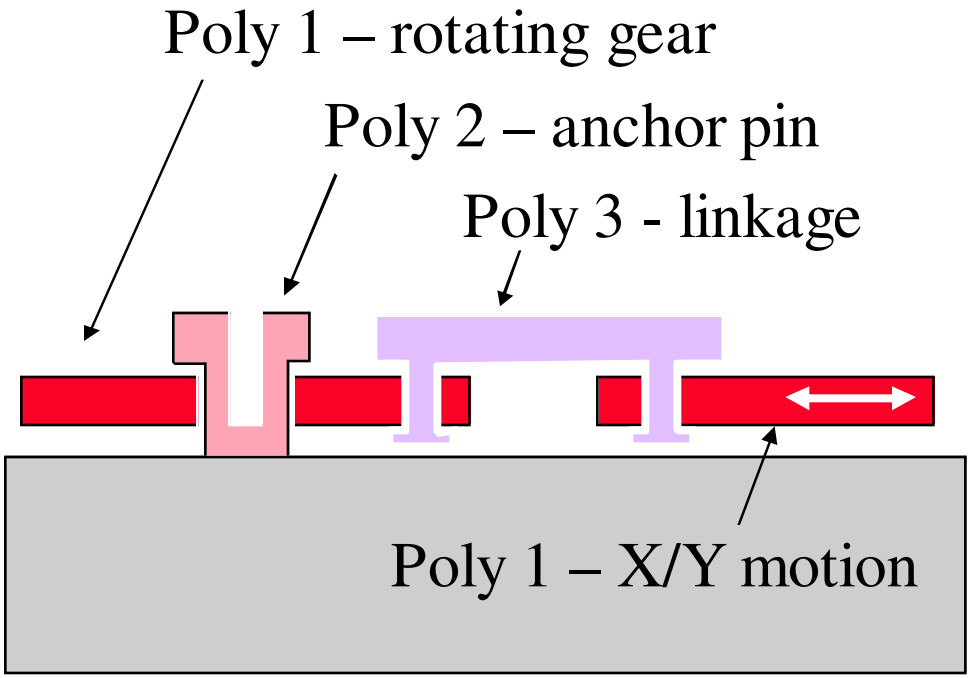




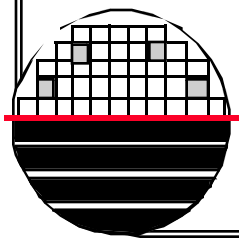
ADDRESSING TOPOLOGY



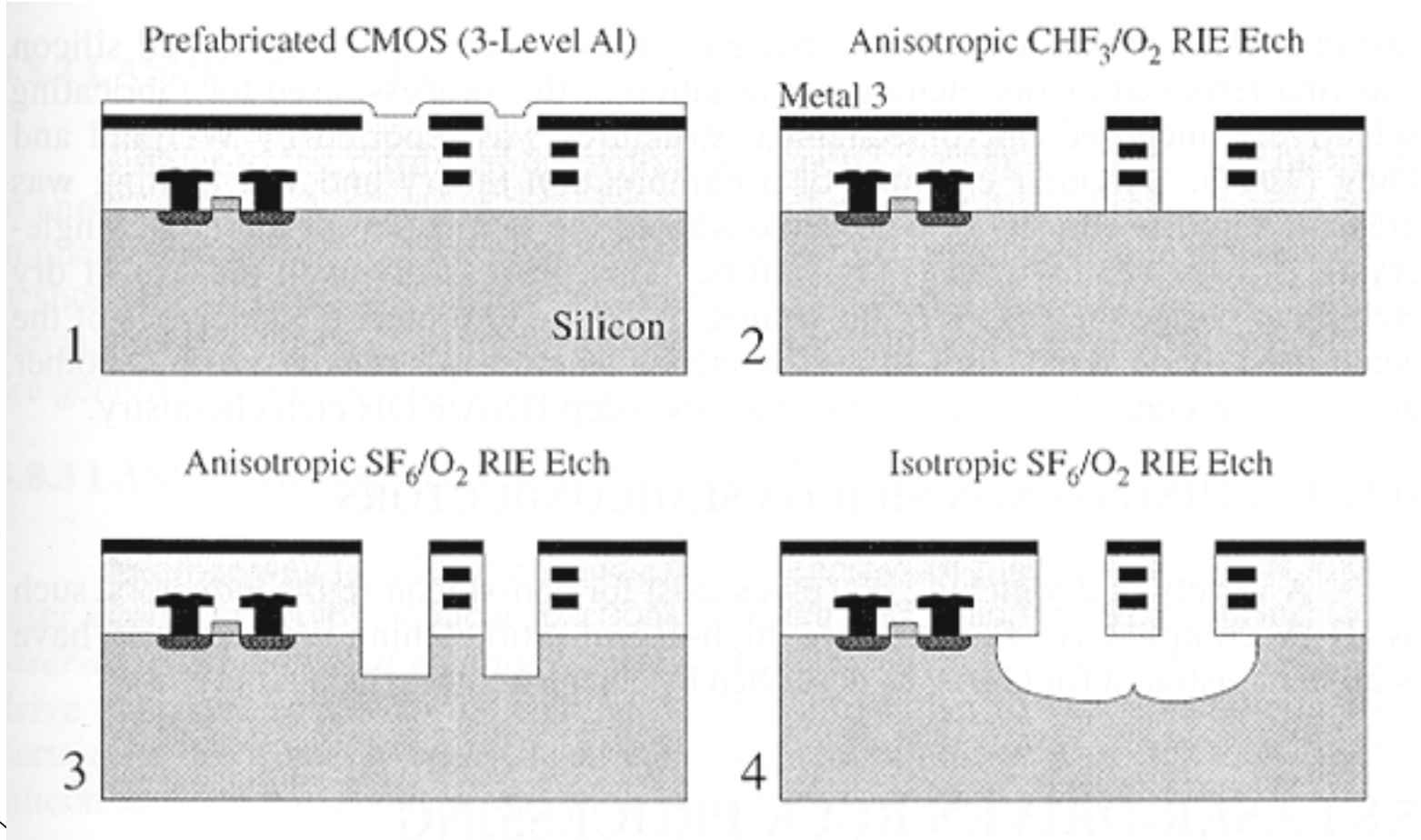
X and Y movement
90° out of phase



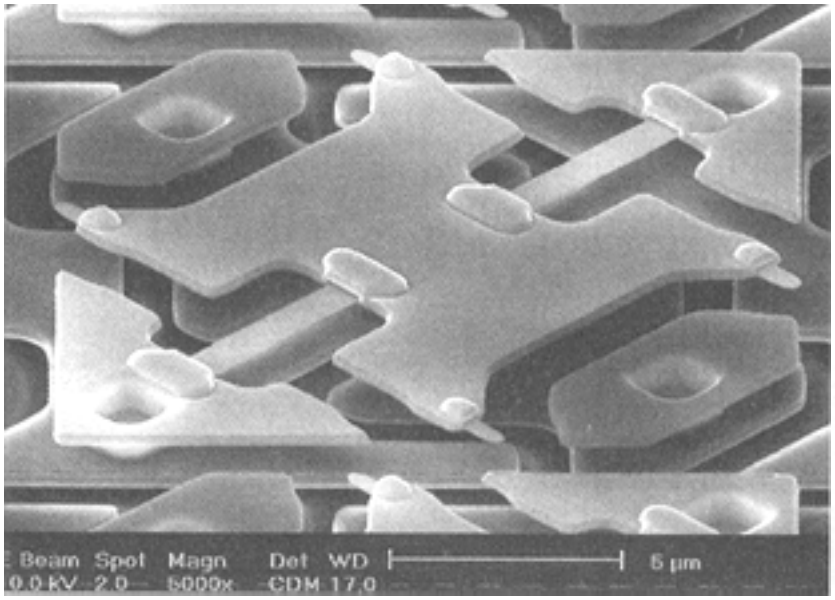
Where is CMP used and why?



CMOS FIRST MEMS AFTER

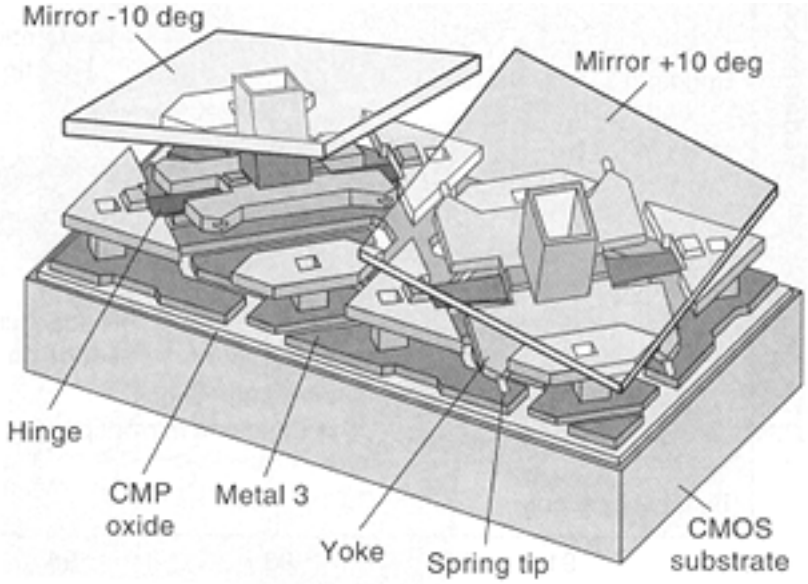


CMOS FIRST MEMS AFTER, TEXAS INSTRUMENTS



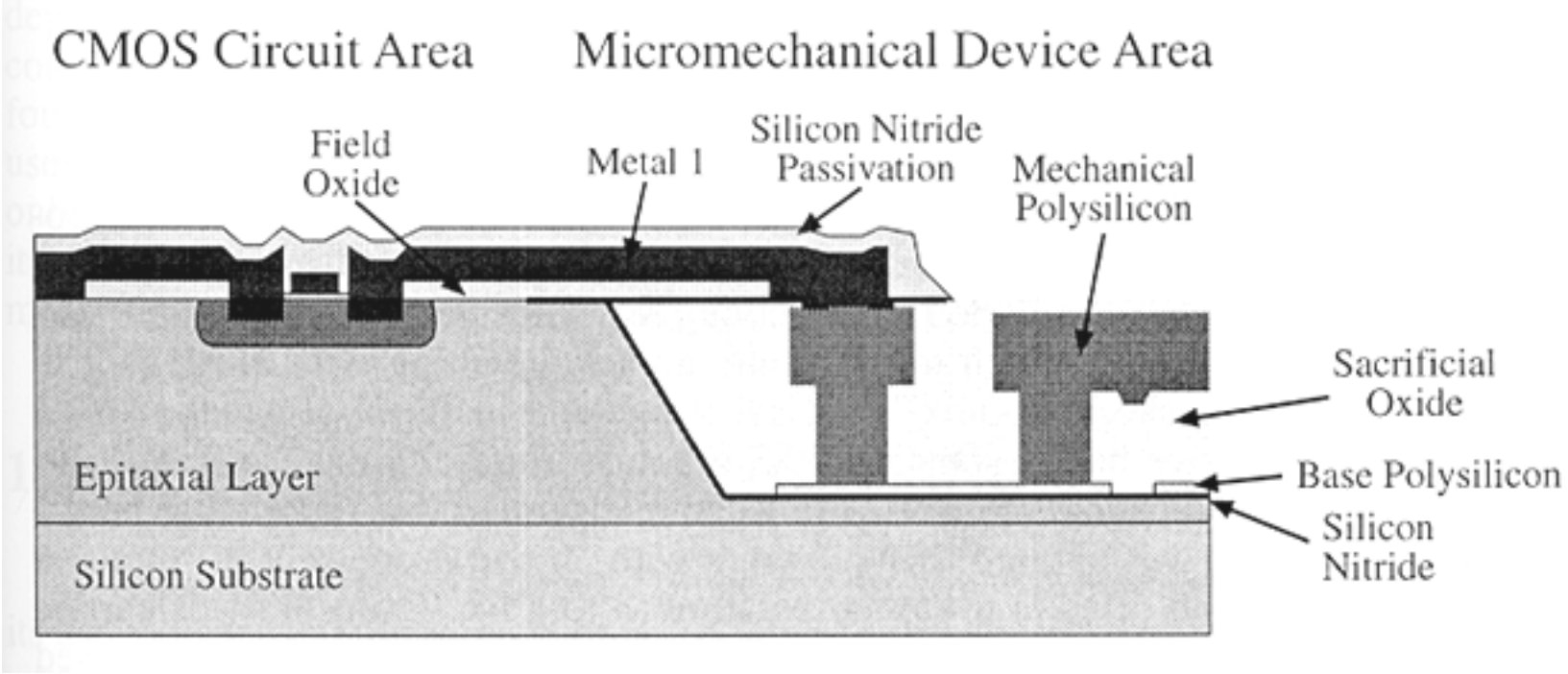
TI Digital Mirror Array

TORSIONAL MIRRORS



1 million Mirrors

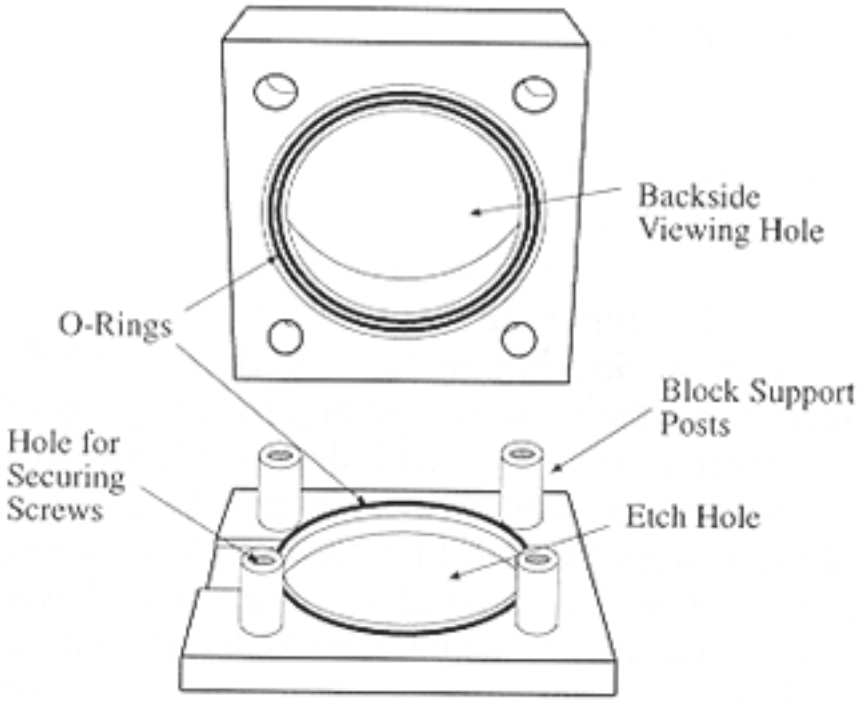
MEMS FIRST CMP THEN CMOS PROCESSING



Buried Polysilicon MEMs with CMP planarization and CMOS post-fabrication (after Nasby, et al, 1996)

PROTECTING ELECTRONICS

1. Poly, Aluminum or nitride layer
2. Glass
3. Organics (Protek)
4. One-sided wafer etcher.



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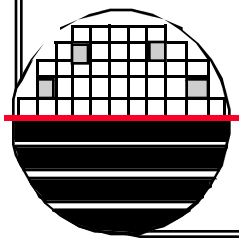
2. "The Challenge of Automotive Sensors," Giachino, J.M., and Miree, T.J., Proceedings of the SPIE Conference on Microlithography and Metrology in Micromachining, Austin, TX, Oct. 23-24, 1995, SPIE Vol. 2640, pp. 89-98.
3. "Integrating SCREAM Micromachined Devices with Integrated Circuits," Shaw, K.A. and Mac Donald, N.C., Proceedings of IEEE International Workshop on Micro Electro Mechanical Systems, San Diego, CA, Fe 11-15, 1996, pp 44-48.
4. "Laminated High-Aspect-Ration Microstructures in a Conventional CMOS Process," Fedder, G.K., et.el., Proceedings of IEEE International Workshop on Micro Electro Mechanical Systems, San Diego, CA, Fe 11-15, 1996, pp 13-18.



HOMEWORK - PROCESS INTEGRATION

1. List a step by step process to make a cantilever accelerometer that has a piezoresistive sensor for measuring the acceleration. There are many different ways to do this so just state your assumptions and use those for your design.
2. Show a cross section with dimensions.
3. Show a top down layout with dimensions
4. Show example calculations relating acceleration to output voltage. Again make appropriate assumptions.