ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Introduction to Mentor Graphics: Schematic Capture, Circuit Simulation and IC Layout

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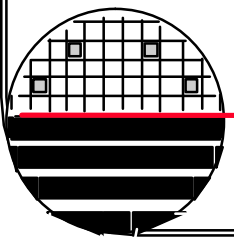

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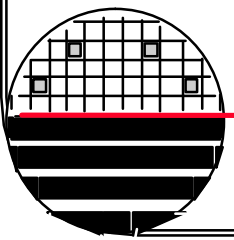
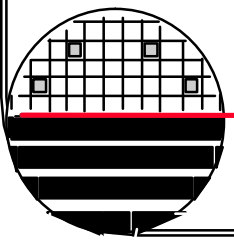


INTRODUCTION

This document is intended to help students get started in using the mentor graphics tools on the computers in the VLSI laboratory at RIT.



VLSI DESIGN CENTER AT RIT

The VLSI Design Center (room 17-2500) consists of AMD Athlon 64 FX-51 Gentoo LINUX workstations, file servers and printers. The workstations are primarily PC's running LINIX operating system. The PC's are fast, have lots of RAM and disk space. There are two file servers for user accounts and application software. The two main print devices are a HP laser printer and a HP 36 inch color plotter. There devices are connected through an Ethernet based network. The primary application software, on this network, is the very sophisticated and tightly integrated Mentor Graphics suite of EDA (Electronic Design Automation) tools.

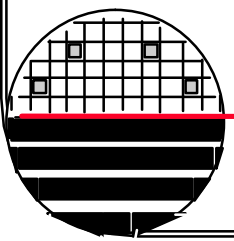
Accounts on the computers and access to the room are controlled by the computer engineering department. Currently Charles Gruener for computer accounts and Rick Tolleson for card swipe room access.

BASICS - DESKTOP

A graphical interface that provides workspaces, windows, menus, controls, and a front panel to help you organize and manage your software applications.

The **Front Panel** has a tool bar (usually at the bottom of the screen). The tool bar has a K-Gear icon which allows access to editors, graphics programs and the open office software package. The open office package has calculators, drawing programs, equation editor and word processing. You can change the settings for the look and feel of the desktop and the windows that are running. I suggest that you do not go too wild changing things , instead stick to getting the job done.

There are four “desk tops” available to run programs on. The toolbar tells you which desktop you are looking at and what is running in each window on the desktop.

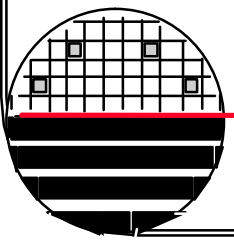


BASICS CONTINUED

The Mouse: is a three button mouse. The left mouse button is used to select or "click" on something. The right mouse button is used for popup menus. The middle mouse button is typically defined for each application and does not have a common function. For example in the layout software "IC" the middle mouse button shifts the layout so that the clicked location is centered in the workspace.

Log Out: click on K Gear icon, select Log Out…, Select End Current Session

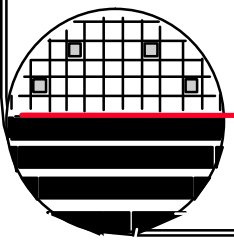
Restore Session: If there is no activity for several minutes the screen will be locked and require the user to type his password to restore the session.



BASIC COMMANDS

Command	Description
ls	list the files and directories in the current directory
cd	change directory
cd ..	go up one directory
mv	move a file (rename a file)
rm	remove a file (delete a file)
pwd	display path of current directory
mkdir	create a new directory
rmdir	remove a directory
yppasswd	change your password

It is important to remember that since this is a UNIX operating system, the commands are case sensitive.



LOGIN

Usually the workstation screen will be blank, press any key to view a login window.

Login: ----------

Password: **********

The screen background will change and the control panel will appear.

[ ] Click the left mouse button on the terminal icon. A window will appear that says Shell-Konsole on the top and has a Unix prompt inside.

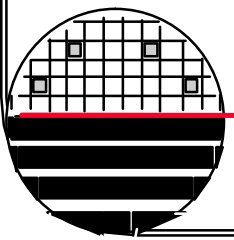
[ ] At the Unix prompt, change your password. Type **password** and follow instructions

[ ] then type **pwd <RET>**to view the path to your directory and write it down exactly as shown.

[ ] Type the command **ls <RET>** at the :prompt to see a list of directories and files, the account may be empty.

[ ] Make a subdirectory **mkdir directory_name <RET>**

[ ] then change to that directory **cd directory_name <RET>**, the directory should be empty. Type **ls** to see.



DESIGN MANAGER

The design manager is a software package used to organize a design and the many software tools that can be used with the design. It can be started by

[ ] typing **dmgr <RET>** or type **dmgr_ic** for additional tools including layout software IC

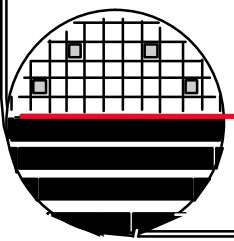
The left side of the window is the Tools window, the middle section is the Navigator window which allows you to see (navigate) the files and folders in your directory . The session palette on the right allows you to open another series of windows within the design manager. Maximize the design manager window. Highlight the tools window and click on VIEW>UPDATE WINDOW repeat for navigator window.

Function keys: Along the bottom is the function key menu. Each function key can have three or four functions depending on if it is pressed alone, or simultaneously with the shift key or simultaneously with the ctrl key or simultaneously with the alt key.

[ ] In the navigator window double click on the folder you made.

SCHEMATIC CAPTURE USING "DA"

Electronic circuits can be simulated to determine how they perform. To do that the simulator needs to know the components in the circuit and how they are connected. This can be given "graphically" in a schematic or as a net list "text file". Mentor Graphics calls its schematic capture software "Design Architect" or "DA" for short. Basically DA allows the designer to place components on a sheet and then interconnect them with wires. The components can be basic such as resistors, capacitors, transistors, or more advanced components such as logic gates (AND, OR, etc.). Additional components such as input ports, power supplies, signal sources are also added. Finally the software checks the schematic for obvious errors and creates a net list to be used by the simulation software.



GATE LEVEL SCHEMATIC CAPTURE USING DA

[ ] The first step is to invoke the design architect software. Double click on the Design Architect icon (design_arch) in the tools window of design manager. Maximize window.

[ ] Once in design manager, you can open a sheet by selecting OPEN SHEET in the session palette along the right side of the window. Type in the component path and component name. (specify your subdirectory, e.g. /home/username/directory_name/component_name)
For example: **/home/rep9161/emcr201/xor** where emcr201 is a directory level and xor is a circuit design (which also happens to contain sub-directories).
leave sheet = sheet1 and start up path = blank. Click OK

[ ] Choose the appropriate library of components. Click on Library Icon and gen_lib. Right click and select show scroll bars.

[ ] Build your gate level schematic by selecting and placing logic gates, input ports and output ports on your schematic. Spread out the components so that the wiring will not be too crowded. Use the + and - keys on the numeric keypad to zoom your view in or out, the arrow keys allow you to scroll around and shift F8 shows the entire view.
[ ] Function key F2, unselects all.

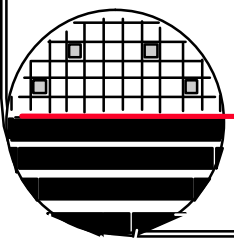
SCHEMATIC CAPTURE CONTINUED

[ ] Route wire connections using the mouse and the **F3** function key. **F3** will begin a wire connection and a double click of the mouse will end a wire connection. Wires that cross will only be connected if you stop and click at the connection point while drawing the wires (look for the connection dots or squares)

[ ] Change the net labels by placing the cursor over the word net and pressing **SHIFT/F7** or PROPERTIES>MODIFY using the pop-up menu accessed through the right mouse button. Change new value to A, B, …. Q….,etc. Click OK. Press F2 (unselect)

Make sure that nothing is selected (check the SEL count)

[ ] Add Name, Date, and Title by click of right mouse button and finding DRAW>TEXT option. Click OK. Place text. Press F2 (unselect)



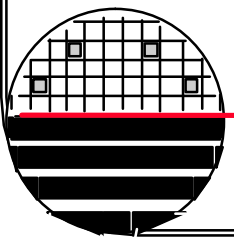
CHECKING, PRINTING, LINKING TO MODELS

[ ] Check your sheet for dangling (unconnected) wires (nets) and pins.
Use CHECK>SHEET>with defaults from the pull down menus in the top banner.
[ ] Save your schematic once it has been checked and has no errors. (1 warning)
Select File and Save Sheet.
[ ] Select File and Print Sheet. Printer name is **prec10**. Click OK.
[ ] After capturing the project we need to link all the appropriate gate and transistor models to the schematic description.
[ ] right click on menu palette along right side of workspace.
[ ] Select display schematic palette
[ ] Select Session
[ ] Set Viewpoint
[ ] Create new viewpoint
[ ] Enter component name (like XOR)
[ ] Enter viewpoint name (like XOR_VPT)
[ ] Select Quick_Sim……
[ ] Close Design Architect

CIRCUIT SIMULATION USING "QUICKSIM"

Once a net list is available the circuit can be simulated to see how it performs. "Quicksim" is a digital simulator which applies digital signals (low/high only) to the input ports and predicts the digital signals at all the other nodes in the circuit. "Accusim" is an analog simulator which applies analog signals to the input ports and predicts the analog signals at all the other nodes in the circuit.

This section of notes detail the use of Quicksim II a digital simulator.



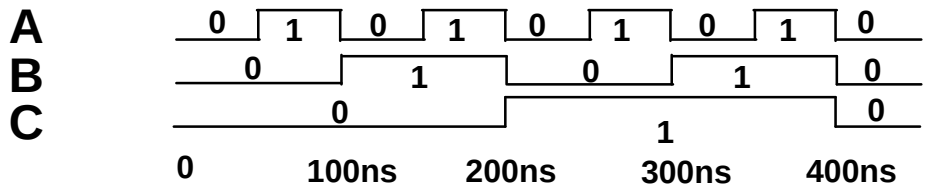
CIRCUIT SIMULATION USING "QUICKSIM II"

With the viewpoint set correctly we can use *QuickSIM II* to apply a series of pulses to the circuit inputs which exercise all of the circuit functions and simulate the circuit's output responses.

You now have to set up the input stimuli necessary to check the functionality of your logic. The inputs should simulate all possible combinations of the input variables. For example, for a three binary input circuit (A,B,C) there are $2^3 = 8$ possible combinations.

This can be done by making each input a 'clock' and adjusting the period so that each input in the truth table is simulated as shown

Just how to do this is given on the next page!



CIRCUIT SIMULATION USING "QUICKSIM II"

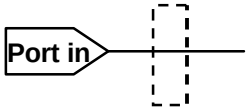
[ ] In the design manager navigator window.
You should see a file with your component name on it.

[ ] Open the tool, QuickSim II, by double clicking on its icon.
- [ ] Use navigator or type in entire path to component
- [ ] Select OK
- [ ] Maximize window

[ ] Open sheet (leave it 1/4 size)

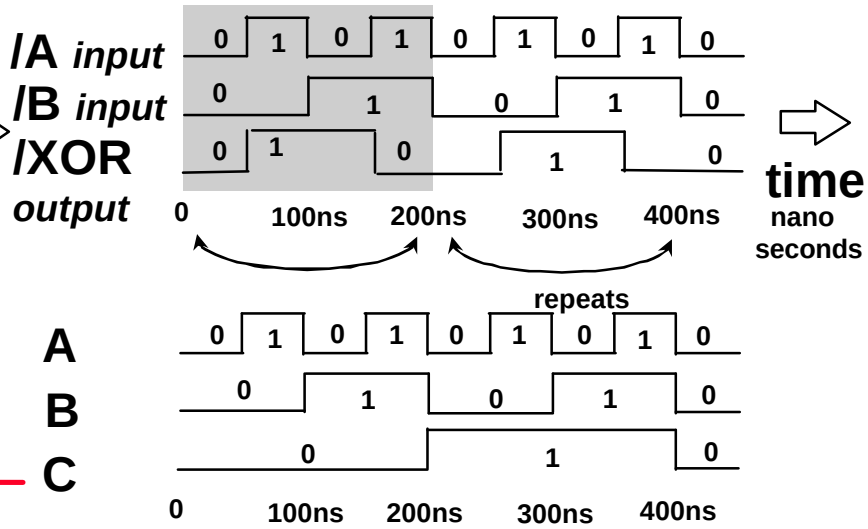
[ ] Select an input node in the schematic window, then select SETUP>FORCE>CLOCK
- [ ] fixed
- [ ] /A or /B … etc. /Q…..etc.
- [ ] Period = …..
- [ ] Stop time = 800...
- [ ] Single Transition
- [ ] 50% duty cycle
- [ ] OK
- [ ] Repeat for all input nodes

Selection box



Press and hold left mouse button

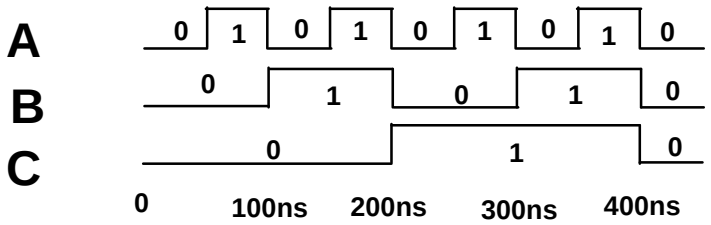
Verification of the XOR circuit



CIRCUIT SIMULATION USING "QUICKSIM II"

[ ] Select each input in turn using the left mouse (see illustration).
Do them in order A, B, C, etc. and then outputs Q1,Q2...
[ ] Select Trace (blue button, generates timing diagram)
[ ] The List option will produce a truth table for the selected inputs/outputs. By default, the List option will try to poll the values of the output during a high-low or low-high transition of the inputs. This produces erroneous output for the truth table during the transition time.

To fix this go to Setup -> Window Attributes -> List Defaults
[ ] Un-check "On Change" Button
[ ] Set List Period = ½ Shortest Period Input Force
[ ] Set List Offset = ¼ Shortest Period Input Force

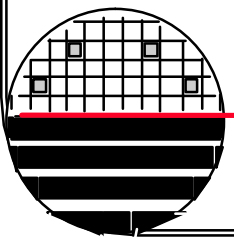


For this example, The A signal has a Period of 100ns. The List Period Should be set to 50ns and the List Offset to 25ns

[ ] Now, Select List (blue button, makes a truth table)

CIRCUIT SIMULATION USING "QUICKSIM II"

[ ] Run, until Stop (blue button)
[ ] To re-simulate select
    [ ] Reset (blue button)
    [ ] State
    [ ] Do Not Save
    [ ] OK
    [ ] Then select Run, until stop
[ ] Print out trace, Click on the trace window to activate it,
    select FILE>PRINT (printer mgcprec10)
[ ] Print out List, Click on the List window to activate it,
    select FILE>PRINT (printer mgcprec10)



PRINTING THE RESULTS

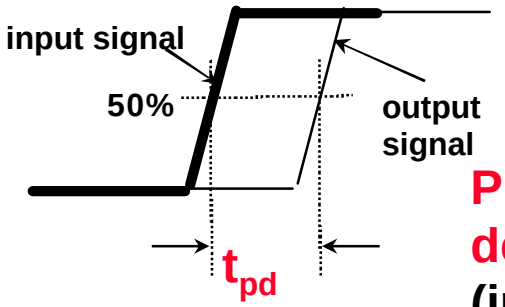
Verify that YOUR circuit performs as required. To reset the simulation time back to zero chose *RESET*, otherwise running new simulations will continue from the endpoint of the last simulation.

When your circuit works, highlight the trace window and print the trace to the mgc printer. Clearly label the trace plot! This means writing on the printout exactly what is happening.

After you have shown by simulation that your circuit functions and have printed out the simulation waveform or list, have the lab instructor date and sign it in your notebook.

Definitions

Propagation delay for a non-inverting gate (AND, OR)



Propagation delay time (input high to output high)

CIRCUIT SIMULATION USING ACCUSIM

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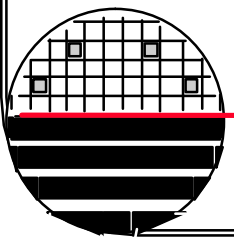
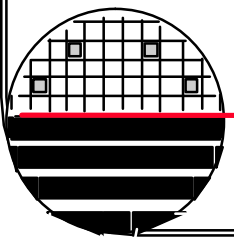
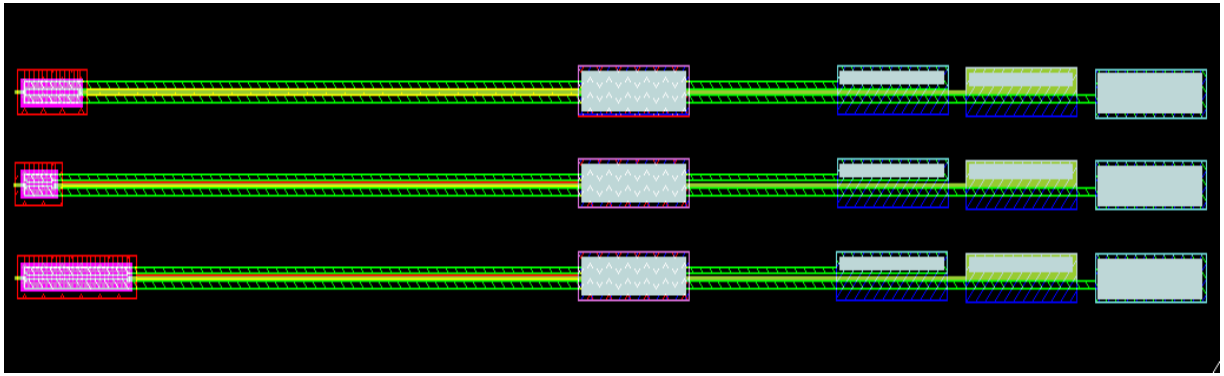


CIRCUIT SIMULATION USING ACCUSIM



IC LAYOUT USING "IC"

"ic" is the name of the layout editor used for microcircuit designs.



GETTING STARTED

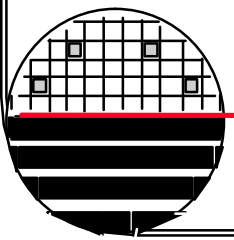
Usually the workstation screen will be blank, press any key to view a login window.

Login: username

Password: *********

The screen background will change and the control panel will appear. Click the left mouse button on the terminal icon. A window will appear that says Shell-Konsole on the top and has a Unix prompt inside. Type the command **ls** at the prompt to see a list of directories and files, the account should be empty.

Type **ic** <RET>, it will take a few seconds, then maximize the IC Station window by clicking the left mouse button on the large square in the upper right corner of the IC Station window.



SETTING PROCESS AND GRID

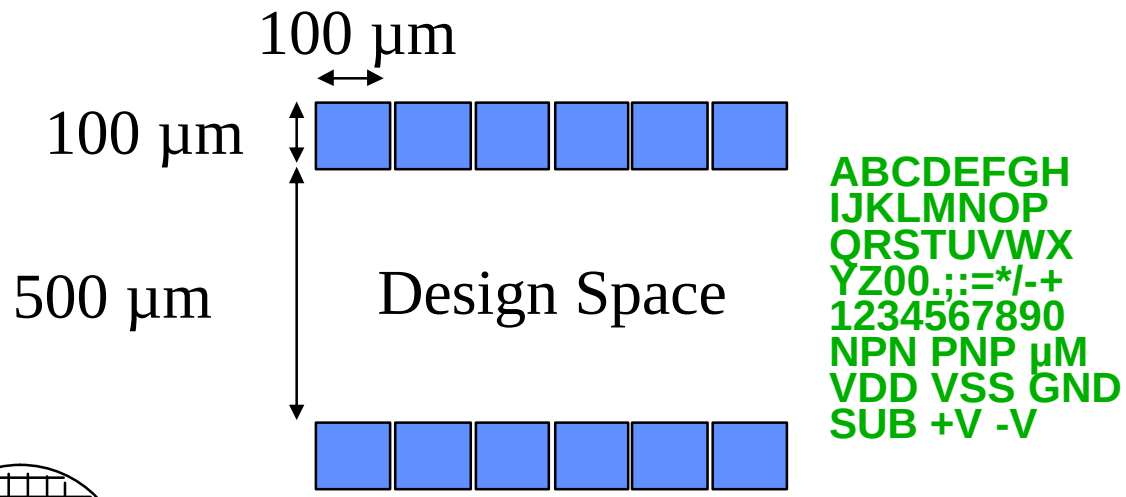
In the session menu palette on the right hand side of the screen, under Cell, select Create, using the lift mouse button. For cell name type the name your **design_name** . Also set the process to the RITPMOS process by typing **/tools/ritpub/process/ritpmos** in the process field and click on return OK. In the gray area under the banner at the top of the screen, the process should now read RITPMOS. Select other>show layer palette, click/drag on layers 1 to 4 then press select. Layers colors and shading should appear in upper right corner.

A large window with a black background and white dots should appear. We can now check the grid settings. In the top banner choose **Other > Window > Set Grid**. Set the Snap to 10 for both x and y, minor=1, major=10, then click on OK

The cursor position is given at the top center of the window. The layer being used and the number of items selected is shown at the top right. The 12 gray buttons which correspond to the F1-F8 and 4 white buttons allow multiple functions. For example push F2 to (Unselect All). To get the next function listed below that (Unselect Area) push shift and F2. To get the function listed on the bottom for the F2 key (Move) press the CTRL key and the F2 key.

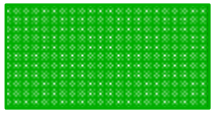
ADDING PAD CELL AND LETTERS

From the banner at the top of the page choose **Objects>add>cell**. A tan pop-up window will appear at the bottom of the page. Type in the following cell name, all lower case, **/tools/ritpub/padframes/ritpmos/ritpmos_12_pads** and click the left mouse button on the location button. Then position the cursor at the origin 0,0 and click the left mouse button. Click the left mouse button on the cancel button on the tan pop-up box. Press SHIFT and F8 to View All. You should see a white box with ritpmos_12_pads written inside it. Type flatten and select, OK. Press F2 to unselect all.

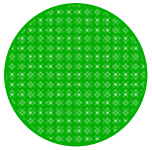


DRAWING BOXES, CIRCLES AND OBJECTS

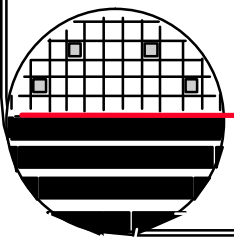
Select easy edit, Select Shape, Select Options, see the layer names, colors, shading pattern. **DRAW BOXES** by click and drag of mouse. Unselect by pressing F2 function key. The Notch command is useful to change the size of a selected box or merge rectangular shapes into more complex objects. The following command will draw a 3000 µm by 3000 µm box with level 5 color/shading. **$add_shape([[0,0],[3000,3000]],5)**



DRAW CIRCLES by typing **$set_location_mode(@arc)** return. The following command will draw a 100µm radius circle centered at (0,0) using 300 straight line segments.
$add_shape($get_circle([0,0],[100,0],300),3)
To reset to rectangles type $set_location_mode(@line) return.



SELECT OBJECTS by clicking or by click and drag. Selected objects will appear to have a bright outline. Selected objects can be moved (**Move**), copied (**Copy**), deleted (**Del**) or notched (**Notc**). To **Unselect** objects press F2.



ADJUSTING VIEW

ZOOM IN OUT: pressing the + or - sign on right key pad will zoom in or out. Also pressing shift + F8 will zoom so that all objects are in the view area. Select view then area and click and drag a rectangle will zoom so that the objects in the rectangle are in the view area.

MOVING VIEW CENTER: pressing the middle mouse button will center the view around the pointer.

LASER PRINT OUTPUT: Select File and Print, OK. This gives a laser printer output of entire cell. Select printer **prec10**, clear width, len, pages, scale by using backspace so nothing is in those boxes. Say OK.

PRINT PART OF LAYOUT: first create a panel. Under objects, select add a panel, name it and click on rectangle symbol. Then use the left mouse button to drag a rectangle around the objects you want in the panel to be printed. Then select File and Print and enter panel name, click on print set up, printer is **prec10**, clear width, len, pages, scale by using backspace so nothing is in those boxes. Say OK.

OTHER – ADDING TEXT

ADDING TEXT: From the banner at the top of the page choose **Objects>add>cell**. A tan pop-up window will appear at the bottom of the page. Type in the following cell name, all lower case, **/tools/ritpub/padframes/ritpmos/ritpmos_12_pads** and click the left mouse button on the location button. Then position the cursor to the side of your layout and click the left mouse button. Click the left mouse button on the cancel button on the tan pop-up box. Press SHIFT and F8 to View All. You should see a white box with ritpmos_12_pads written inside it. Type flatten and select, OK. Press F2 to unselect all. Use select and copy to place letters you want. To change letters to a different layer use objects and **set layers**. Don't forget to delete the extra letters and numbers you don't want.

ADDING TEXT: Open another layout design. Type **$add_device("$pgtext")** . Once the text is correct save file. Go back to your design and Add/Cell browse for the name you used to save the file. Use the scale option to make the lettering bigger. Try 3 instead of 1.

CHANGING SIZE OF TEXT: Bring in the **ritpmos_12_pads** as indicated above. Scale can be set to some number before the cell is flattened. Try 3 to make letters 100 um high.

SETTING CELL ORIGIN: under CONTEXT

OTHER

COPY A CELL FROM A STUDENTS ACCOUNT TO ume ACCOUNT: To copy from one students account to ume account

1. From the menu bar: File>Open>Cell
    1. Use "Navigator" to locate the cell to be inserted
    2. Keeping the right mouse button depressed in the path window, copy to clipboard the path of the cell
    3. Cancel the Open Cell window
2. From the Menu bar: Objects >Add>Cell
    1. Keeping the right mouse button depresses in the Cell Name window, Paste the path that was copied above
    2. Click on Location and place the cell

COPY A CELL FROM A STUDENTS ACCOUNT TO ANOTHER ACCOUNT: To copy from one students account to any other account

1. Select MGC > Design Management . Copy Object
    1. From:/home/username/subdirectory/filename.*
    2. To:/dropbox/lffeee
2. From a term prompt type chmod 644 /dropbox/lffeee/filename.*
3. Then anyone can copy object from the dropbox to their account

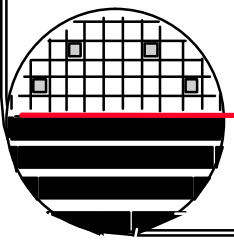
OTHER

COPY A CELL FROM A STUDENTS ACCOUNT TO ume ACCOUNT: To copy from one students account to any other account first have student set protection on their file, directory and account so world can read.

Type pwd 755
From the students main directory type chmod 755 . (note space then period)
if the file is in a sub directory type chmod 755 dirname
then from in the subdirectory type chmod 755 filename.* (note pereiod and *, no spaces)

Once that is done then in a different account press F5 and type path and filename, then peek, and flatten peeked.

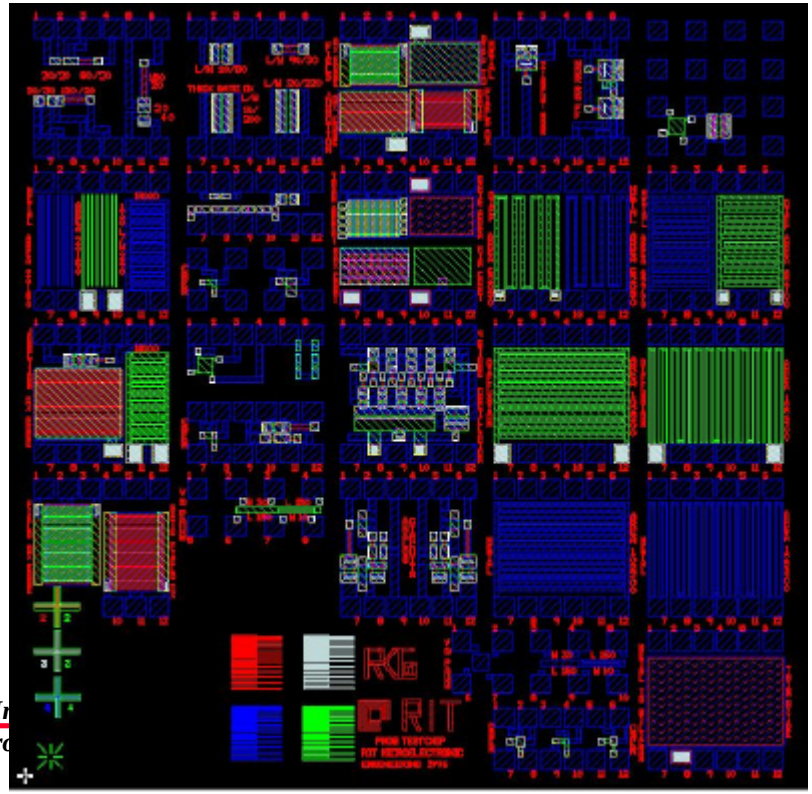
I understand the 755 setting will be reset to a default setting that does not allow others to read, automatically after about 5 minutes.



OTHER

GRAB A PLOT TO PUT IN POWERPOINT, ETC.: Open the K-Gear icon on the bottom of the desktop. Select K-Snapshot Screen Capture Program. Choose the capture mode you want. Set delay time to 5 seconds. Click on New Snapshot. Select Save As.

Email the picture to yourself using the K-Gear Bowser and mymail.rit.edu.



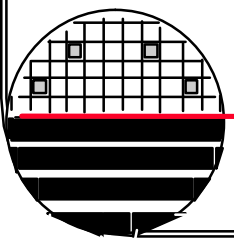
DATA PREP AND MASKMAKING

1. Using Mentor Graphics Design Tools, layout the device layers and save in mentor format. Mentor- ICGraph files (filename.iccel), all layers, polygons with up to 200 vertices

2. Convert the layout information to GDSII file format. GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

3. The GDSII format is then transferred to the CATS system for fracturing (conversion to MEBES format), and other data manipulations such as rotate, mirror, size, bias, and boolean combinations. MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only

4. Save the file and to transfer to the MEBES.



CREATING A GDS FILE

Rochester Institute of Technology
Semiconductor & Microsystems Fabrication Laboratory

Mask Making
Order Request

How to Create Your GDS File

1. At the command prompt, (ex. cjg9411@jafar:~$) change to the directory in which your Mentor Graphics design is located.

2. Type the following command to create your gds file: (remember, Unix is case sensitive, so a capital A is different from a lowercase a)

   iclink –co –so –i <directory>/<design name> -d –g <design name>.gds

   <directory> is the full path to the directory you are currently in (ex. /users/students/cjg9411/vlsi) and <design name> is the name of the Mentor Graphics file, without any extension. (Don't type the < or the > in the command, just the names of the directory and design)

3. Once iclink successfully creates the gds file, it will be placed in your home directory. Change back to that directory if you are not currently there, and issue the following command.

   cp <design name>.gds /dropbox/masks

   This copies the gds file over to the /dropbox/masks directory where we will be able to access it. Files will only stay in that folder for 2 weeks, after which they are automatically deleted.

4. Only one other command needs to be issued so that we will be able to have access to your file, and that is the following:

   /usr/bin/chmod 644 /dropbox/masks/<design name>.gds

   This changes the permissions such that we will have read-only access to your file. Only you will be able to delete your file if necessary before the 2-week limit.

MEBES - Manufacturing Electron Beam Exposure System

MASK PROCUREMENT

Design Layers: There may be many design layers in a design. For example the well layer and the lettering for the well layer may be on different design layers but merged to make the well mask. Resolution and overlay designs may be on different layers to be merged with other layers to make a mask. Boolean combinations are defined for the merge as well as other transformations such as bloat, rotate, and mirror. As a result this information needs to be made available to the mask provider as part of the mask order.

Clear field and Dark field describe the general appearance of the mask which is important in determining the layers in the streets between die.

Dummy features are sometimes added to a layer (tiling) such as shallow trench mask to improve performance of subsequent processes, such as CMP in the case of shallow trench.

MASK ORDER FORM

Rochester Institute of Technology
Semiconductor & Microsystems Fabrication Laboratory

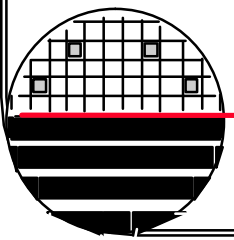
Mask Making
Order Request

RIT Mask order form is found at the following link:

http://smfl.microe.rit.edu/forms/Order_Request.dot

Customer Information	
Name	
Company	
Department	
Street Address	
City, State and Zip Code	,
Phone Number	( ) -
Project Code	
E-mail Address	
Order Date	July 23, 2007
Order Due Date	

Mask Information		
SEE PAGE 2 FOR INSTRUCTIONS ON CREATING YOUR GDS FILE!		
Design Name	.gds	
Number of Design Layers in Layout		
Number of Mask Levels		
Cell Layout Size	X: μm	Y: μm
Alignment Key (Center of Die is Origin)	X: μm	Y: μm
Fracture Resolution	☐ 0.5μm	☐ μm
Scale Factor	5X	
Orientation	☐ Mirror135	☐
Rotation	☐ None	☐
Plate Size	5" x 5" x 0.090" – Email for other sizes	
Number of Levels on Plate	1	
Array	☐ None ☐ Array with rows and columns	



MASK ORDER FORM

Rochester Institute of Technology
Microelectronic Engineering

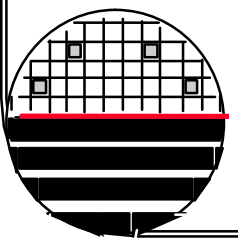
Date
Requestor Dr. Lynn Fuller

Attachment for Mask Order Form

Design Description: Sub-CMOS Mixed Analog Digital Test Chip **gds File:** /home/ume/subcmos_040203.gds

Fracture Resolution	0.5	**Mirror**	135	**Plate Size**	5"x5"x0.090"
Scale Factor	5X	**Rotate**	none	**# of levels/plate**	1
Array	none				

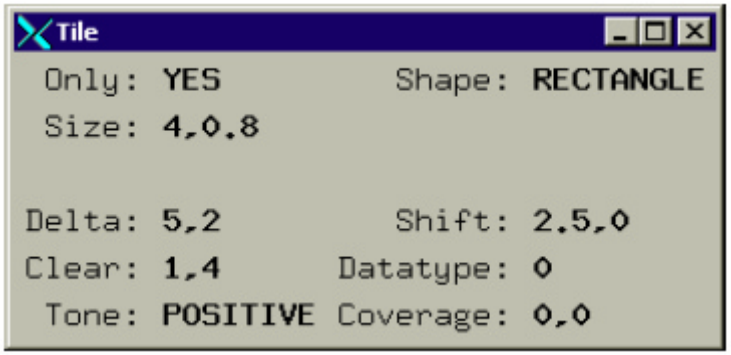
Design Layer Name	Number	Mask Level Name	Number	Boolean Function	Comments
NWELL	1	n-well.i	1	(1 OR 52 OR 51) INVERT	Dark Field Mask
		p-well.e	52		
		n-well.e	51		
ACTIVE	2	active-area.i	3	(3 OR 53)	Clear Field Mask
		active-area.e	53		
STOP	3	n-well.i	1	(1 OR 54)	Clear Field Mask
		n-implant.e	54		
PMOSVT	4	p-implant.i	5	(5 OR 55)	Clear Field Mask
		p-implant.e	55		
POLY	5	poly.i	6	none	Clear Field Mask, Bias layer 6 +0.5 µm
LDD-N	6	n-implant.i	4	(4 OR 56) INVERT	Dark Field Mask
		poly.e	56		
LDD-P	7	p-implant.i	5	(5 OR 56) INVERT	Dark Field Mask
		poly.e	56		
N+DS	8	n-implant.i	4	(4 OR 58) INVERT	Dark Field Mask
		contact_a.e	58		
P+DS	9	p-implant.i	5	(5 OR 57) INVERT	Dark Field Mask
		contact_p.e	57		
CC	10	contact_a.i	8	(8 OR 7) INVERT	Dark Field Mask
		contact_p.i	7		
METAL1	11	metal1.i	9	none	Clear Field Mask
VIA	12				not used in this design

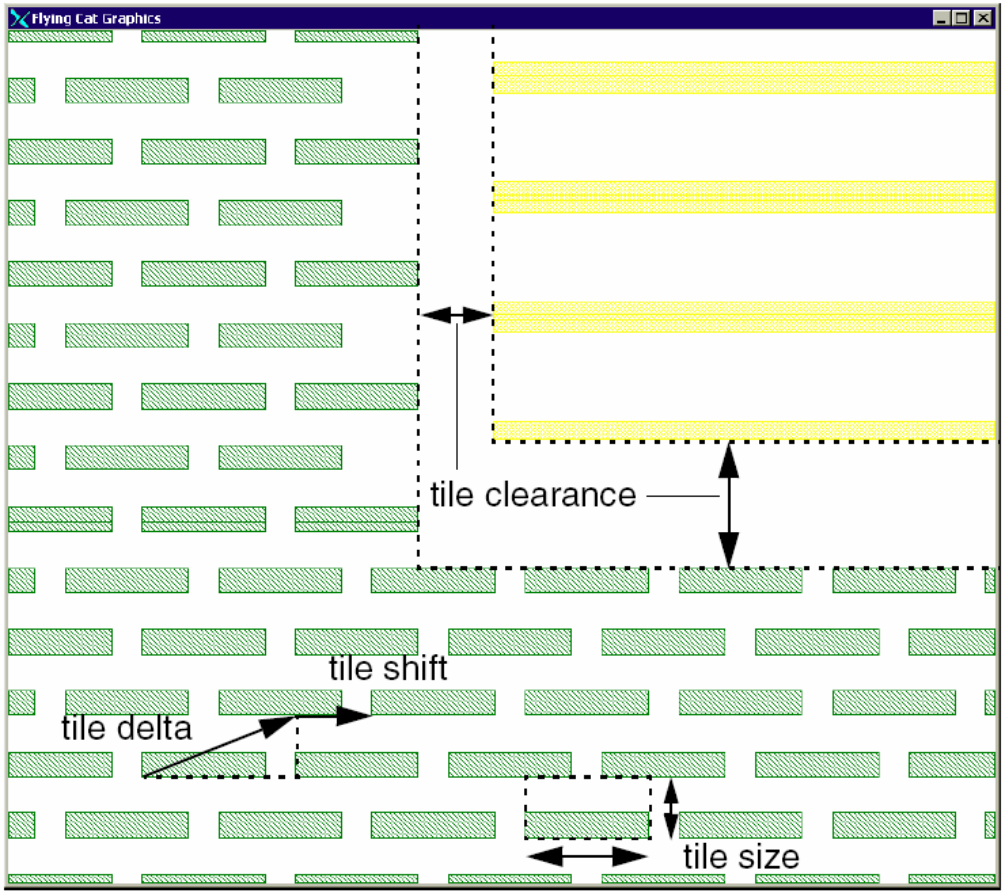


PHOTOMASK

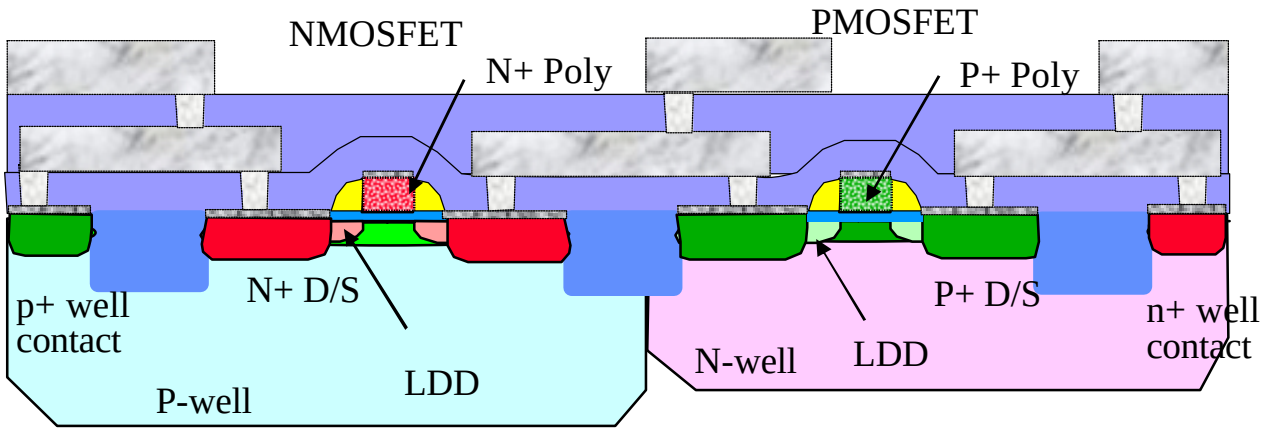
TILING FOR STI LAYER MASKMAKING

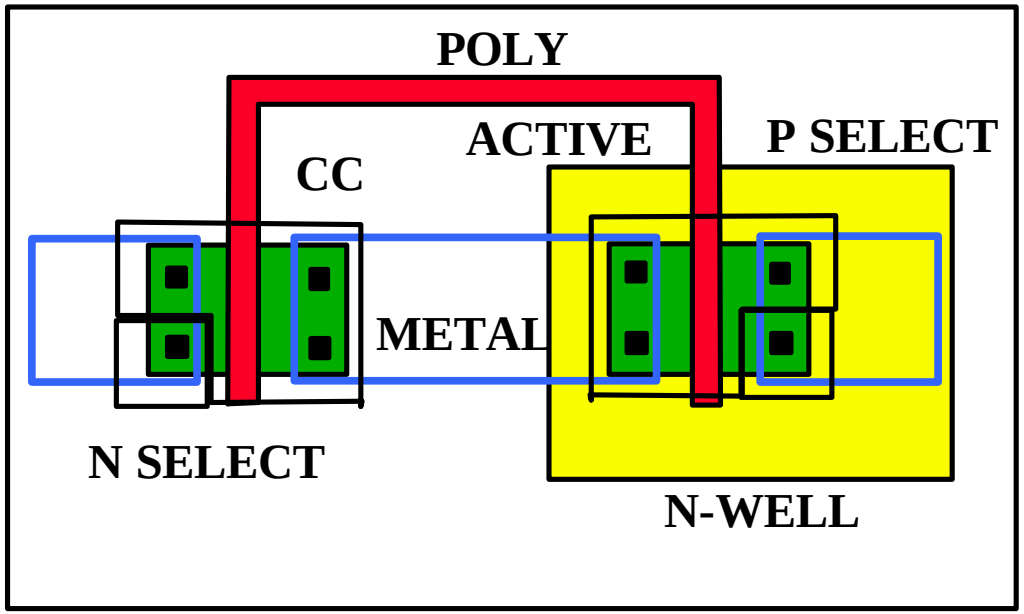
Synopsys, Inc.
CATS Software for transcription of CAD design files into readable e-beam and laser formats.

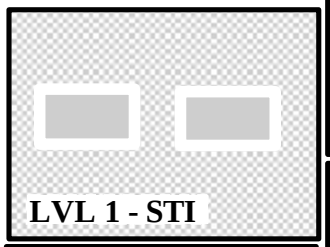


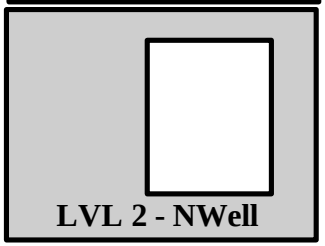


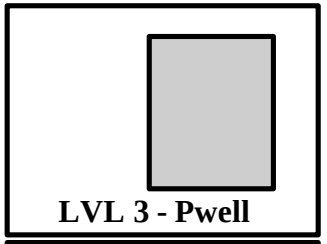
RIT ADVANCED CMOS PROCESS

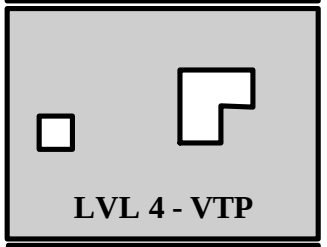


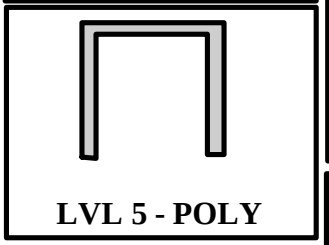




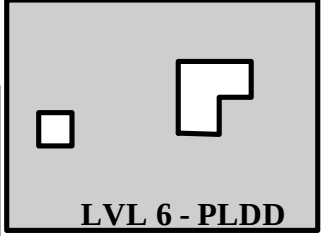


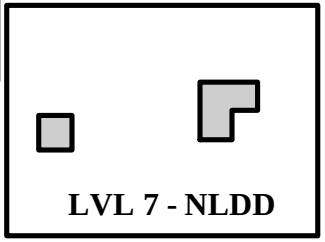


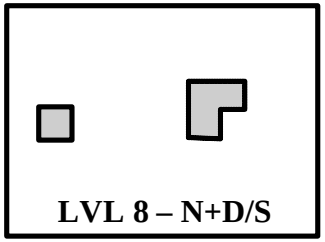


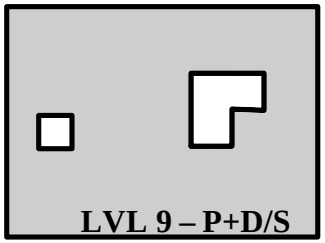


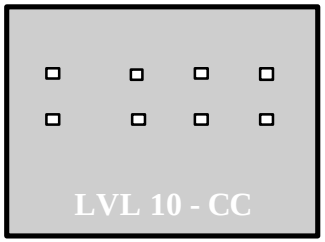
11 PHOTO LEVELS

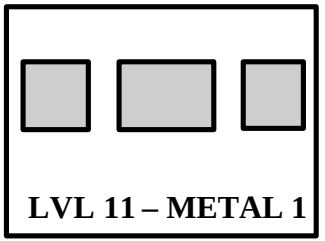




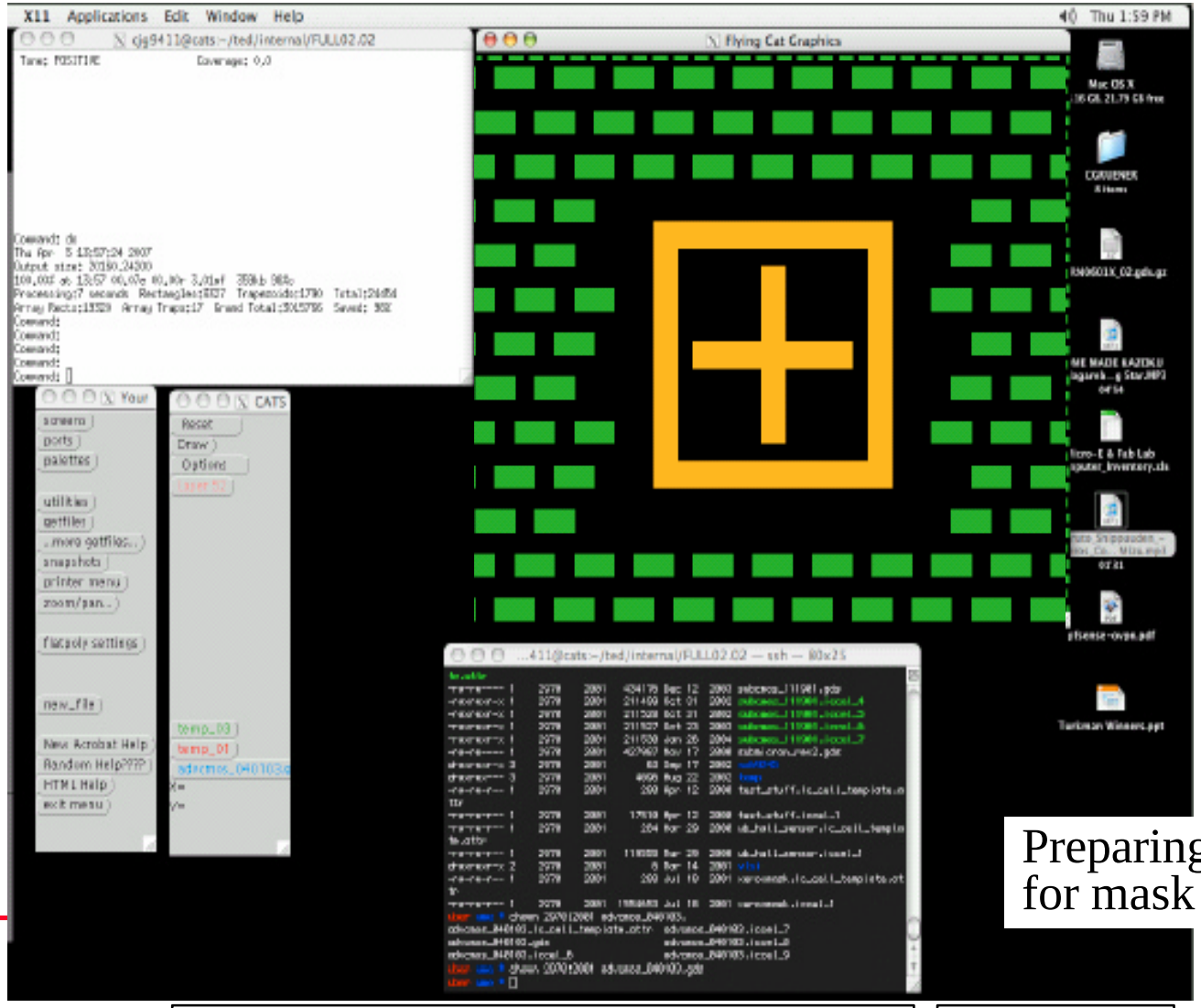








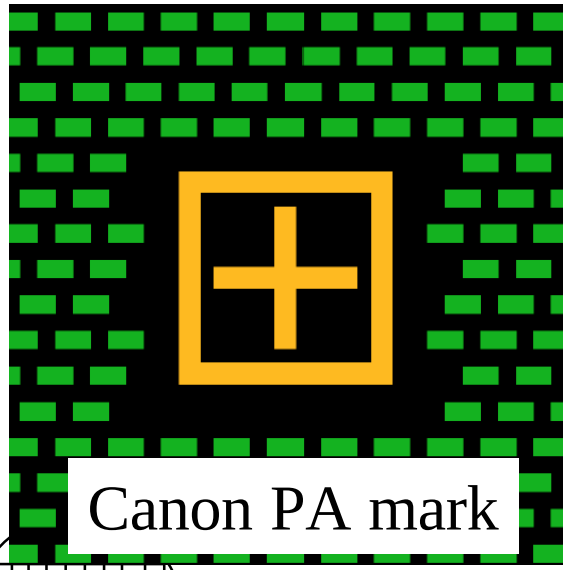
CATS



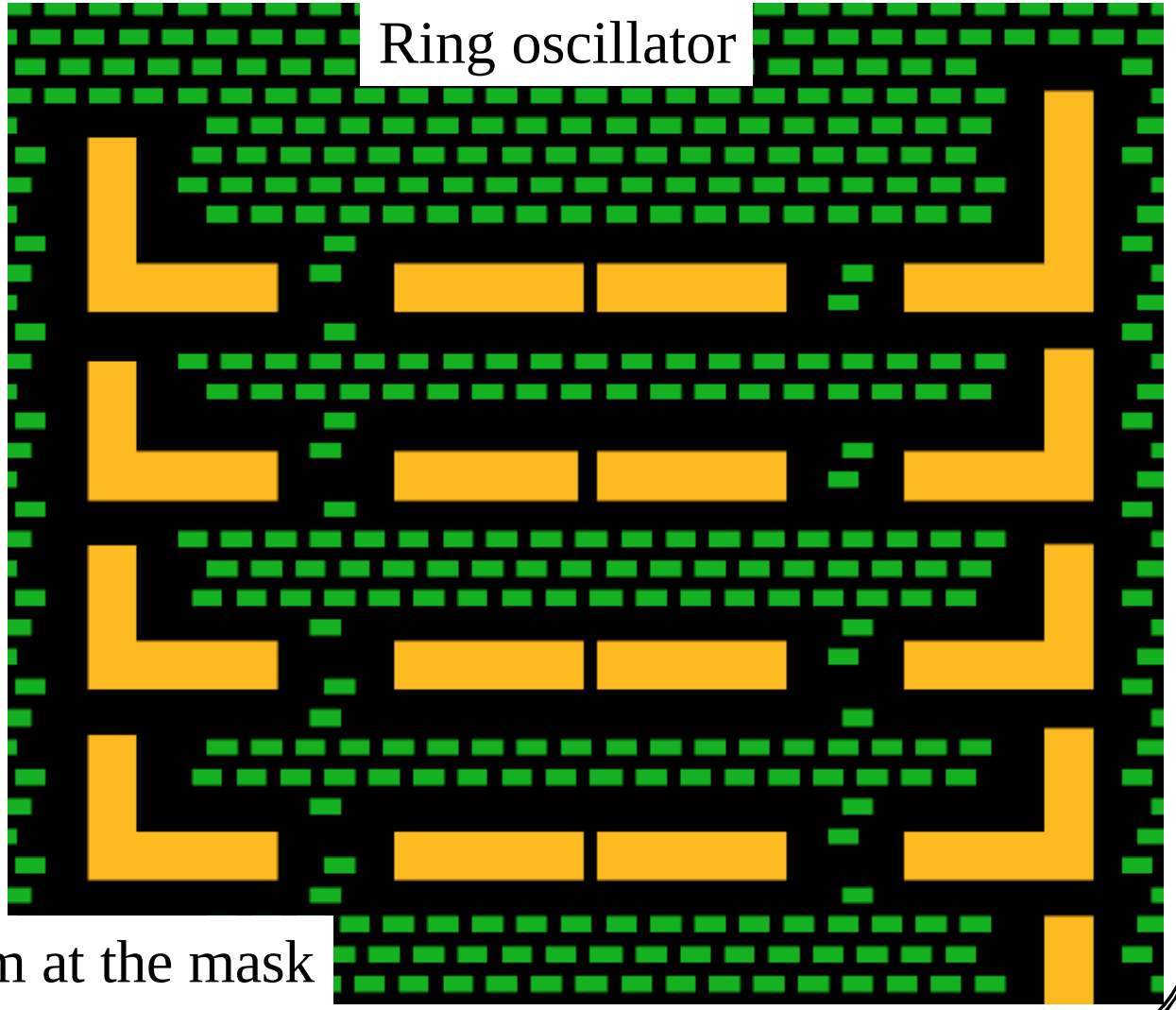
Preparing data files for mask making

TILING FOR RIT'S ADV-CMOS PROCESS STI LEVEL

COMPACT NO
TILE ONLY NO
TILE SHAPE RECTANGLE
TILE SIZE 50,25
DILE DELTA 75,50
TILE CLEAR 50,50
TILE SHIFT 25,0



Canon PA mark



Ring oscillator

Sizes are in µm at the mask

REFERENCES

1. Principles of CMOS VLSI Design, 2nd Ed., Neil H.E.Weste, Kmran Eshraghian, Addison Wesley, 1993.
2. Physical Design Automation of VLSI Systems, Bryan Preas, Michael Lorenzeti, Benjamin/Cummings, 1988.
3. VLSI Engineering, Thomas Dillinger, Prentice Hall, 1988.
4. Synopsys, Inc, CATS user guide, Y-2006.09, September 2006.