SMFL Users News Letter – Number 140715 V8.1

This News Letter is intended to provide information of interest to MicroE faculty and other users of the SMFL. It is a report on equipment and processes used in the SMFL with emphasis on changes, problems, and details that may not be generally available to users. I distribute this to the MicroE faculty and others. If you feel that this News Letter has some information that might be useful to your graduate students please forward it to them. Past newsletters are posted on Dr. Fuller's webpage.

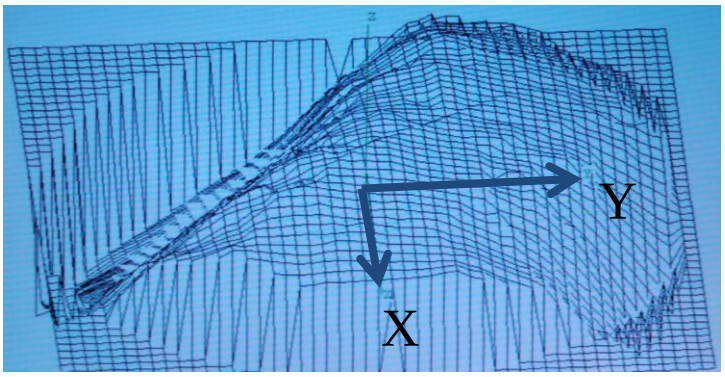
Thickness Measurement and Calibration for Aluminum Deposited in the CVC601:

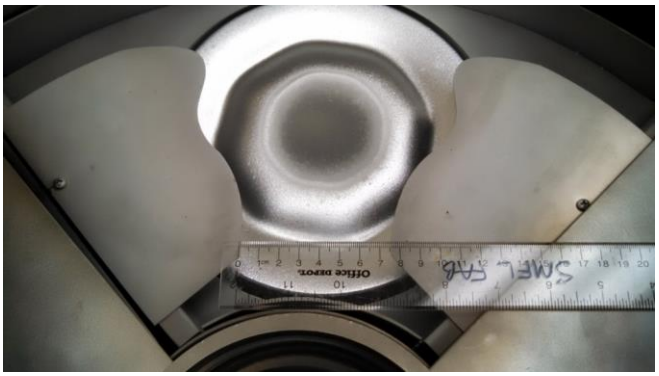
This document contains information on measurement and calibration of sputtered aluminum thickness for the CVC601 tool. After sputtering aluminum the thickness is measured using the CDE Resistivity Mapper (4pt Probe). The thickness, W, is found from the known Resistivity of Aluminum, Rho, divided by the measured Sheet Resistance, Rs.

$$Rs = (\pi/\ln 2)(V/I) \; ; \text{Thickness } W = Rho/Rs$$

These measurements are Calibrated by comparing to thickness measured using the Tencore P2.

Our report is given on my webpage: http://people.rit.edu/lffeee/AluminumCalibration.pdf





The shields appear to be too narrow near the center of the tool giving thinner coating on the inside edge of the wafer. This was verified using the 3D map from the 4pt probe. Periodic shield shape and location adjustments may be required to keep the uniformity as desired.

Testing of PMOS Digital Circuits Using the Analog Discovery Module:

The Logic Analyzer interprets a "high" as +3.3 V, and "low" as 0 V, in PMOS logic "high" is – 5 V and "low" is 0V. An operational amplifier (Op Amp) is used to convert the digital pattern generator 0 to +3.3 V signal to 0 to -5V that becomes the input to the PMOS logic circuit. A similar Op Amp circuit is used to convert the PMOS logic output to logic levels that can be interpreted by the logic analyzer. The logic analyzer interprets positive voltages (more than +1.65V) as logic high and lower voltages (including negative voltages) as logic low. These circuits and other details are shown in detail in our report.

It is on my webpage: http://people.rit.edu/lffeee//PMOS_Digital_Test.pdf