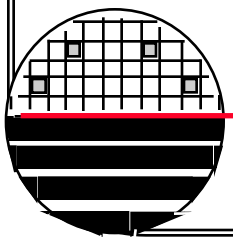
ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

NMOS Inverter Lab

Dr. Lynn Fuller
Webpage: http://people.rit.edu/lffeee/
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035

Email: Lynn.Fuller@rit.edu
MicroE webpage: http://www.microe.rit.edu

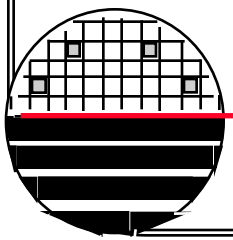


INTRODUCTION

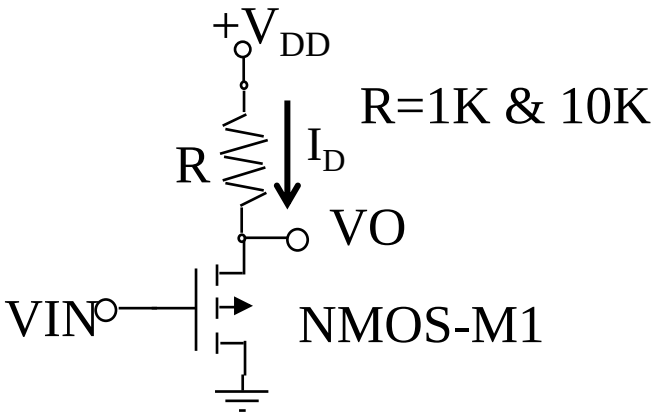
In this lab we will investigate the NMOS Inverter with different loads. Including:

1. Resistor Load = 1K
2. Resistor Load = 10K
3. Enhancement NMOS Load with Substrate connected to the Ground, and Gate connected to the Drain
4. Enhancement NMOS Load with Substrate connected to the Source, and Gate connected to the Drain
5. Enhancement NMOS Load with Substrate connected to Ground and Gate connected to V++

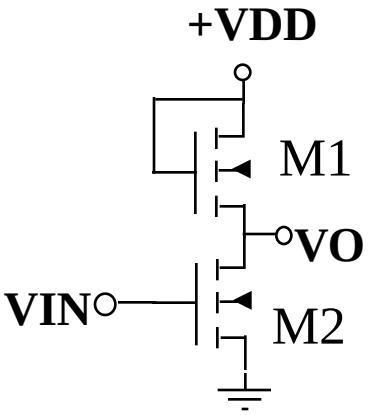
The VTC will be found using SPICE and the noise margins found from the points where the derivative of the VTC is -1, these simulations are done with arbitrary L and W's given in the lab document. Not L and W's of the ALD1103 chip.



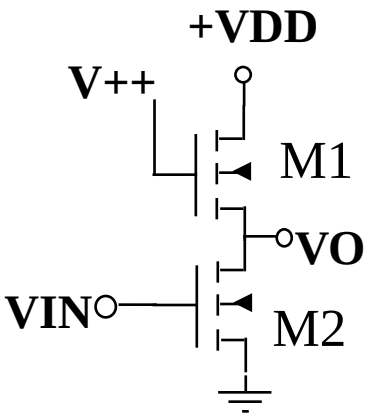
VARIOUS NMOS INVERTERS



RESISTOR LOAD

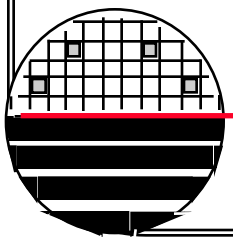


NMOS ENHANCEMENT LOAD



NMOS ENHANCEMENT LOAD V++ GATE BIAS

Also, NMOS Enhancement Load with M1 substrate connected to Ground or with M1 substrate connected to the M1 Source

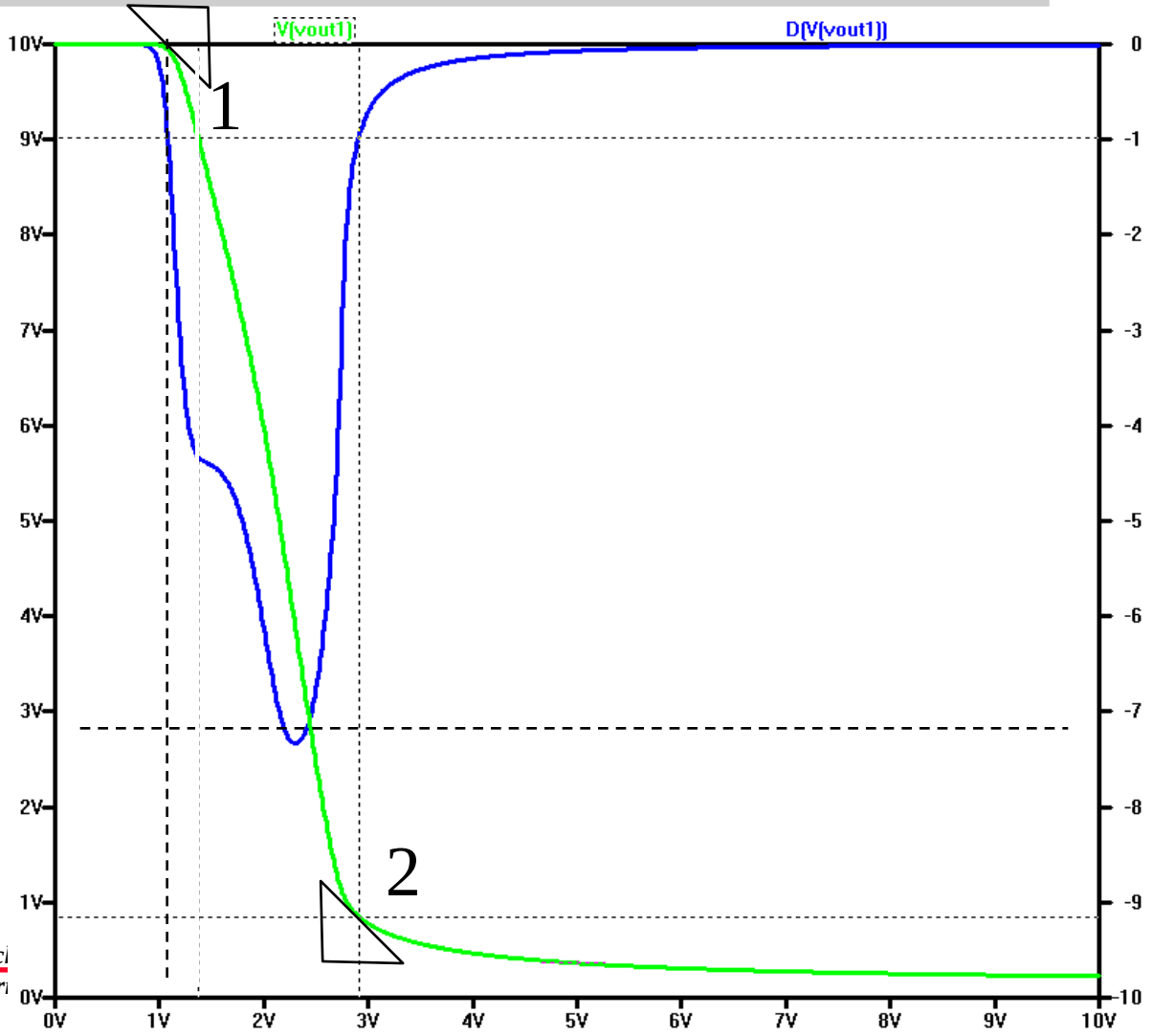


SPICE CALCULATIONS FOR NOISE MARGINS

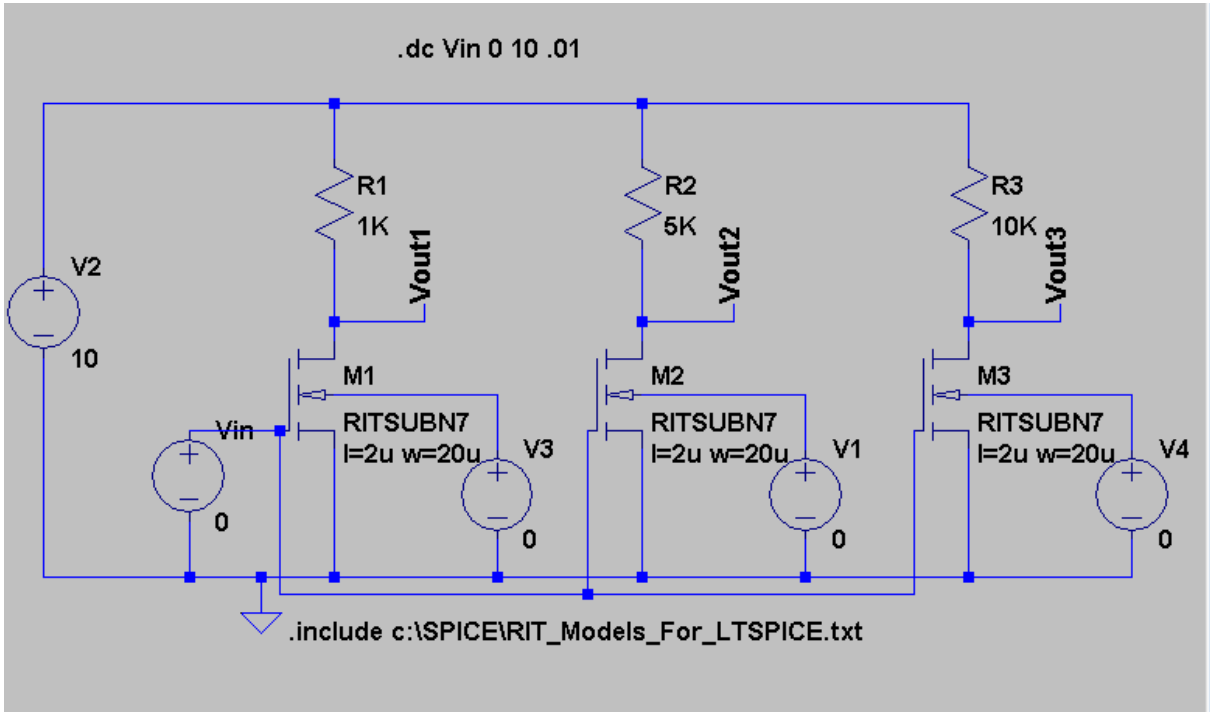
RL = 10K

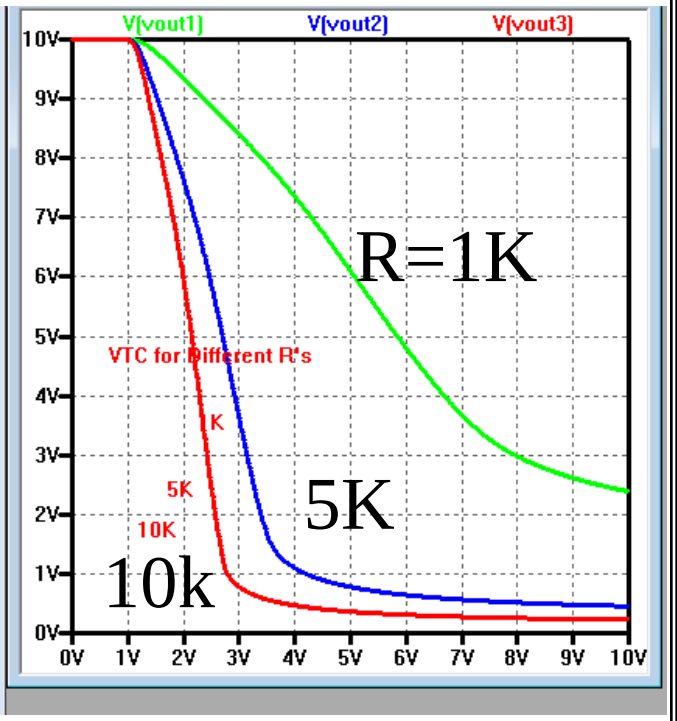
VIL = 1.0
VIH = 2.91
VOH = 10.0
VOL = 0.91
Δ0 = VIL – VOL
=1.0-0.91= 0.08
Δ1=VOH-VIH=
=10-2.91=7.09

Max Gain = -7.2

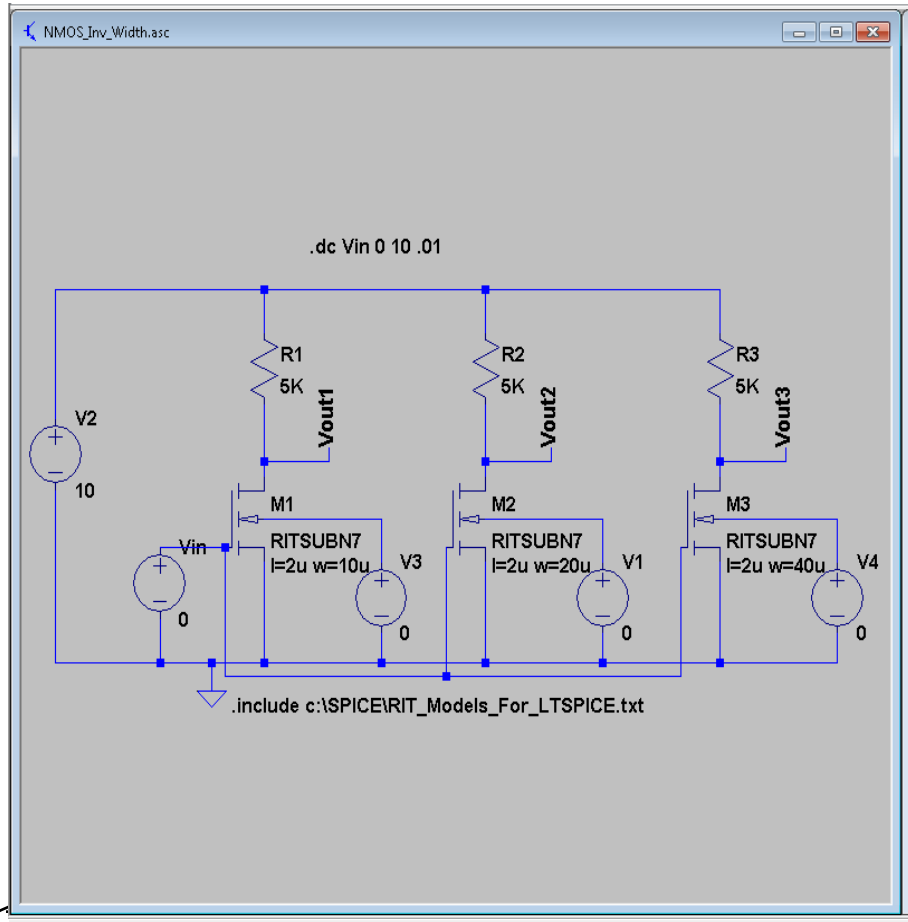


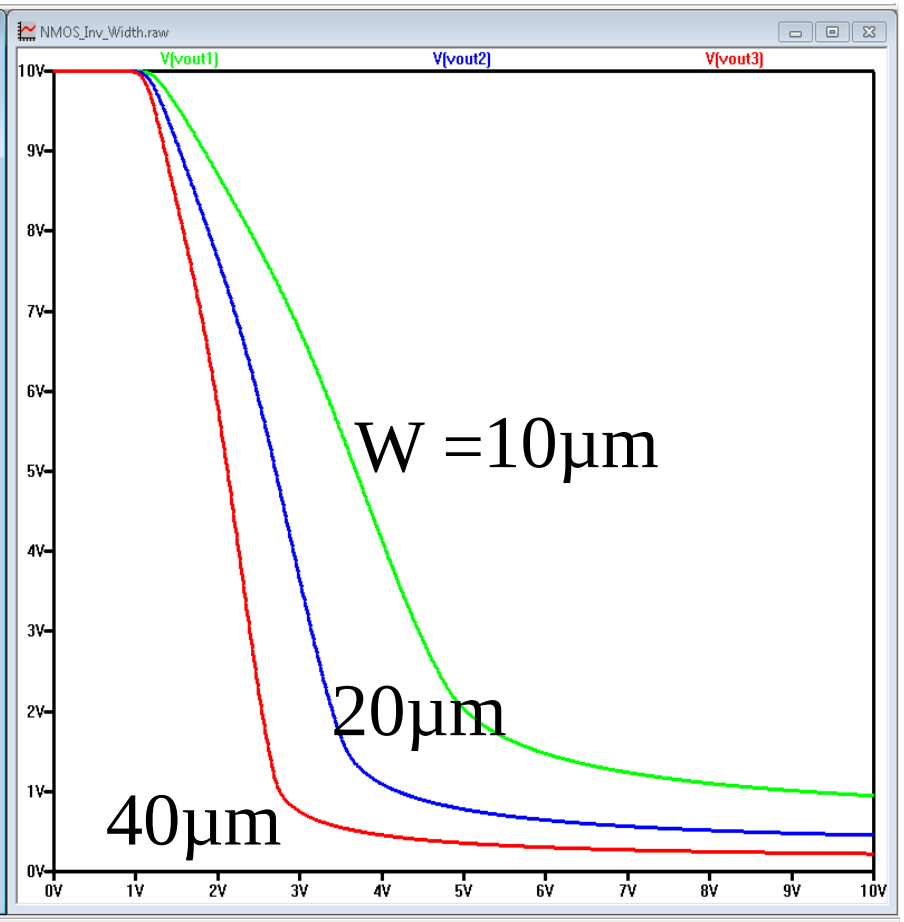
LTSPICE - INVERTER VTC – FOR DIFFERENT RL



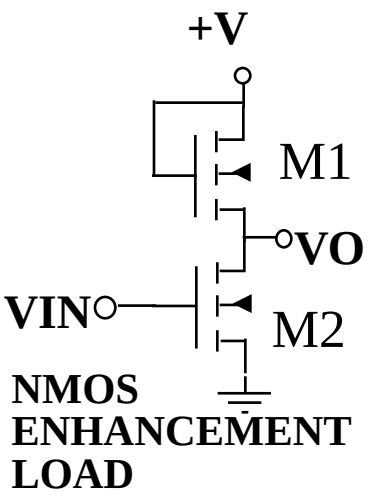


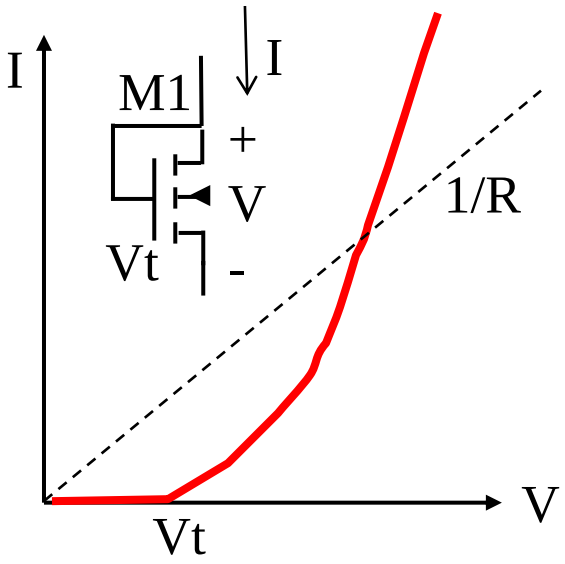
LTSPICE – INVERTER VTC FOR DIFFERENT W

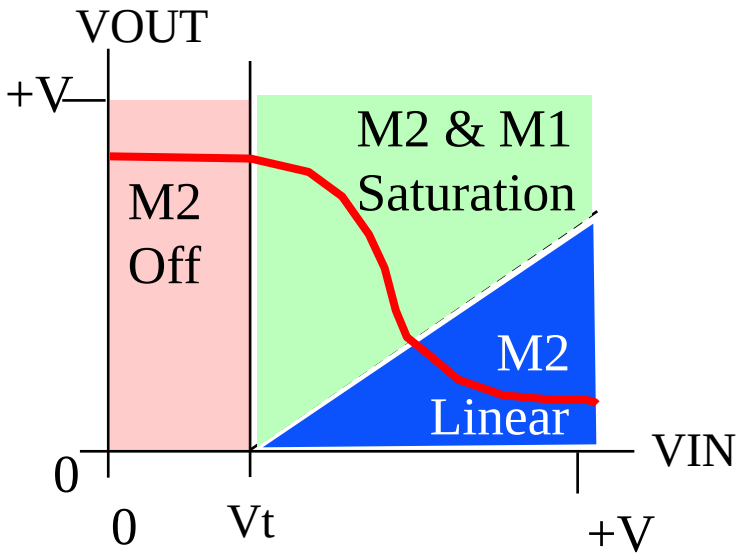




VTC NMOS INVERTER- NMOS ENHANCEMENT LOAD







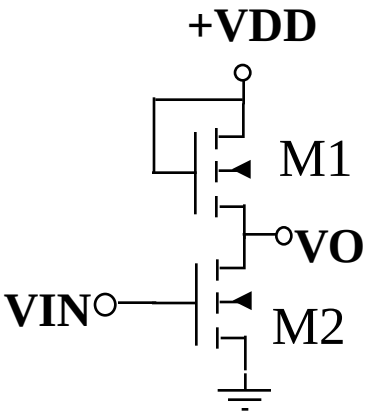
M2 is the switch and M1 is the load. The load limits the current when M2 is on. The load could be a resistor but an NMOS transistor with gate connected to the drain is smaller in size and also limits current. See the I-V characteristics. In the first quadrant the transistor approximates the resistor. However, Vout high is below VDD by the threshold voltage of M1

Cox' = Cox/Area = εoεr/Xox

$$I_D = \frac{\mu W\, Cox'\, (Vg-Vt)^2}{2L}$$

Saturation

DERIVATION OF GAIN EXPRESSION



Assume Vout = Vin and both transistors are in saturation for the steep part of the VTC. The current in M1 is equal to the current in M2 is equal. Also assume Vt is the same for both transistors.

$$I_2 = I_1$$

$$uW_2\ Cox'/2L_2\ (V_G-V_t)^2 = uW_1\ Cox'/2L_1\ (V_G-V_t)^2$$

$$W_2/L_2\ (V_G-V_t)^2 = W_1/L_1\ (V_G-V_t)^2$$

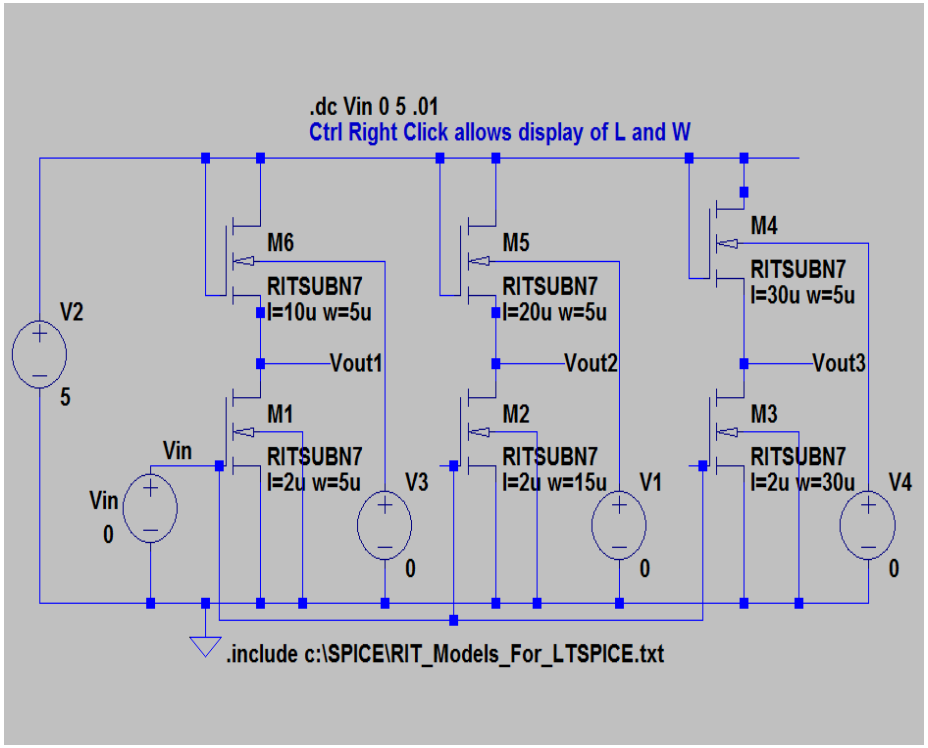
But, V_{G2} is VIN and V_{G1} = VO +Vt

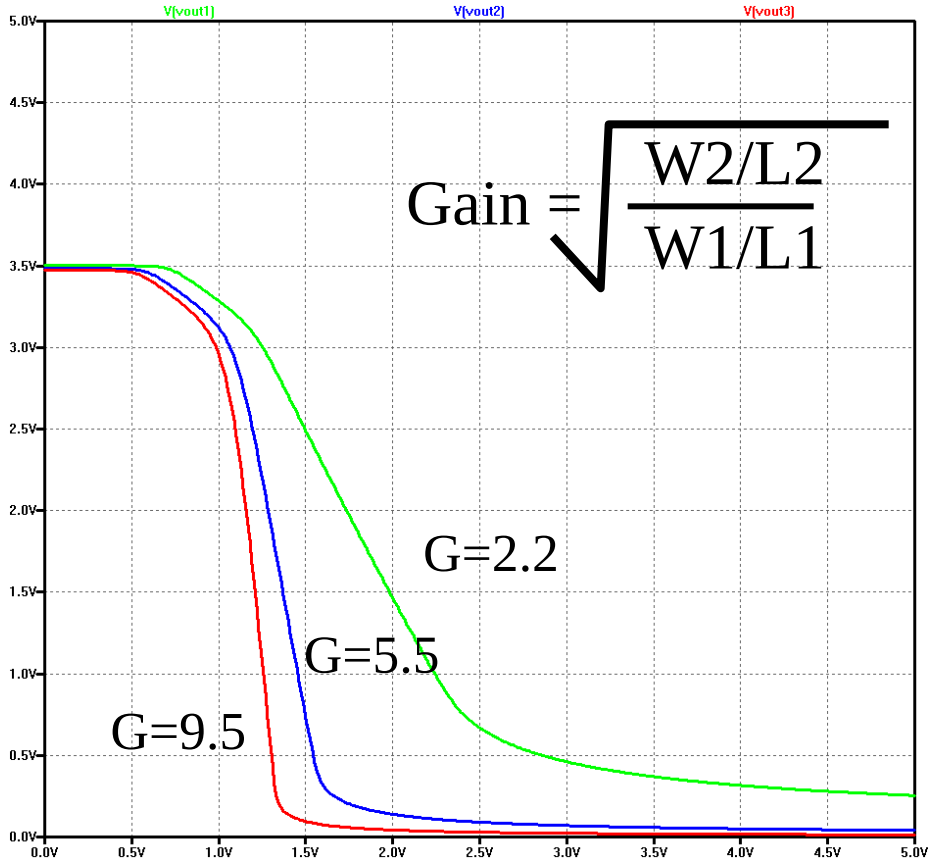
$$(W_2/L_2)\ (V_{IN}-V_t)^2 = (W_1/L_{1)}\ (VO + Vt - V_t)^2$$

$$Gain = \delta\ VO/\delta\ V_{IN}$$

$$Gain = \sqrt{\frac{W2/L2}{W1/L1}}$$

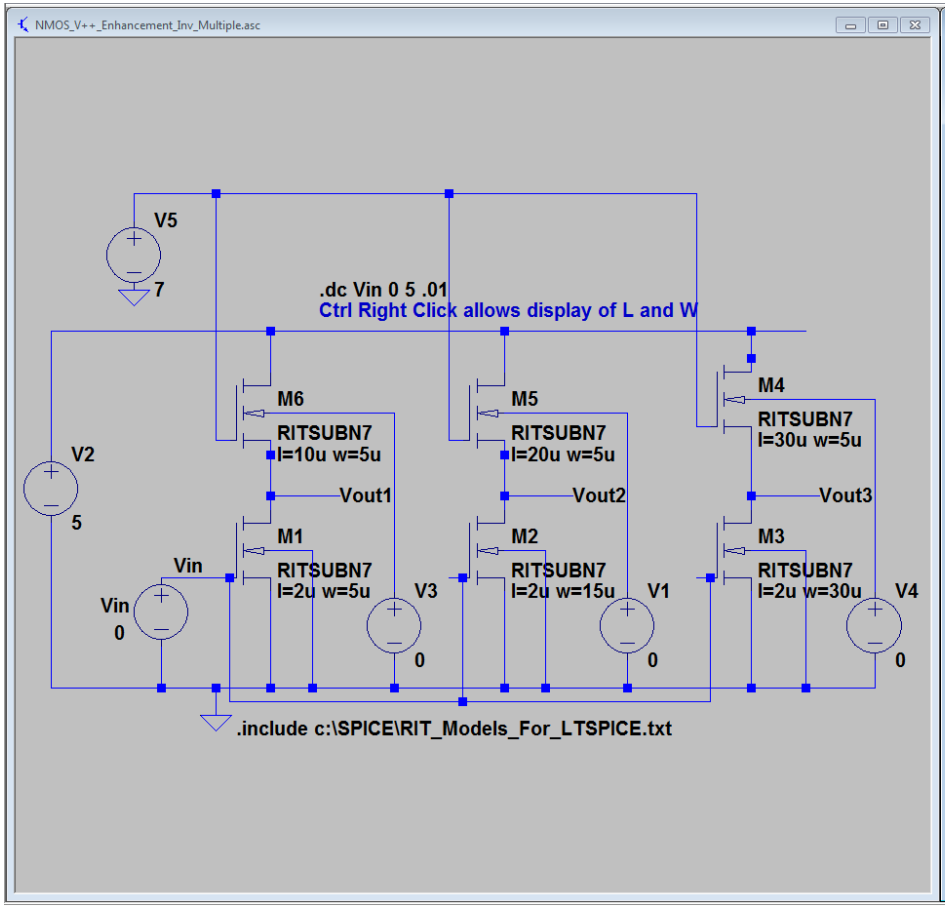
VTC NMOS INVERTER- NMOS ENHANCEMENT LOAD

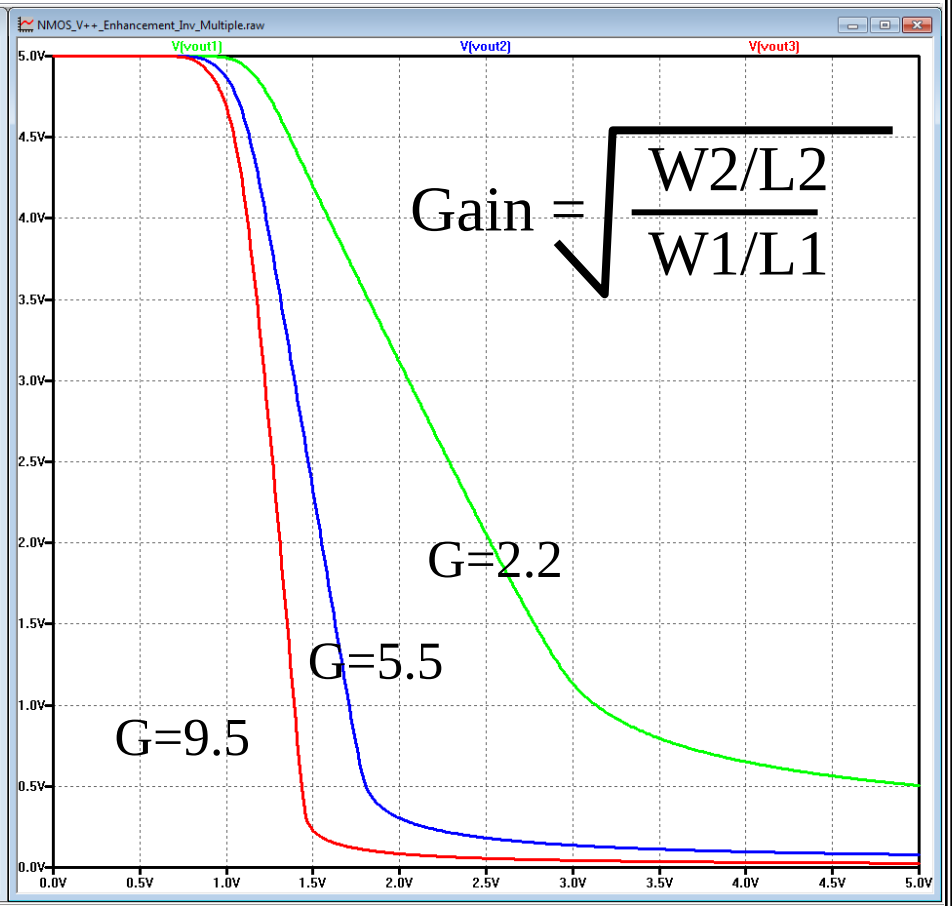




Note: increasing L of the load is equivalent to increasing R of a resistor load, Vout high is Vdd – Vt_{M1} , Gain is shown.

VTC NMOS INVERTER- NMOS ENHANCEMENT LOAD AND V++ GATE BIAS





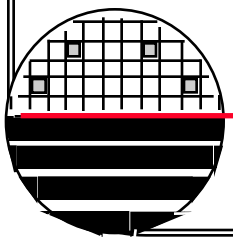
Note: increasing L of the load is equivalent to increasing R of a resistor load, Vout high is Vdd, Gain is shown.

SUMMARY

This laboratory is mostly a SPICE investigation of various NMOS inverter realizations. The VTC is found for given L's and W's. Values are found for noise margin calculations. Appropriate SPICE models are used for the transistor sizes used in the simulations.

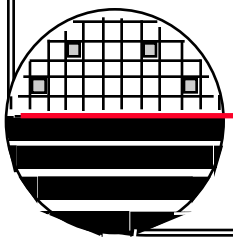
The build part of the laboratory is limited to the L and W of the transistors provided inside the ALD1103 chip. These sizes are L=10u and W=880u. Calculation of the Gain of the inverter with NMOS load gives a gain of 1 which is not sufficient for a good VTC. However, we can observe the VoH for the different NMOS load inverter realizations.

The resistor load inverter works okay.



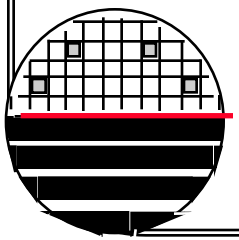
REFERENCES

1. Sedra and Smith, 5.1-5.4
2. Device Electronics for Integrated Circuits, 2nd Edition, Kamins and Muller, John Wiley and Sons, 1986.
3. The Bipolar Junction Transistor, 2nd Edition, Gerald Neudeck, Addison-Wesley, 1989.



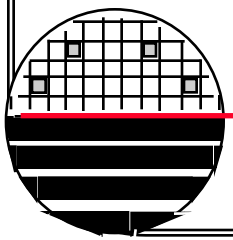
SPICE MODELS FOR MOSFETS

```
*SPICE MODELS FOR RIT DEVICES - DR. LYNN FULLER 4-10-2014
*LOCATION DR.FULLER'S WEBPAGE - http://people.rit.edu/lffeee/CMOS.htm
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=1u W=200u
.MODEL RIT4007N7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=1u W=200u
.MODEL RIT4007P7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



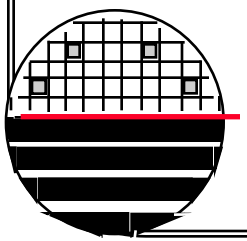
SPICE MODELS FOR MOSFETS

```
*Used for ALD1103 chips
*Note: Properties L=10u W=880u
.MODEL RITALDN3 NMOS (LEVEL=3
+TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0= 1215 VTO=0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5
+NSUB=1.57E16 XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)
*
*Used for ALD1103 chips
*Note: Properties L=10u W=880u
.MODEL RITALDP3 PMOS (LEVEL=3
+TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0=550 VTO=-0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5
+NSUB=1.57E16 XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)
```



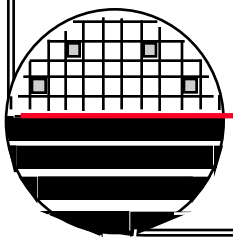
SPICE MODELS FOR MOSFETS

```
*4-4-2013 LTSPICE uses Level=8
*For RIT Sub-CMOS 150 process with L=2u
.MODEL RITSUBN8 NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013  LTSPICE uses Level=8
*For RIT Sub-CMOS 150 process with L=2u
.MODEL RITSUBP8 PMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



SPICE MODELS FOR MOSFETS

* From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL RITSUBP7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)



SPICE MODELS FOR MOSFETS

```
*4-4-2013  LTSPICE uses Level=8
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSN     NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013  LTSPICE uses Level=8
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSP     PMOS (LEVEL=8
+TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
```