

**ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING**

CMOS Process Integration Course Outline

Dr. Lynn Fuller

webpage: <http://people.rit.edu/lffeee>

Electrical and Microelectronic Engineering

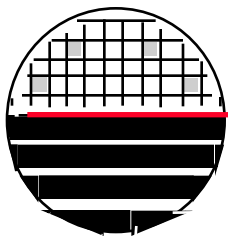
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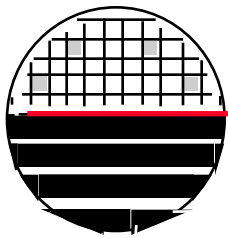


4-27-2014 Outline.ppt

INTRODUCTION

This course offers detailed instruction on the physics behind the operation of a modern integrated circuit, and the processing technologies required to make them. Also covered is the process integration techniques from design thru manufacturing of nanoscale devices.

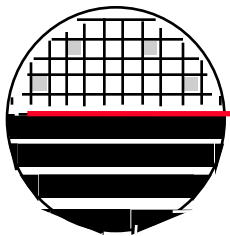
- 1. Basic Device Operation:** Participants learn the fundamentals of transistor operation. They learn why CMOS (Complimentary Metal Oxide Semiconductor) devices dominate the industry today.
- 2. Fabrication Technologies:** Participants learn the fundamental manufacturing technologies that are used to make modern integrated circuits. They learn the typical CMOS process flows used in integrated circuit fabrication.
- 3. Current Issues in Process Integration:** Participants learn how device operation is increasingly constrained by three parameters. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
- 4. An Overview of Issues Related to Process Integration:** Participants learn about the image of new materials, yield, reliability and scaling on technology and process integration. They receive an overview of the major reliability mechanisms that affect silicon ICs today.



COURSE OBJECTIVES

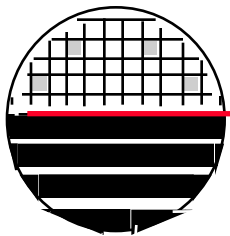
Course Objectives: Participants will understand

1. The requirements for realizing nano-scale MOSFETs.
2. Scaling of MOSFET in deep sub-micrometer regime.
3. Process technologies used in the fabrication of nano-scale MOSFETs.
4. Why and how strained silicon is used in today's nano-scale MOSFETs.
5. New device structures such as FinFETs.
6. How process modeling is used in process integration.
7. How to evaluate and compare CMOS device performance.
8. Improve technical vocabulary and understanding as it relates to advanced CMOS technologies.



TOPICS COVERED

Review of Process Technology
Review of Semiconductor Device Physics (MOSFETs)
Advanced MOSFET
Deep Sub-micrometer Process Technology
Strained Silicon Devices
Fin FETs
Advanced Process Technology
(High K, Metal Gate, Steep Retrograde Wells, etc.)
Advanced Lithography
Process Integration
Advanced CMOS Process Integration
Technology CAD (SILVACO)
MOSFET Device Test (gm, V_t , DIBL, Sub V_t swing, gate delay, ft)
Reliability (FIT, accelerated test)
Back End Process Technology (Low K, copper, CMP, Dual
Damascene, Salicide)



LECTURE DOCUMENTS

April 20, 2014
[Dr. Lynn Fuller](#)

<http://people.rit.edu/lffeee/CMOS-Shortcourse.html>

Shortcourse: Process Integration

Lesson	Discussion Topic	Lecture Documents	Reference Documents
	Introduction	Outline.pdf	
1.	Review of Device and Process Technology	REVIEW.pdf	Calculations.xls
2.	Advanced MOSFET Basics	MOSFET Basics.pdf	
3.	Advanced CMOS Technology Parts 1	ADV CMOS Part 1.pdf	
4.	Advanced CMOS Technology Part 3	ADV CMOS Part3.pdf	
5.	Calculations for Advanced CMOS	Adv CMOS Calc.pdf	
6.	Deep Submicrometer Scaling	250nmProcessIntegration.pdf	
7.	Lithography	Lithography-ASML.pdf	
8.	Advanced CMOS Process Integration	AdvCmosProcessIntegration.pdf	
9.	Introduction to TCAD	TCAD-SILVACO.pdf	
10.	RIT's 100nm CMOS Process Simulation	100nmProcessSimulation.pdf	
11.	RIT's 100nm CMOS Process Crossections	100nmCMOS_Xsection.pdf	
12.	Testing Device Problem Analysis	Device Test.pdf	
13.	Defects, Yield and Reliability	Reliability.pdf Defects.pdf	
14.	Back End Processes	Back End.pdf	Gas Flow.wmv

ESTIMATED TIME SCHEDULE

Day One

Review of Semiconductor Technology	1.5 hr
MOSFET Basics	1.5 hr
Advanced CMOS Process Technology	1.0 hr

Lunch

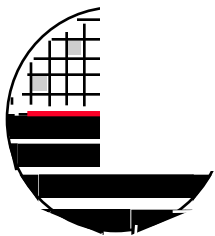
Advanced CMOS Process Technologies	2.0 hr
Process Design Calculations	2.0 hr

Day Two

Deep Submicron Scaling	1.0 hr
Lithography	1.0 hr
Advanced CMOS Process Integration	2.0 hr

Lunch

Process Modeling TCAD (SILVACO)	1.0 hr
CMOS Device Testing	1.0 hr
Defects, Yield and Reliability	1.0 hr
Other	1.0 hr



TEXTBOOK/REFERENCES

There is no text for this course. You may wish to use the following textbooks as references. Lecture notes are available on Dr. Fuller's webpage: <http://people.rit.edu/lffeee>

1. Silicon Processing for the VLSI Era Volume I, S. Wolf and R.N. Tauber, Lattice Press, Sunset Beach, CA, 1986.
2. The Science and Engineering of Microelectronic Fabrication, S.A. Campbell, Oxford University Press, New York, NY, 1996.
3. VLSI Technology, Edited by S.M. Sze, McGraw-Hill Book Company, 1983.

