ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

PMOS Integrated Circuit Test Results

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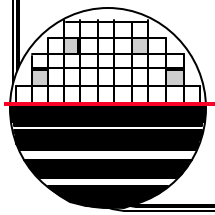
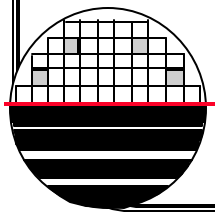


OUTLINE

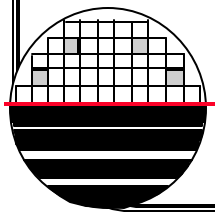
Introduction
Inverter
NOR (2,3,4 input)
XOR
4:2 Encoder
4 input Multiplexer
Clocked Data Latch
Full Adder
1:4 Demultiplexer/Decoder
JK Flip Flop
Analog Multiplexer
Binary Counter



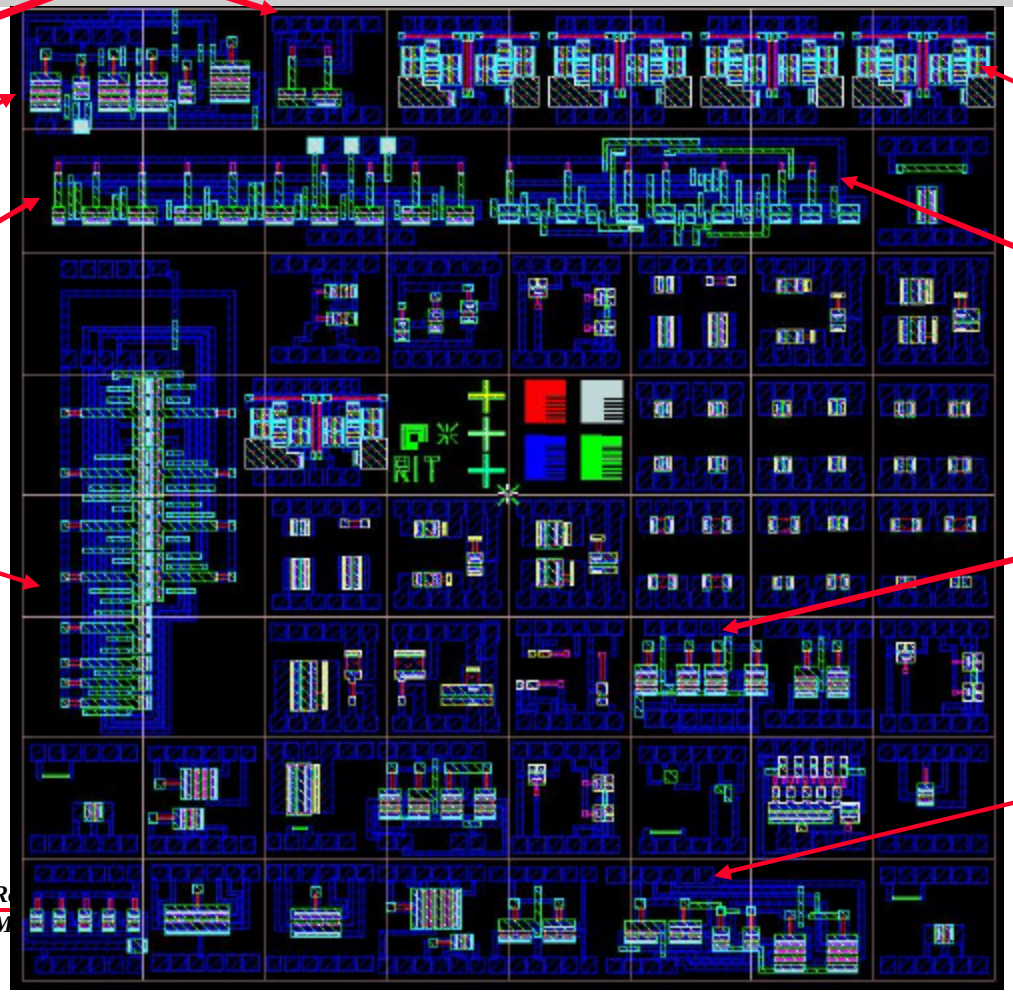
INTRODUCTION

We have been making transistors and integrated circuits at RIT since 1977. We have used Metal Gate PMOS, Bipolar, NMOS, and CMOS technologies.

This document shows some test results for integrated circuits made in Metal Gate PMOS technology.

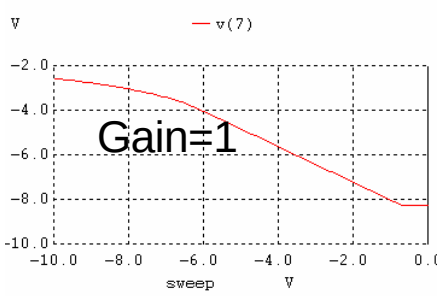


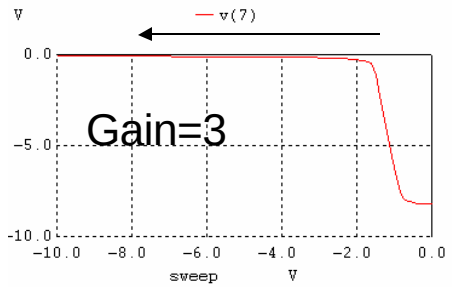
PMOS TEST CHIP FROM FEB 2007 SHORT COURSE



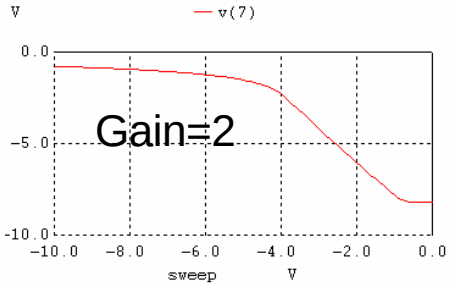
PMOS INVERTER SPICE SIMULATION

Vin

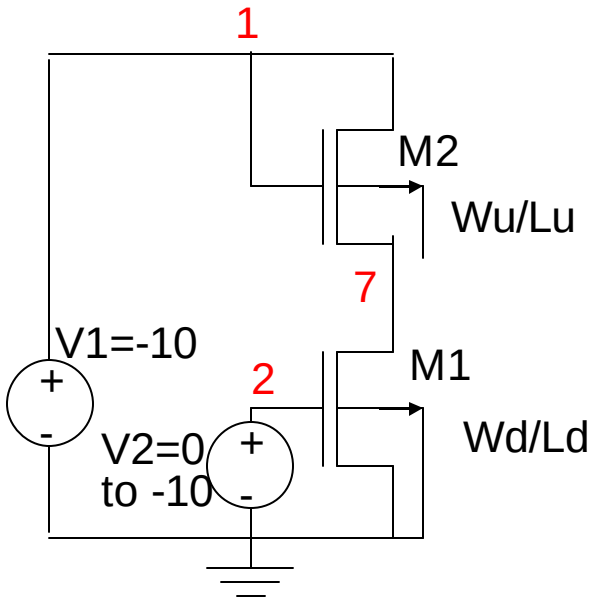




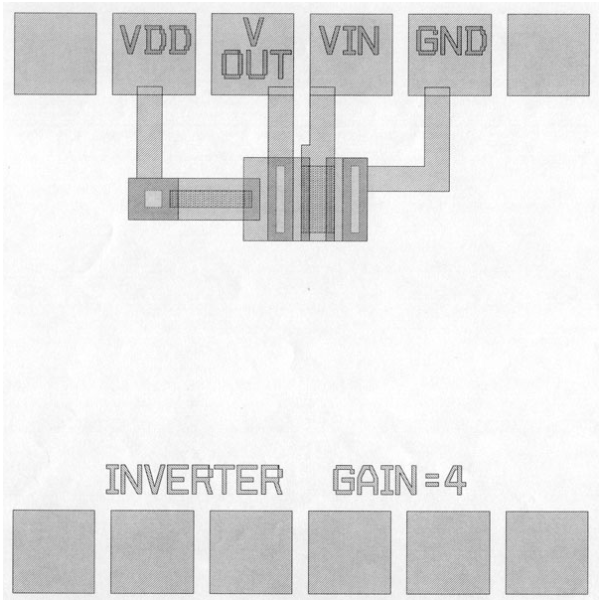
Vout

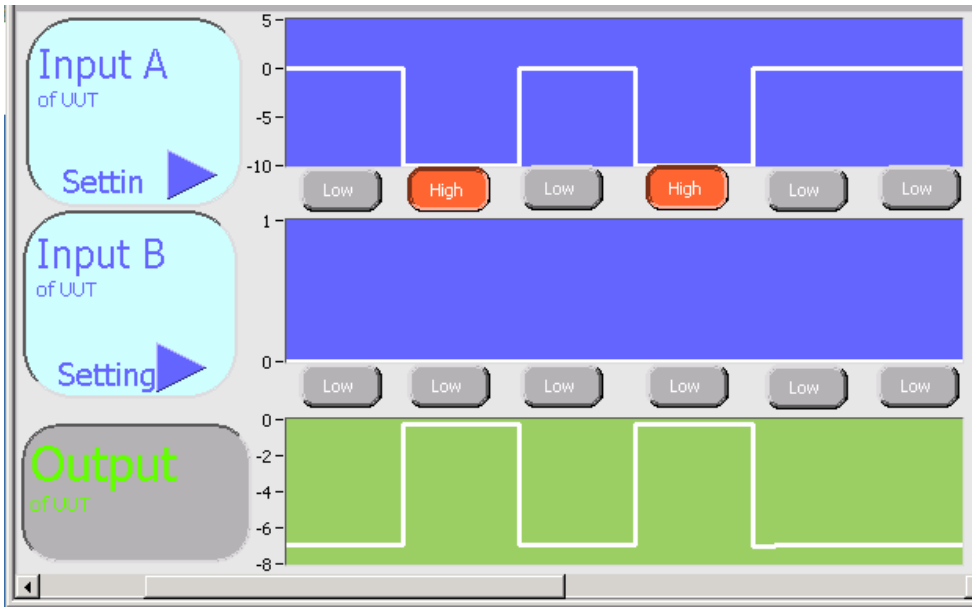


$$\text{Gain} = \left(\frac{Wd/Ld}{Wu/Lu}\right)^{0.5}$$

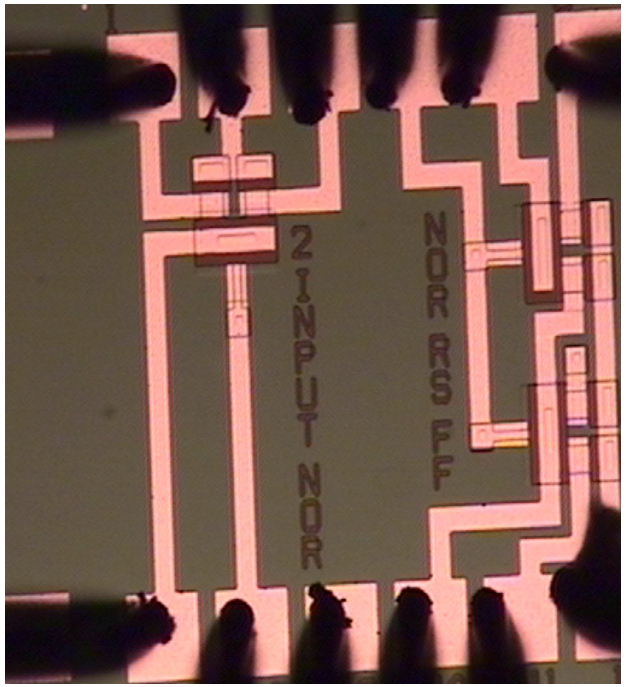


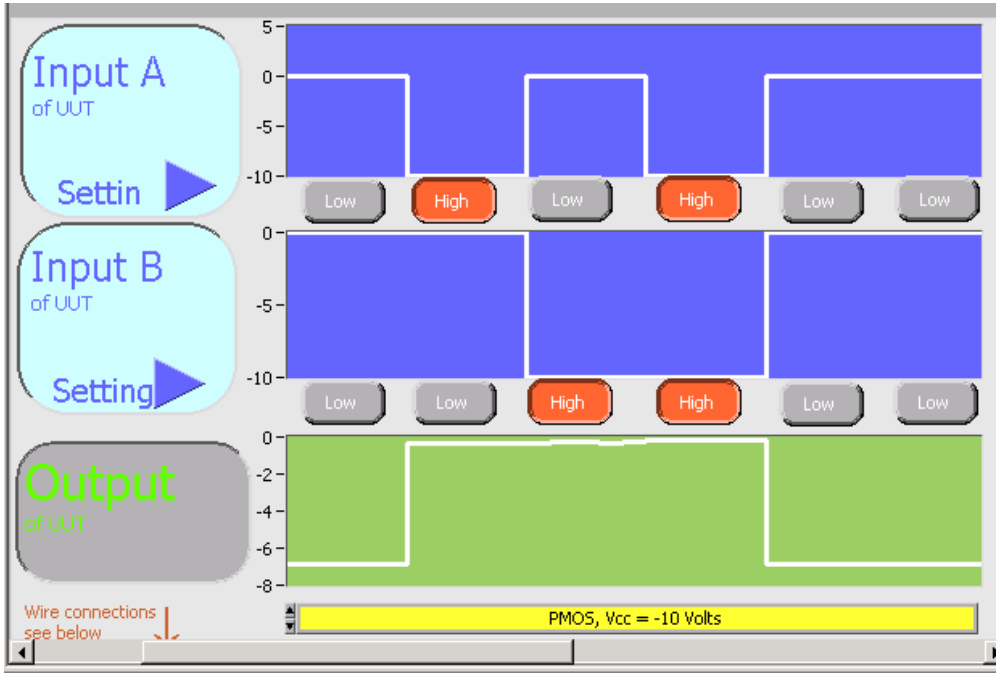
PMOS INVERTER GAIN = 4





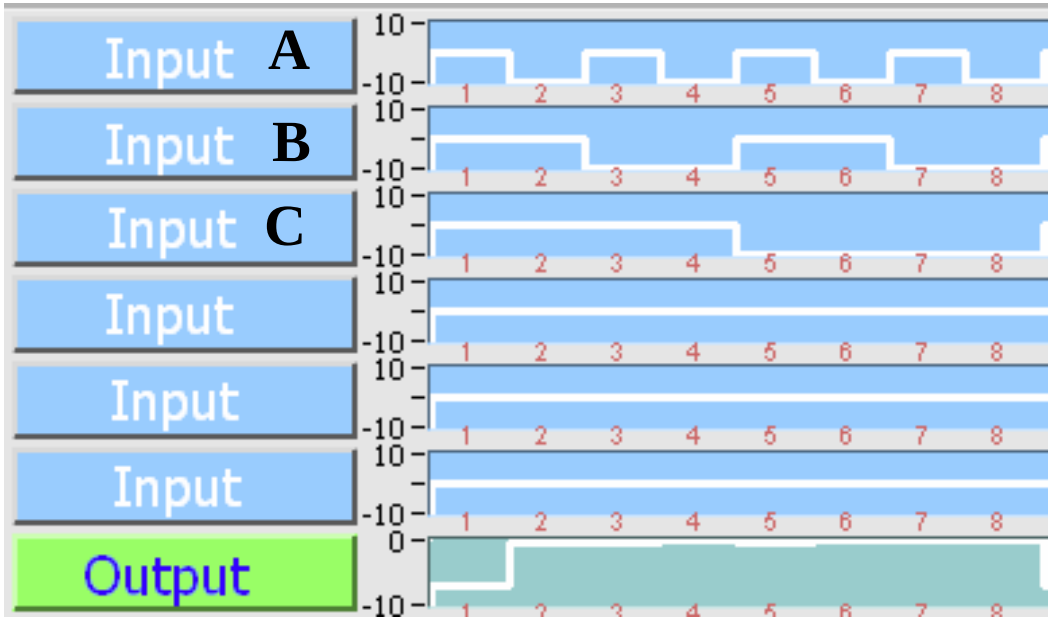
PMOS 2-INPUT NOR

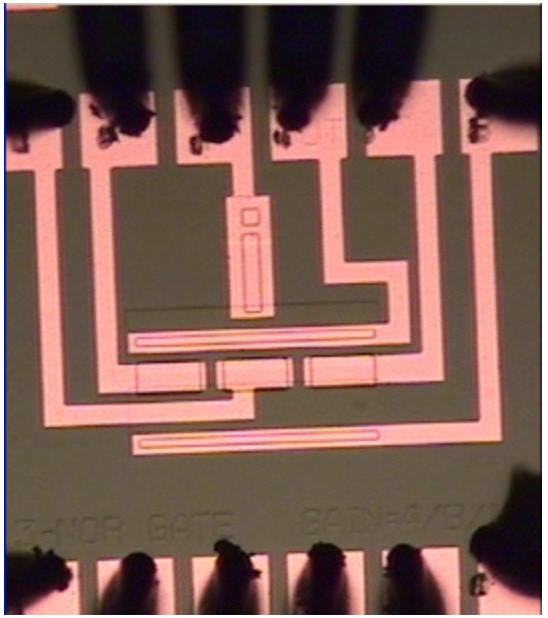




Test for PMOS Two Input NOR, Gain = 4 or 8

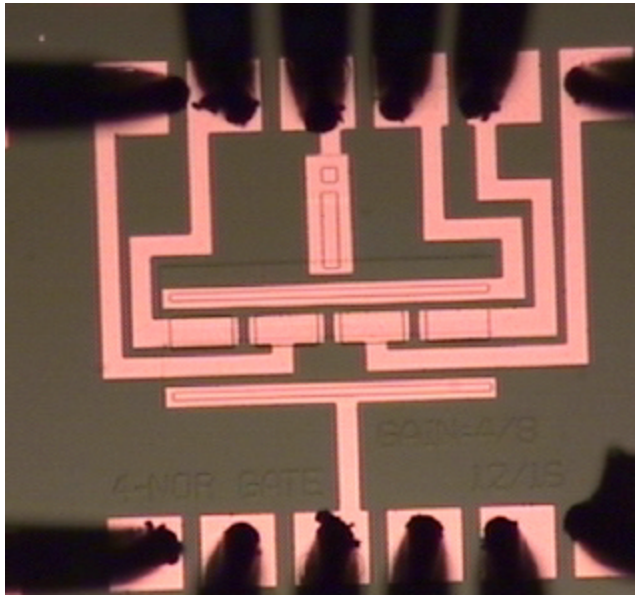
PMOS 3-INPUT NOR

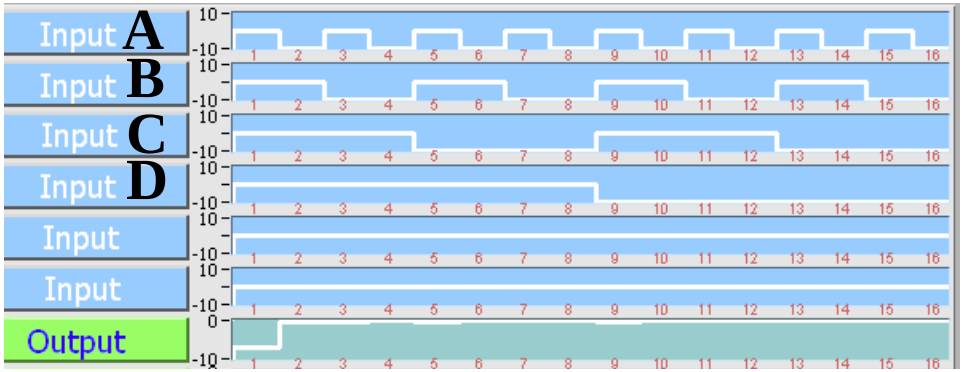




In PMOS logic low is 0 volts,
logic high is approximately -Vdd

PMOS 4-INPUT NOR





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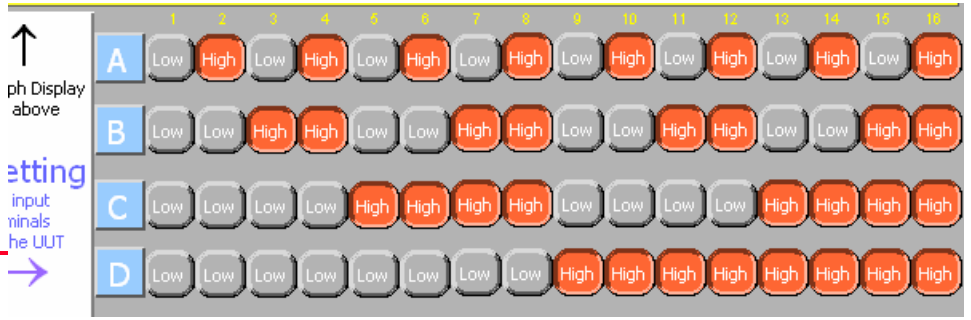
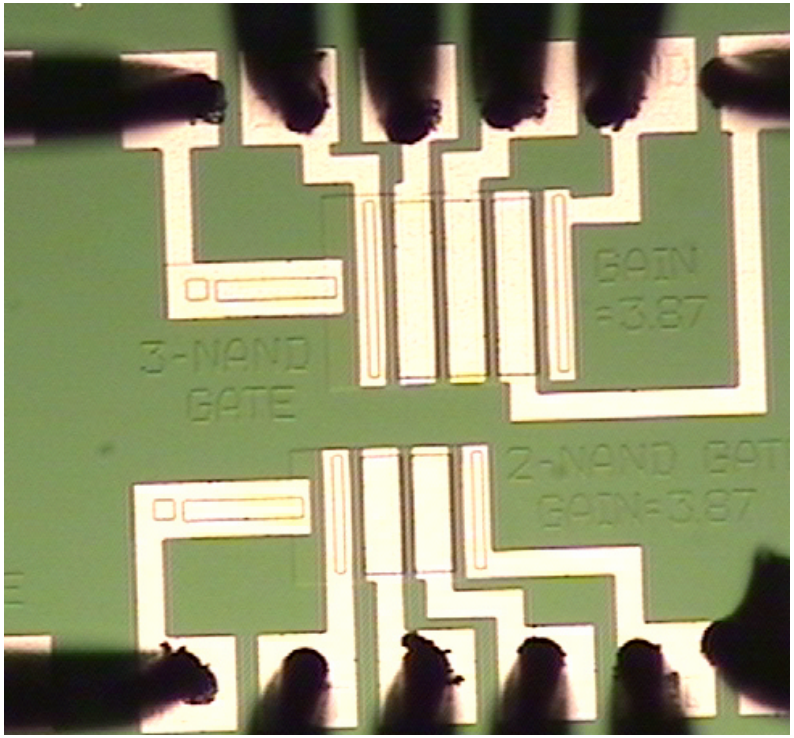
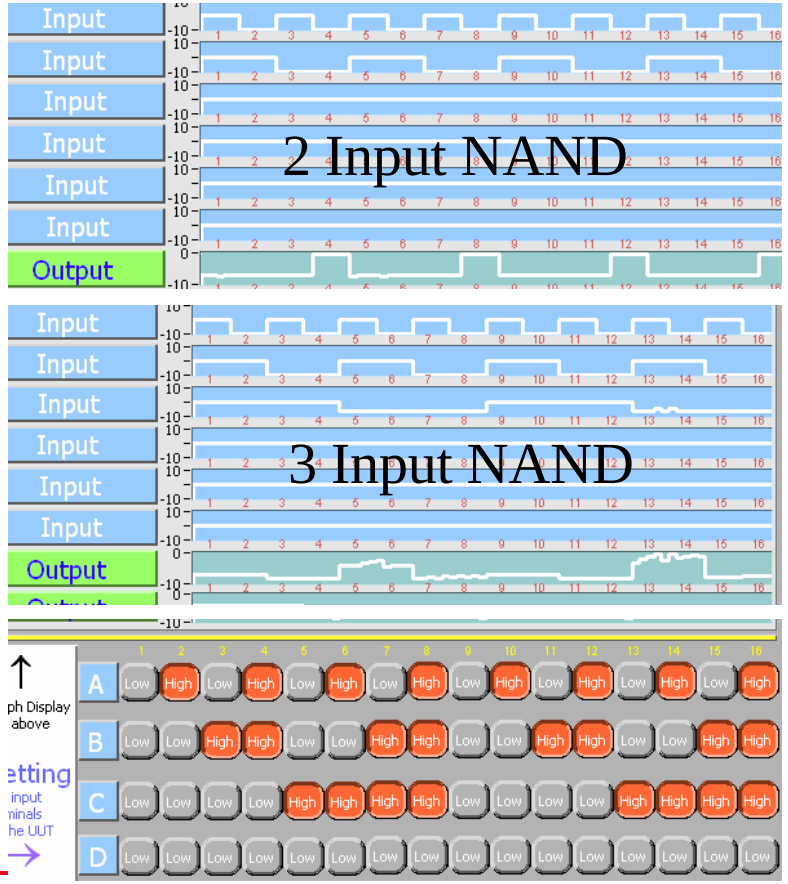
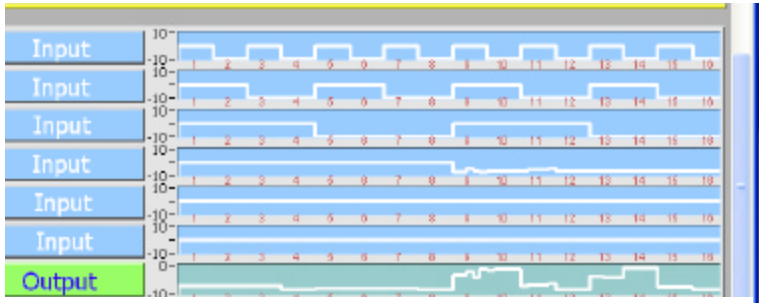


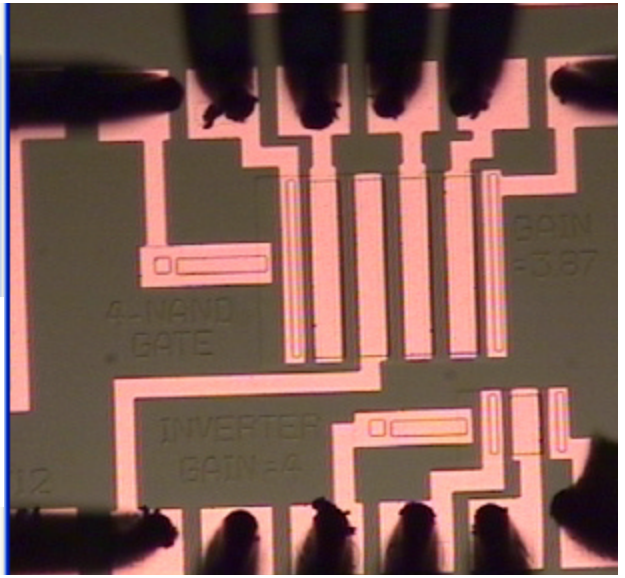
PMOS 2 AND 3 INPUT NAND



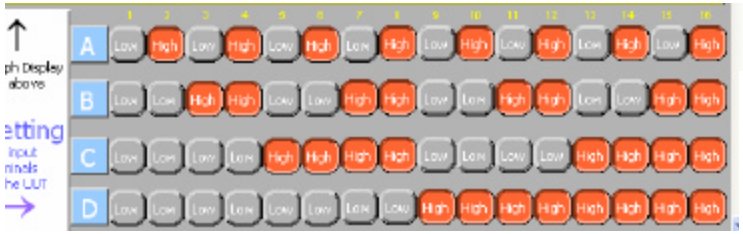


PMOS 4-INPUT NAND



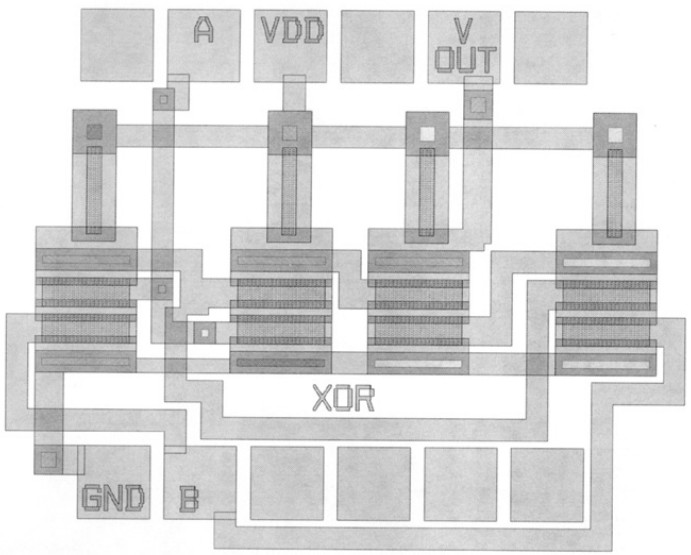


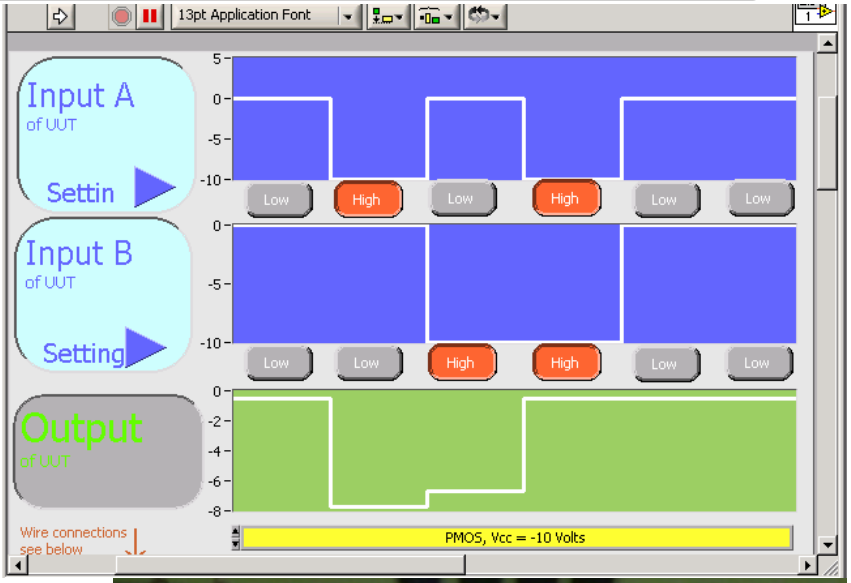
Build IC's with NOR gates (2-input NAND works okay)



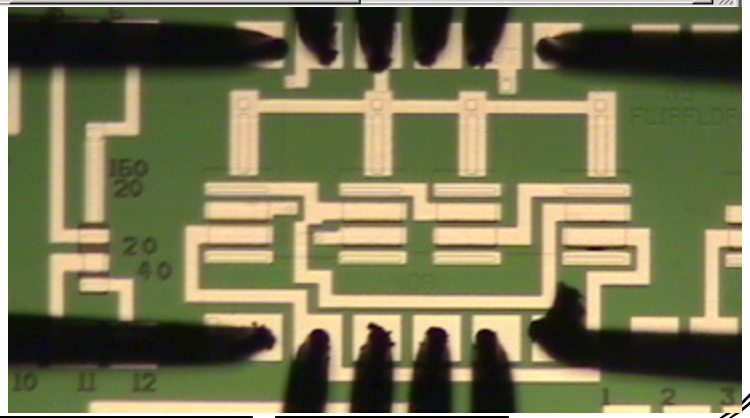
Note: NAND gates have problems with so many transistors in series between the supply and ground. Here 5 transistors each with Vt ~2 volts in series and a 10 volt supply

PMOS 2-INPUT XOR

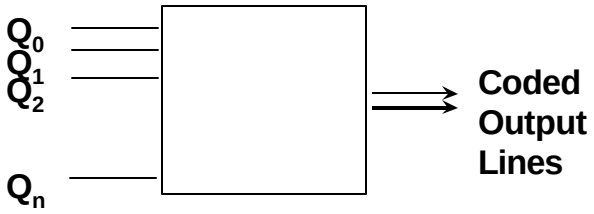




In PMOS logic low is 0 volts, logic high is approximately -Vdd



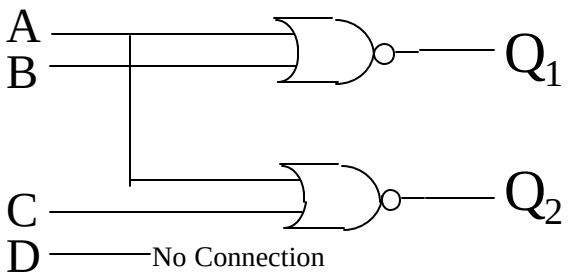
4:2 PMOS ENCODER

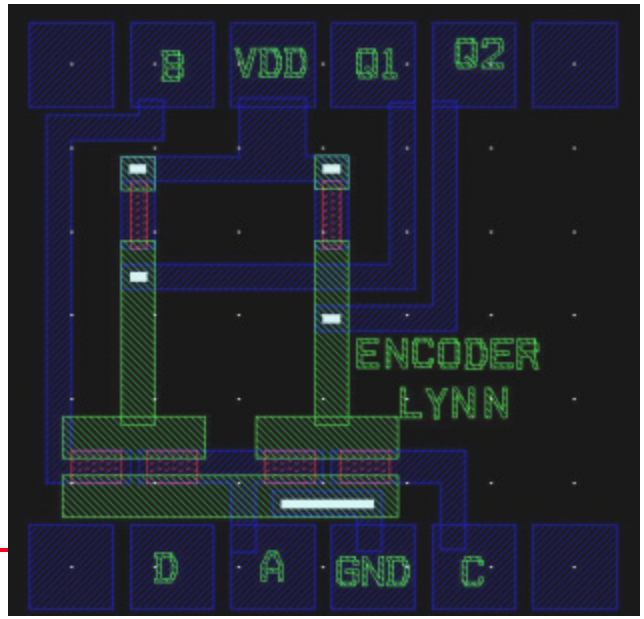


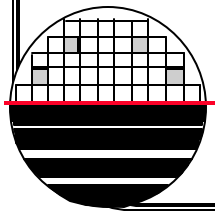
Digital Encoder

512 inputs can be coded into 9 lines which is a more dramatic benefit

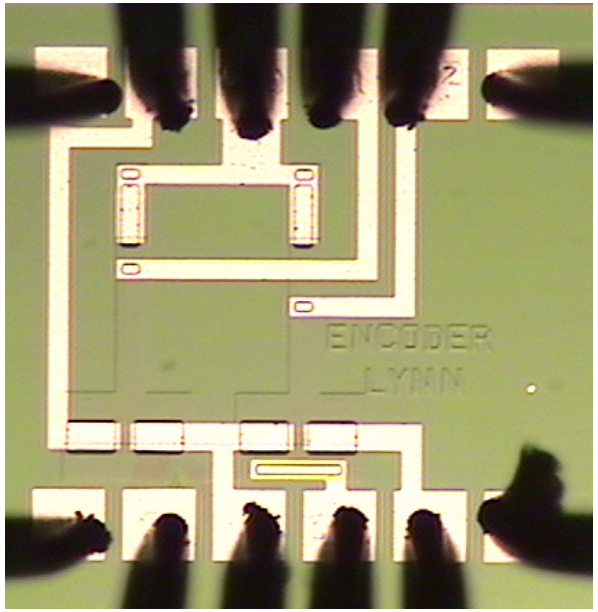
INPUTS				OUTPUTS	
A	B	C	D	Q_1	Q_2
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

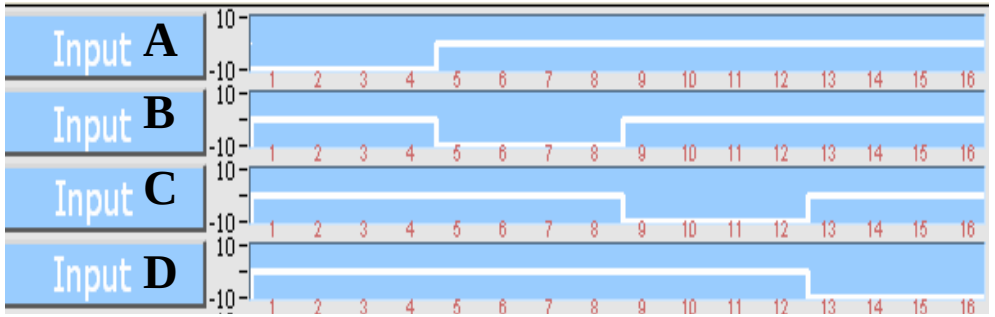




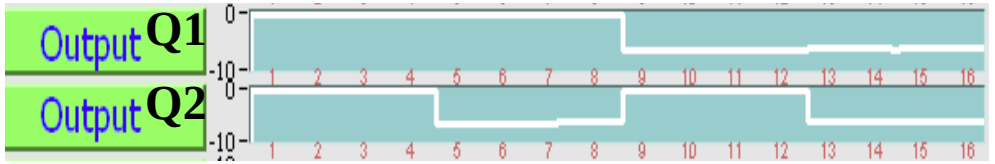


4:2 PMOS ENCODER

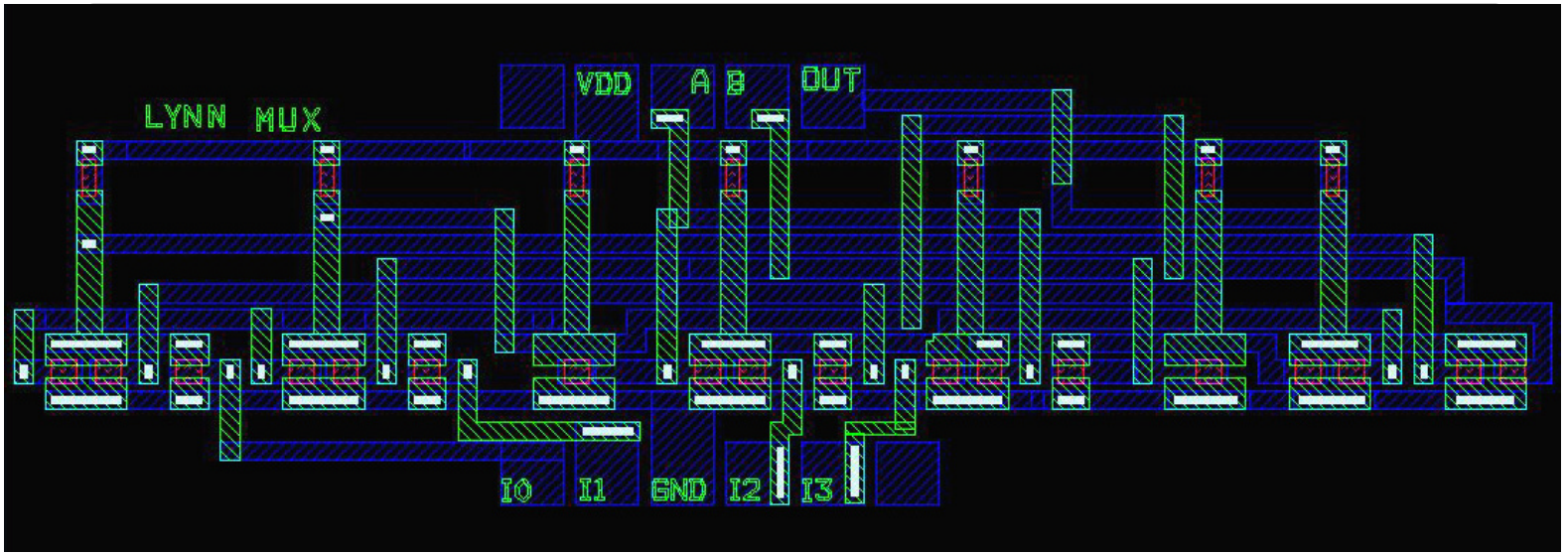




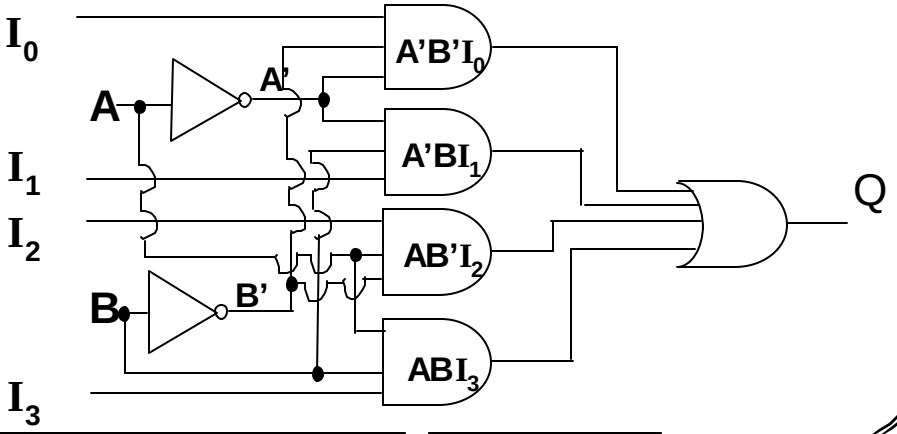
In PMOS logic low is 0 volts, logic high is approximately -Vdd



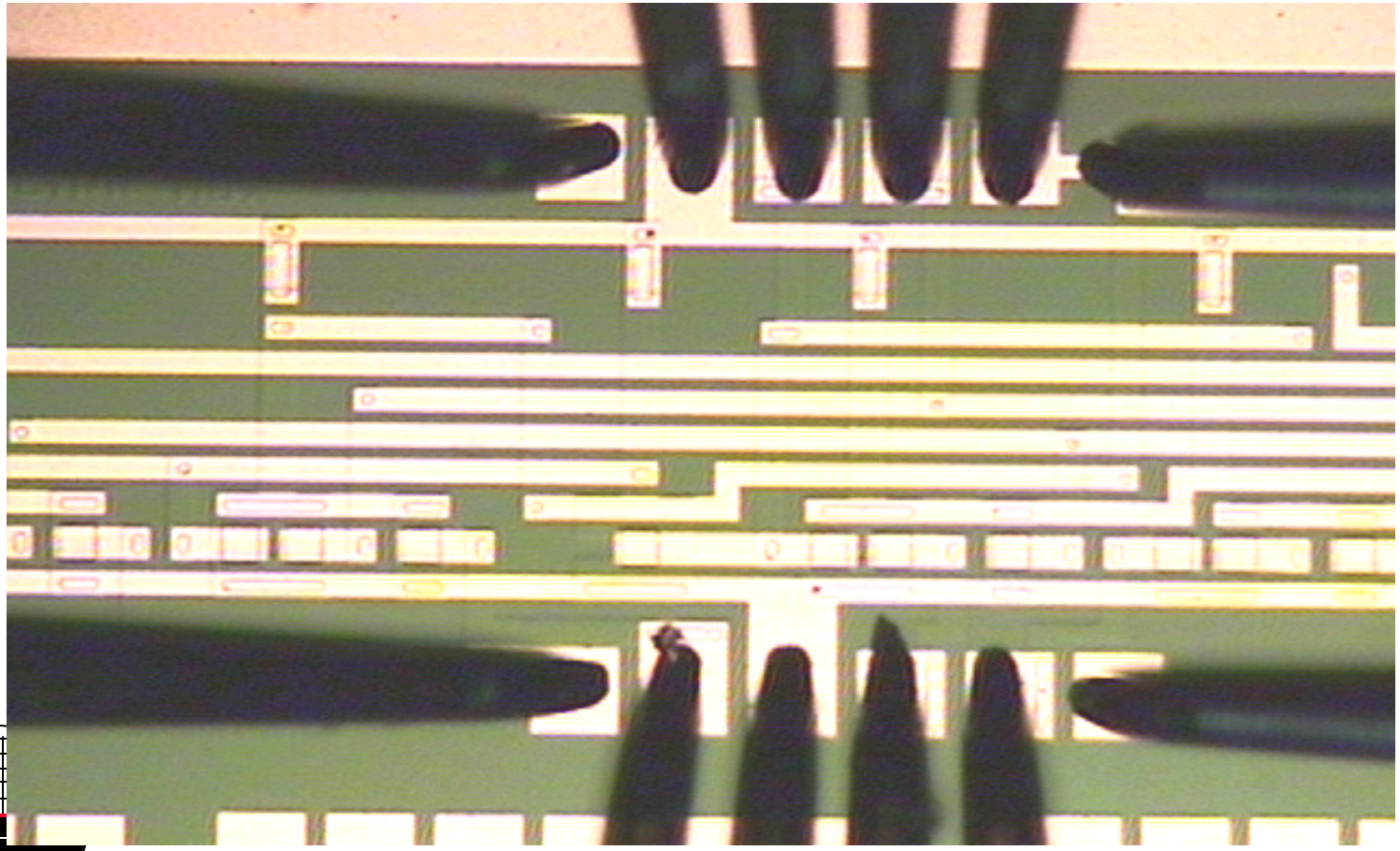
MUX LAYOUT AND GATE LEVEL SCHEMATIC



25 Transistors

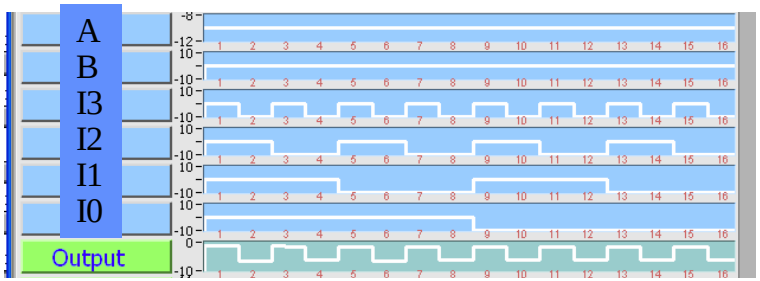


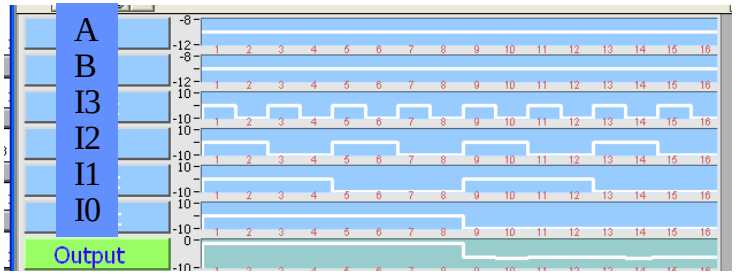
PMOS 4-INPUT MULTIPLEXER



PMOS Integrated Circuit Test Results

MUX TEST RESULTS





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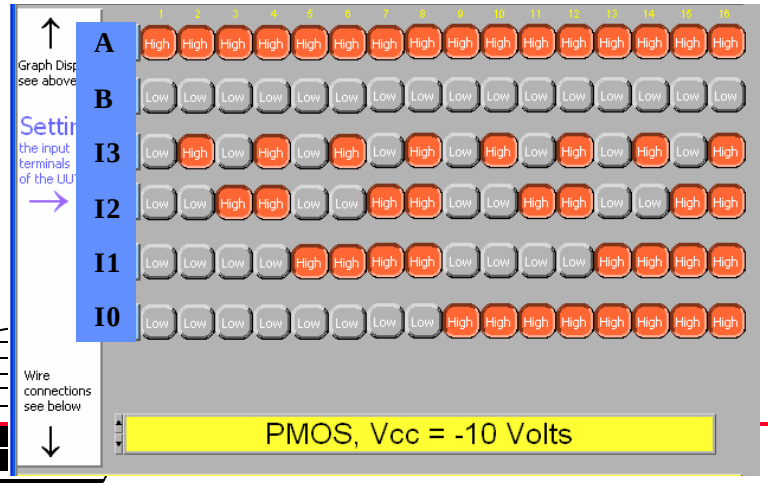
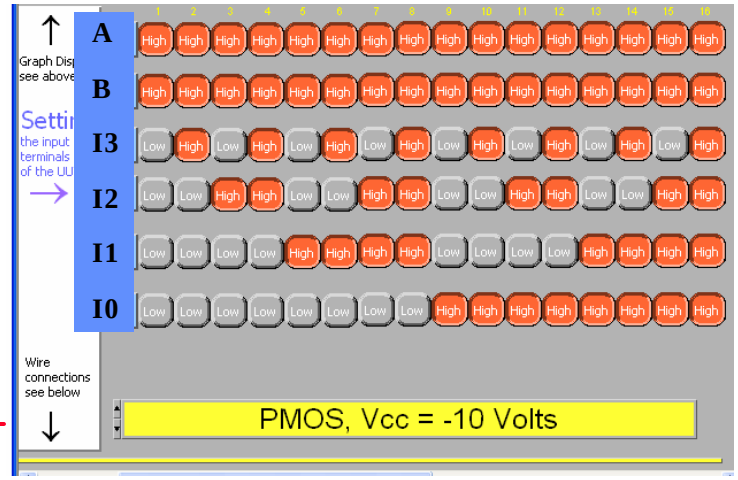
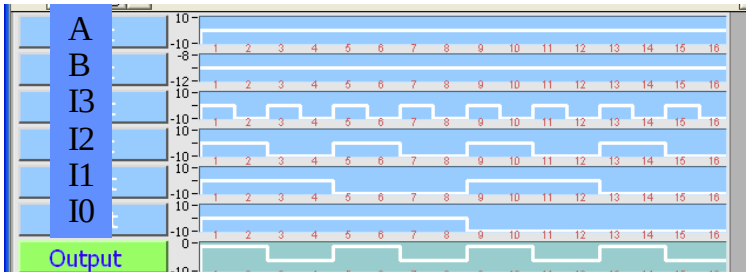
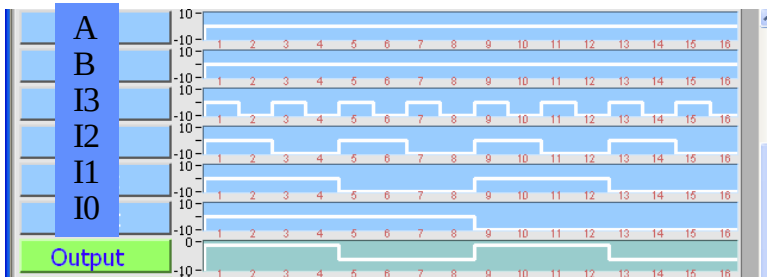




PMOS Integrated Circuit Test Results

MUX TEST RESULTS





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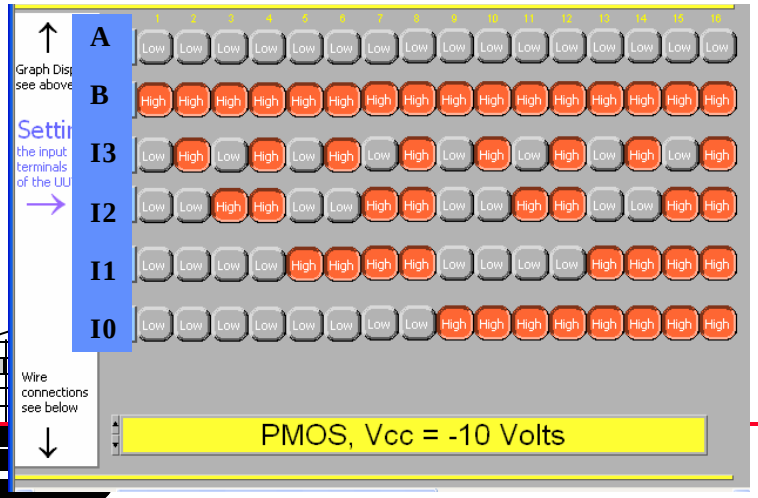
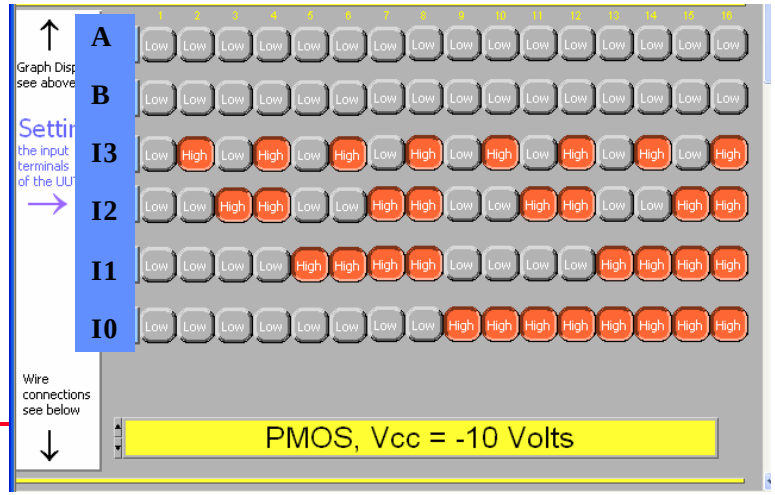
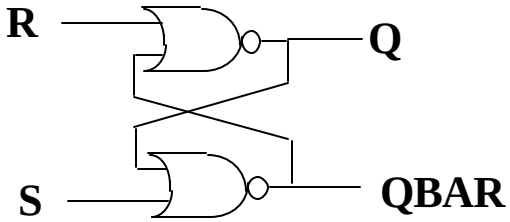




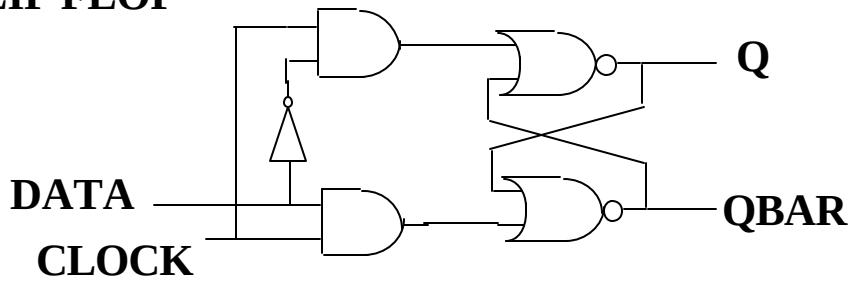
PMOS CLOCKED DATA LATCH

RS FLIP FLOP

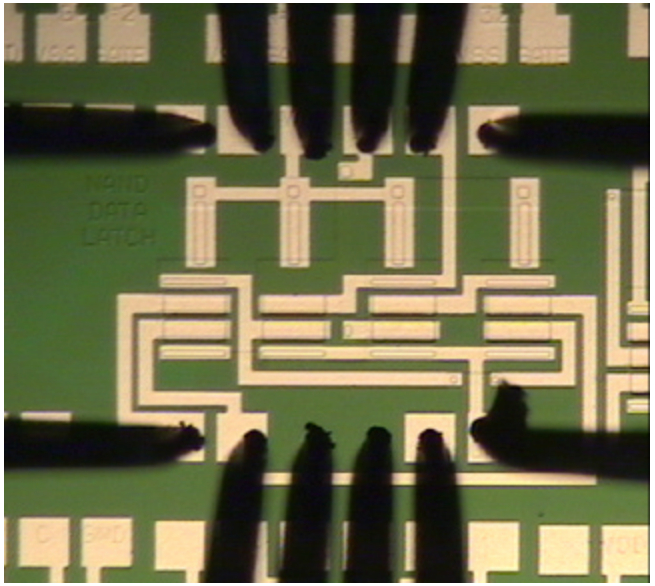


R	S	Q_{t+1}
0	0	Q_t
0	1	1
1	0	0
1	1	INDETERMINATE

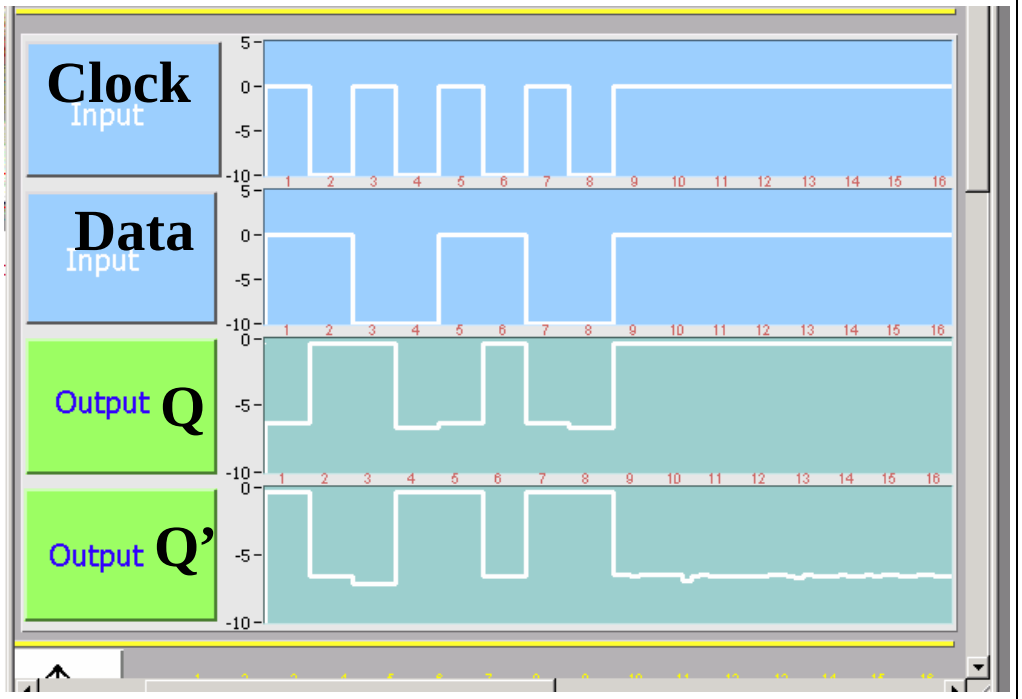
D FLIP FLOP



PMOS CLOCKED DATA LATCH



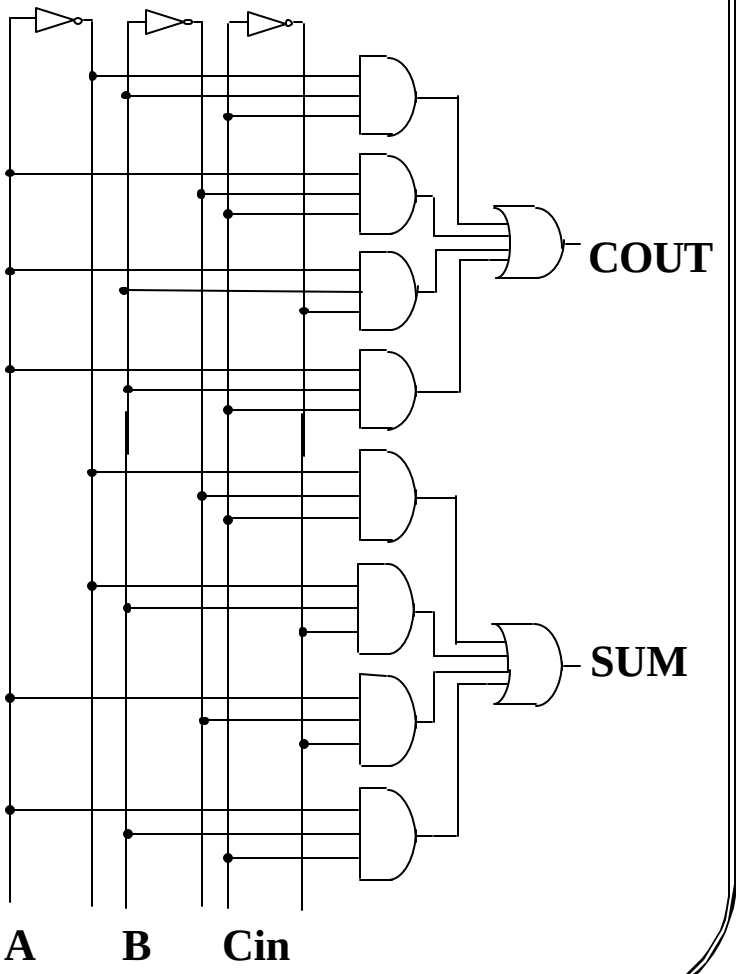
PMOS D - FlipFLop



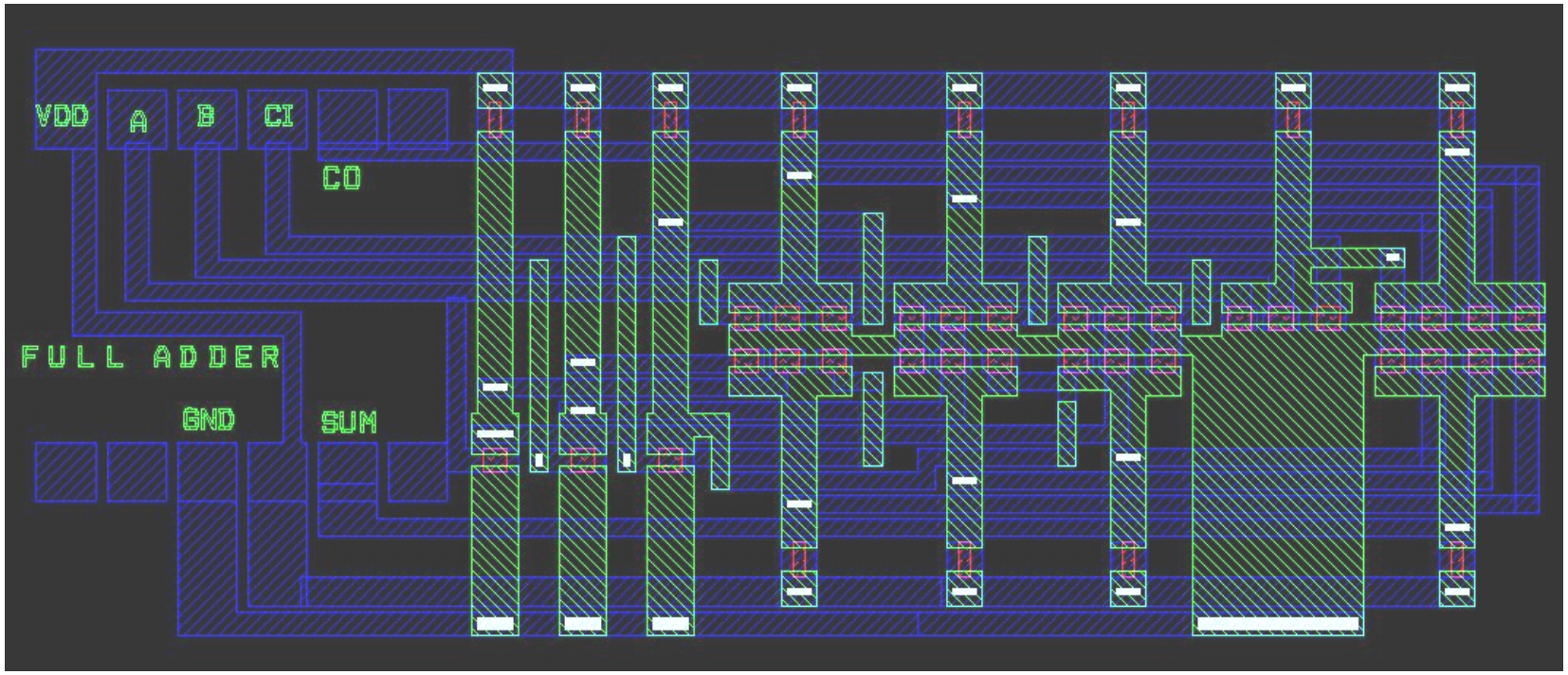
In PMOS logic low is 0 volts, logic high is approximately -Vdd

PMOS FULL ADDER

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

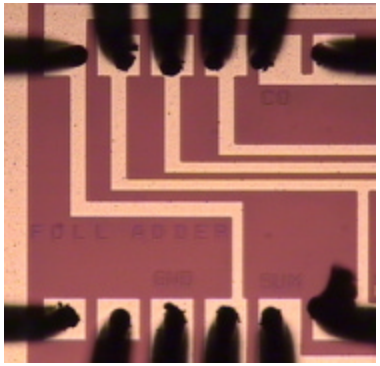


PMOS FULL ADDER

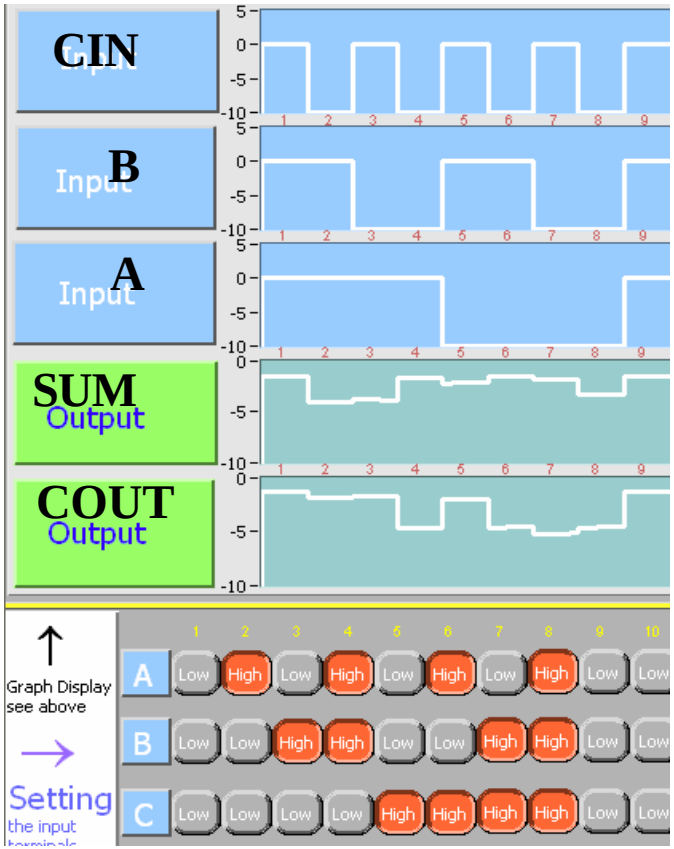


Error…. Inverters and Gate Gain is Too Low

PMOS FULL ADDER



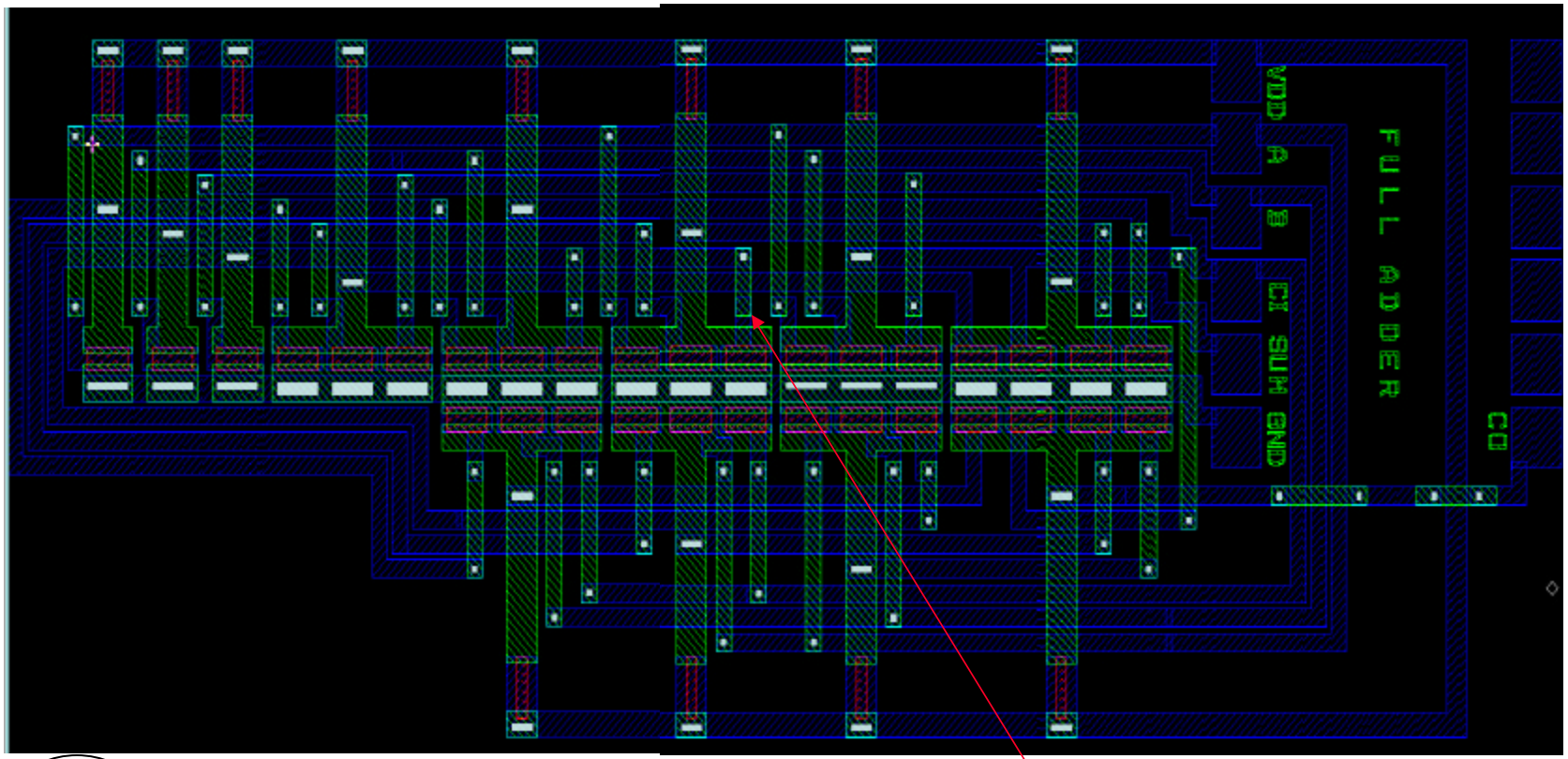
A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



In PMOS logic low is 0 volts, logic high is -Vcc

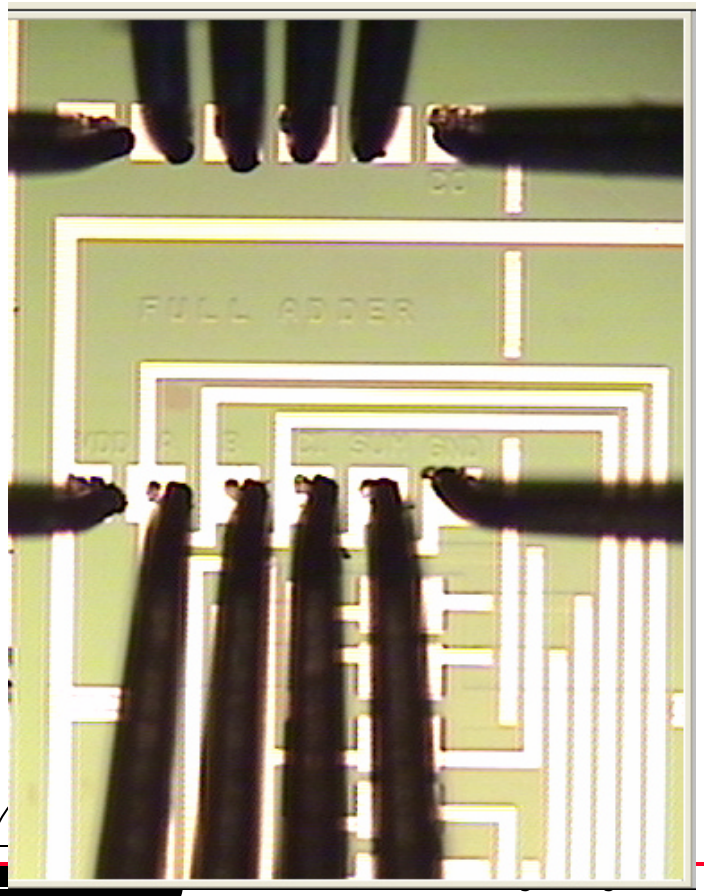
PMOS Integrated Circuit Test Results

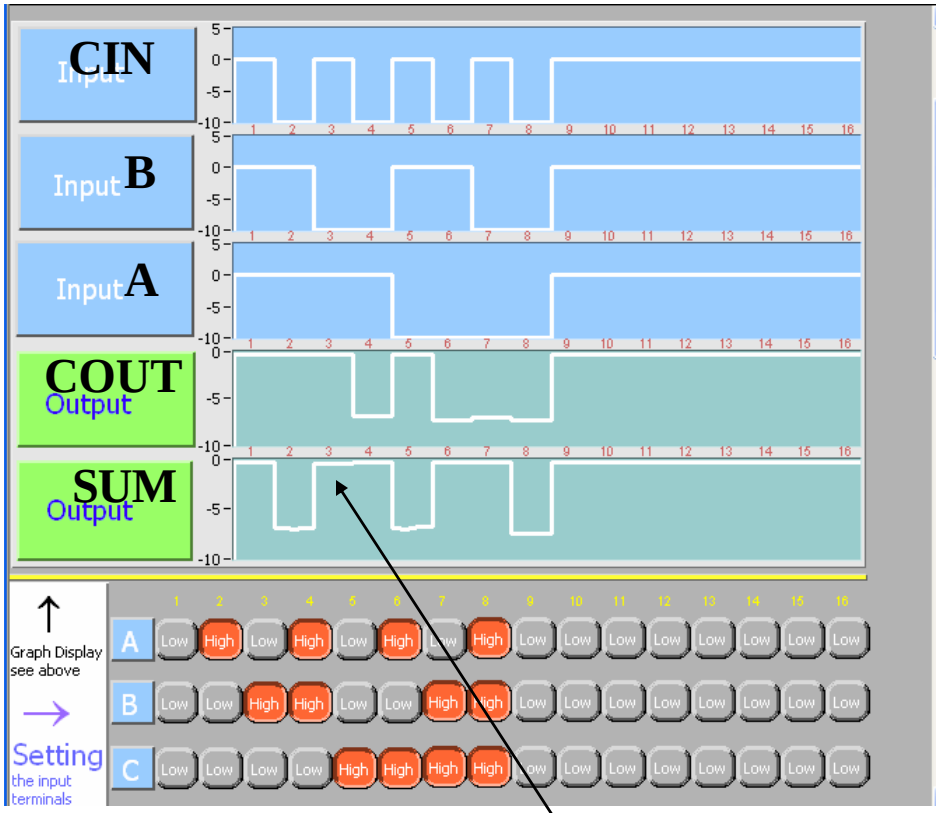
VERSION 4



Missing contact cut

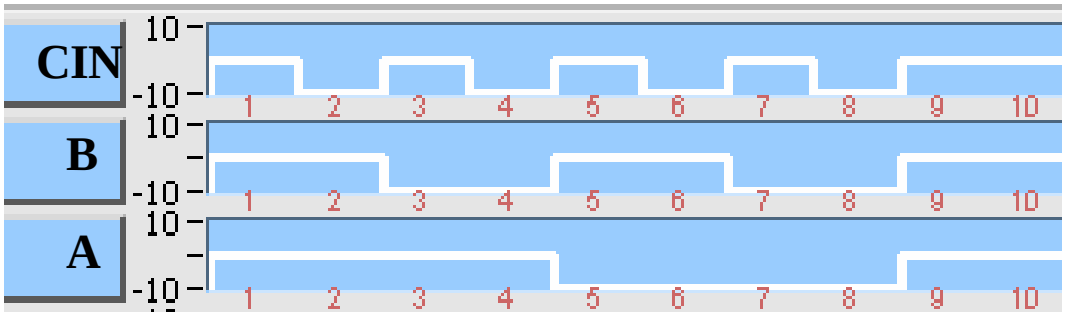
TEST RESULTS FOR VERSION 4



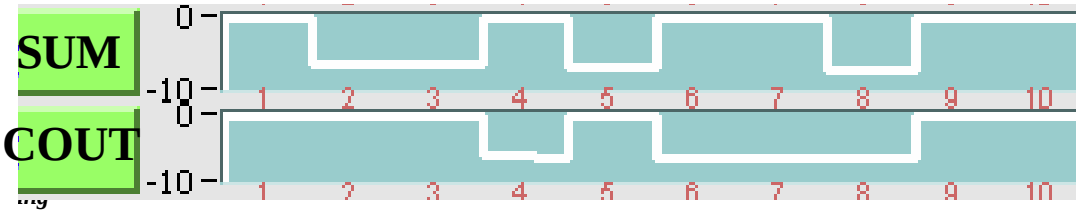


TEST RESULTS FOR VERSION 5

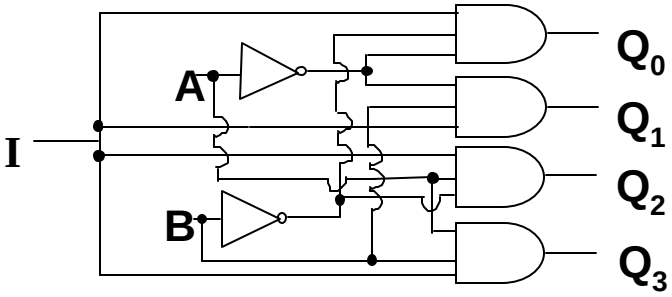
A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

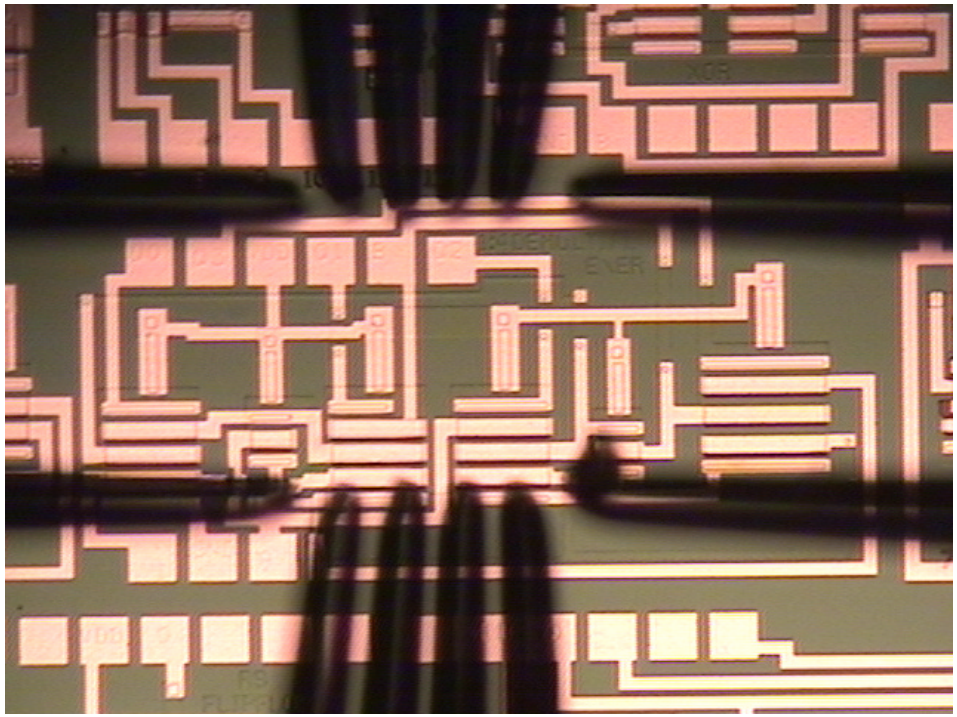


In PMOS logic low is 0 volts, logic high is approximately -Vdd



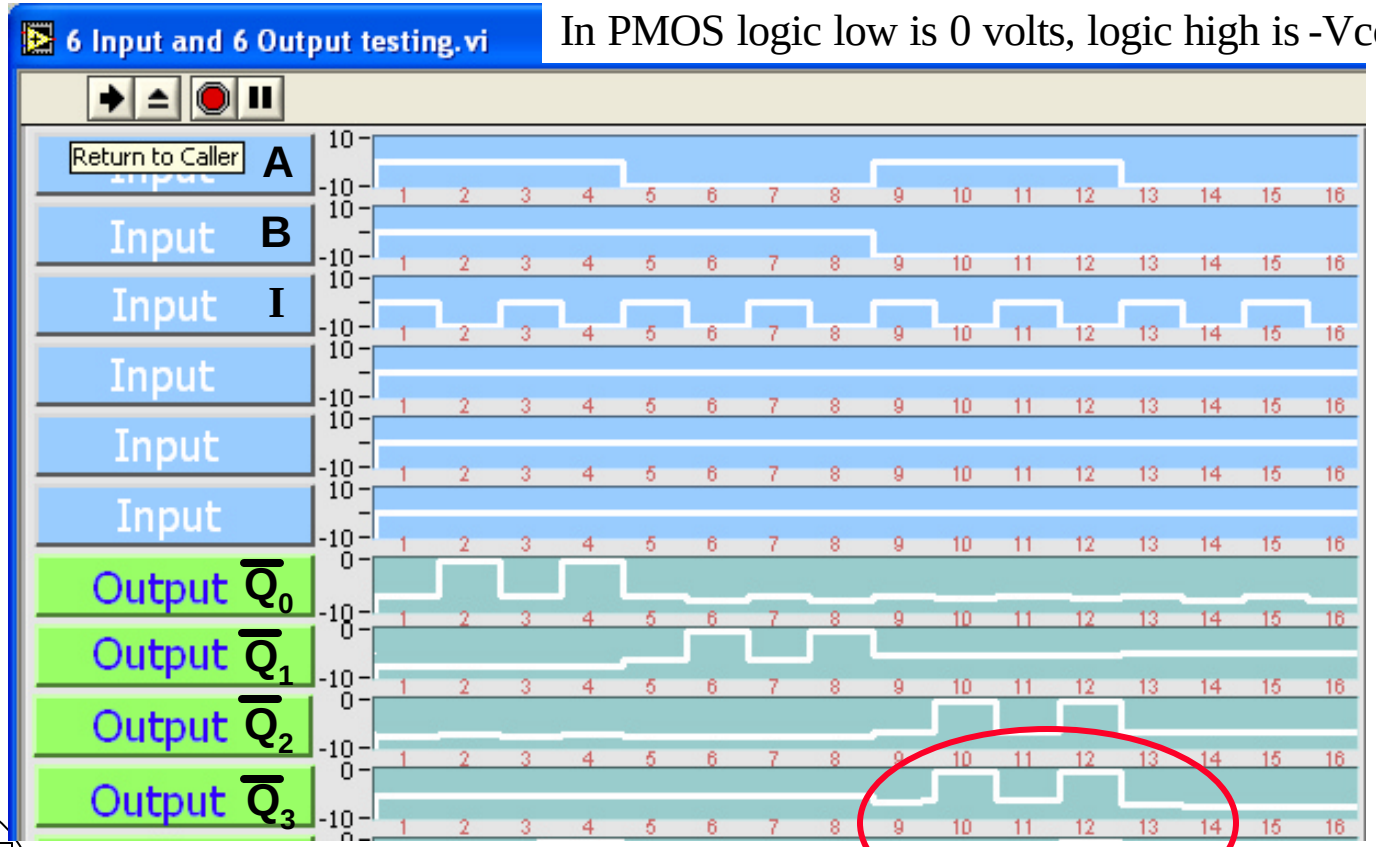
1:4 DEMULTIPLEXER





INPUTS		OUTPUTS			
A	B	Q_0	Q_1	Q_2	Q_3
0	0	I	0	0	0
0	1	0	I	0	0
1	0	0	0	I	0
1	1	0	0	0	I

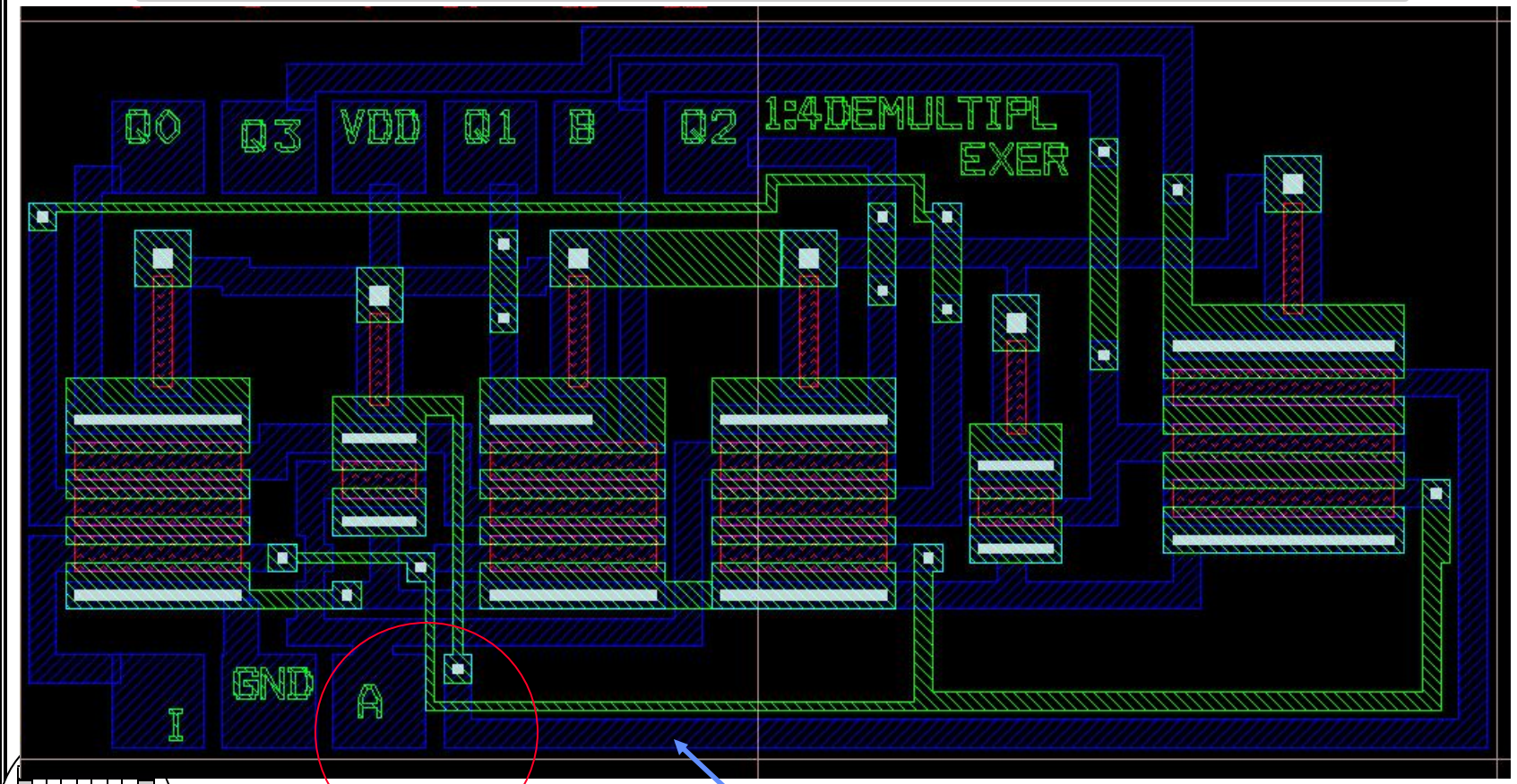
1:4 DEMULTIPLEXER



In PMOS logic low is 0 volts, logic high is -Vcc

Error
Logic Design Mistake

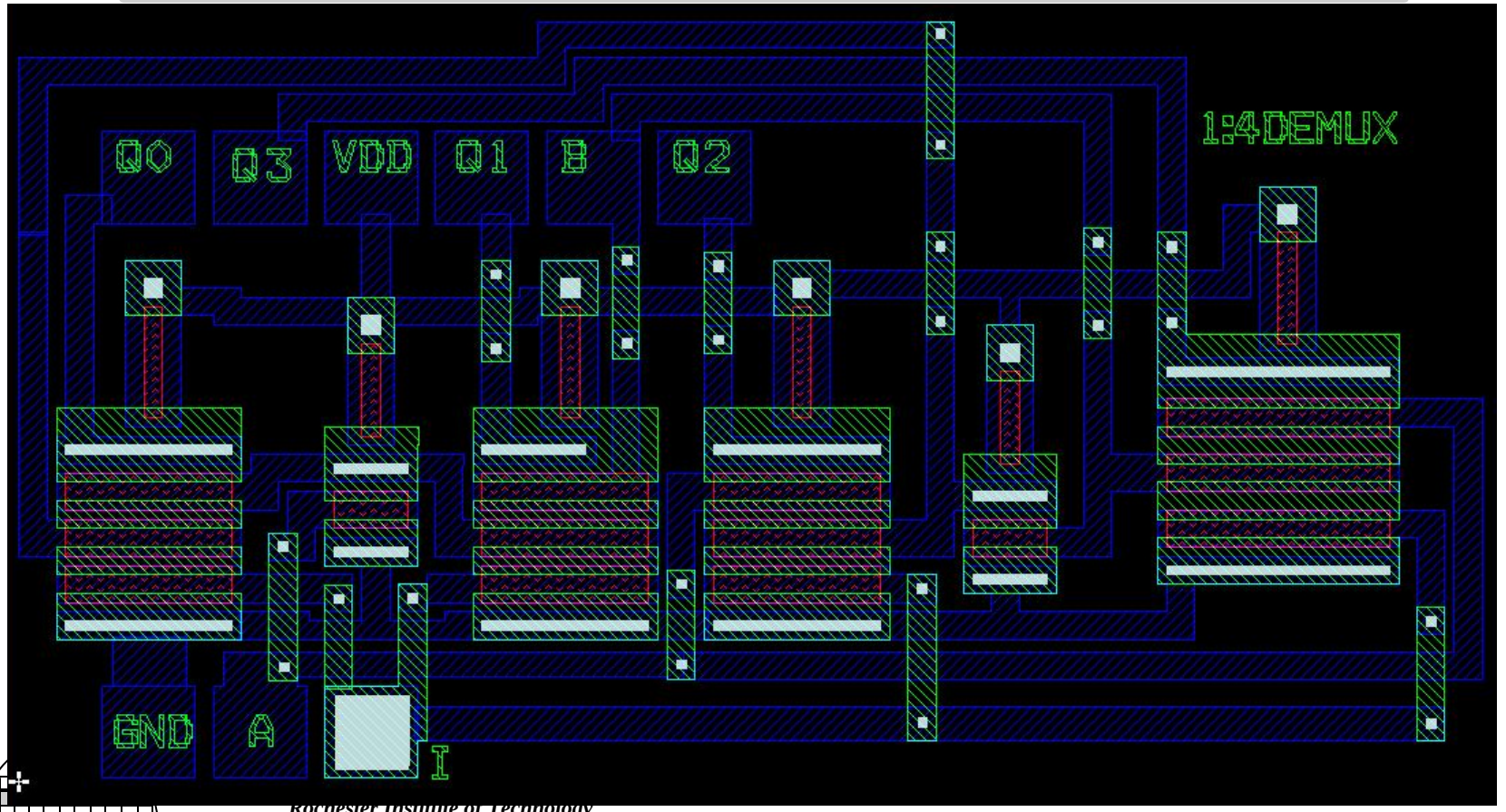
1:4 DEMULTIPLEXER (with error)



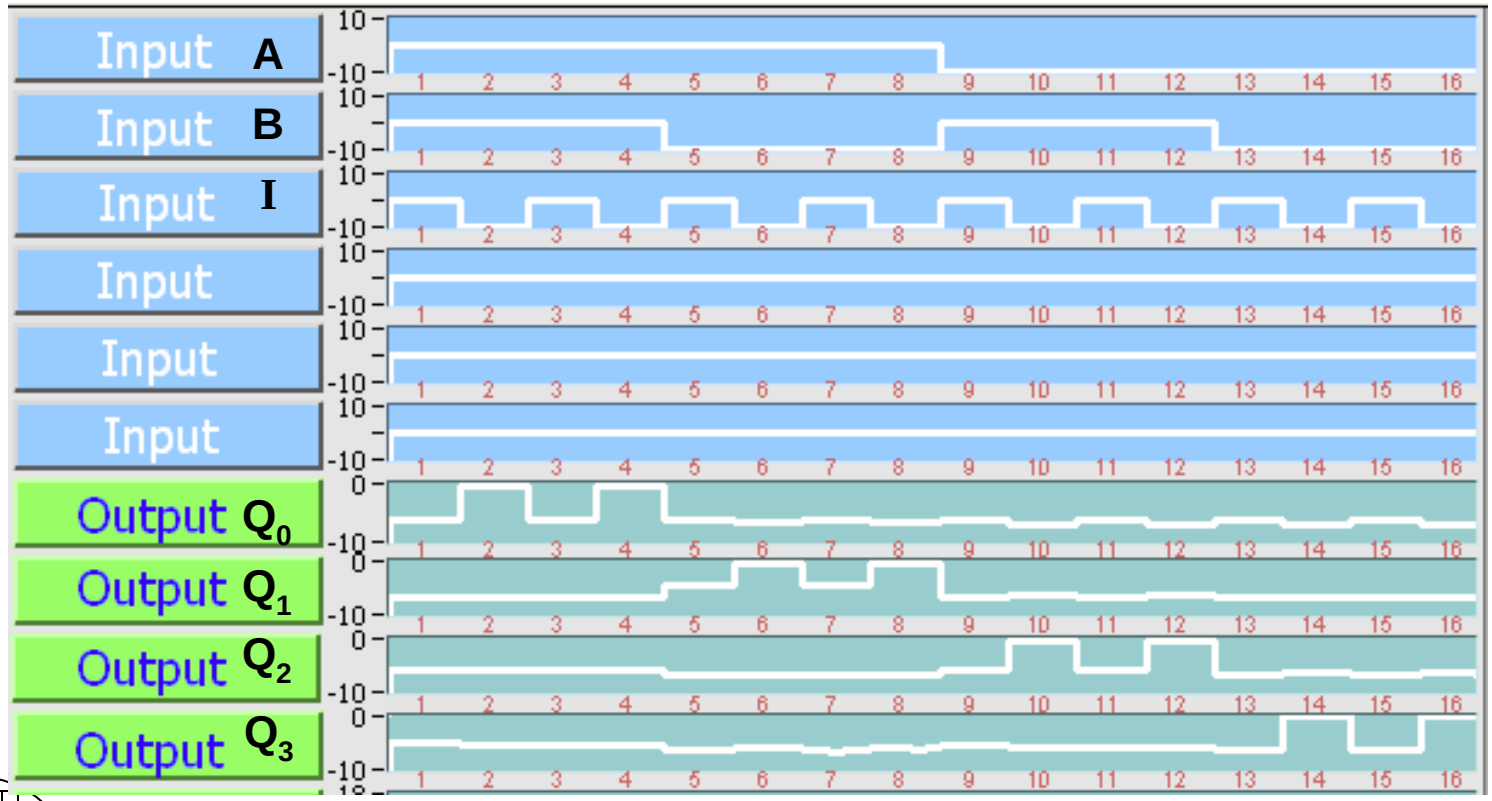
Error

This should be A instead of A'

1:4 DEMULTIPLEXER (version four)



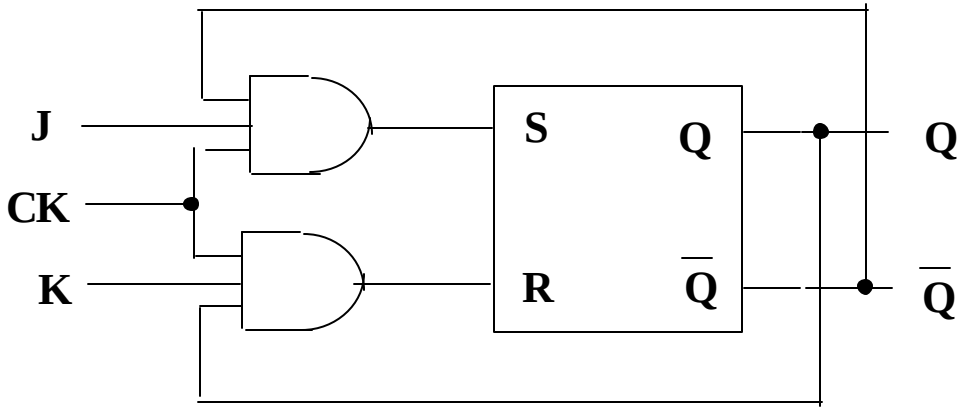
TEST RESULT 1:4 DEMULTIPLEXER (version four)

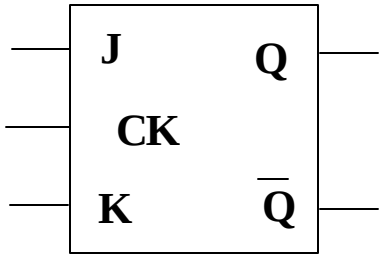


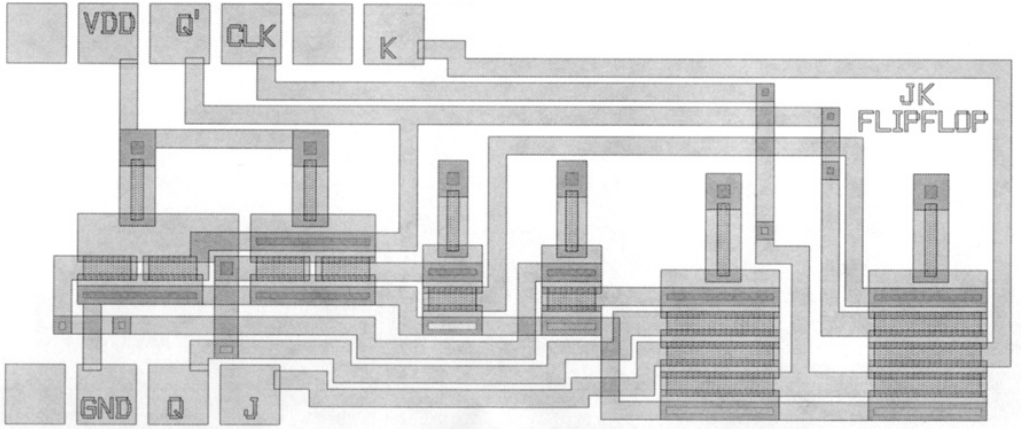
JK FLIP FLOP

JK TRUTH TABLE

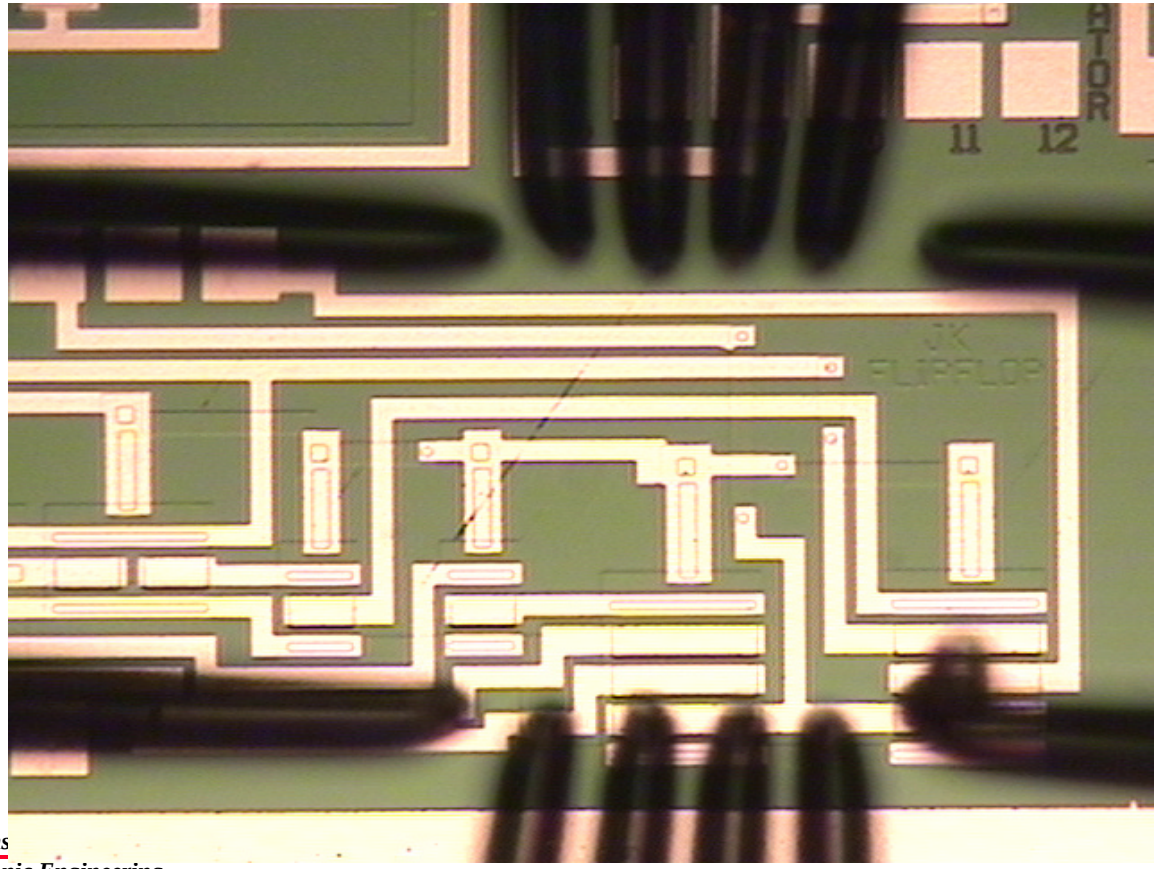
J	K	Qn+1
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$



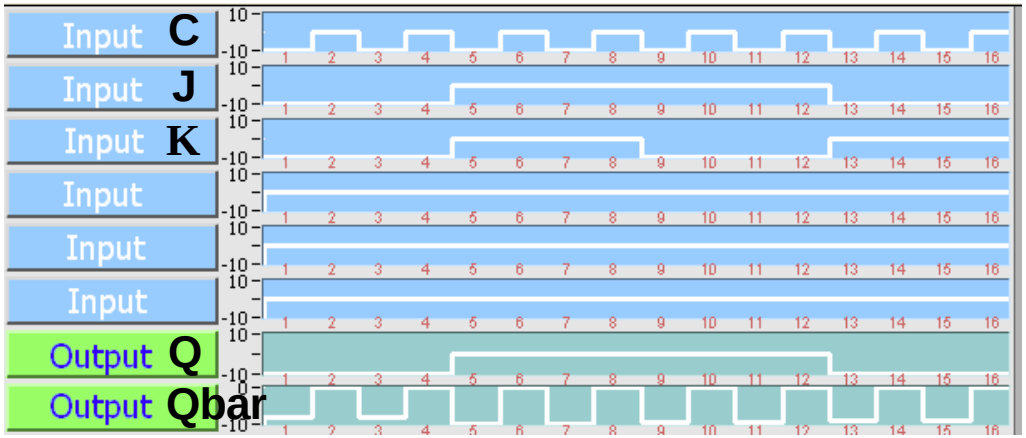




JK FLIP FLOP

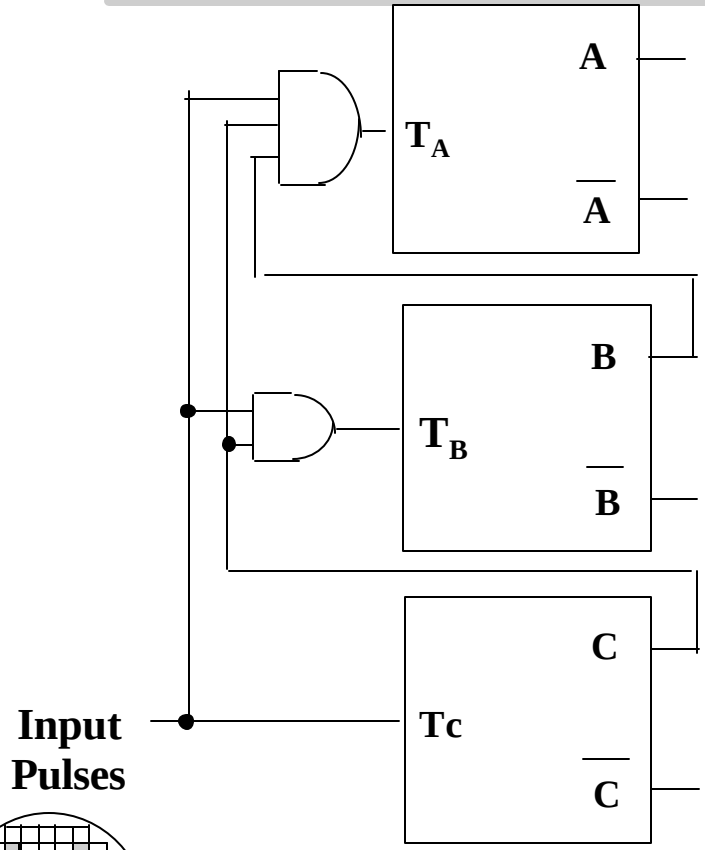


JK FLIP FLOP



In PMOS logic low is 0 volts, logic high is -Vcc

BINARY COUNTER USING T TYPE FLIP FLOPS



State Table for Binary Counter

Present State			Next State			F-F Inputs		
A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

TOGGEL FLIP FLOP

BC \ A	0	1
00	0	0
01	0	0
11	1	1
10	0	0

T_A

BC \ A	0	1
00	0	0
01	1	1
11	1	1
10	0	0

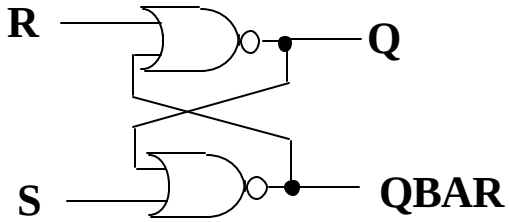
T_B

BC \ A	0	1
00	1	1
01	1	1
11	1	1
10	1	1

T_C

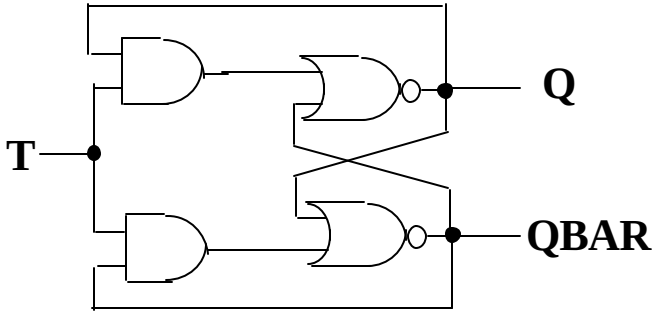
T-TYPE FILP-FLOP

RS FLIP FLOP



R	S	Q
0	0	Qn-1
0	1	1
1	0	0
1	1	INDETERMINATE

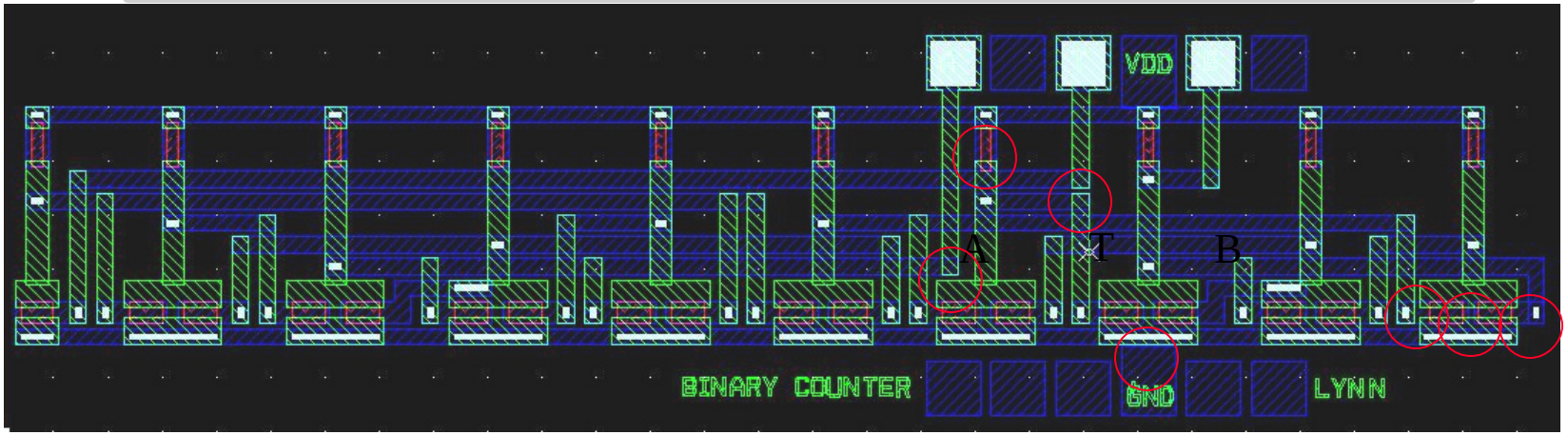
TOGGEL FLIP FLOP



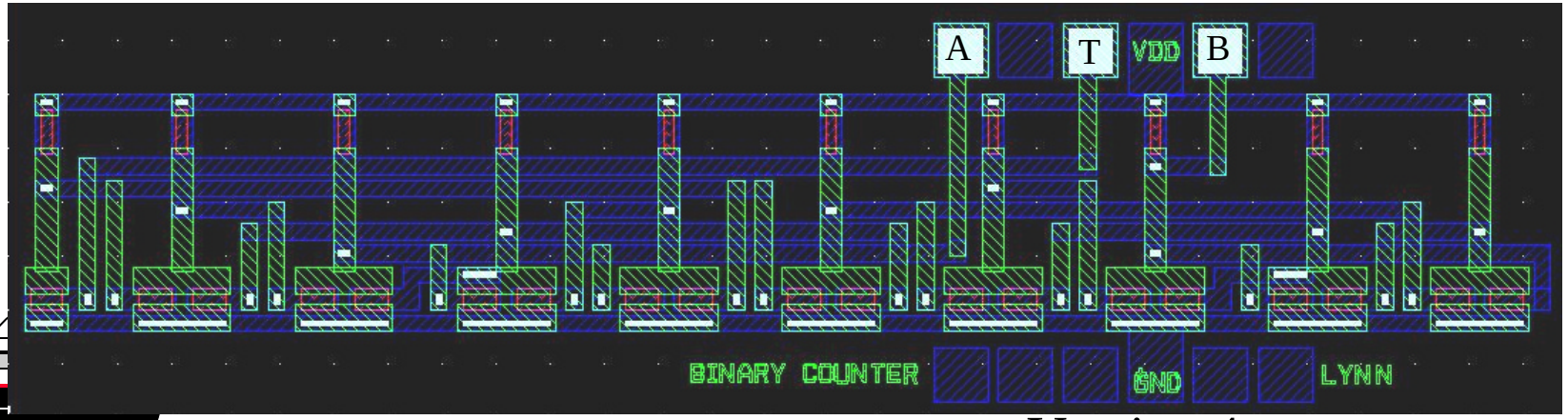
T	Qn-1	Q
0	0	0
0	1	1
1	0	1
1	1	0

Q: TOGGELS HIGH AND LOW WITH EACH INPUT

BINARY COUNTER

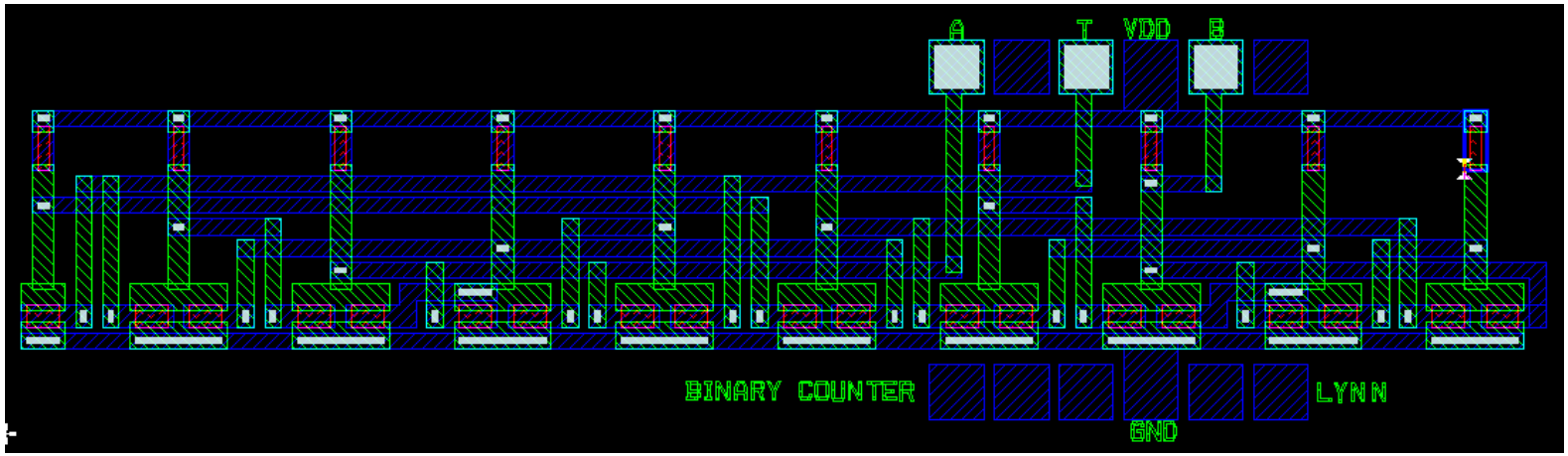


Version 3



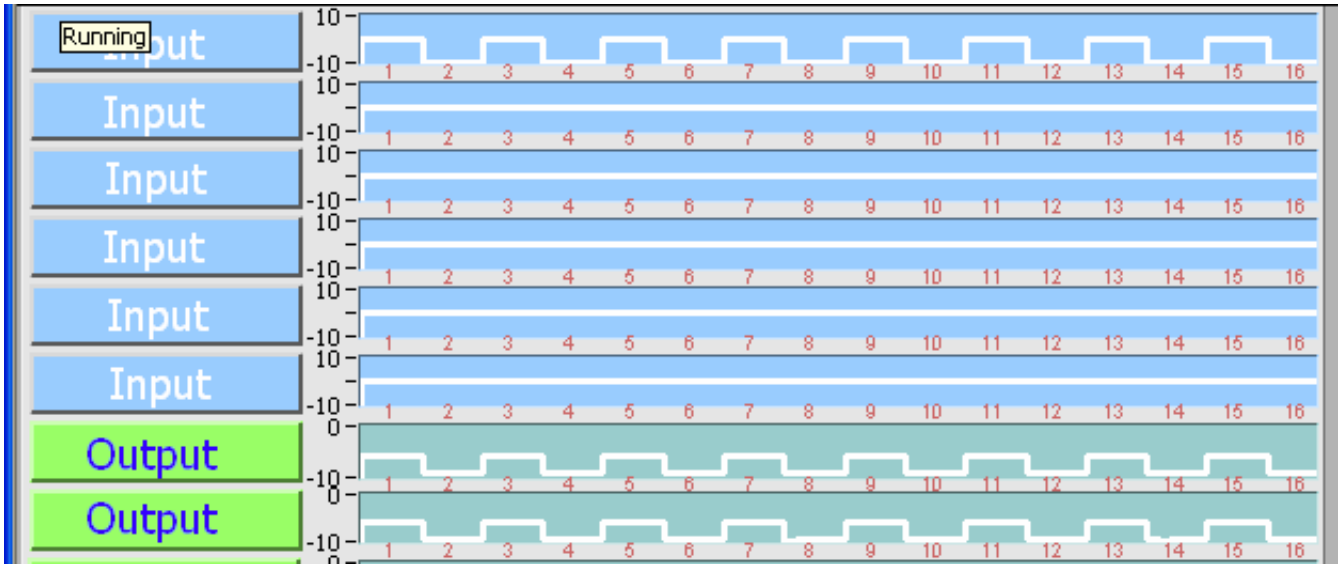
Version 4

BINARY COUNTER

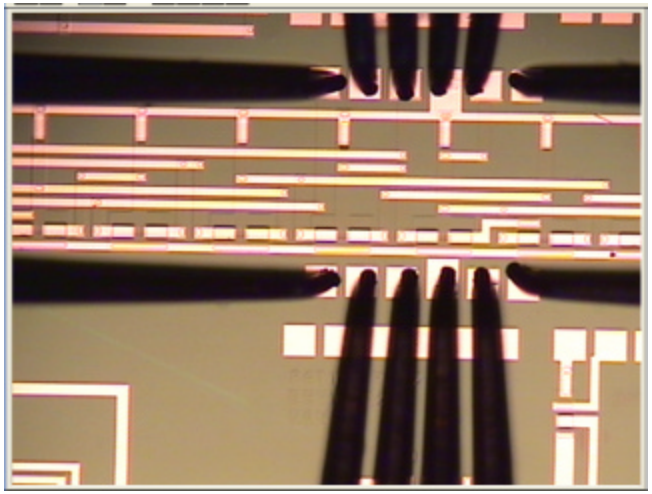


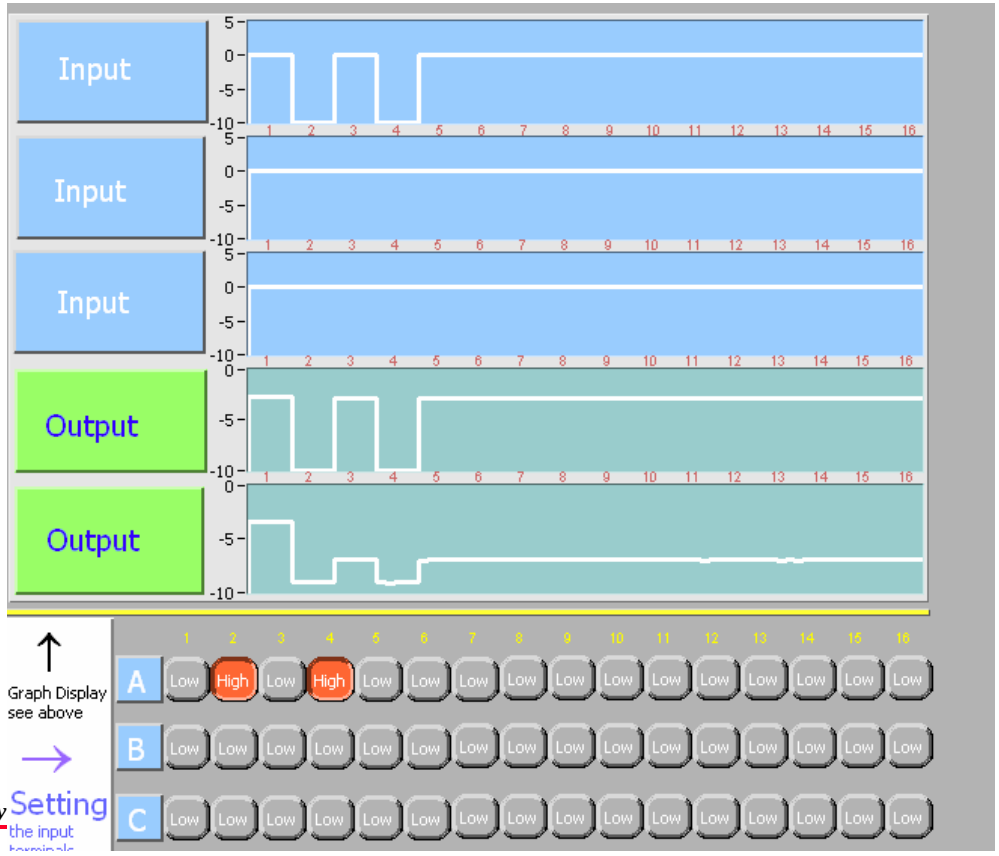
Version 5

BINARY COUNTER VERSION 3

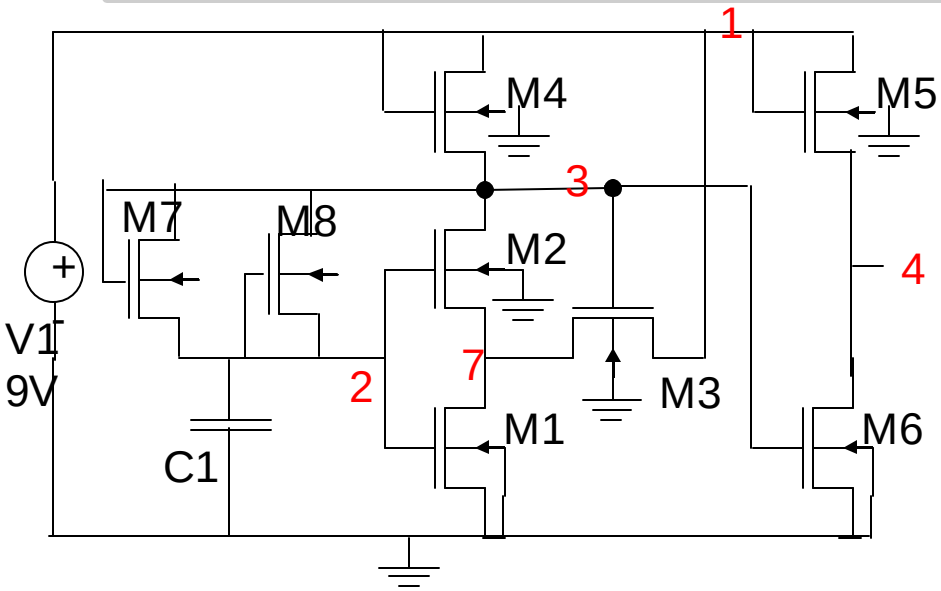


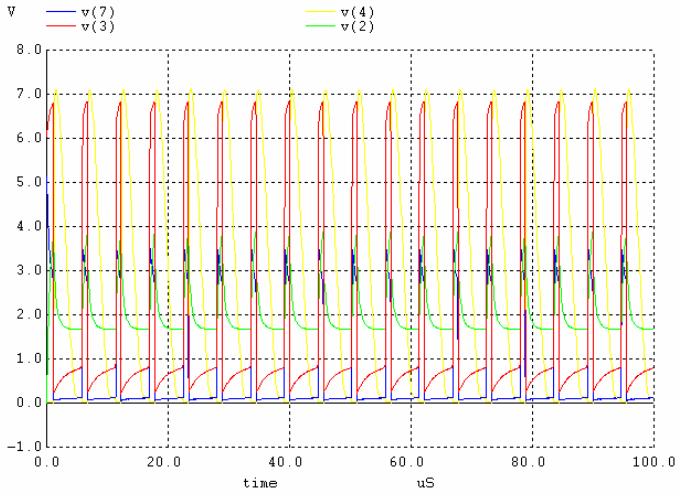
BINARY COUNTER VERSION 4





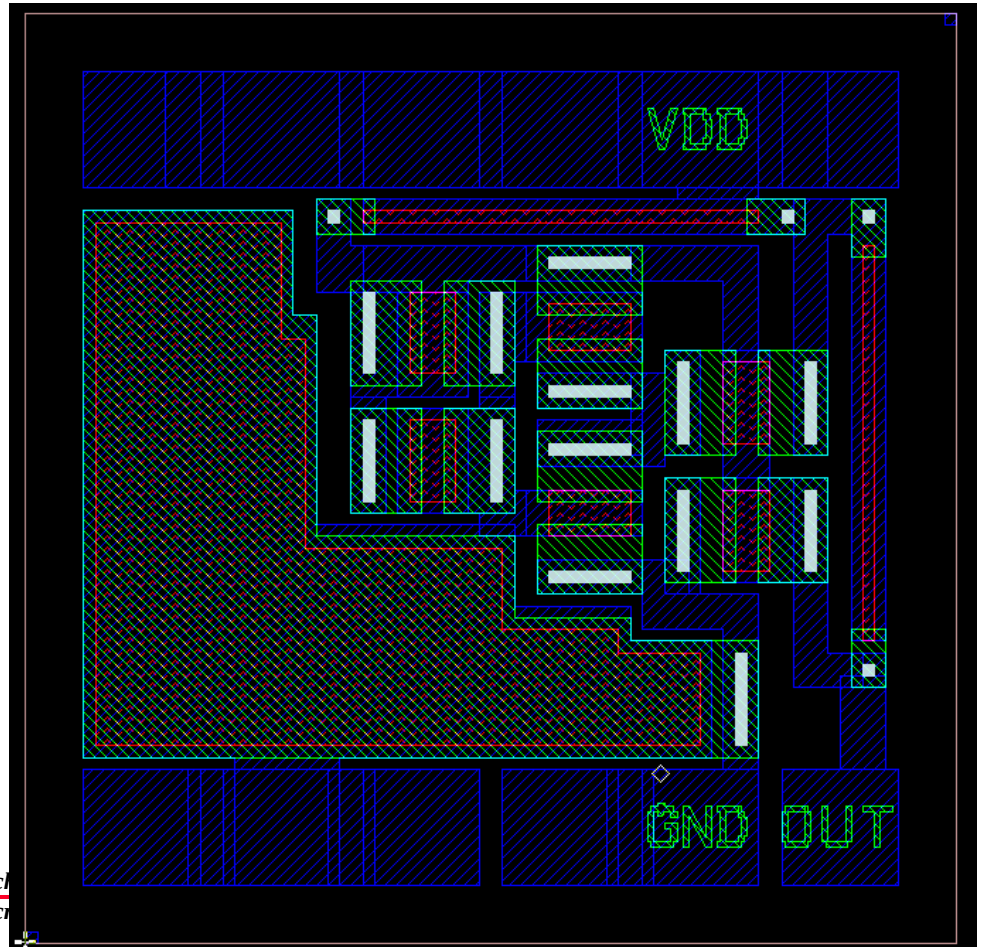
RC OSCILLATOR, INVERTER WITH HYSTERESIS





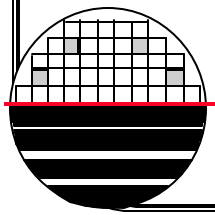
3.0pF

RC OSCILLATOR LAYOUT

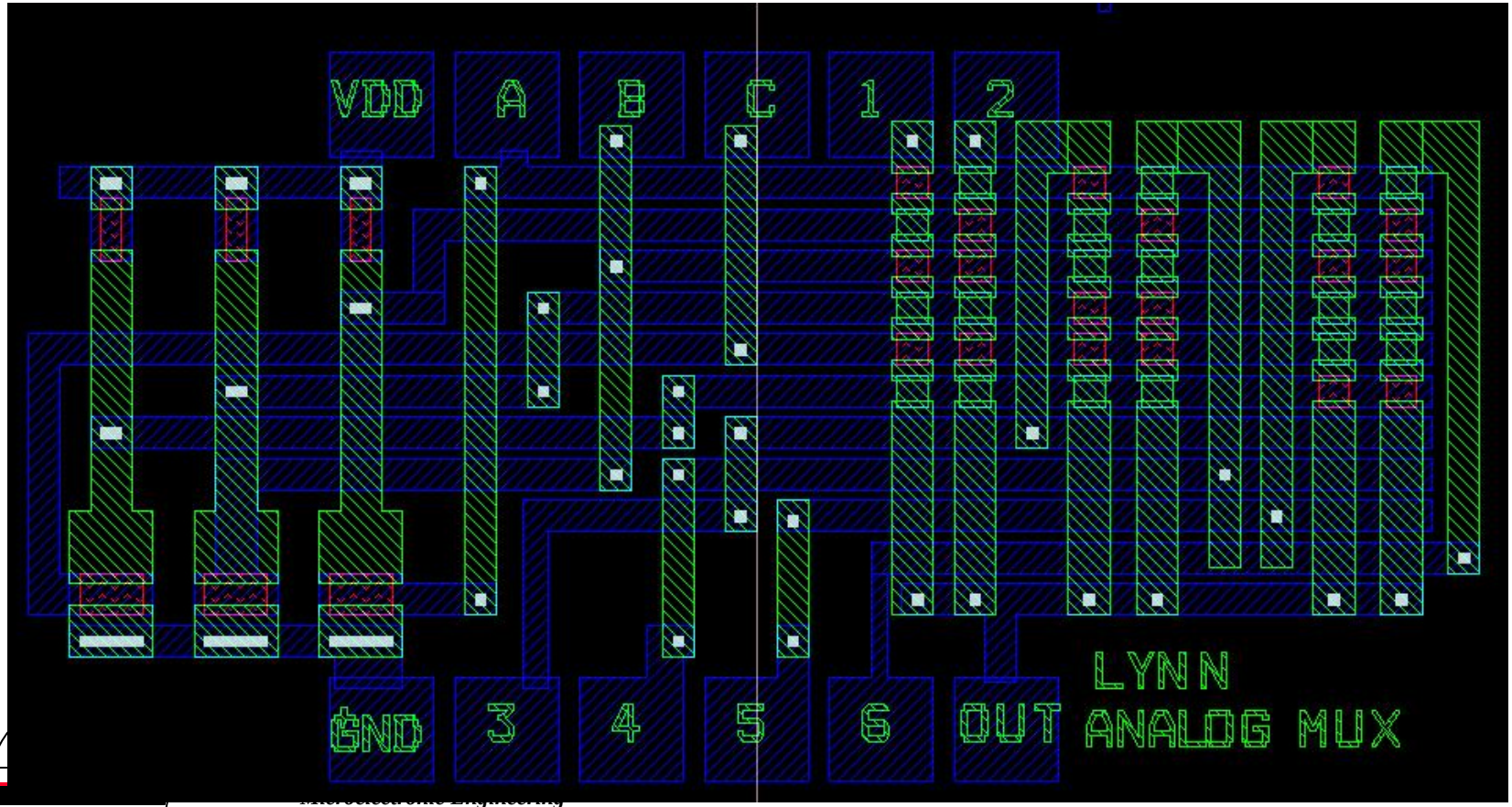


RC OSCILLATOR TEST RESULTS

Test Results



PMOS ANALOG MUX



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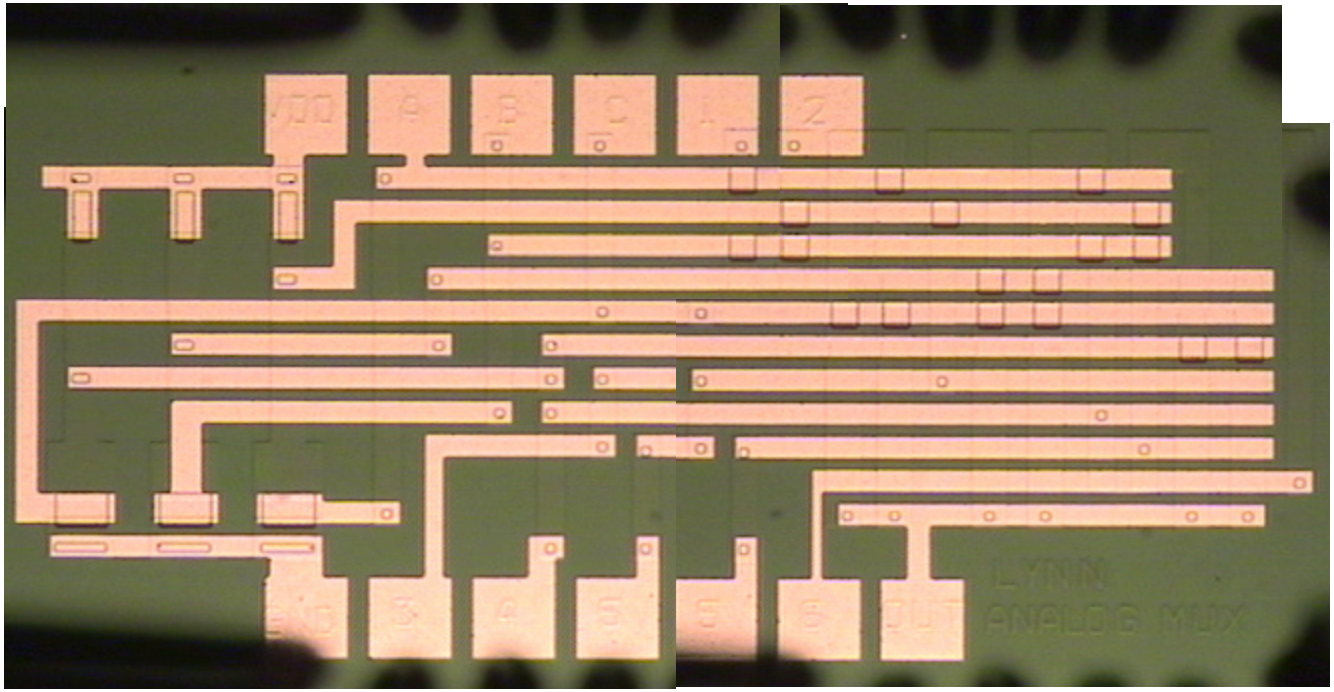
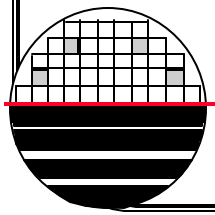


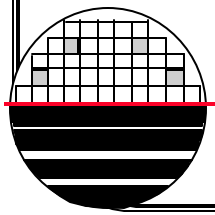
PMOS ANALOG MUX

Test Results



REFERENCES

1. CMOS Analog Circuit Design, Phillip E. Allen, Douglas R. Holberg, Holt, Rinehart and Winston, 1987.
2. Fundamentals of Logic Design, 2nd Edition, Charles H. Roth, Jr.,West Publishing Company, 1979.
3. Microelectronic Circuit Design, Richard C. Jaeger, McGraw-Hill, 1997.
4. Microelectronics, Jacob Millman, McGraw-Hill, 1979.



HOMEWORK

1. Redesign the XOR using only NOR gates.
2. Redesign the Data Latch using only NOR gates.