ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

PMOS Testing at Rochester Institute of Technology

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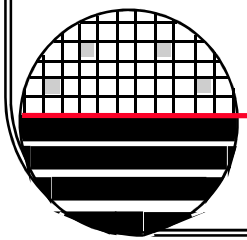
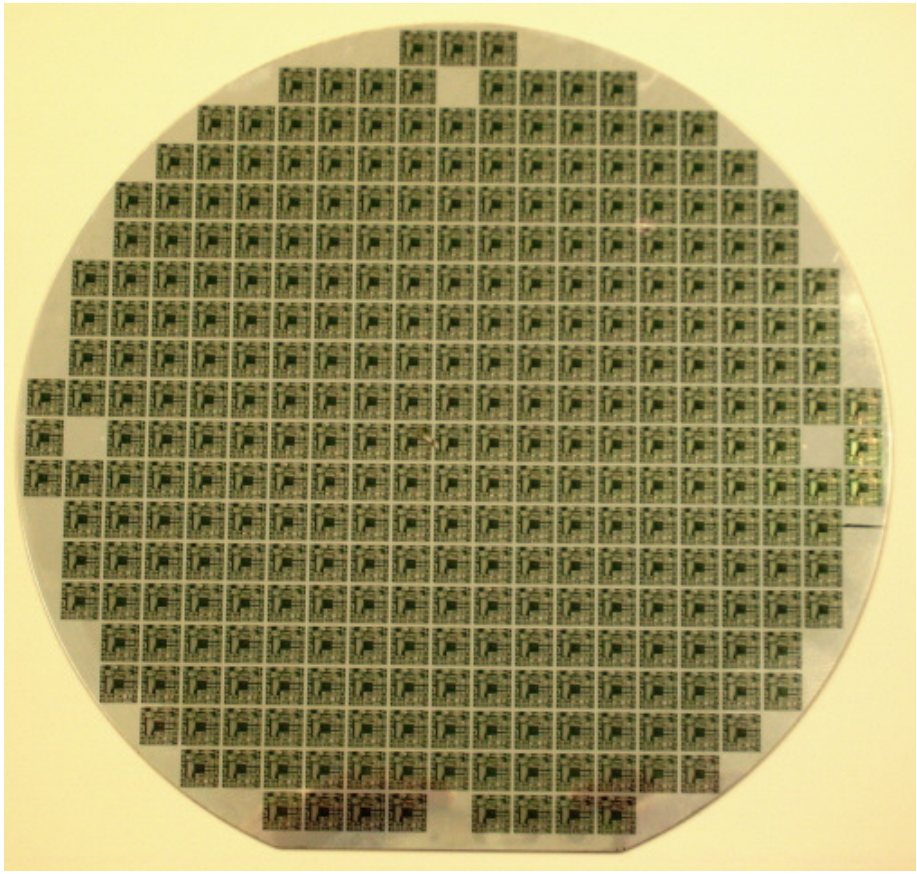


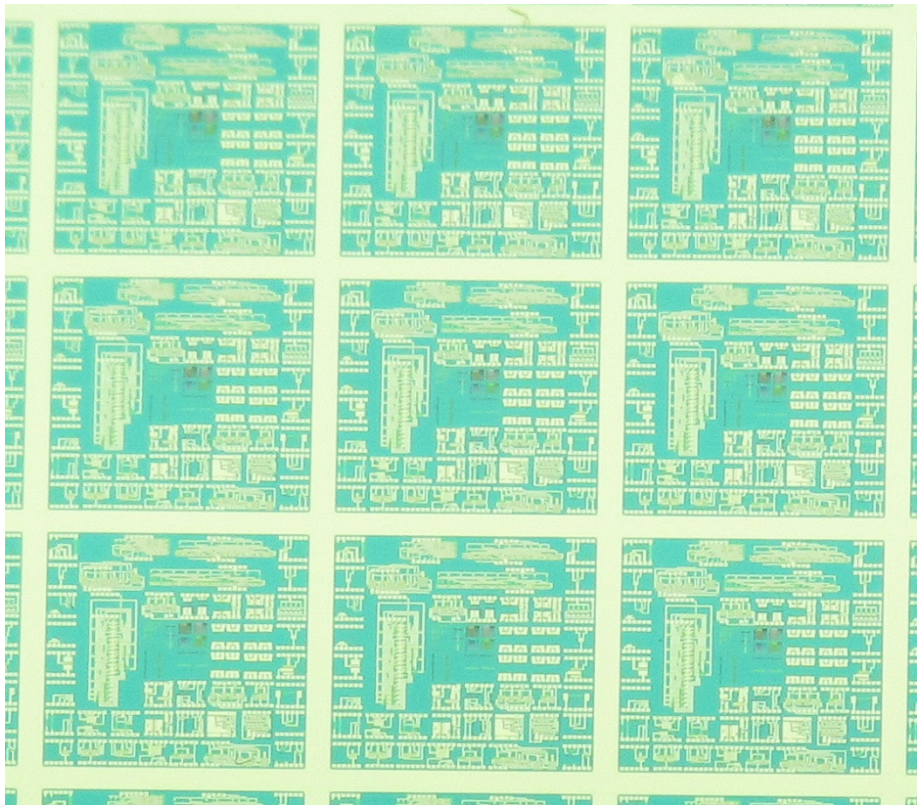
OUTLINE

- Test Chip
- Test Equipment
- Resistive Structures
- Transistors
- Integrated Circuits
- Ring Oscillator
- Digital Circuits

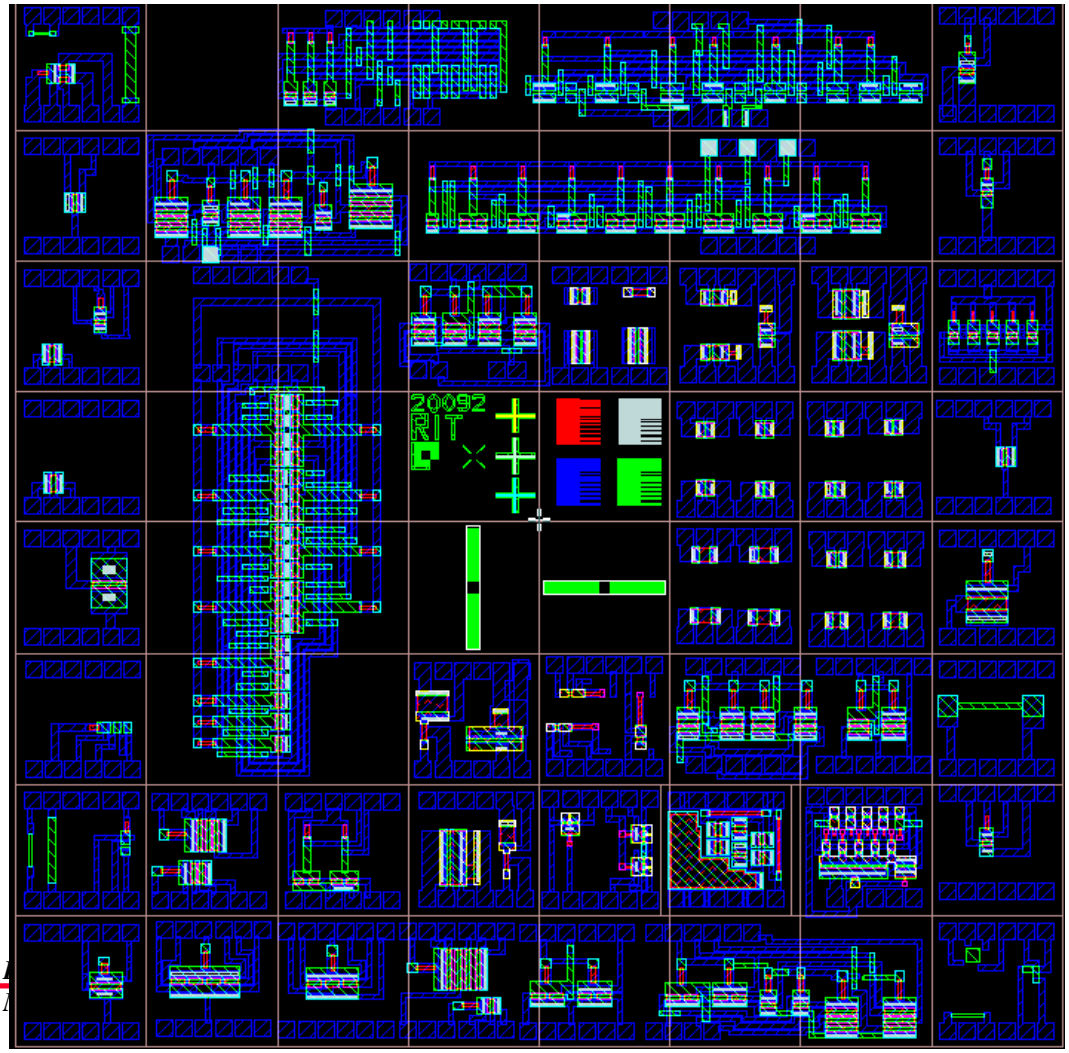


THE TEST CHIP

- Alignment Marks
- CD Linewidth, Overlay
- Van Der Pauw, p+ DS, Metal
- MOSFET's,
- Inverters
- Ring Oscillator
- CBKR
- Digital Circuits



PMOS TEST CHIP

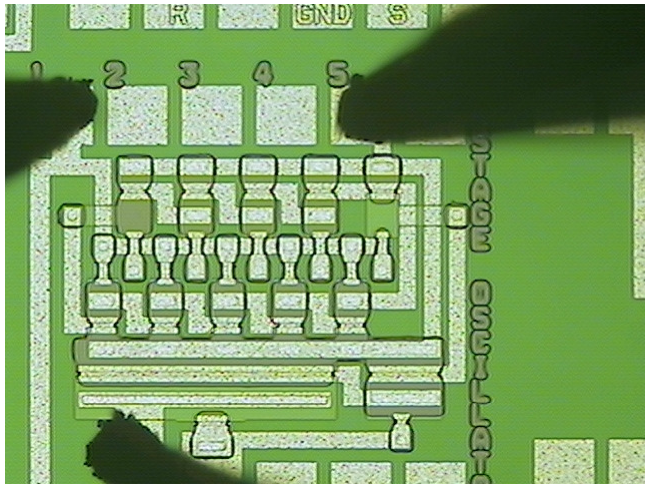


Fall 2010

TEST FACILITY

HP4145
Semiconductor Paramater Analyzer

Keithley
7001 Switch Matrix



Computer
ICS Software
Camera

Ultracision
Semi-Automatic
Wafer Prober

Test Fixture
and
Manual Probe Station

TEST EQUIPMENT

Automatic Prober

Semi-automatic Prober

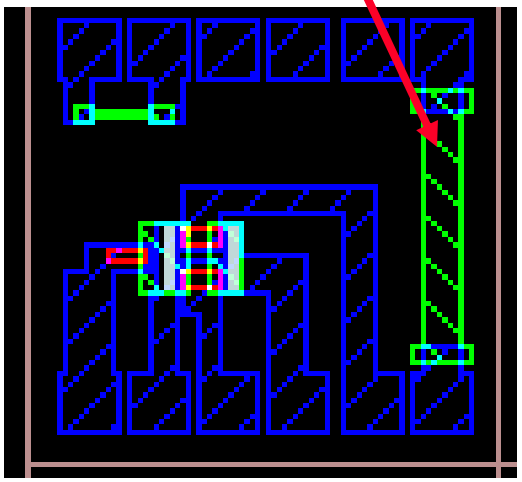
TEST EQUIPMENT

Manual Prober

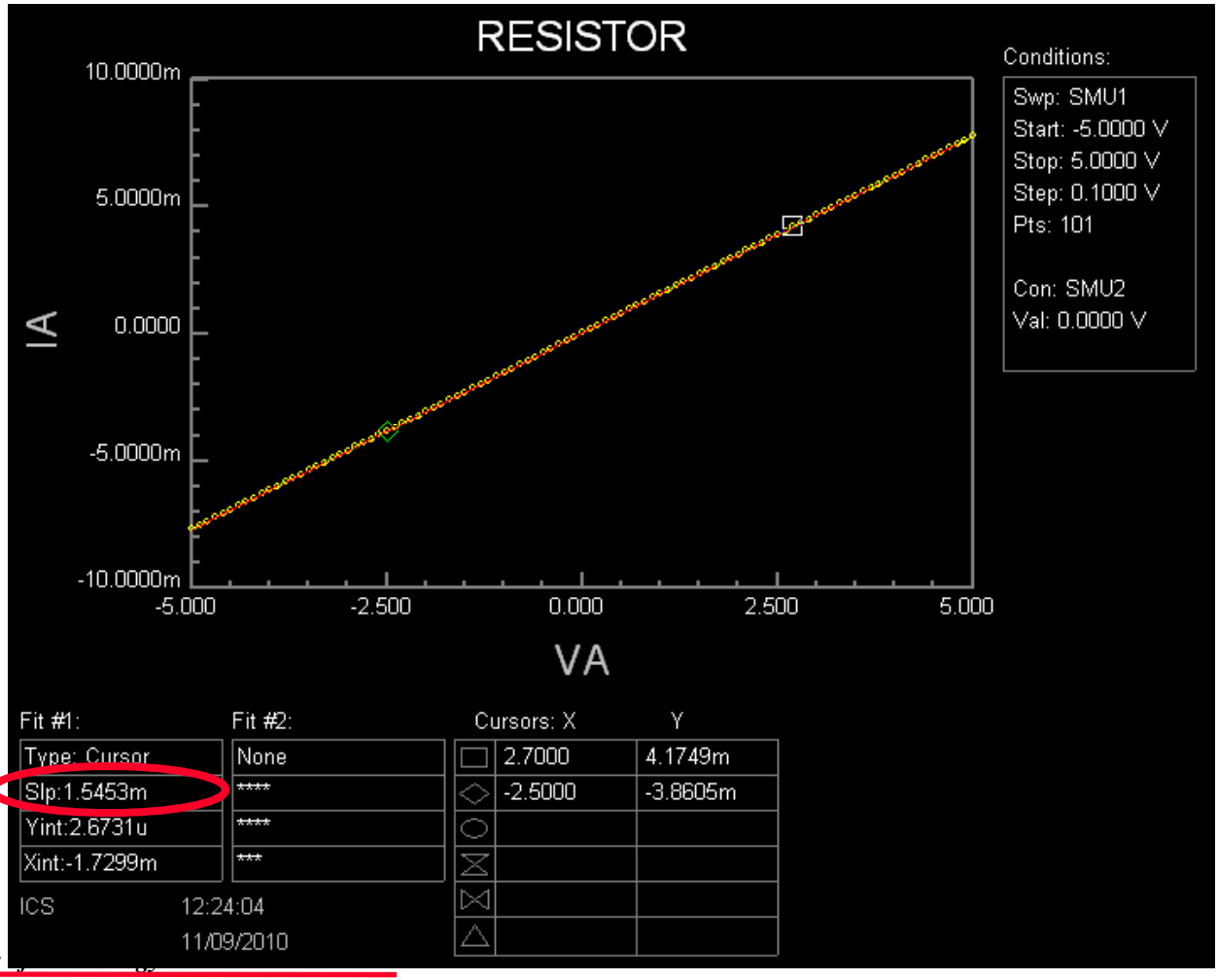
RESISTOR TEST RESULTS

R = Rhos L/W

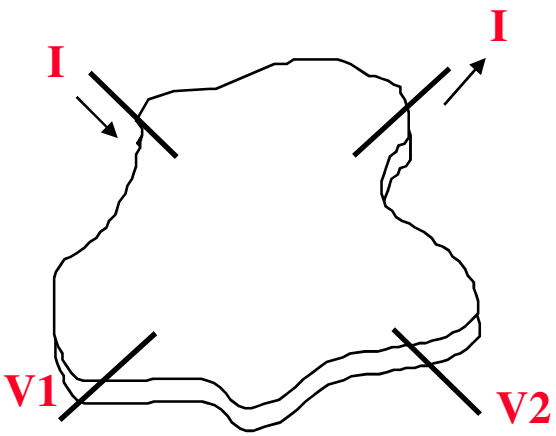
L/W = 400/60

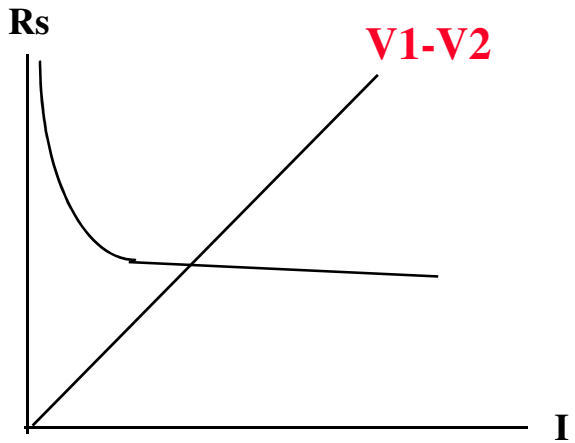


R = V/I = 1/slope
= 647 Ω

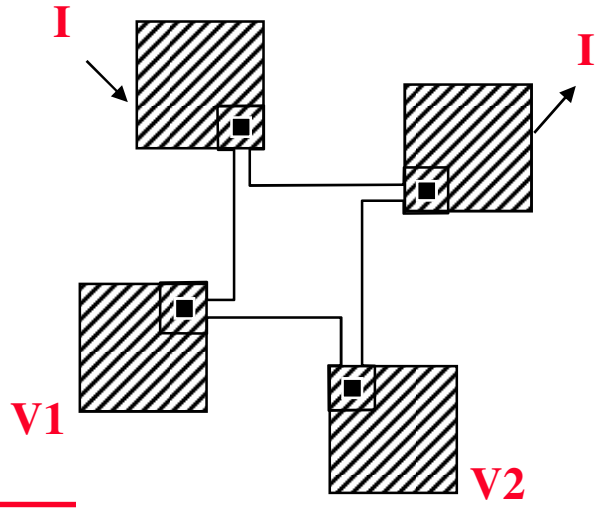


VAN DER PAUW TEST STRUCTURES FOR SHEET RESISTANCE

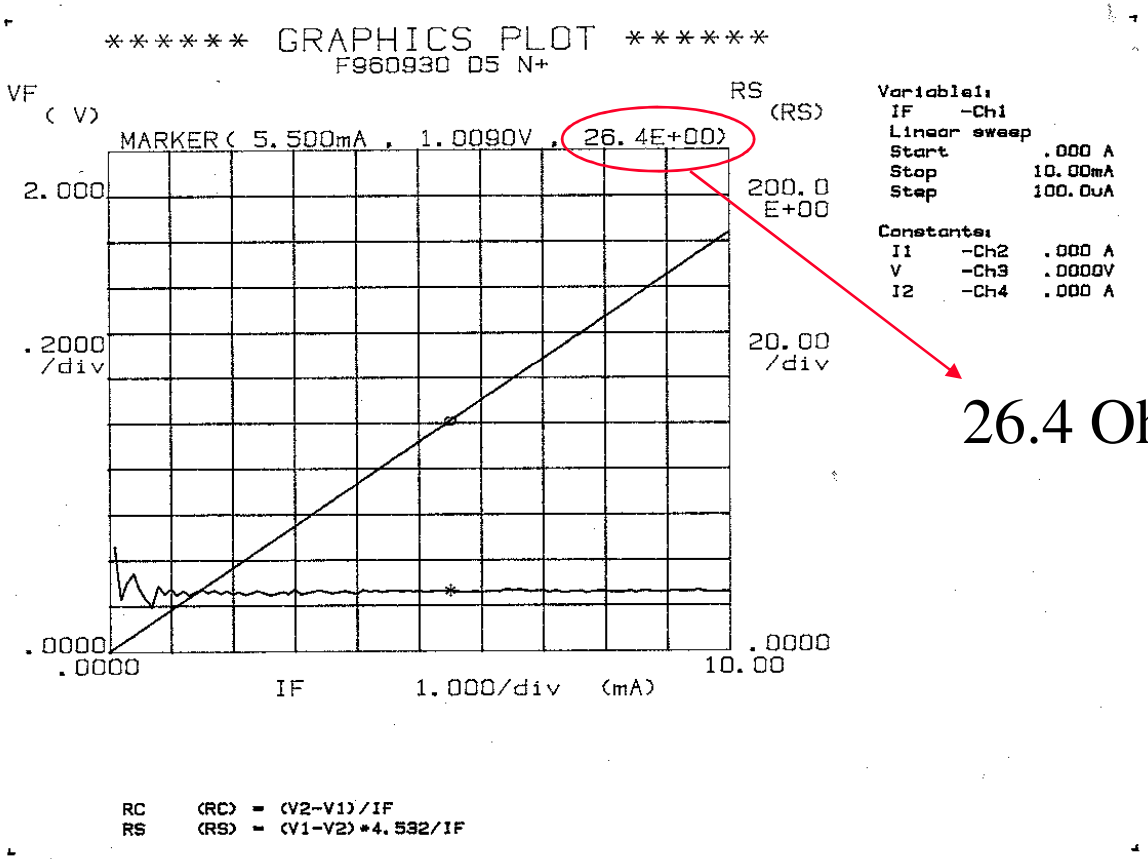




$$Rs = \frac{(V1-V2)\ \Pi}{I \quad \ln 2}$$

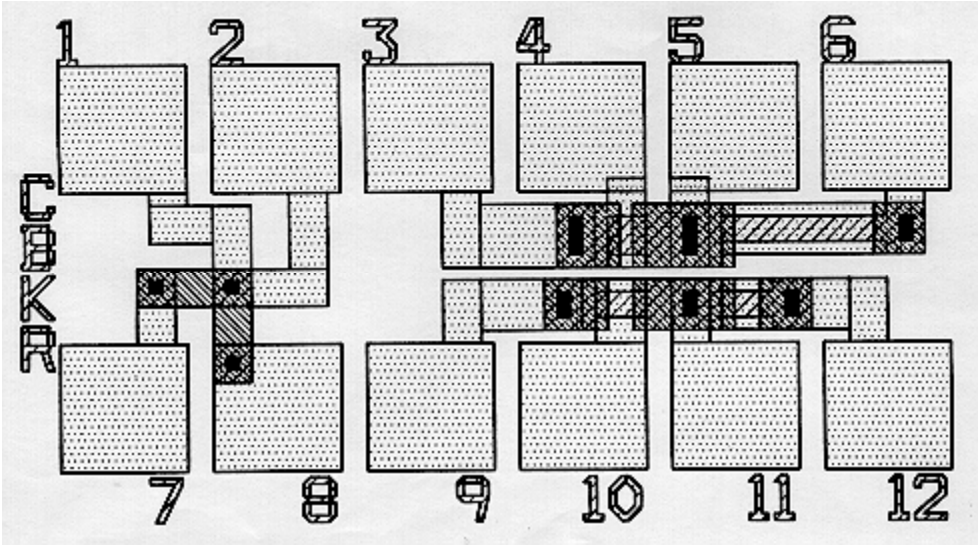


VAN DER PAUW TEST RESULTS

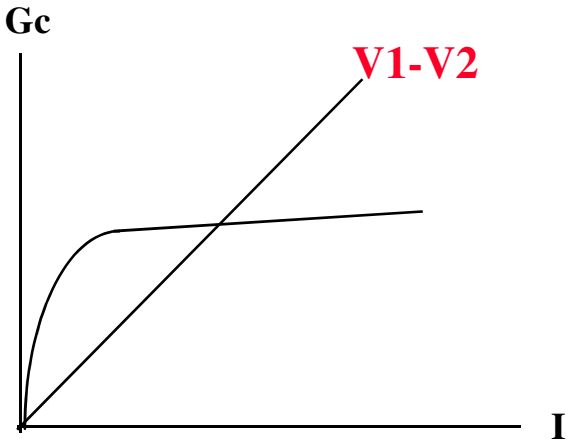


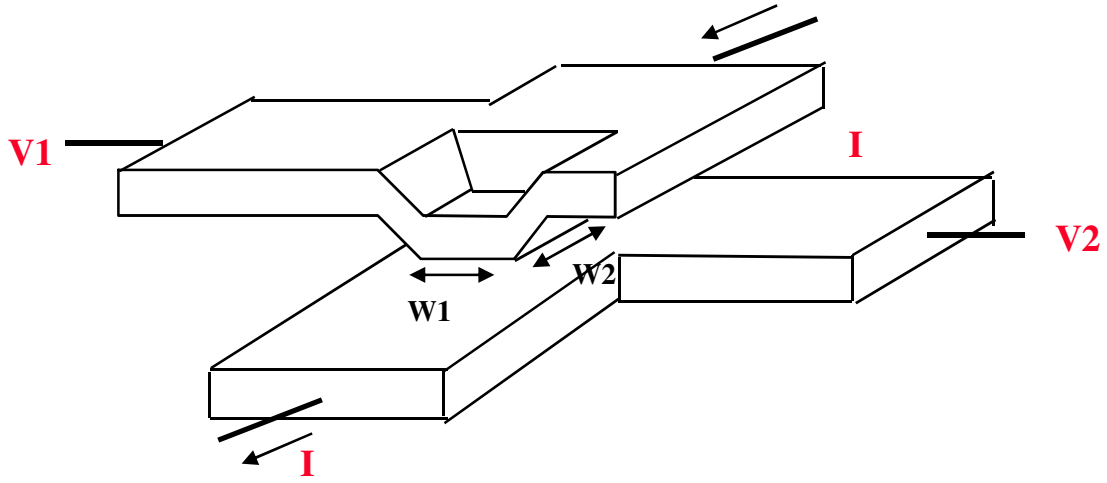
26.4 Ohms

CBKR AND INVERTERS



CROSS BRIDGE KELVIN RESISTANCE TEST STRUCTURES FOR CONTACT RESISTANCES

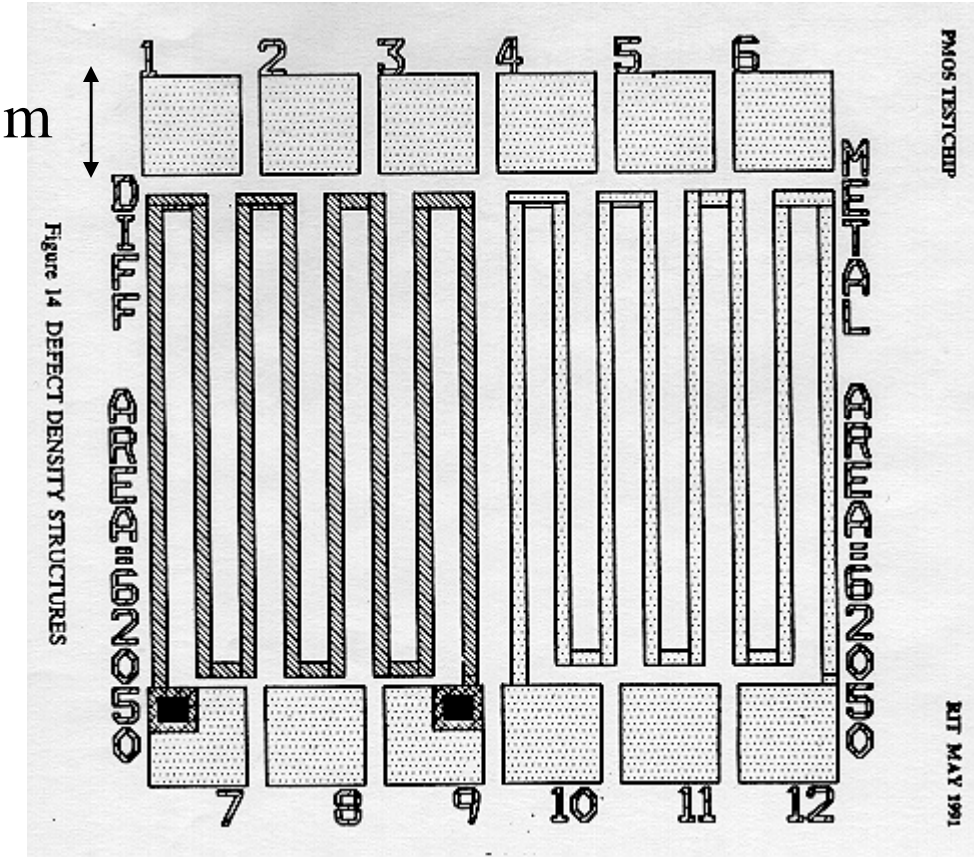




$$Rc = \frac{(V1-V2)}{I} \quad \text{ohms}$$

$$Gc = \frac{I}{(V1-V2)} \frac{1}{W1 \times W2} \quad \text{mhos}/\mu m^2$$

METAL AND DIFFUSION SERPENTINE

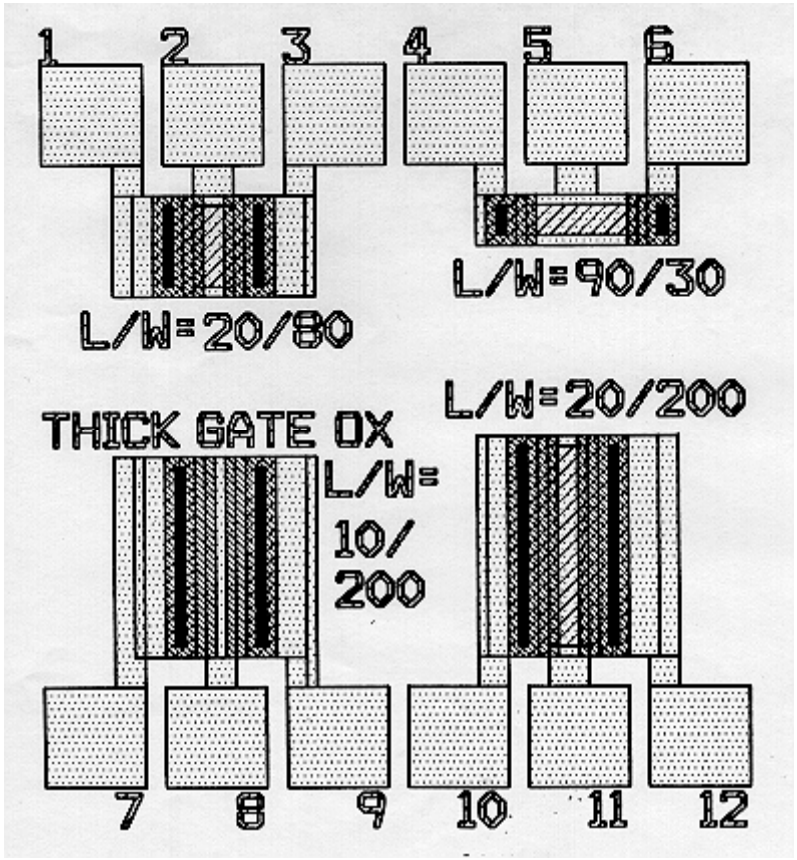


Line width = 15 µm
Line Space = 30 µm
L/W = 269
Area Covered by metal
= 62050 µm^2

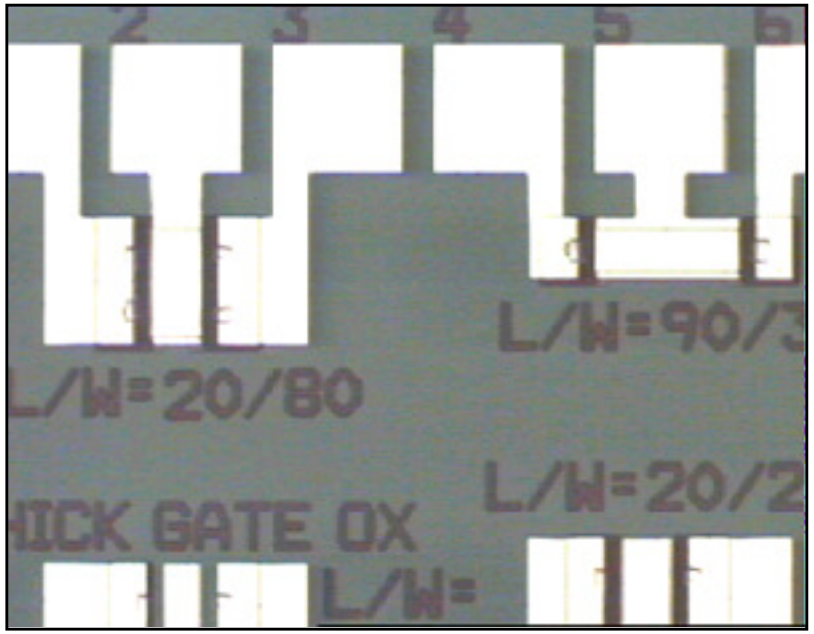
R = Rhos L/W

Defect density (in #/cm^2) = (# defective x 1612) / (# tested)

PMOS TRANSISTORS

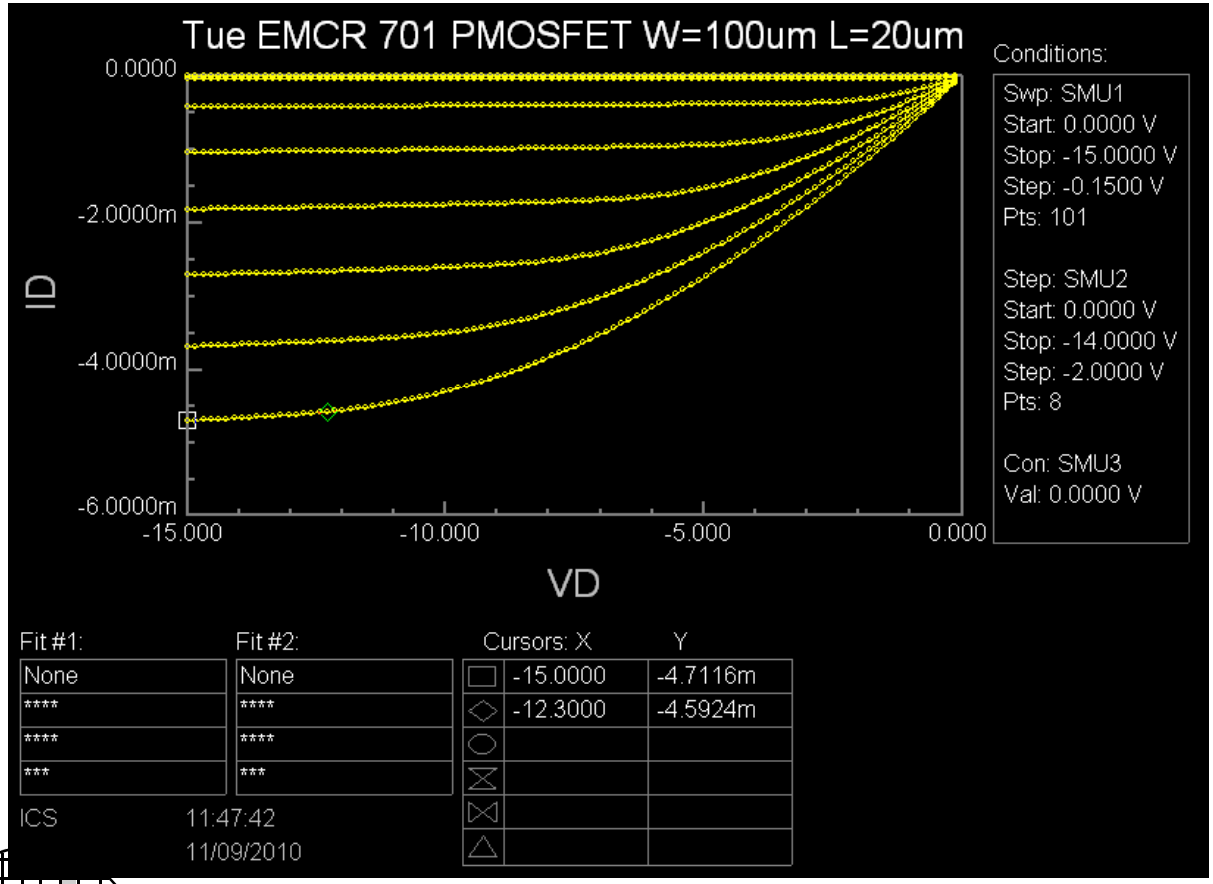


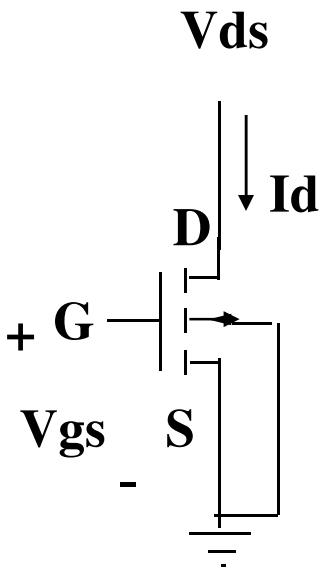
Layout



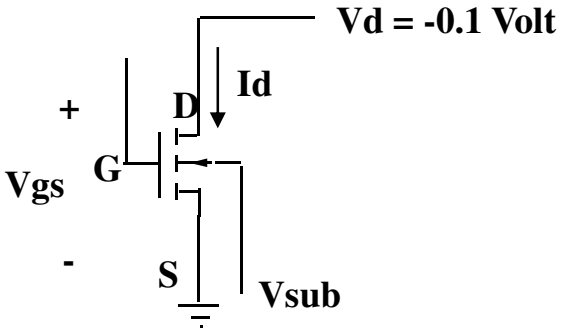
Photograph

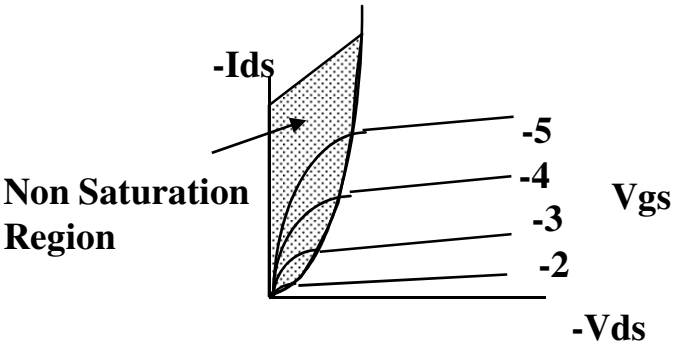
PMOS TRANSISTOR TEST RESULTS

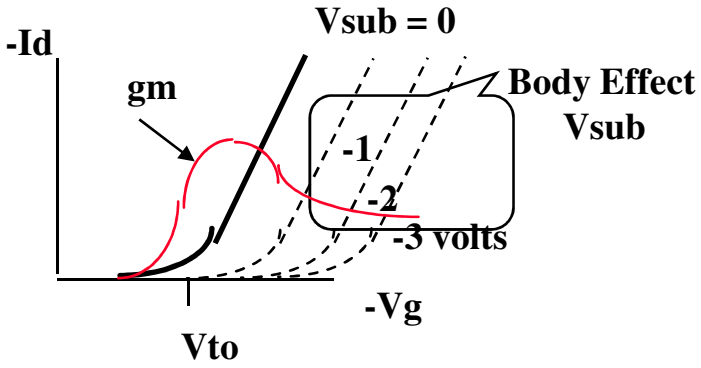


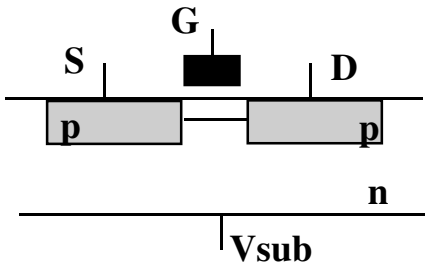


TRANSISTOR LINEAR REGION VT, GM





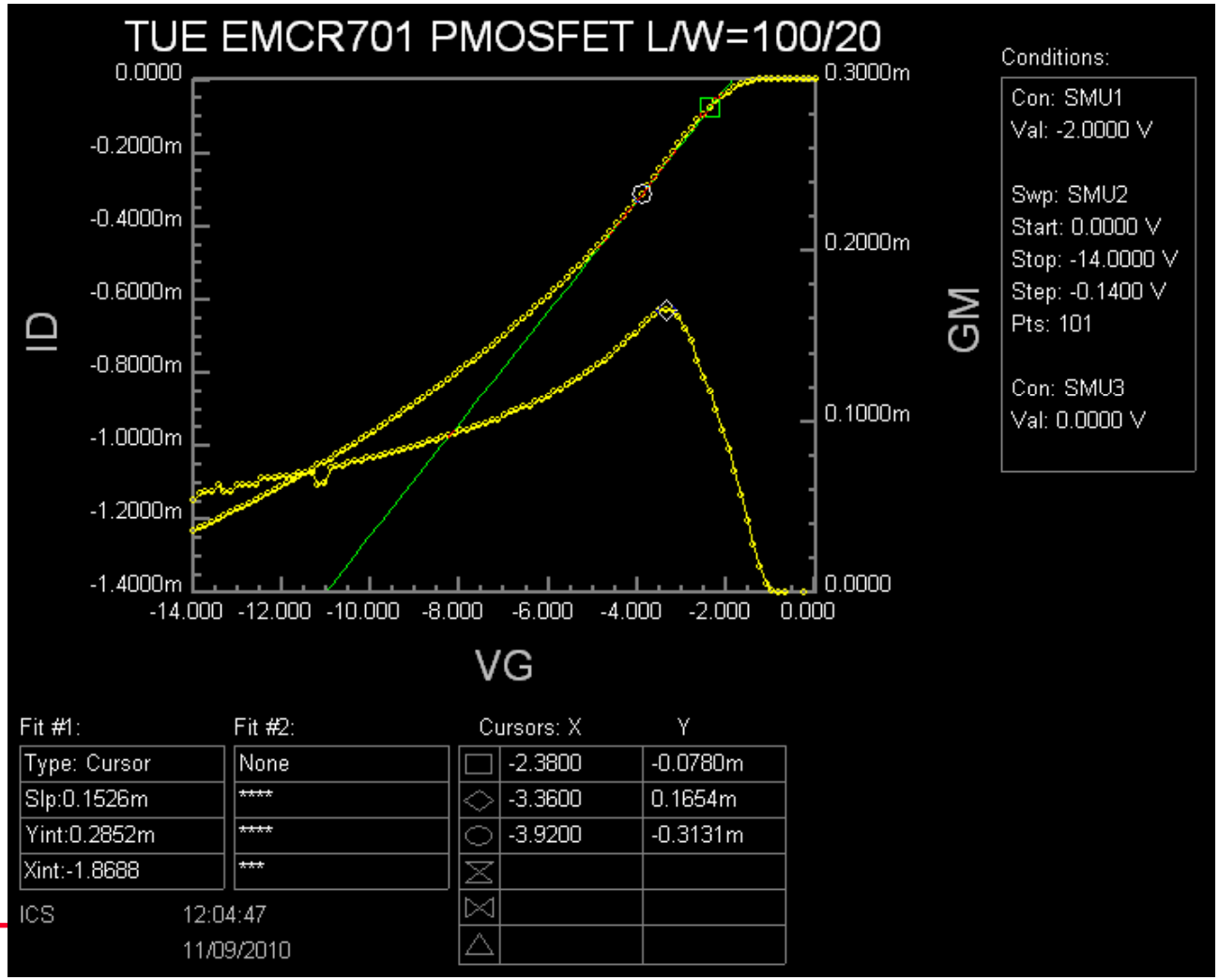




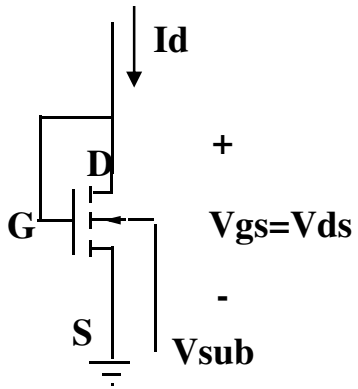
$$gm = \Delta Id/\Delta Vg$$

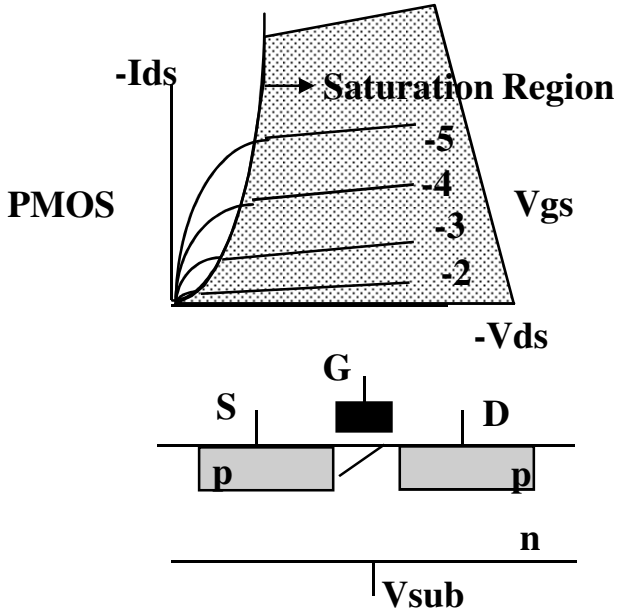
pMOSFET with Vt=-1, since the Drain is at -0.1 volts and the source is at zero. Both drain and source will be on at gate voltages greater than -1.1 volt. the transistor will be in the non saturation region.

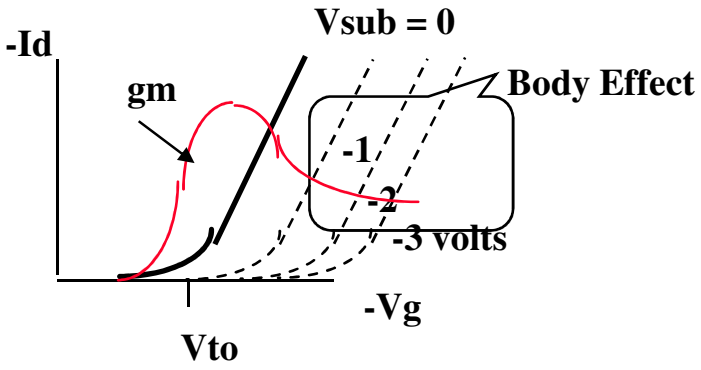
LINEAR REGION TEST RESULTS



TRANSISTOR SATURATION REGION VT, GM



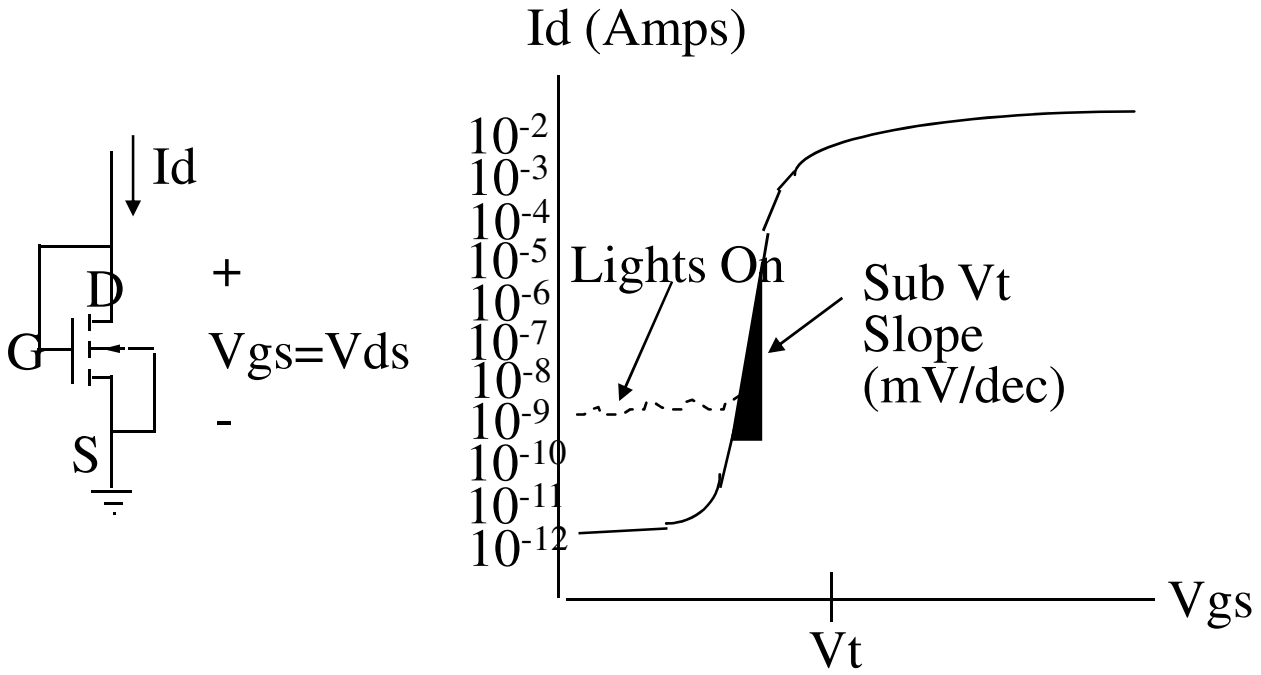




$$gm = \Delta Id/\Delta Vg$$

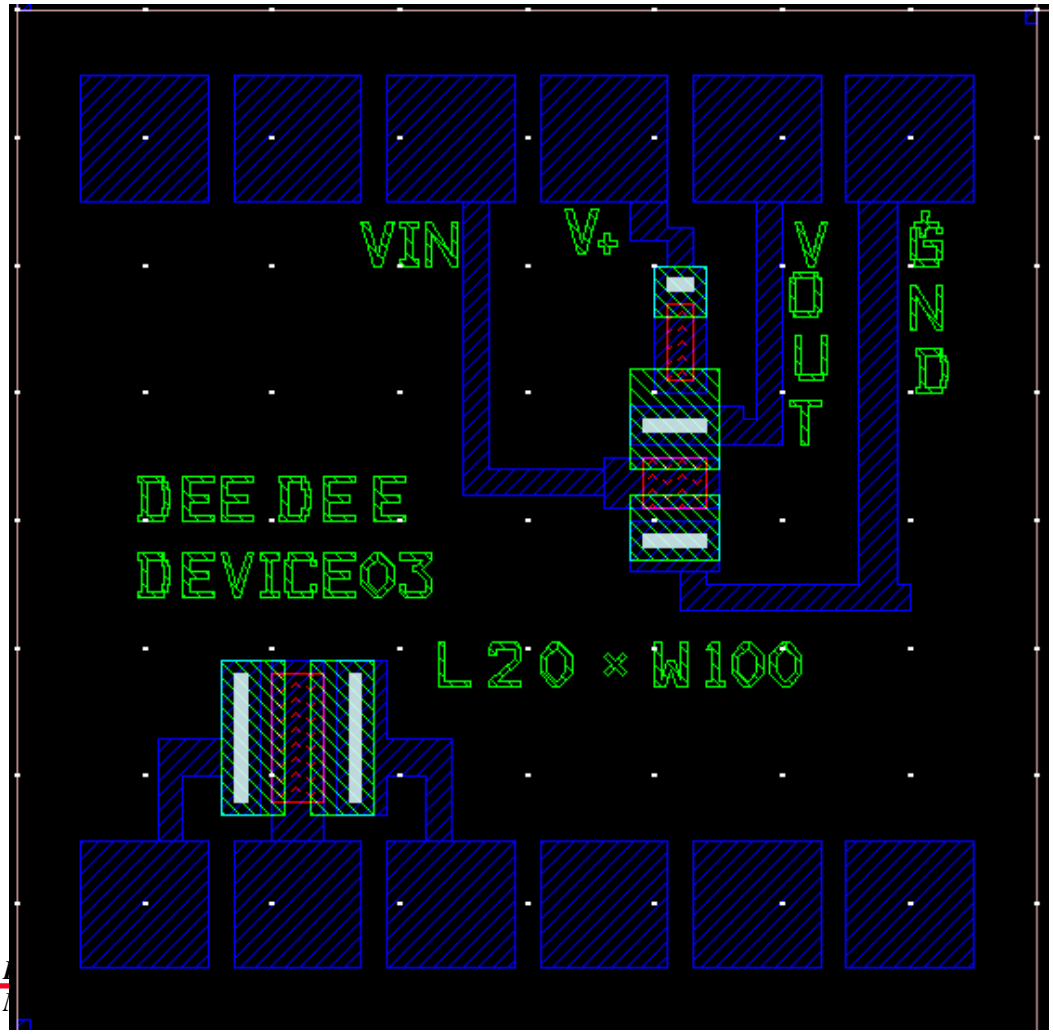
pMOSFET with Vt=-1, Drain end is never on because Voltage Gate to Drain is Zero. Therefore this transistor is always in Saturation Region if the gate voltage is above the threshold voltage.

TRANSISTOR SUB THRESHOLD ID-VGS



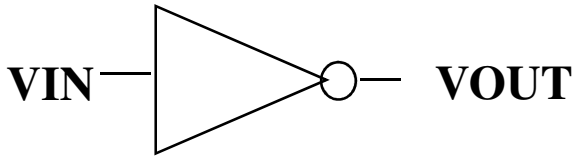
The subthreshold characteristics are important in VLSI circuits because when the transistors are off they should not carry much current since there are so many transistors. (typical value about 100 mV/decade)

INVERTERS

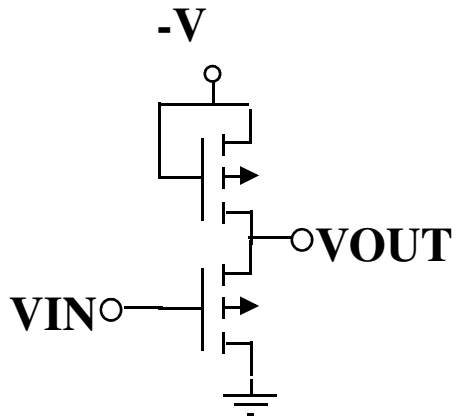


L = 40µm
W = 20µm
L = 20µm
W = 50µm

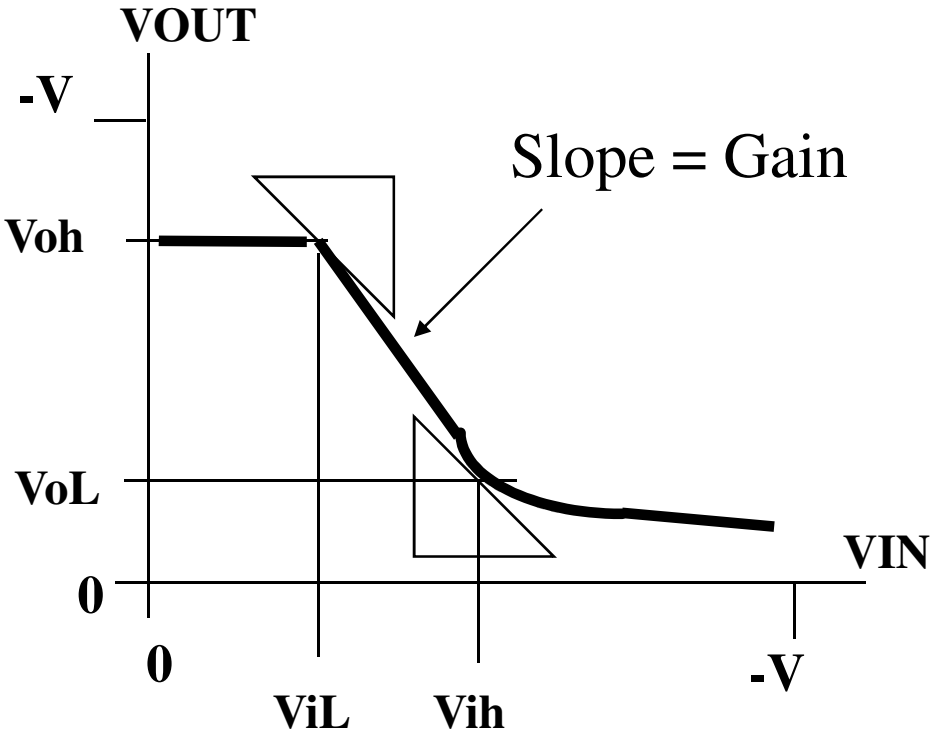
INVERTERS



$$\text{Inverter Gain} = \sqrt{\frac{Wd/Ld}{Wu/Lu}}$$



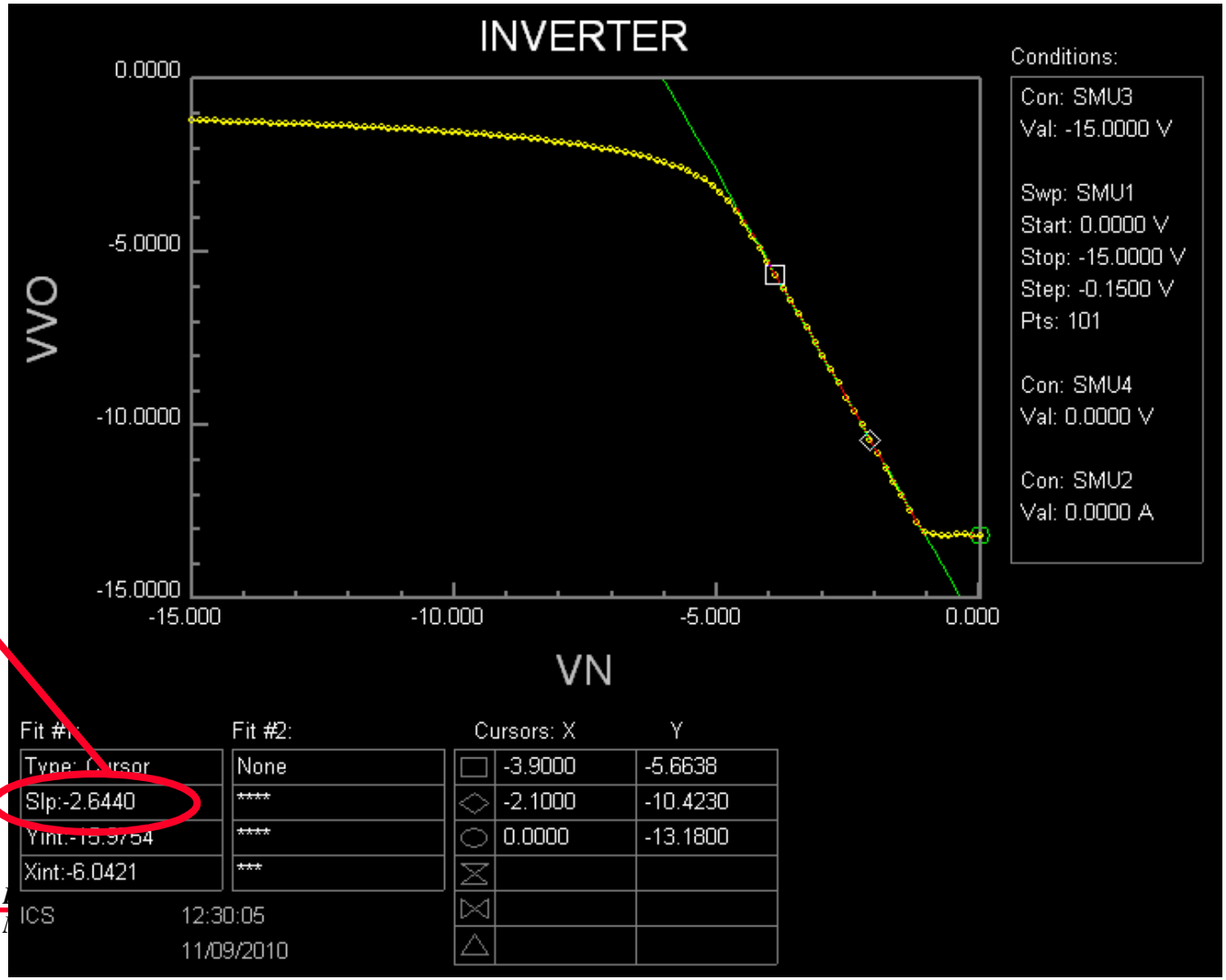
PMOS Inverter with Enhancement Load



Δ 0 noise margin = ViL - Voh

Δ 1 noise margin = Voh - Vih

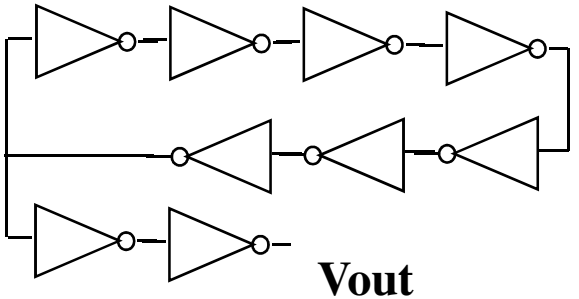
INVERTER TEST RESULTS



Gain = -2.64

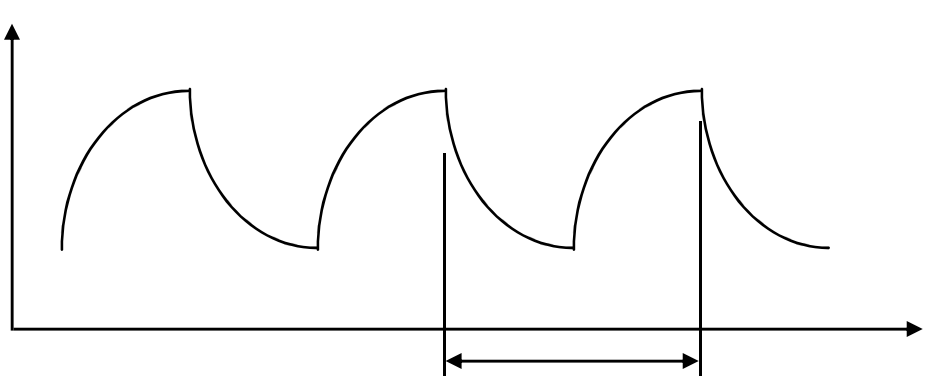
RING OSCILLATOR, td

Seven stage ring oscillator with two output buffers

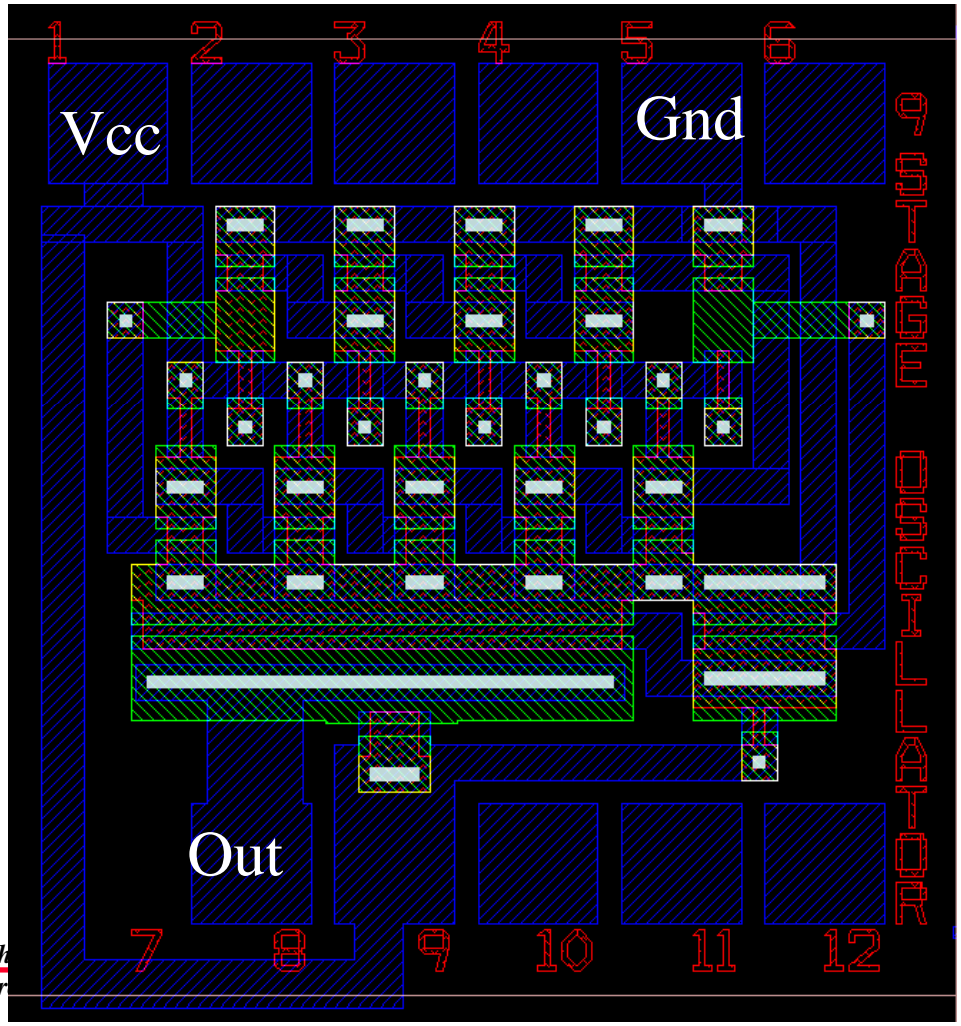


td = T / 2 N

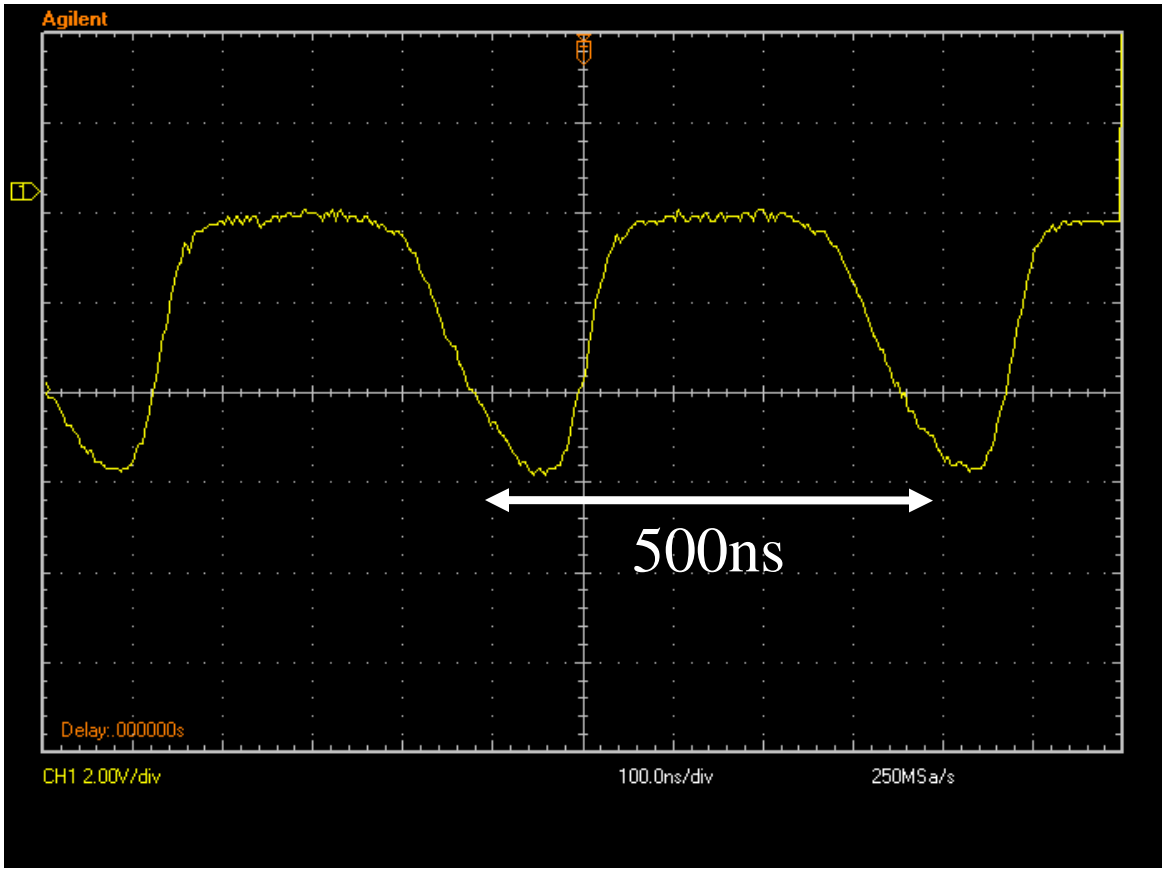
td = gate delay
N = number of stages
T = period of oscillation



9 STAGE RING OSCILLATOR

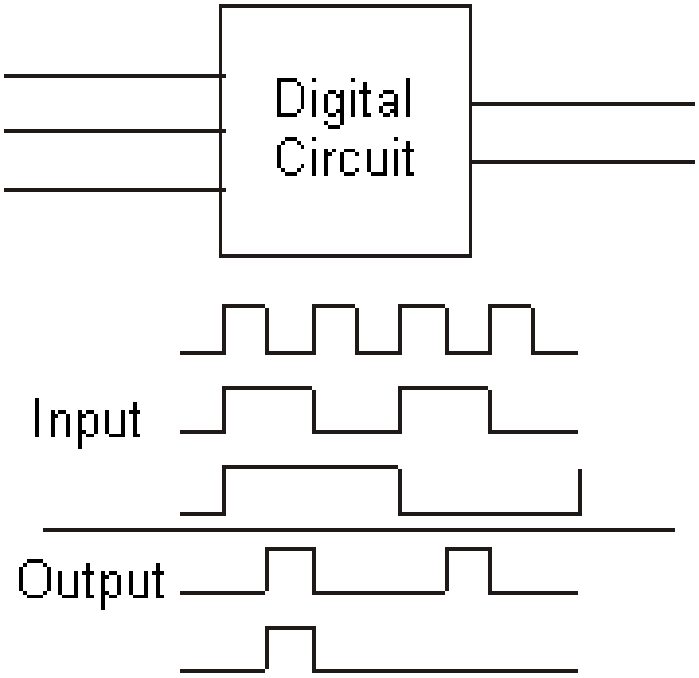


RING OSCILLATOR OUTPUT

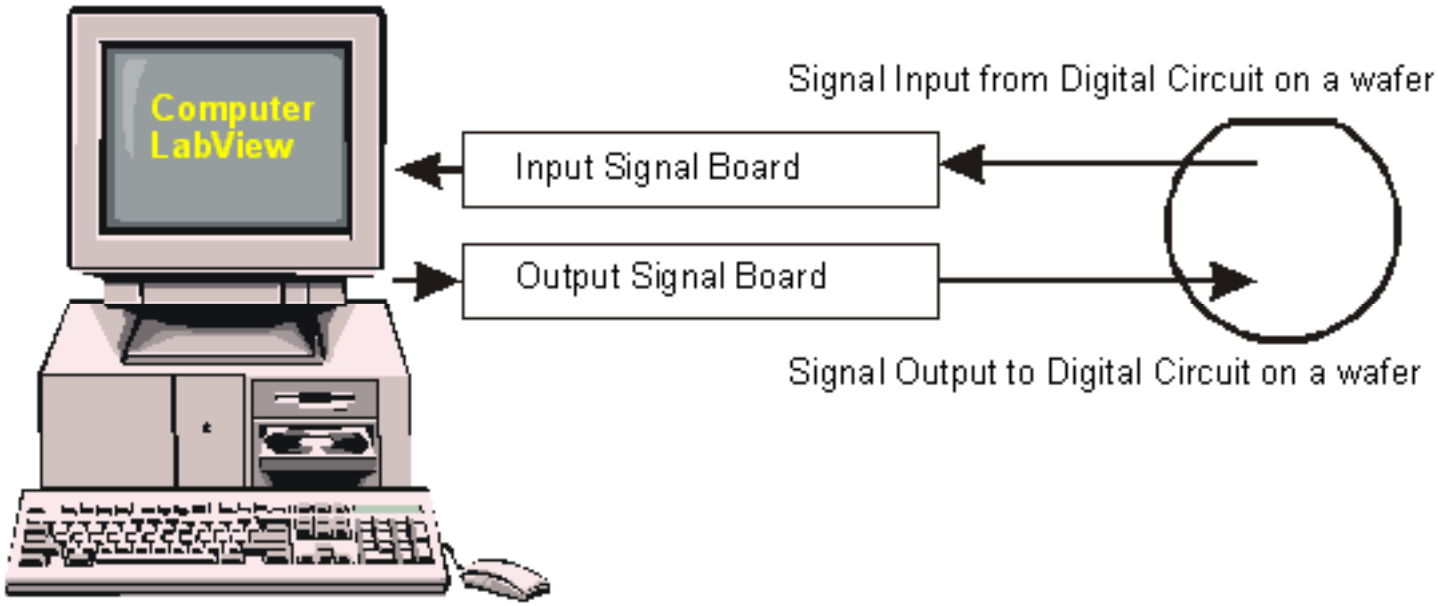


td = T / 2n
= 500 ns / 2 / 9
= 28 ns

DIGITAL CIRCUIT TESTING



LAB VIEW SOFTWARE

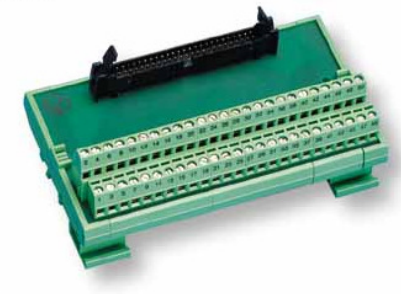


HARDWARE FOR OUTPUT

AT-AO-6

- Available for ISA computers
- 6 analog outputs; 12-bit resolution, 300 kS/s maximum update rate
- 8 digital I/O lines (5 V/TTL)
- 4-20 mA current sinks
- NI-DAQ driver with DAQ channel wizard for reduced configuration

CB50

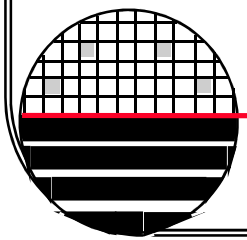


- Low-cost accessory with 50 screw terminals for easily connecting field I/O signals to your DAQ board
- One 50-pin header for directly connecting to 50-pin cables
- Mounts on a standard DIN rail or flush on a wall or panel.
- Dimensions: 13.5 by 7.3 cm (5.3 by 2.9 in.)
- Download PDFs for compatibility charts, more detailed descriptions, and ordering information

NB1

- 50-pin ribbon cable for any board with a 50 pin connector
- Connects to 50pin connector accessories
- 1 m and 2 m length options
- Download PDFs for compatibility charts, more detailed descriptions, and ordering information

6 Analog Outputs
Ribbon Cable
Terminal Board



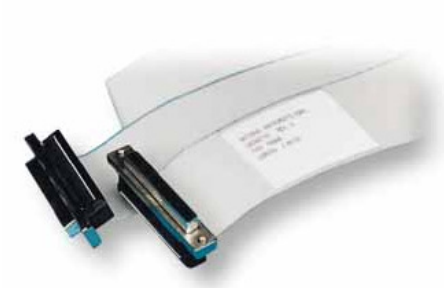
HARDWARE FOR INPUT

AT-MIO-16E-10

- Available for ISA computers
- Up to 16 analog inputs; 12-bit resolution; 100 kS/s sampling rate
- Two 12-bit analog outputs; 8 digital I/O lines; two 24-bit counters
- Calibration certificate included for NIST traceability
- NI-DAQ driver with DAQ channel wizard for reduced configuration

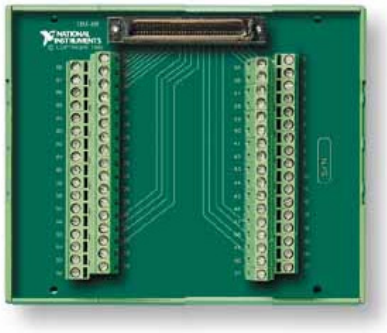
16 Analog Inputs
Ribbon Cable
Terminal Board

R6868



- 68-pin flat ribbon cable terminated with two 68-pin connectors
- 1 m length available
- Download PDFs for compatibility charts, more detailed descriptions, and ordering information

TBX-68



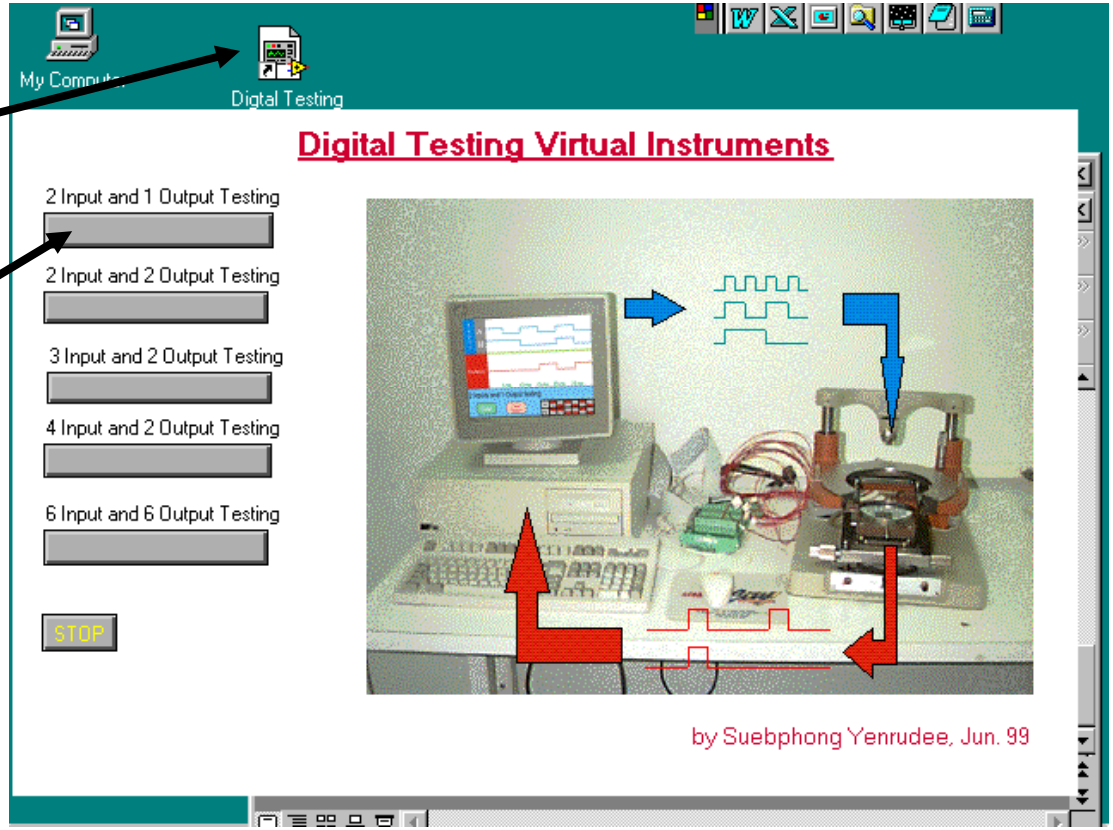
- Termination accessory with 68 screw terminals
- Easy connection of field I/O signals to 68-pinDAQ devices
- Mounted in plastic base; includes hardware for mounting on a standard DIN rail
- Dimensions: 12.50 by 10.74 cm (4.92 by 4.23 in.)
- Download PDFs for compatibility charts, more detailed descriptions, and ordering information

FINAL SYSTEM

CUSTOM SOFTWARE INTERFACE

Click on digital testing icon to invoke the lab view software and this main menu.

Click to select the type of test you wish to run.



MAIN MENU

NOR GATE AND NOR FLIP FLOP

PMOS 2 INPUT NOR

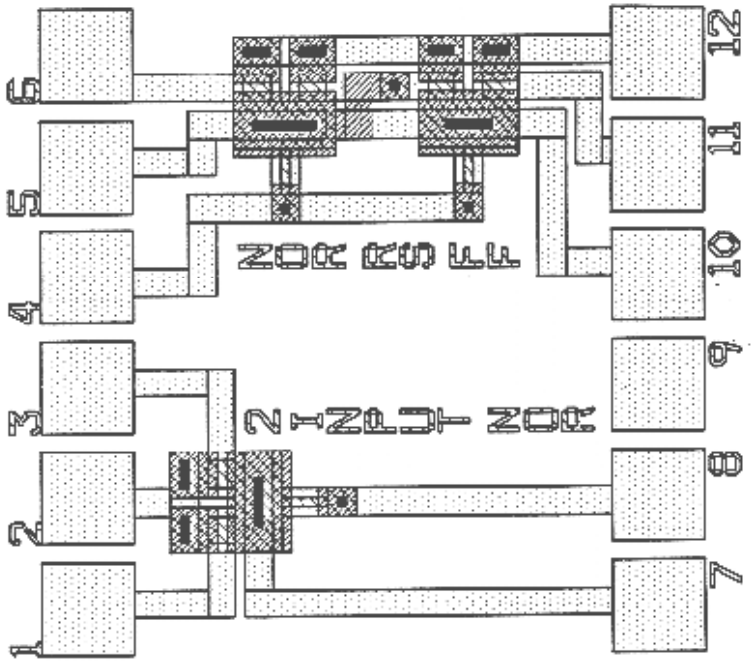
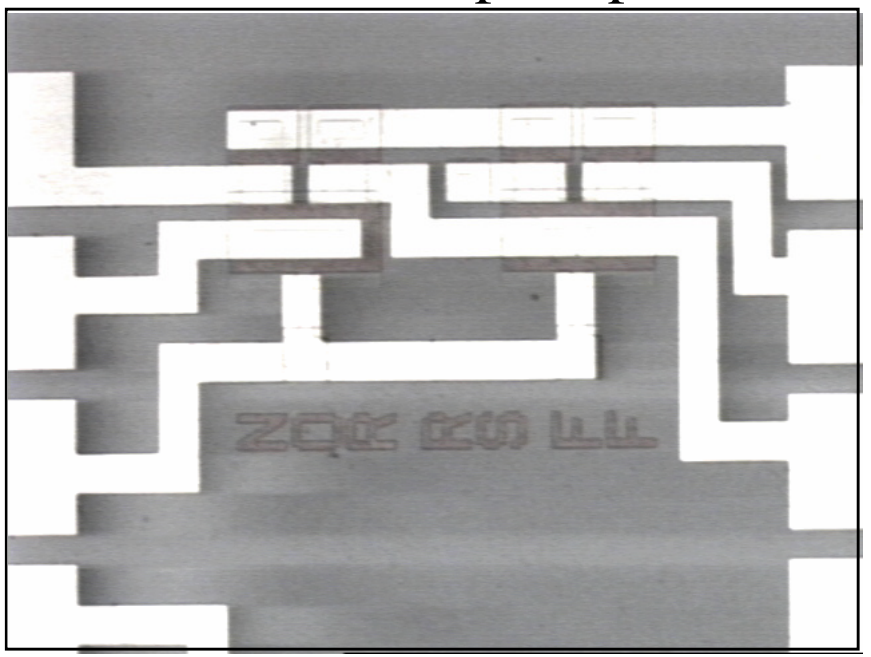
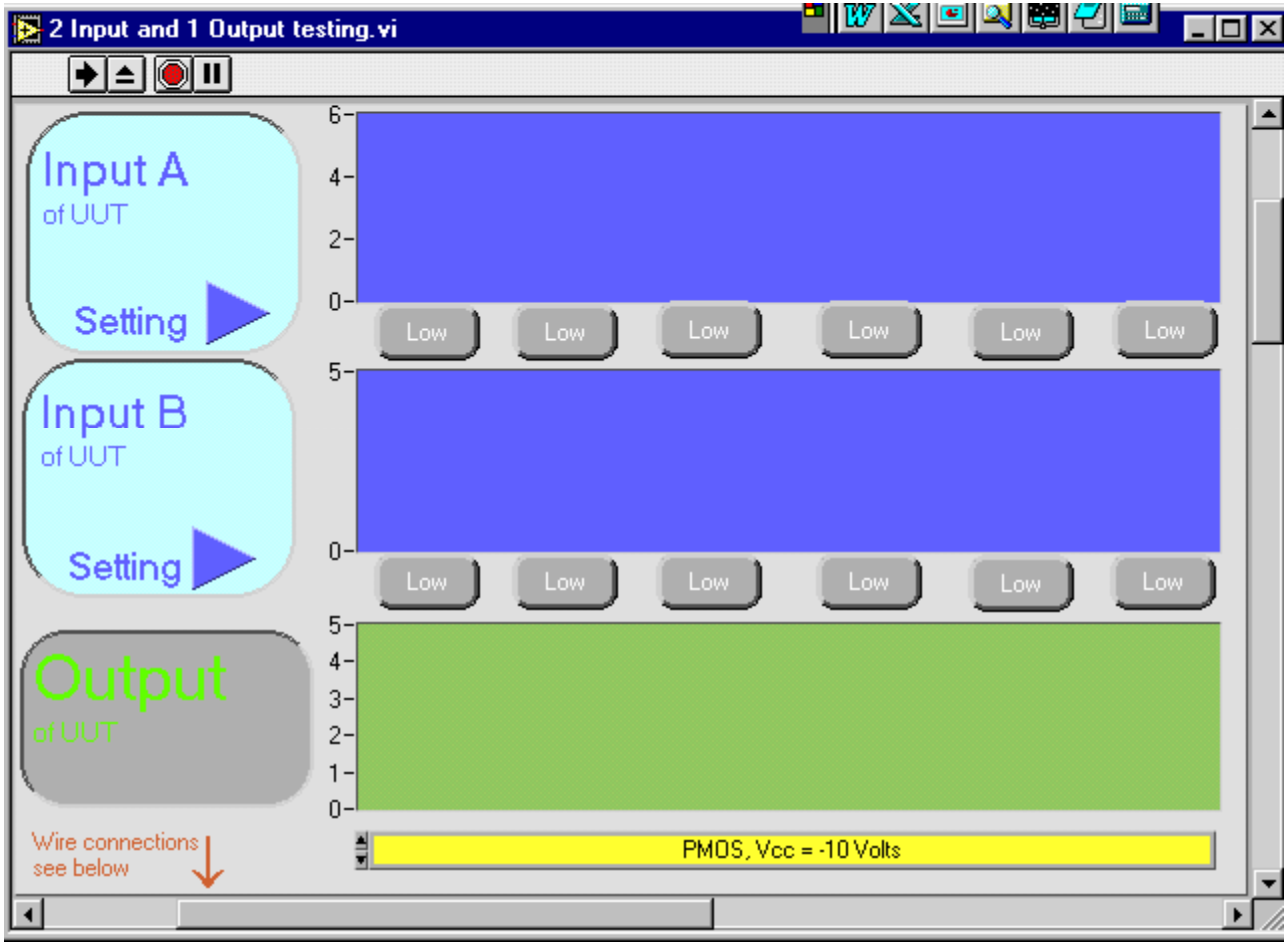


Figure 7 DIGITAL DEVICES

PMOS NOR RS Flip Flop



TESTING TWO INPUT ONE OUTPUT LOGIC GATES



FOUR CHOICES FOR SUPPLY VOLTAGES

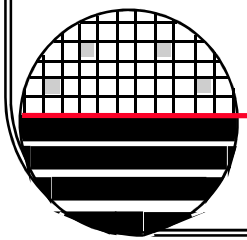
CLICK TO SELECT ONE

PMOS, Vcc = -10 Volts

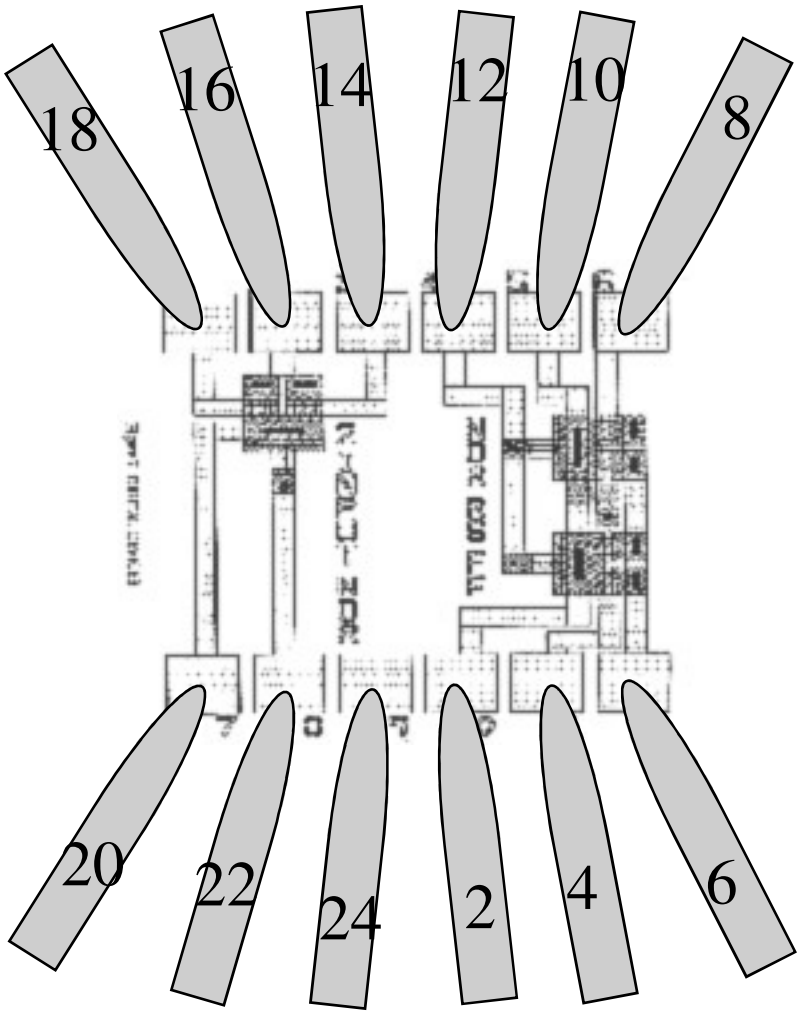
CMOS/TTL Vcc = +5 Volts

NMOS, Vcc = +10 Volts

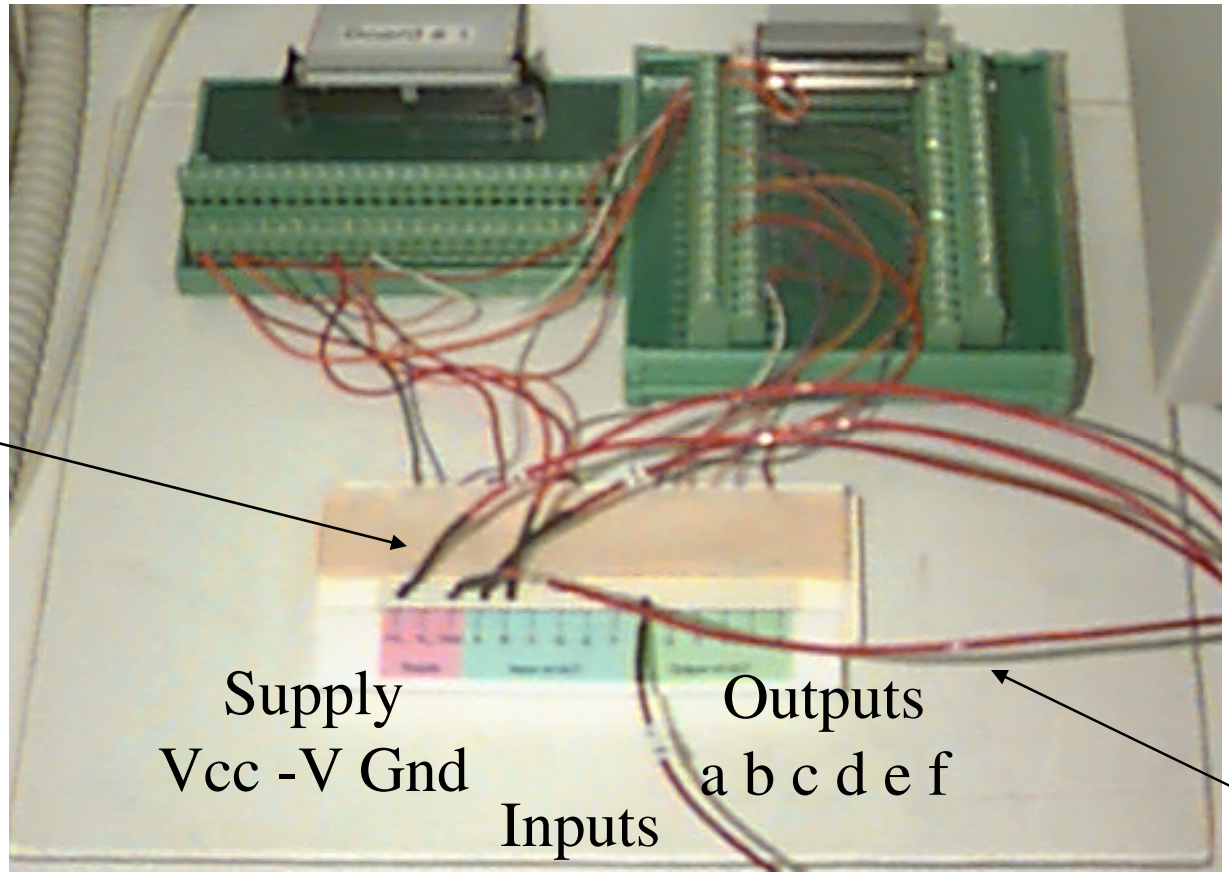
ANALOG, Vcc = +5 Volts, Vdd = -5 Volts



PROBE CARD/WIRE CONNECTIONS



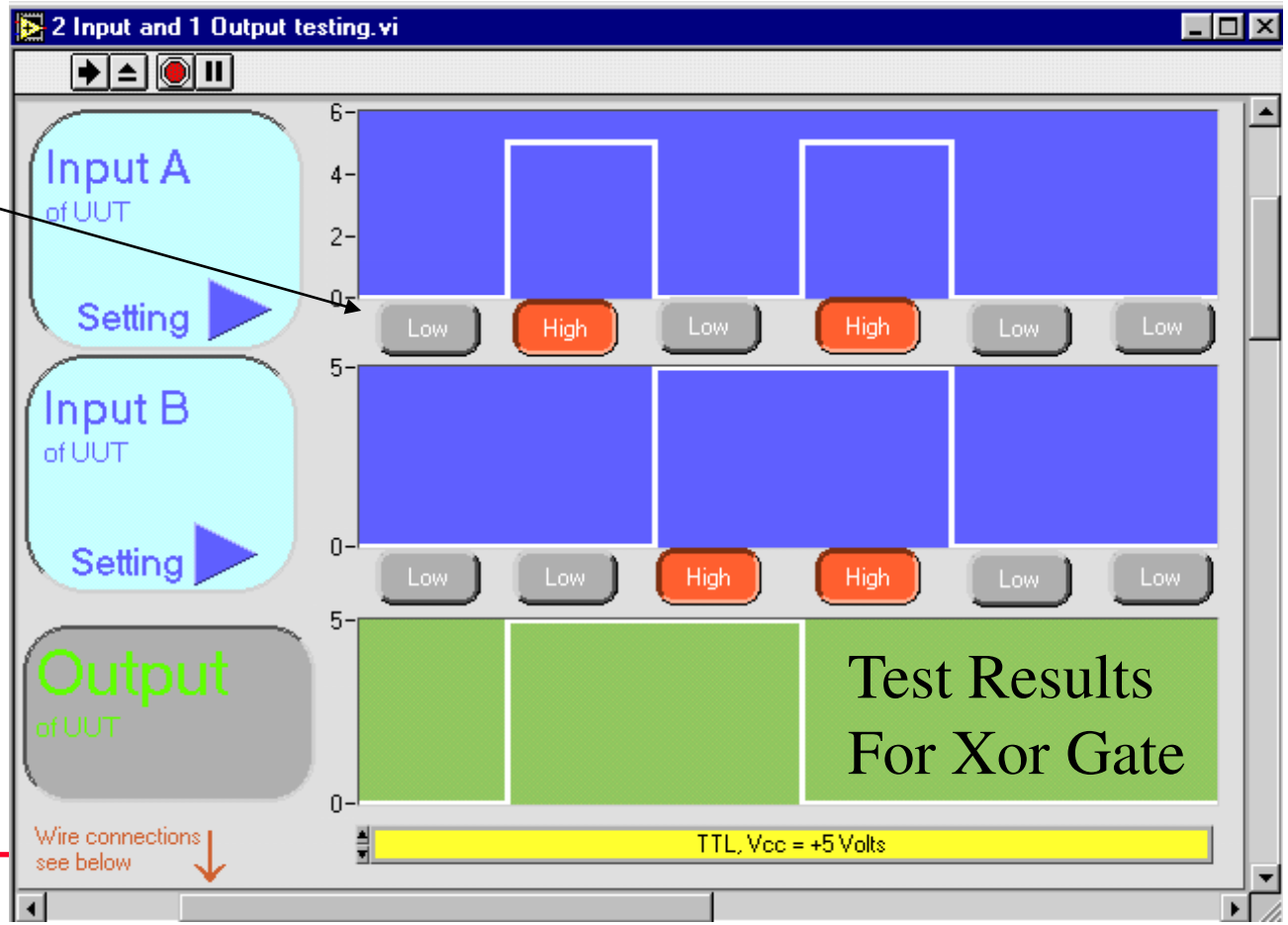
SWITCH MATRIX (MANUAL)



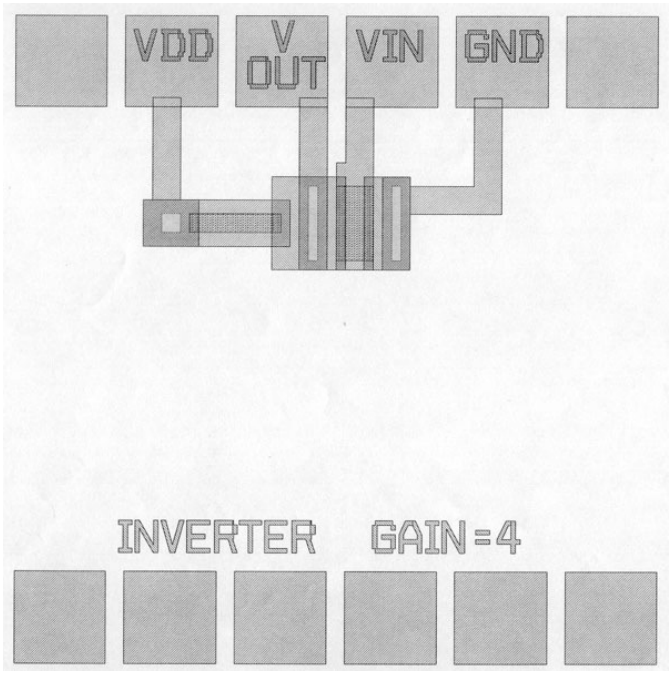
RUN TEST

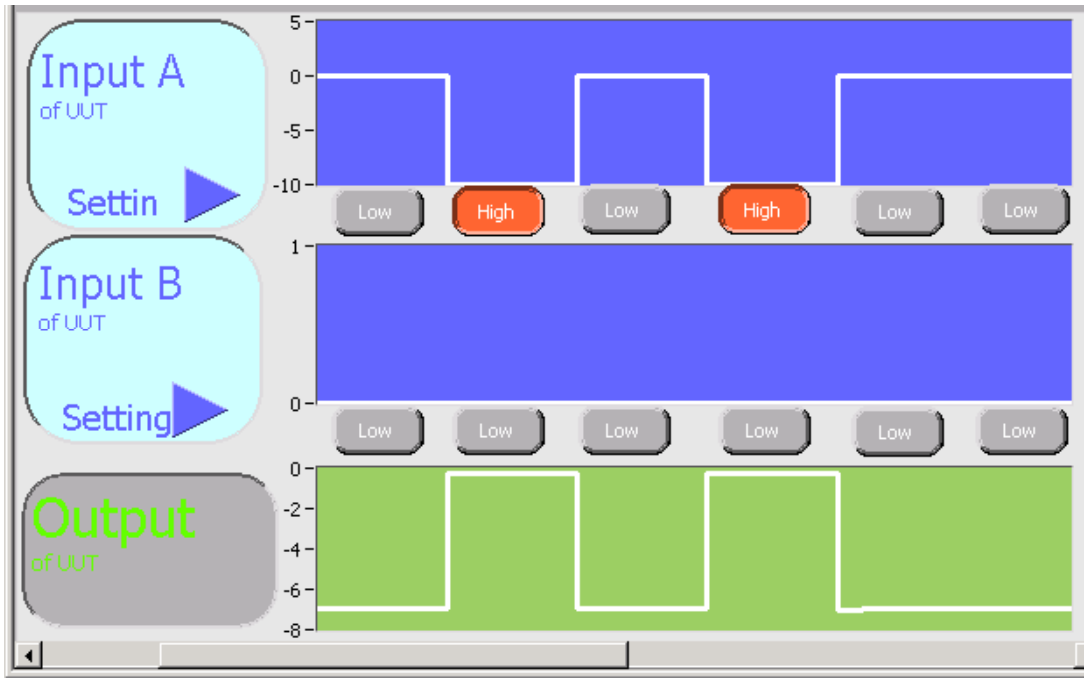
Click to Start Test
Stop Test

Click to Select When Output is High or Low

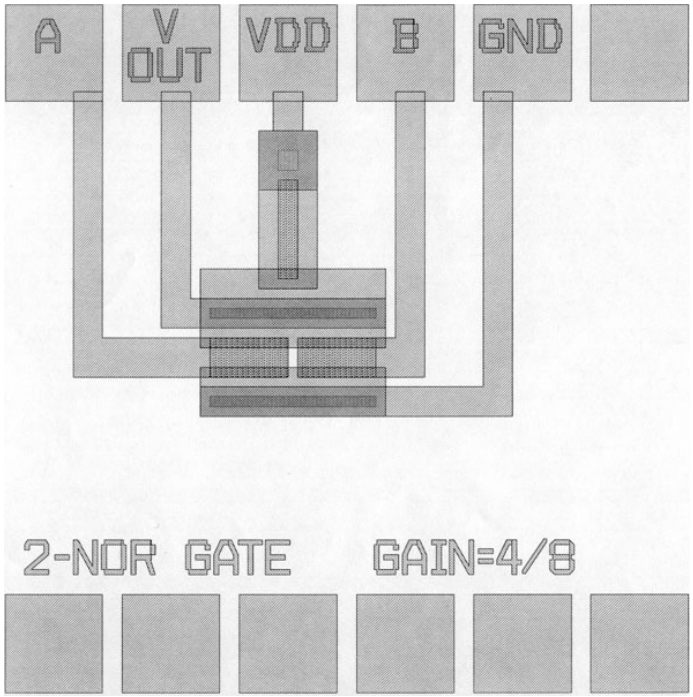


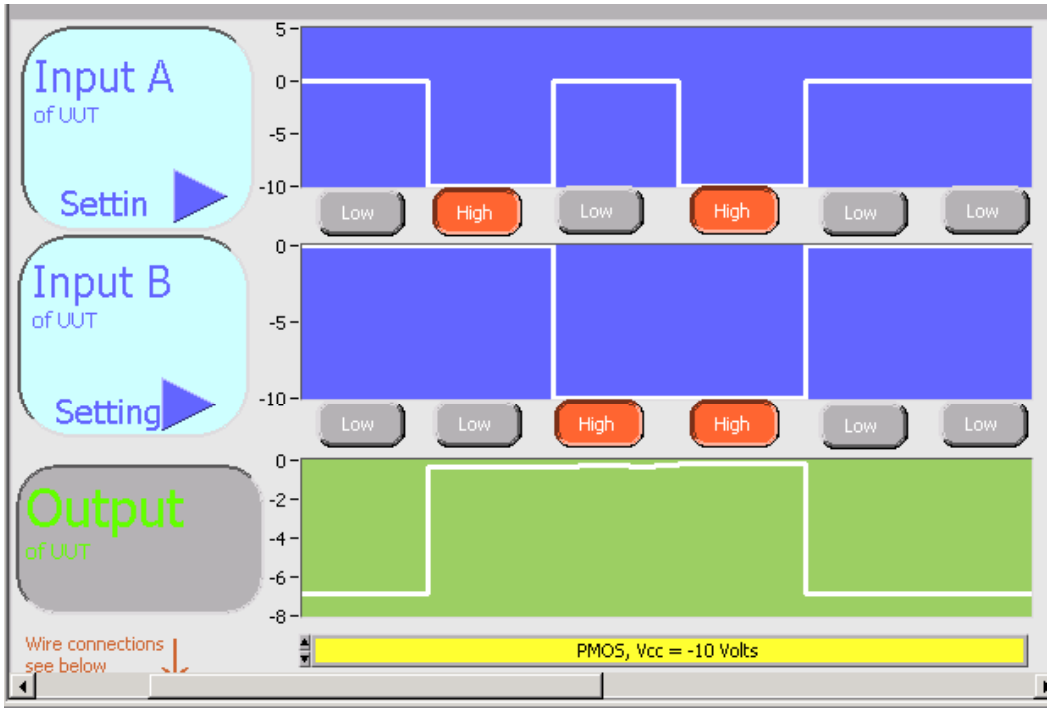
PMOS INVERTER GAIN=4





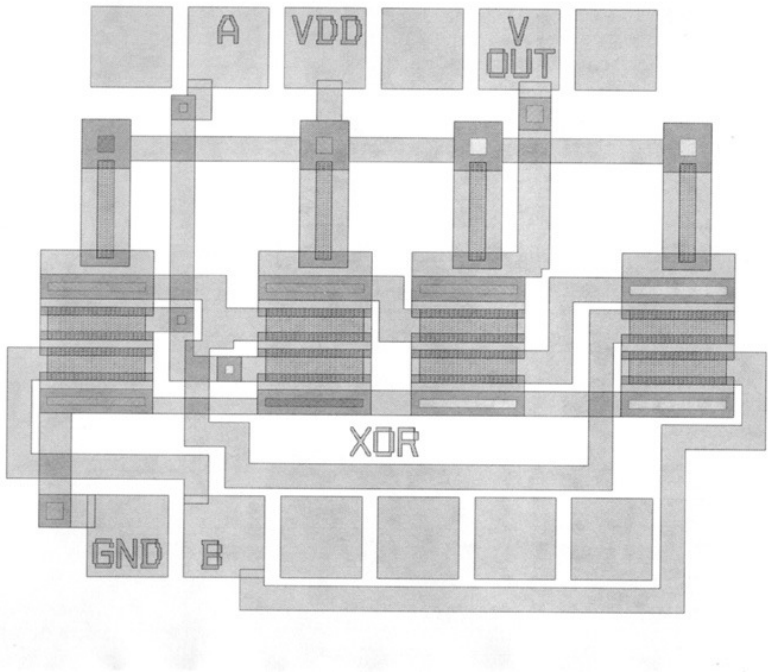
PMOS 2-INPUT NOR

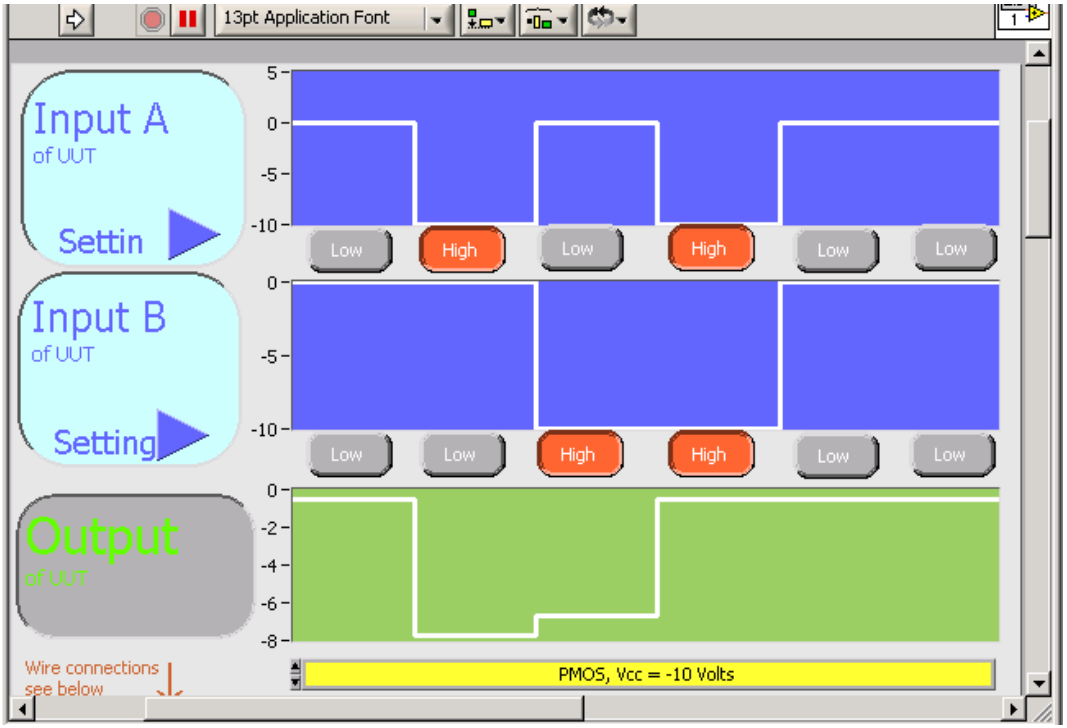




Test for PMOS Two Input NOR, Gain = 4 or 8

PMOS 2-INPUT XOR

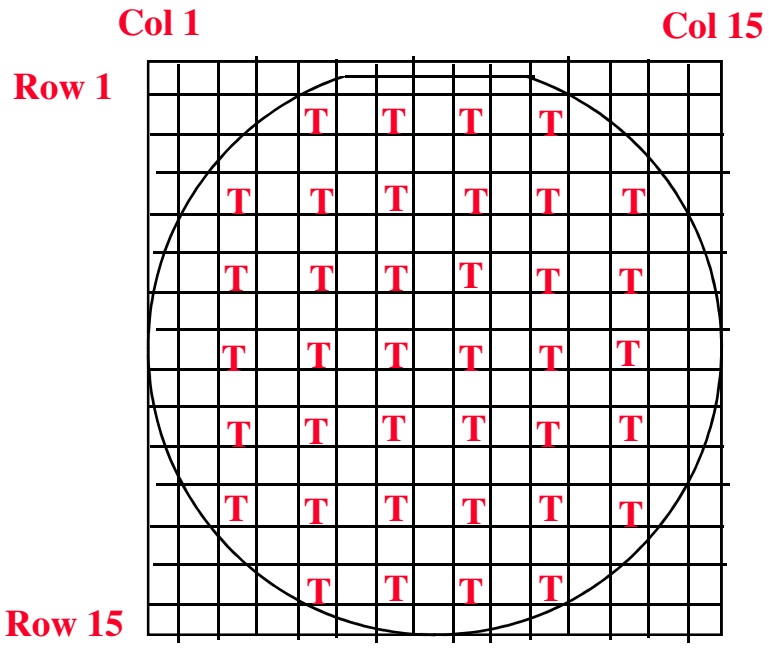




WAFER MAPS FOR MESA

nmos Vt target +1

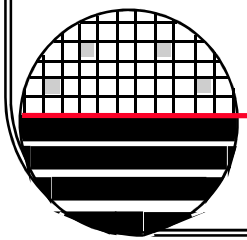
000000000000000
000050505050000
000000000000000
005060507050700
000000000000000
004040304030300
000000000000000
004040404040400
000000000000000
004050405090600
000000000000000
005050606060700
000000000000000
000050505050000
000000000000000



row 1 is the first row in which a full die is located
column 1 is the first column in which a full die is locatedd

WAFER MAPS FOR MESA

Code	
0	no die
1	value<(Target-40%)
2	(Target-40%)<value<(Target-30%)
3	(Target-30%)<value<(Target-20%)
4	(Target-20%)<value<(Target-10%)
5	(Target-10%)<value<(Target+10%)
6	(Target+10%)<value<(Target+20%)
7	(Target+20%)<value<(Target+30%)
8	(Target+30%)<value<(Target+40%)
9	(Target+40%)<value



WAFER MAP

Wafer Map Generator

Robert Manley, April 6, 2007

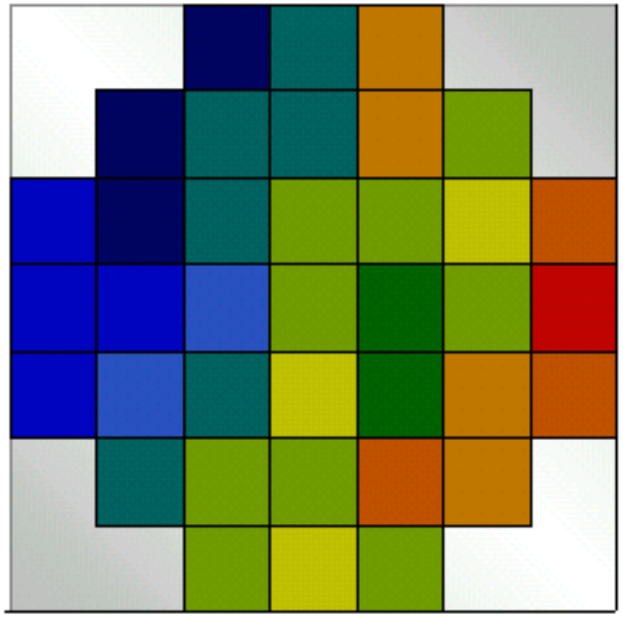
Die #	Enter Value
2	41.5743
3	45.3252
4	50.3482
7	41.5575
8	45.329
9	45.3527
10	50.3377
11	47.8361
13	42.7587
14	41.551
15	45.3116
16	47.8679
17	47.7949
18	49.103
19	51.5933
20	42.7823
21	42.7843
22	44.0555
23	47.8541
24	46.5718
25	47.8439
26	52.8681
27	42.8304
28	44.065
29	45.3343
30	49.1166
31	46.5419
32	50.3617
33	51.5929
36	45.3247
37	47.8316
38	47.8832
39	51.5937
40	50.3843
41	47.8326
42	49.0811

Map Physical Layout

	1	2	3	4	5	6	7
1			2	3	4		
2		7	8	9	10	11	
3	13	14	15	16	17	18	19
4	20	21	22	23	24	25	26
5	27	28	29	30	31	32	33
6		35	36	37	38	39	
7			42	43	44		

Max	52.8681
Min	41.551
Range	11.3171
# Inc.	11
Inc. Size	1.02883

Wafer Flat

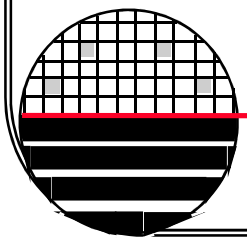


52.87	to	51.84
51.84	to	50.81
50.81	to	49.78
49.78	to	48.75
48.75	to	47.72
47.72	to	46.70
46.70	to	45.67
45.67	to	44.64
44.64	to	43.61
43.61	to	42.58
42.58	to	41.55

Example: Given a wafer with test chips located as shown and nmos threshold voltage data encoded and stored in MESA as shown. Reconstruct a wafer map using EXCELL spreadsheet.

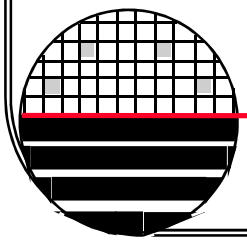
FUTURE WORK

- **More Automation**
- **Improved Wafer Mapping**
- **More Complete Testing**



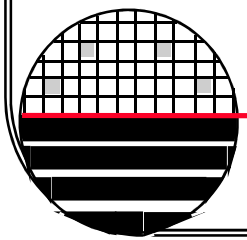
CONCLUSION

- **A test specification has been developed**
- **A history data base has been developed**
- **Testing is very time consuming. It takes us 9 hours to do all the specified tests and even then we only test a few devices on a wafer.**
- **Currently we test about 1% of the devices**



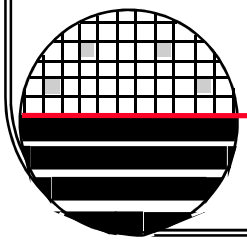
REFERENCES

1. LabView Software, National Instruments,
http://www.natinst.com

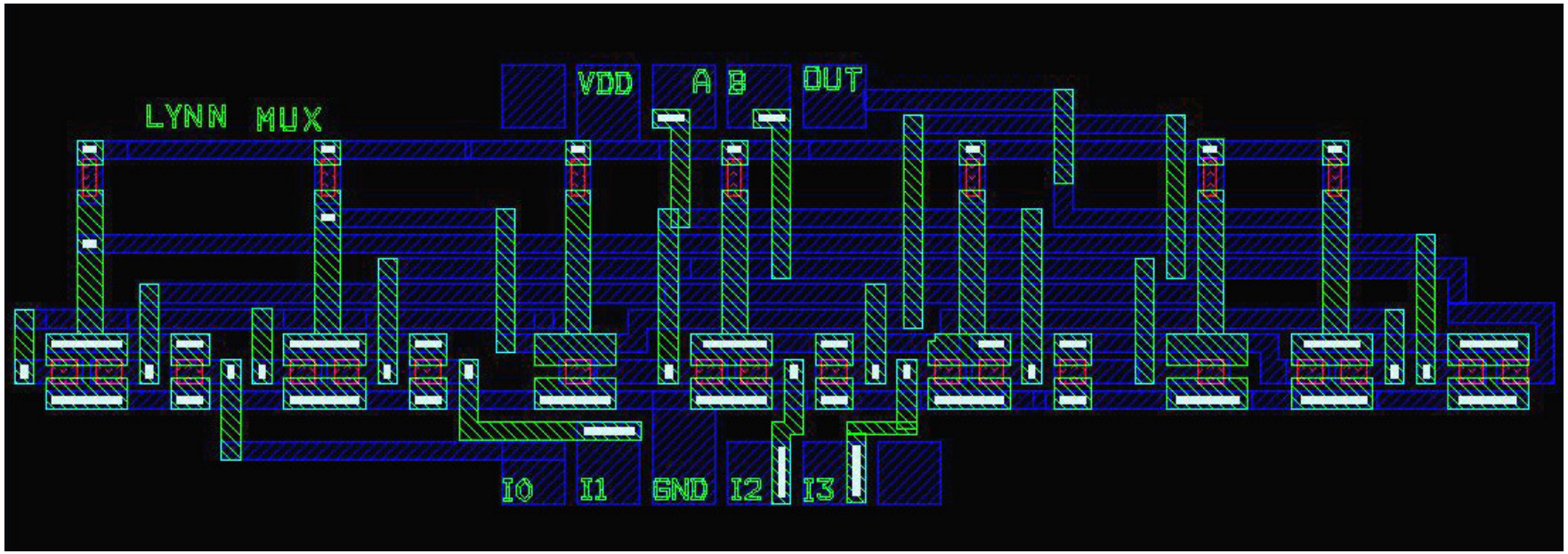


REVIEW QUESTIONS - PMOS TEST SPECIFICATION

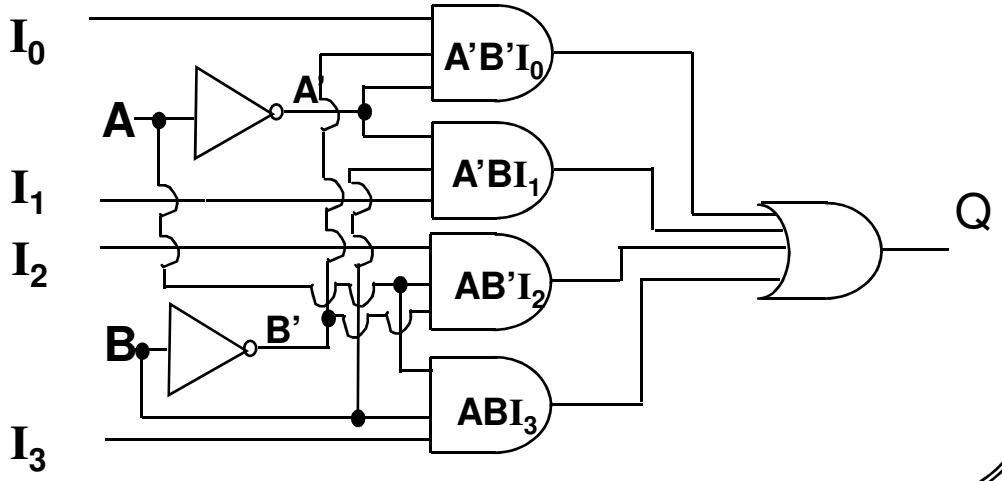
1. How is Vt and gm found from the transistor family of curves.
2. Is the Vt and gm the same in the non-saturation region as in the saturation region?
3. What is the significance of the sub-threshold slope. What is the difference between sub-threshold slope and sub-threshold swing?
4. What is the significance of the noise margin.
5. What is the purpose of the ring oscillator test structure.



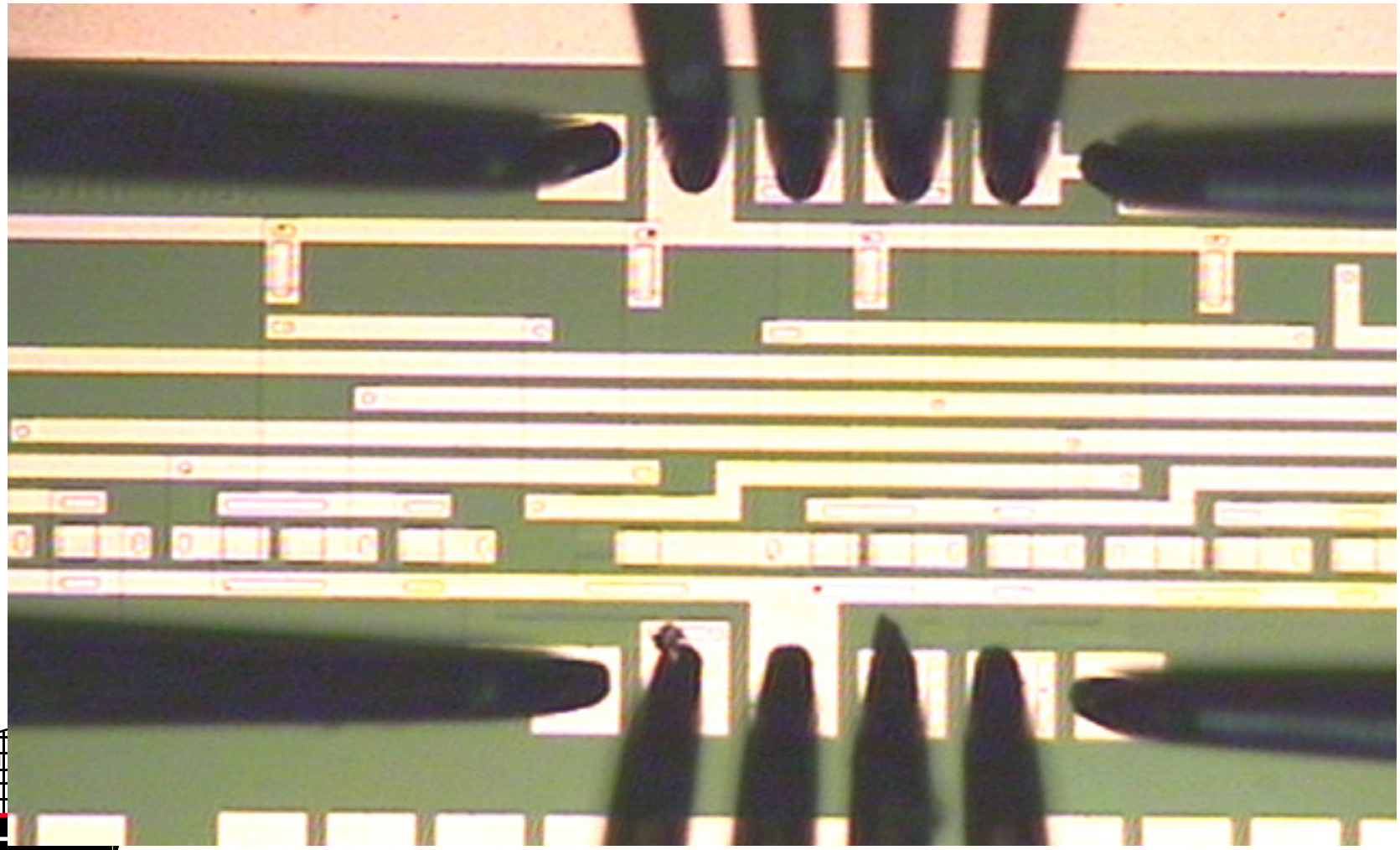
MUX LAYOUT AND GATE LEVEL SCHEMATIC



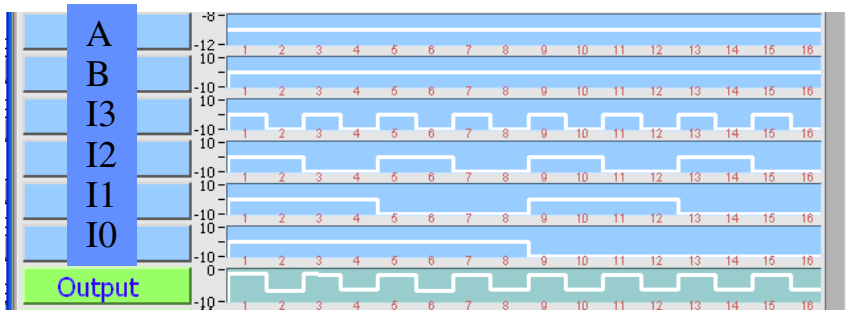
25 Transistors

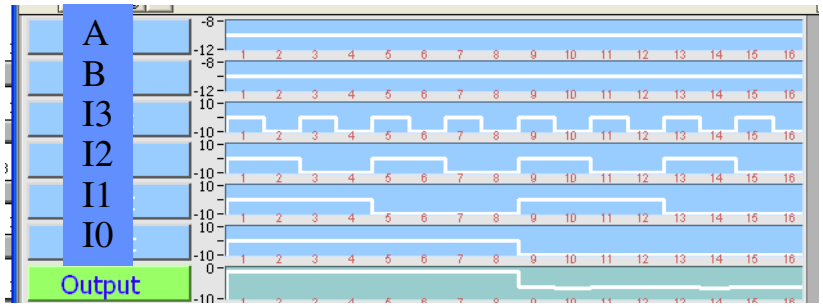


PMOS 4-INPUT MULTIPLEXER

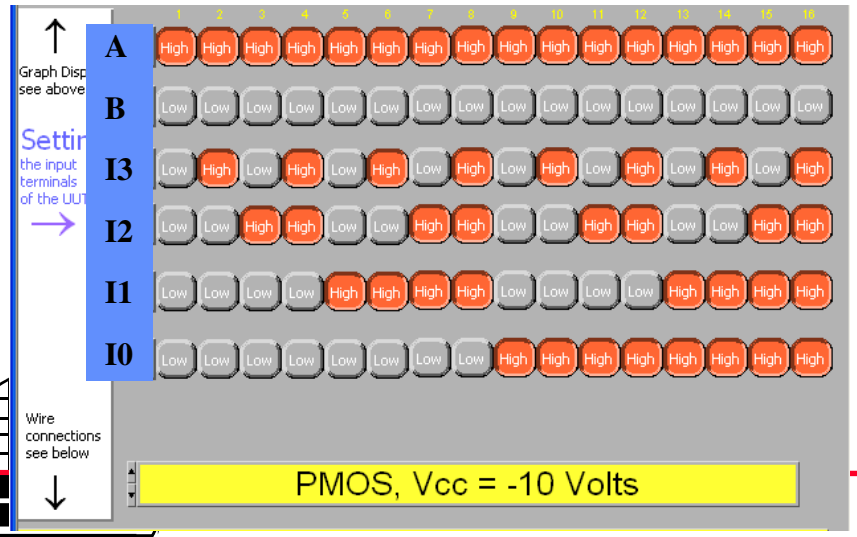


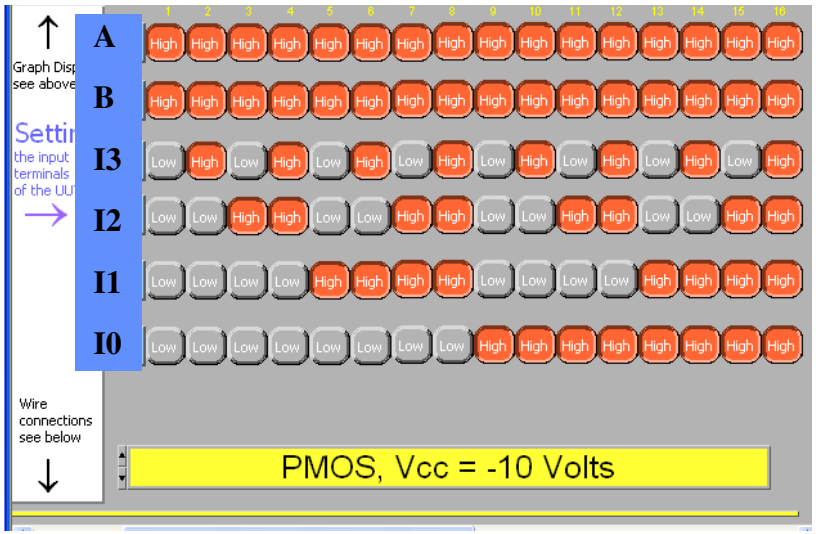
MUX TEST RESULTS



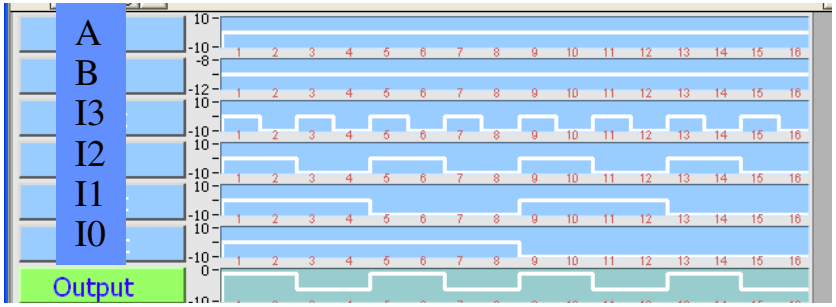


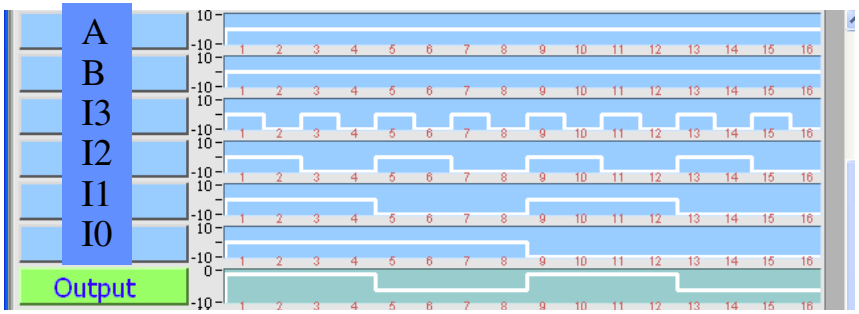
In PMOS logic low is 0 volts, logic high is -Vcc



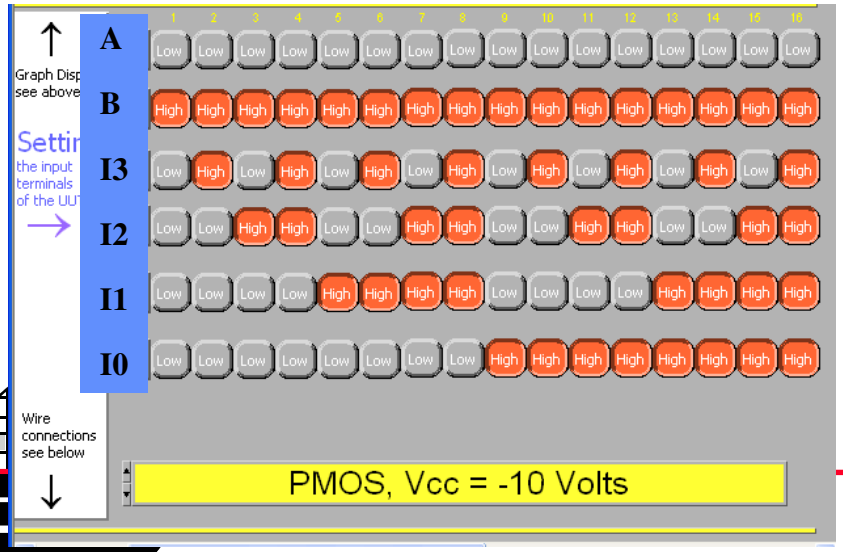


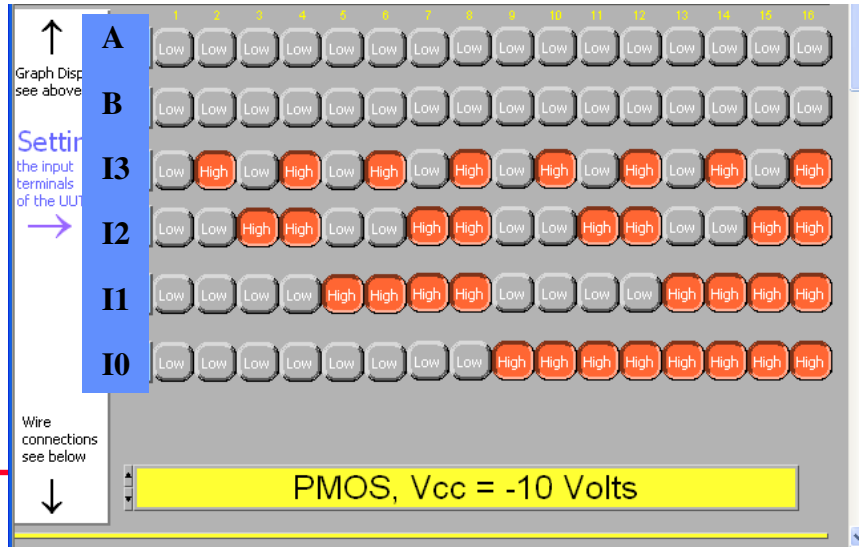
MUX TEST RESULTS



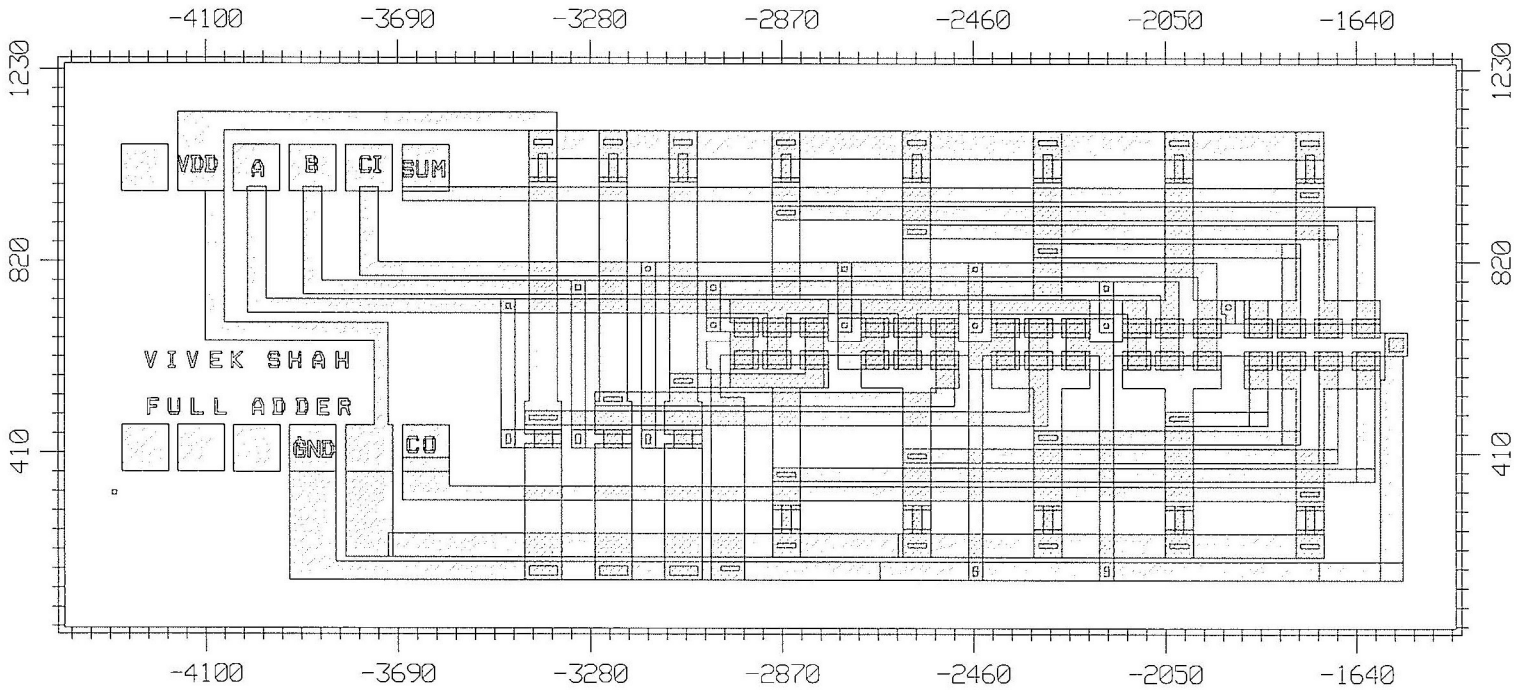


In PMOS logic low is 0 volts, logic high is -Vcc

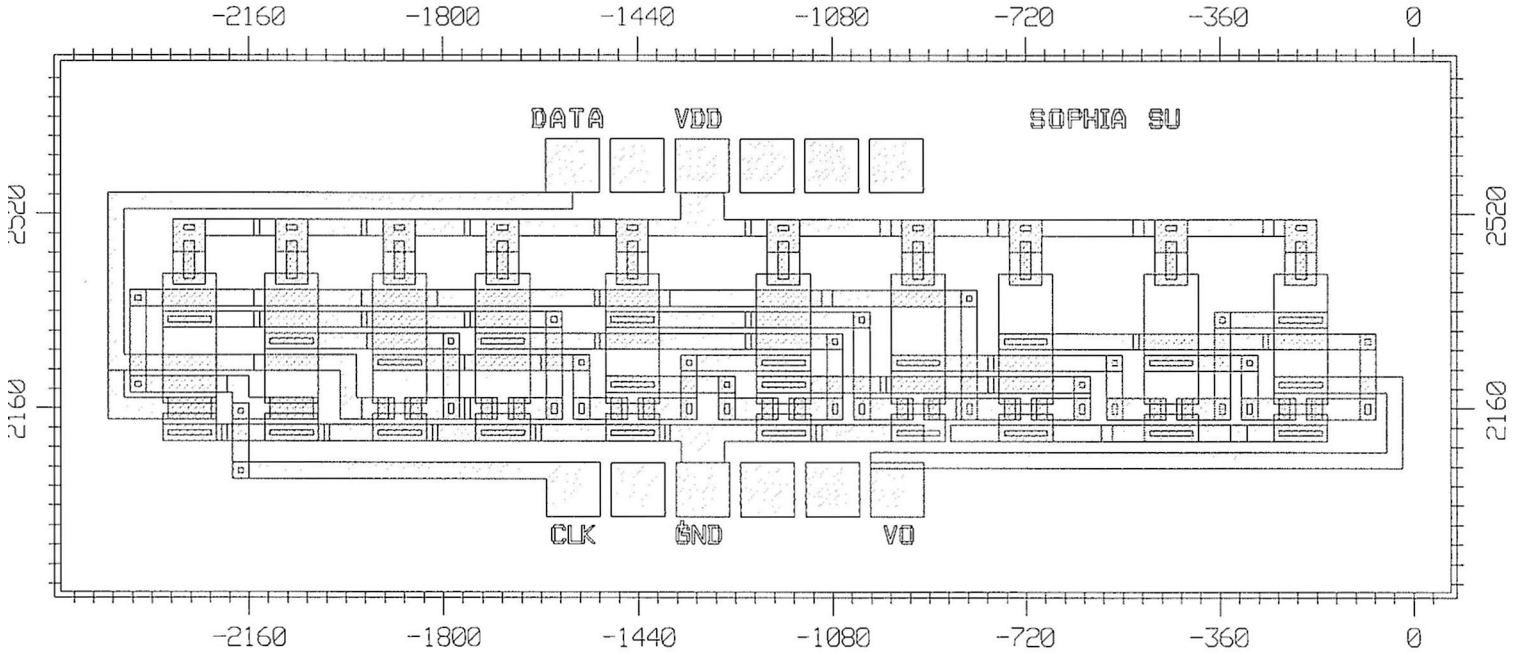




PMOS FULL ADDER



PMOS CLOCKED DATA LATCH



PMOS ANALOG MUX