Power Conditioning Electronics

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OUTLINE

Introduction
Power Conditioning
Voltage Regulators
Analog Switches
Two Phase Clocks
Voltage Inverters, Doublers, Tripler's

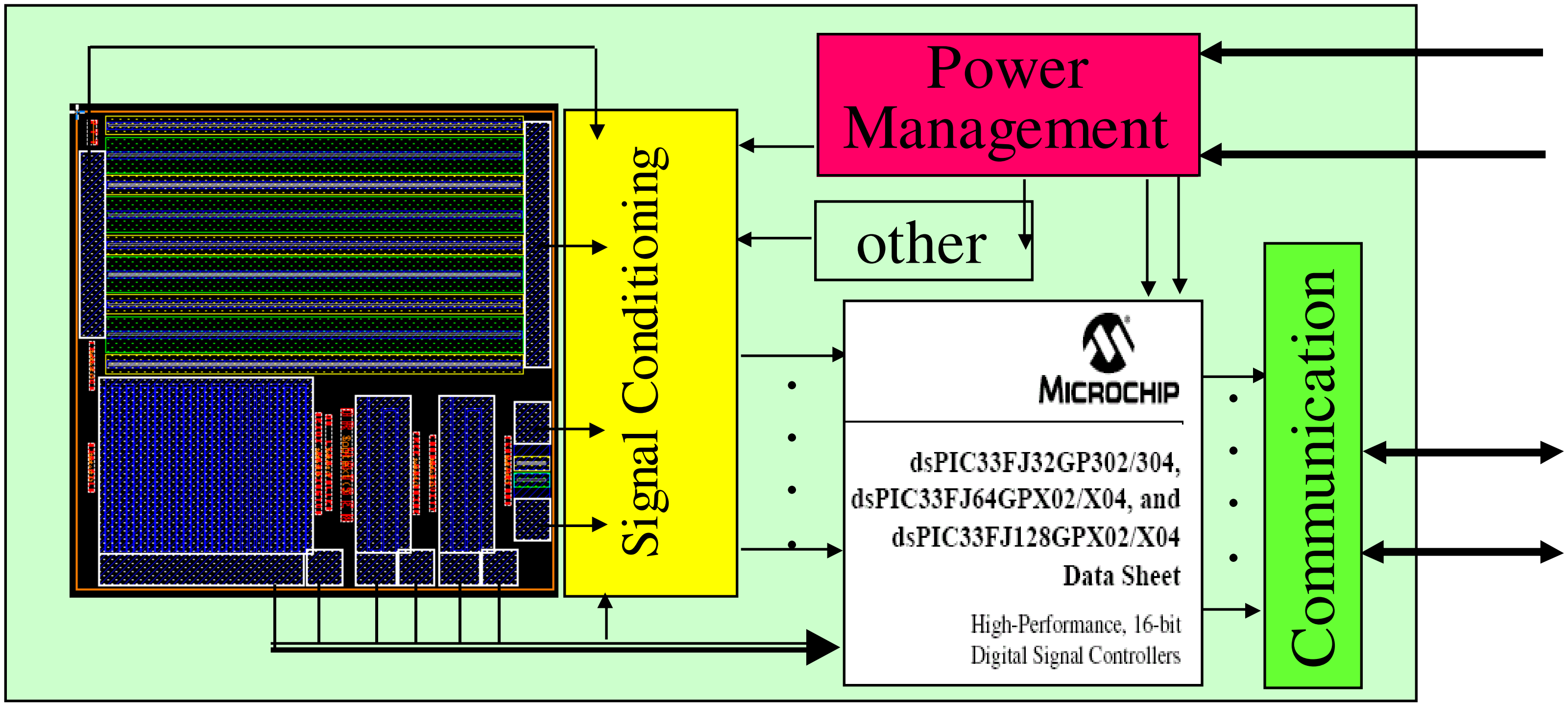
INTRODUCTION

The design of microsystems involves the integration of MEMS, on chip custom integrated circuits, off chip electronics, such as power supply chips, microcontrollers and communication components. The integration is often done at the printed circuit board (PCB) level.

This document will look at the power management electronics used in these systems.

MICROSYSTEM

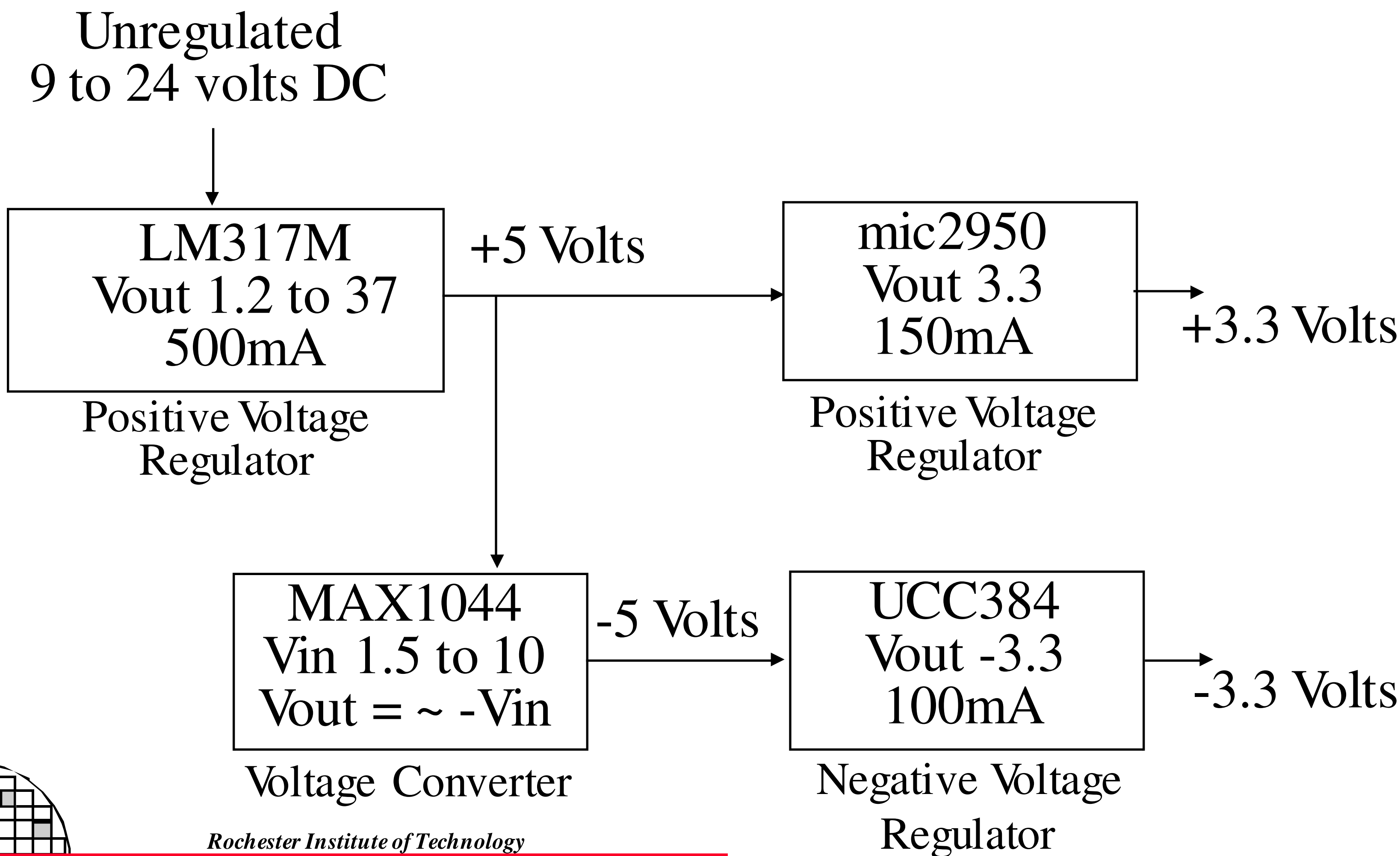
Multi-Sensor MEMs Chip



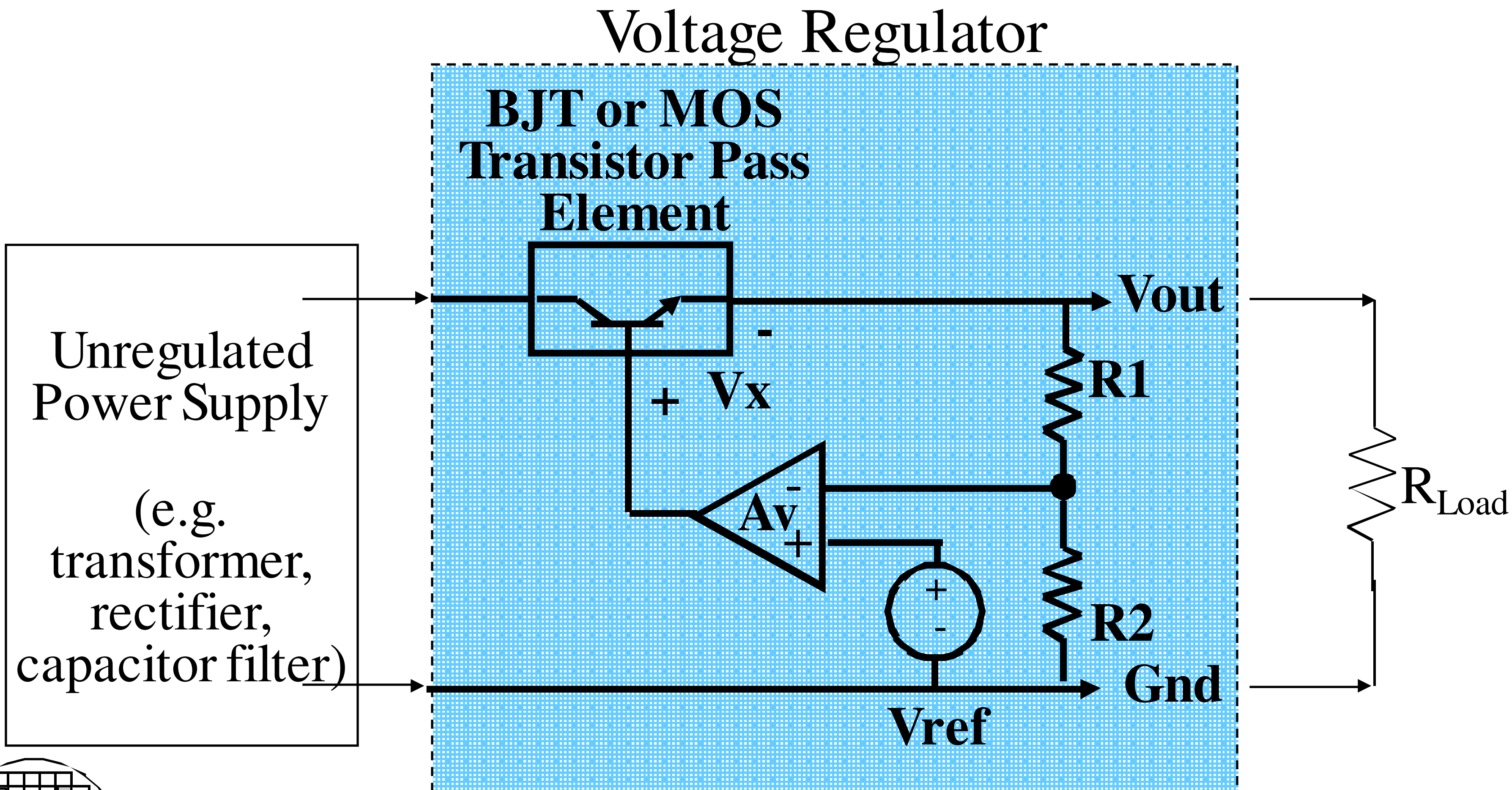
Micro Controller

Signal Conditioning
Electronics

POWER CONDITIONING EXAMPLE



BASIC VOLTAGE REGULATOR

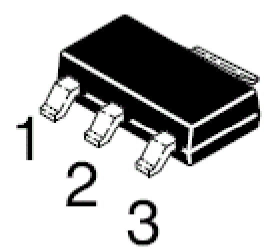


$$Vout = Vref(1+R1/R2)$$

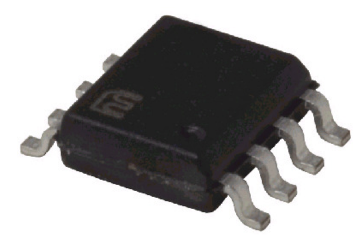
POWER SUPPLY COMPONENTS

Description	**Digikey Part Number**	**Package**	**~Price**
POS Lin Regulator Variable	LM317MBSTT3GOS CT-ND	SOT-223	\$0.72
POS Lin Regulator 3.3 Volt	576-1151-ND	8-SOIC	\$1.11
Voltage Converter CMOS SW-CAP	MAX1044CPA+-ND	8-DIP	\$2.68
Voltage Converter CMOS SW-CAP	MAX1044CSA+-ND	8-SOIC	\$3.26
NEG Lin Regulator	296-11417-5-ND	8-SOIC	\$5.60

8-DIP

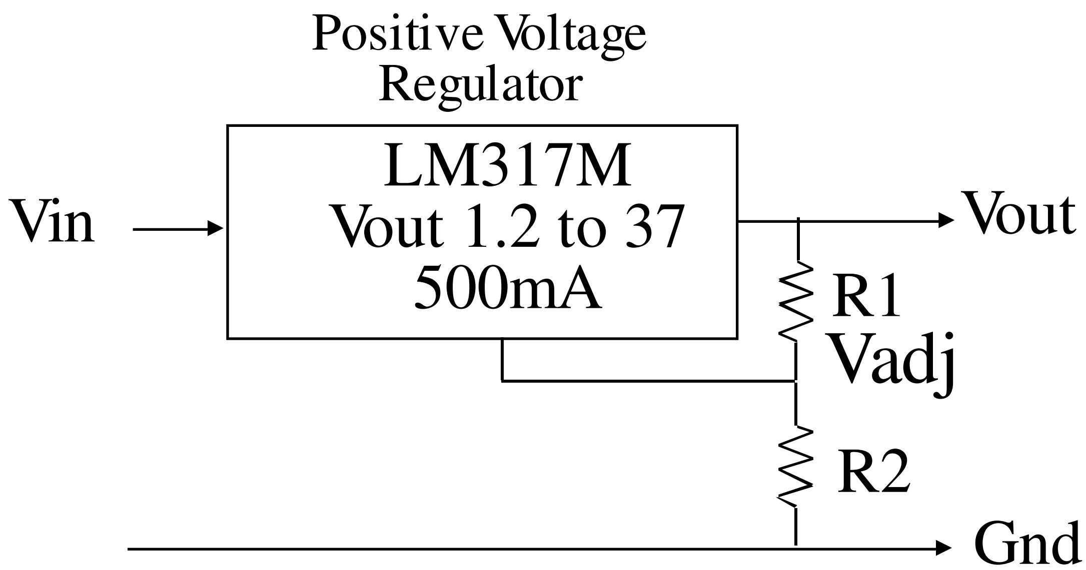


SOT-223



8-SOIC

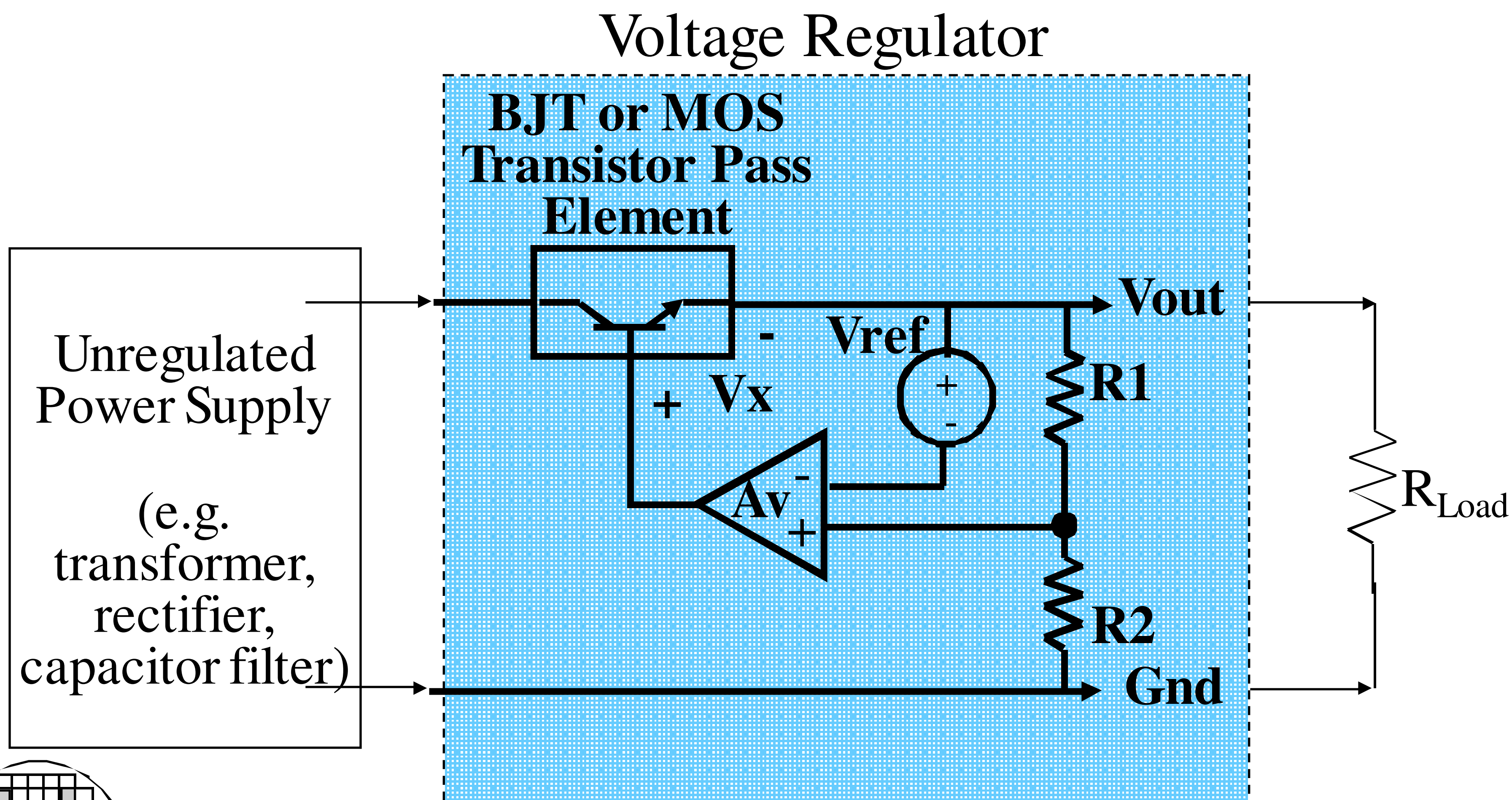
VOLTAGE REGULATOR



$$Vout = 1.25(1+R2/R1)$$

Note: see data sheets for LM317M-D.pdf
the reference is between Vout and Vadj
not between Vadj and ground.

VOLTAGE REGULATOR (Vref to Vout not to ground)



Vout = Vref(1+R2/R1)

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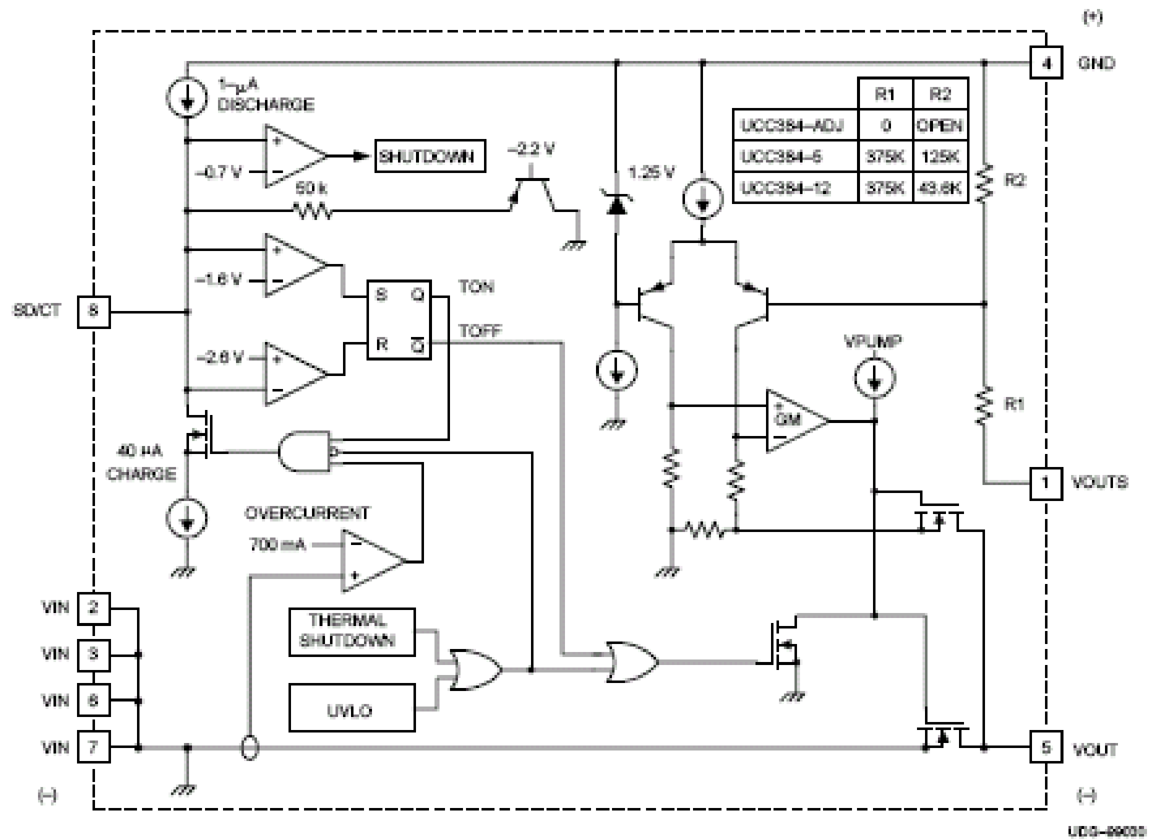
NEGATIVE VOLTAGE REGULATOR

UCC284–5, UCC284–12, UCC284–ADJ, UCC384–5, UCC384–12, UCC384–ADJ
LOW-DROPOUT 0.5-A NEGATIVE LINEAR REGULATOR

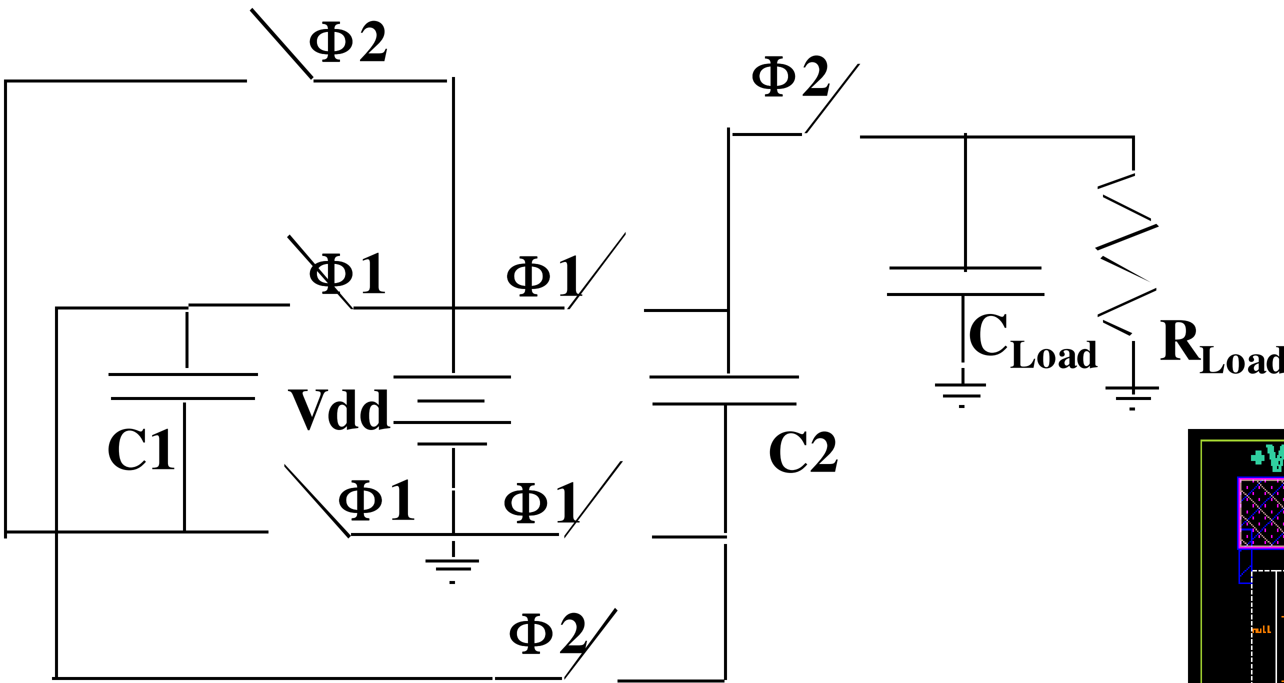
SLUS234D – JANUARY 2000 – REVISED FEBRUARY 2002

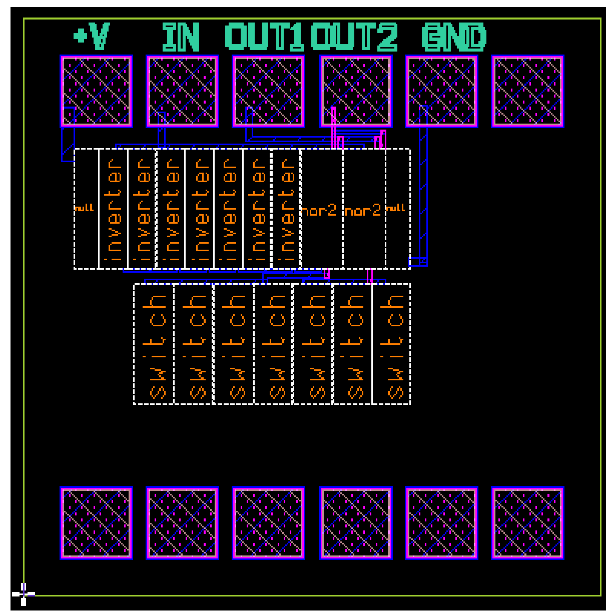
$$Vout = Vref(1+R1/R2)$$

functional block diagram



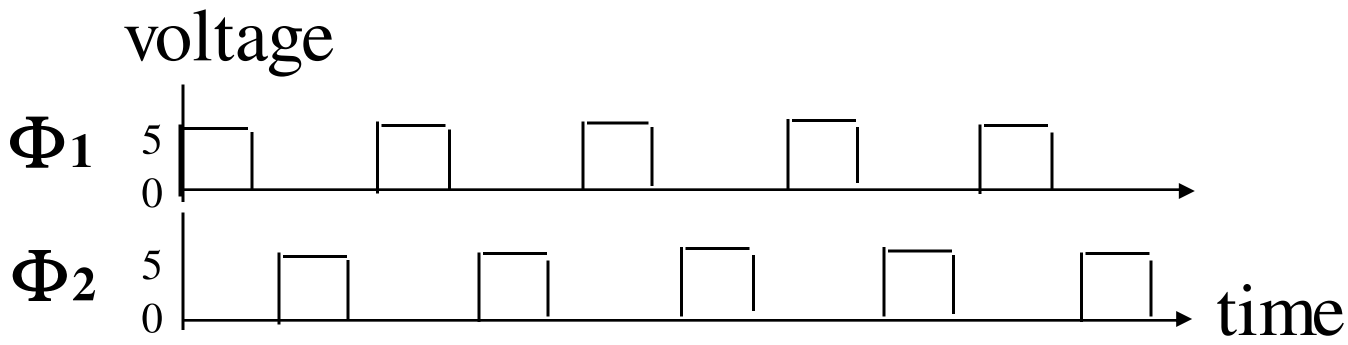
SWITCHED CAPACITOR VOLTAGE TRIPLER



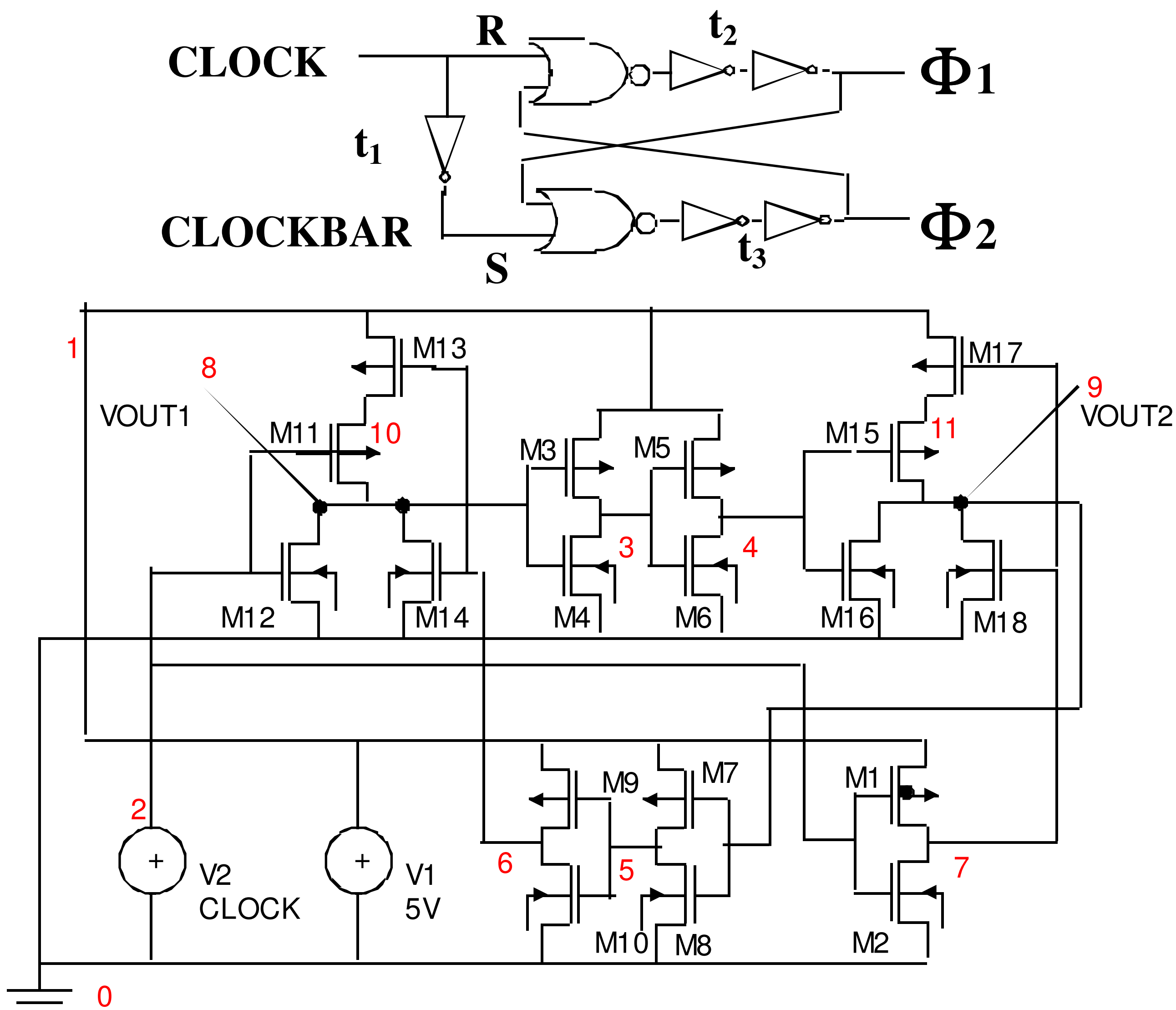


When ϕ1 is high switches put C1 and C2 in parallel with Vdd. When ϕ2 is high switches put C1, C2 and Vdd in series, tripling the voltage to the load.

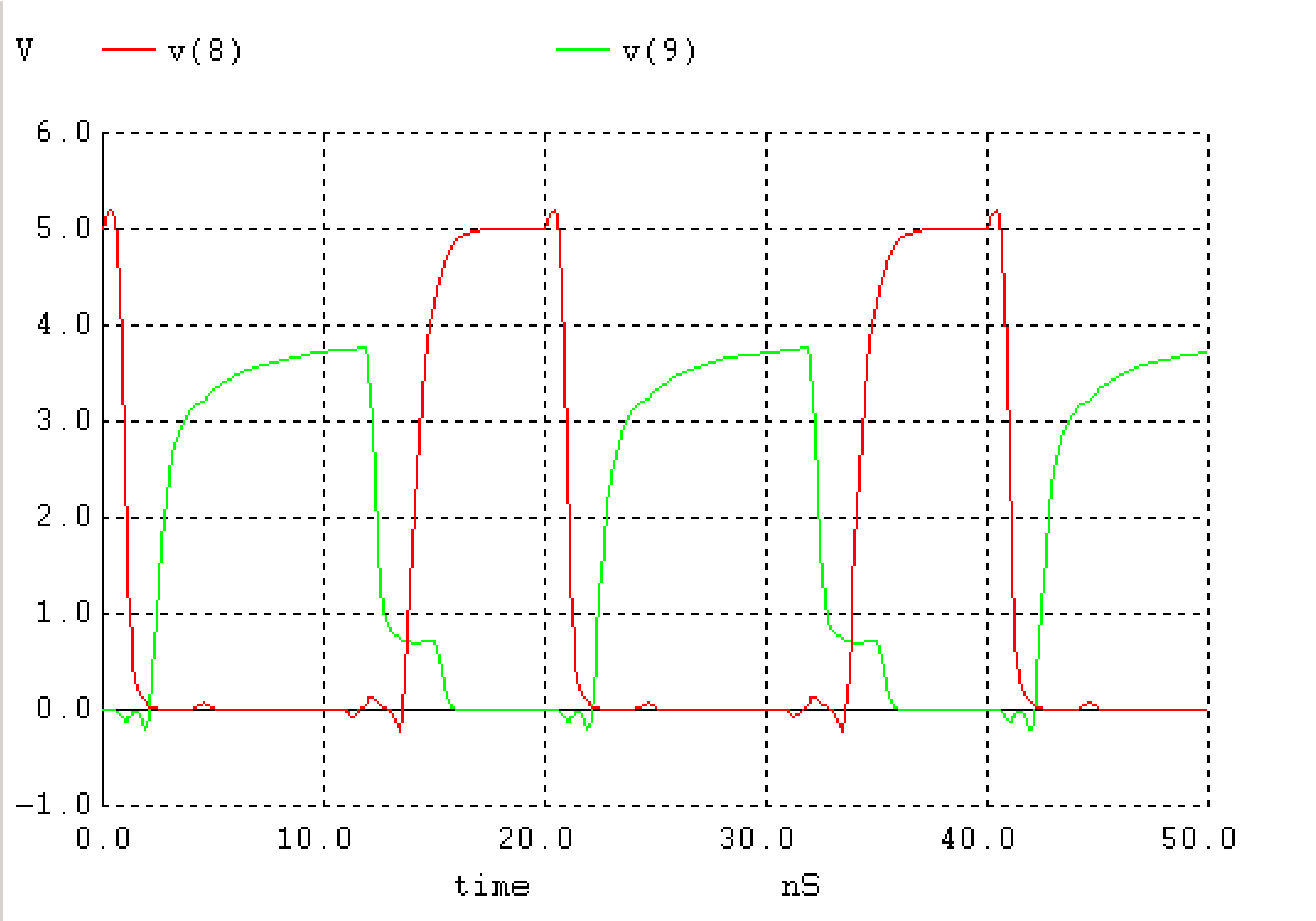
TWO PHASE NON OVERLAPPING CLOCK



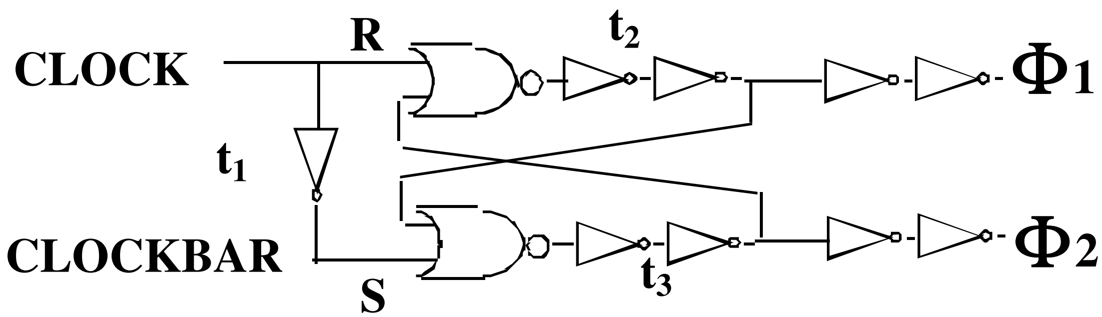
VERSION 2 OF TWO PHASE NON OVERLAPPING CLOCK

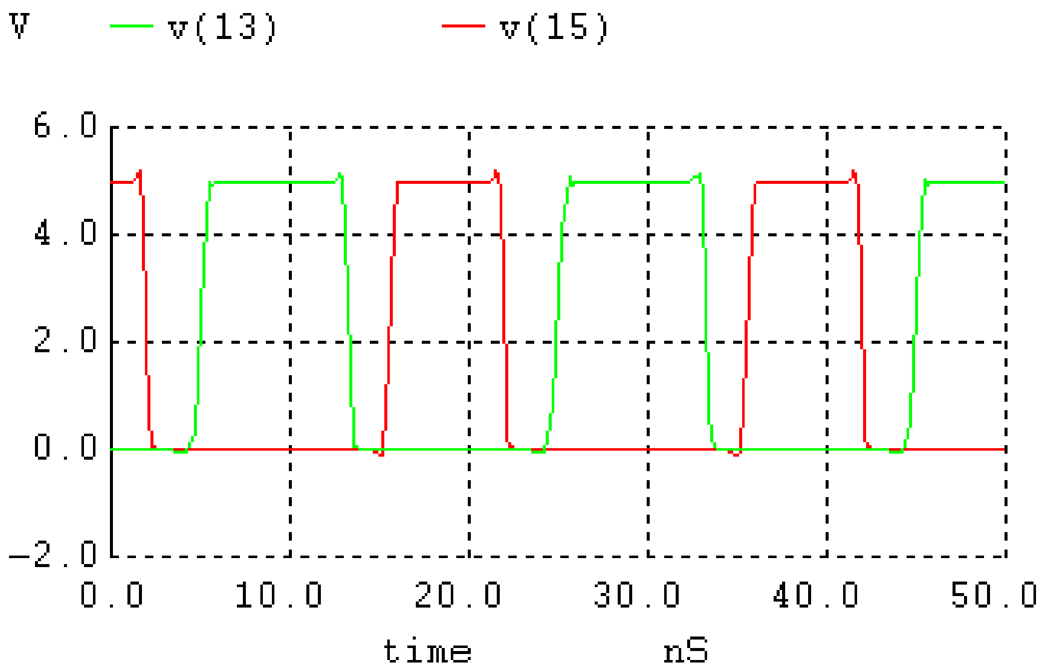


WINSPICE SIMULATION FOR VERSION TWO

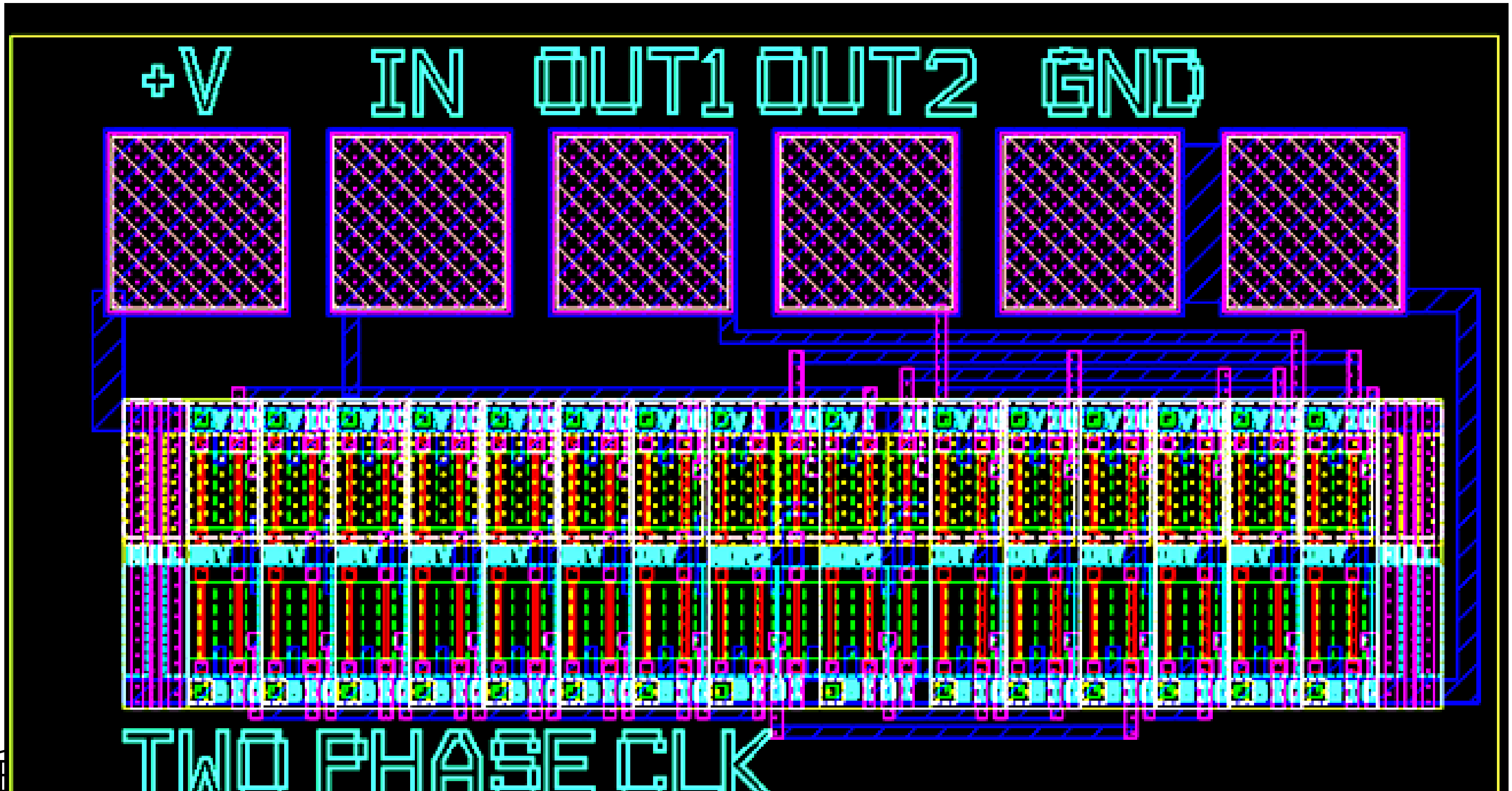


WINSPICE SIMULATION FOR VERSION TWO + BUFFERS

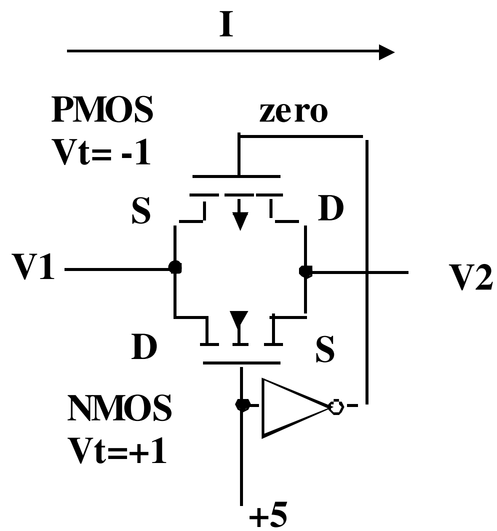




LAYOUT FOR TWO PHASE CLOCK

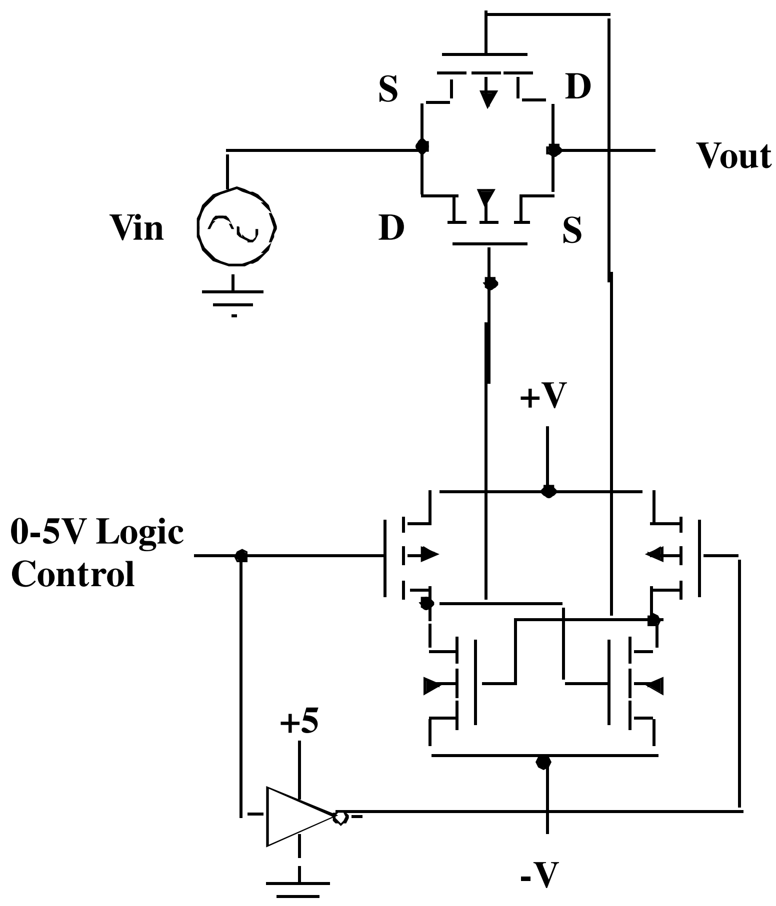


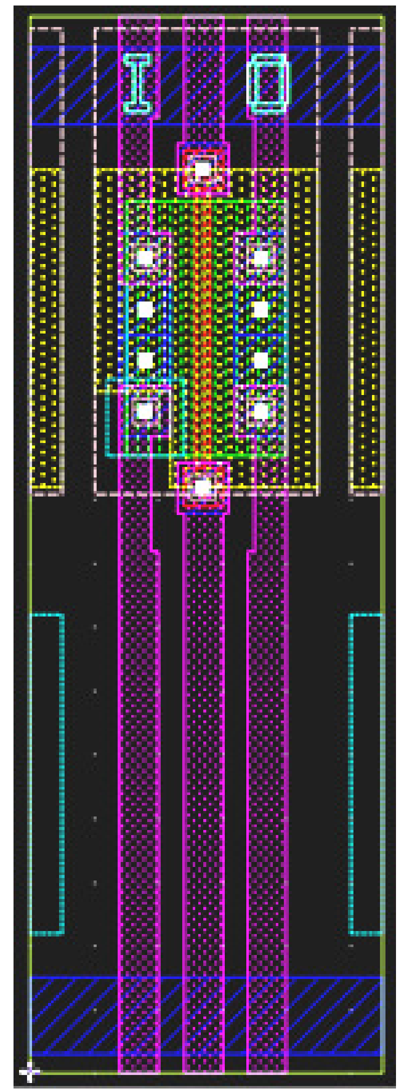
ANALOG SWITCHES



For current flowing to the right (ie V1>V2) the PMOS transistor will be on if V1 is greater than the threshold voltage, the NMOS transistor will be on if V2 is <4 volts. If we are chargeing up a capacitor load at node 2 to 5 volts, initially current will flow through NMOS and PMOS but once V2 gets above 4 volts the NMOS will be off. If we are trying to charge up V2 to V1 = +1 volt the PMOS will never be on. A complementary situation occurs for current flow to the left. Single transistor switches can be used if we are sure the Vgs will be more than the threshold voltage for the specific circuit application. (or use larger voltages on the gates)

(+V to -V) ANALOG SWITCH WITH (0 to 5 V) CONTROL

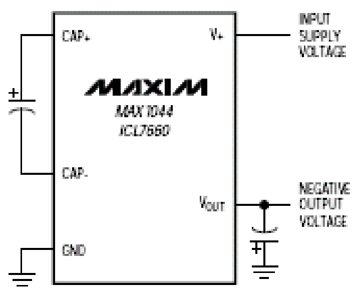




SWITCHED CAPACITOR VOLTAGE CONVERTER

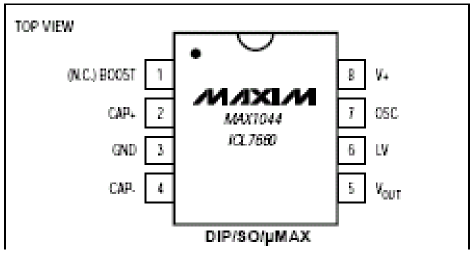
Portable Telephones
Op-Amp Power Supplies
EIA/TIA-232E and EIA/TIA-562 Power Supplies
Data-Acquisition Systems
Hand-Held Instruments
Panel Meters

Typical Operating Circuit



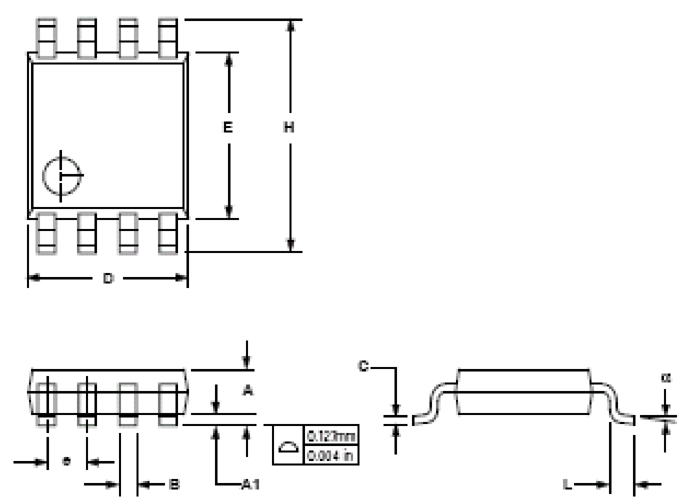
NEGATIVE VOLTAGE CONVERTER

Pin Configurations



MAX1044CSA+-ND
CMOS
1.5 to10 Volt Supply

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
E	0.116	0.120	2.95	3.05
e	0.0256		0.65	
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

21-0036

8-PIN μMAX PACKAGE

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MAX1044 VOLTAGE CONVERTER

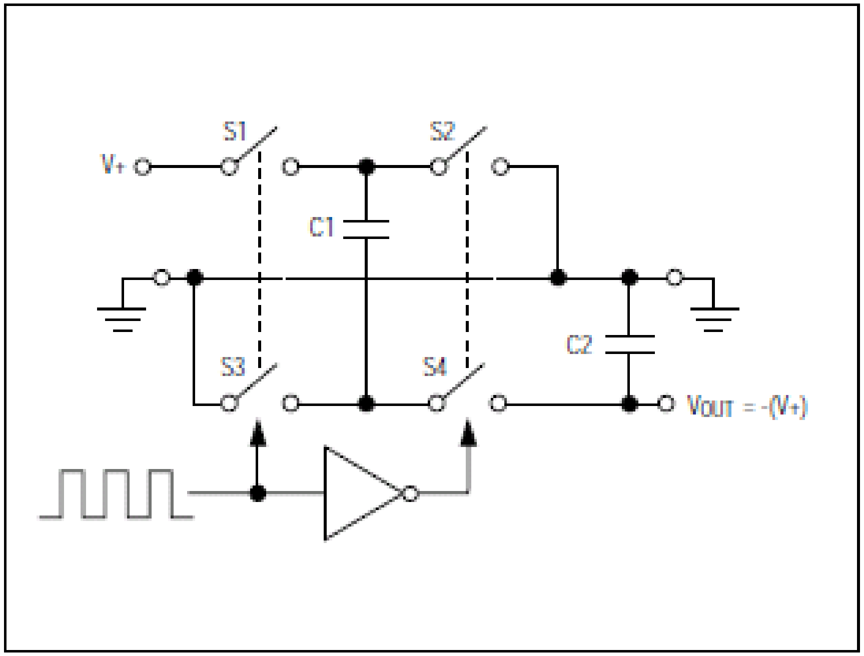

Figure 2. Ideal Voltage Inverter

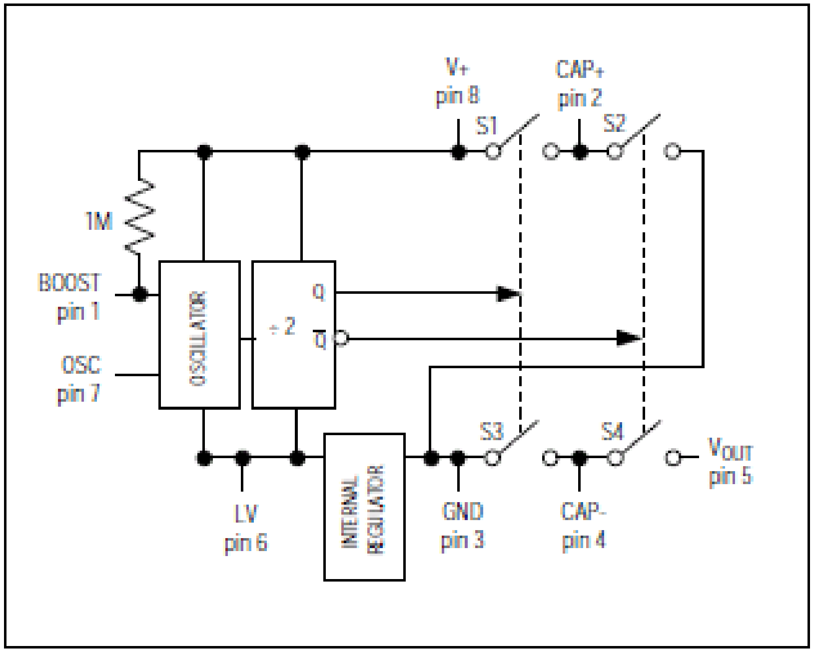

Figure 4. MAX1044 and ICL7660 Functional Diagram

REFERENCES

1. Dr. Fullers webpage http://people.rit.edu/lffeee

HOMEWORK – POWER CONDITIONING

1. Sketch a schematic showing battery, switches and capacitors of the positive-to-negative switched capacitor voltage converter.

2. Design a 6 volt regulator using a 741 op amp and a BJT transistor.

3. Do a SPICE simulation of the two phase clock version two with buffers shown in these lecture notes.