ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

2D Process Modeling with Silvaco ATHENA

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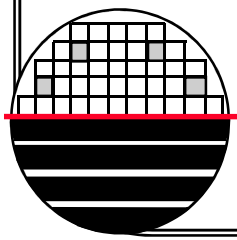

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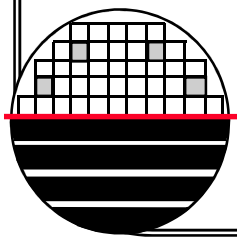
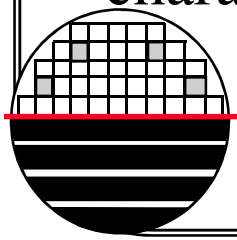


INTRODUCTION

SUPREM – **S**tanford **U**niversity **PR**ocess **E**ngineering **M**odule, 1977

ATHENA is Silvaco, Inc's. version of SUPREM. ATHENA is normally used in conjunction with VWF Interactive tools. These include DECKBUILD, TONYPLOT,DEVEDIT, MASKVIEWS and OPTIMIZER. DECKBUILD provides an interactive run time environment. TONYPLOT supplies scientific visualization capabilities. DEVEDIT is an interactive tool for structure and mesh specification and refinement, and MASKLVIEWS is an IC Layout Editor. The OPTIMIZER supports black box optimizations across multiple simulators. ATHENA is frequently used in conjunction with ATLAS device simulator. ATHENA predicts the physical structure that result from processing. These physical structures are used as input by ATLAS, which then predicts the electrical characteristics associated with specified bias conditions.

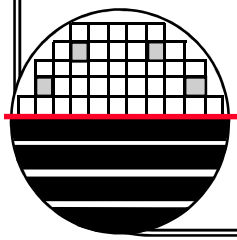


TIPS AND PRINTING TONYPLOT

Tips: The software runs on a UNIX computer. The commands are case sensitive. The pull down menus are often enabled with a right mouse click (RMC) and then the desired selection is made with a left mouse click (LMC).

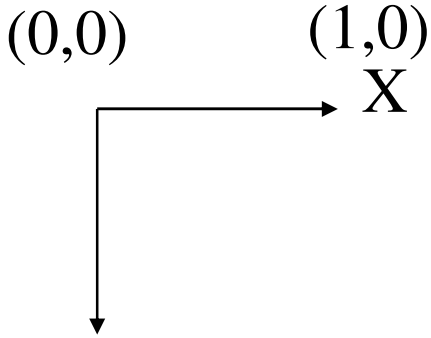
Example: once you run ATHENA you most often generate a graph of the results using the software TONYPLOT. To print the plot you need to do the following:

Pull down Print on the top banner (right mouse click, RMC)
Select Printers (left mouse click, LMC)
Pull down Queue (right mouse click, RMC)
Select prec2 (left mouse click, LMC)
Update
Save Set Up (click on icon at bottom right)
Pull down Print on top banner (RMC)
Select Print view (LMC)



GETTING STARTED

To get started you need to invoke the DECKBUILD application. DECKBUILD will allow you to specify the process steps you want to analyze.

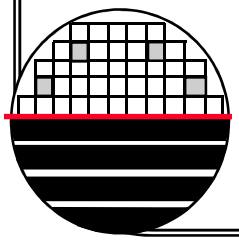


Open terminal window (shell)
Type **deckbuild**

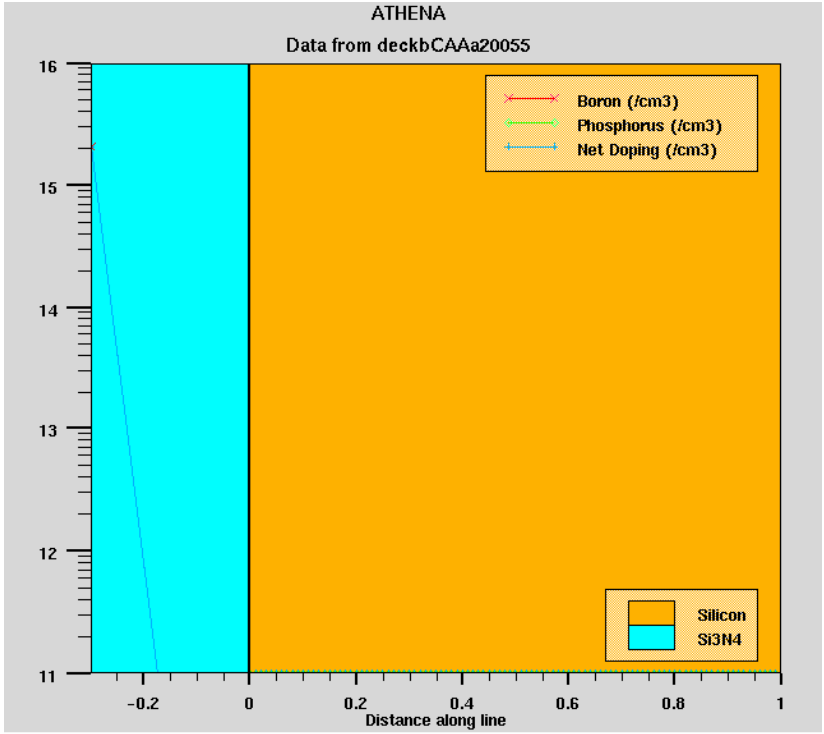
commands (RMC) select mesh define
commands select mesh initialize (LMC)
commands select process (RMC) deposit (LMC)
select parameters for nitride layer
commands select process (RMC) select implant (LMC)
select parameters for ion implant
tonyplot
quit

DECKBUILD EXAMPLE

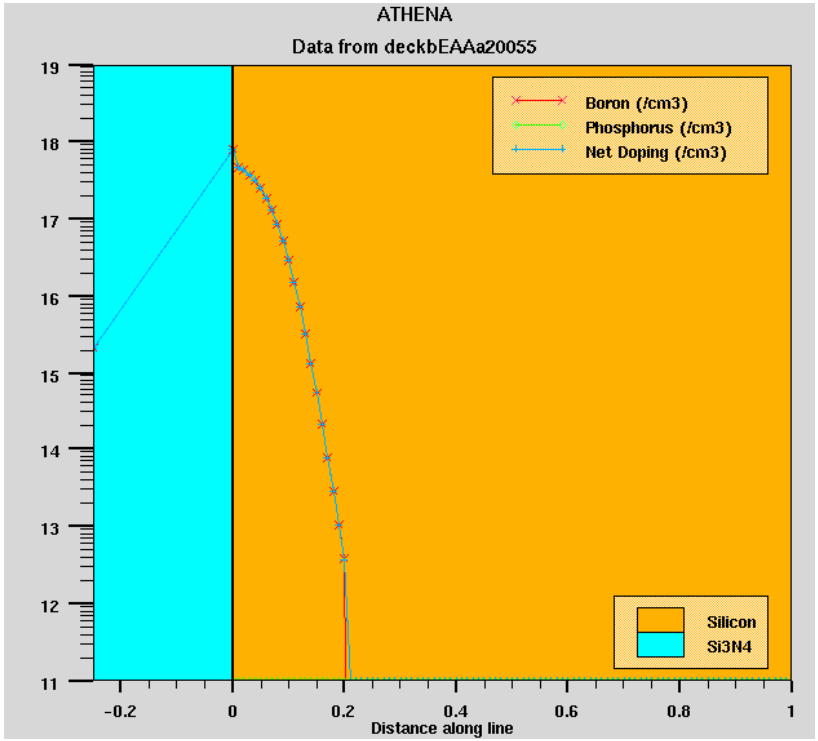
```
go athena
#comment lines start with #
#near location 0µm on the x line set grid approximately 0.1 µm
#near location 1µm on the x line set grid approximately 0.1 µm
line x loc=0.00 space=0.1
line x loc=1.00 space=0.1
#near location 0µm on the y line set grid approximately 0.01 µm
#near location 2µm on the y line set grid approximately 0.01 µm
line y loc=0.00 space=0.01
line y loc=2.00 space=0.01
#
init silicon phosphorous resistivity=15 orientation=100
#change nitride thickness to investigate implant penetration
deposit nitride thick=0.30
# dual Pearson model is SIMS verified empirical model
implant boron dose=8.0e12 energy=100 tilt=0 \
            rotation=0 crystal lat.ratio1=1.0 lat.ratio2=1.0
#
tonyplot
quit
```



TONY PLOT FOR EXAMPLE



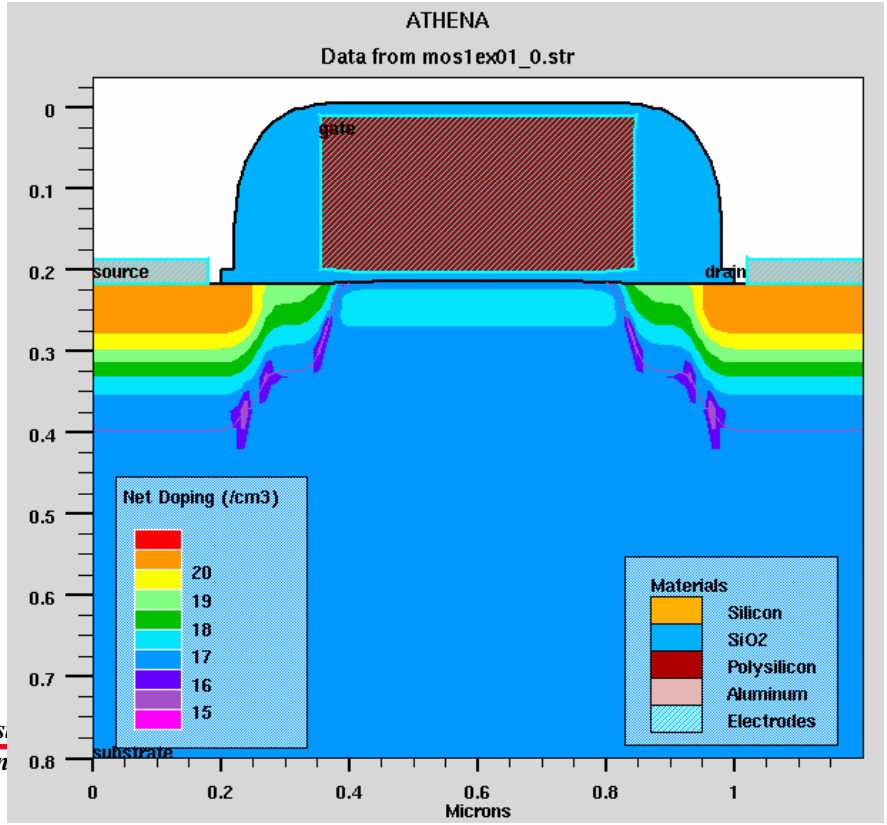
3000 Å Nitride



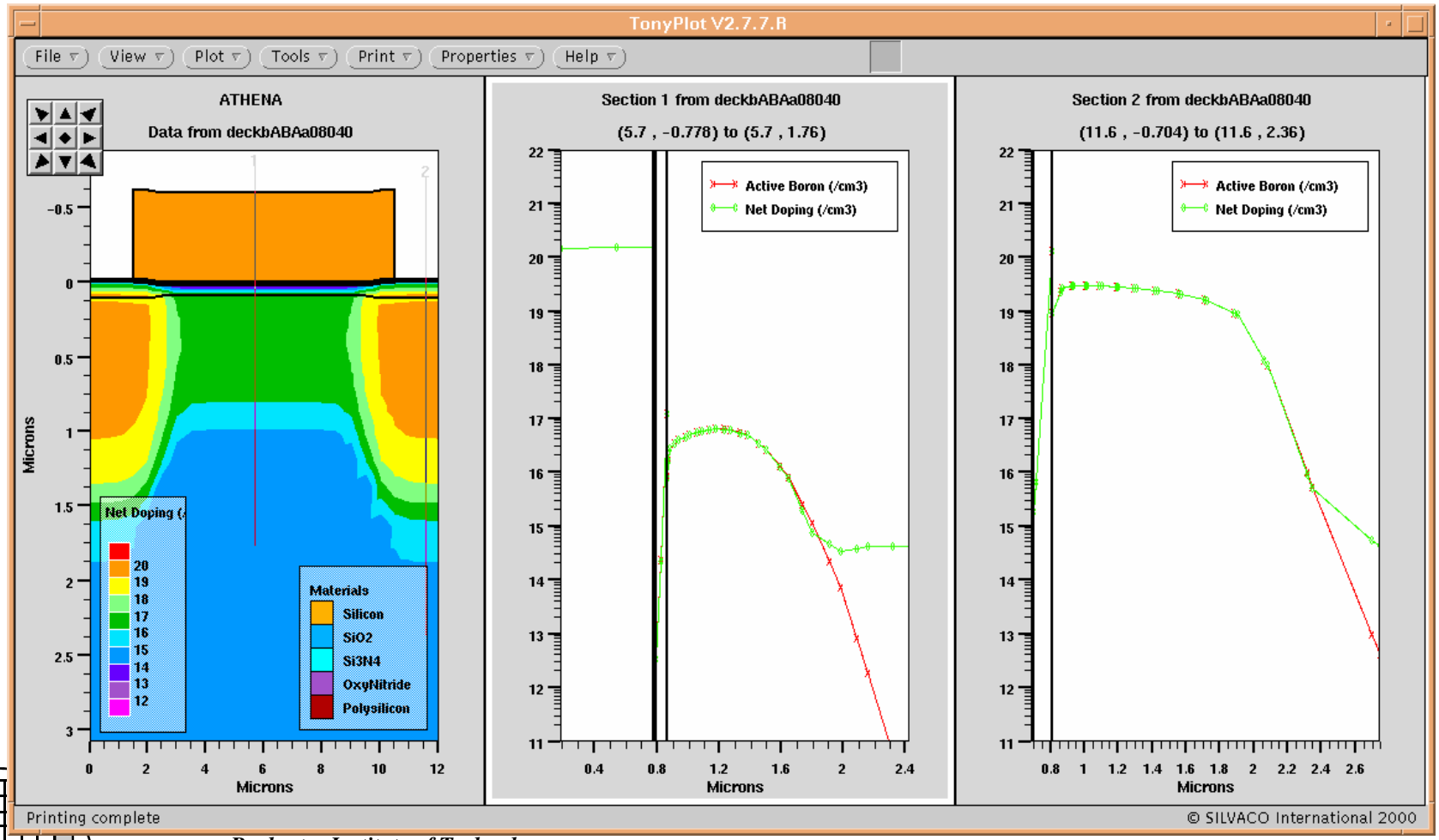
2500 Å Nitride

SUMMARY

Silvaco ATHENA (SUPREM) analysis allows for the calculation of resultant impurity concentrations, layer thickness, and much more for processes such as oxidation, diffusion, implantation and deposition for temperatures above 800 C.



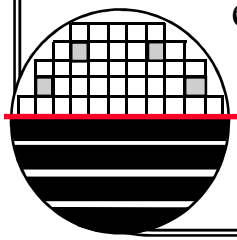
SILVACO ATHENA SIMULATIONS OF D/S IMPLANT



EXTRACT

The extract command provides a way to output important device parameters such as oxide thickness, junction depth, sheet resistance, surface concentration, and threshold voltage. These results are available in the run dialog window and in the results.final file. These commands can be placed anywhere in the input file. A few extract commands are shown below:

```
extract name="Source Oxide Thickness" thickness material="SiO~2" \
        mat.occno=1 x.val=2.0
extract name="Final Source xj" xj material="Silicon" mat.occno=1 x.val=2.0 \
        junc.occno=1
extract name="p-type Sheet Rs" p.sheet.res material="Silicon" mat.occno=1 \
        x.val=2.0 region.occno=1
extract name="Surface Concentration" surf.conc impurity="Net Doping" \
        material="Silicon" mat.occno=1 x.val=10.0
extract name="VTO" 1dvt ntype qss=3e11 workfunc=4.15 x.val=10.0
```



RESULTS.FINAL FILE

First Oxide=7611.19 angstroms (0.761119 um) X.val=2

2nd Oxide Thickness=8944.31 angstroms (0.894431 um) X.val=10

2nd Oxide Thickness=4251.74 angstroms (0.425174 um) X.val=2

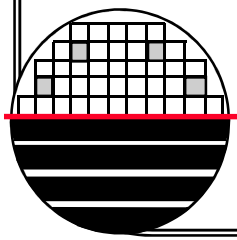
Gate Oxide Thickness=754.154 angstroms (0.0754154 um) X.val=10

Final Source xj=1.84039 um from top of first Silicon layer X.val=2

p-type Sheet Rs=95.5111 ohm/square X.val=2

Surface Concentration=6.86682e+14 atoms/cm3 X.val=10

VTO=-2.08365 V X.val=10



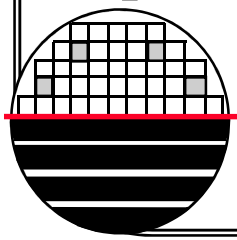
VIEWING AND PRINTING INPUT AND RESULTS FILES

The input file created using DECKBUILD can be saved as a text file. Select file on the top banner (RMC) and select Save As (LMC) and enter the filename.in

This text file can be viewed using KWrite, WordPad or other text editor. It can be sent to another computer using secure ftp (such as WinSCP) where it can be edited, read and/or printed.

These files can be printed in the VLSI lab by opening another Terminal Window and at the command type lpr filename.in <RET>

The output results file is saved as results.final in the same directory as the input file. This is also a text file that can be opened in KWrite, WordPad or other editor and sent to another computer using secure ftp.



SILVACO ATHENA (SUPREM) EXAMPLE

```
go athena
# set grid
line x loc=0.0 spac=0.1
line x loc=1.0 spac=0.05
line x loc=10.0 spac=0.05
line x loc=12.0 spac=0.1

line y loc=0.0 spac=0.01
line y loc=2.2 spac=0.01
line y loc=3.5 spac=0.3
line y loc=6.0 spac=0.5
```

Starting wafer resistivity = 11.3 ohm-cm

```
init silicon phosphor resistivity=11.3 orientation=1.00 space.mult=5.0

# ramp up from 800 to 900°c soak 50 min dry o2, ramp down to 800 n2
diff time=10 temp=800 t.final=900 dryo2 press=1.0 hcl.pc=0
diff time=50 temp=900 dryo2 press=1.0 hcl.pc=0
diff time=20 temp=900 t.final=800 nitro press=1.0 hcl.pc=0
```

} Grow Kooi oxide 1000 Å

```
deposit photoresist thickness=1.0
etch phtotoresist left ;1.x=2.0
etch photoresist right p1.x=10.00
```

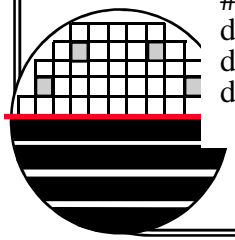
Ion Implant P-type D/S at Dose = 1E15

```
# ion implant drain and source
implant boron dose=1e15 energy=70 tilt=0 rotation=0 crysatal lat.ratio1=1.0 lat.ratio2=1.0

Etch photoresist all
```

Strip photoresist

```
# ramp up from 800 to 1000°c soak 90 min, ramp down to 800 n2
diff time=20 temp=800 t.final=1000 nitro press=1.0 hcl.pc=0
diff time=90 temp=1000 nitro press=1.0 hcl.pc=0
diff time=40 temp=1000 t.final=800 nitro press=1.0 hcl.pc=0
```

} Anneal D/S implant



SILVACO ATHENA (SUPREM) EXAMPLE

Ion Implant P-type channel at
Dose = 0, 4E12, 4e11, 1e12

```
# ion implant channel
implant boron dose=4e12 energy=100 tilt=0 rotation=0 crysatal lat.ratio1=1.0 lat.ratio2=1.0

etch oxide all

# ramp up from 800 to 1000°c soak 90 min dry o2, ramp down to 800 n2
diff time=20 temp=800 t.final=1000 dryo2 press=1.0 hcl.pc=0
diff time=90 temp=1000 dryo2 press=1.0 hcl.pc=0
diff time=40 temp=1000 t.final=800 nitro press=1.0 hcl.pc=0
```

Grow 700 Å gate oxide

```
deposit nitride thick=0.010
```

Deposit 100 Å nitride

```
# ramp up from 800 to 1000°c soak 50 min dry o2, ramp down to 800 n2
diff time=10 temp=800 t.final=1000 dryo2 press=1.0 hcl.pc=0
diff time=50 temp=1000 dryo2 press=1.0 hcl.pc=0
diff time=20 temp=1000 t.final=800 nitro press=1.0 hcl.pc=0
```

Temp cycle for growth of oxynitride

```
deposit oxynitride thick=0.01
```

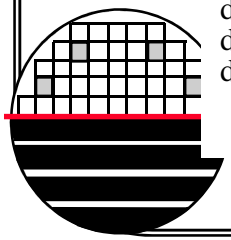
Deposit 100 Å oxynitride

```
deposit poly thick=0.60 c.phosphor=4e20
```

Deposit 6000 Å poly

```
# ramp up from 800 to 1000°c soak 30 min, ramp down to 800 n2
diff time=20 temp=800 t.final=1000 nitro press=1.0 hcl.pc=0
diff time=30 temp=1000 nitro press=1.0 hcl.pc=0
diff time=40 temp=1000 t.final=800 nitro press=1.0 hcl.pc=0
```

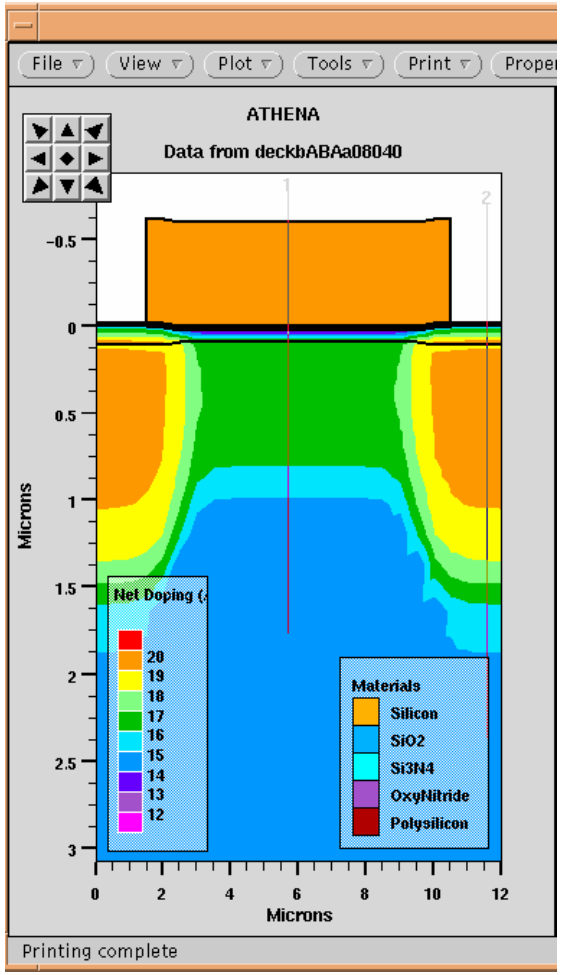
Temp cycle for poly dope



SILVACO ATHENA (SUPREM) EXAMPLE

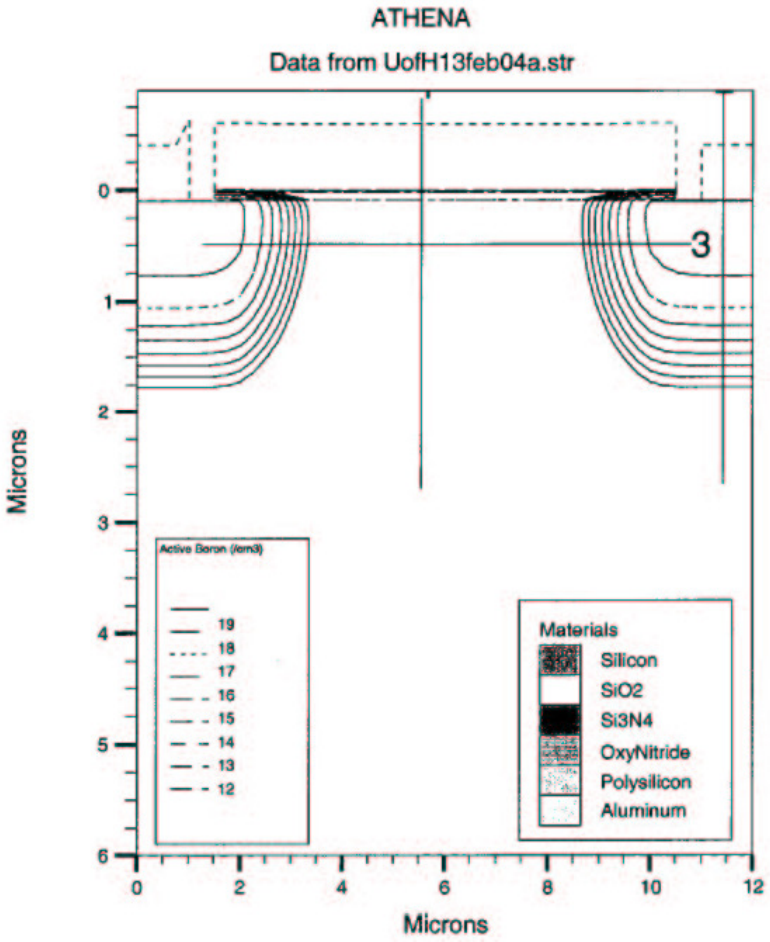
```
etch poly left p1.x=1.5
etch poly right p1.x=10.5

etch oxynitride left p1.x=1.5
etch oxynitride right p1.x=10.5

etch nitride left p1.x=1.5
etch nitride right p1.x=10.5

etch oxide left p1.x=1.5
etch oxide right p1.x=10.5

deposit alumin thick=0.5

etch alum start x=1.0 y= -2.0
etch cont x=1.0 y= 2.0
etch x=11.0 y= 2.0
etch done x=11.0 y= -2.0

struct outfile=UofH.str

tonyplot UofH.str

quit
```

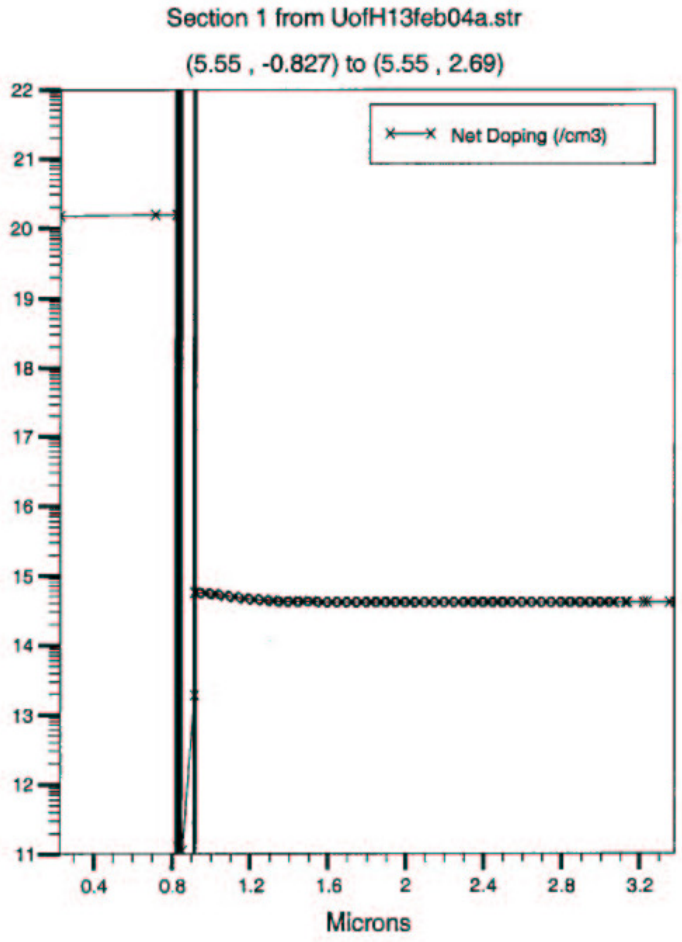
Deposit 5000 Å aluminum



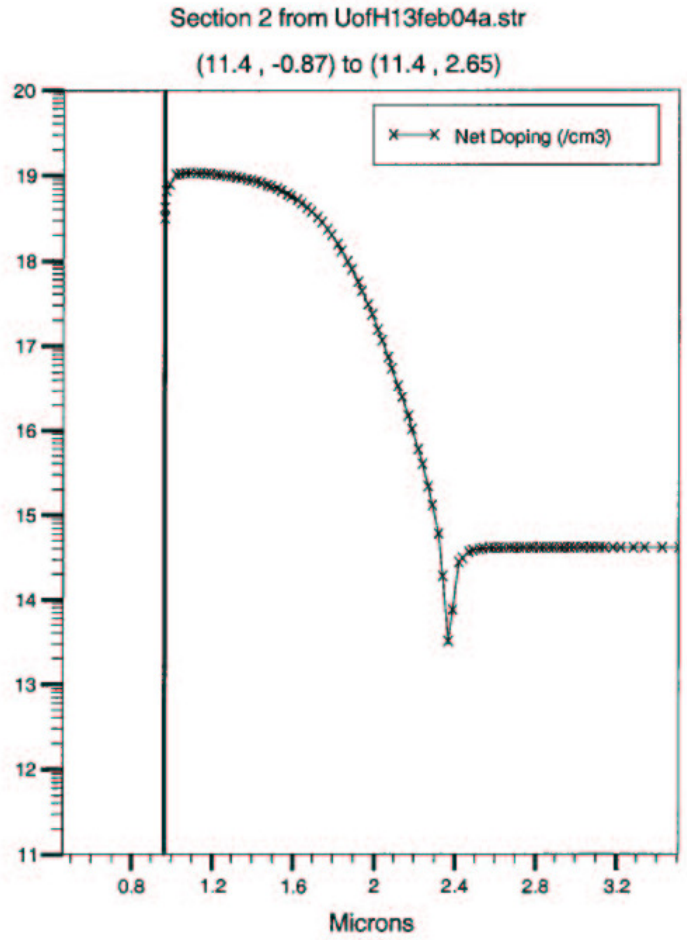
Tonyplot example Only

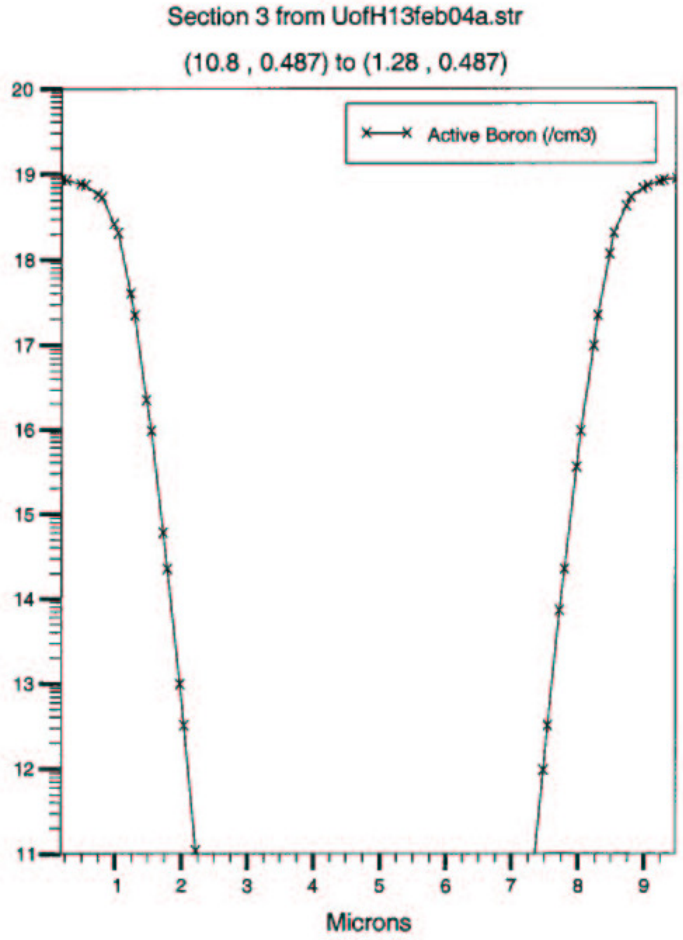
SILVACO ATHENA (SUPREM)





SILVACO ATHENA (SUPREM)





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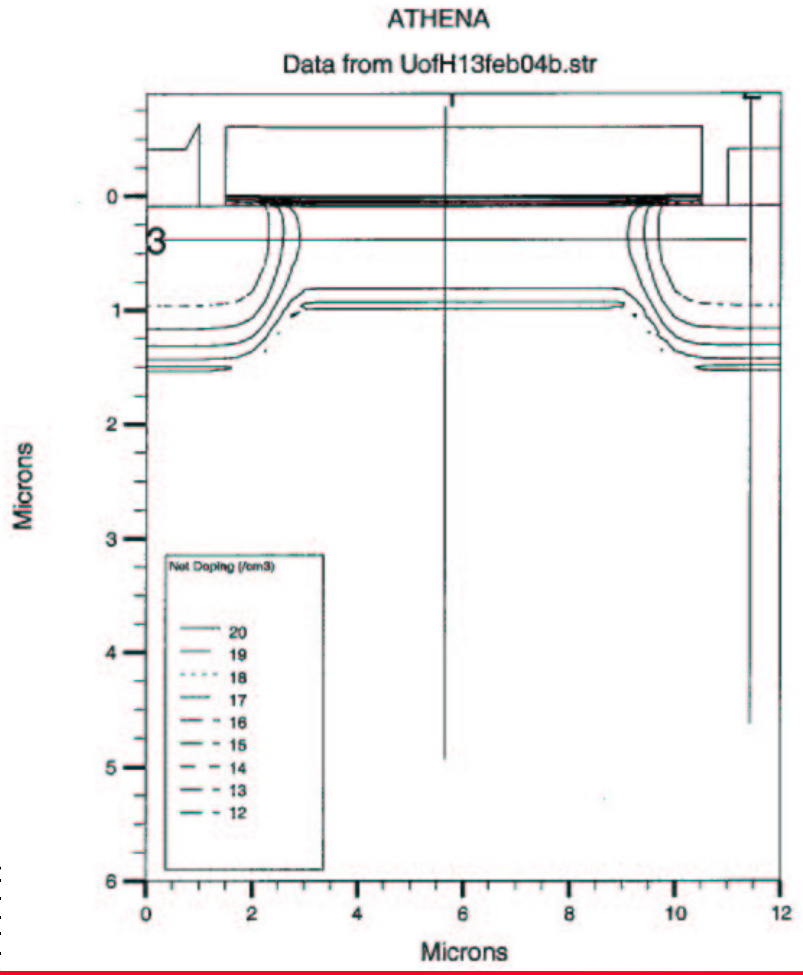
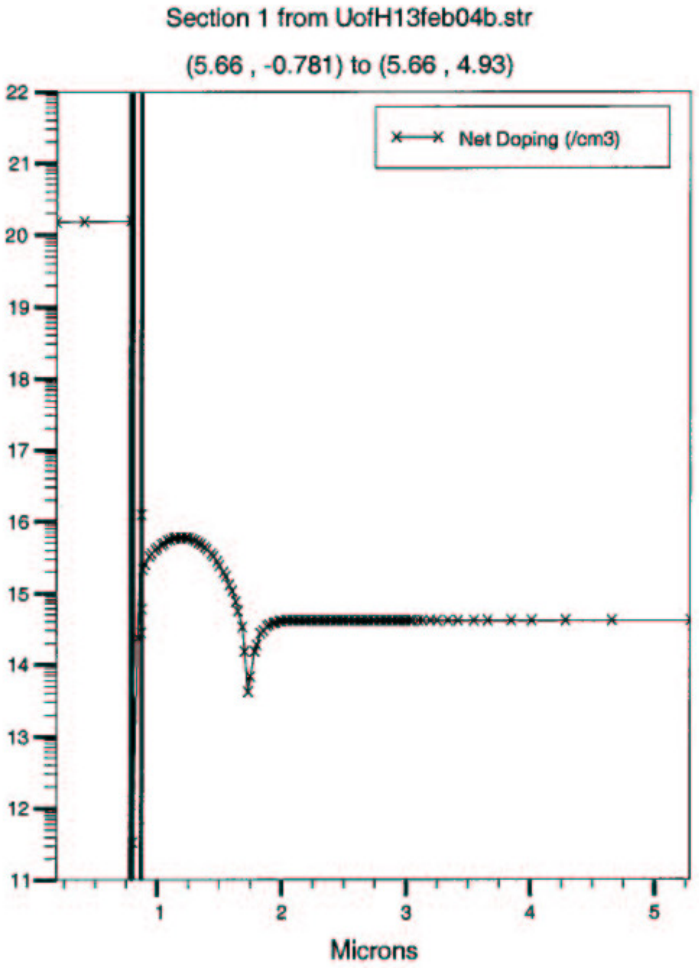
SILVACO ATHENA (SUPREM)





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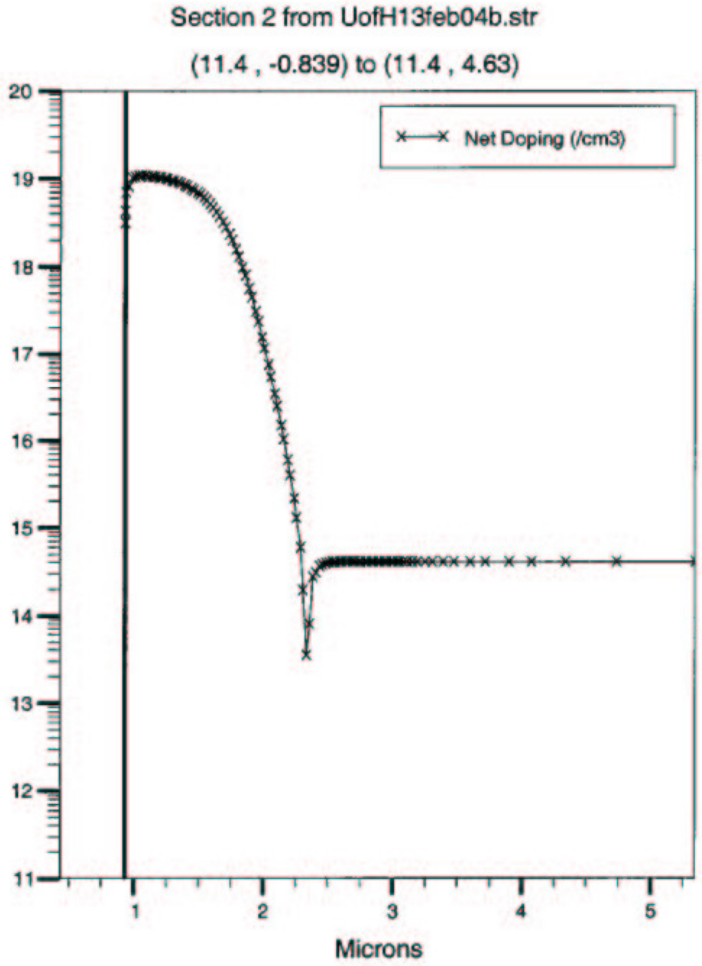
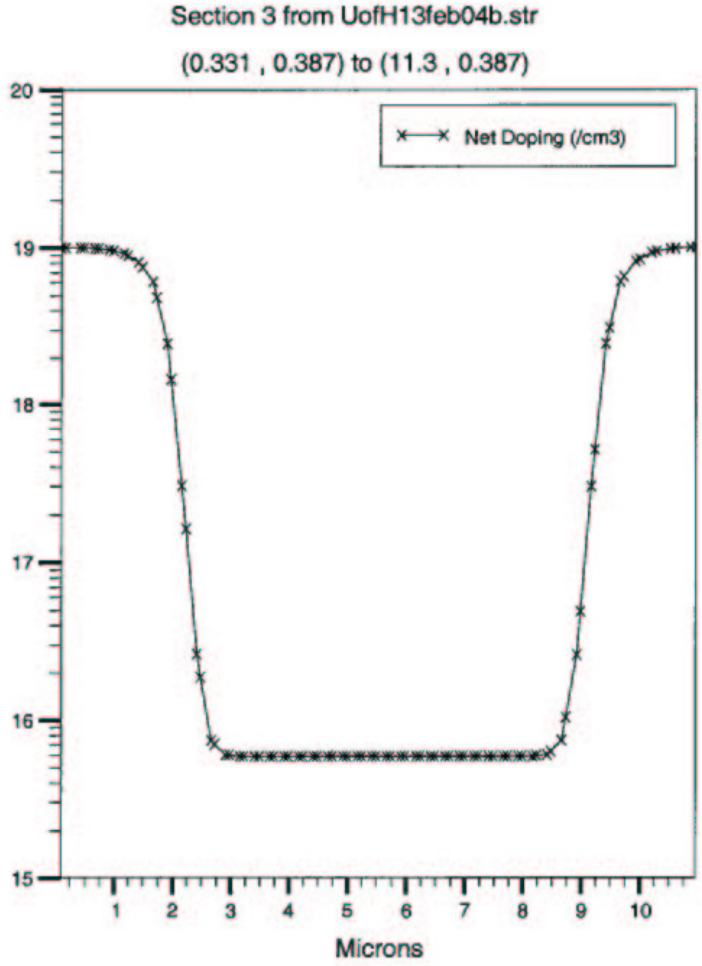
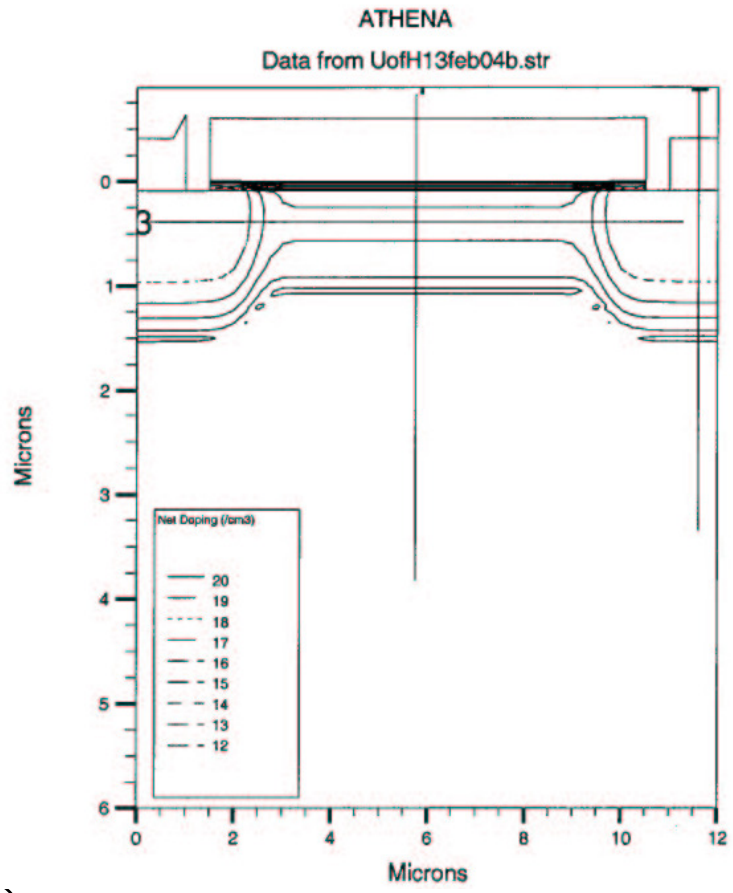
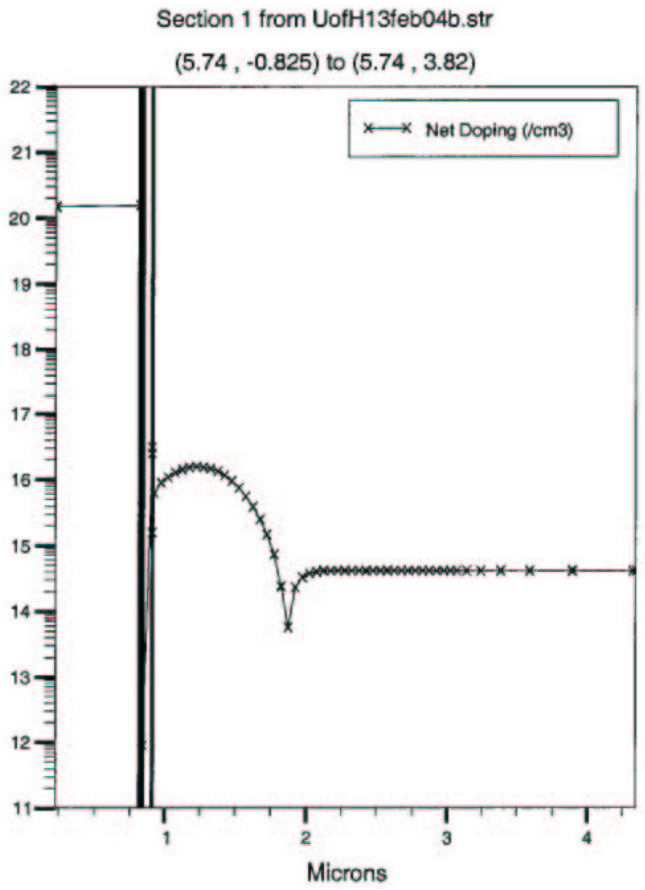
SILVACO ATHENA (SUPREM)



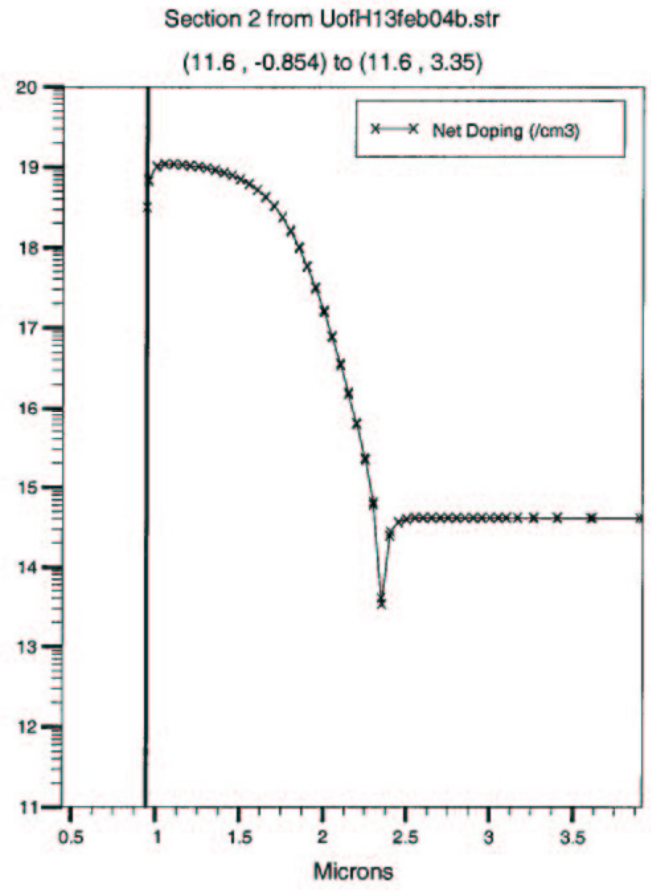


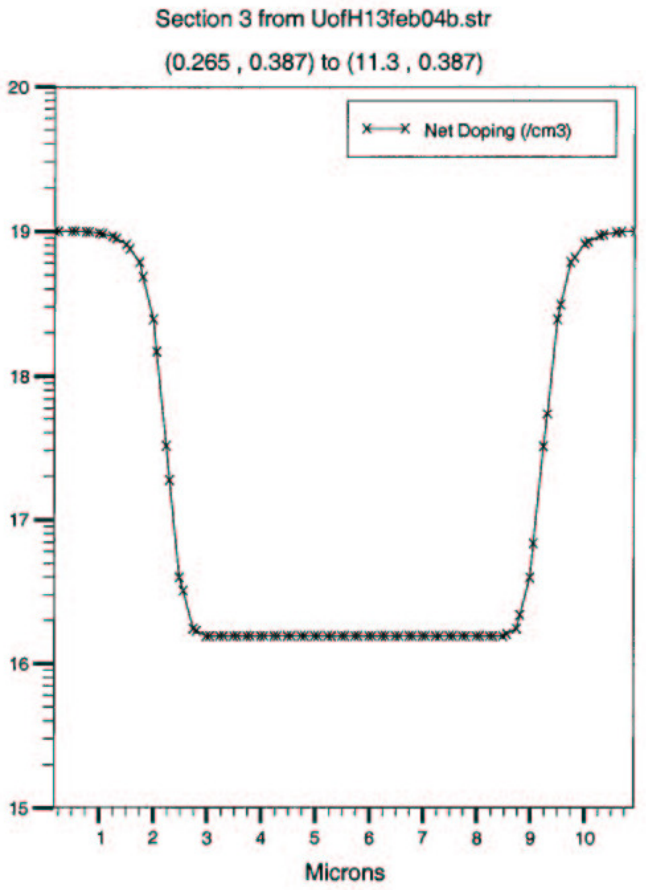
SILVACO ATHENA (SUPREM)





SILVACO ATHENA (SUPREM)





SILVACO ATLAS (DEVICE SIMULATOR) EXAMPLE

```
Go athena
Init infile=UofH.str
```

Read in structure file created by Athena

```
#name the electrodes…
Electrode name=gate x=6
Electrode name=source x=0
Electrode name=drain x=12
Electrode name=substrate backside
```

Define location of gate, source and drain

```
Extract name="vt" 1dvt ptype qss=1e11 workfunc=4.11 x.val=6

Go atlas

# define the gate workfunction
Contact name=gate n.poly
# define the Gate Qss
Interface qf=1e11

# use the cvt mobility model for MOS
Models cvt srh

# set gate biases with Vds=0.0
Solve init
Solve vgate=0 outf=solve_temp0
Solve vgate=-1 outf=solve_temp1
Solve vgate=-1 outf=solve_temp2
Solve vgate=-3 outf=solve_temp3
Solve vgate=-4 outf=solve_temp4
Solve vgate=-5 outf=solve_temp5
```

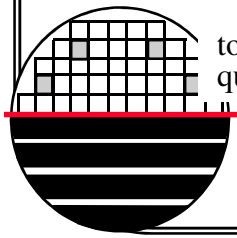
Step gate voltage from 0 to –5 volts in 1 volt steps

```
# load in temporary file and ramp Vds
Load infile=solve_temp0
Log outf=Vg_0.log
Solve name=drain vdrain=0 vfinal=-5 vstep=-0.5
```

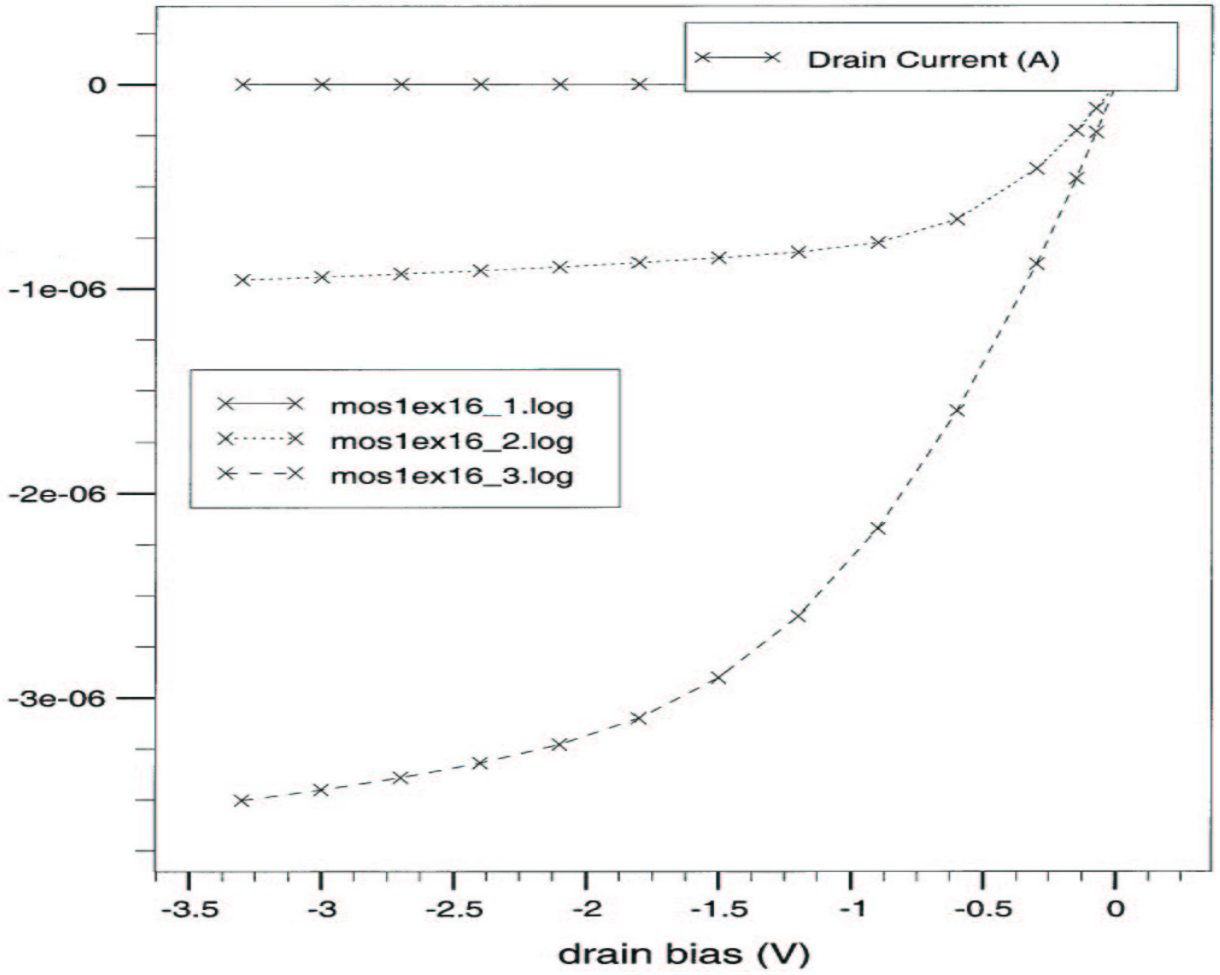
SILVACO ATLAS (DEVICE SIMULATOR EXAMPLE

```
# load in temporary file and ramp vds
load infile=solve_temp1
log outf=vg_1.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp2
log outf=vg_2.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp3
log outf=vg_3.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp4
log outf=vg_4.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp5
log outf=vg_5.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# extract max current and saturation slope
extract name="pidsmax" max(abs(i."drain"))
extract name="p_sat_slope" slope(minslope(curve(abs(v."drain"), abs(i."drain"))))

tonyplot –overlay vg_0.log vg_1.log vg_2.log vg_3.log vg_4.log vg_5.log –set mos1ex09_1
quit
```

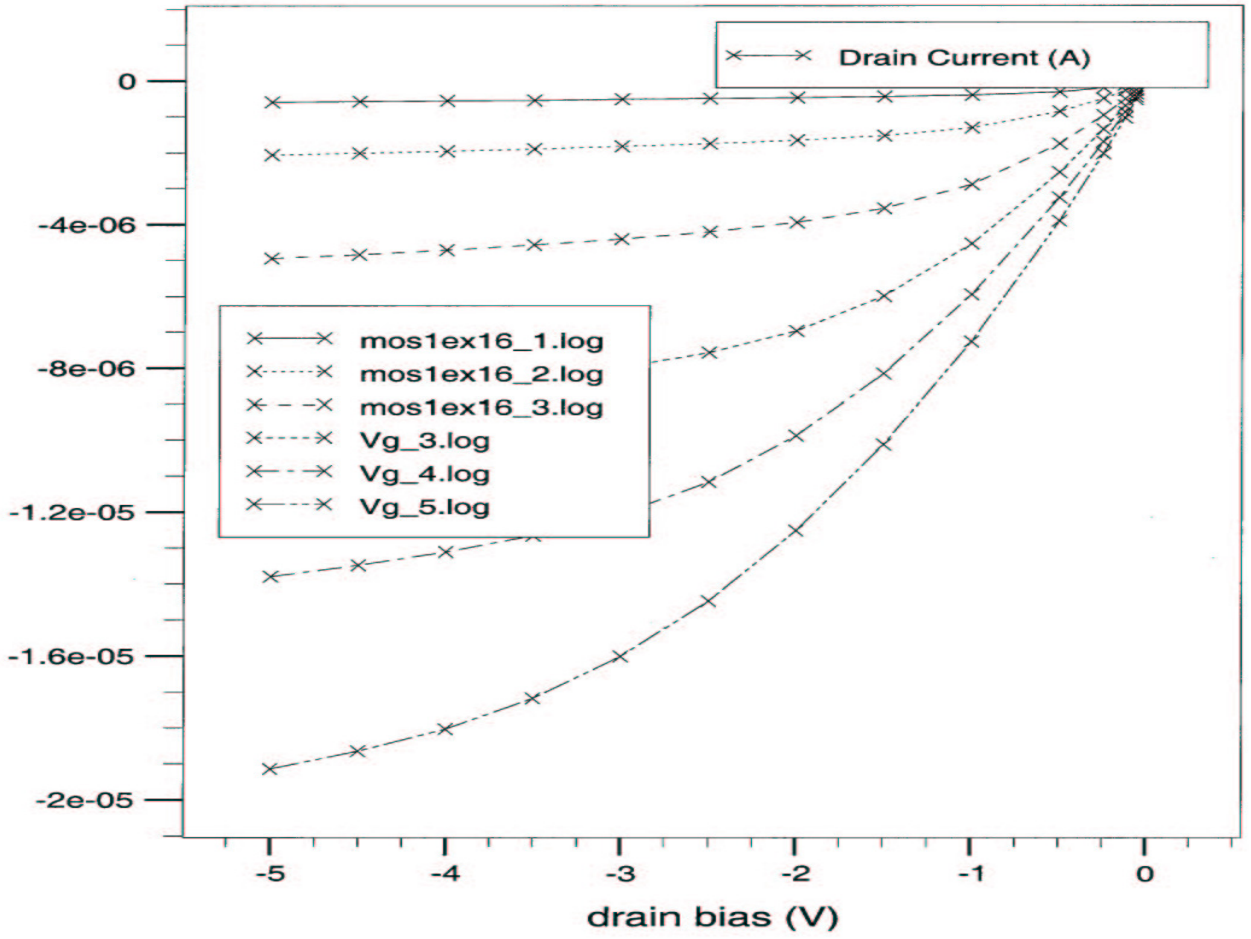
Sweep drain voltage from 0 to –5 volts in 0.5 volt steps



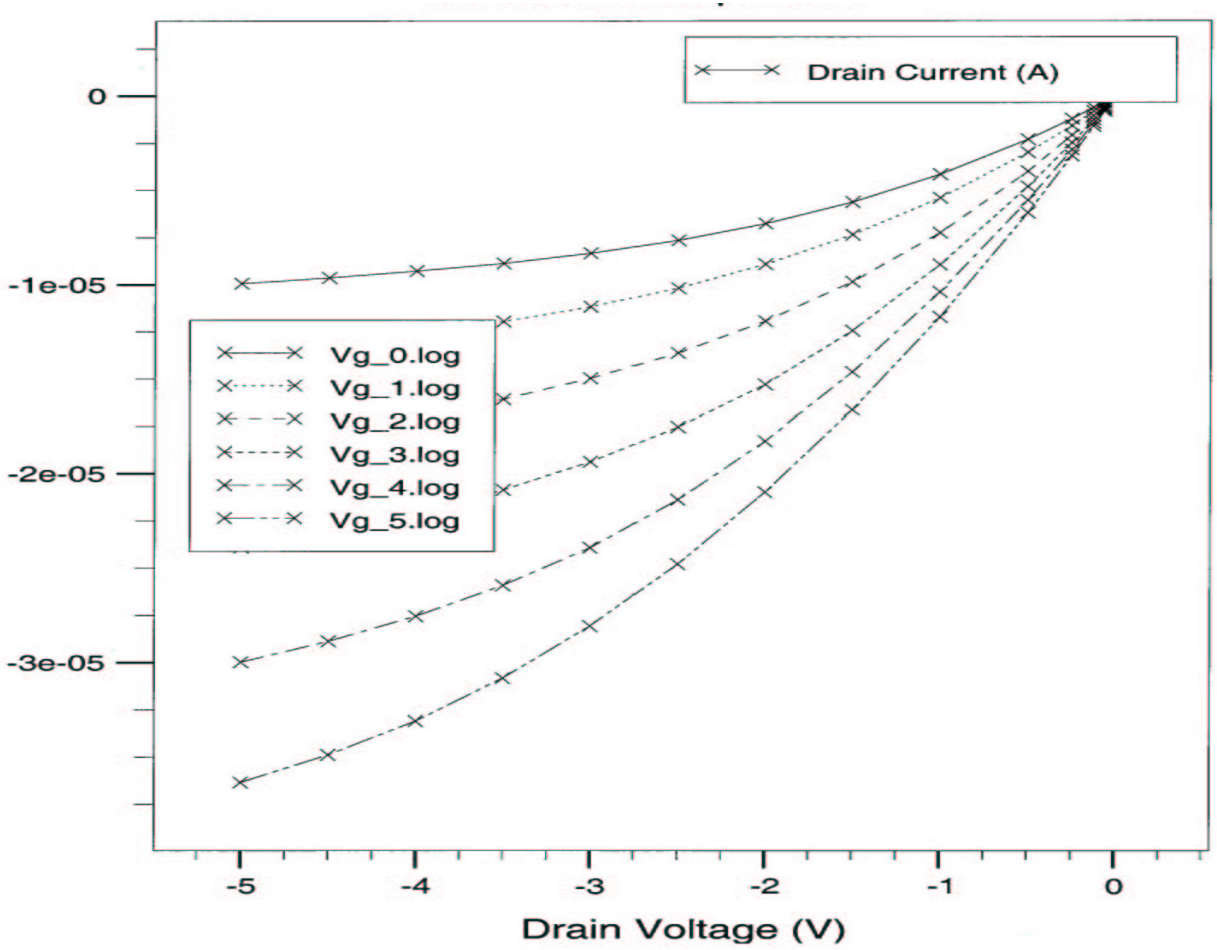
ATLAS SIMULATED FAMILY OF CURVES



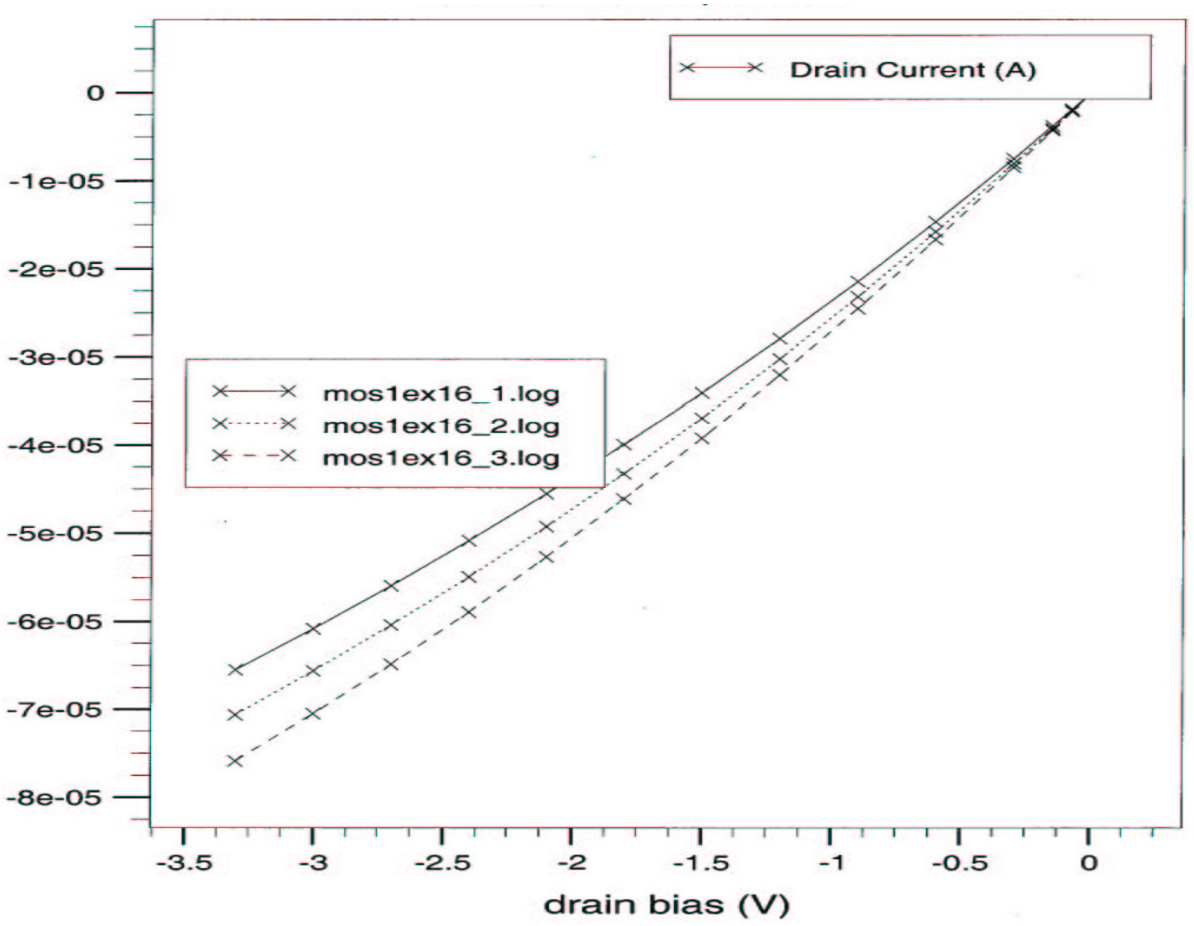
ATLAS SIMULATED FAMILY OF CURVES



ATLAS SIMULATED FAMILY OF CURVES



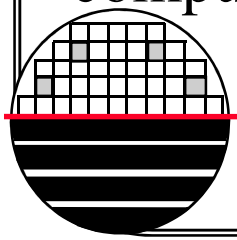
ATLAS SIMULATED FAMILY OF CURVES



VLSI DESIGN CENTER AT RIT

The VLSI Design Center (room 17-2500) consists of AMD Athlon 64 FX-51 Gentoo LINUX workstations, file servers and printers. The workstations are primarily PC's running LINIX operating system. The PC's are fast, have lots of RAM and disk space. There are two file servers for user accounts and application software. The two main print devices are a HP laser printer and a HP 36 inch color plotter. There devices are connected through an Ethernet based network. The primary application software, on this network, is the very sophisticated and tightly integrated Mentor Graphics suite of EDA (Electronic Design Automation) tools.

Accounts on the computers and access to the room are controlled by the computer engineering department. Currently Charles Gruener for computer accounts and Rick Tolleson for card swipe room access.

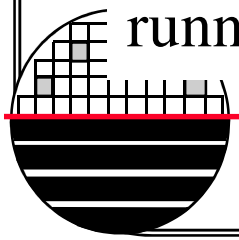


BASICS - DESKTOP

A graphical interface that provides workspaces, windows, menus, controls, and a front panel to help you organize and manage your software applications.

The **Front Panel** has a tool bar (usually at the bottom of the screen).
The tool bar has a K-Gear icon which allows access to editors, graphics programs and the open office software package. The open office package has calculators, drawing programs, equation editor and word processing. You can change the settings for the look and feel of the desktop and the windows that are running. I suggest that you do not go too wild changing things , instead stick to getting the job done.

There are four “desk tops” available to run programs on. The toolbar tells you which desktop you are looking at and what is running in each window on the desktop.

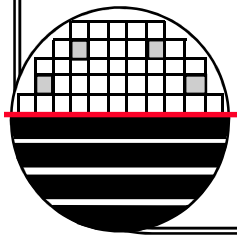


BASICS CONTINUED

The Mouse: is a three button mouse. The left mouse button is used to select or "click" on something. The right mouse button is used for popup menus. The middle mouse button is typically defined for each application and does not have a common function. For example in the layout software "IC" the middle mouse button shifts the layout so that the clicked location is centered in the workspace.

Log Out: click on K Gear icon, select Log Out…, Select End Current Session

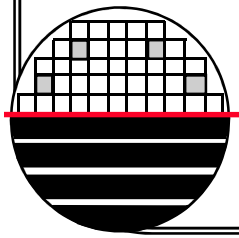
Restore Session: If there is no activity for several minutes the screen will be locked and require the user to type his password to restore the session.



BASIC UNIX COMMANDS

Command	Description
ls	list the files and directories in the current directory
ls xxx*	list file or folders beginning with name xxx
cd	change directory
mv	move a file (rename a file)
rm	remove a file (delete a file)
pwd	print path of current directory
mkdir	create a new directory
rmdir	remove a director
more filename	displays contents of filename

It is important to remember that since this is a UNIX operating system, the commands are case sensitive.



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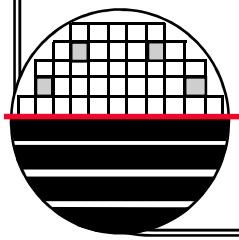
2. The Science and Engineering of Microelectronic Processing, Stephen Campbell
3. Technology Modeling Associates, TMA-SUPREM-4, Instruction Manual.
4. Silvaco Modeling, Inc.
5. MicroTec-3.03 release note of March 27, 1998 floppy-disk contains a complete set of MicroTec-3.03 programs for 2D semiconductor process and device simulation and the Manual in Adobe Acrobat format. http://www.siborg.ca



HOMEWORK – SILVACO 2D SIMULATIONS

1. Determine the minimum nitride thickness that can be used for the locos process in the RIT sub micron CMOS process that will work as a ion implant masking layer during the channel stop implant.
2. Determine the minimum field oxide thickness that can be used for masking subsequent ion implants.
3. Determine the minimum poly thickness that can be used for masking n+ and p+ D/S implants.
4. Determine the maximum time that the wafers can be at 1000 C before phosphorous from the poly gate will penetrate the gate oxide and dope the channel region of the FET.