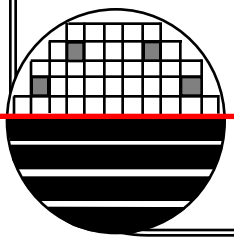
ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

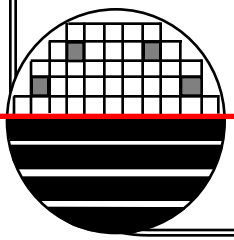
SPICE Examples

Dr. Lynn Fuller
Electrical and Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041
Dr. Fuller's Webpage: http://people.rit.edu/lffeee
Email: Lynn.Fuller@rit.edu
Dept Webpage: http://www.microe.rit.edu

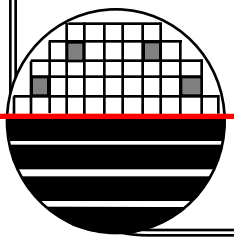


ADOBE PRESENTER

This PowerPoint module has been published using Adobe Presenter. Please click on the Notes tab in the left panel to read the instructors comments for each slide. Manually advance the slide by clicking on the play arrow or pressing the page down key.



OUTLINE

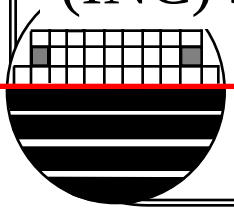


INTRODUCTION

SPICE (Simulation Program for Integrated Circuit Engineering) is a general-purpose circuit simulation program for non-linear DC, non-linear transient, and linear AC analysis. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, transmission lines, switches, and several semiconductor devices: including diodes, BJTs, JFETs, MESFETs, and MOSFETs. Circuits with large numbers of all types of components can be simulated.

SPICE input files and output files are simple text files (e.g. name.txt)

Input files include a TITLE, circuit description NET LIST, analysis directives (COMMANDS), and lists of other text files to include (INC) such as model libraries (LIB) and an END command.



INTRODUCTION

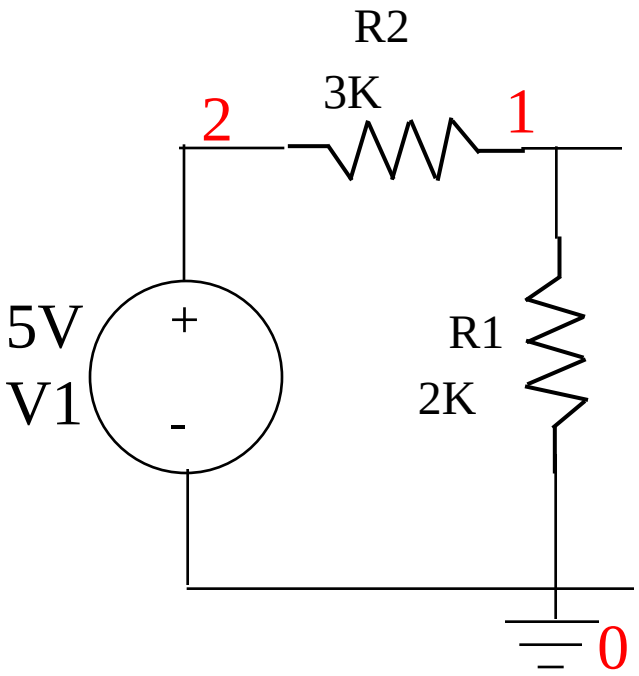
PSpice Lite 9.2 is one of the OrCAD family of products, from Cadence Design Systems, Inc., offering a complete suite of electronic design tools. It is free and includes limited versions of OrCAD Capture, for schematic capture, PSpice for analog circuit simulation and Pspice A/D for mixed analog and digital circuit simulation. PSpice Lite 9.2 is limited to 64 nodes, 10 transistors, two operational amplifiers and 65 primitive digital devices. See page 35 (xxxv) of the PSpice Users Guide.

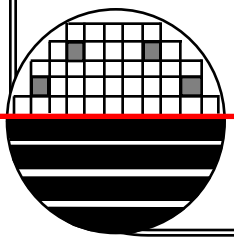
LT SPICE – is a free SPICE simulator with schematic capture from Linear Technology. It is quite similar to PSpice Lite but is not limited in the number of devices or nodes. Linear Technology (LT) is one of the industry leaders in analog and digital integrated circuits. Linear Technology provides a complete set of SPICE models for LT components.

CREATING THE INPUT FILE

The input file can be generated from a schematic capture program, or just typed in a text editor such as “Notepad” or “WordPad”

```
*Simple Resistor Divider
R1 1 0 2K
R2 2 1 3K
V1 2 0 DC 5
.DC V1 0  5 .1
.END
```



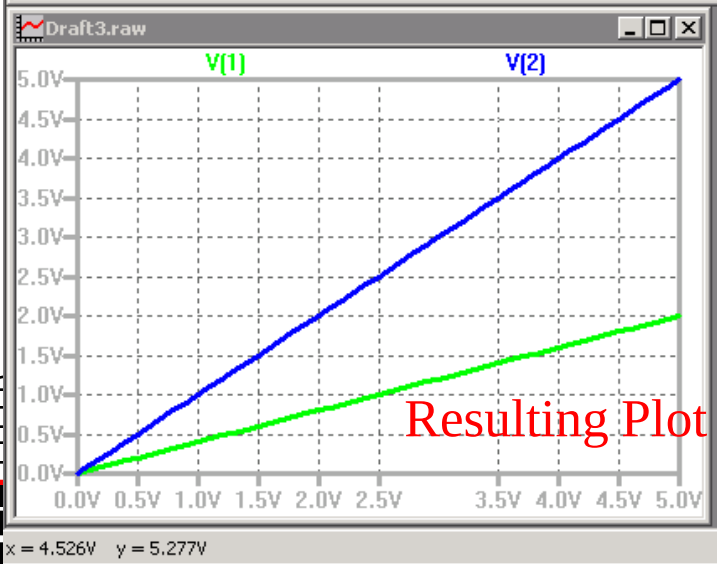


LTSPICE USING INPUT FILE INSTEAD OF SCHEMATIC

Draft3.asc

```
.include C:\SPICE\SimpleExample.txt
.op
```

.op is a spice directive to do DC operating point analysis



Resulting Plot

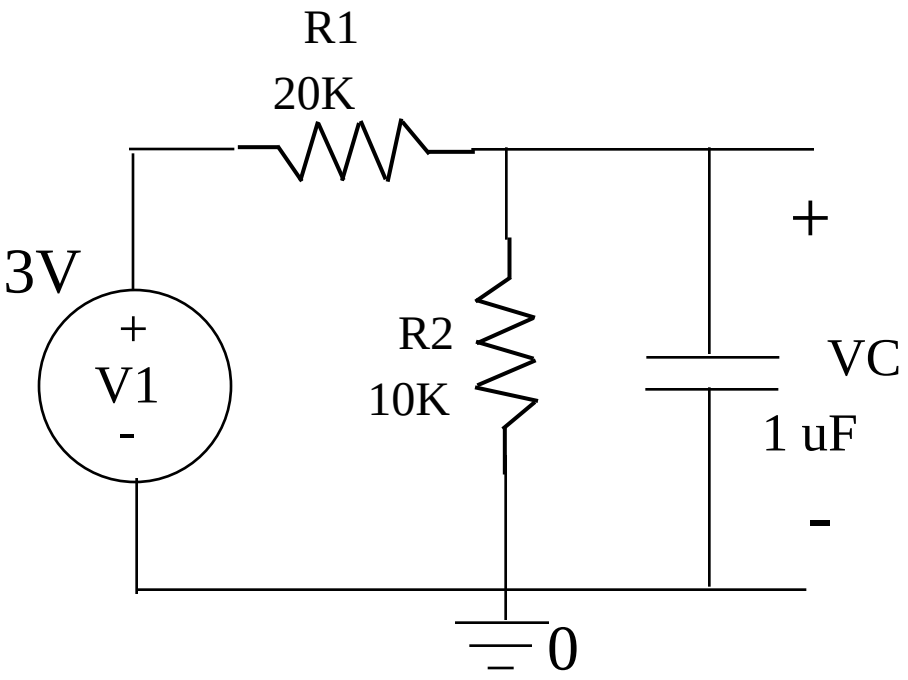
SimpleExample.txt - Notepad

File Edit Format View Help

```
*DR FULLER - SIMPLE EXAMPLE TITLE
* THE FIRST LINE IS THE TITLE
* LINES THAT START WITH * ARE COMMENT LINES AND DO NOTHING
* UPPER AND lower case text ARE TREATED THE SAME
* CIRCUIT IS DESCRIBED BELOW (NET LIST)
R1 1 0 2K ; resistor R1 between node 1 and zero has value 2000 ohms
R2 2 1 3K
V1 2 0 DC 5 ; voltage source V1 is a DC source of 5 volts
*
* REQUESTED ANALYSIS (DIRECTIVES OR COMMANDS)
.DC V1 0 5 .1 ; find all node voltages and branch currents for V1 starti
* incrementing by 0.1 volts ending at 5 volts
*
*.INCLUDE File_name.txt ;(none for this example)
*
.END
```

This is a text file located at C:\SPICE\SimpleExample.txt

RC DIVIDER CIRCUIT

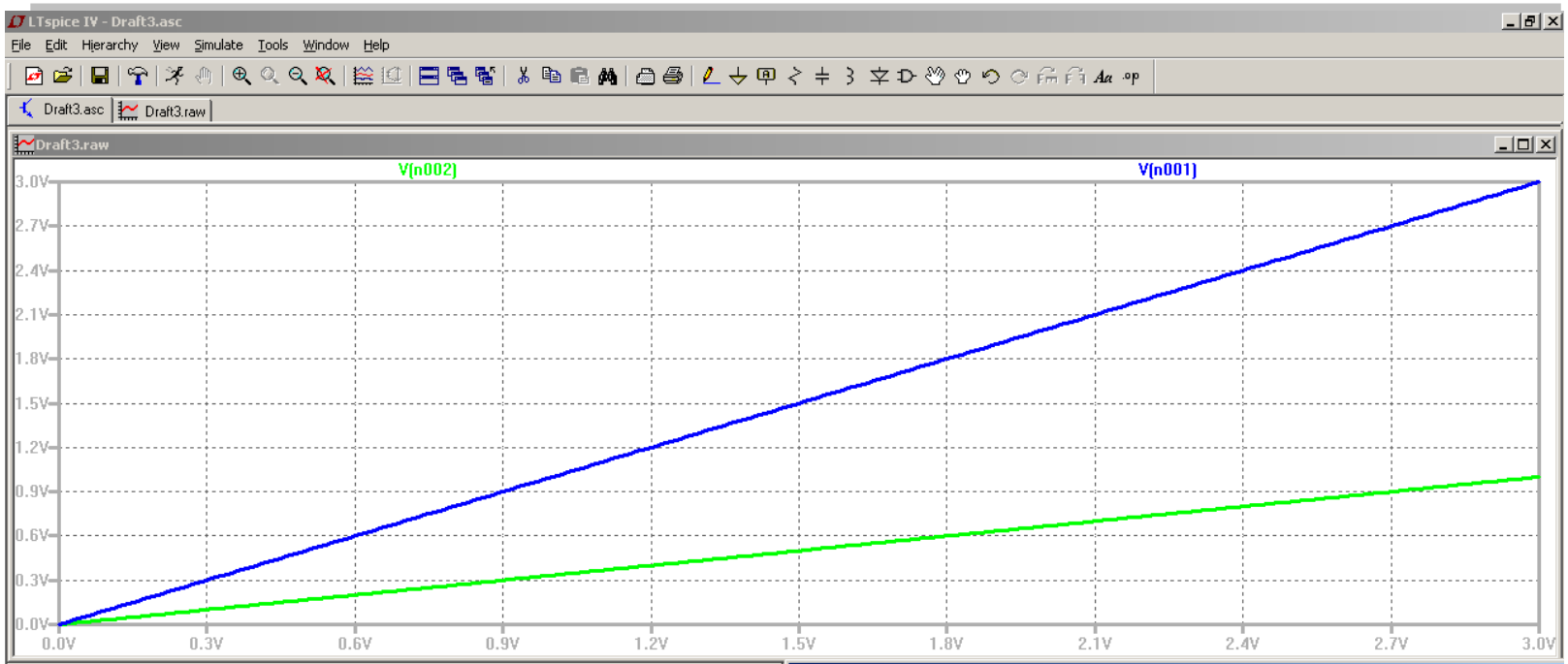


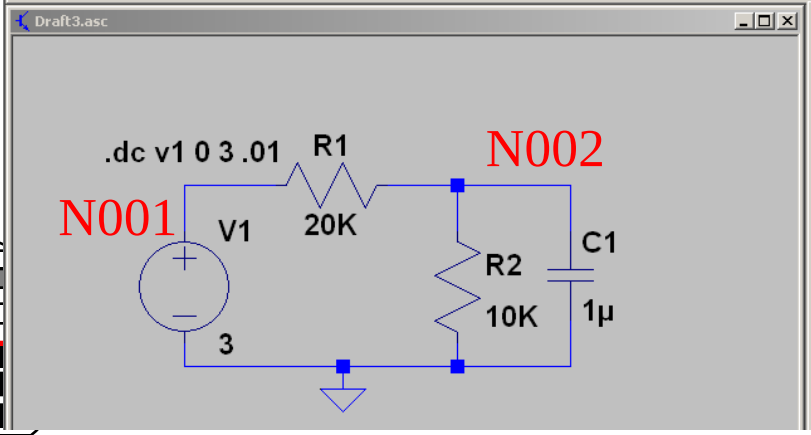
Calculate VC as the voltage V1 is swept from 0 to 3 volts

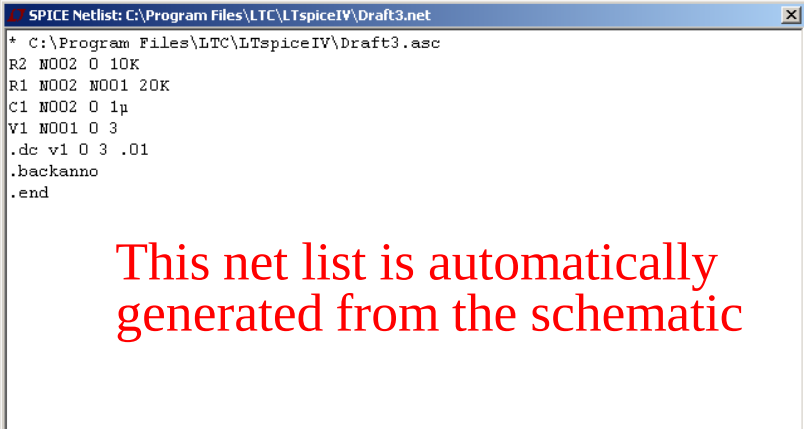
Change the V1 to a 3 volt pulse function and plot VC versus time.

Change the voltage V1 to an AC voltage source and plot VC versus frequency

DC SPICE ANALYSIS USING LTSPICE

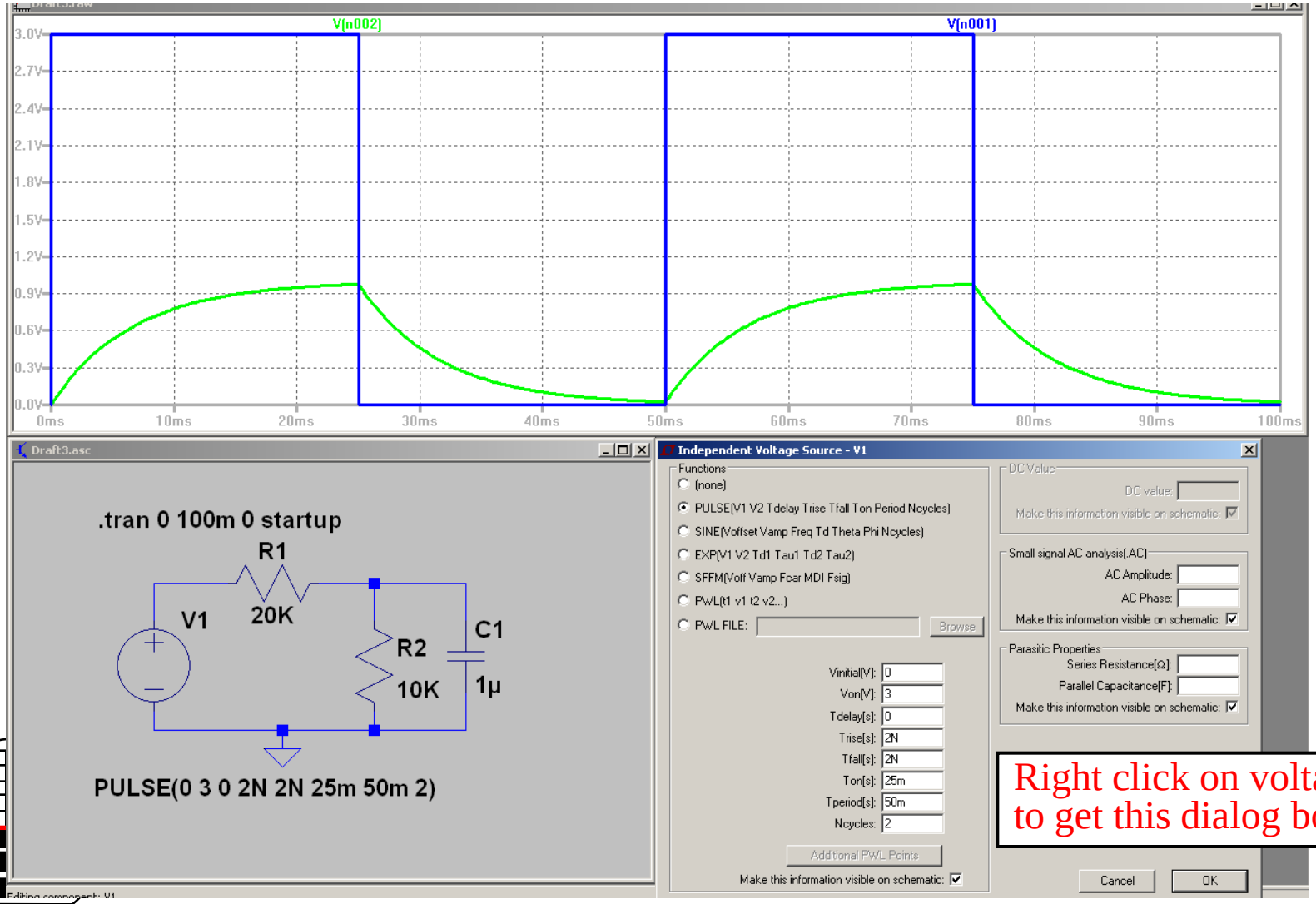






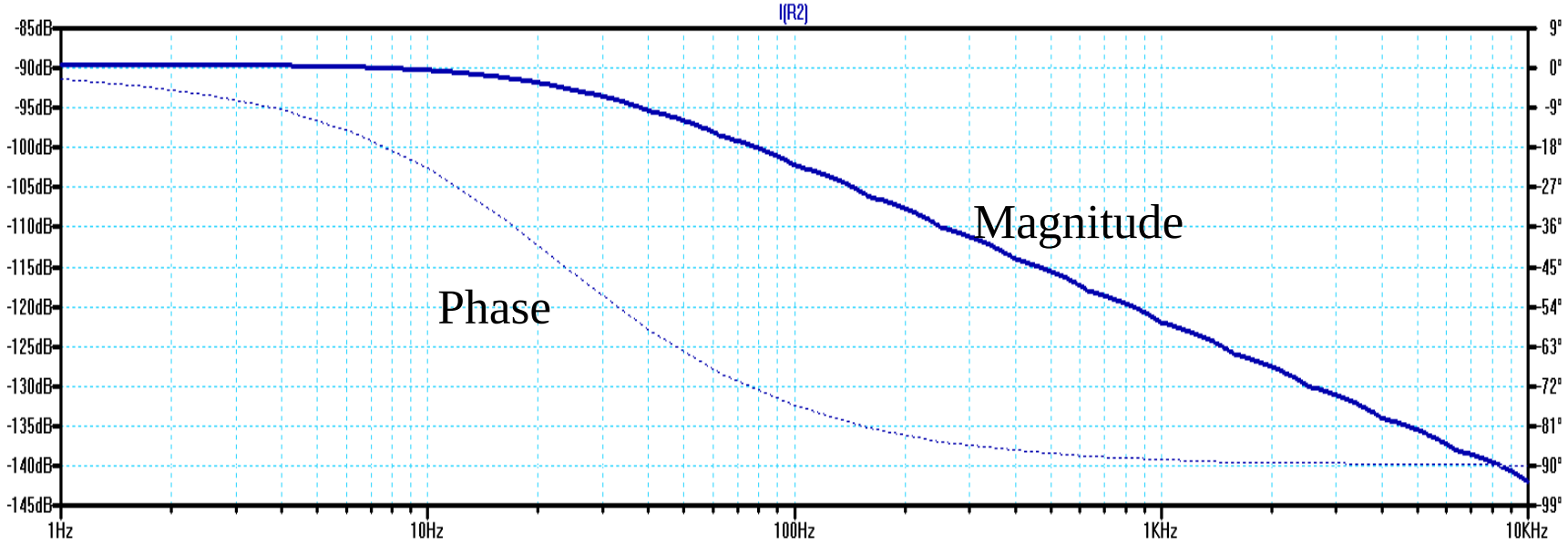
This net list is automatically generated from the schematic

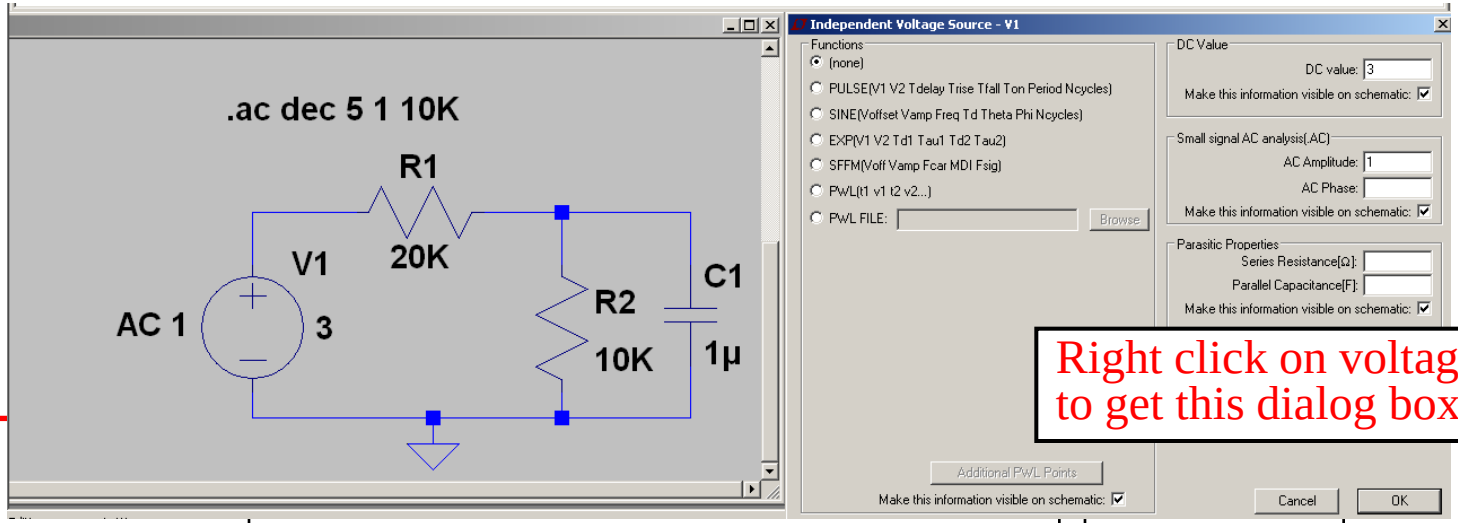
TRANSIENT ANALYSIS USING LTSPICE



Right click on voltage source to get this dialog box

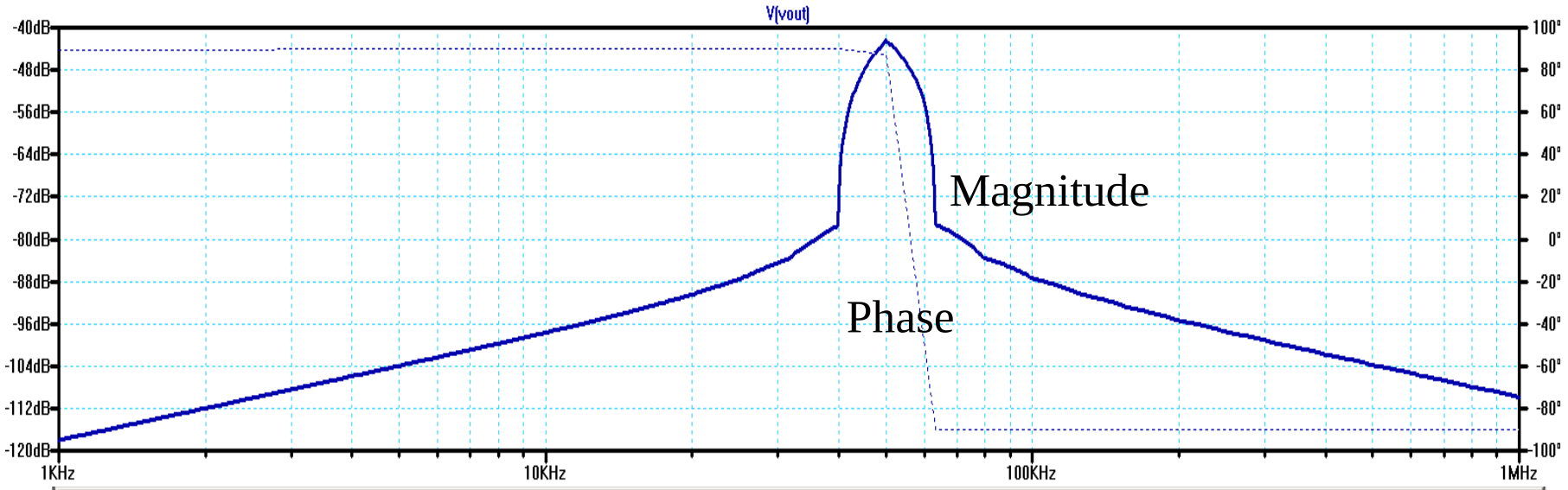
AC ANALYSIS USING LTSPICE

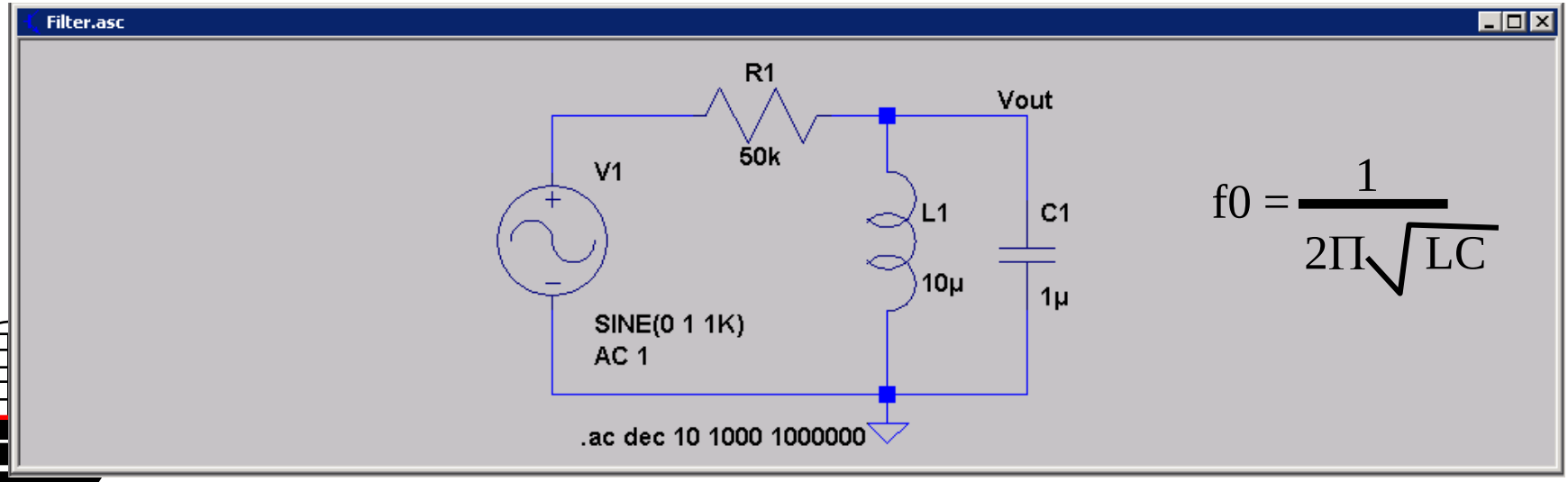




Right click on voltage source to get this dialog box

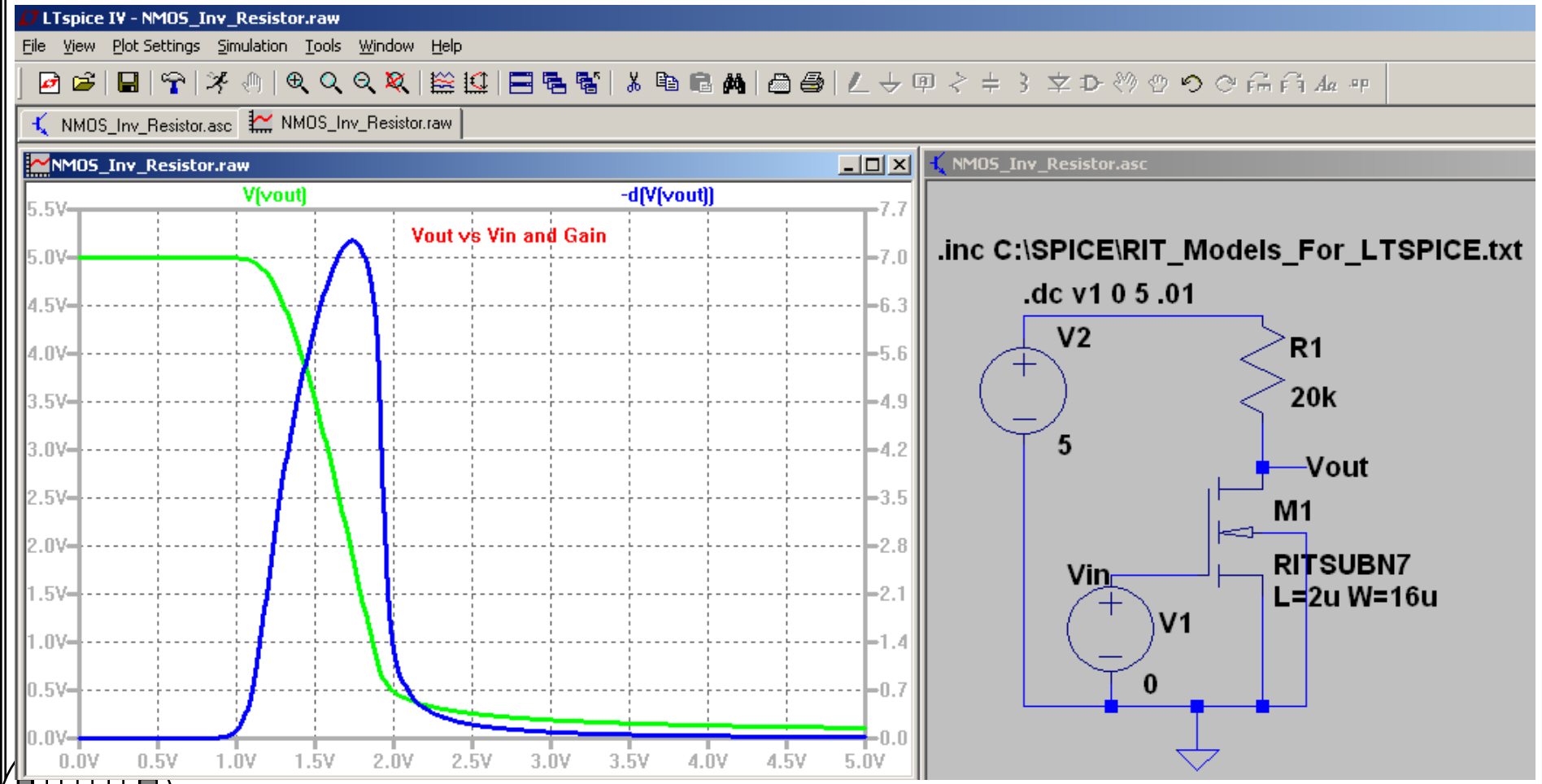
LC FILTER



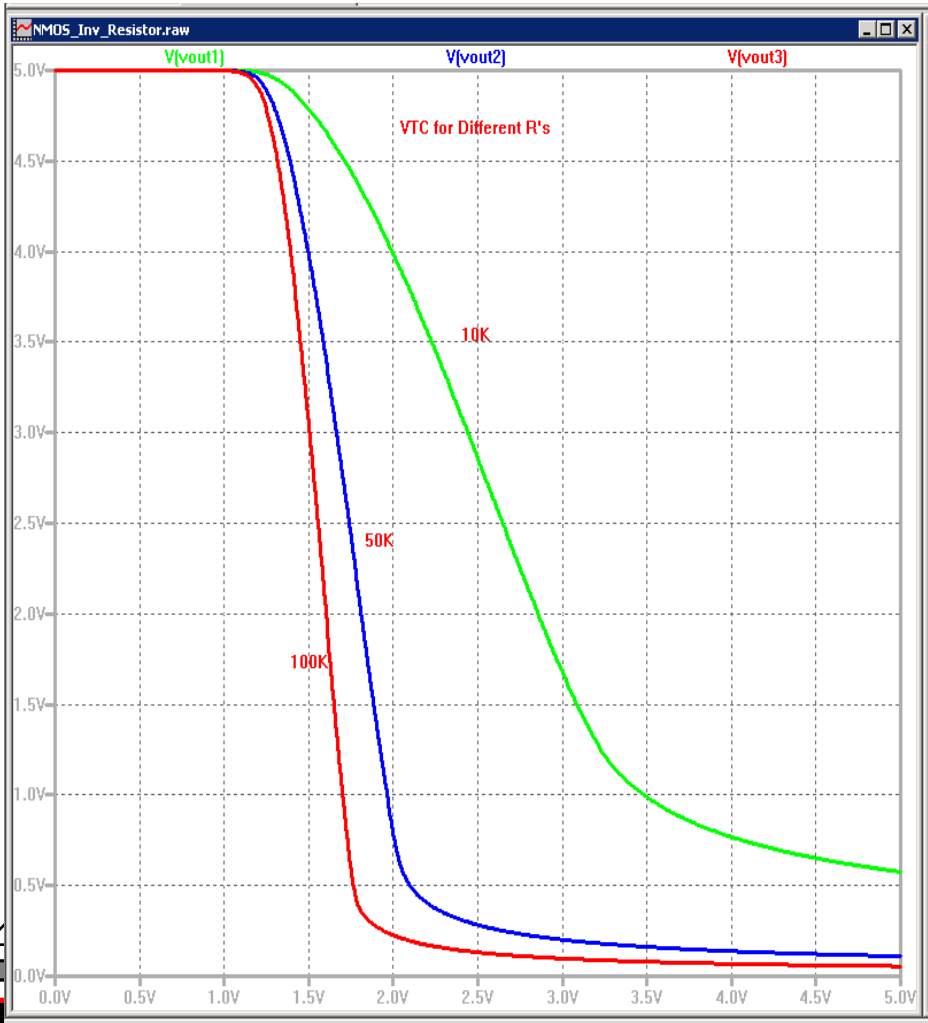


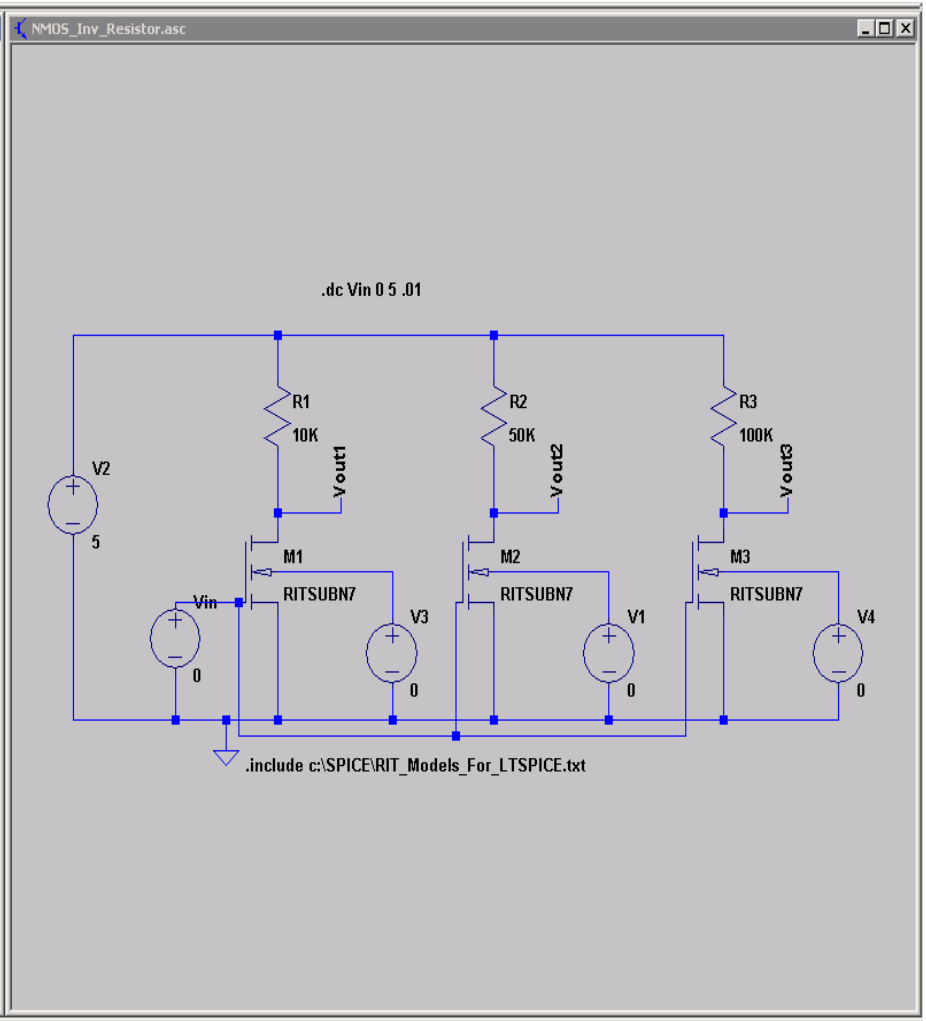
$$f0 = \frac{1}{2\Pi\sqrt{LC}}$$

NMOS INVERTER WITH RESISTER LOAD

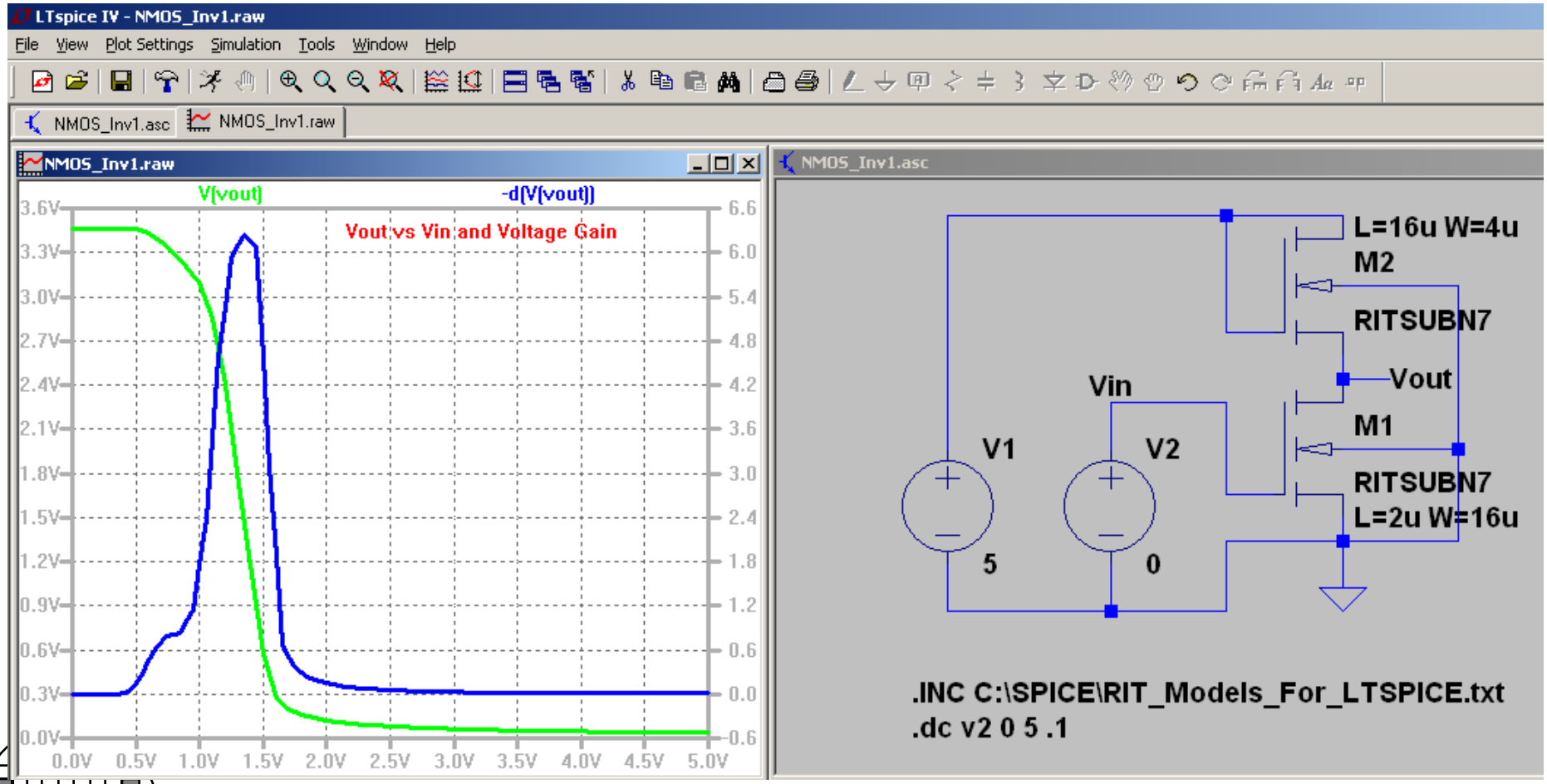


NMOS INVERTER RESISTIVE LOADS





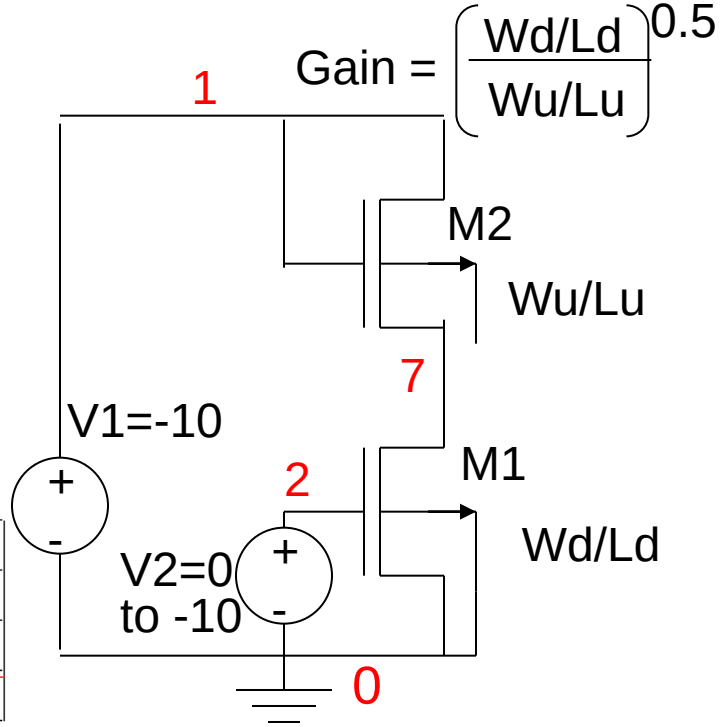
NMOS INVERTER WITH NMOS LOAD

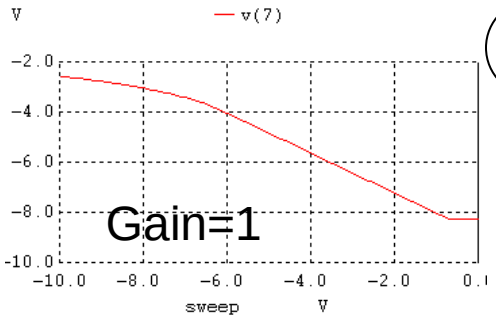


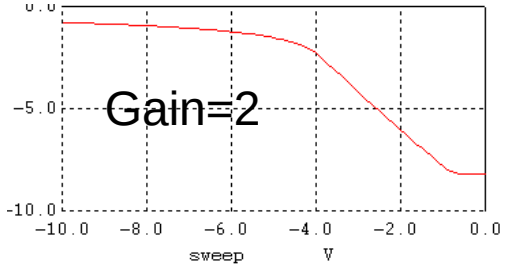
PMOS INVERTER WITH PMOS LOAD

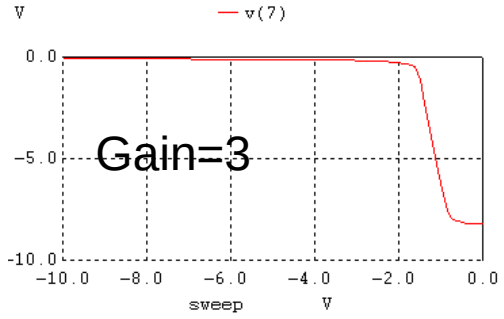
```
INVERTER USING RIT PMOSFET, Dr. Lynn Fuller, 2-11-2007
*LINE ABOVE IS TITLE
*
*START WIN SPICE AND ENTER LOCATION AND NAME OF INPUT FILE
*THIS FILE IS PMOS_INVERTER.TXT
*EXAMPLE: winspice> source c:/spice/PMOS_INVERTER.txt
*
*THE TRANSISTOR MODELS ARE IN THE FILE NAMED BELOW
.INCLUDE E:\SPICE\WINSPICE\RIT_MICROE_MODELS.TXT
*
*CIRCUIT DESCRIPTION
*
*VOLTAGE SOURCES
V1 1 0 DC -10
V2 2 0 DC 0
*
*TRANSISTORS
M1 7 2 0 0 RITPMOS49 L=20U W=60U
M2 1 1 7 0 RITPMOS49 L=60U W=20U
*
*REQUESTED ANALYSIS
.OP
.DC V2 0 -10 -0.1
.PLOT DC V(7)
*
.END
```

$$\text{Gain} = \left(\frac{Wd/Ld}{Wu/Lu}\right)^{0.5}$$

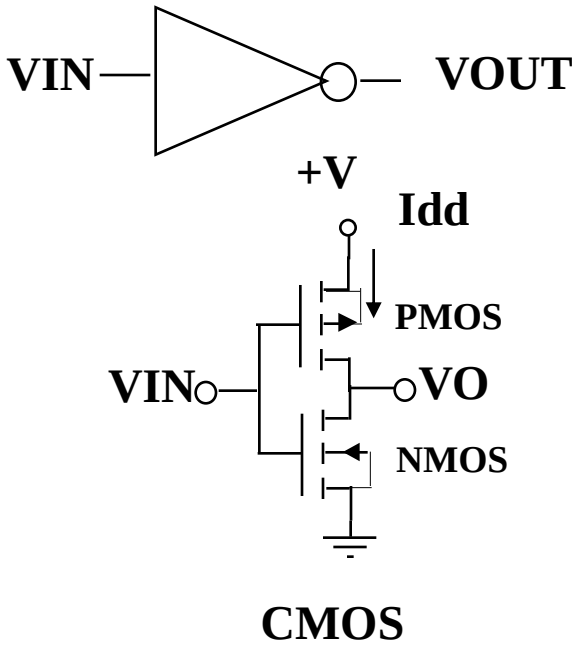


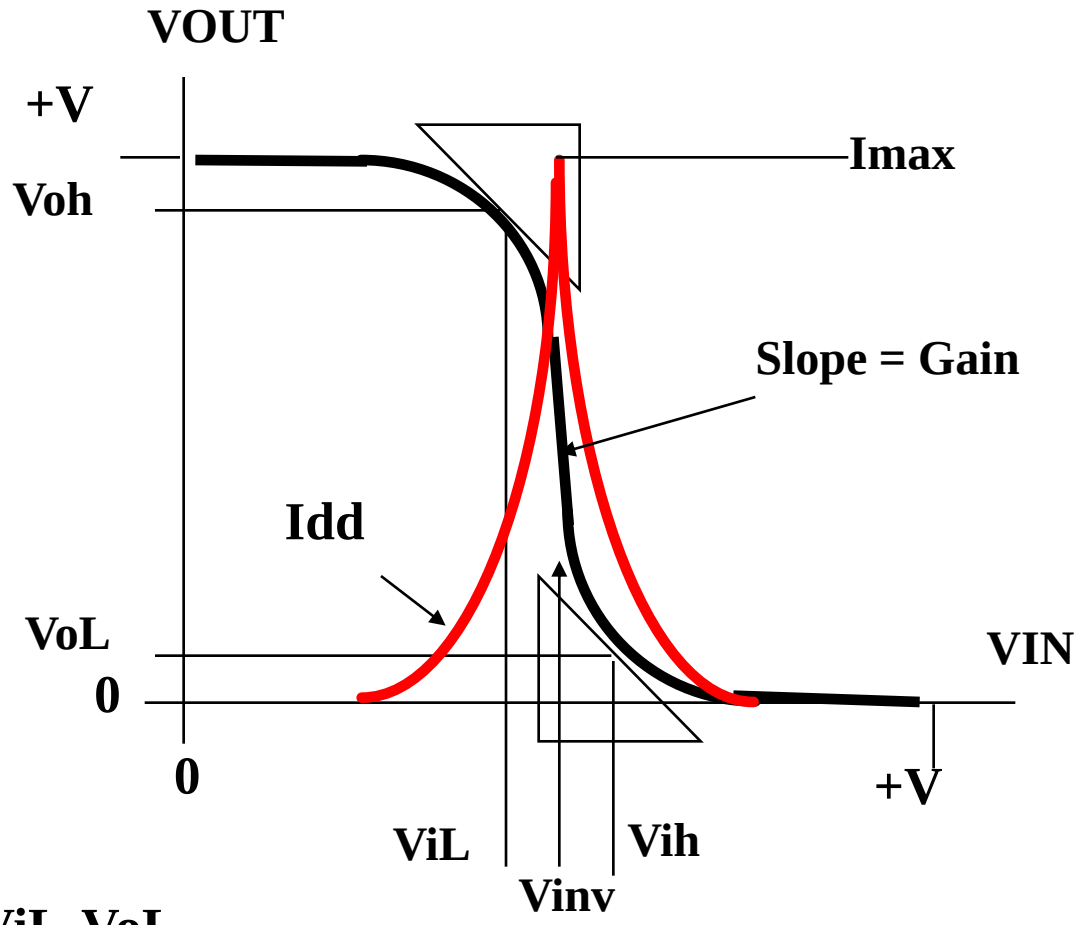






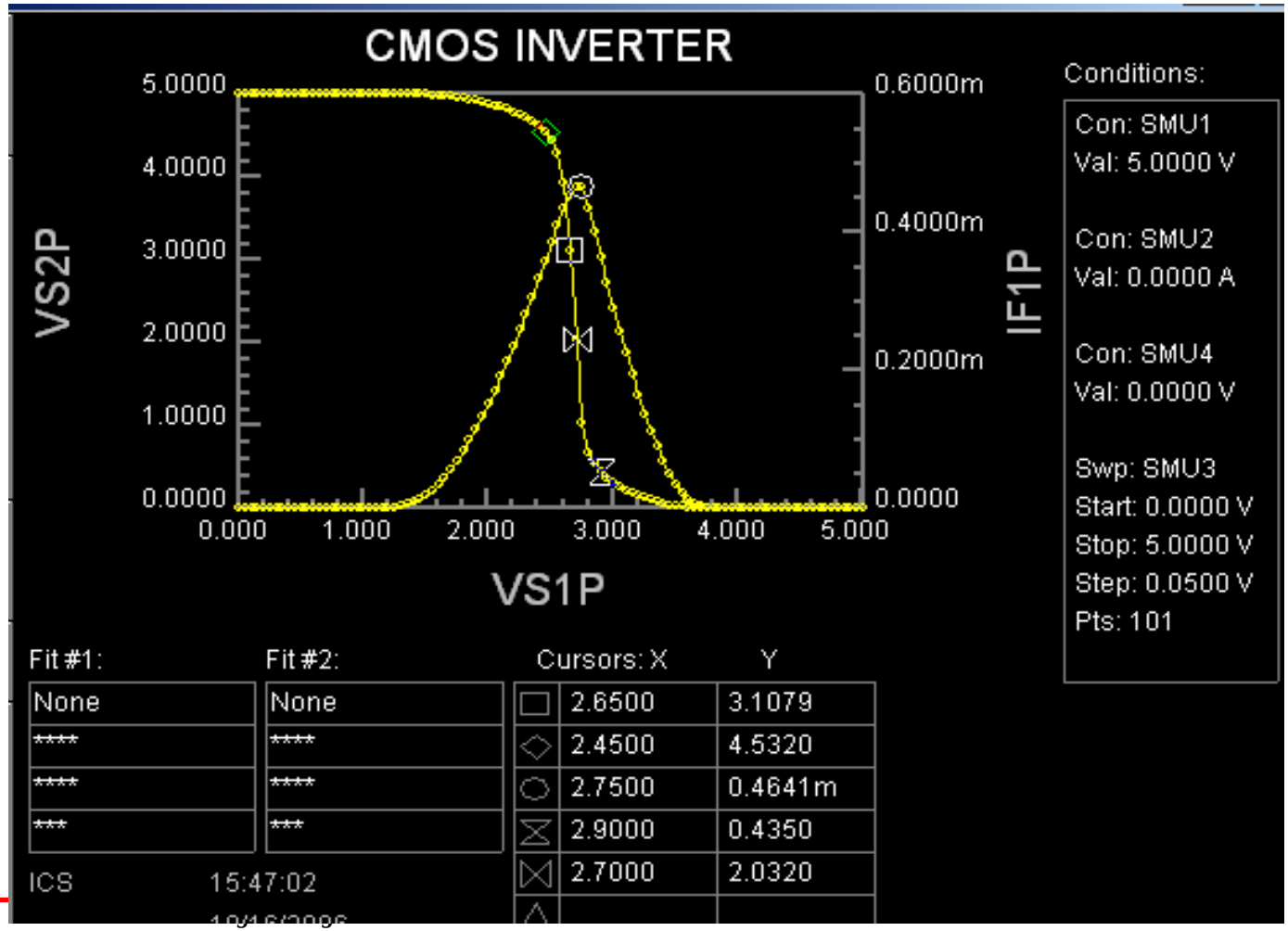
CMOS INVERTER VOUT VS VIN (VTC)



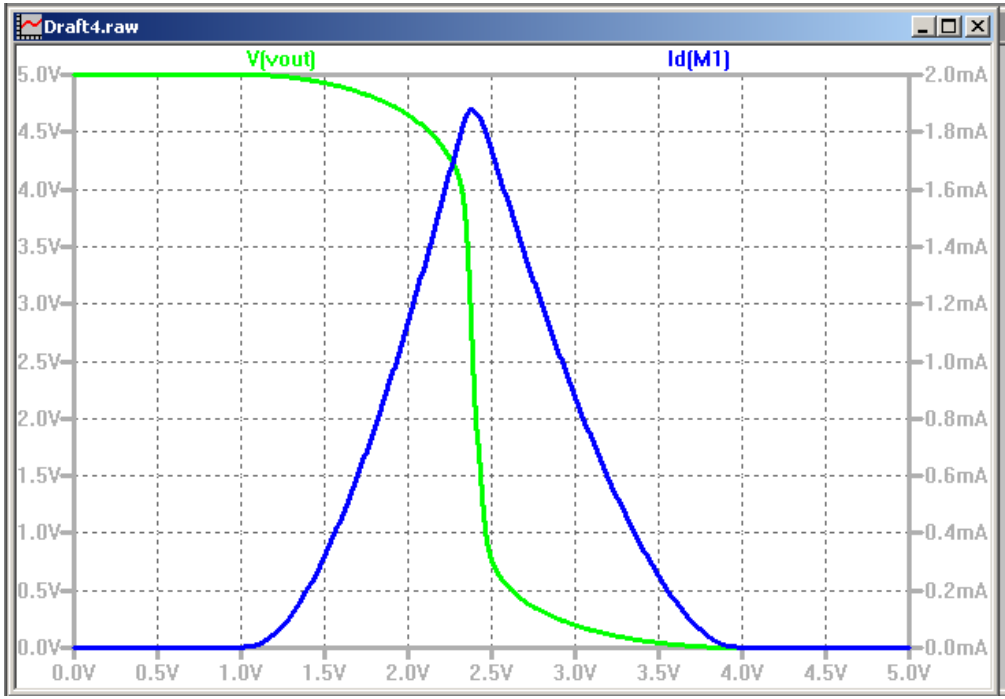


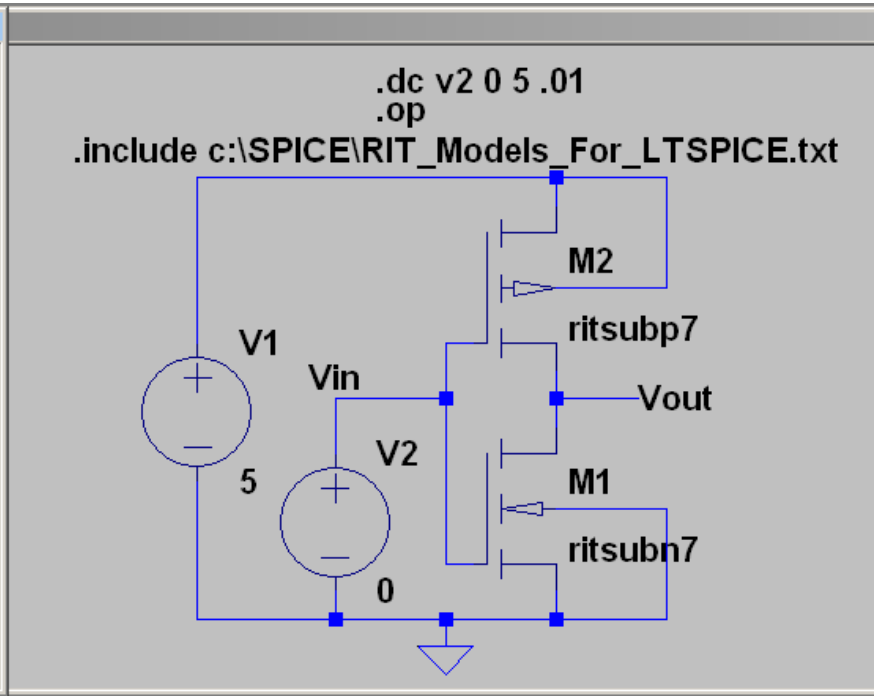
Δ0 noise margin=ViL-VoL
Δ1 noise margin=VoH-ViH

MEASURED CMOS INVERTER VOUT & I VS VIN



DC SIMULATION OF INVERTER VOUT & I VS VIN

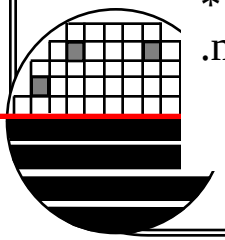




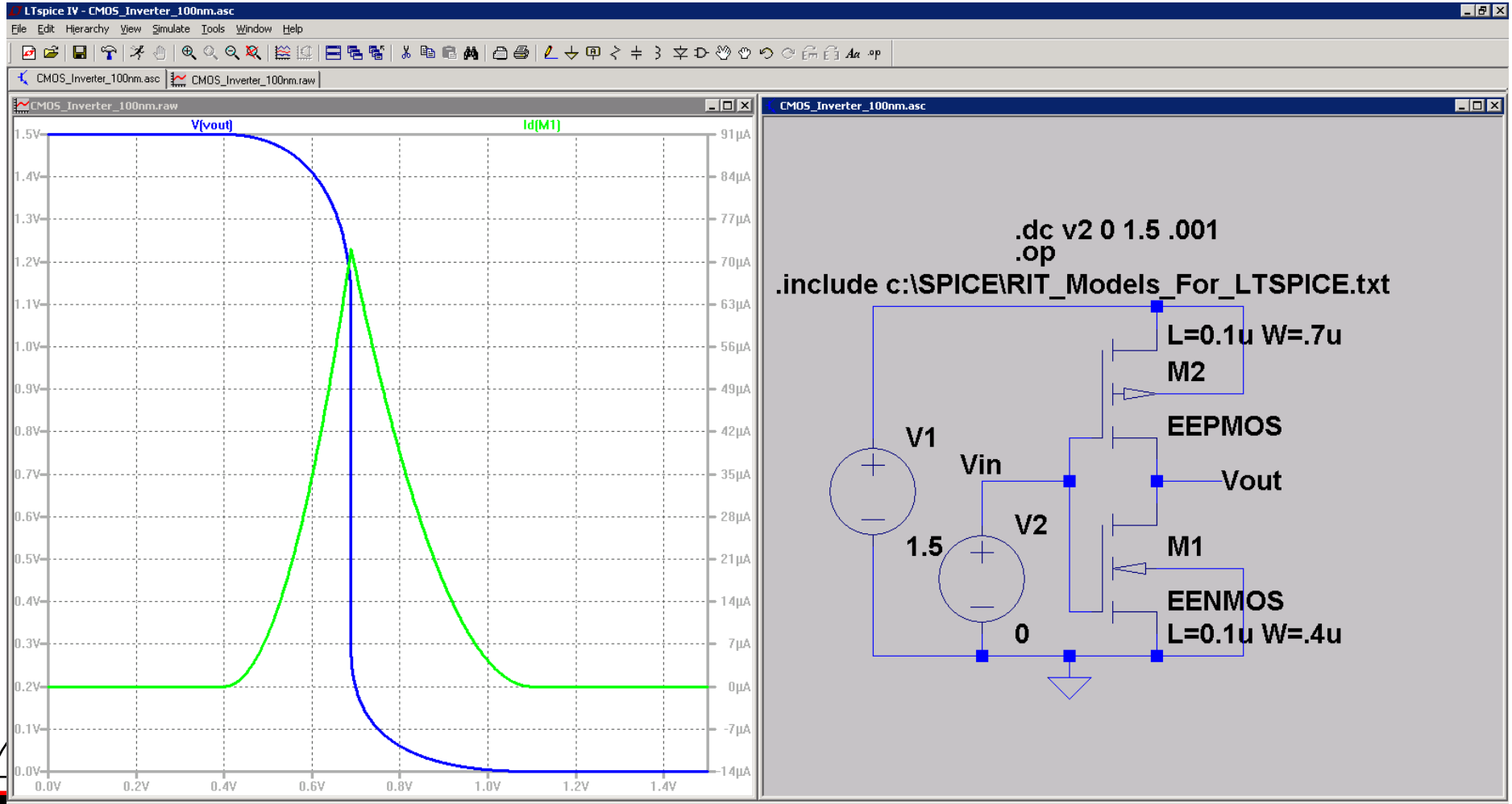
What happens to the voltage transfer curve (VTC) and noise margins when one of the threshold voltages is changed by 0.3 volts? What happens when width of transistors is changed.

SIMPLE AND ADVANCED SPICE MODEL

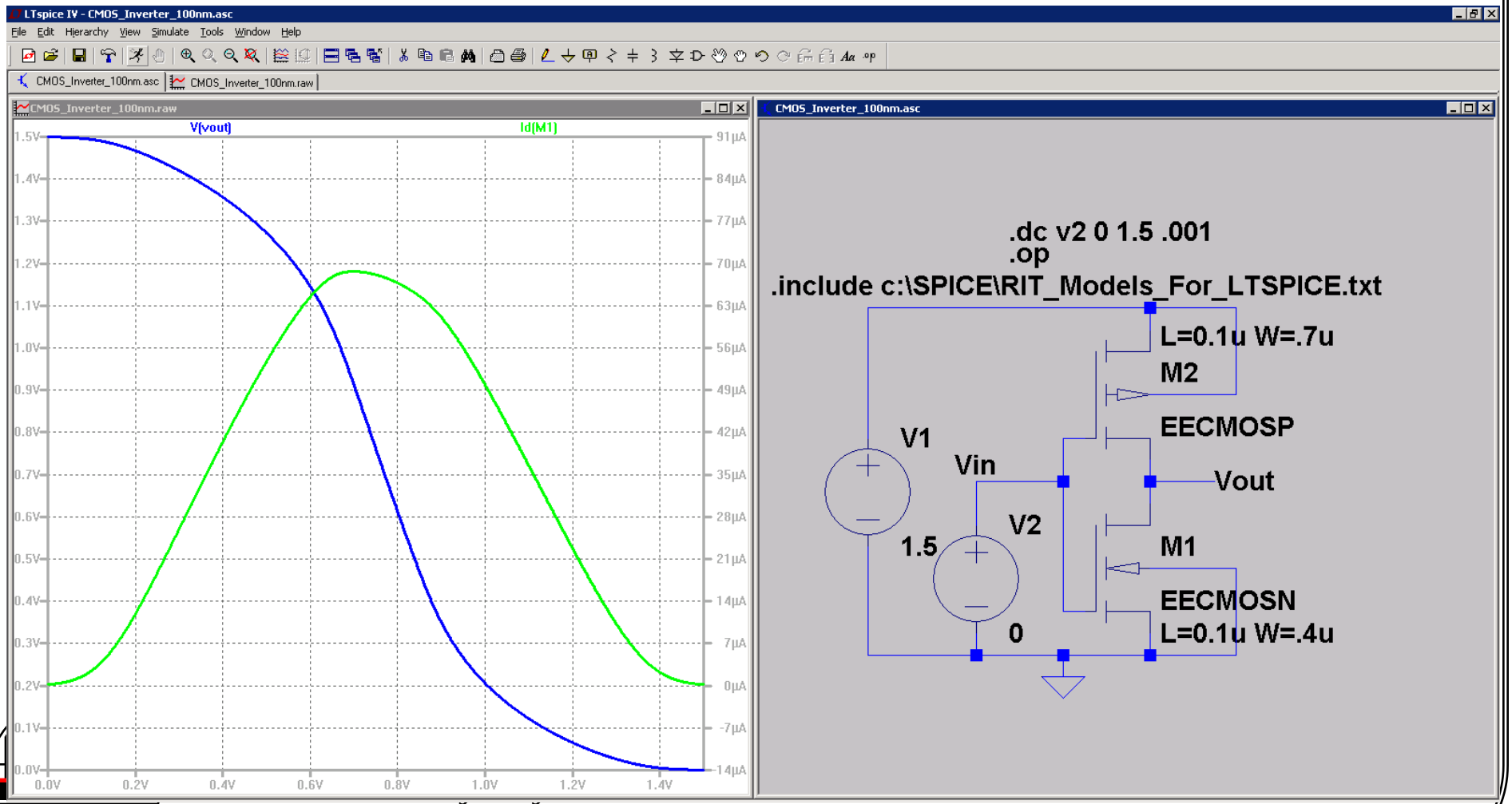
```
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSN     NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSP      PMOS (LEVEL=8
+TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
* From Electronics II EEEE482 SIMPLE MODEL
.model EENMOS       NMOS (VTO=0.4 KP=432E-6 GAMMA=0.2 PHI=.88)
*
* From Electronics II EEEE482 SIMPLE MODEL
.model EEPMOS       PMOS (VTO=-0.4 KP=122E-6 GAMMA=0.2 PHI=.88)
```



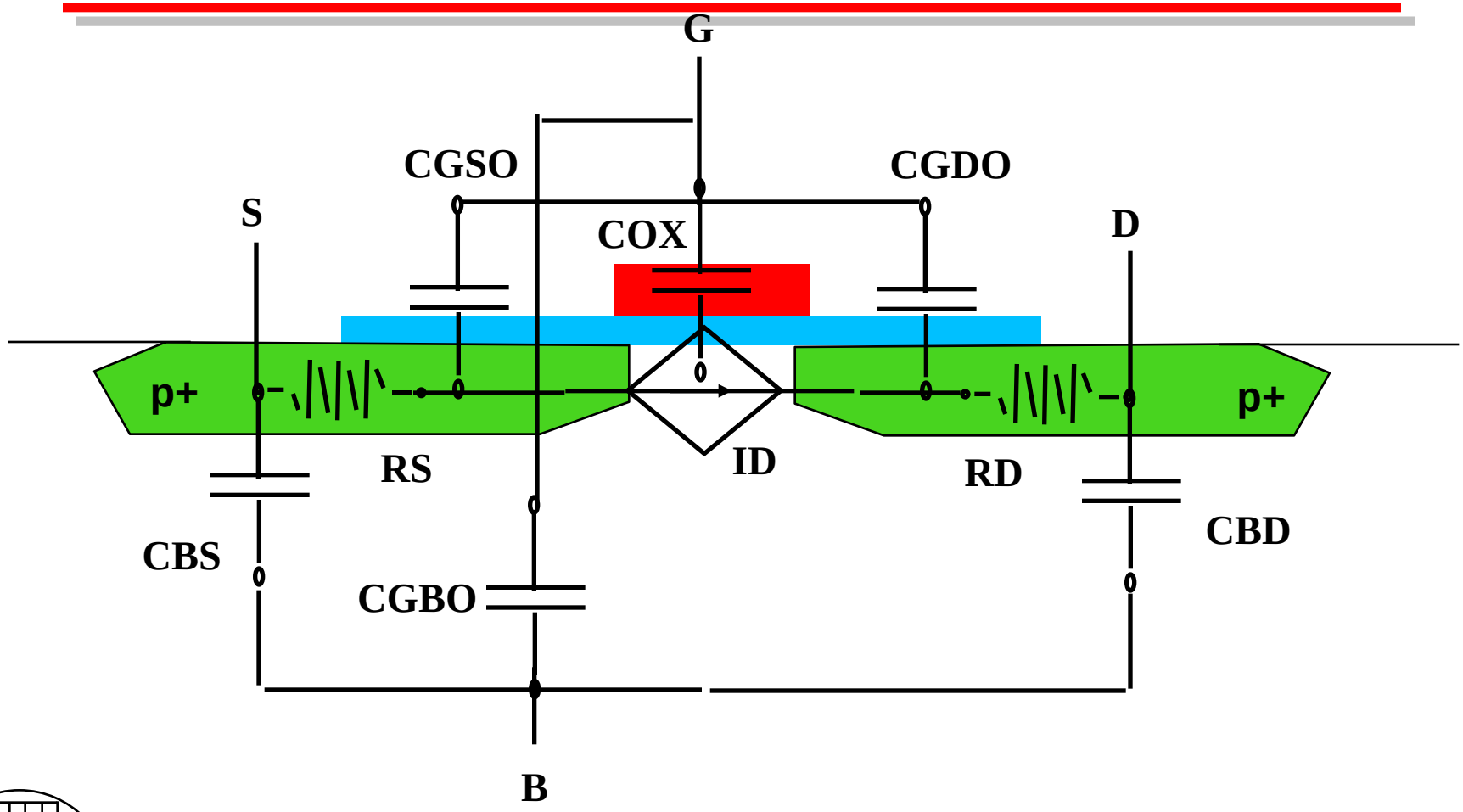
CMOS INVERTER WITH LEVEL 1 SPICE MODEL



CMOS INVERTER WITH LEVEL 8 SPICE MODEL



SPICE LEVEL-1 MOSFET MODEL



where ID is a dependent current source using simple long channel equations.

AC MODEL FOR MOSFETS

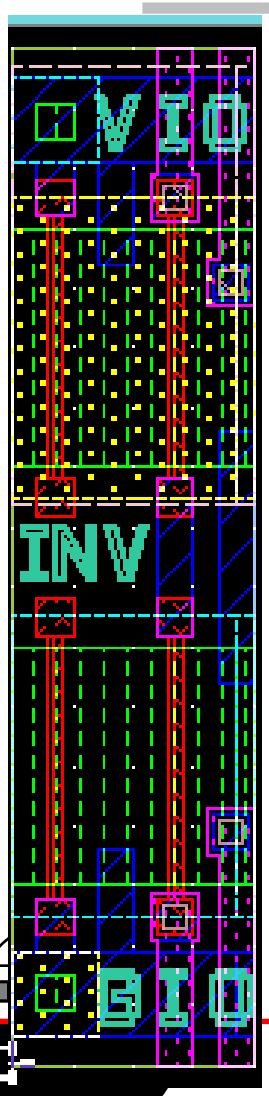
The SPICE model parameters that effect the AC response of a MOSFET are the resistance and capacitance parameters shown here:

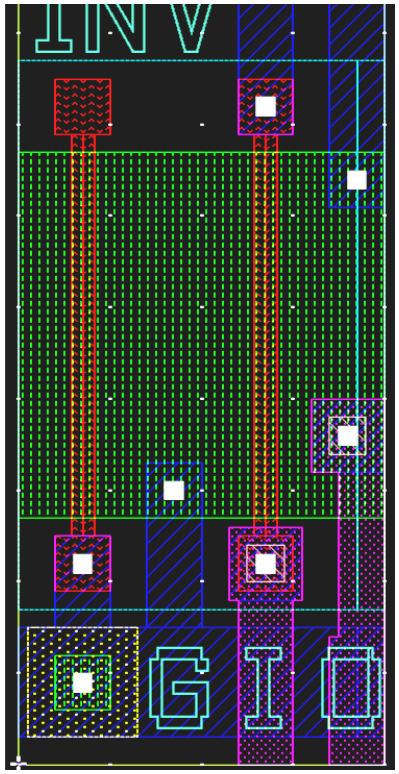
RS,RS	Source/Drain Series Resistance, ohms
RSH	Sheet Resistance of Drain/Source, ohms
CGSO,CGDO	Zero Bias Gate-Source/Drain Capacitance, F/m of width
CGBO	Zero Bias Gate-Substrate Capacitance, F/m of length
CJ	DS Bottom Junction Capacitance, F/m2
CJSW	DS Side Wall Junction Capacitance, F/m of perimeter
MJ	Junction Grading Coefficient, 0.5
MJSW	Side Wall Grading Coefficient, 0.5

These are combined with the transistors properties to obtain the internal resistance and capacitance values for each transistor.

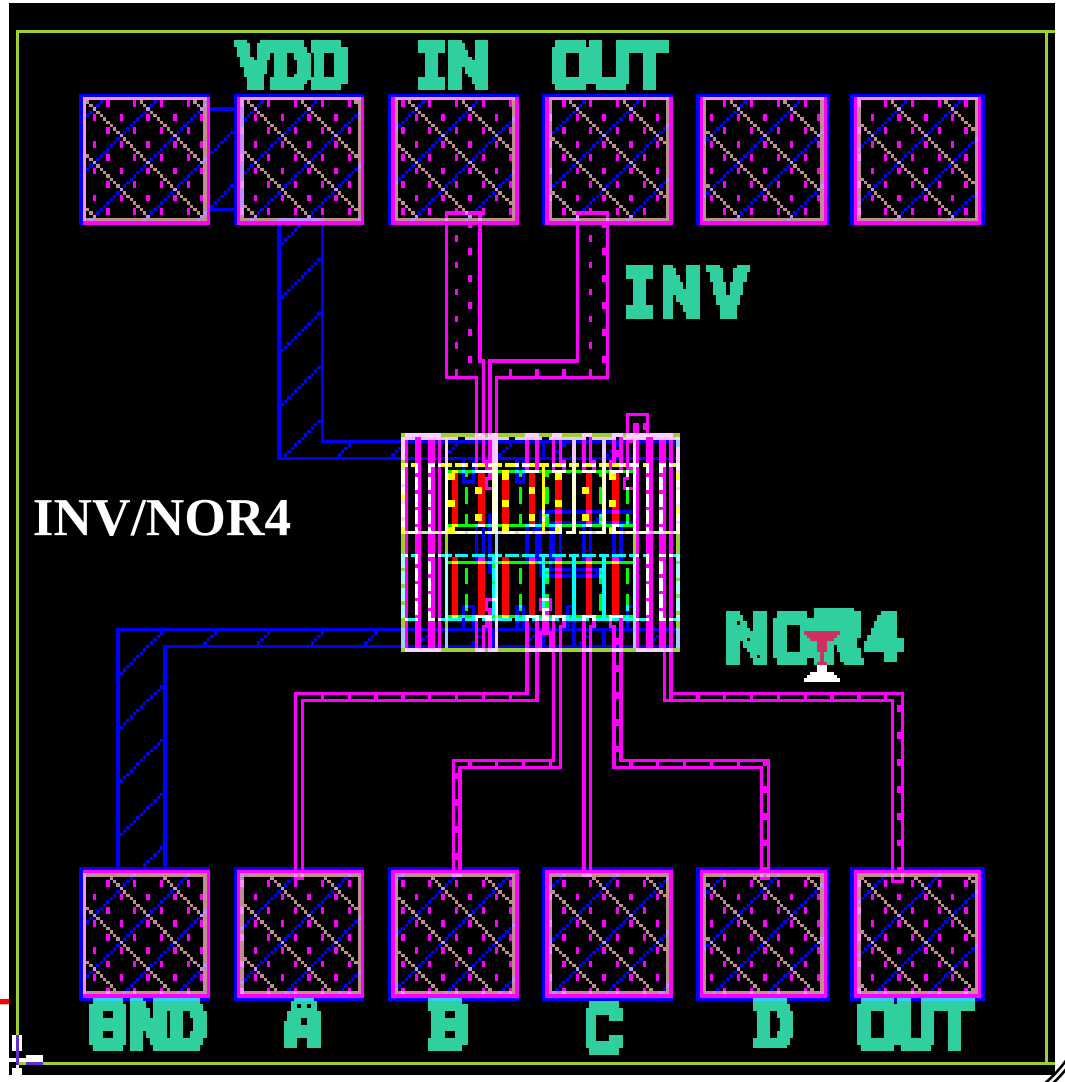
L, W	Length and Width
AS,AD	Area of the Source/Drain
PS,PD	Perimeter of the Source/Drain
NRS,NRD	Number of squares Contact to Channel

INVERTER LAYOUT





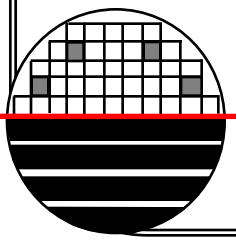
W = 40 µm
Ldrawn = 2.5µm
Lpoly = 1.5µm
Leff = 1.0 µm\
Pd=680p
Ad=114u



FIND DIMENSIONS OF THE TRANSISTORS

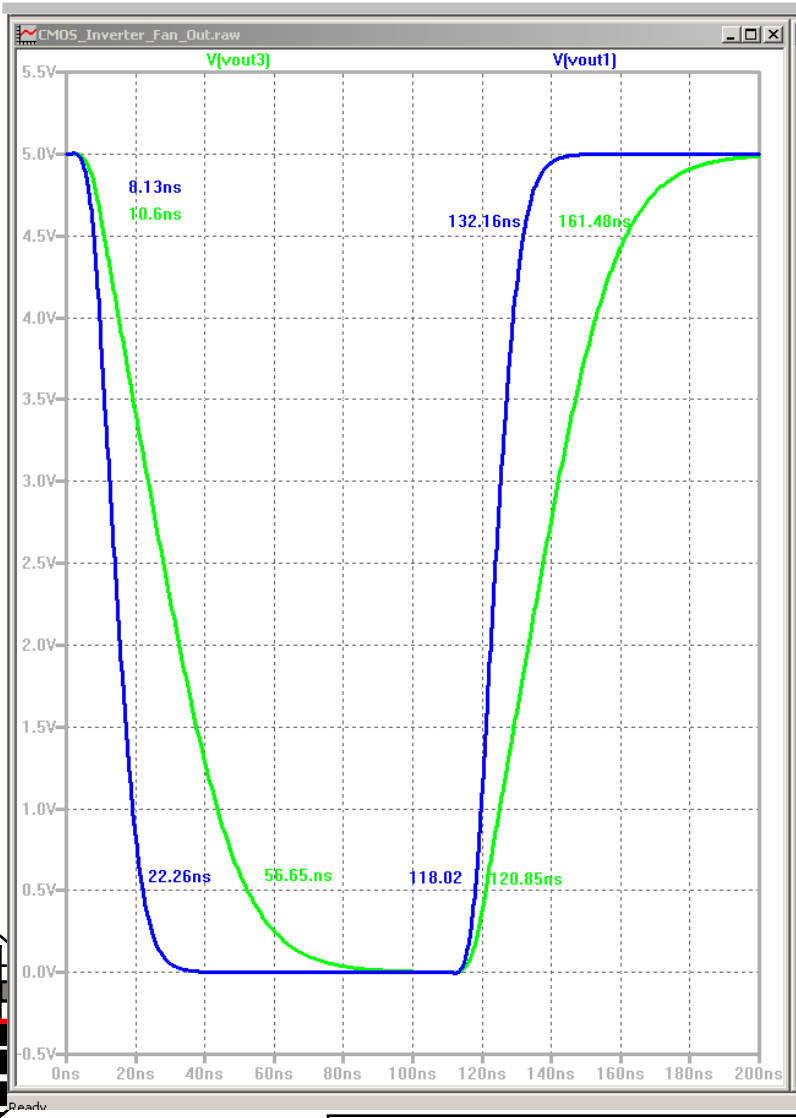
Inverter

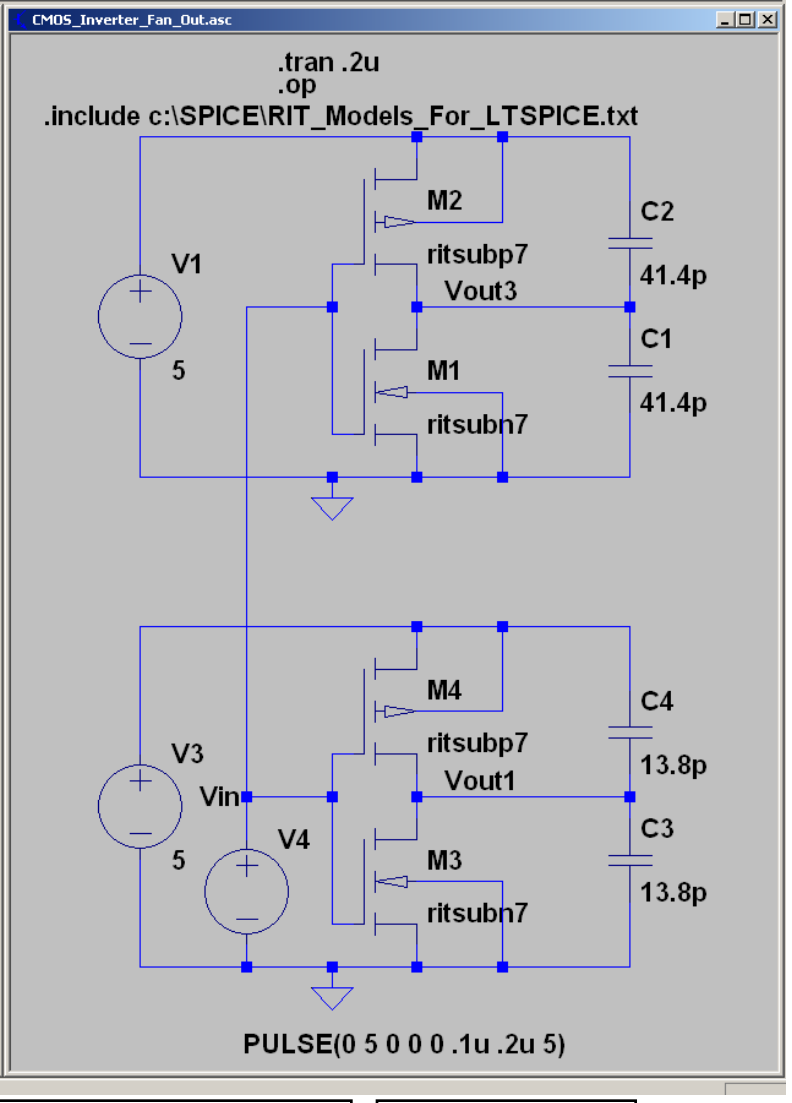
	NMOS	PMOS
L	1.5u	1.5u
W	40u	40u
AD	17ux40u=680p	17ux40u=680p
AS	17ux40u=680p	17ux40u=680p
PD	2x(17u+40u)=114u	2x(17u+40u)=114u
PS	2x(17u+40u)=114u	2x(17u+40u)=114u



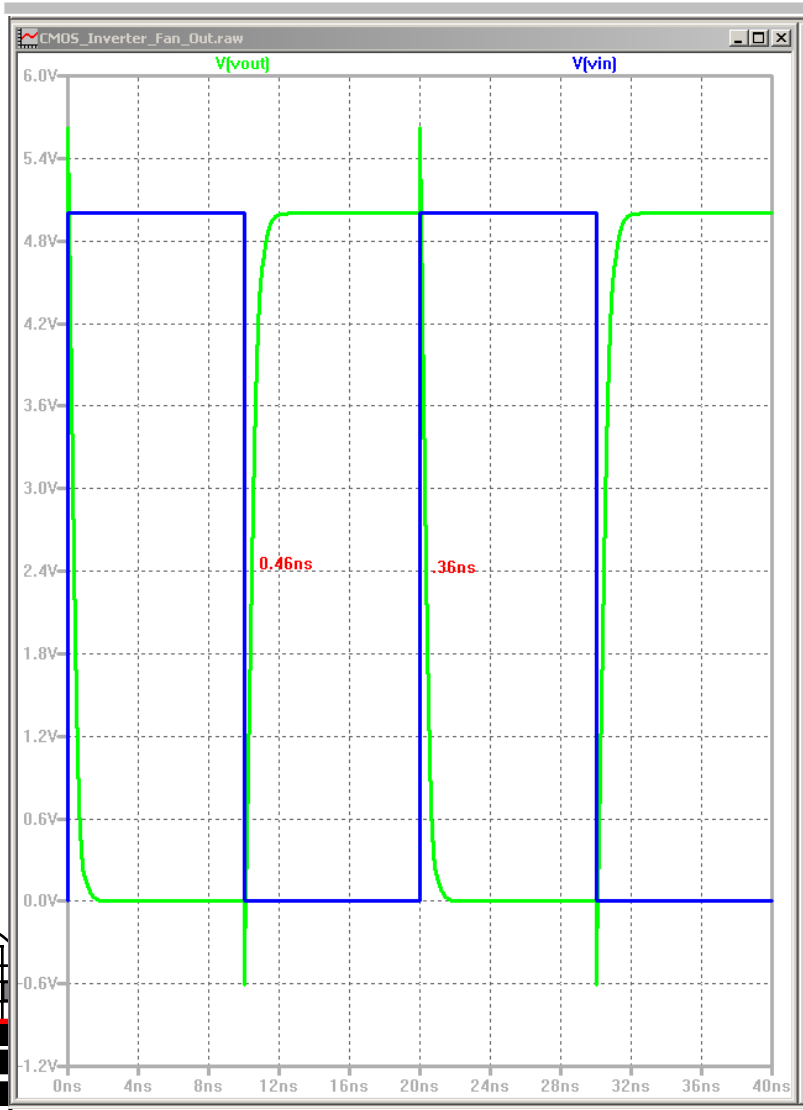
Right mouse click on each transistor and add these values to the properties.

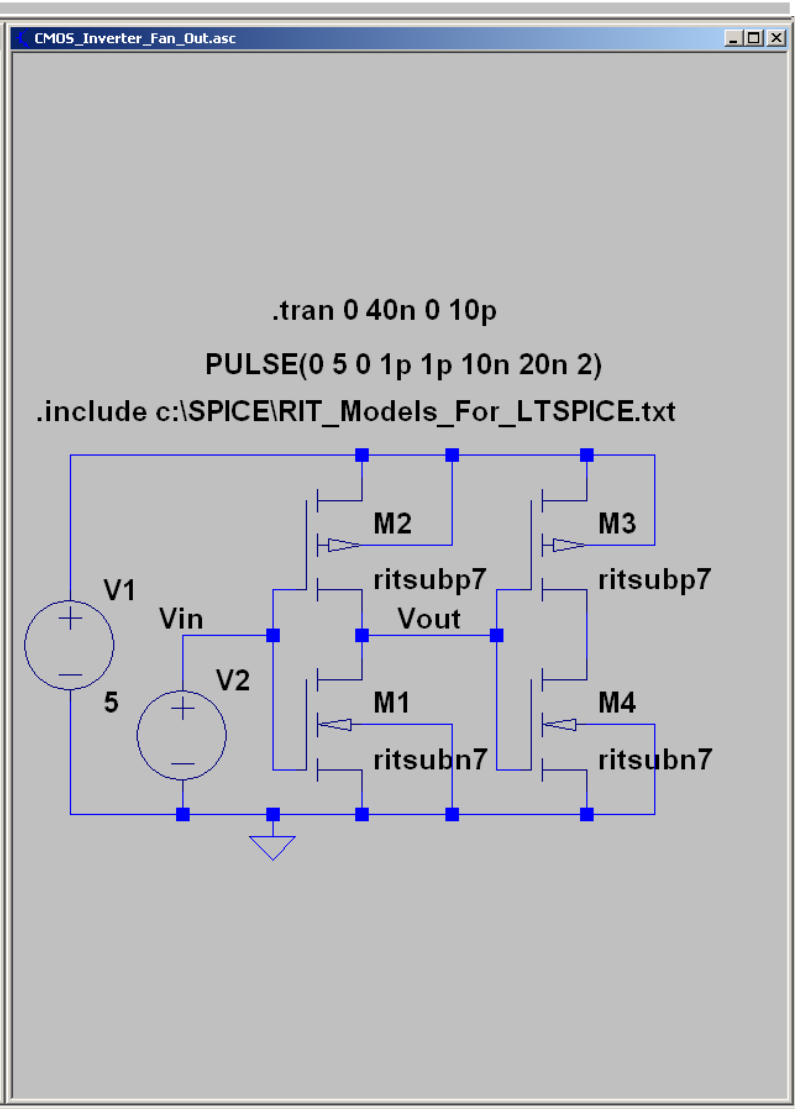
RISE TIME AND FALL TIME LTSPICE SIMULATION





SIMULATION OF GATE DELAY IN SINGLE INVERTER



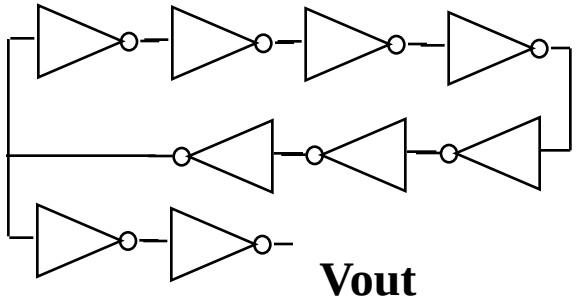


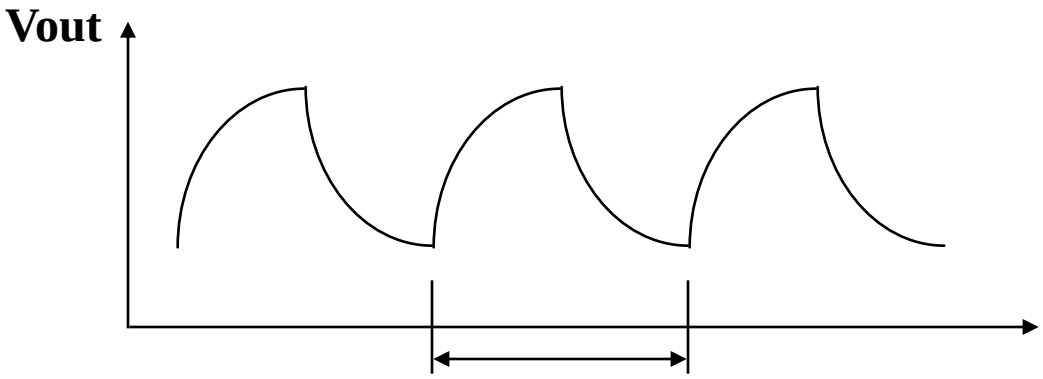
RING OSCILLATOR, td, THEORY

Seven stage ring oscillator with two output buffers

td = T / 2 N

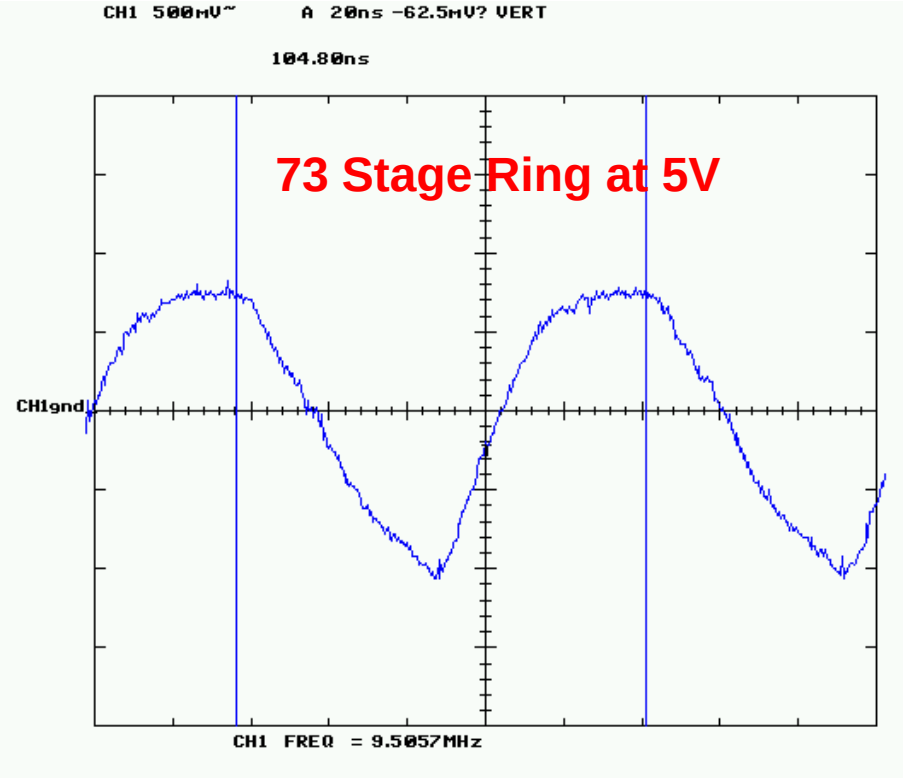
td = gate delay
N = number of stages
T = period of oscillation

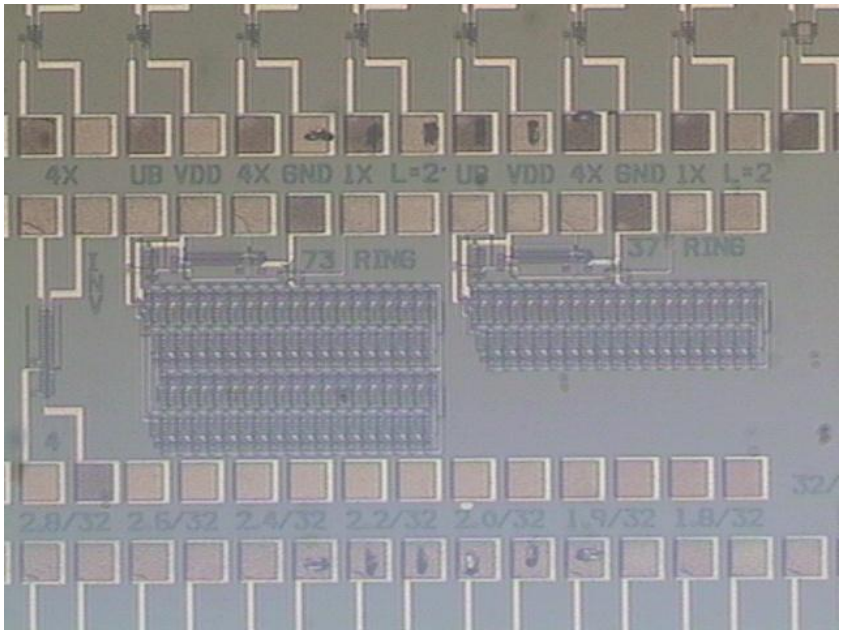




T = period of oscillation

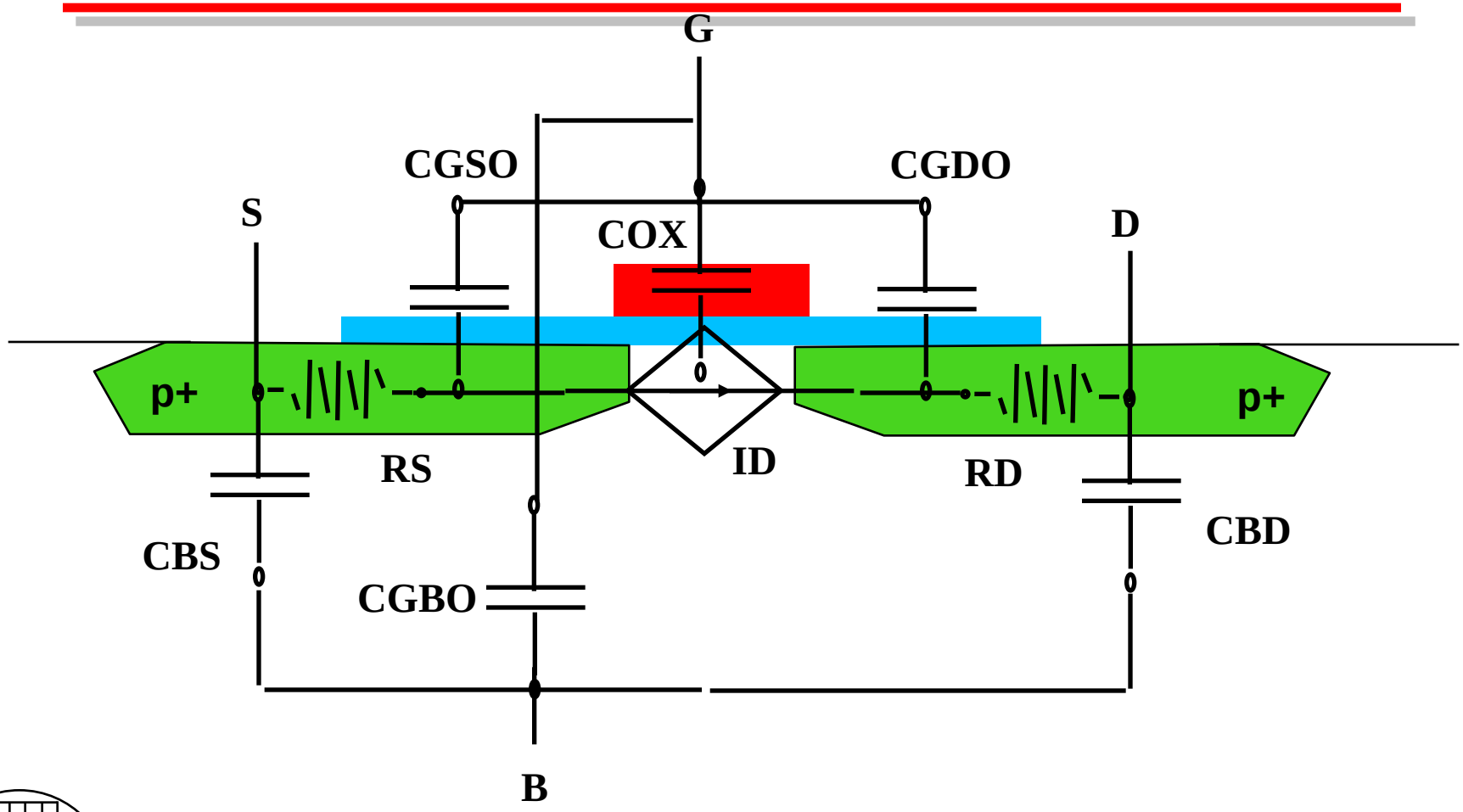
MEASURED RING OSCILLATOR OUTPUT





td = 104.8ns / 2(73) = 0.718 ns

SPICE LEVEL-1 MOSFET MODEL



where ID is a dependent current source using simple long channel equations.

AC MODEL FOR MOSFETS

The SPICE model parameters that effect the AC response of a MOSFET are the resistance and capacitance parameters shown here:

RS,RS	Source/Drain Series Resistance, ohms
RSH	Sheet Resistance of Drain/Source, ohms
CGSO,CGDO	Zero Bias Gate-Source/Drain Capacitance, F/m of width
CGBO	Zero Bias Gate-Substrate Capacitance, F/m of length
CJ	DS Bottom Junction Capacitance, F/m2
CJSW	DS Side Wall Junction Capacitance, F/m of perimeter
MJ	Junction Grading Coefficient, 0.5
MJSW	Side Wall Grading Coefficient, 0.5

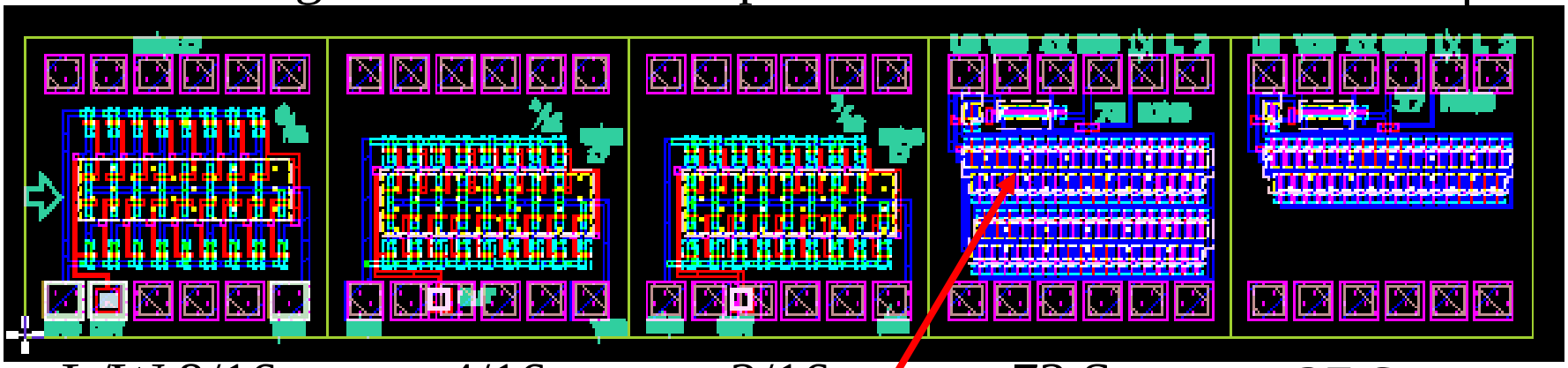
These are combined with the transistors properties to obtain the internal resistance and capacitance values for each transistor.

L, W	Length and Width
AS,AD	Area of the Source/Drain
PS,PD	Perimeter of the Source/Drain
NRS,NRD	Number of squares Contact to Channel

RING OSCILLATOR LAYOUTS

17 Stage Un-buffered Output

L/W=2/30 Buffered Output



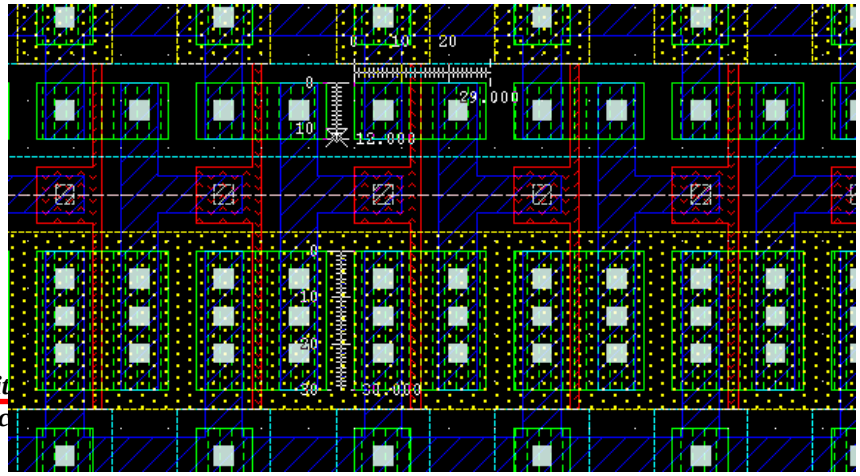
L/W 8/16

4/16

2/16

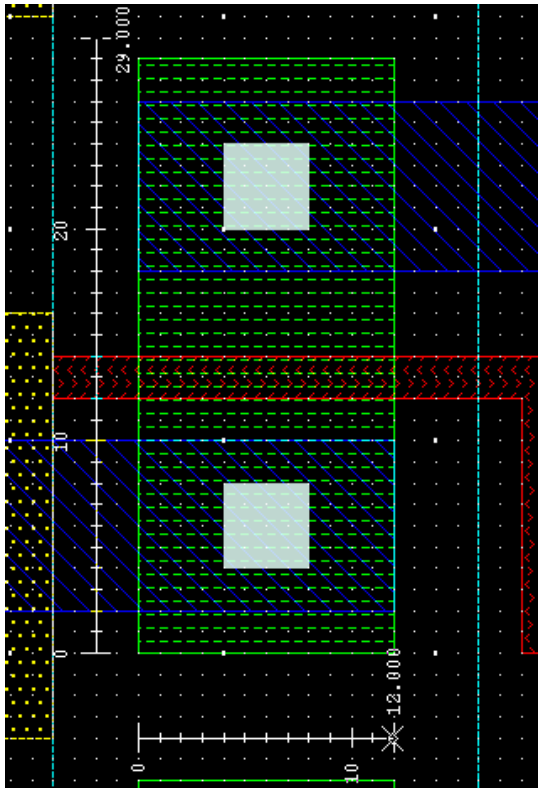
73 Stage

37 Stage

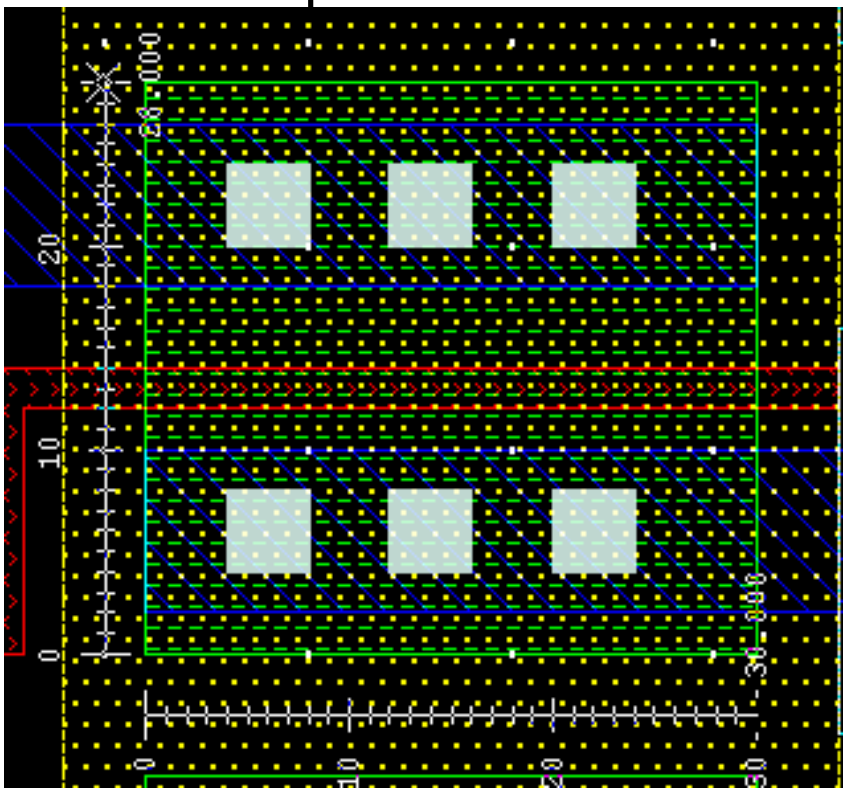


MOSFETS IN THE INVERTER OF 73 RING OSCILLATOR

nmosfet



pmosfet

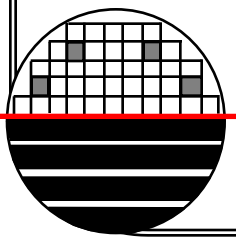


73 Stage Ring Oscillator

FIND DIMENSIONS OF THE TRANSISTORS

	NMOS	PMOS
L	2u	2u
W	12u	30u
AD	12ux12u=144p	12ux30u=360p
AS	12ux12u=144p	12ux30u=360p
PD	2x(12u+12u)=48u	2x(12u+30u)=84u
PS	2x(12u+12u)=48u	2x(12u+30u)=84u
NRS	1	0.3
NRD	1	0.3

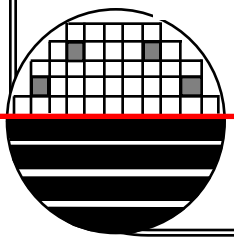
73 Stage



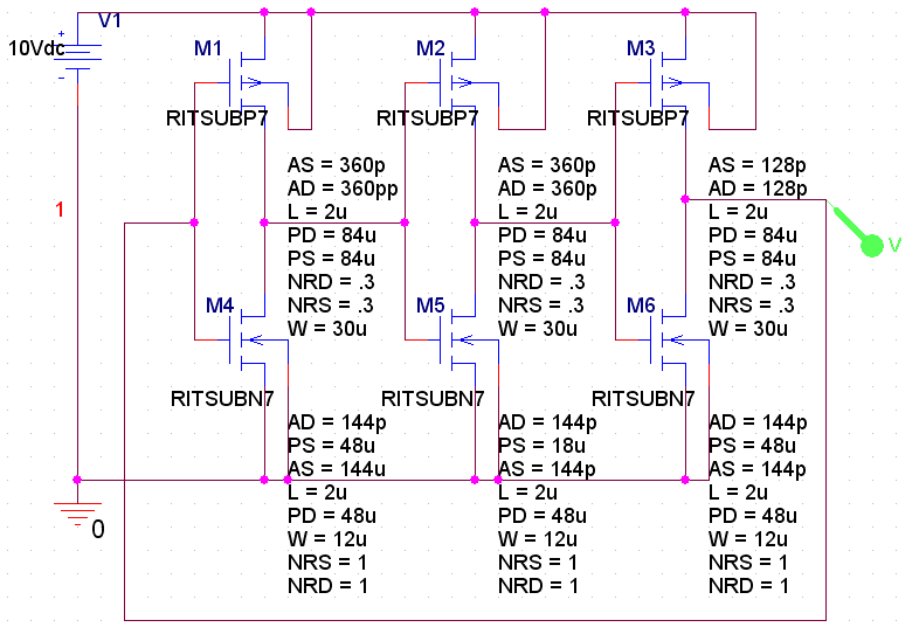
Right mouse click on each transistor and add these values to the properties.

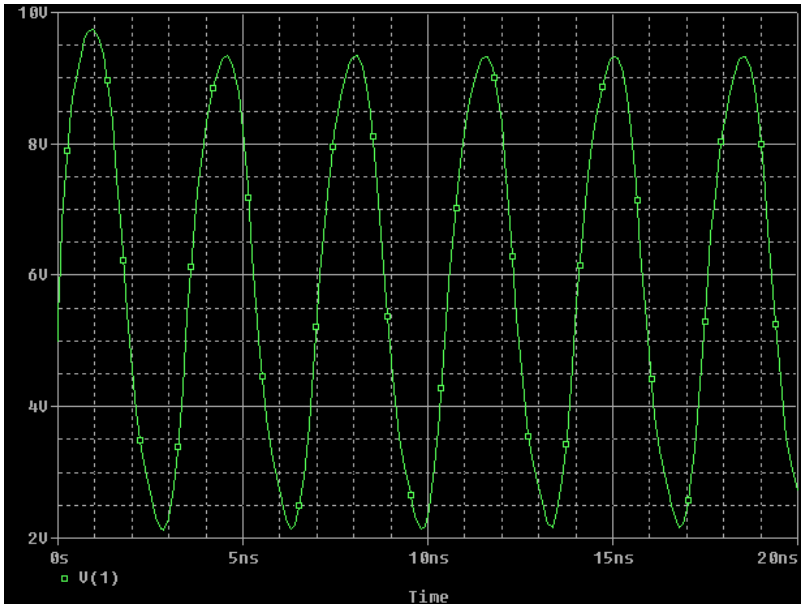
LEVEL = 7

```
*2-15-2009
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8 NSS=3E11
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=50 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*2-17-2009
.MODEL RITSUBP7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8 NSS=3E11 PCLM=5
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7 NGATE=5E20
+RSH=50 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



SIMULATED OUTPUT AT 10 VOLTS



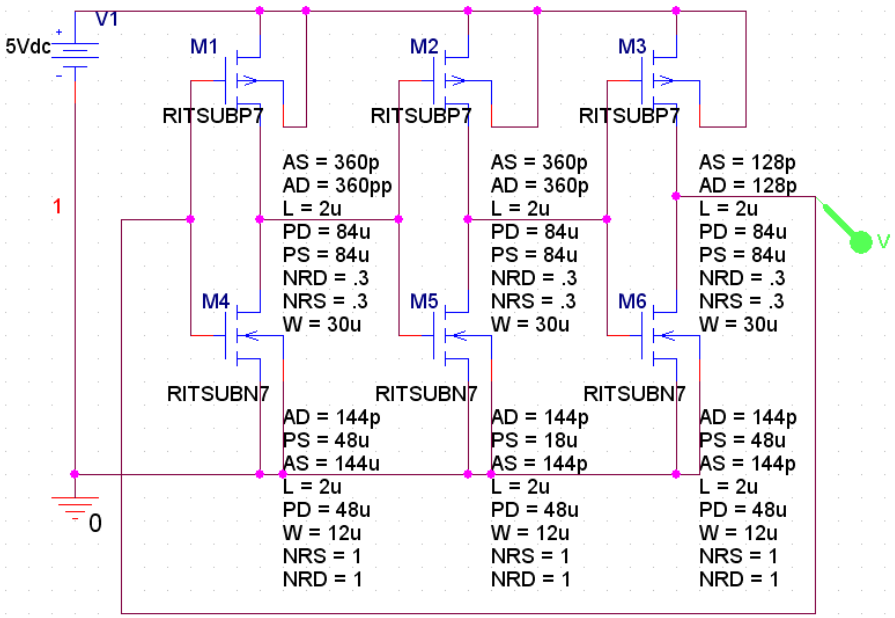


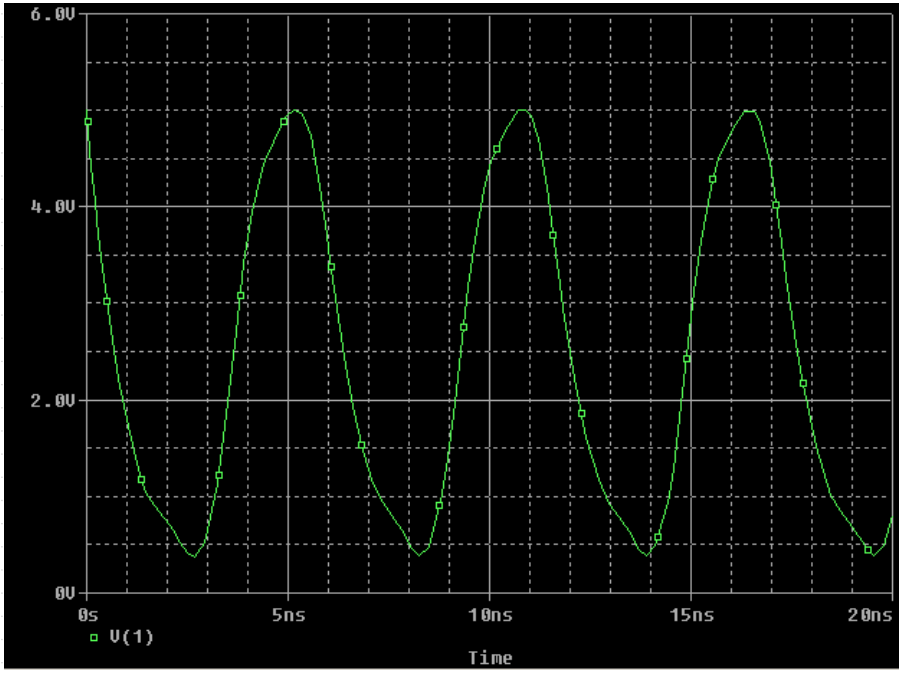
Three Stage Ring Oscillator with Transistor Parameters for 73 Stage Ring Oscillator and Supply of 10 volts

td = T / 2N = 3.5nsec / 2 / 3

td = 0.583 nsec

SIMULATED OUTPUT AT 5 VOLTS





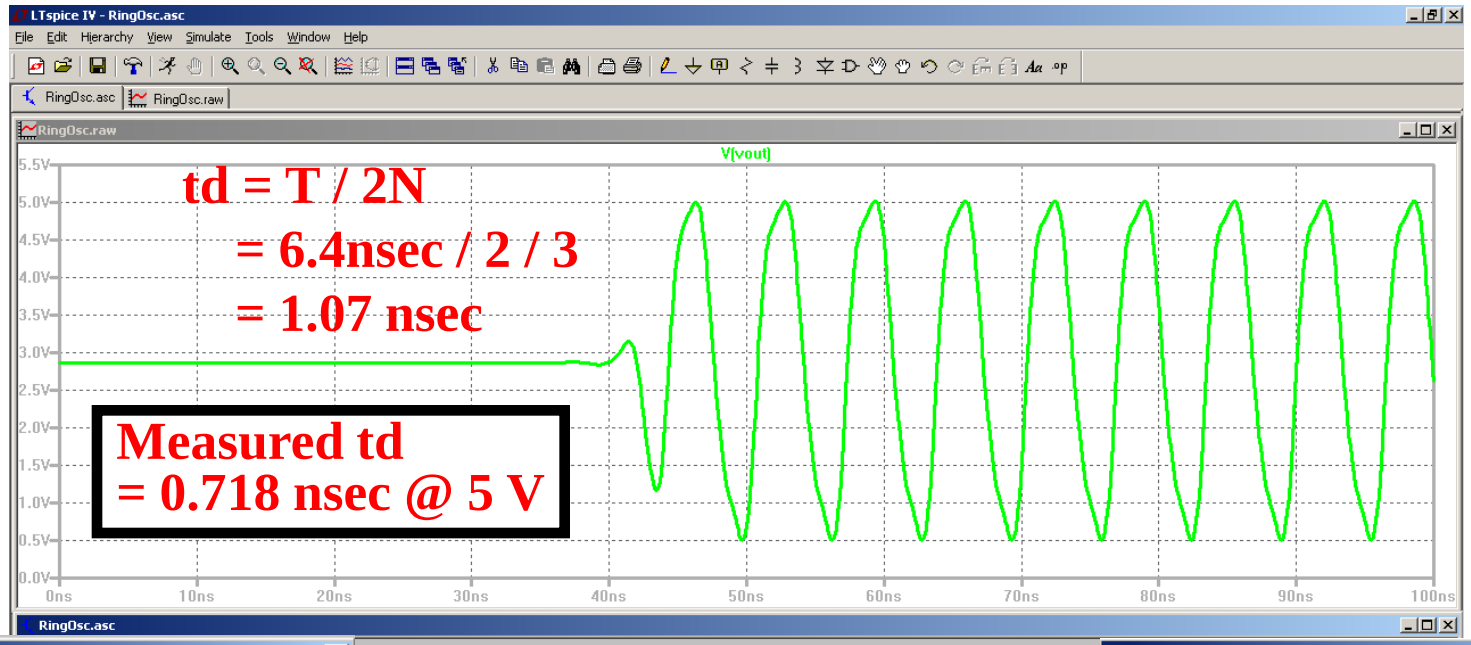
Three Stage Ring Oscillator with Transistor Parameters for 73 Stage Ring Oscillator and Supply of 5 volts

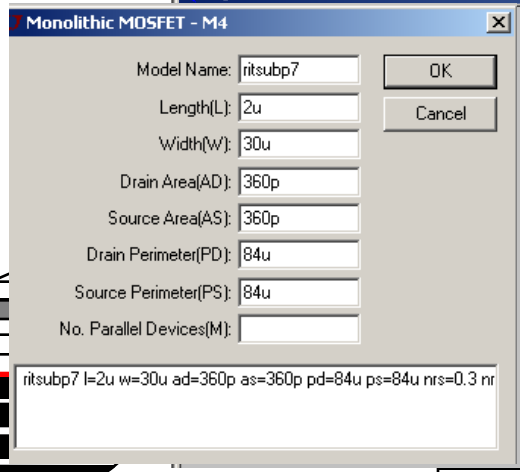
Measured td = 0.718 nsec @ 5 V

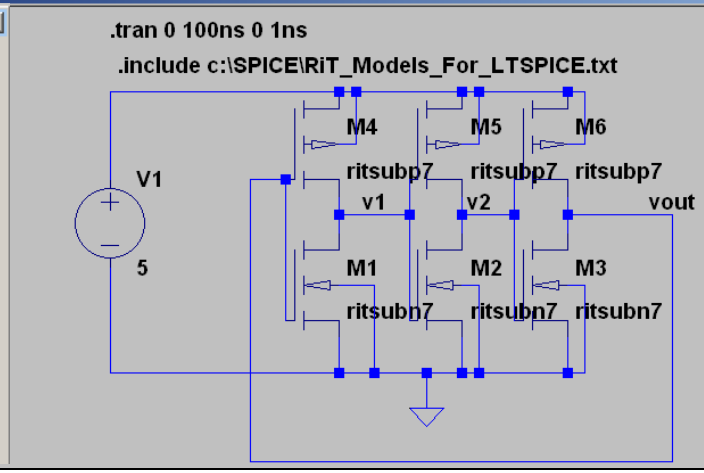
td = T / 2N = 5.5nsec / 2 / 3

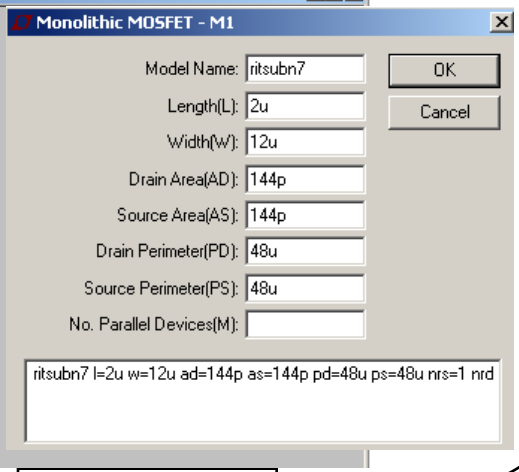
td = 0.92 nsec

RING OSCILLATOR USING LTSPICE









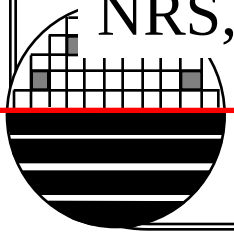
CONCLUSION

Since the measured and the simulated gate delays, td are close to correct, then the SPICE model must be close to correct. The inverter gate delay depends on the values of the internal capacitors and resistances of the transistor.

Specifically:
RS, RS, RSH
CGSO, CGDO, CGBO
CJ, CJSW

These are combined with the transistors

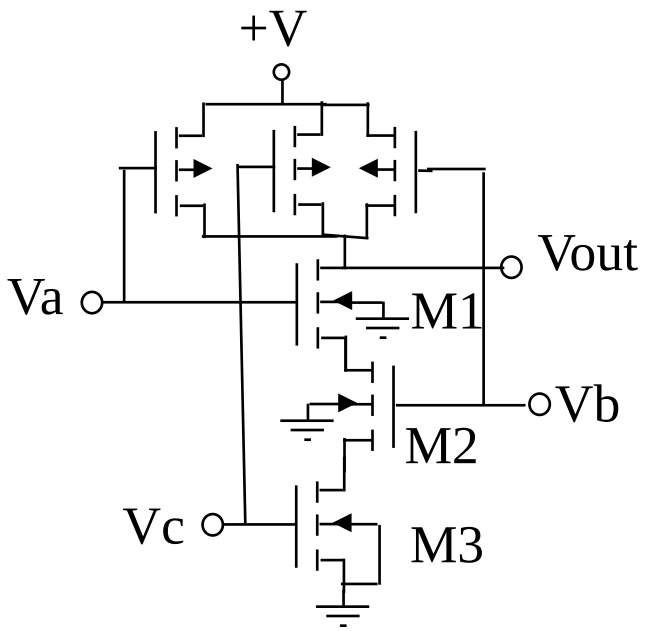
L, W	Length and Width
AS,AD	Area of the Source/Drain
PS,PD	Perimeter of the Source/Drain
NRS,NRD	Number of squares Contact to Channel



VTC FOR THREE INPUT NAND GATE

TRUTH TABLE

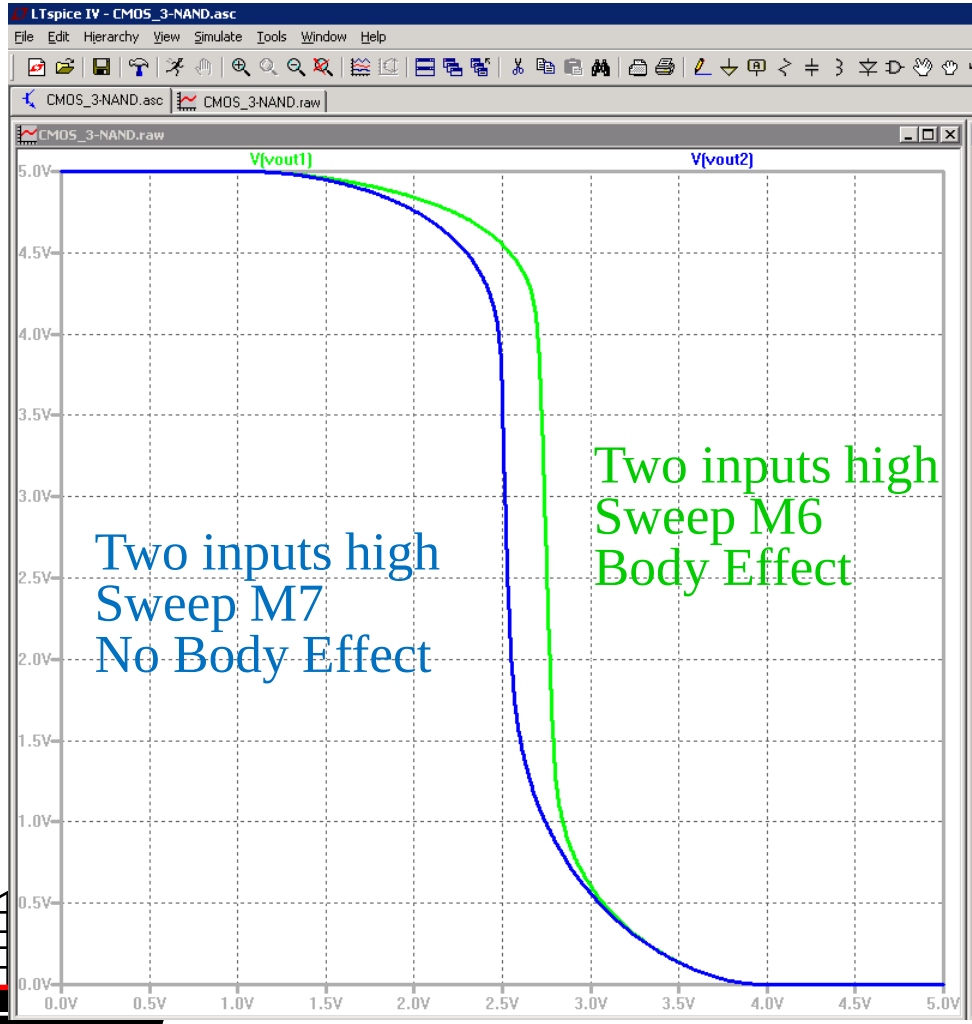
Va	Vb	Vc	Vout
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

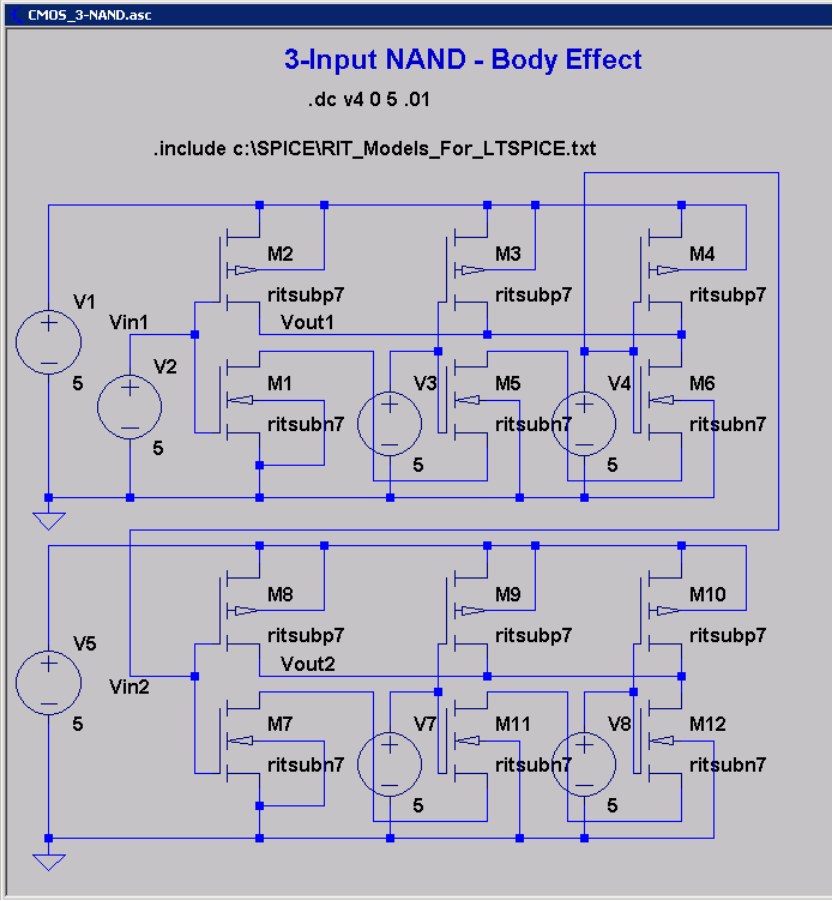


M3 has Vt = Vto
M1 has Vt = Vto + Body Effect

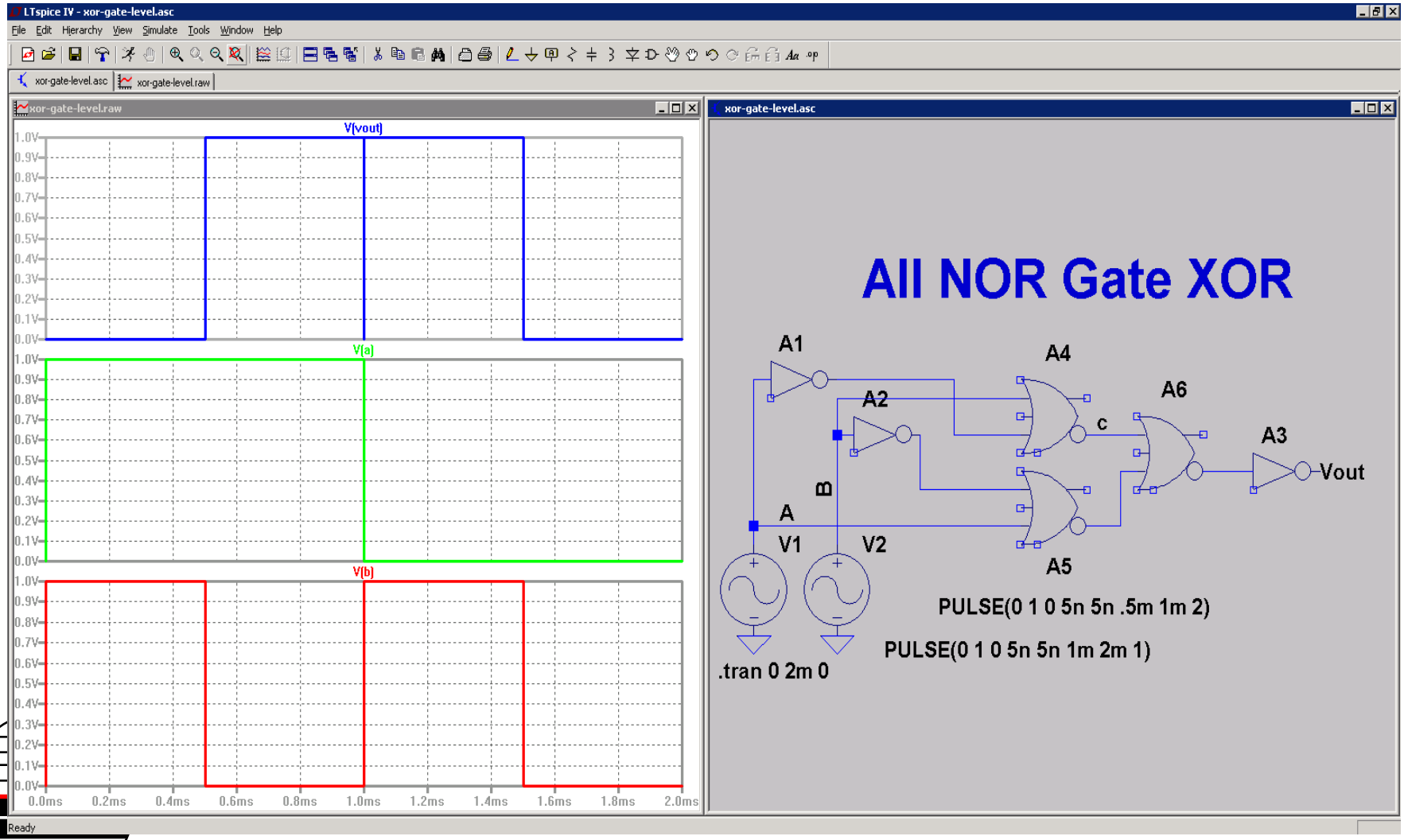
Thus the Voltage Transfer Curve (VTC) is different depending on which transistor is going from low to high (with other two high)

3-INPUT NAND- BODY EFFECT

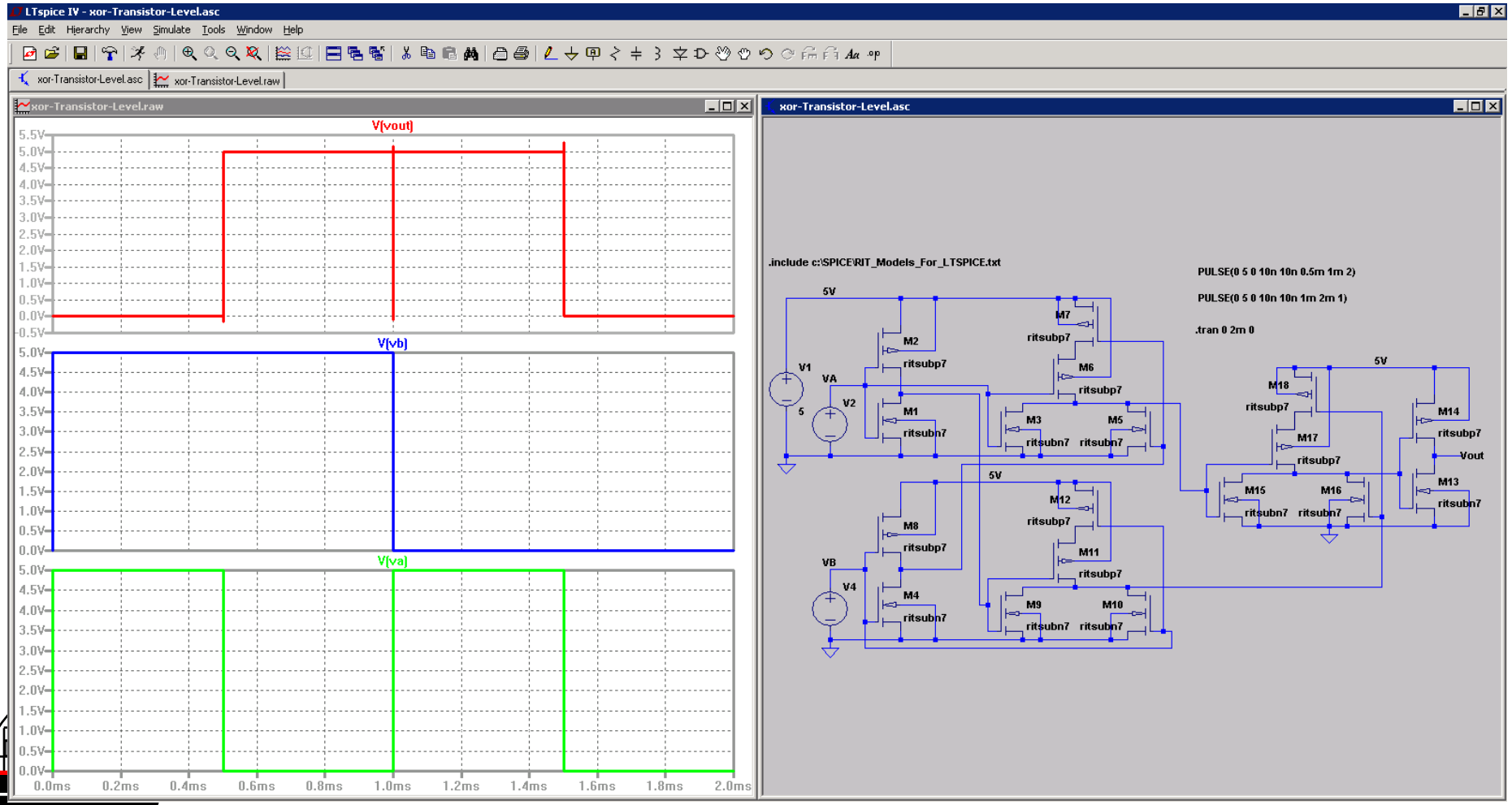




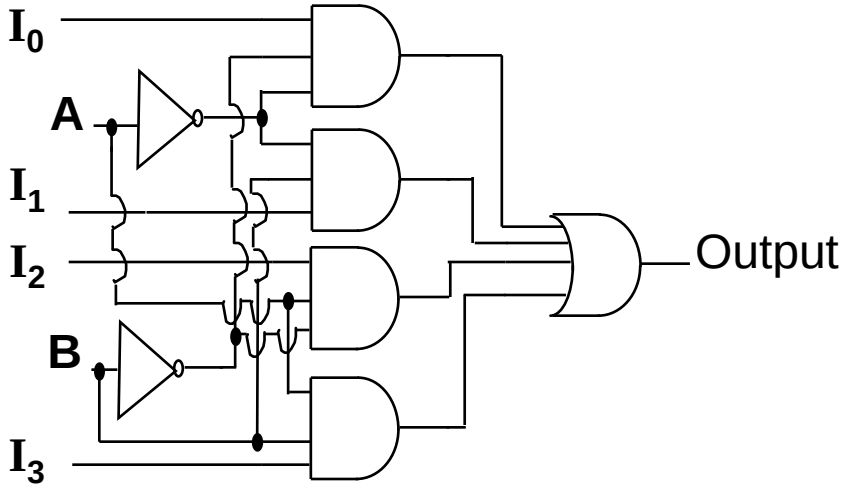
GATE LEVEL SIMULATION OF XOR – ALL/NOR



TRANSISTOR LEVEL SIMULATION OF XOR – ALL/NOR



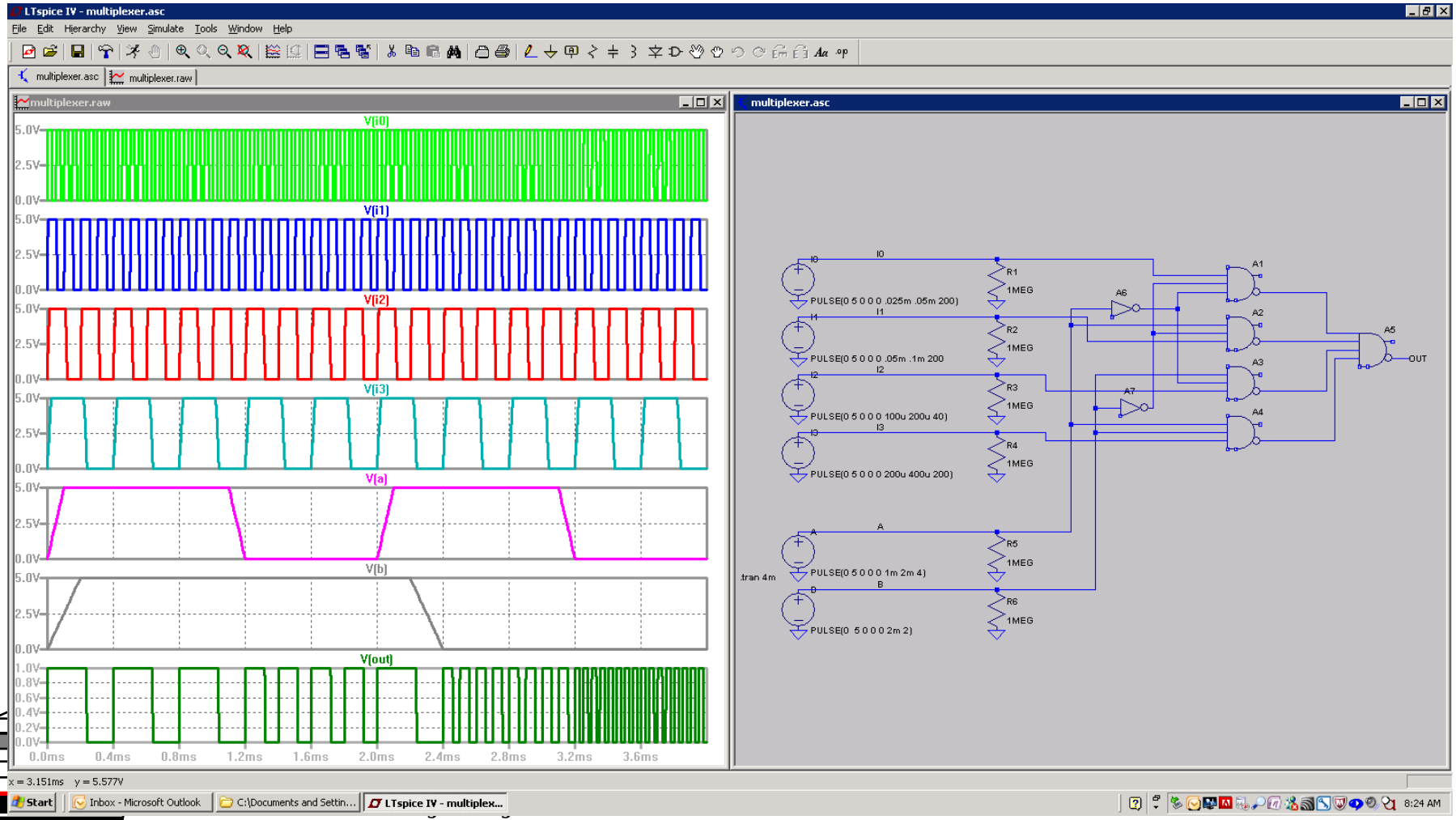
4 TO 1 MULTIPLEXER



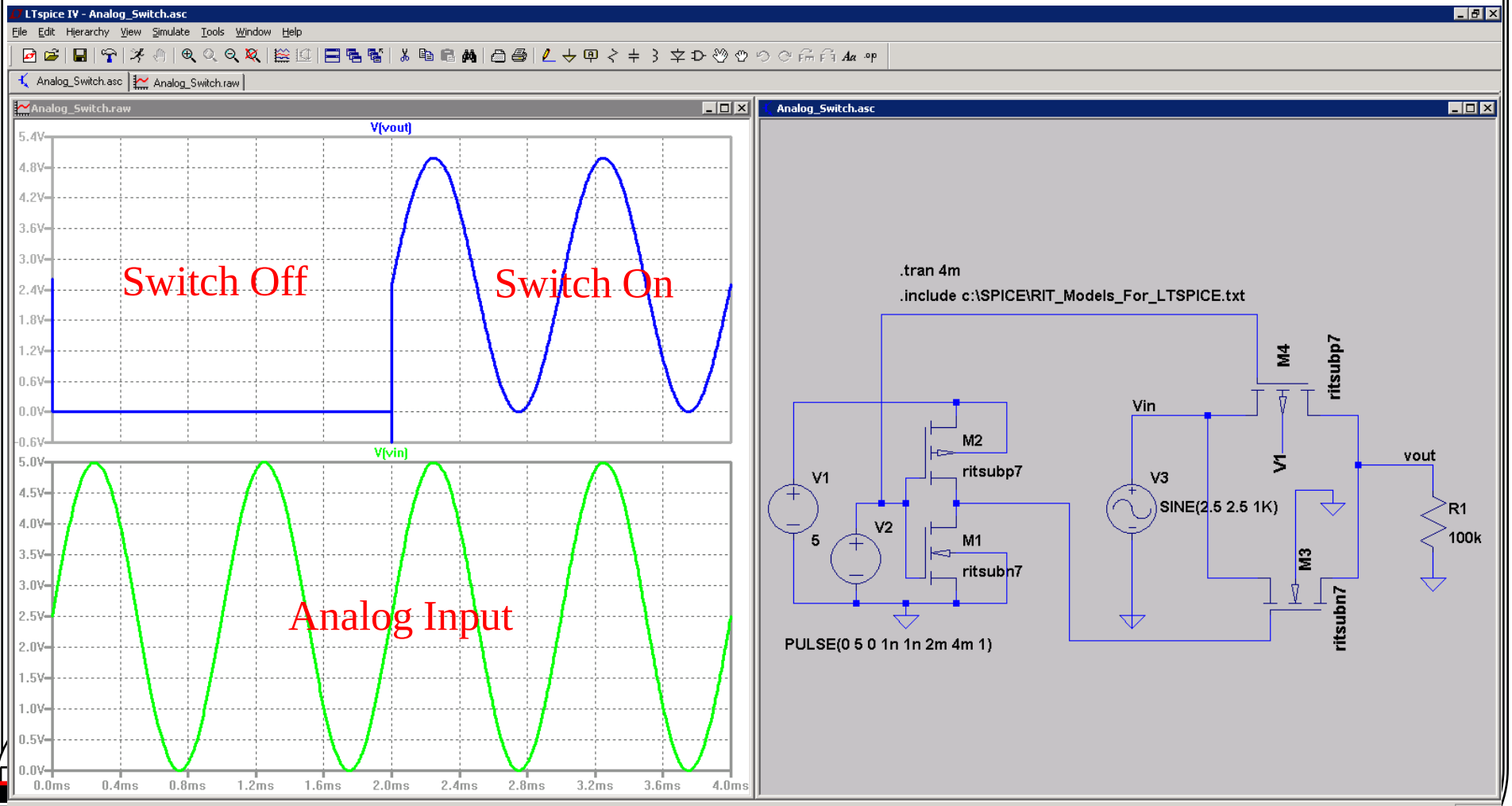
Digital signals A and B control which of the four inputs is directed to the output

A	B	Out
0	0	I0
0	1	I1
1	0	I2
1	1	I3

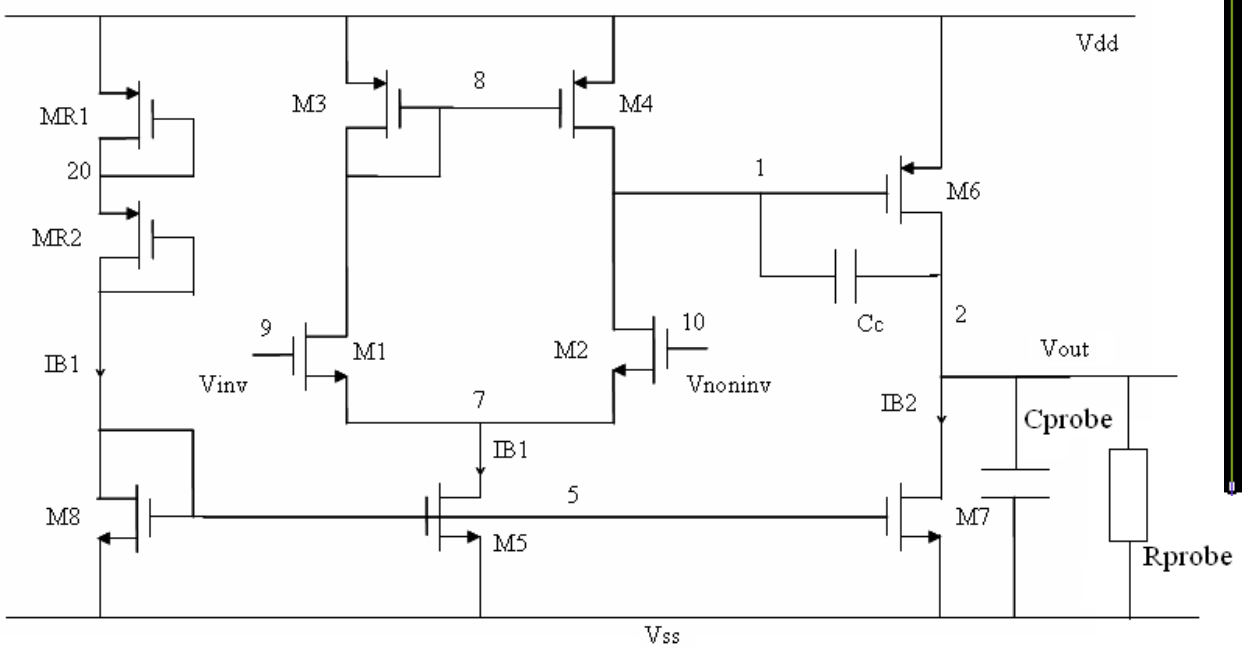
4 TO 1 MUX - GATE LEVEL SIMULATION



ANALOG SWITCH



BASIC TWO STAGE OPERATIONAL AMPLIFIER

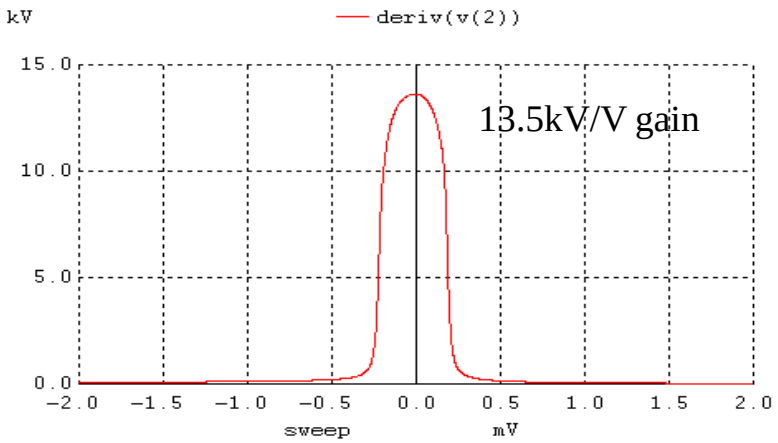


Schematic

Layout

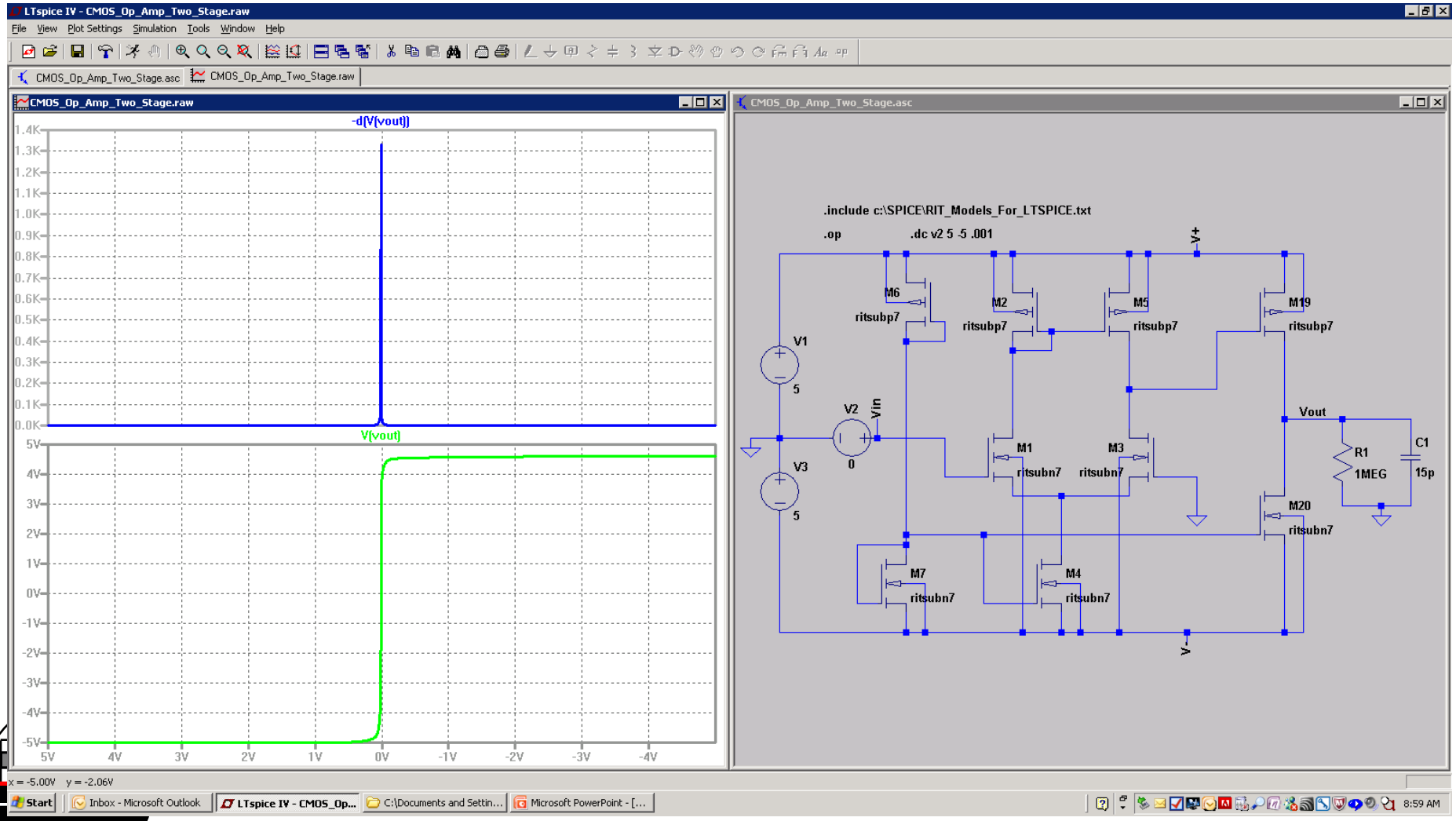
SPICE ANALYSIS OF OP AMP

```
.incl rit_sub_param.txt
m1 8 9 7 6 cmosn w=9u l=5u nrd=1 nrs=1 ad=45p pd=28u as=45p ps=28u
m2 1 10 7 6 cmosn w=9u l=5u nrd=1 nrs=1 ad=45p pd=28u as=45p ps=28u
m3 8 8 4 4 cmosp w=21u l=5u nrd=1 nrs=1 ad=102p pd=50u as=102p ps=50u
m4 1 8 4 4 cmosp w=21u l=5u nrd=1 nrs=1 ad=102p pd=50u as=102p ps=50u
m5 7 5 6 6 cmosn w=40u l=5u nrd=1 nrs=1 ad=205p pd=90u as=205p ps=90u
m6 2 1 4 4 cmosp w=190u l=5u nrd=1 nrs=1 ad=950p pd=400u as=950p ps=400u
m7 2 5 6 6 cmosn w=190u l=5u nrd=1 nrs=1 ad=950p pd=400u as=950p ps=400u
m8 5 5 6 6 cmosn w=40u l=5u nrd=1 nrs=1 ad=205p pd=90u as=205p ps=90u
vdd 4 0 3
vss 6 0 -3
cprobe 2 0 30p
Rprobe 2 0 1meg
cc 1 2 0.6p
mr1 20 20 4 4 cmosp w=6u l=10u nrd=1 nrs=1 ad=200p pd=60u as=200p ps=60u
mr2 5 5 20 4 cmosp w=6u l=10u nrd=1 nrs=1 ad=200p pd=60u as=200p ps=60u
****************
**************
```

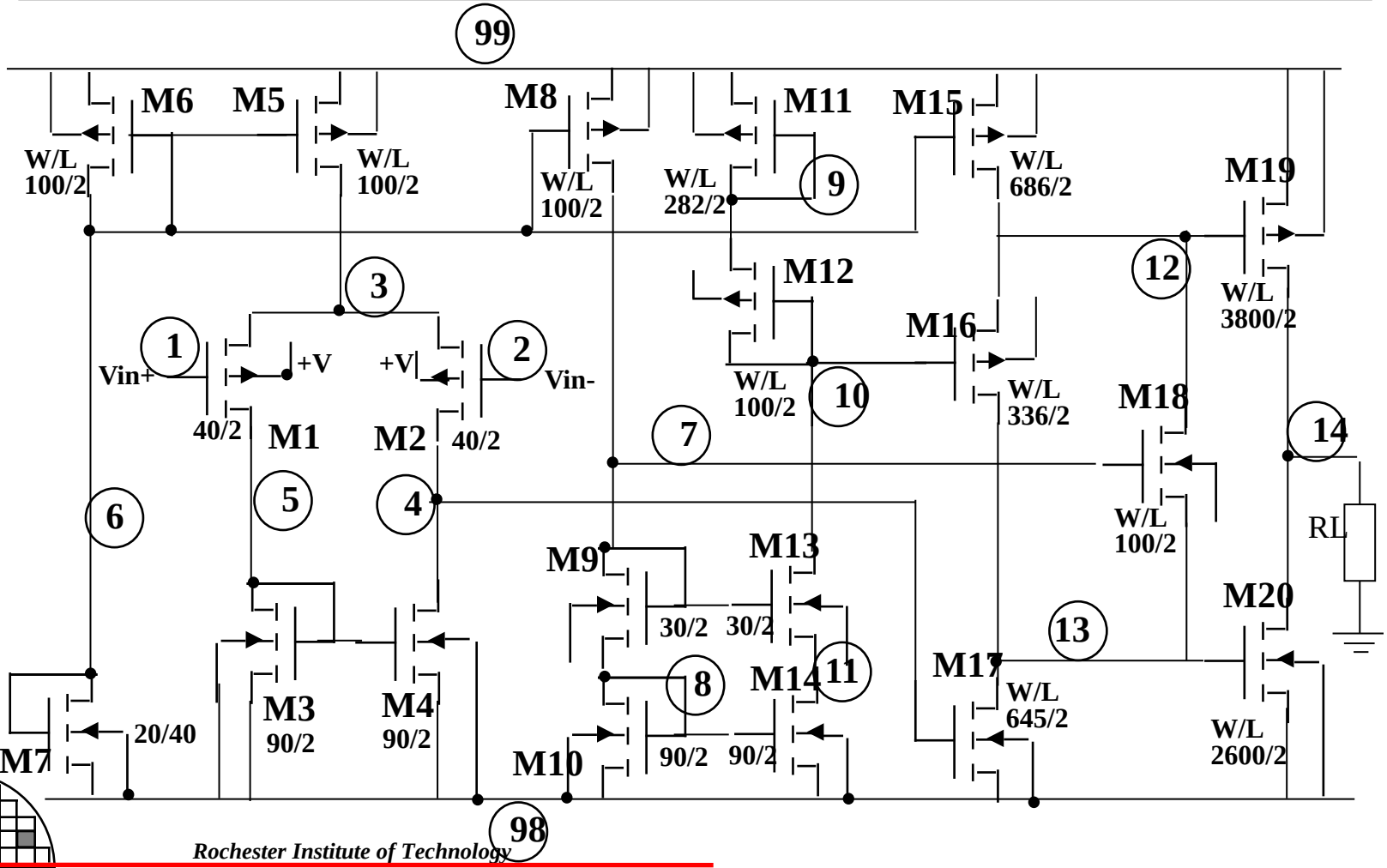



```
***dc open loop
      gain*********
vi1 9 0 0
vi2 10 0 0
*.dc vi2 -0.002 0.002 1u
.dc vi2 -1 1 0.1m
*****open loop frequency
      characteristics*****
*vi1 9 0 0
*vi2 10 0 dc 0 ac 1u
*.ac dec 100 10 1g
.end
```

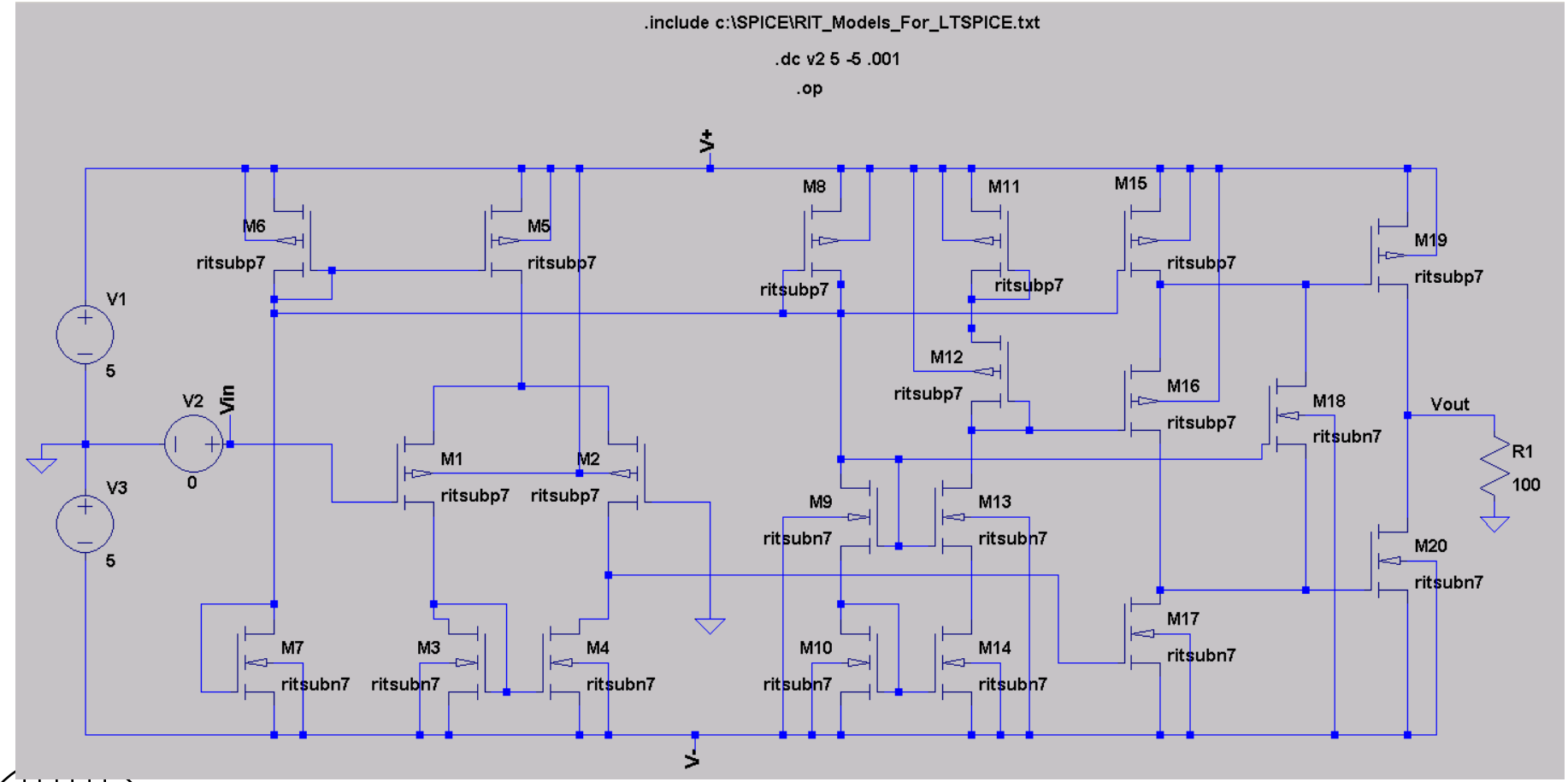
BASIC TWO STAGE OP AMP - LOADING



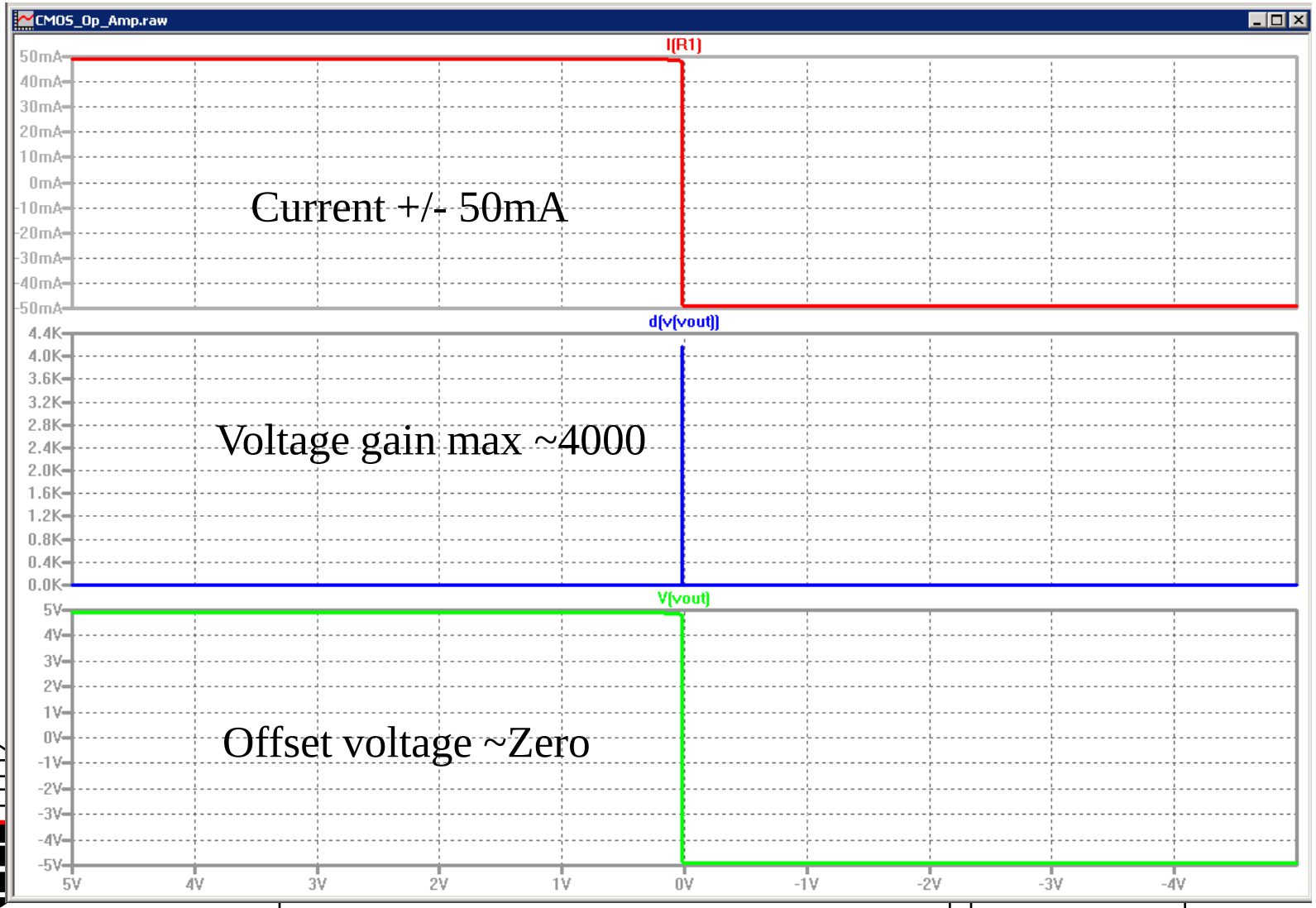
RIT OP AMP WITH OUTPUT STAGE – W/L



RIT OP AMP WITH OUTPUT STAGE

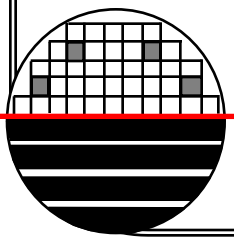


RIT OP AMP WITH OUTPUT STAGE – RL=100

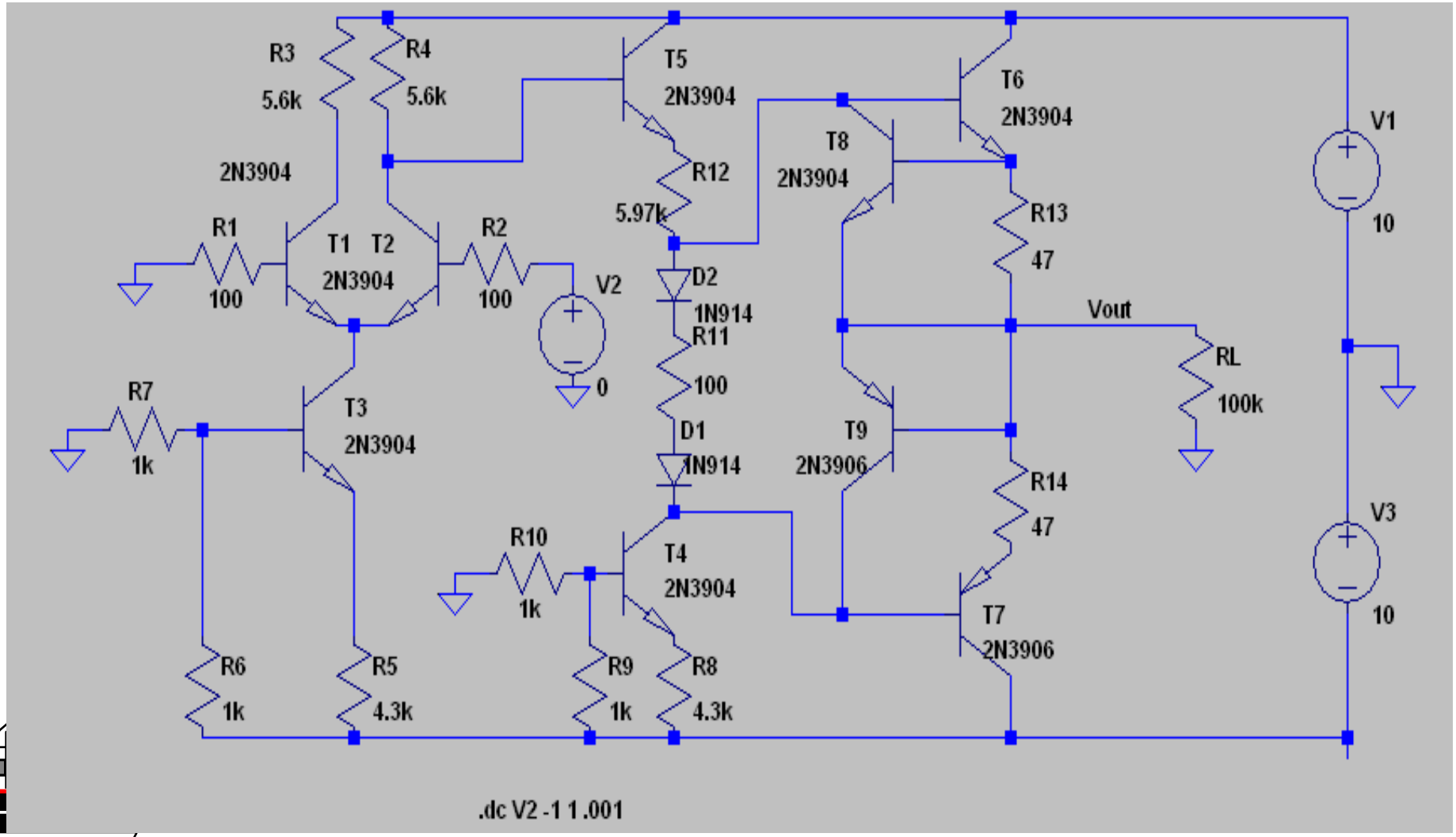


OTHER RESULTS

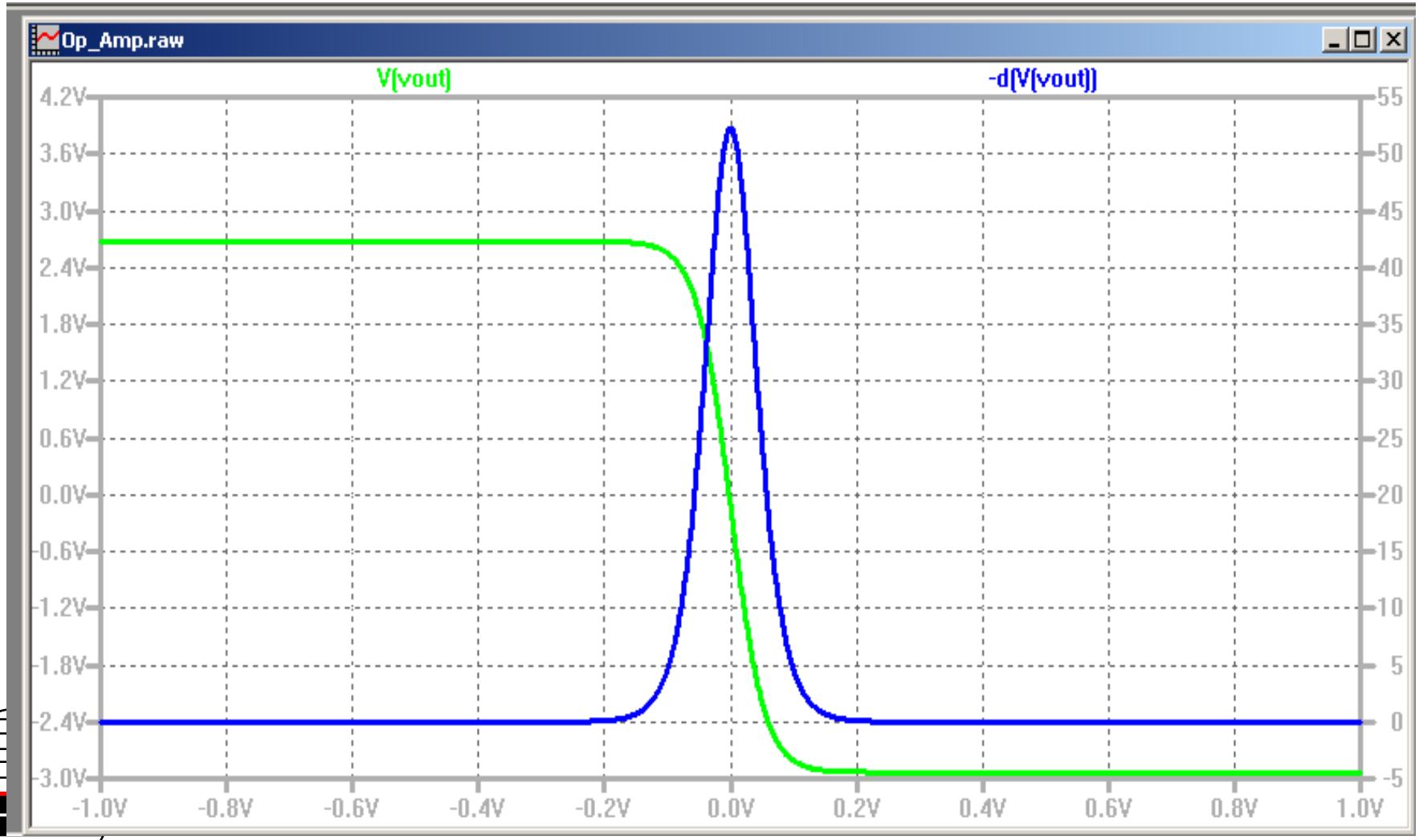
Voltage Gain for 1 MEG Load
Voltage Gain vs RL
Output Resistance
Gain versus Frequency (Gain Bandwidth Product)
Lowest Supply Voltage
Single Supply Operation
Rail-to-Rail Operation
Offset Voltage
Effect of variation of Vt, temperture
more



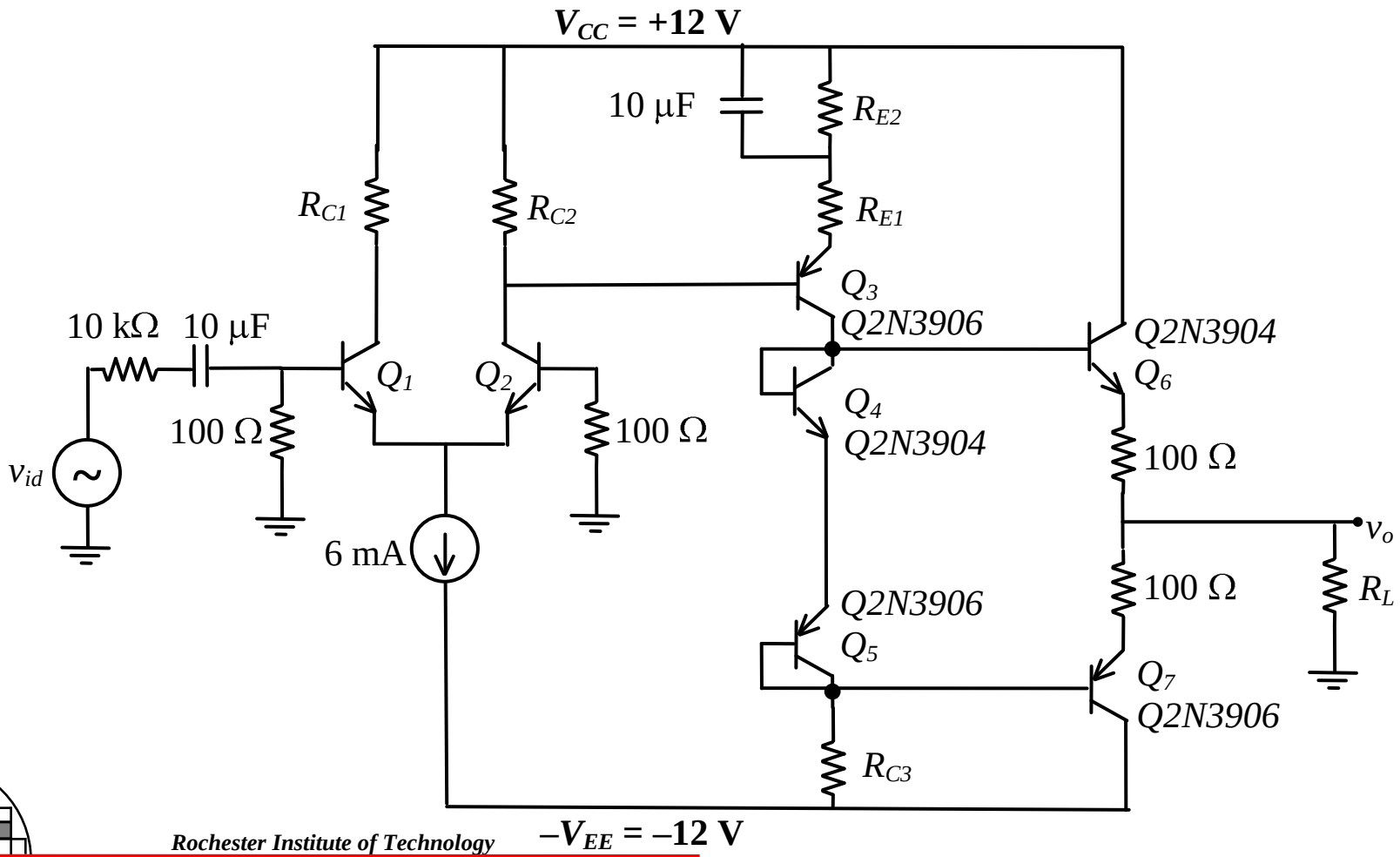
SIMPLE BJT OP AMP



SIMPLE BJT OP AMP

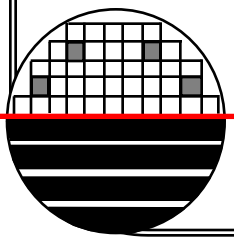


BJT OP AMP USE IN ELECTRONICS LAB

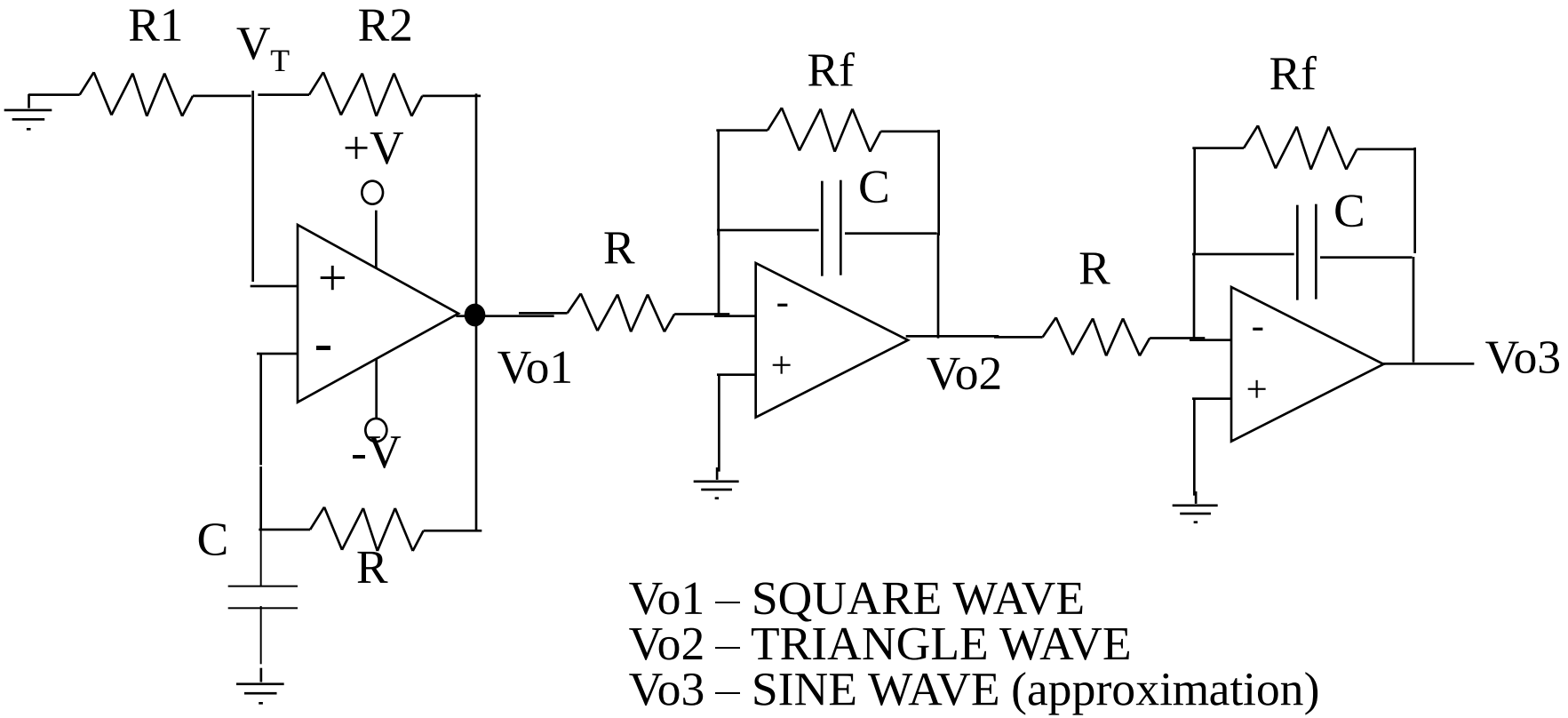


BJT OP AMP SPICE SIMULATION

Electronics II
Lab Assignment

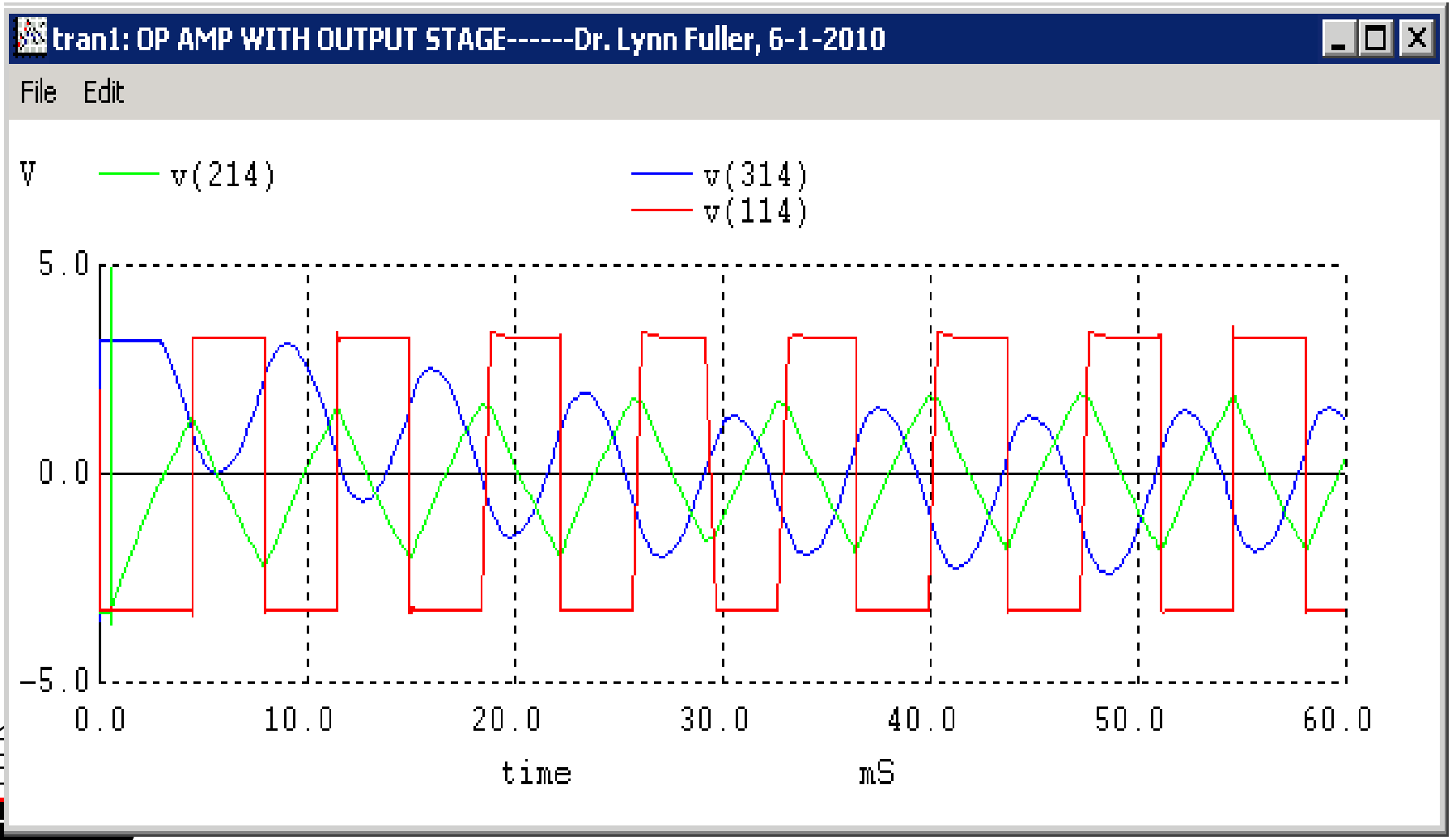


WAVEFORM GENERATOR

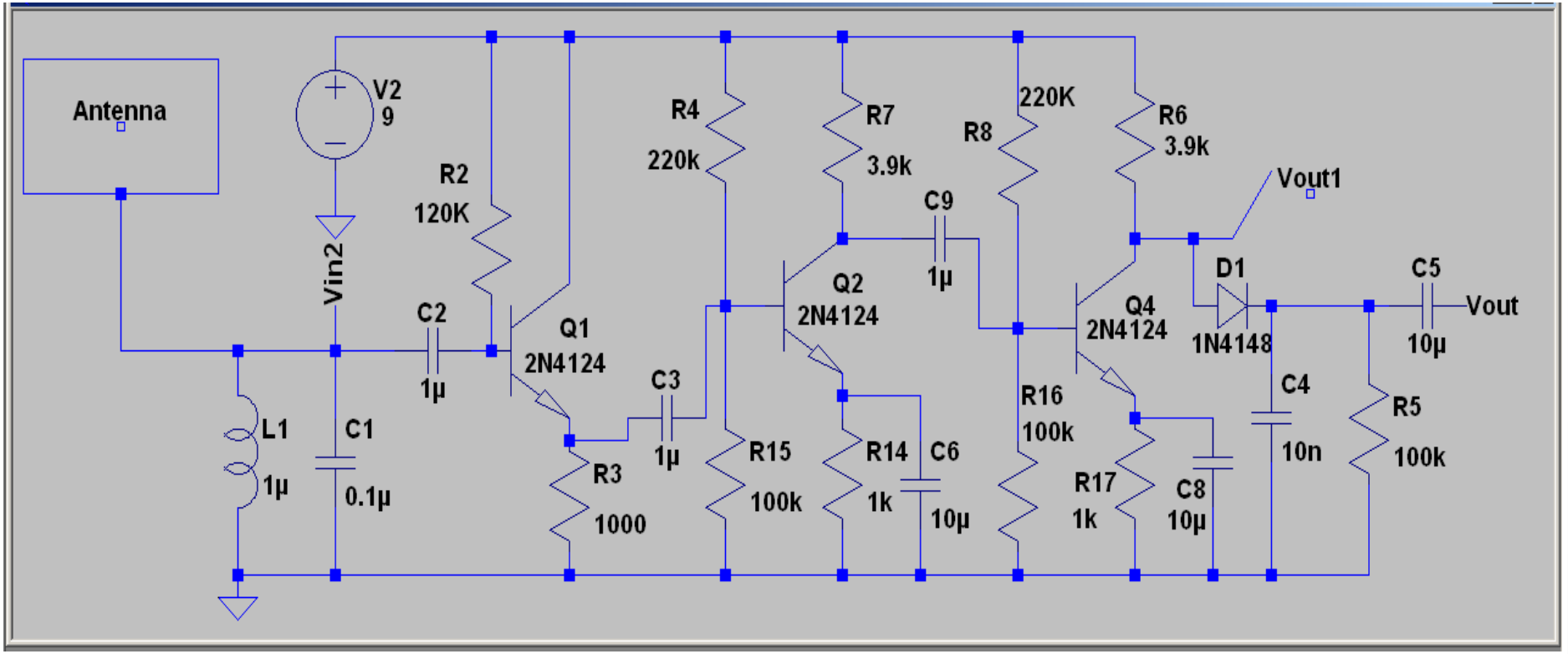


Vo1 – SQUARE WAVE
Vo2 – TRIANGLE WAVE
Vo3 – SINE WAVE (approximation)

WAVEFORM GENERATOR



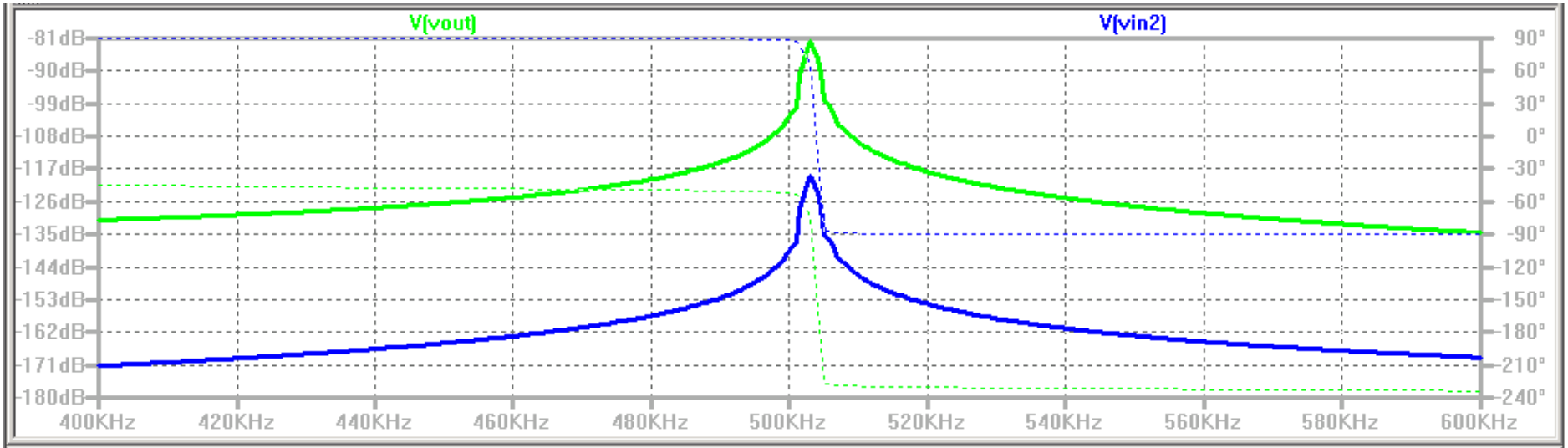
AM RECEIVER

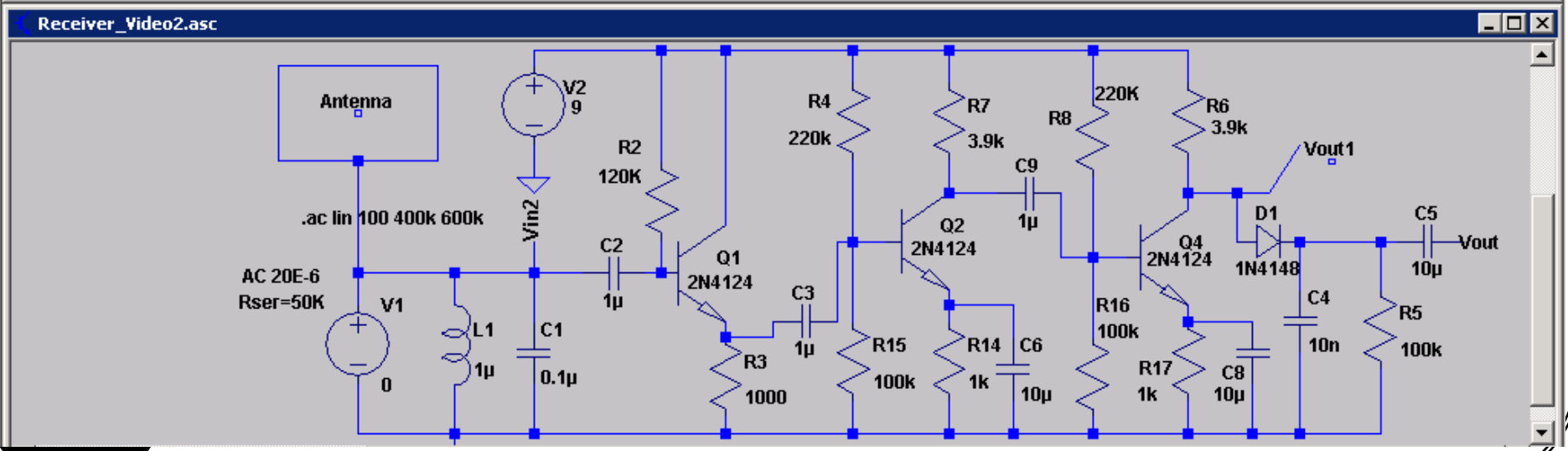


LC Filter

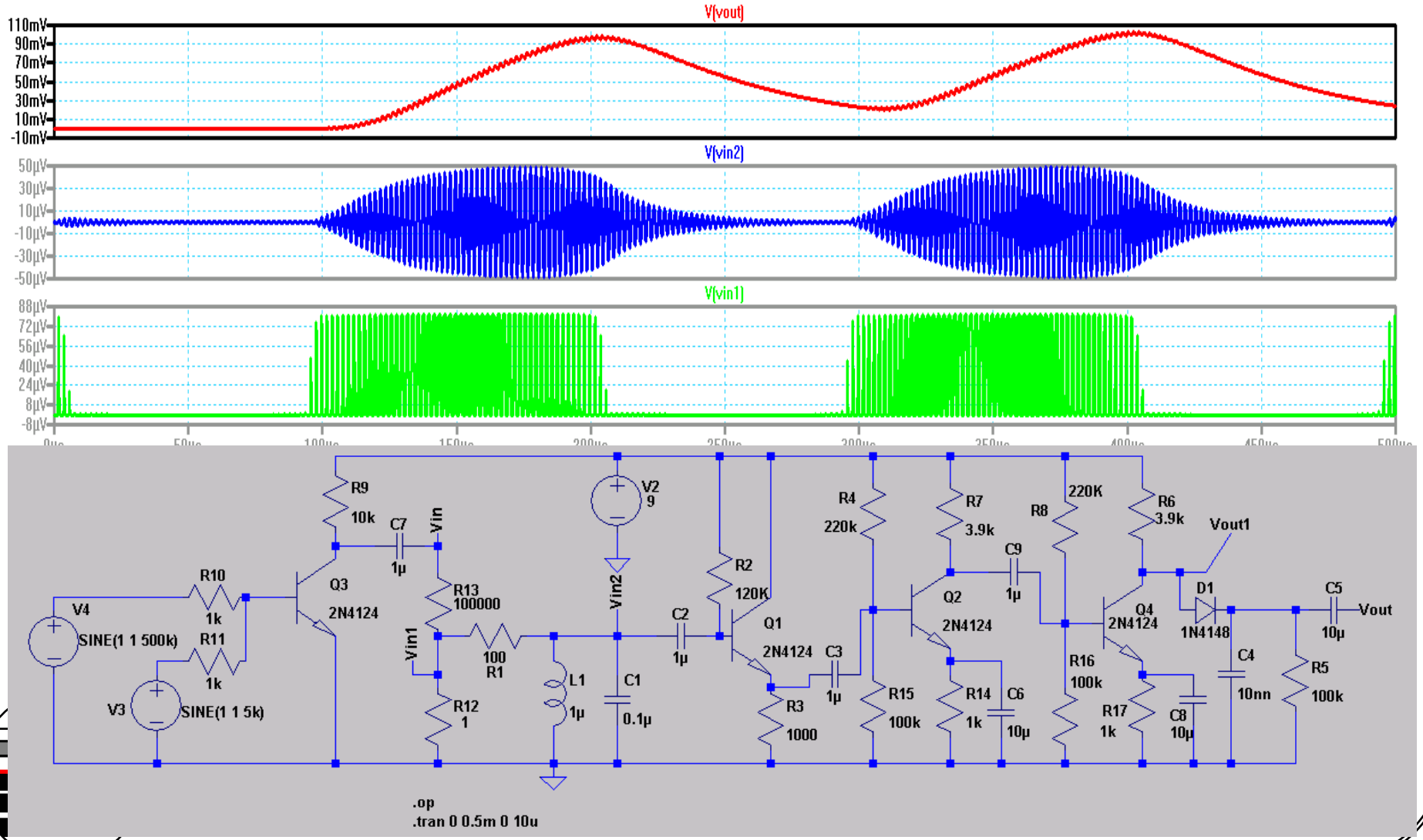
Three Stage Amplifier
Input 10's of uV Output 100's of mV

AM RECEIVER SIMULATION



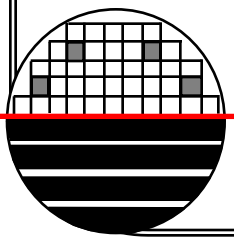


AM RECEIVER SIMULATION



REFERENCES

1. MOSFET Modeling with SPICE, Daniel Foty, 1997, Prentice Hall, ISBN-0-13-227935-5
2. Operation and Modeling of the MOS Transistor, 2nd Edition, Yannis Tsividis, 1999, McGraw-Hill, ISBN-0-07-065523-5
3. UTMOST III Modeling Manual-Vol.1. Ch. 5. From Silvaco International.
4. ATHENA USERS Manual, From Silvaco International.
5. ATLAS USERS Manual, From Silvaco International.
6. Device Electronics for Integrated Circuits, Richard Muller and Theodore Kamins, with Mansun Chan, 3rd Edition, John Wiley, 2003, ISBN 0-471-59398-2
7. ICCAP Manual, Hewlet Packard
8. PSpice Users Guide.



HOMEWORK – SPICE EXAMPLES

Do SPICE for one of the following:

1. Do a SPICE simulation for one of the more complicated examples shown in this document.
2. Do a SPICE simulation for a completely different circuit not shown in this document.