ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Introduction to Modeling MOSFETS in SPICE

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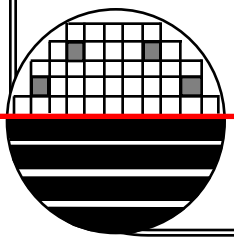
Dept Webpage: http://www.microe.rit.edu

ADOBE PRESENTER

This PowerPoint module has been published using Adobe Presenter. Please click on the Notes tab in the left panel to read the instructors comments for each slide. Manually advance the slide by clicking on the play arrow or pressing the page down key.



OUTLINE

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SPICE
Shichman and Hodges Model
MOSFET Attributes
Changing MOSFET SPICE Model
Ids-Vds Family of Curves
Ids-Vgs
Measured MOSFET Characteristics
AC Attributes
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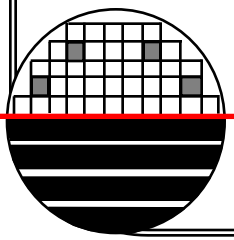


INTRODUCTION

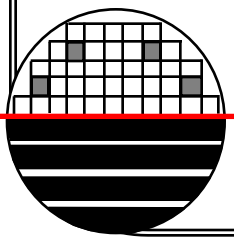
PSpice Lite 9.2 is one of the OrCAD family of products, from Cadence Design Systems, Inc., offering a complete suite of electronic design tools. It is free and includes limited versions of OrCAD Capture, for schematic capture, PSpice for analog circuit simulation and Pspice A/D for mixed analog and digital circuit simulation. PSpice Lite 9.2 is limited to 64 nodes, 10 transistors, two operational amplifiers and 65 primitive digital devices. See page 35 (xxxv) of the PSpice Users Guide.

LT SPICE – is a free SPICE simulator with schematic capture from Linear Technology. It is quite similar to PSpice Lite but is not limited in the number of devices or nodes. Linear Technology (LT) is one of the industry leaders in analog and digital integrated circuits. Linear Technology provides a complete set of SPICE models for LT components.

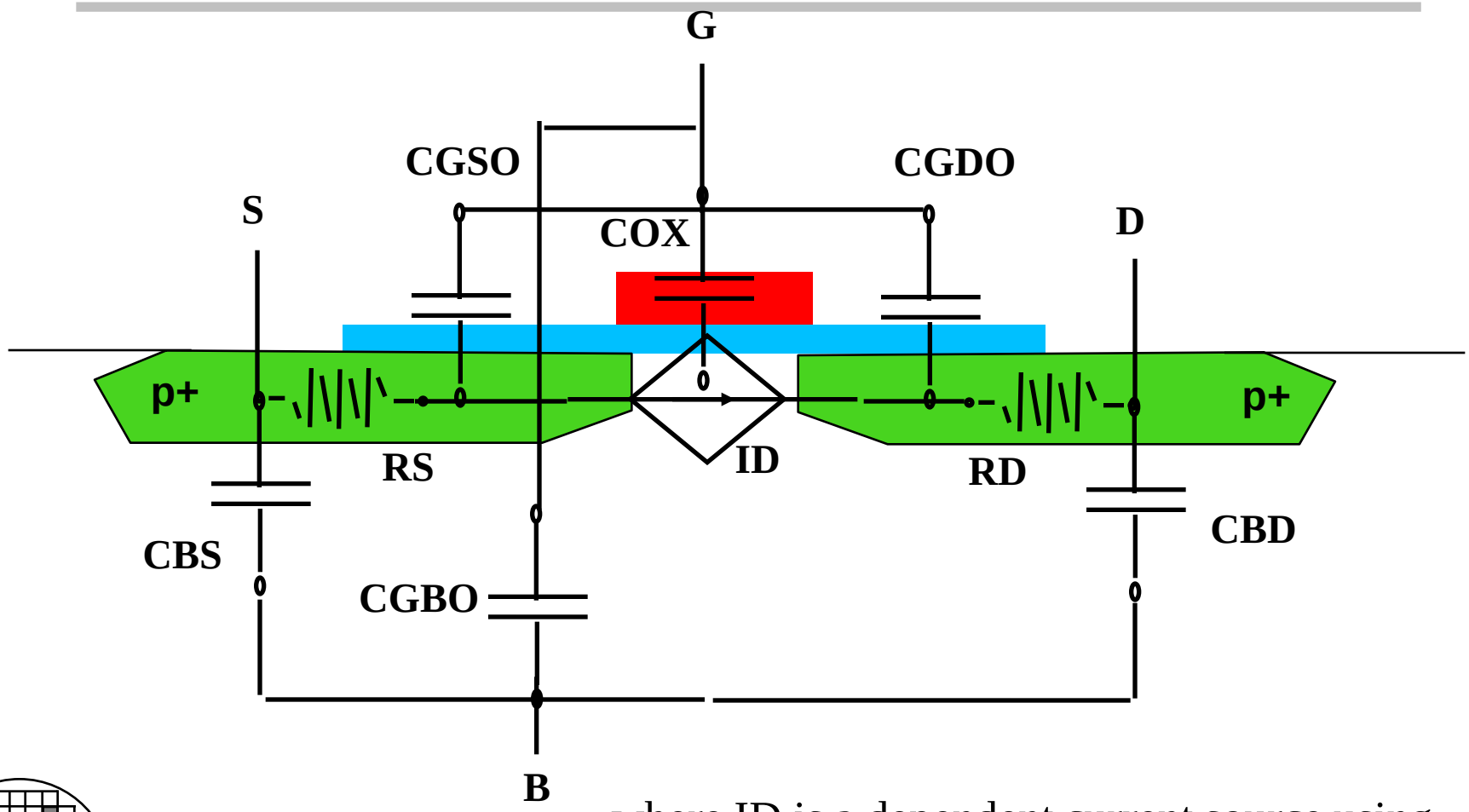
MOSFET DEVICE MODELS

MOSFET Device models used by SPICE (Simulation Program for Integrated Circuit Engineering) simulators can be divided into three classes: First Generation Models (Level 1, Level 2, Level 3 Models), Second Generation Models (BISM, HSPICE Level 28, BSIM2) and Third Generation Models (BSIM3, Level 7, Level 8, Level 49, etc.) The newer generations can do a better job with short channel effects, local stress, transistors operating in the sub-threshold region, gate leakage (tunneling), noise calculations, temperature variations and the equations used are better with respect to convergence during circuit simulation.

In general first generation models are recommended for MOSFETs with gate lengths of 10um or more. If not specified most SPICE MOSFET Models default to level=1 (Shichman and Hodges)

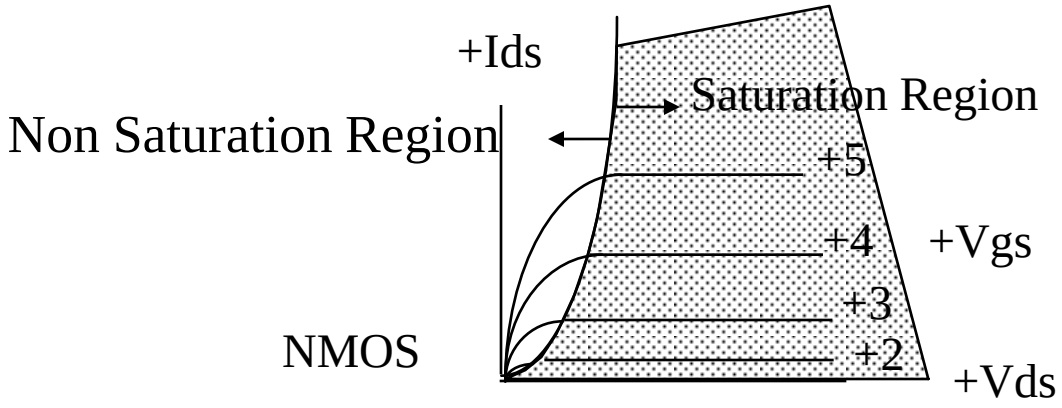


SPICE LEVEL-1 MOSFET MODEL



where ID is a dependent current source using the equations on the next page

SPICE LEVEL 1 - SHICHMAN AND HODGES



$$I_{Dsat} = \frac{\mu W\, Cox'}{2L}(Vg-Vt)^2$$

Saturation Region

$$I_D = \frac{\mu W\, Cox'}{L}(Vg-Vt-V_d/2)V_d$$

Non Saturation Region

where μ, Cox'and Vt are given in equations on the next pages

SPICE LEVEL-1 EQUATIONS FOR UO, VTO AND COX'

Mobility: (cm2/V-s)

$$\mu = \mu_{min} + \frac{(\mu_{max} - \mu_{min})}{\{1 + (N/N_{ref})^{\alpha}\}}$$

Parameter	Arsenic	Phosphorous	Boron
μ_{min}	52.2	68.5	44.9
μ_{max}	1417	1414	470.5
N_{ref}	9.68X10^16	9.20X10^16	2.23X10^17
α	0.680	0.711	0.719

Threshold Voltage: +/- nmos/pmos

$$VTO = \Phi ms - q\ NSS/Cox' +/ -2[\Phi F] +/-2\ (q\varepsilon o \varepsilon rsi\ NSUB\ [\Phi F])^{0.5}/Cox'$$

$[\Phi F] = (KT/q)\ \ln (NSUB/ni)$ where ni = 1.45E10 and KT/q = 0.026

Absolute value

PHI = 2 [ΦF]

Gate Capacitance per unit area Cox'

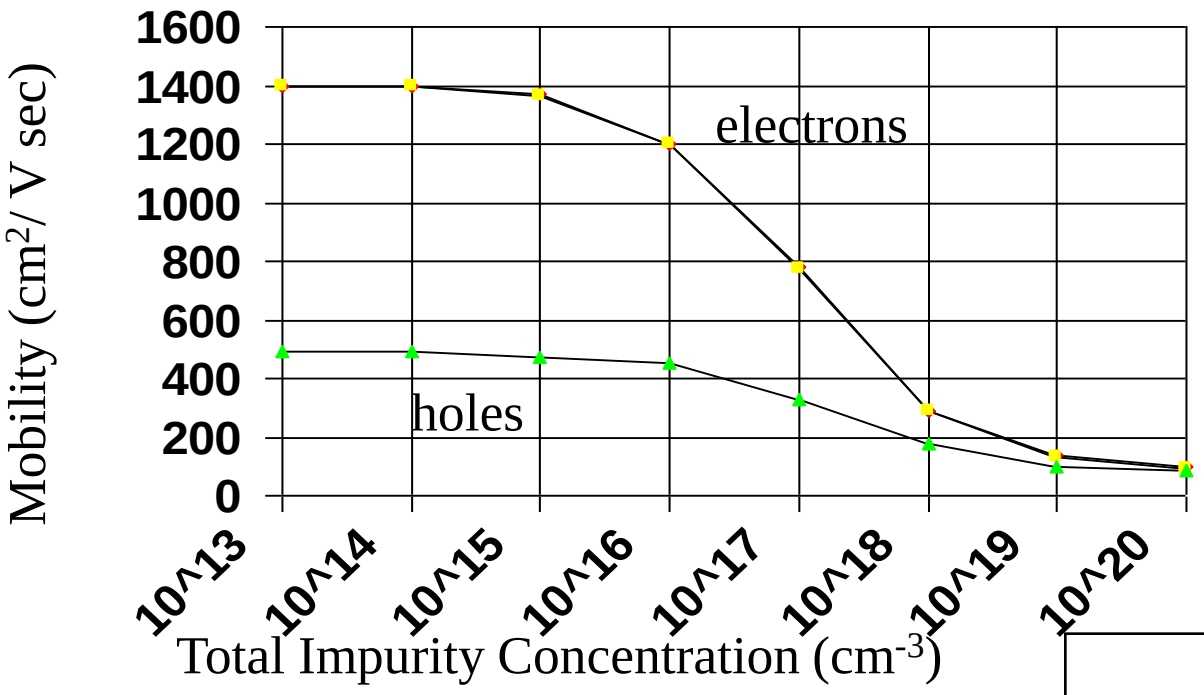
$$Cox' = \varepsilon rox\ \varepsilon o/TOX = 3.9\ \varepsilon o/TOX$$

where $\varepsilon r\ si = 11.7$ and $\varepsilon r\ ox = 3.9$

$\varepsilon o = 8.85E\text{-}12$ F/m or 8.8eE-14F/cm

q = 1.6E-19

MOBILITY MODEL



Electron and hole mobilities in silicon at 300 K as functions of the total dopant concentration (N). The values plotted are the results of the curve fitting measurements from several sources. The mobility curves can be generated using the equation below with the parameters shown:

$$\mu(N) = \mu_{mi} + \frac{(\mu_{max} - \mu_{min})}{\{1 + (N/N_{ref})^{\alpha}\}}$$

From Muller and Kamins, 3rd Ed., pg 33

Parameter	Arsenic	Phosphorous	Boron
μ_{min}	52.2	68.5	44.9
μ_{max}	1417	1414	470.5
N_{ref}	9.68X10^16	9.20X10^16	2.23X10^17
α	0.680	0.711	0.719

LONG CHANNEL THRESHOLD VOLTAGE, VT

Flat-band Voltage $V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C'_{ox}} - \frac{1}{C'_{ox}} \int_0^{Xox} \frac{X \quad \rho(x)}{X_{ox}} dx$

p-type substrate (n-channel) | n-type substrate (p-channel)

$Q_{ss} = q N_{ss}$

Bulk Potential : $\phi_p = -KT/q \quad \ln (N_A / n_i)$ | $\phi_n = +KT/q \quad \ln (N_D / n_i)$

Work Function Difference: $\phi_{M\,S} = \phi_M - (X + Eg/2q + [\phi_p])$ | $\phi_{M\,S} = \phi_M - (X + Eg/2q - [\phi_n])$

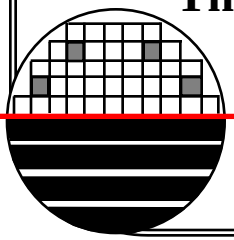
Maximum Depletion Width: (W_{dmax}) $\sqrt{\frac{4\,\varepsilon s[\phi_p]}{qNa}}$ | $\sqrt{\frac{4\,\varepsilon s[\phi_n]}{qNd}}$

Threshold Voltage: p-type substrate

$$VT = V_{FB} + 2[\phi_p] + \frac{1}{C'_{ox}} \sqrt{2\,\varepsilon s\, q\, Na\, (2[\phi_p] + Vsb)}$$

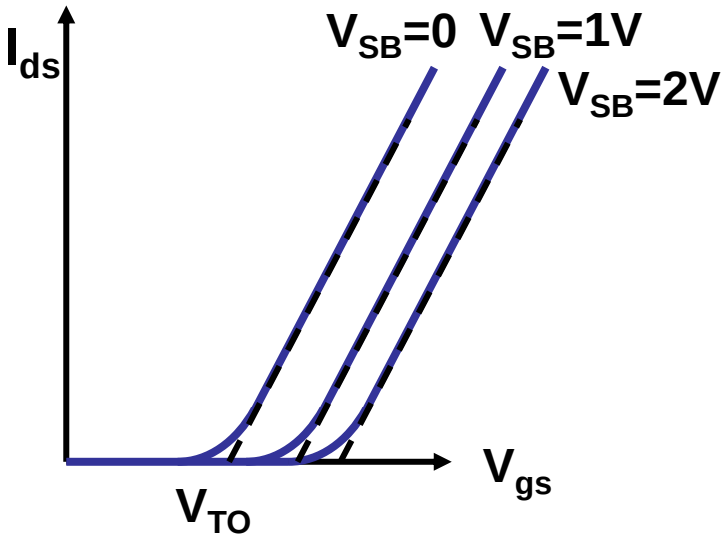
Threshold Voltage: n-type substrate

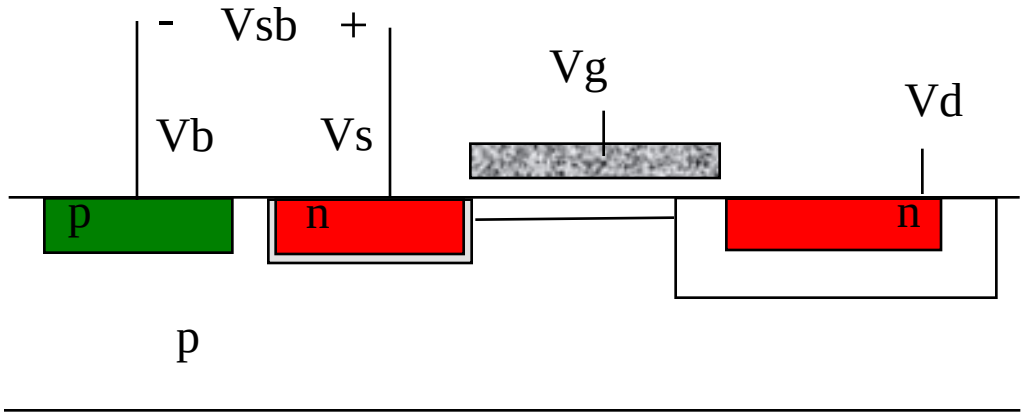
$$VT = V_{FB} - 2[\phi_n] - \frac{1}{C'_{ox}} \sqrt{2\,\varepsilon s\, q\, Nd\, (2[\phi_n] + Vbs)}$$



BACK-BIASING EFFECTS – GAMMA

Body Effect coefficient GAMMA or γ :





$$\gamma = \frac{1}{C_{ox}'}\sqrt{2q\varepsilon_{Si}N_{sub}}$$

$$V_T = \Phi_{MS} - \frac{Qss}{C_{ox}'} + 2\phi_F + \gamma\sqrt{2\phi_F + V_{SB}}$$

where εr si = 11.7 and εr ox = 3.9
εo = 8.8eE-14F/cm
q = 1.6E-19

VT ADJUST IMPLANT

The threshold voltage can be adjusted with an ion implant. If total implant dose is shallow (within W_{dmax}) then the change in Vt is:

$$+/- \Delta Vt = q\ Dose^*/Cox'$$

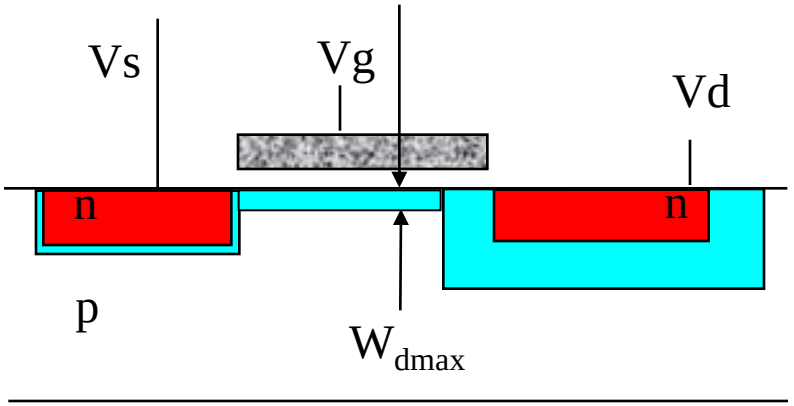
where Dose* is the dose that is added to the Si

Boron gives + shift
Phosphorous gives - shift

Cox' is gate oxide capacitance/cm^2
Cox' = $\varepsilon o \varepsilon r$ / Xox

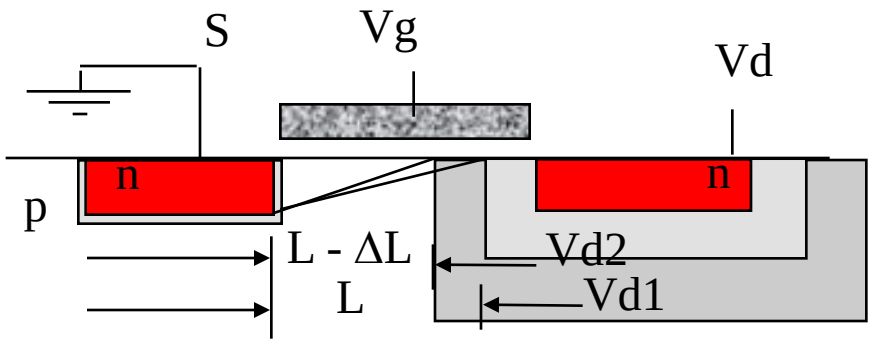
Maximum Depletion Width:

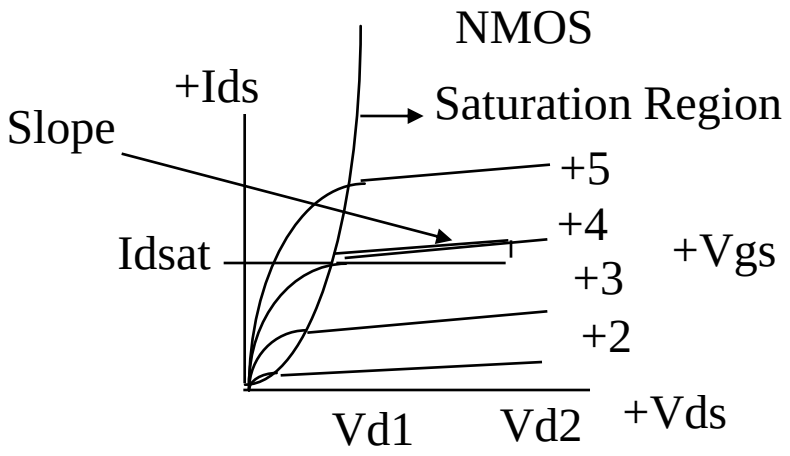
$$Wdmax = \sqrt{\frac{4\,\varepsilon s[\phi_p]}{qN}}$$



CHANNEL LENGTH MODULATION - LAMBDA

Channel Length Modulation
Parameter λ
λ = Slope/ Idsat





$$I_{Dsat} = \frac{\mu W\, Cox'}{2L}(Vg-Vt)^2(1+\lambda Vds)$$

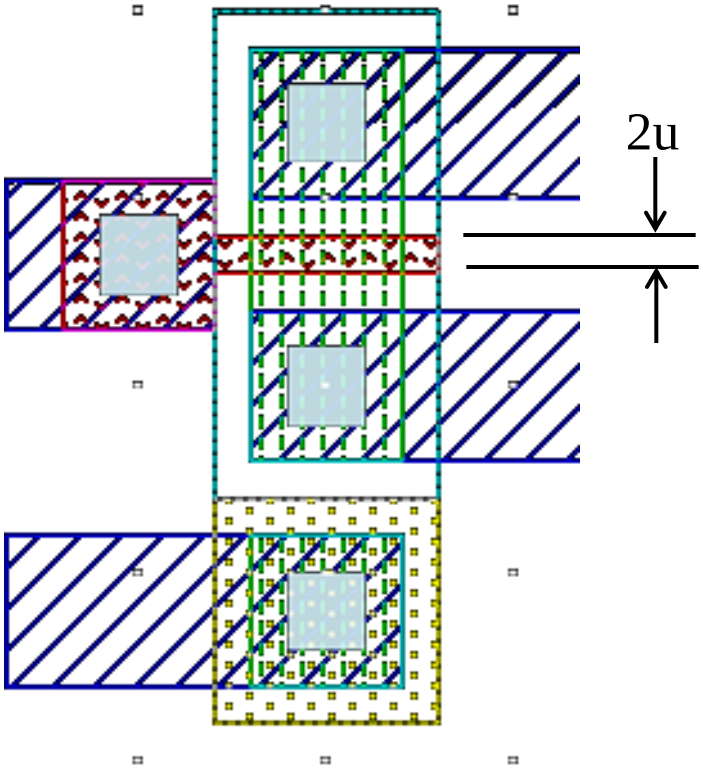
Saturation Region

NMOS Transistor
DC Model, λ is the channel length modulation parameter and is different for each channel length, L. Typical value might be 0.02

$$I_D = \frac{\mu W\, Cox'}{L}(Vg-Vt-V_d/2)V_d(1+\lambda Vds)$$

Non Saturation Region

TRANSISTOR PROPERTIES OR ATTRIBUTES

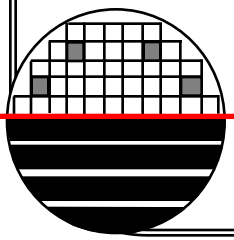


NMOS 2/8

L= 2u
W = 8u
Ad = 8u x10u = 80p
As = Ad = 80p
Pd = 8u+10u+8u+10u = 36u
Ps = Pd = 36u
Nrs = 1
Nrd = 1

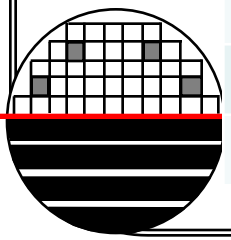
LTSPICE MOSFET ATTRIBUTES

MOSFETS are four terminal devices (Drain, Gate, Source and Substrate). L and W are channel length and width in meters, Ad and As are area of drain and source in square meters. If not specified default values are used. (see next page) Perimeter of Drain and source (PD and PS) in meters is used to calculate drain and source side wall capacitance. If PD and PS are not given the default is zero. NRD and NRS are multiplied by the drain and source sheet resistance to give series resistance RD and RS. The default value for NRD and NRS is one.



LTSPICE MOSFET ATTRIBUTE DEFAULT VALUES

Name	Description	Unit	Default	Example
L	Default Length	m	defl	100u
W	Default Width	m	defw	100u
Ad	Default drain area	m2	defad	1000p
As	Default source area	m2	defas	1000p
Pd	Default drain perimeter	m	0	200u
Ps	Default source perimeter	m	0	200u
Nrd	Default drain squares	-	1	1
Nrs	Default source squares	-	1	1
Nrg	Default gate squares	-	0	1
Nrb	Default bulk squares	-	0	1
Lmin	Bin length lower limit	m	0	10u
Lmax	Bin length upper limit	m	0	20u
Wmin	Bin width lower limit	m	0	10u
Wmax	Bin width upper limit	m	0	20u



MOSFET DEFINITION - LTSPICE

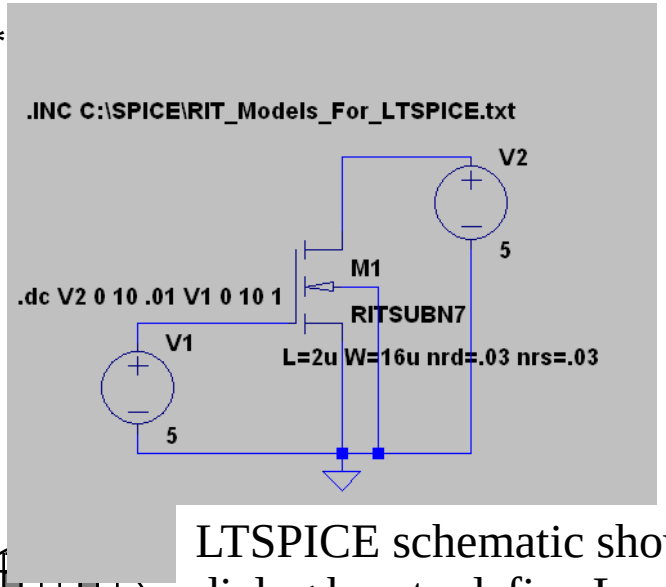
For example:

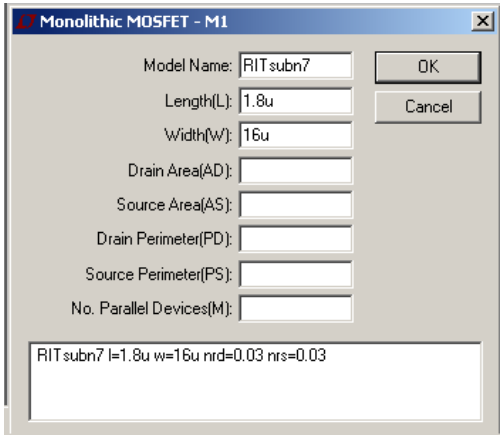
* SPICE Input File
* MOSFET names start with M…. M2 is the name for the MOSFET below and its drain, gate, source
* and substrate is connected to nodes 3,2,0,0 respectively. The model name is RITSUBN7.
* The parameters/attributes is everything after that.

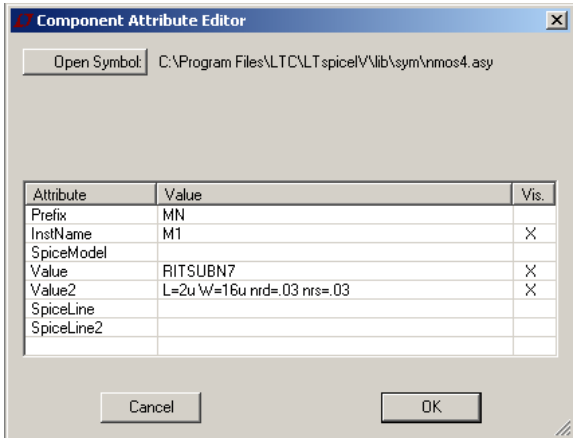
M2 3 2 0 0 RITSUBN7 L=2U W=16U ad=96e-12 as=96e-12 pd=44e-6 ps=44e-6 nrd=1.0 nrs=1.0

*

*







LTSPICE schematic showing **.Include** and **.dc** sweep commands. Properties dialog box to define L and W values. Note: attributes with no entry field **nrs** and **nrd** are typed in bottom box. Attribute Editor (CTRL R-click on the transistor) allows attributes with Vis.=X to be displayed on the schematic.

MOSFET DEFINITION - PSPICE

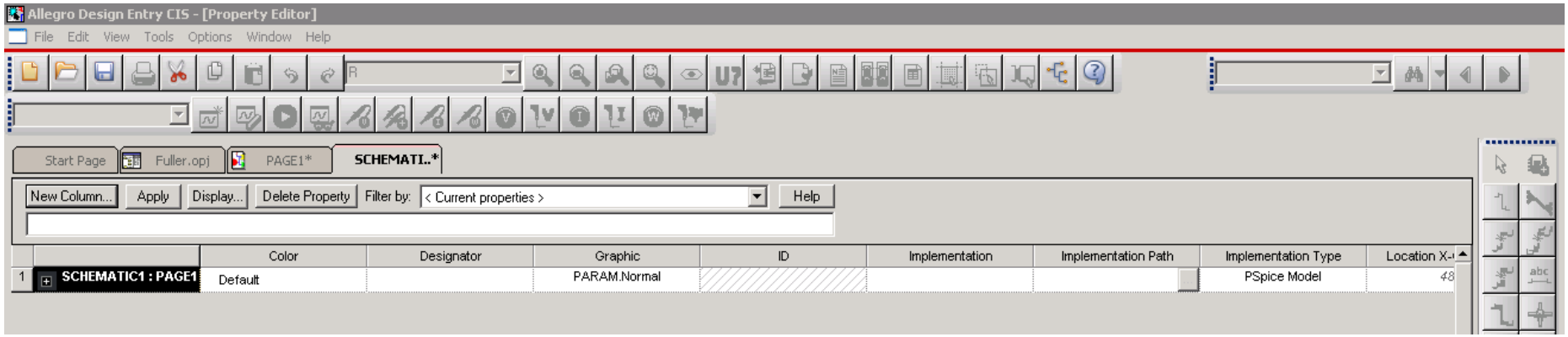
For example:

* SPICE Input File
* MOSFET names start with M…. M2 is the name for the MOSFET below and its drain, gate, source
* and substrate is connected to nodes 3,2,0,0 respectively. The model name is RITSUBN7.
* The parameters/attributes is everything after that.

M2 3 2 0 0 RITSUBN7 L=2U W=16U ad=96e-12 as=96e-12 pd=44e-6 ps=44e-6 nrd=1.0 nrs=1.0

*

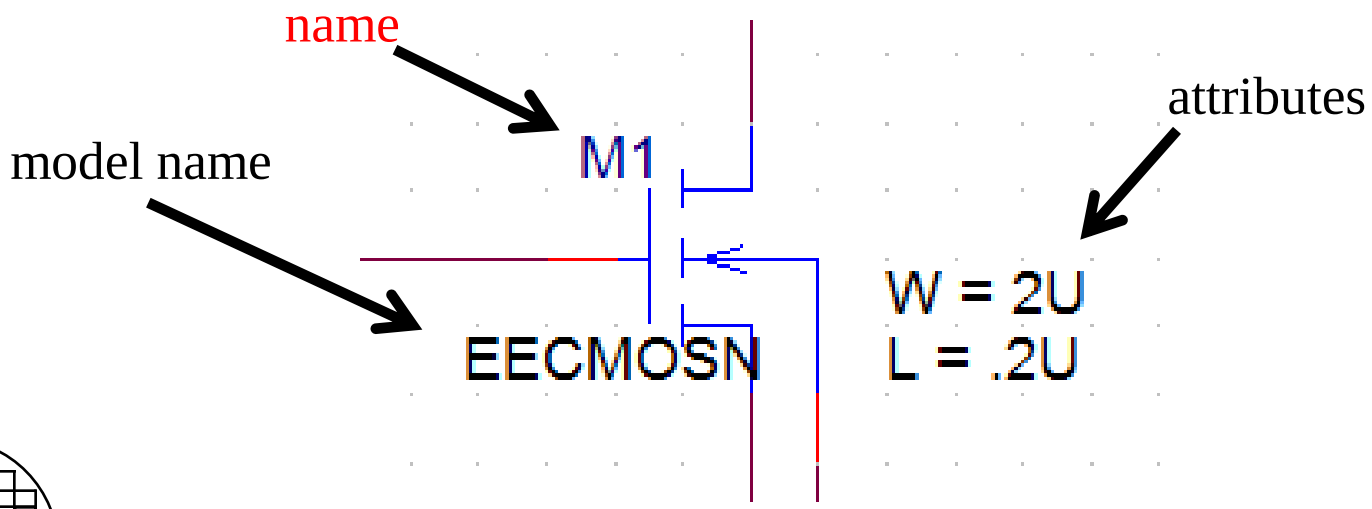
*

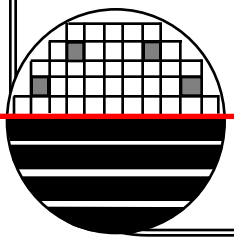


In PSPICE the Attribute Editor (CTRL R-click on the transistor) allows attributes values to be set, new attribute columns to be created, and attributes can be selected to be displayed on the schematic..

MOSFET DEFINITION - PSPICE

In SPICE a transistor is defined by its **name** and associated **properties or attributes** and its **model**. MOSFET names start with M, attributes (L, W, Ad, As, etc.) are specified by the user and shown in the input file net list. Some attributes can be displayed on the schematic. The model is specified in a file in a given location or is defined in a library.





CHANGING THE MOSFET SPICE MODEL IN LTSPICE

There a several ways to change the MOSFET SPICE model. A good way to do it is create a text file on your computer and put your models in that text file and save it in some folder. You can copy models from Dr. Fuller's webpage to start your collection of models.

See: http://people.rit.edu/lffeee/CMOS.htm

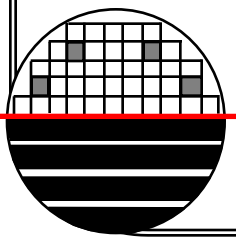
Example contents of that file is shown on the page below.

Next you change the model name for your transistor by right click on the model name shown in your schematic and typing the model name used in the model file. (for example: RITSUBN7)

Finally you place a SPICE directive on your schematic by clicking on the .op icon on the top banner and type the following command:

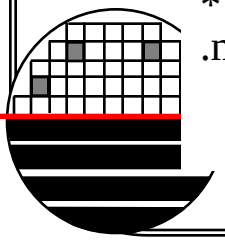
.include Drive:\path\folder\filename

For example .include C:\SPICE\RIT_Models_For_LTSPICE.txt



SIMPLE AND ADVANCED SPICE MODELS

```
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSN     NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSP      PMOS (LEVEL=8
+TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
* From Electronics II EEEE482 SIMPLE MODEL
.model EENMOS       NMOS (VTO=0.4 KP=432E-6 GAMMA=0.2 PHI=.88)
*
* From Electronics II EEEE482 SIMPLE MODEL
.model EEPMOS       PMOS (VTO=-0.4 KP=122E-6 GAMMA=0.2 PHI=.88)
```



CHANGING THE MOSFET SPICE MODEL IN PSPICE

FULLERMOSFET.lib:Mbreakn - AMS Model Editor - [Model Text]

File Edit View Model Plot Tools Window Help

cadence

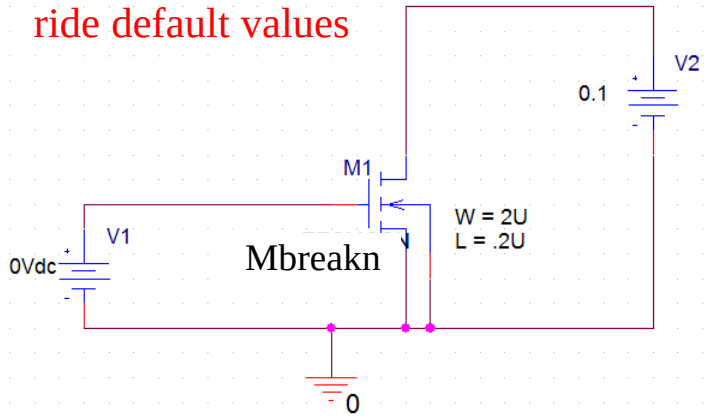
Models List

Model Name	Type
Mbreakn	MOS

```
.model Mbreakn NMOS vto=0.4 kp=432u gamma=0.2 phi=0.88 l=0.1u
```

Right click and select EDIT SPICE MODEL to type in underlined parameters

L and W shown on the schematic over ride default values



Start Page | FullerMOS..* | PAGE1* | SCHEMATI..* | ID-VGS-S

View output file to see this listing of spice model parameters including default values for L and W

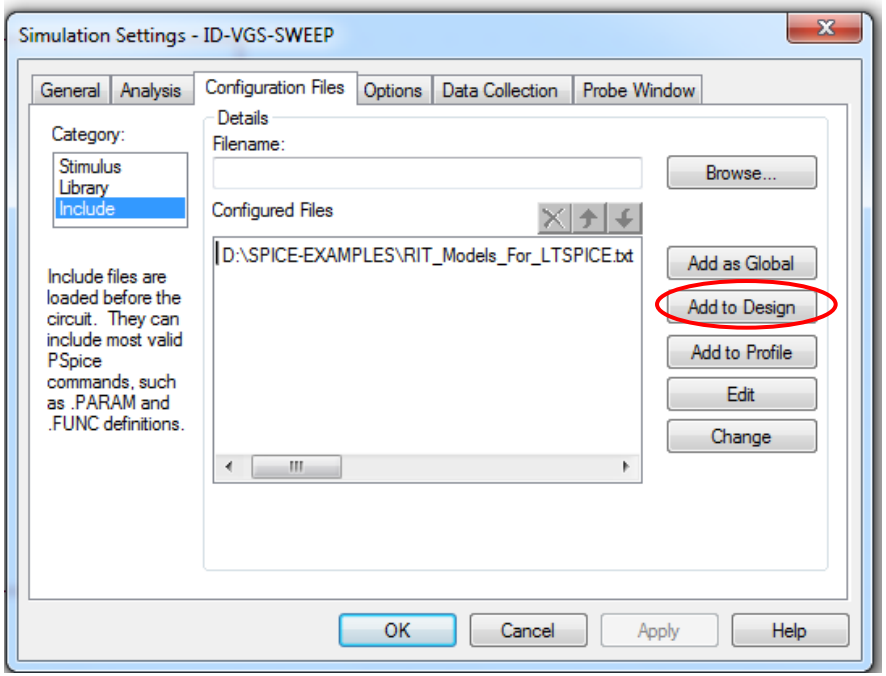
```
63:          LEVEL    1
64:              L  100.000000E-09
65:              W  100.000000E-06
66:            VTO     .4
67:             KP  432.000000E-06
68:          GAMMA     .2
69:            PHI     .88
70:         LAMBDA    0
71:             IS   10.000000E-15
72:             JS    0
73:             PB     .8
74:           PBSW     .8
75:             CJ    0
76:           CJSW    0
77:           CGSO    0
78:           CGDO    0
79:           CGBO    0
80:            TOX    0
81:             XJ    0
82:          UCRIT   10.000000E+03
83:         DIOMOD    1
84:            VFB    0
85:           LETA    0
86:           WETA    0
87:             U0    0
88:           TEMP    0
89:            VDD    5
90:          XPART    0
91:
92:
```

CHANGING THE MOSFET SPICE MODEL IN PSPICE

RIT_Models_For_LTSPICE.txt - Notepad

File Edit Format View Help

```
*SPICE MODELS FOR RIT DEVICES - DR. LYNN FULLER 12-9-2013
*LOCATION DR.FULLER'S COMPUTER DESKTOP/SPICE/MODELS/
*and also at: http://people.rit.edu/lffeee/CMOS.htm
*
.model RITMEMDIODE D IS=3.02E-9 N=1 RS=207
+VJ=0.6 CJO=200e-12 M=0.5 BV=400
*
.model SolarCell D IS=235e-9 N=1 RS=6.85 CJO=200e-12 M=0.5 BV=400
*
*4-4-2013
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTHO=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*4-4-2013
.MODEL RITSUBP7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTHO=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
* From Electronics I EEEE481
.model EENMOS2 NMOS LEVEL=2
+VTO=0.7 KP=25E-6 LAMBDA=0.02 GAMMA=0.9 TOX=90E-9 NSUB=3.7E15
*
* From Electronics II EEEE482
.MODEL QRITNPN NPN (BF=416 IKF=.06678 ISE=6.734E-15 IS=6.734E-15 NE=1.259 RC=1 RB=10 VA=109)
*
* From Electronics II EEEE482 FOR ~100nm Technolog
.model EECMOSN  NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTHO=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSP  PMOS (LEVEL=8
+TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
+VTHO=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
* From Electronics II EEEE482 SIMPLE MODEL
.model EENMOS   NMOS (VTO=0.4 KP=432E-6 GAMMA=0.2 PHI=.88)
*
* From Electronics II EEEE482 SIMPLE MODEL
.model EEPMOS   PMOS (VTO=-0.4 KP=122E-6 GAMMA=0.2 PHI=.88)
```

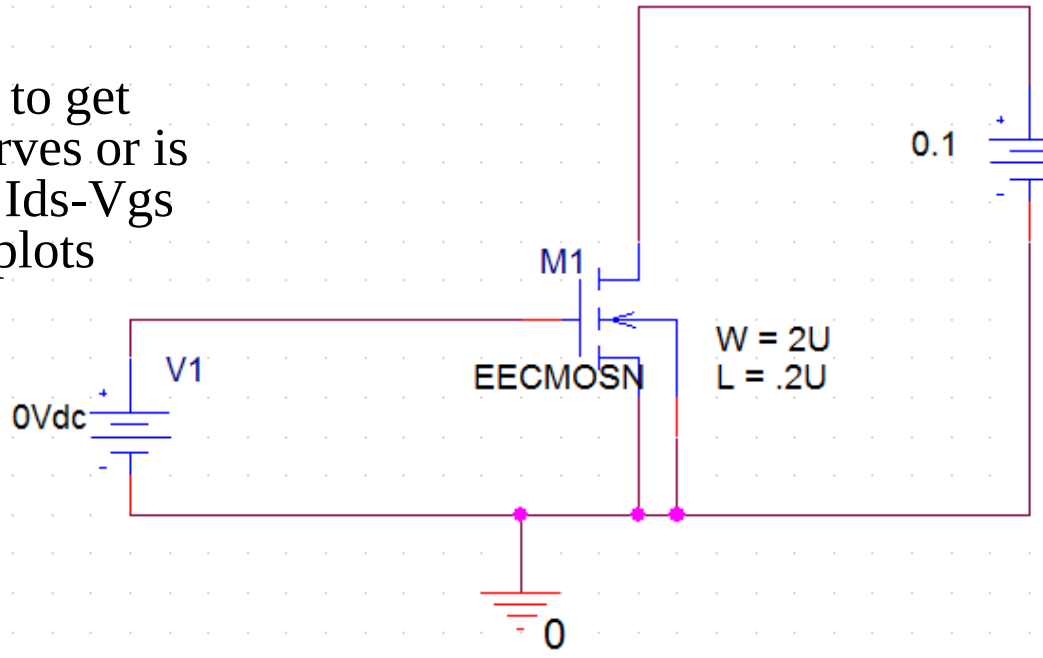


In PSPICE models saved in a text file can be included as a configuration file in the Simulation Settings dialog box as shown above. Change the component model name to the model name in the text file.

COMPARISON OF MOSFET CHARACTERISTICS

The circuit shown can be used to see the transistor family of Ids-Vds curves, Ids-Vgs plot and Ids-Vgs (Ids on log scale) Subthreshold plot. We can investigate the effect of changing attributes, SPICE model and model parameters.

V1 is steped to get family of curves or is swept to get Ids-Vgs and Sub-Vt plots



V2 is swept to get family of curves or is held constant to get Ids-Vgs plots

PSPICE MOSFET MODEL PARAMETERS

95 mosfet model parameters used by cadence PSPICE for Level 8 BSIM

Start Page | FullerMOS..* | PAGE1*

```
280:                EECMOSP
281:                PMOS
282:         LEVEL    8
283:             L   100.000000E-06
284:             W   100.000000E-06
285:           VTO    -.4
286:            KP   414.377300E-06
287:         GAMMA    0
288:           PHI
289:        LAMBDA    0
290:           RSH    1.000000E+03
291:            IS    1.000000E-15
292:            JS   35.100000E-09
293:          JSSW   35.100000E-09
294:            PB     .94
295:          PBSW     .94
296:            CJ   528.000000E-06
297:          CJSW   119.000000E-12
298:          MJSW     .5
299:          CGSO   450.000000E-12
300:          CGDO   450.000000E-12
301:          CGBO   575.000000E-12
302:          NSUB    50.000000E+15
303:           TOX     5.000000E-09
304:            XJ    50.000000E-09
305:         UCRIT    10.000000E+03
306:        DIOMOD    1
307:           VFB    -1
308:          LETA    0
309:          WETA    0
310:            U0   100
311:          TEMP
312:           VDD
313:         XPART    0
314:          VTH0    -.4
315:            UA    1.000000E-09
316:            UB   100.000000E-21
317:            UC   -46.500000E-12
318:          VSAT    80.000000E+03
319:          RDSW   200
320:          VOFF    -.08
321:          PCLM    5
322:            A0    1
323:            A1    0
324:            A2    1
325:         NPEAK   100.000000E+15
```

```
326:            XT   50.000000E-09
327:           LDD    0
328:          LITL   27.386130E-09
329:           UA1    1.000000E-09
330:           UB1   -1.000000E-18
331:           UC1     .025
332:          DSUB     .56
333:         NGATE   500.000000E+18
334:        MOBMOD    0
335:          PRWG    1
336:          LINT   10.000000E-09
337:          WINT   10.000000E-09
338:           DLC   10.000000E-09
339:           DWC   10.000000E-09
340:            CF   107.725800E-12
341:          NOIA    9.900001E+18
342:          NOIB    2.400000E+03
343:          NOIC    1.400000E-12
344:       VERSION    4.1
345:          PBSWG     .94
346:          MJSWG     .5
347:          CJSWG   119.000000E-12
348:          JTSCD   35.100000E-09
349:         JSTSCD   35.100000E-09
350:           TOXM    3.000000E-09
351:            LLC    0
352:            LWC    0
353:           LWLC    0
354:            WLC    0
355:            WWC    0
356:           WWLC    0
357: BSIM4oxideTrapDensityC    8.750000E+09
358:           toxp    3.000000E-09
359:             eu    1
360:           aigc     .31
361:           bigc     .024
362:           cigc     .03
363:          aigsd     .31
364:          bigsd     .024
365:          cigsd     .03
366:          dlcig   10.000000E-09
367:            dwj   10.000000E-09
368:         CJSWGD   500.000000E-12
369:         PBSWGD    1
370:         CJSWGS   500.000000E-12
368:         CJSWGD   500.000000E-12
369:         PBSWGD    1
370:         CJSWGS   500.000000E-12
371:         PBSWGS    1
372:           coxe     .01151
373:           coxp     .01151
374: BSIM4factor1    94.868330E-06
```

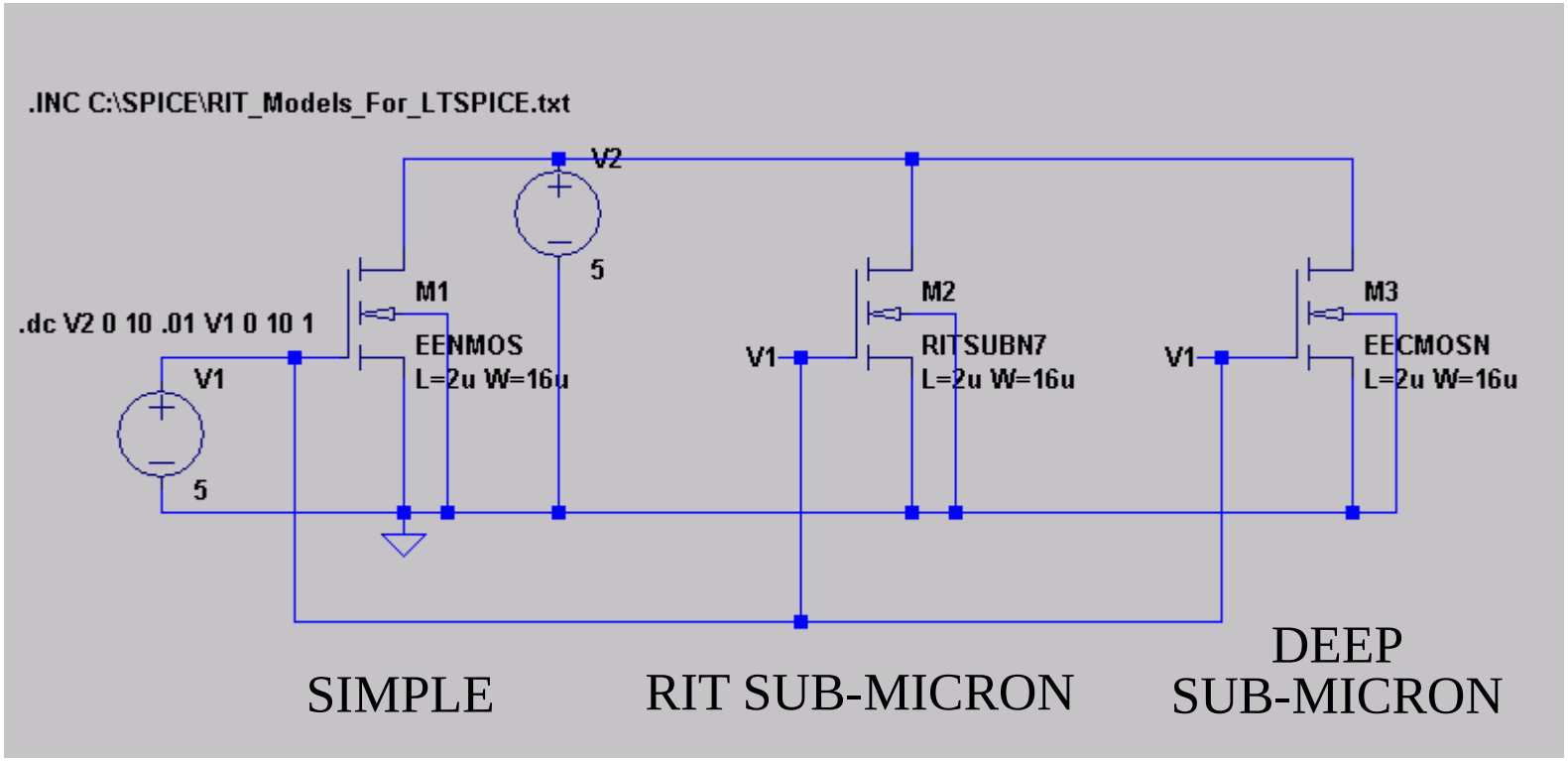
View Output File

31 mosfet model parameters used by cadence PSPICE for Level 1 Shichman and Hodges

FullerMOS..* | PAGE1* | ID-VGS-SW... | SCHEMATI..* | ID-VGS-S...

	EENMOS	EEPMOS
	NMOS	PMOS
LEVEL	1	1
L	100.000000E-06	100.000000E-06
W	100.000000E-06	100.000000E-06
VTO	.4	-.4
KP	432.000000E-06	122.000000E-06
GAMMA	.2	.2
PHI	.88	.88
LAMBDA	0	0
RSH		
IS	10.000000E-15	10.000000E-15
JS	0	0
JSSW		
PB	.8	.8
PBSW	.8	.8
CJ	0	0
CJSW	0	0
MJSW		
CGSO	0	0
CGDO	0	0
CGBO	0	0
NSUB		
TOX	0	0
XJ	0	0
UCRIT	10.000000E+03	10.000000E+03
DIOMOD	1	1
VFB	0	0
LETA	0	0
WETA	0	0
U0	0	0
TEMP	0	0
VDD	5	5
XPART	0	0

LTSPICE CIRCUIT SCHEMATIC

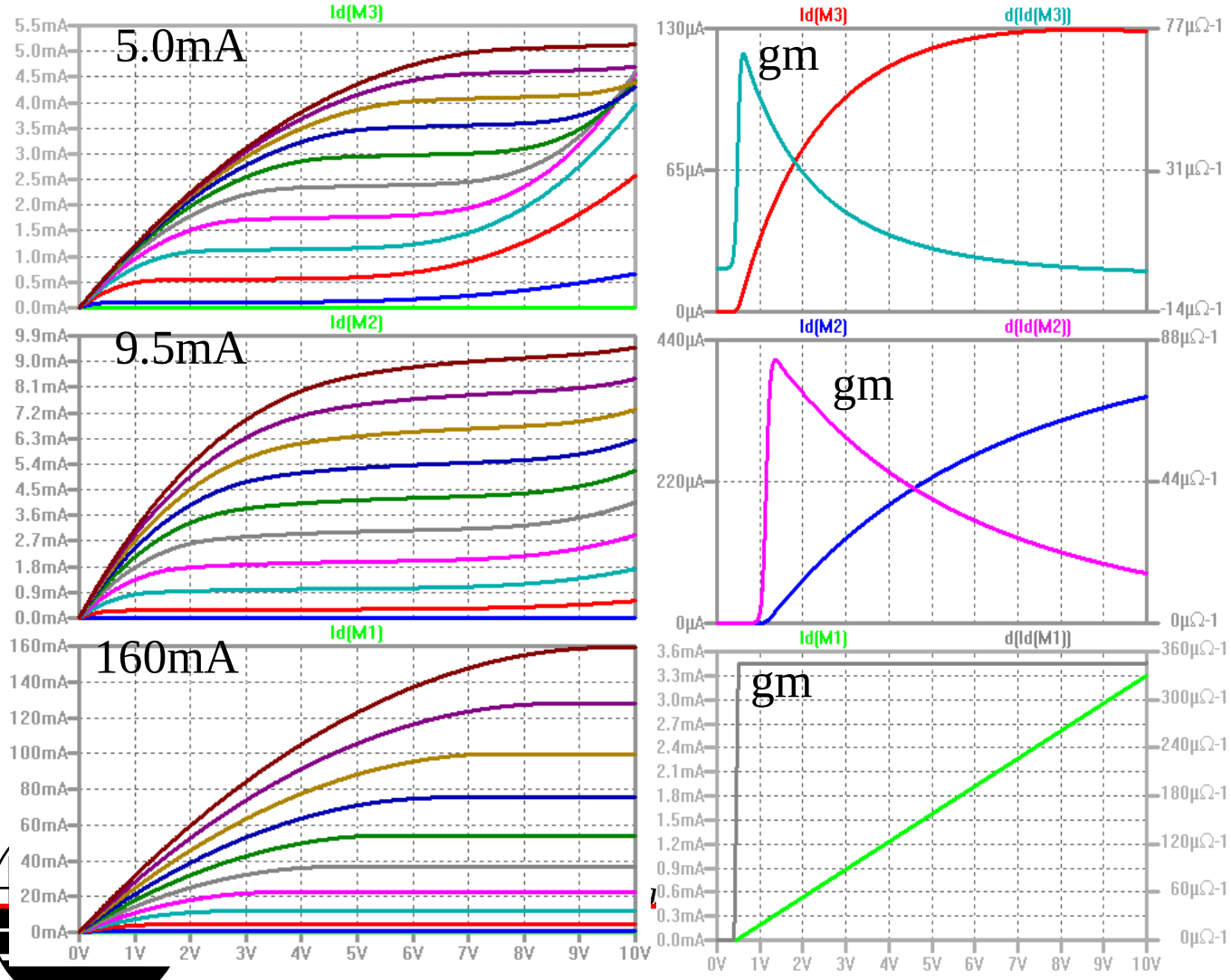


Three transistor all the same L=2u and W=16u but with different SPICE models. (SIMPLE, RIT SUB-MICRON and 100nm DEEP SUB-MICRON

THREE DIFFERENT NMOS SPICE MODELS

```
* From Sub-Micron CMOS Manufacturing Classes in MicroE
.MODEL RITSUBN7       NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
* From Electronics II EEEE482 FOR ~100nm Technology Deep Sub-Micron
.model EECMOSN        NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
* From Electronics II EEEE482 SIMPLE MODEL
.model EENMOS NMOS (VTO=0.4 KP=432E-6 GAMMA=0.2 PHI=.88)
```

LTSPICE OUTPUT FOR ID-VDS AND ID-VG



Model is EECMOSN
L=2u W=16u

Model not good.
Current low and only good out to 3 volts.

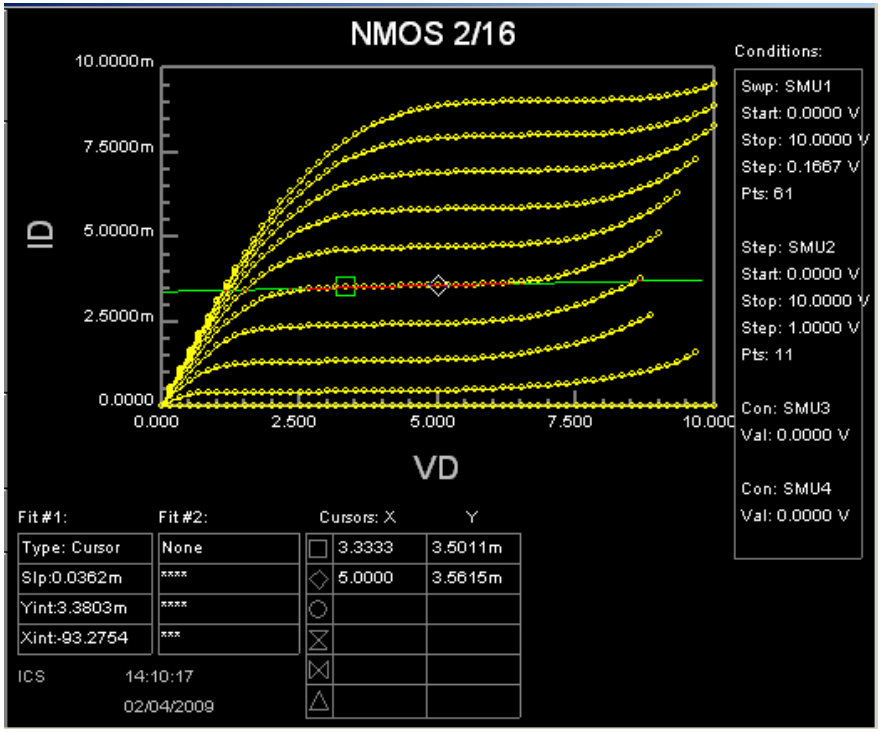
Model is RITSUBN7
L=2u W=16u

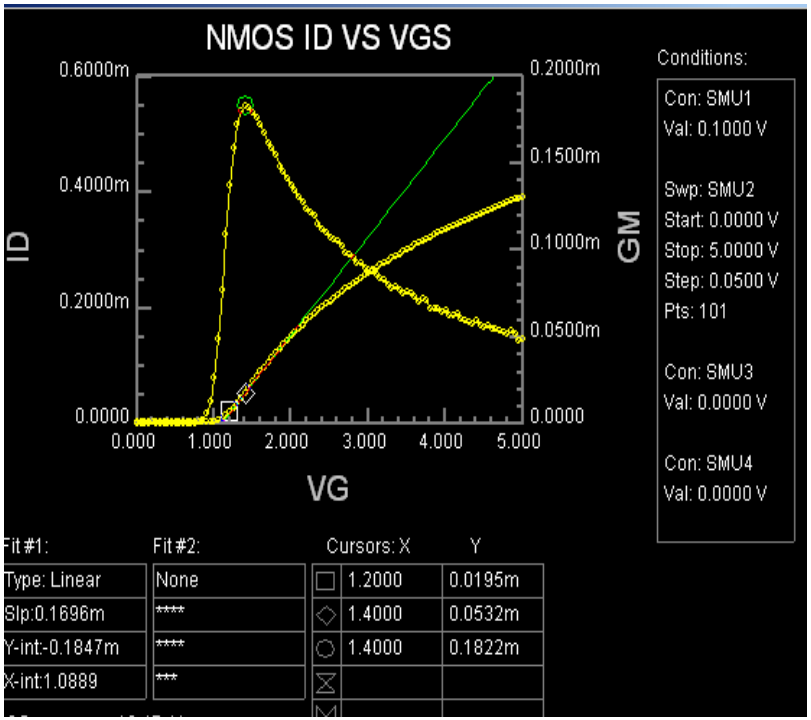
Model good for RIT Sub-Micron MOSFETs

Model is EENMOS
L=2u W=16u

Model not good current too large

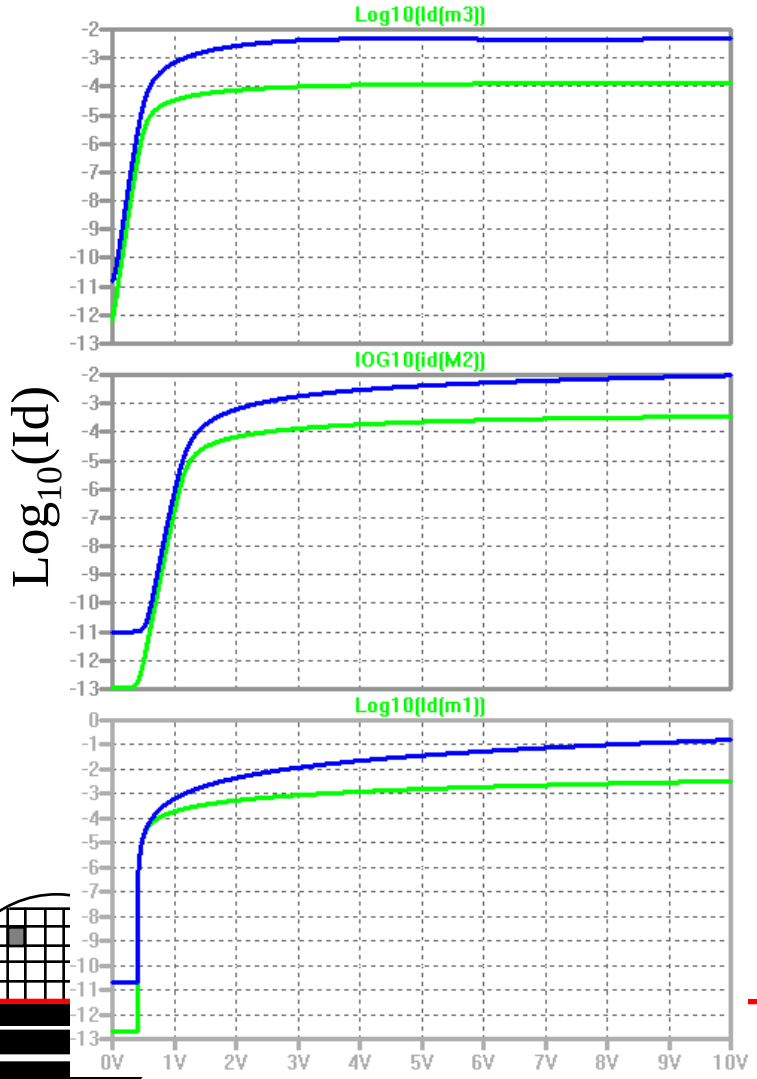
MEASURED MOSFET ID-VDS AND ID-VGS





Imax = 9.5mA

LTSPICE OUTPUT FOR SUBTHRESHOLD ID-VGS



Model is EECMOSN
L=2u W=16u

Model not good MOSFET does not turn off, Vt too low

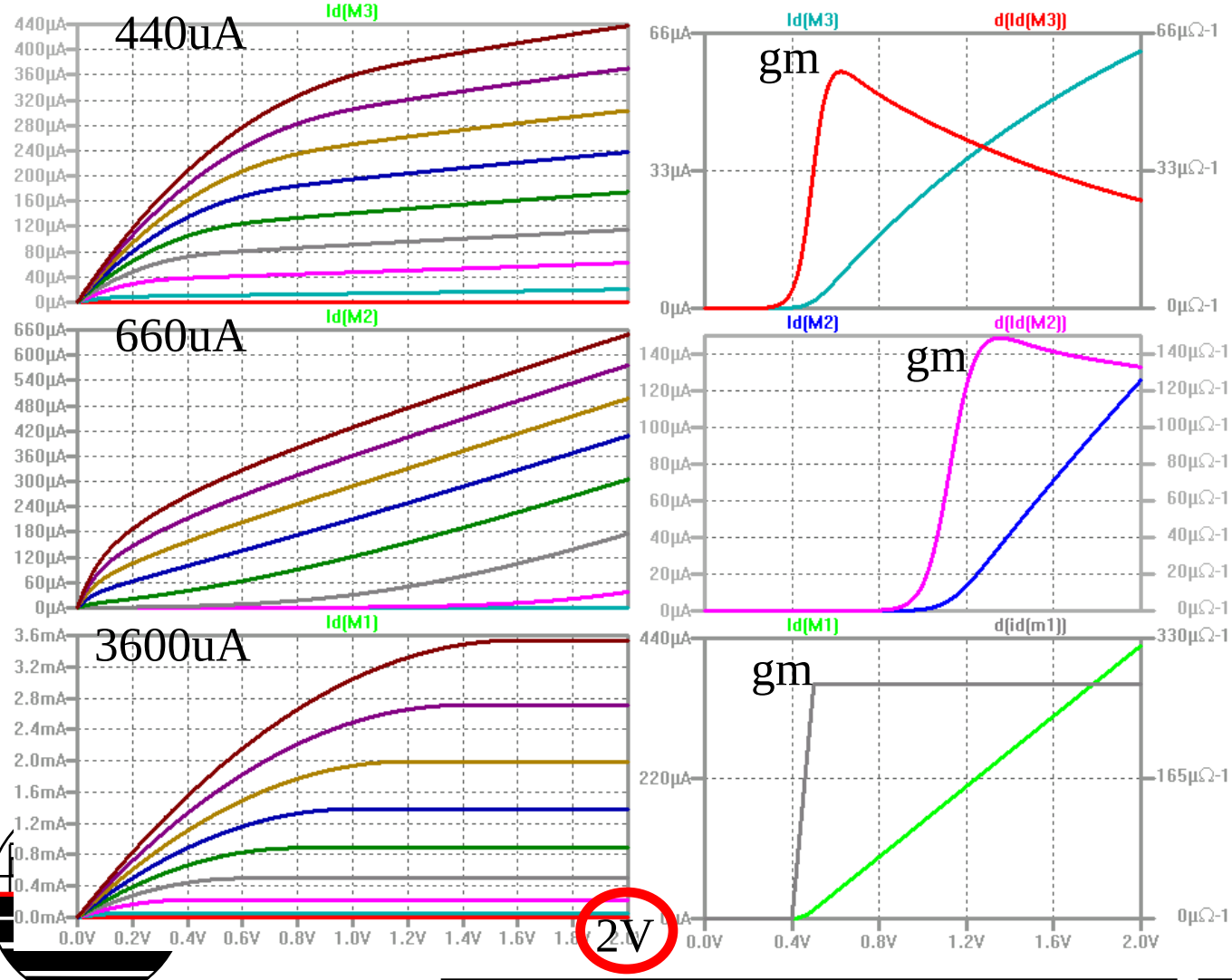
Model is RITSUBN7
L=2u W=16u

Model good

Model is EENMOS
L=2u W=16u

Model incorrect in subthreshold region.
Subthreshold slope not possible.

DEEP SUB-MICRON TRANSISTOR MODELS



Model is EECMOSN
L=0.25u W=1.6u

Model good for Deep Sub-Micron MOSFETs

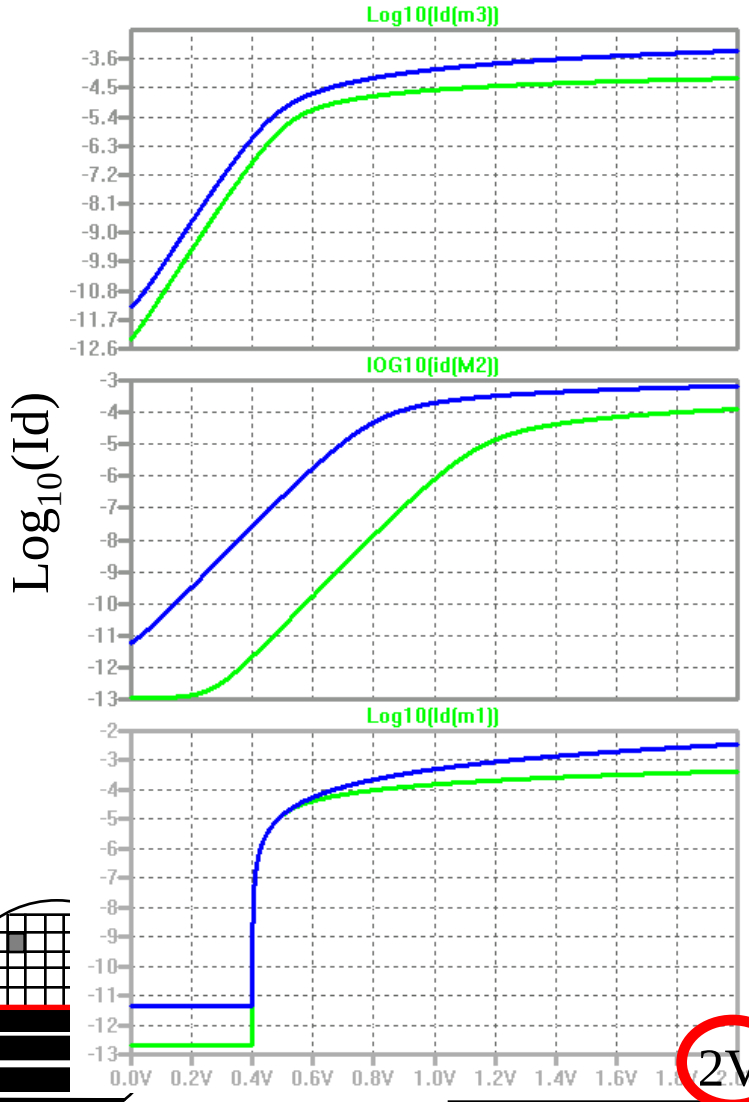
Model is RITSUBN7
L=0.25u W=1.6u

Model not good too much short channel effects

Model is EENMOS
L=0.25u W=1.6u

Model not good current too large does not show mobility degradation

DEEP SUB-MICRON TRANSISTOR MODELS



$Log_{10}(Id)$

Model is EECMOSN
L=0.25u W=1.6u

Model good for Deep Sub-Micron MOSFETs

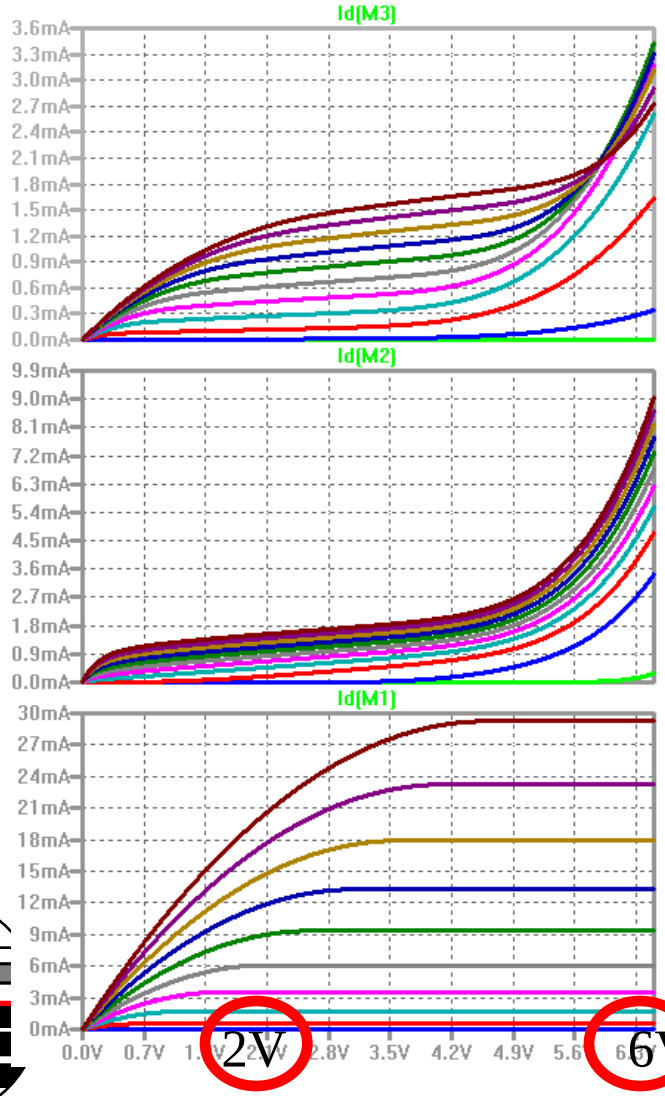
Model is RITSUBN7
L=0.25u W=1.6u

Model not good too much DIBL

Model is EENMOS
L=0.25u W=1.6u

Model incorrect in subthreshold region

DEEP SUB-MICRON TRANSISTOR MODELS



Deep sub-micron transistors show punch through at drain voltages over 3.3 volts. Which is correct.

Problem is worse in the sub-micron transistor because the channel is lighter doped.

Simple model is incorrect.

MOSFET MODELS USED BY LTSPICE

LTSPICE uses several different types of MOSFET models including simple, deep submicrometer, Silicon On Insulator (SOI), Vertical double diffused Power MOSFET. Level = 1 is the default if a model level is not specified.

Level

1 Shichman and Hodges
2 MOS2, Vladimirescu and Liu, UC Berkeley, October 1980
3 MOS3, a semi-emperical model, UC Berkeley

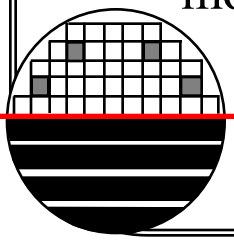
} 1st generation models

4 BSIM UC Berkeley, May 1985
5 BSIM2, UC Berkeley, October 1990
6 MOS6, UC Berkeley, March 1990

} 2nd generation models

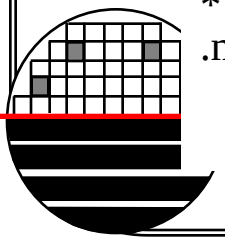
8 BSIM3V3.3.0, UC Berkeley 2005
9 BSIMSOI3.2, Silicon on Insulator (SOI), UC Berkeley 2004
14 BSIM4.6.1, UC Berkeley 2007
more….

} 3rd generation models

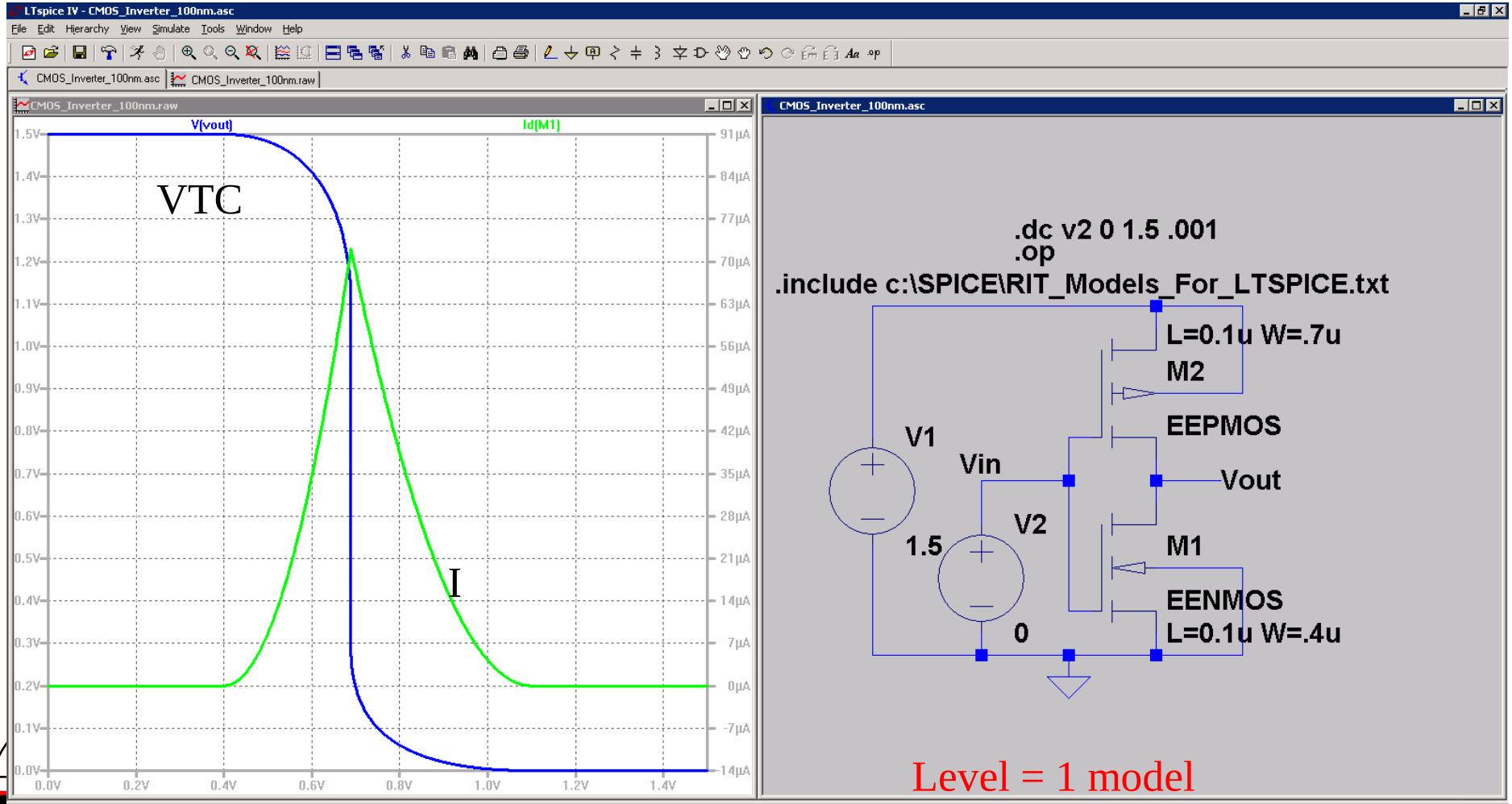


SIMPLE AND ADVANCED SPICE MODEL

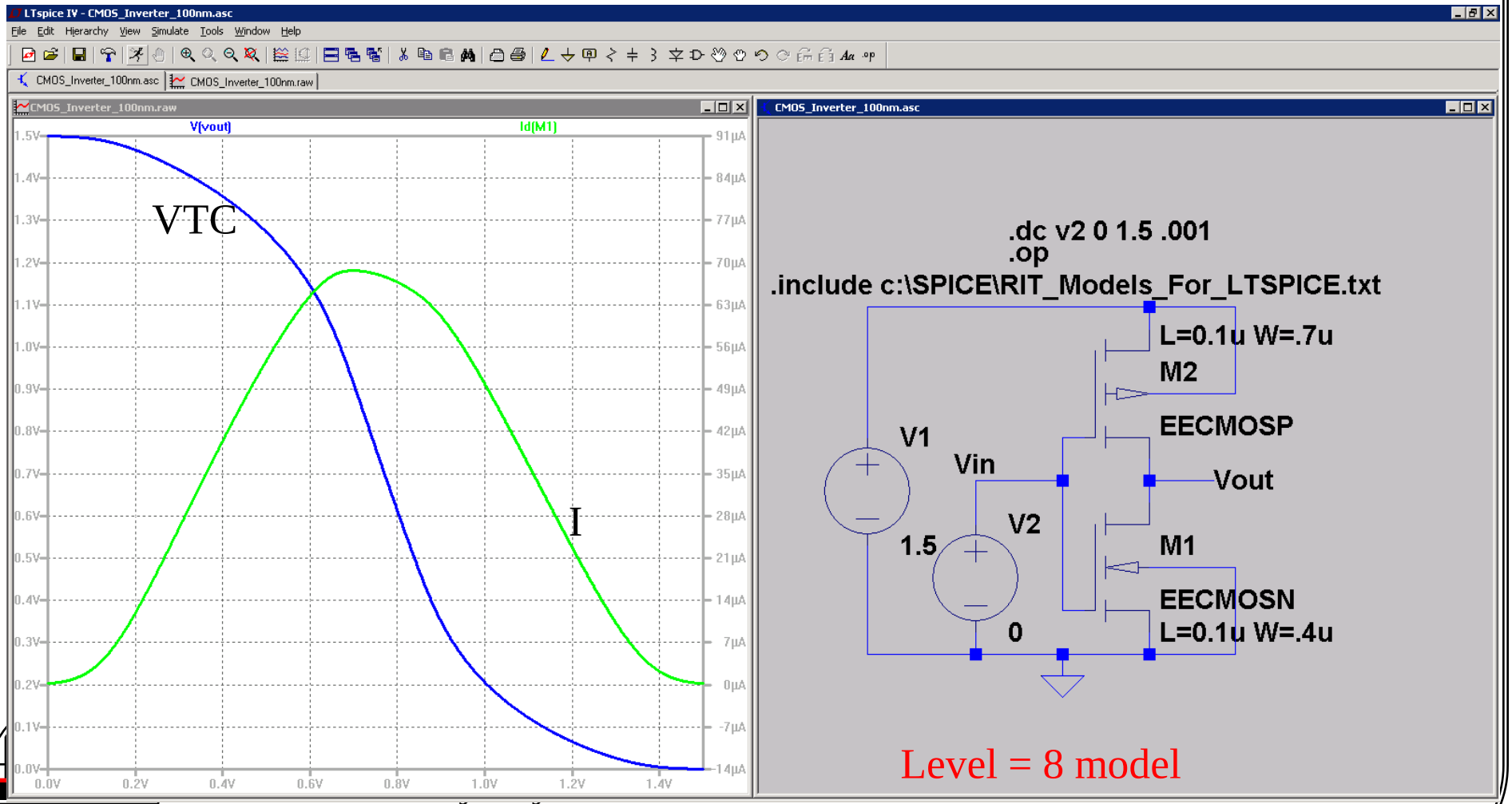
```
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSN     NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSP      PMOS (LEVEL=8
+TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
* From Electronics II EEEE482 SIMPLE MODEL
.model EENMOS       NMOS (VTO=0.4 KP=432E-6 GAMMA=0.2 PHI=.88)
*
* From Electronics II EEEE482 SIMPLE MODEL
.model EEPMOS       PMOS (VTO=-0.4 KP=122E-6 GAMMA=0.2 PHI=.88)
```



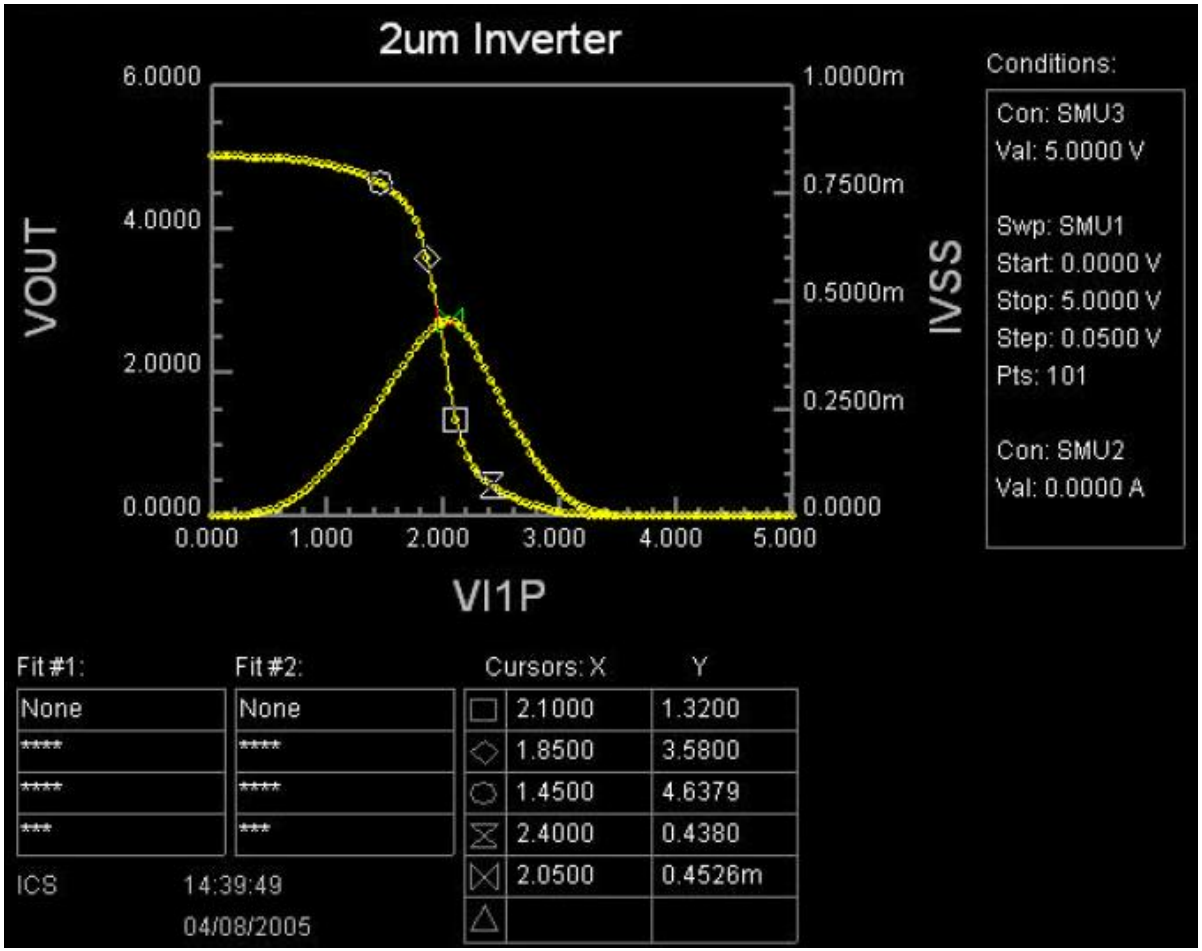
CMOS INVERTER WITH LEVEL 1 SPICE MODEL



CMOS INVERTER WITH LEVEL 8 SPICE MODEL

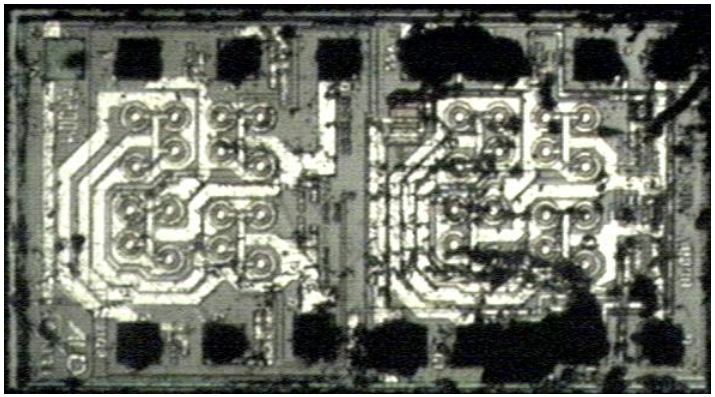


MEASURED VTC L=2um W=40um CMOS INVERTER



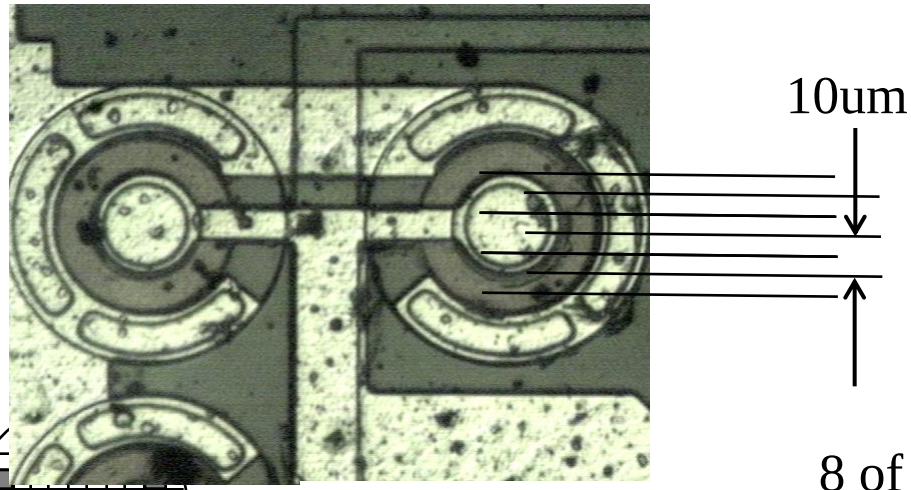
L=2u and W=40u

ADVANCED LINEAR DEVICES ALD 1103



PMOS NMOS

The Advanced Linear Devices ALD1103 is a dual NMOS and PMOS matched pair in a 14 pin package. The ALD 1101 is a dual NMOS matched pair and the ALD 1102 is a dual PMOS matched pair. The 1101/1102 are in an 8 pin package. One chip design for all three products.



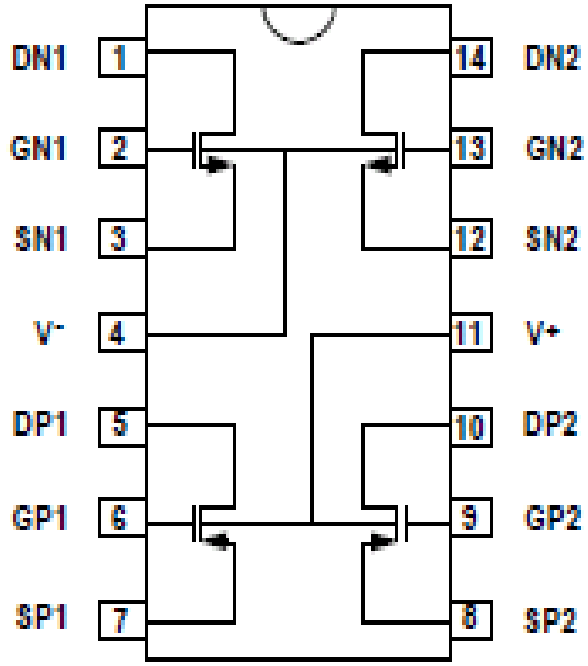
MOSFET

L=10um
W diameter = 35um
W each = Pi D = 110um
W total = 8 x 110 = 880um

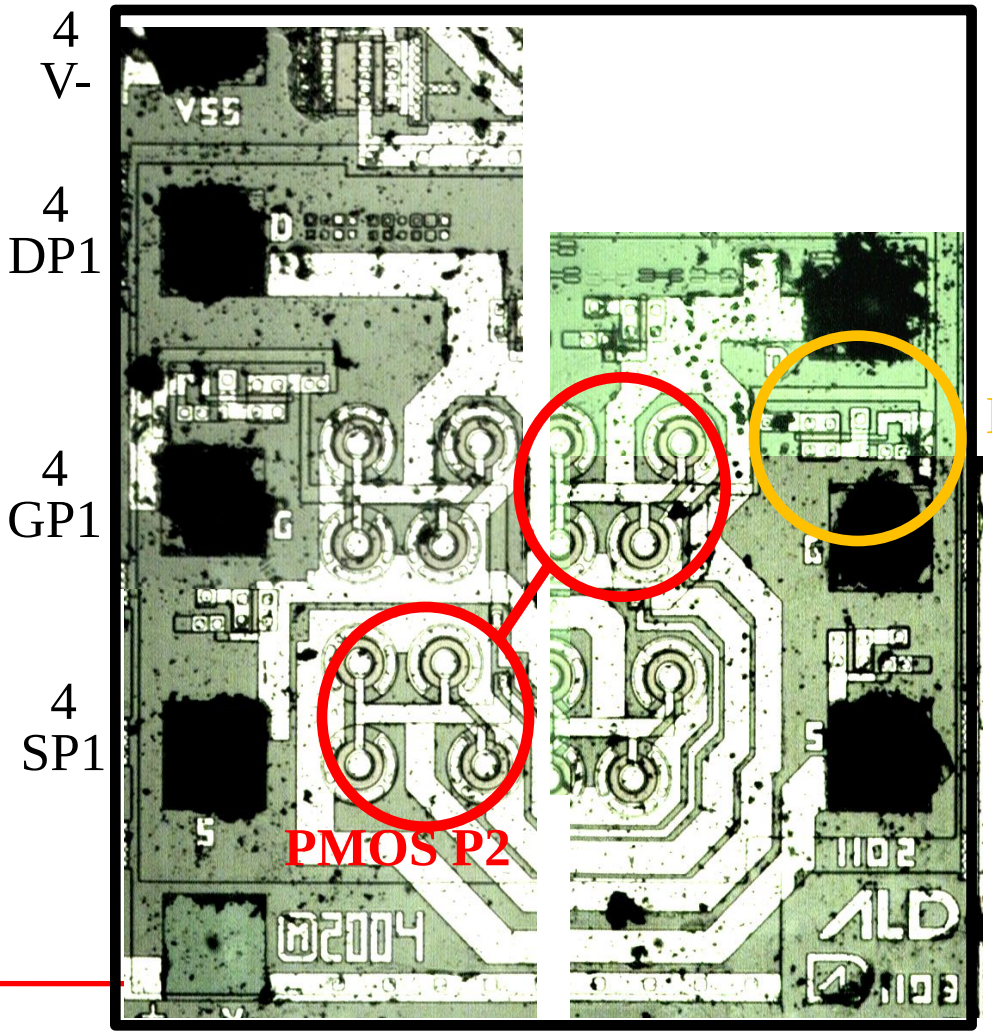
8 of the donut shaped MOSFETs in parallel form one transistor.

ALD1103 LAYOUT

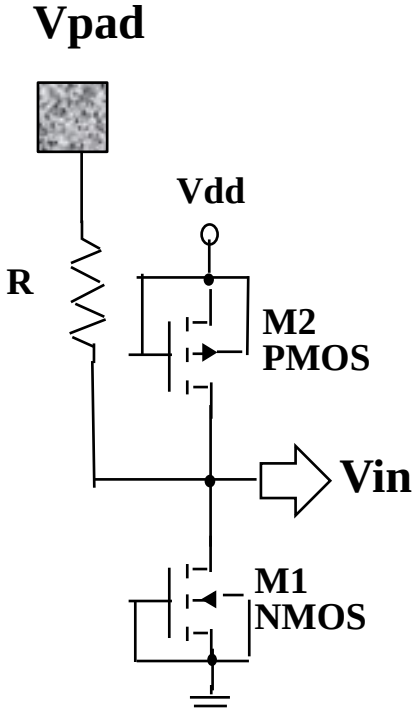
PIN CONFIGURATION



DB, PB, SB PACKAGE



ELECTROSTATIC DISCHARGE - INPUT PAD

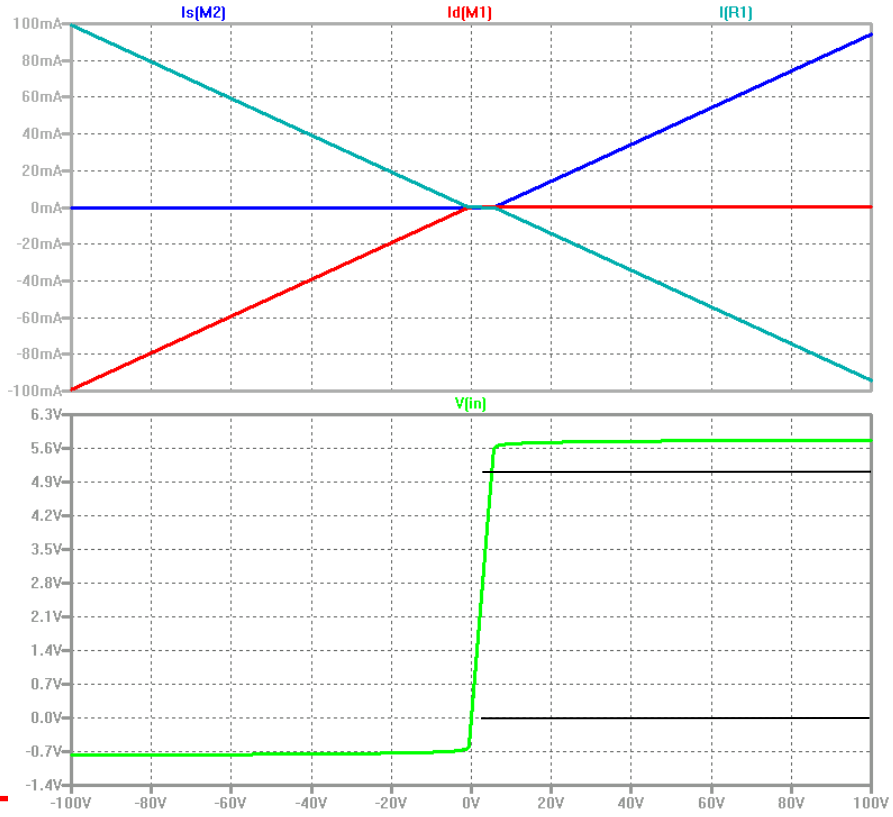


Simulation for Vpad sweep from -100 to +100 volts
Vin is between -1 and +6 Volts and I is through M1 and M2 if Vpad exceeds supply voltages

100mA

0 mA

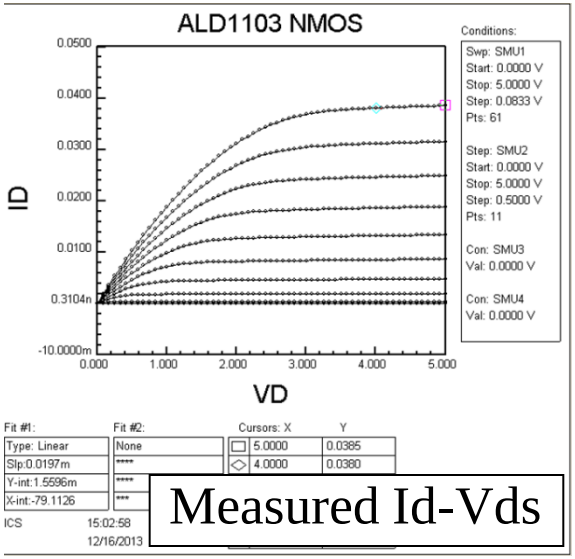
-100mA



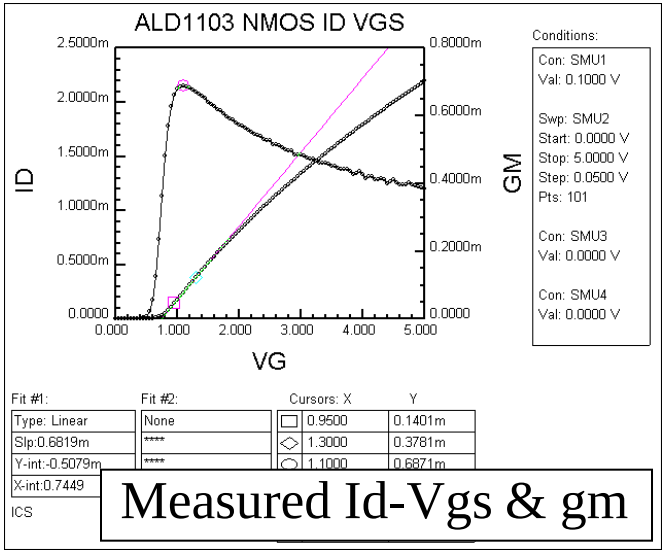
+5V

0V

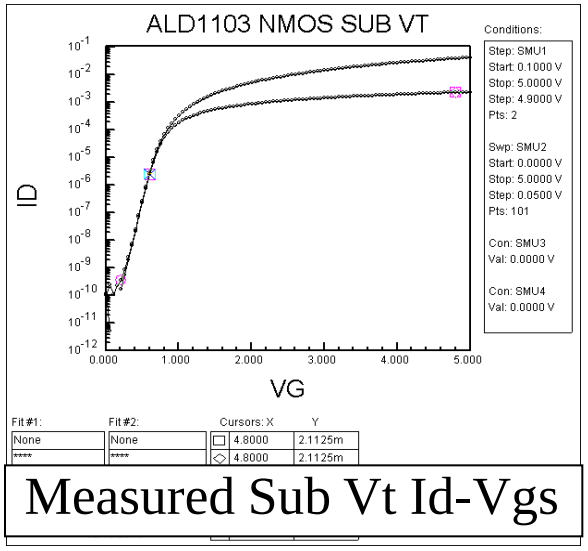
ALD1103 MATCHED NMOS AND PMOS MOSFETS



Measured Id-Vds



Measured Id-Vgs & gm



Measured Sub Vt Id-Vgs

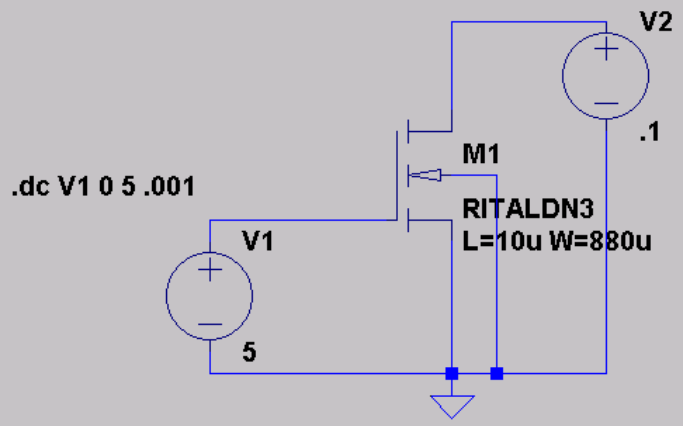
.MODEL RITALDN3 NMOS (LEVEL=3
+TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0= 1215 VTO=0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5
+NSUB=1.57E16 +XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)

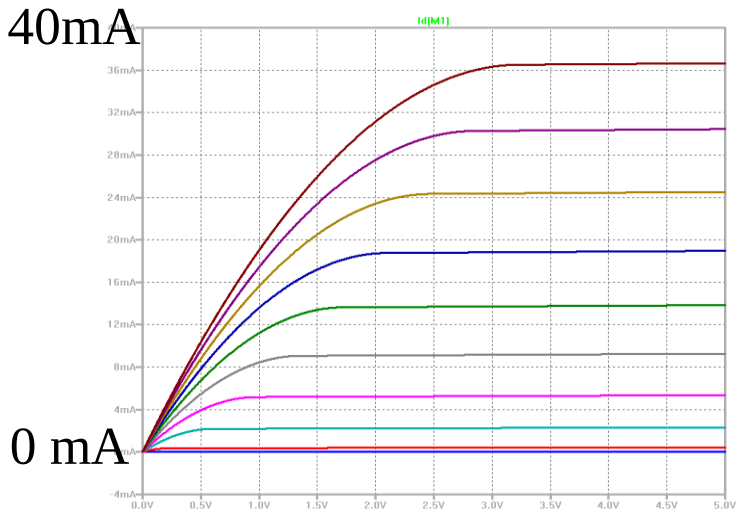
Using a LEVEL=3 model should give good results since L is long, LEVEL 1 OR 2 will not work

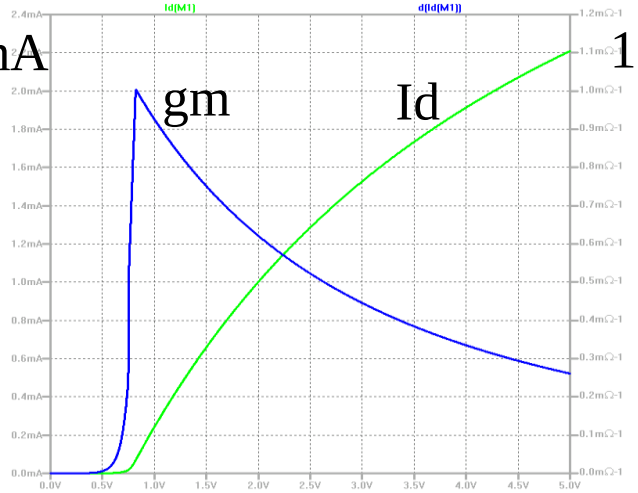
From Dr. Fullers SPICE MOSFET Model Parameter Calculator. xls.

ALD1103 LEVEL=3 NMOS SPICE MODEL AND SIMULATION

```
.MODEL RITALDN3 NMOS (LEVEL=3 TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0= 1215 VTO=0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5 NSUB=1.57E16
+XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)
```







This SPICE model gives good matching between measured and simulated curves.

CD4007 DUAL COMPLEMENTARY PAIR + INVERTER

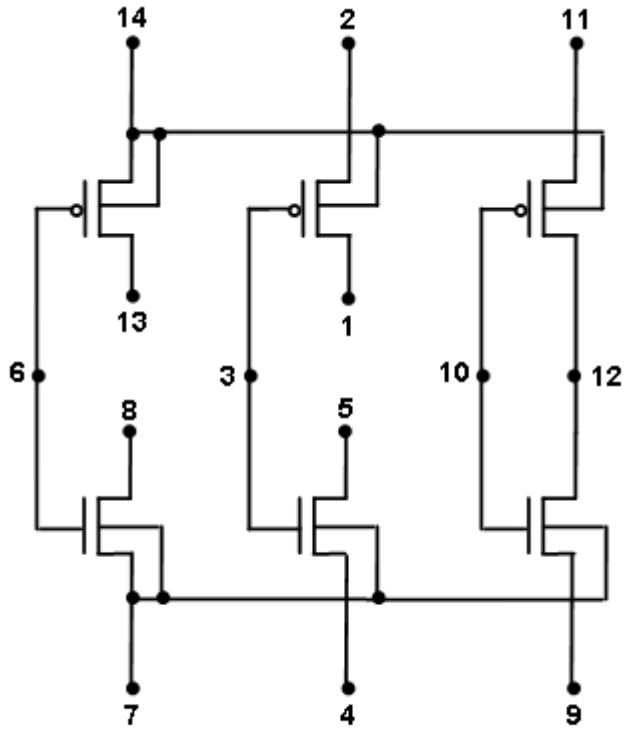
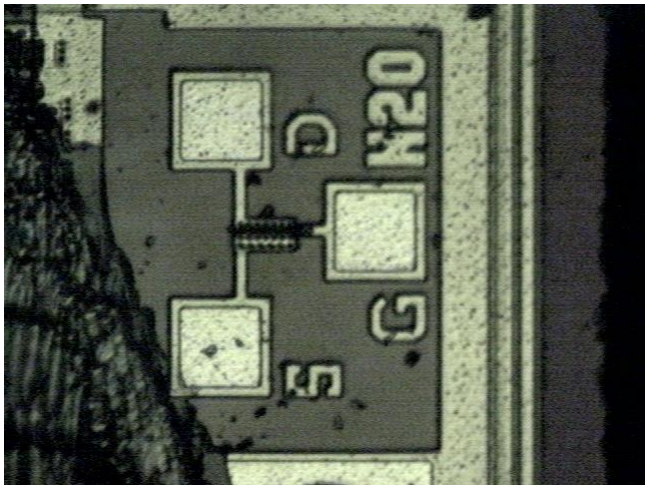
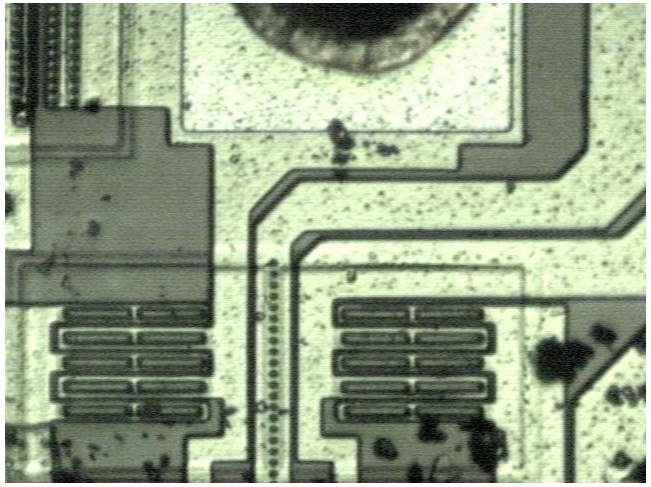
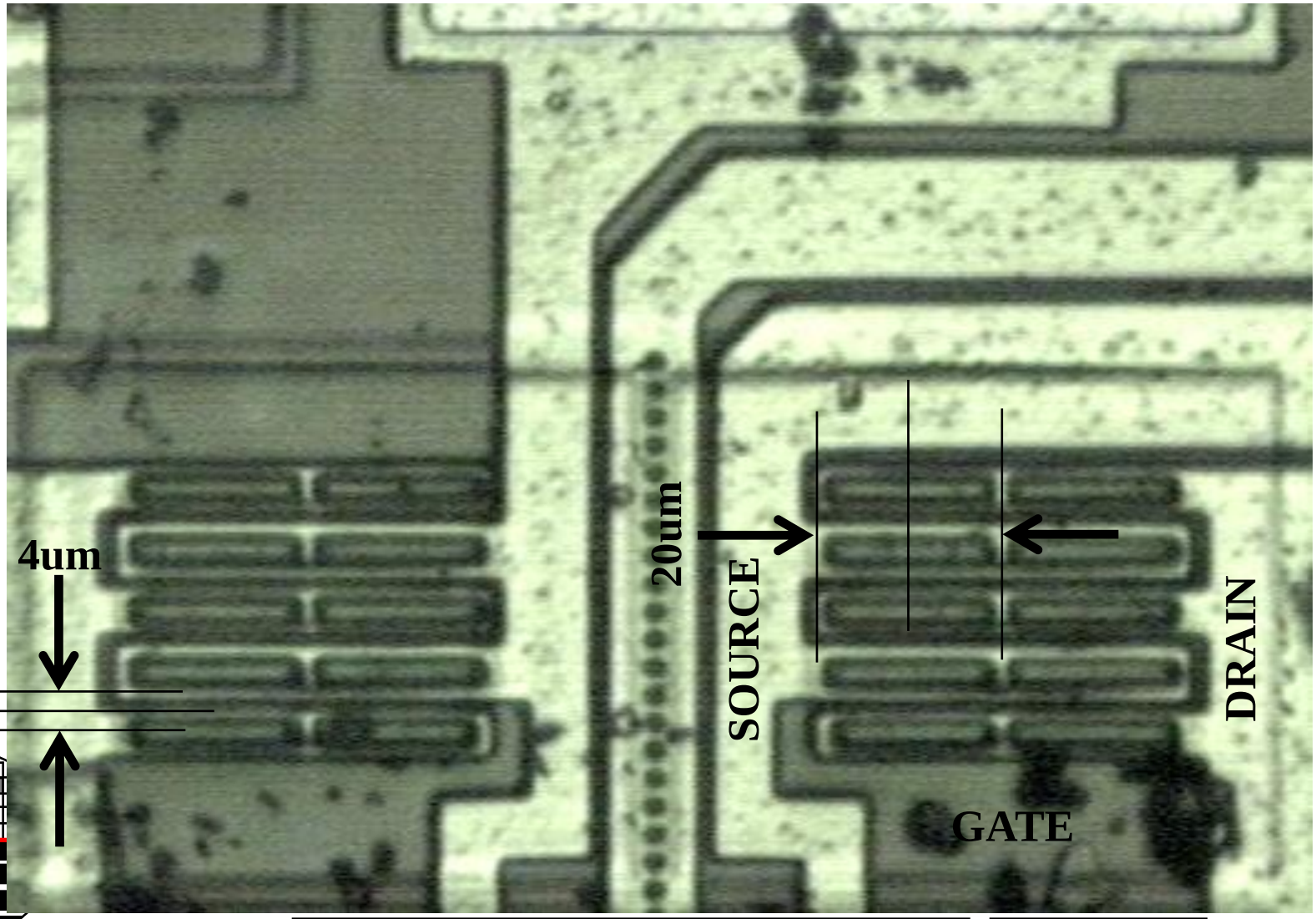


Figure 4(a). Enlarged CD4007 Pin-Out Diagram

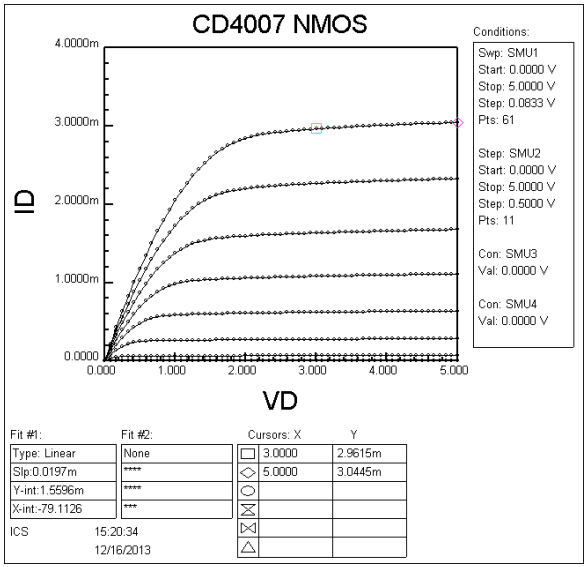


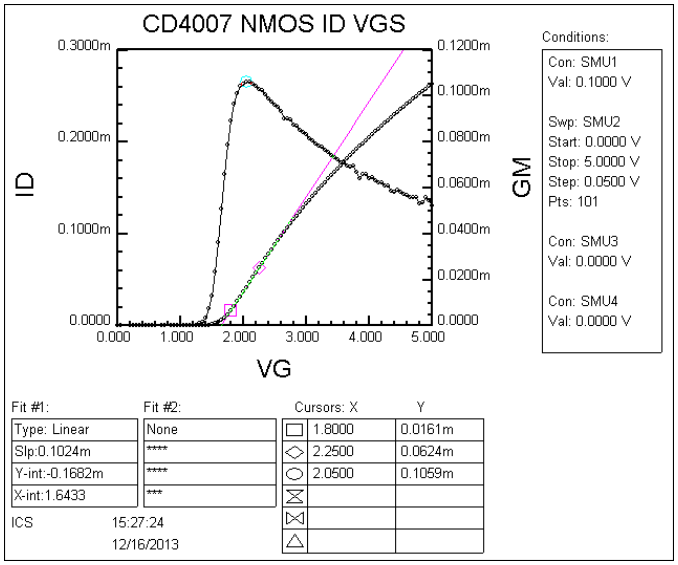


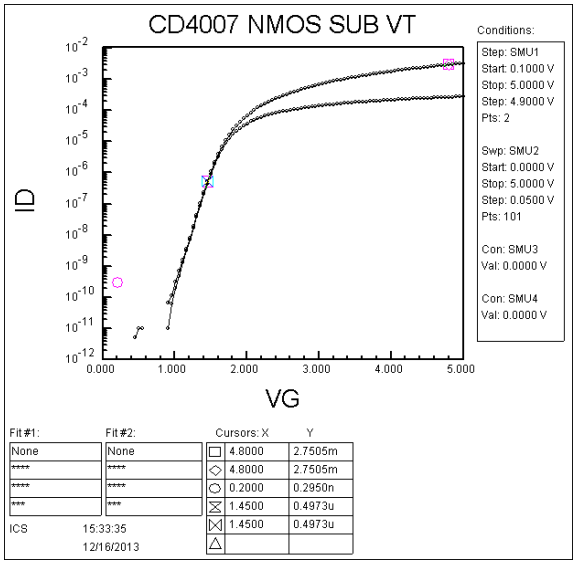
CD4007 DUAL COMPLEMENTARY PAIR + INVERTER



CD4007 DUAL COMPLEMENTARY PAIR + INVERTER

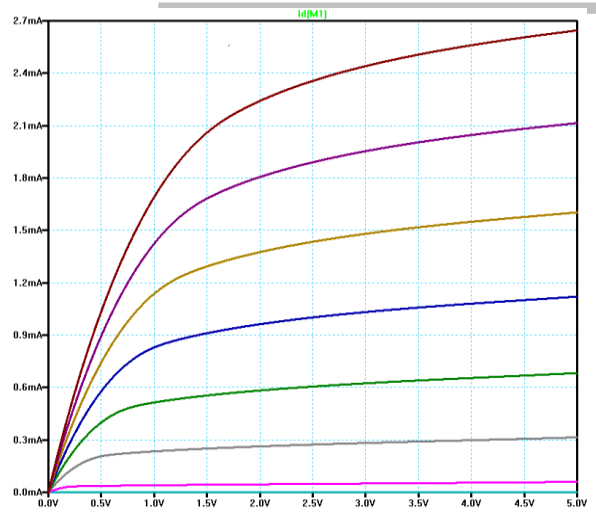


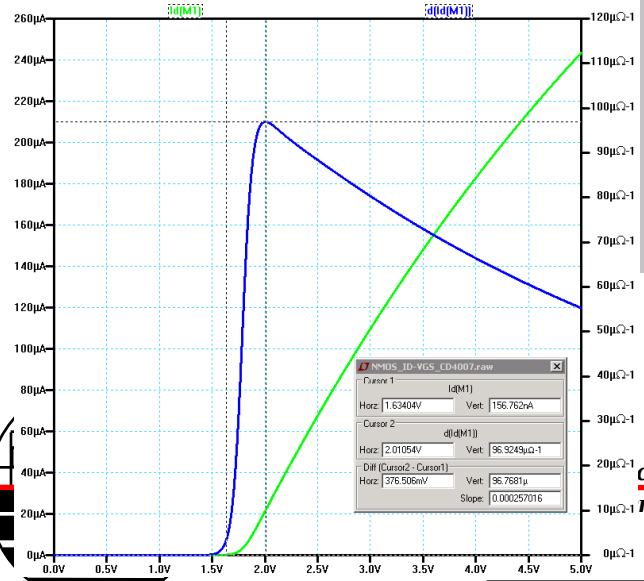




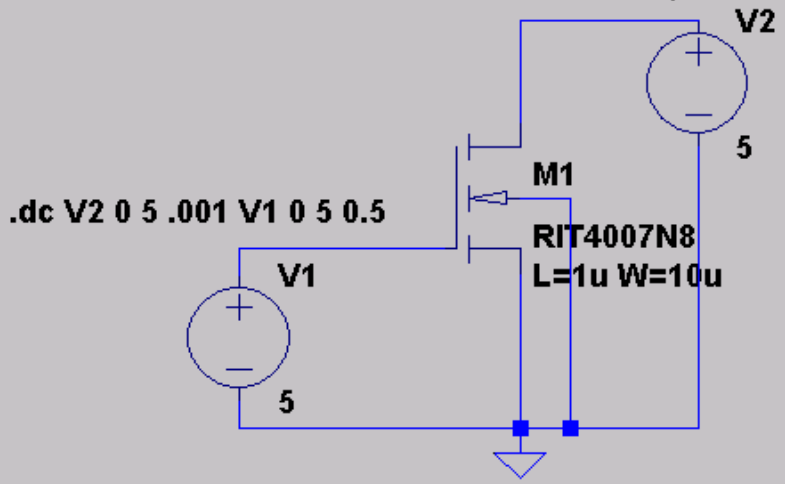

```
.MODEL RIT4007N8 NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
```

CD4007 DUAL COMPLEMENTARY PAIR + INVERTER






```
.MODEL RIT4007N8 NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.6 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
```



.dc V2 0 5 .001 V1 0 5 0.5

chnology
ring

SUMMARY

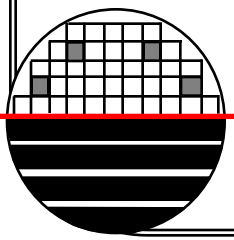
All of these examples are for DC characteristics but similar results would be shown for examples that depend on internal capacitors and resistors such as a study of rise-time, fall time, gate delay, oscillators, multi-vibrators, etc.

In general the third generation SPICE models for MOSFETS give better results.

Level=1 models are not good for MOSFETS with L less than 10um.

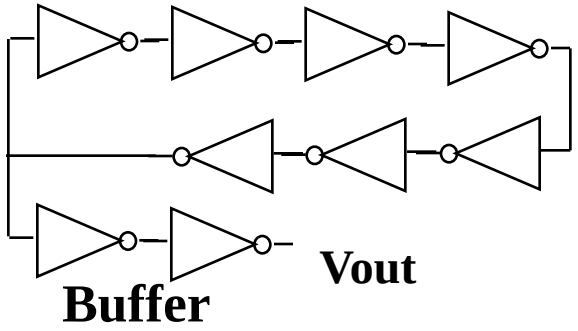
Large MOSFETS, SUB-MICRON MOSFETS and DEEP SUB MICRON MOSFET models have been introduced.

Models should be verified by comparing measured ID-VDS, ID-VGS, and Ring Oscillator output with SPICE simulated results.



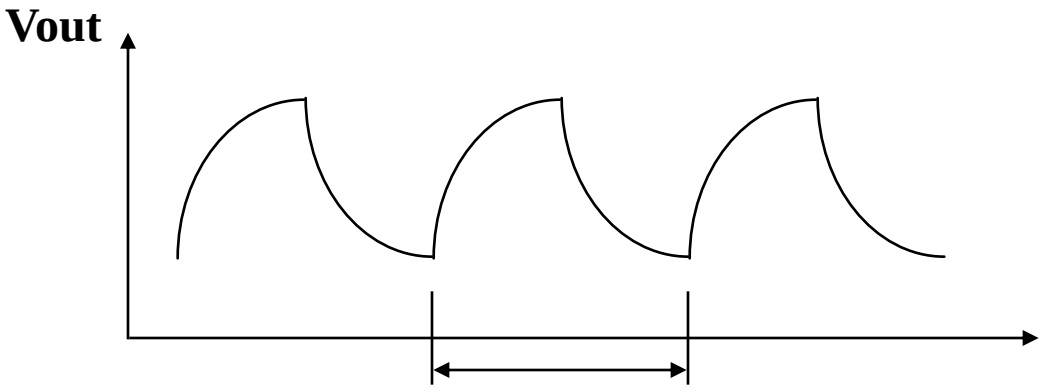
RING OSCILLATOR, td, THEORY

Seven stage ring oscillator with two output buffers



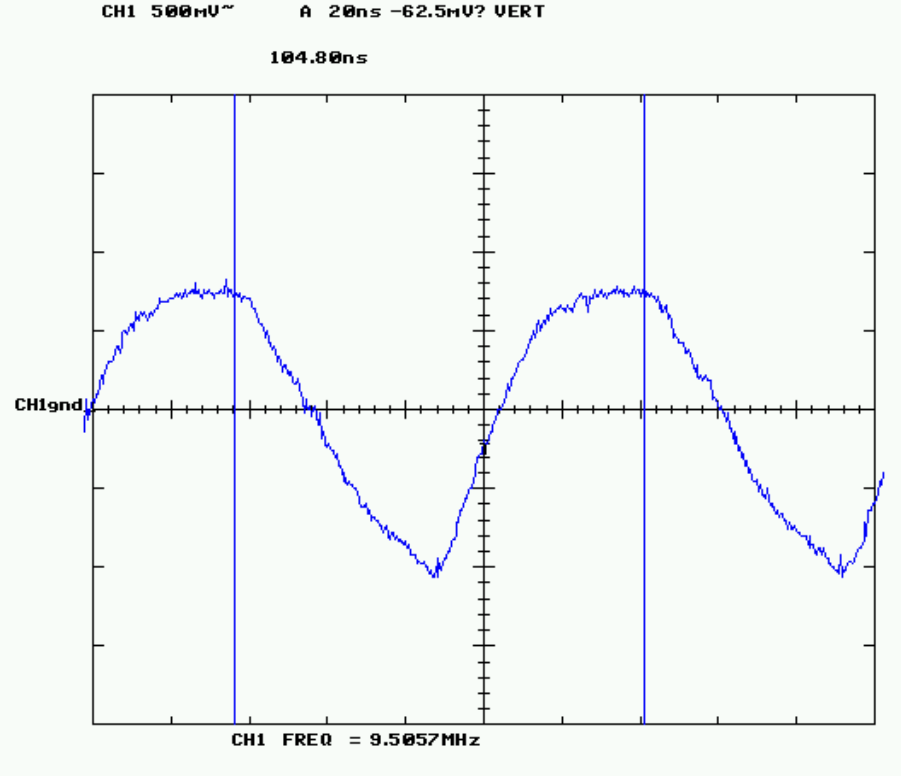
td = T / 2 N

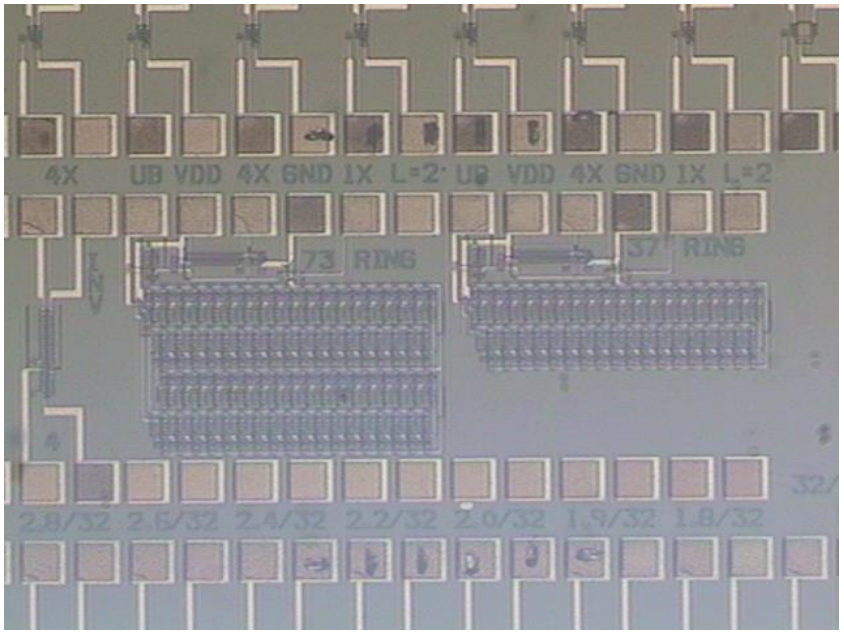
td = gate delay
N = number of stages
T = period of oscillation



T = period of oscillation

MEASURED RING OSCILLATOR OUTPUT





73 Stage Ring at 5V

td = 104.8ns / 2(73) = 0.718 ns

AC MODEL FOR MOSFETS

The parameters that effect the AC response of a MOSFET are the resistance and capacitance values.

RS,RS	Source/Drain Series Resistance, ohms
RSH	Sheet Resistance of Drain/Source, ohms
CGSO,CGDO	Zero Bias Gate-Source/Drain Capacitance, F/m of width
CGBO	Zero Bias Gate-Substrate Capacitance, F/m of length
CJ	DS Bottom Junction Capacitance, F/m2
CJSW	DS Side Wall Junction Capacitance, F/m of perimeter
MJ	Junction Grading Coefficient, 0.5
MJSW	Side Wall Grading Coefficient, 0.5

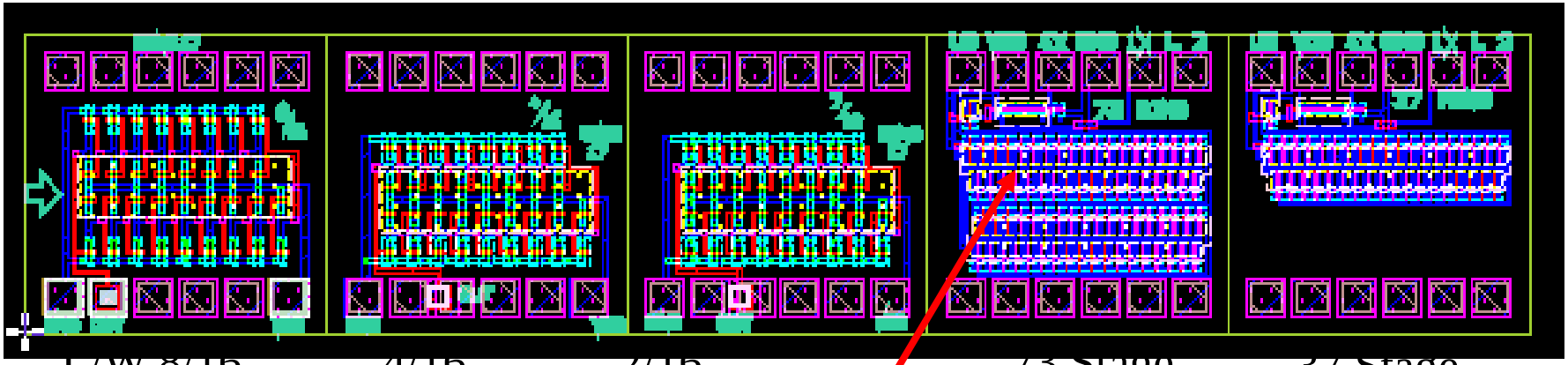
These are combined with the transistors

L, W	Length and Width
AS,AD	Area of the Source/Drain
PS,PD	Perimeter of the Source/Drain
NRS,NRD	Number of squares Contact to Channel

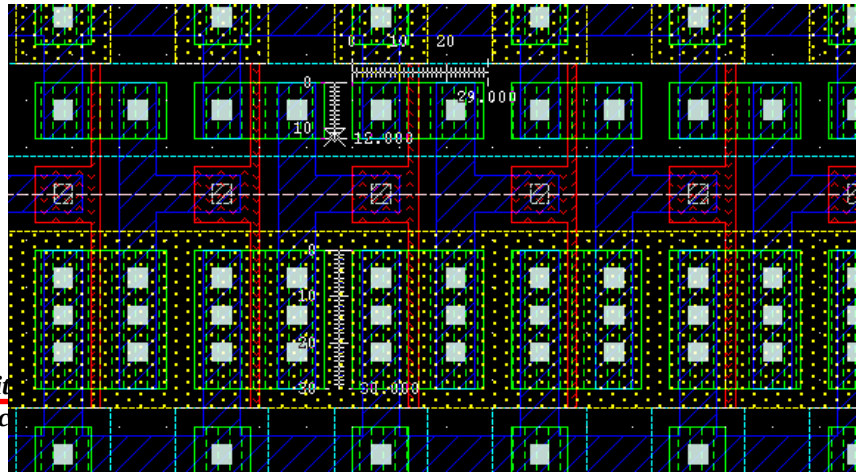
RING OSCILLATOR LAYOUTS

17 Stage Un-buffered Output

L/W=2/30 Buffered Output

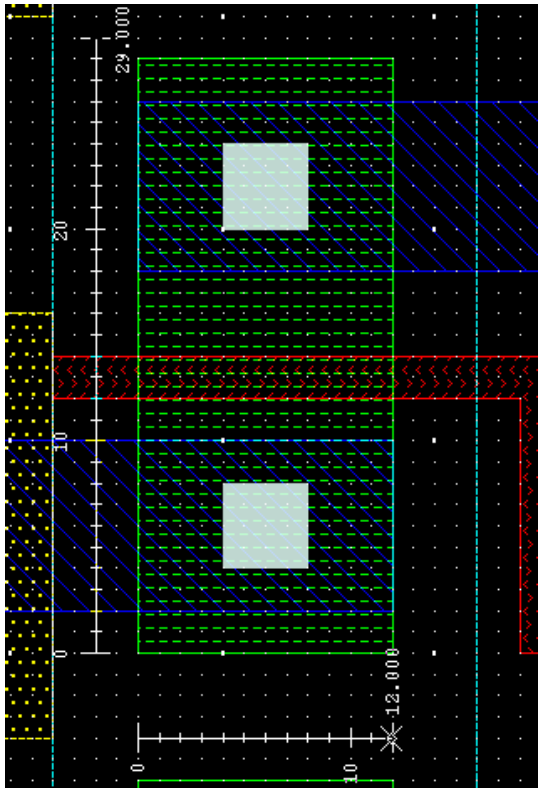


L/W 8/16 4/16 2/16 73 Stage 37 Stage

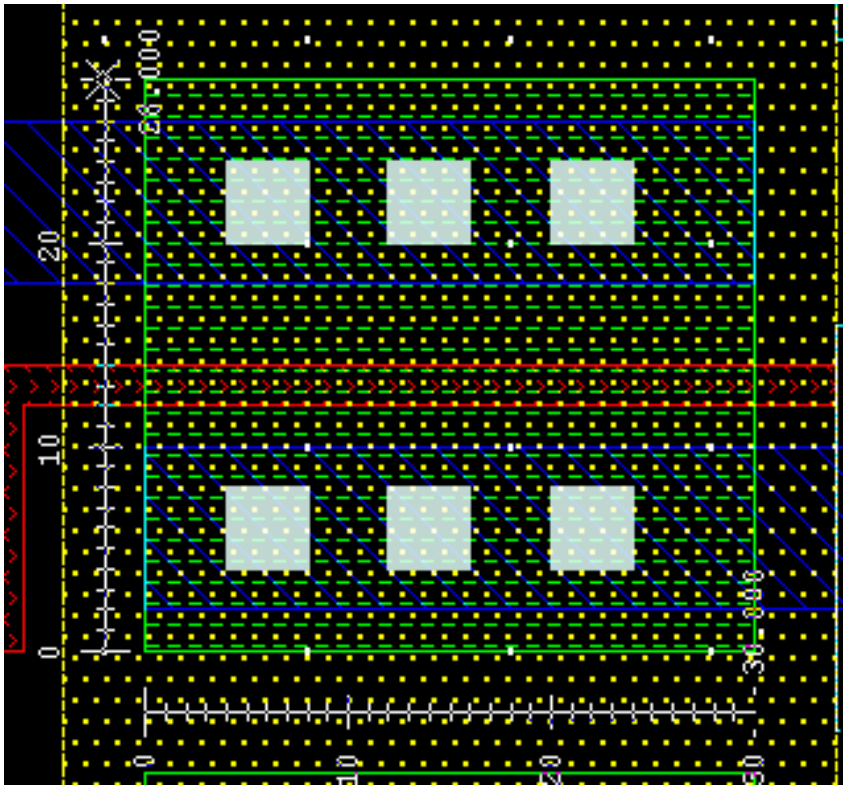


MOSFETS IN THE INVERTER OF 73 RING OSCILLATOR

nmosfet



pmosfet



73 Stage Ring Oscillator

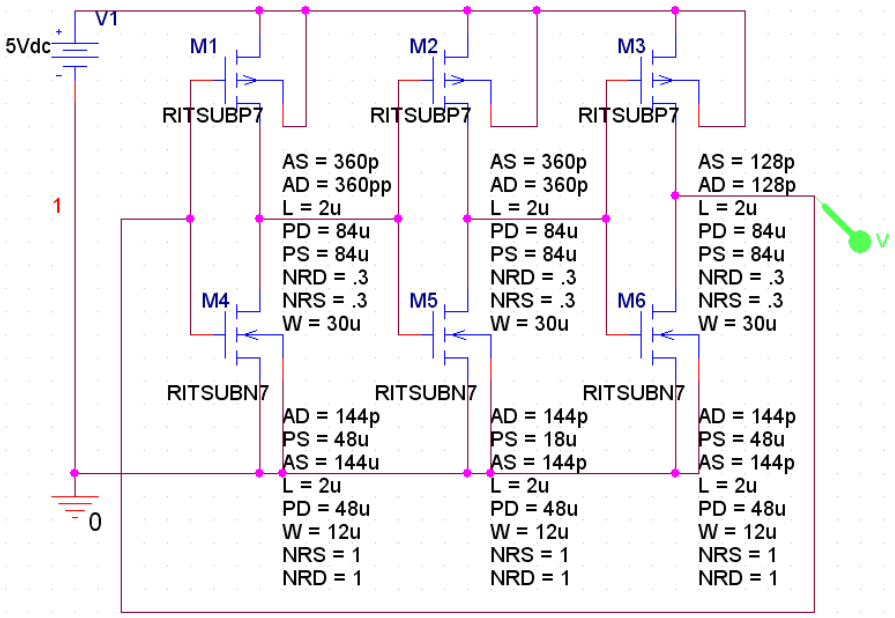
FIND DIMENSIONS OF THE TRANSISTORS

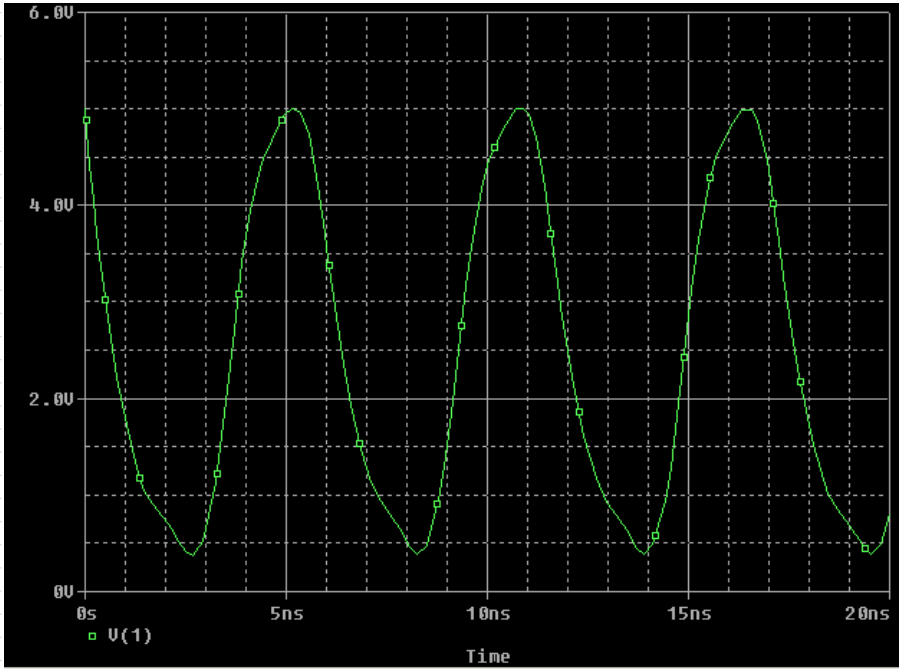
73 Stage

	NMOS	PMOS
L	2u	2u
W	12u	30u
AD	12ux12u=144p	12ux30u=360p
AS	12ux12u=144p	12ux30u=360p
PD	2x(12u+12u)=48u	2x(12u+30u)=84u
PS	2x(12u+12u)=48u	2x(12u+30u)=84u
NRS	1	0.3
NRD	1	0.3

Use Ctrl Click on all NMOS on OrCad Schematic
Use Ctrl Click on all PMOS on OrCad Schematic
Then Enter Dimensions

SIMULATED OUTPUT AT 5 VOLTS





Three Stage Ring Oscillator with Transistor Parameters for 73 Stage Ring Oscillator and Supply of 5 volts

Measured td = 0.718 nsec @ 5 V

td = T / 2N = 5.5nsec / 2 / 3
td = 0.92 nsec

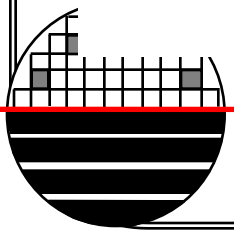
CONCLUSION

Since the measured and the simulated gate delays, td are close to correct, then the SPICE model must be close to correct. The inverter gate delay depends on the values of the internal capacitors and resistances of the transistor.

Specifically:
RS, RS, RSH
CGSO, CGDO, CGBO
CJ, CJSW

These are combined with the transistors

L, W	Length and Width
AS,AD	Area of the Source/Drain
PS,PD	Perimeter of the Source/Drain
NRS,NRD	Number of squares Contact to Channel



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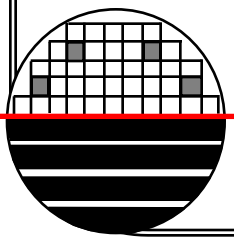
2. Operation and Modeling of the MOS Transistor, 2nd Edition, Yannis Tsividis, 1999, McGraw-Hill, ISBN-0-07-065523-5
3. UTMOST III Modeling Manual-Vol.1. Ch. 5. From Silvaco International.
4. ATHENA USERS Manual, From Silvaco International.
5. ATLAS USERS Manual, From Silvaco International.
6. Device Electronics for Integrated Circuits, Richard Muller and Theodore Kamins, with Mansun Chan, 3rd Edition, John Wiley, 2003, ISBN 0-471-59398-2
7. ICCAP Manual, Hewlet Packard
8. PSpice Users Guide.



HOMEWORK – INTRO TO MOSFET SPICE MODELS

Do SPICE for one of the following:

1. Inverter gate delay is the time it takes for the output voltage to get to ½ of the supply voltage. Use SPICE to get a value for gate delay for rising and falling output. Let L=2um and W=40um for both NMOS and PMOS transistors. State other assumptions. Compare these values to gate delay measured from a ring oscillator.

2. Do a SPICE simulation for the CMOS inverter shown on page 38 and compare to measured VTC and I vs Vin.