ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

# More SPICE Examples

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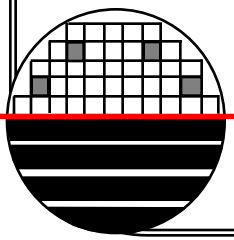
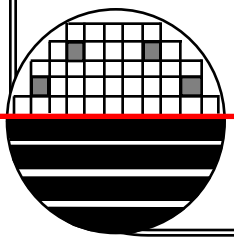


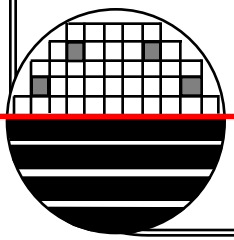
# *ADOBE PRESENTER*

This PowerPoint module has been published using Adobe Presenter. Please click on the Notes tab in the left panel to read the instructors comments for each slide. Manually advance the slide by clicking on the play arrow or pressing the page down key.



# OUTLINE





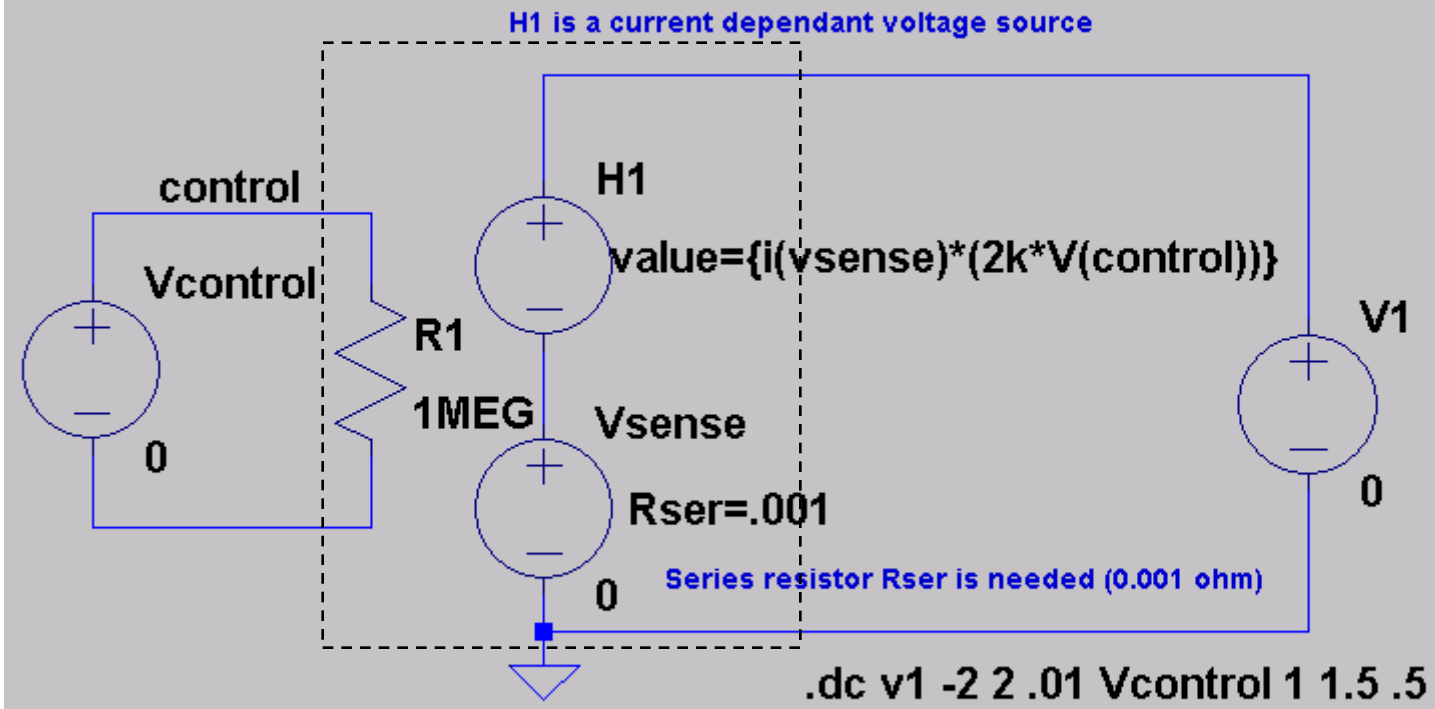
# *INTRODUCTION*

PSpice Lite 9.2 is one of the OrCAD family of products, from Cadence Design Systems, Inc., offering a complete suite of electronic design tools. It is free and includes limited versions of OrCAD Capture, for schematic capture, PSpice for analog circuit simulation and Pspice A/D for mixed analog and digital circuit simulation. PSpice Lite 9.2 is limited to 64 nodes, 10 transistors, two operational amplifiers and 65 primitive digital devices. See page 35 (xxxv) of the PSpice Users Guide.

LT SPICE – is a free SPICE simulator with schematic capture from Linear Technology. It is quite similar to PSpice Lite but is not limited in the number of devices or nodes. Linear Technology (LT) is one of the industry leaders in analog and digital integrated circuits. Linear Technology provides a complete set of SPICE models for LT components.

# VOLTAGE CONTROLLED RESISTOR

Voltage Controlled Resistor inside dashed box

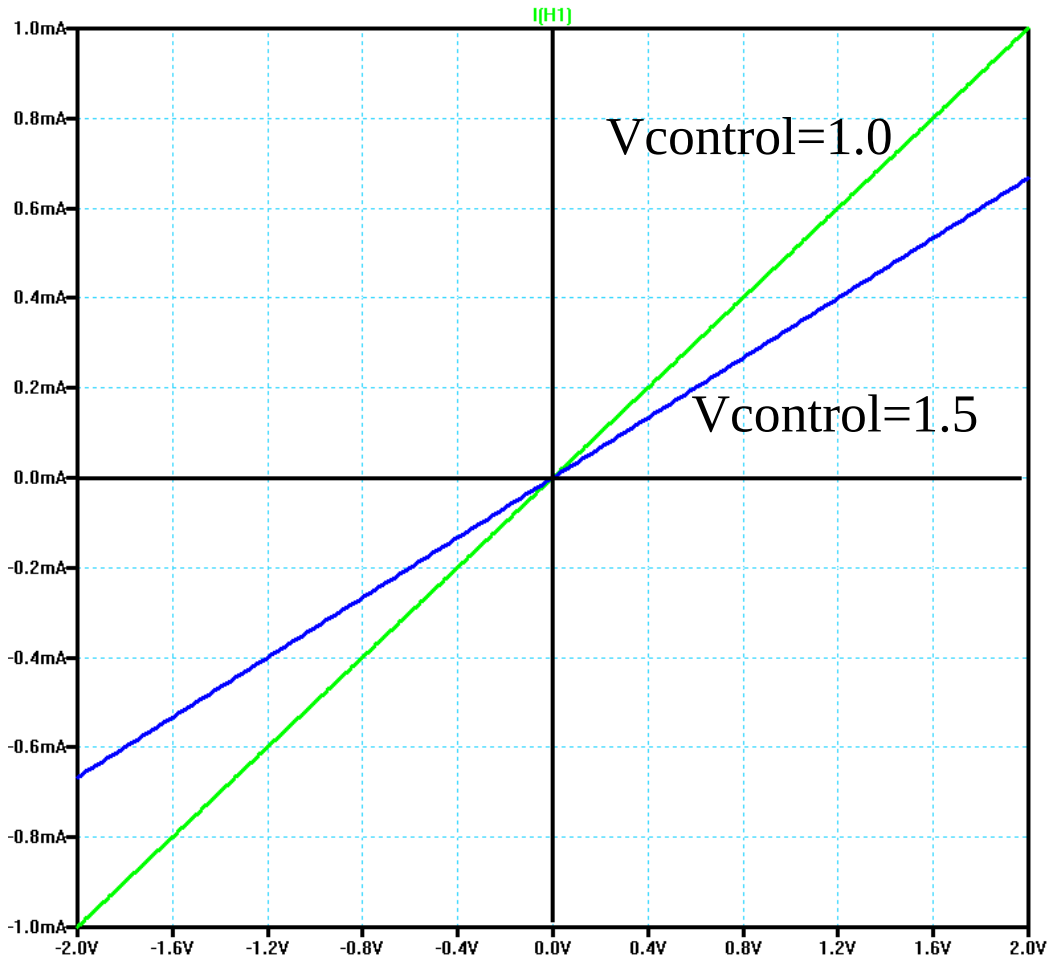



V1 is to test I-V Characteristics

# VOLTAGE CONTROLLED RESISTOR

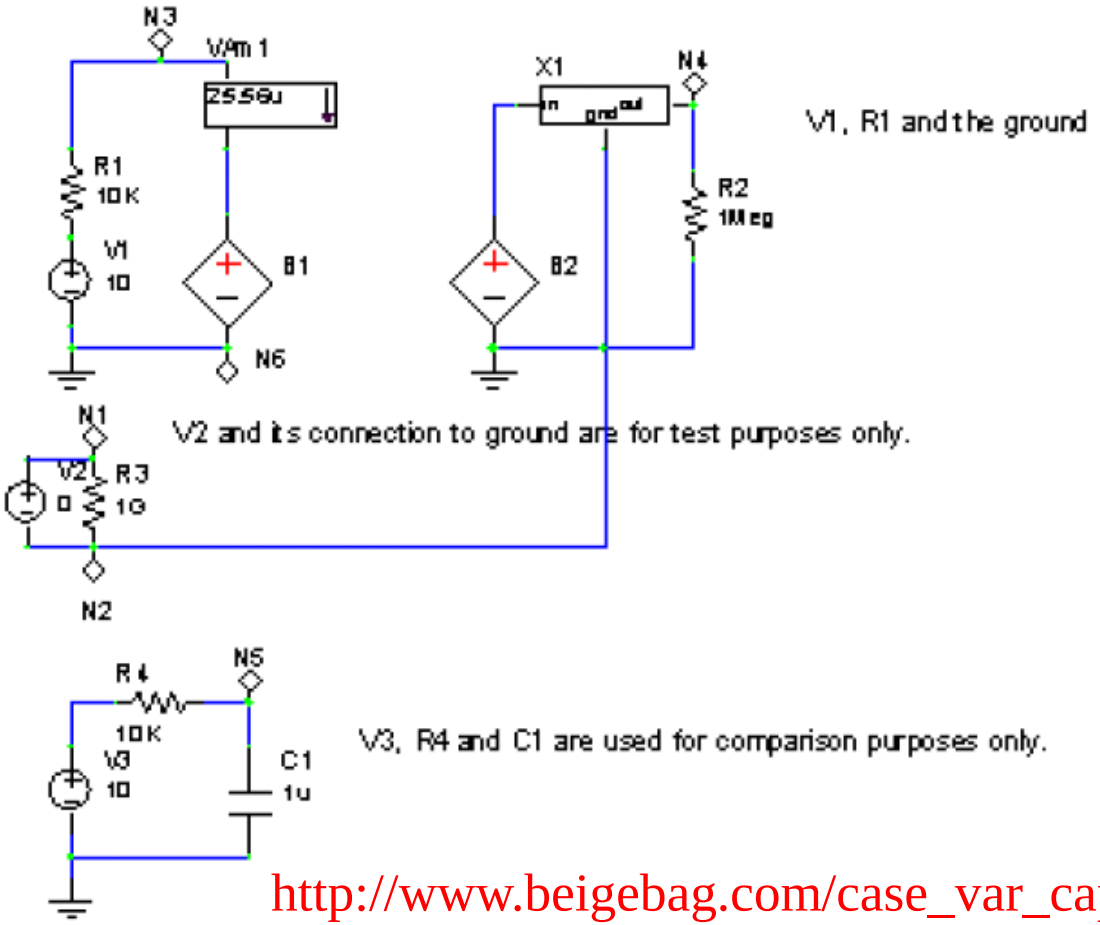
The green line is for control voltage=1.0 giving R=2Kohms, the blue is for control voltage=1.5 giving R=3Kohms.

Imax=2Volts/2Kohms= 1.0mA
Or
Imax=2Volts/3Kohms= 0.66mA



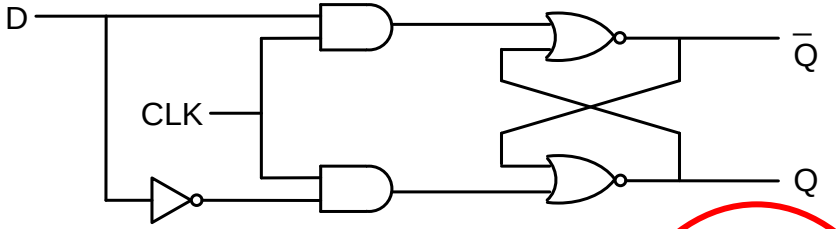
# VOLTAGE VARIABLE CAPACITOR

A model embedded in a test circuit is shown in Figure 1 following:

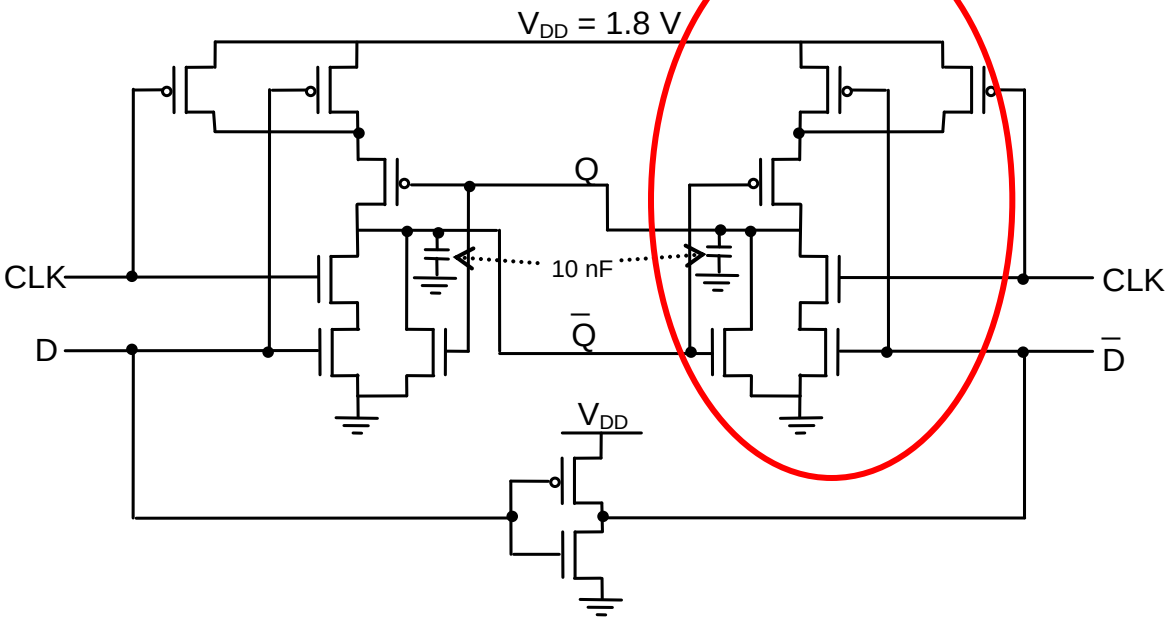



http://www.beigebag.com/case_var_cap.htm

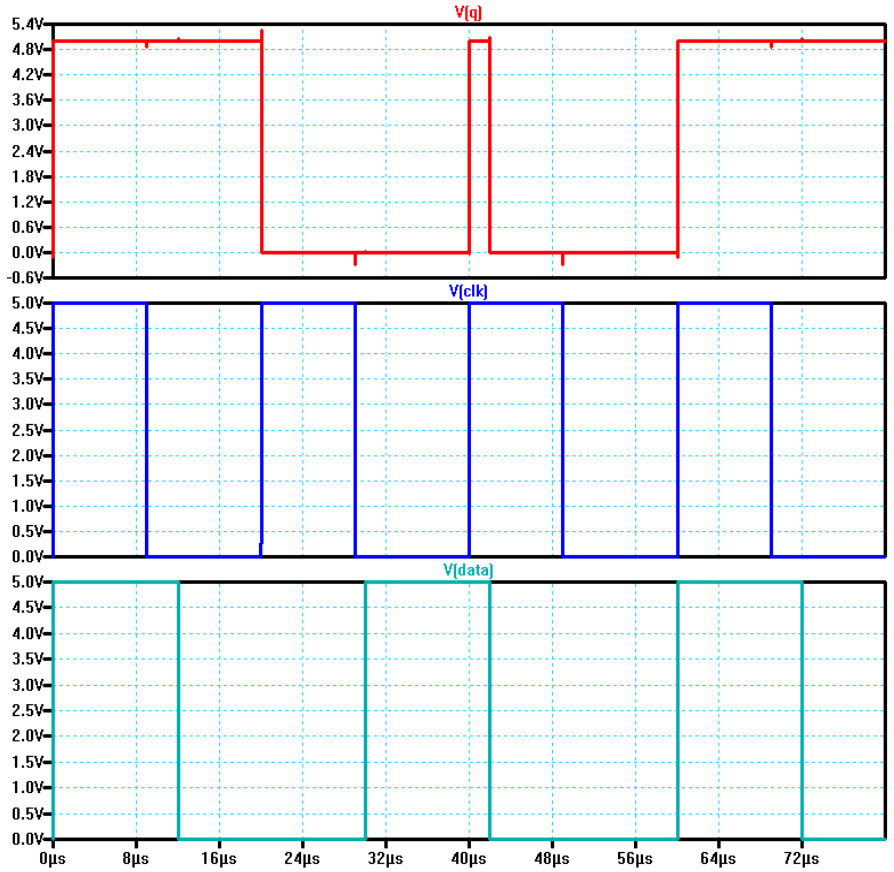
# CLOCKED DATA LATCH WITH AND-OR-INVERT GATE

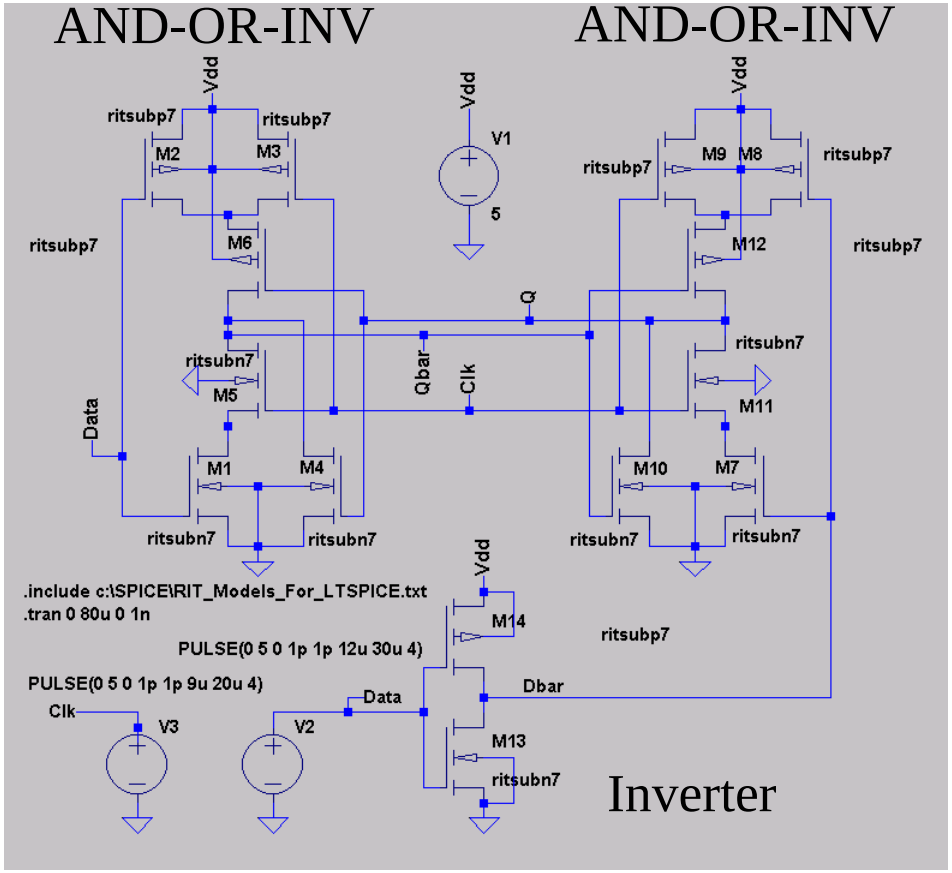



CMOS And Or Invert Gate



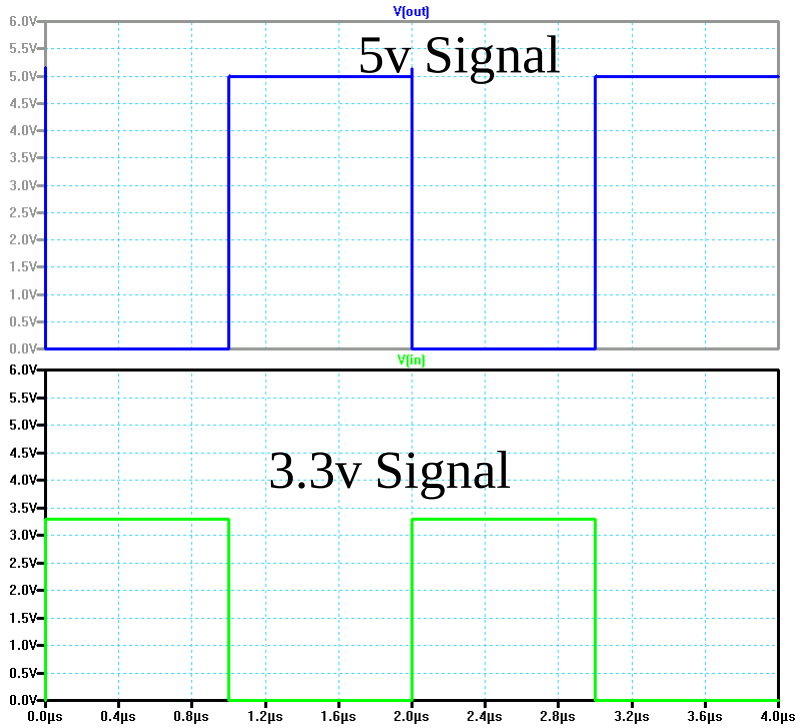
# CLOCKED DATA LATCH WITH AND-OR-INVERT GATE

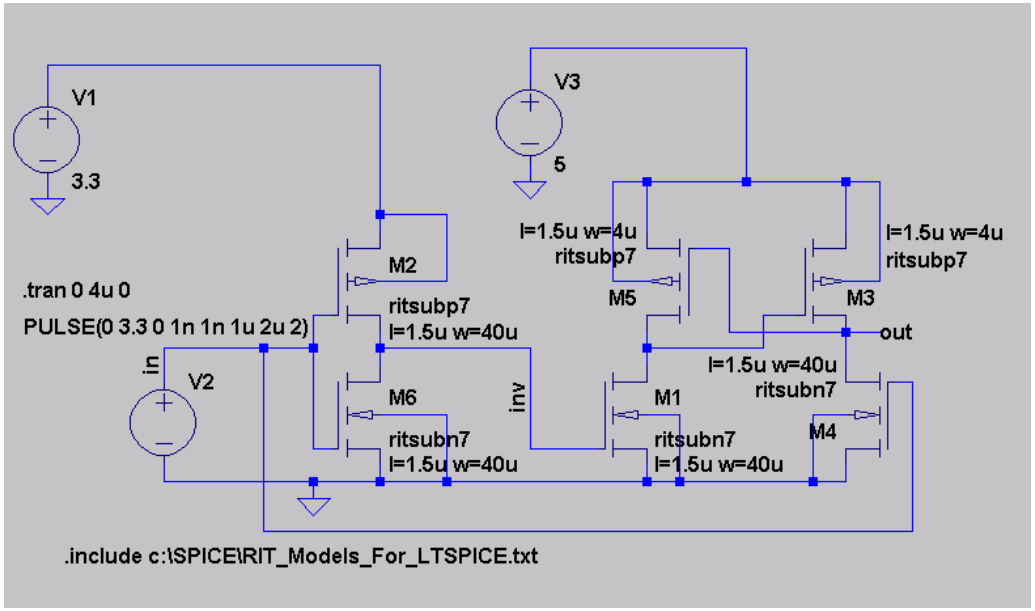



CMOS Clocked Data Latch using AND-OR-INV Gates

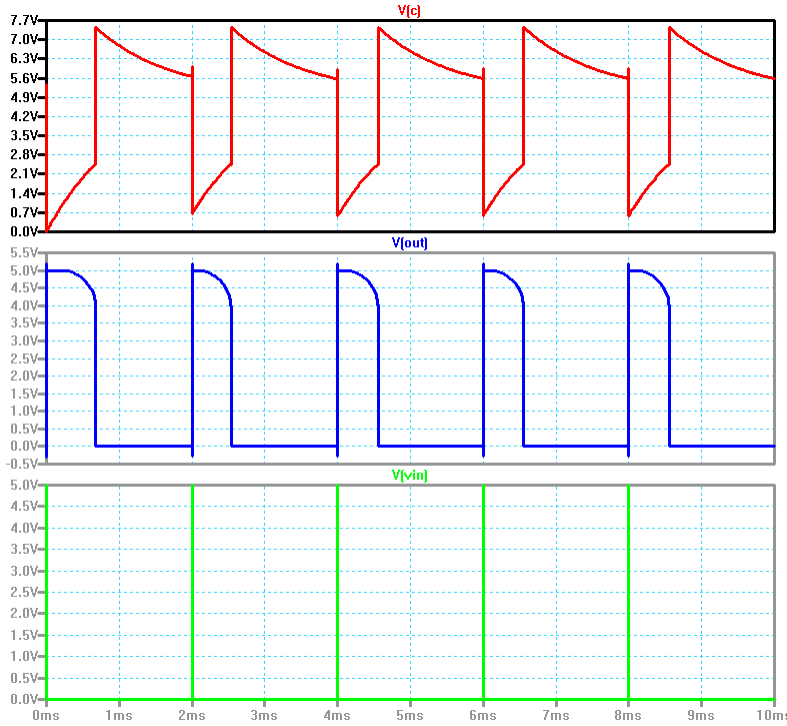
# 3.3V to 5.0 V DIGITAL LEVEL SHIFTER

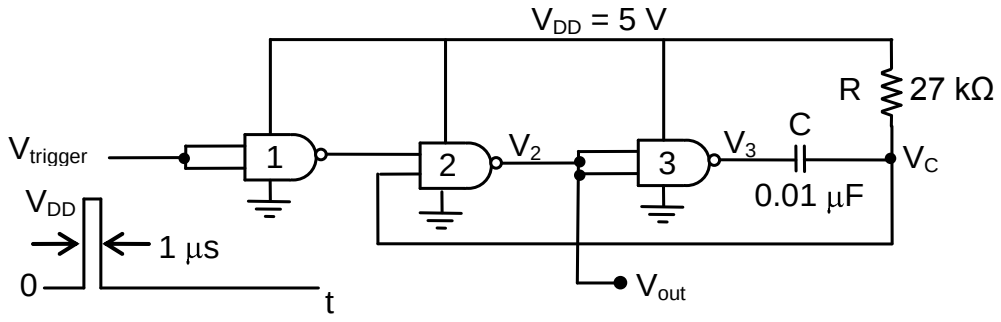


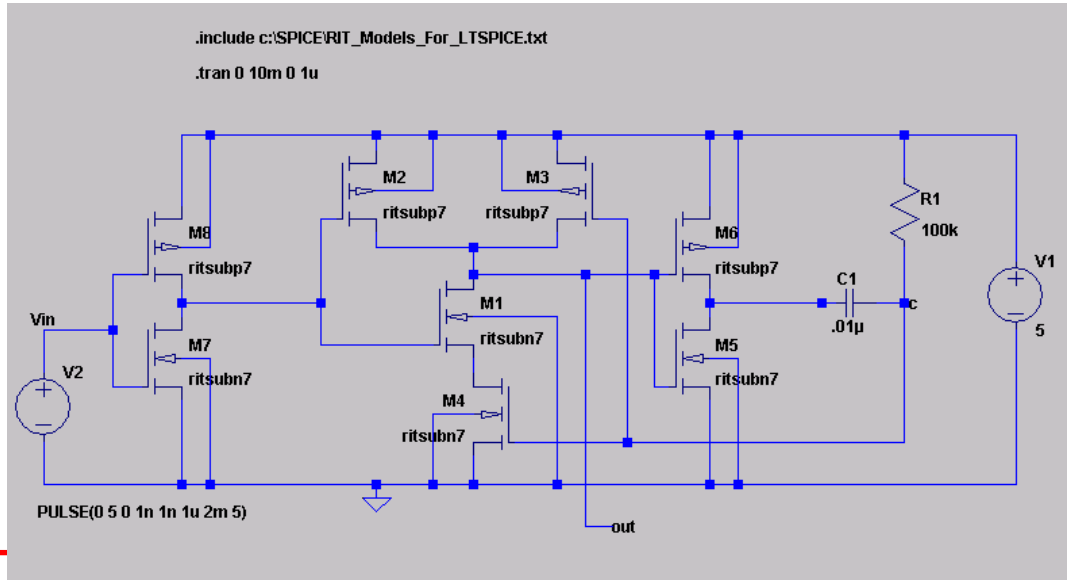

Converts 0-3.3 V digital signals to 0-5.0 volt signals
(An inverter following the output may be used)

# MONOSTABLE MULTIVIBRATOR

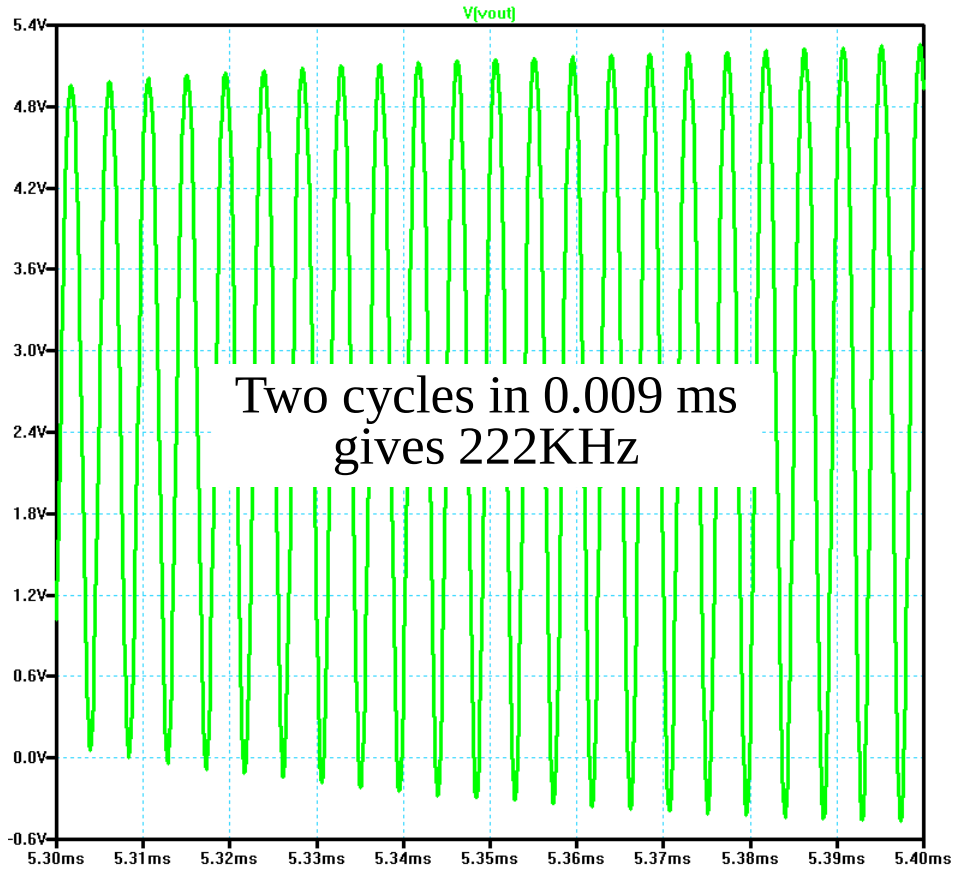


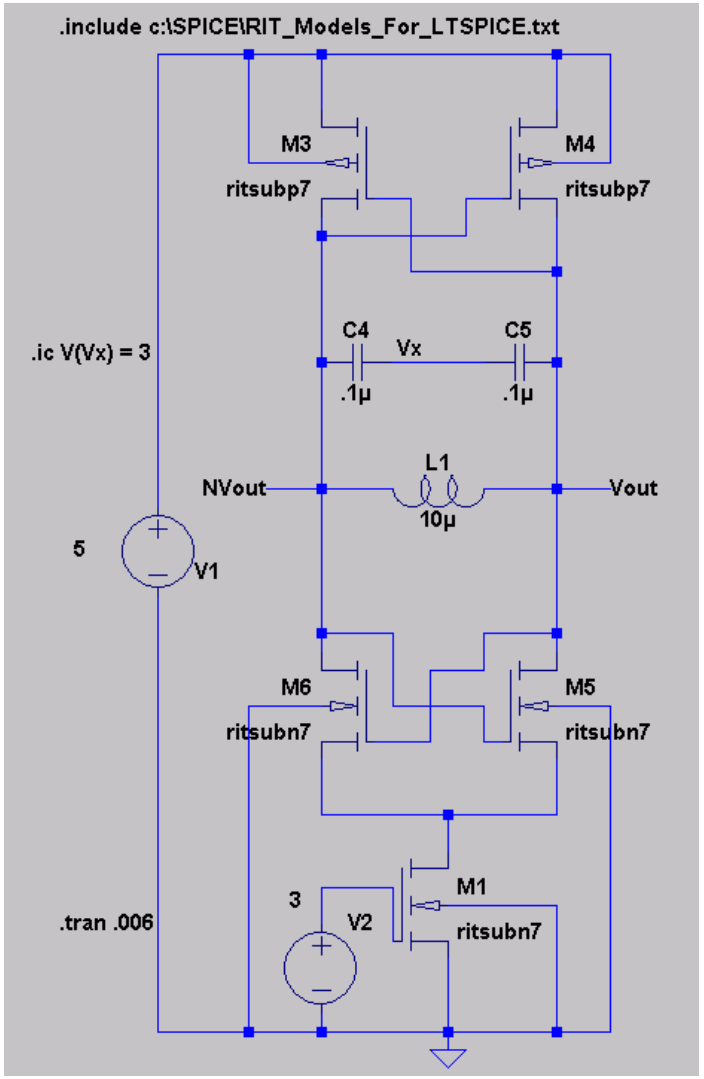




A short pulse will cause Vout to go high and stay high for a time determined by R and C



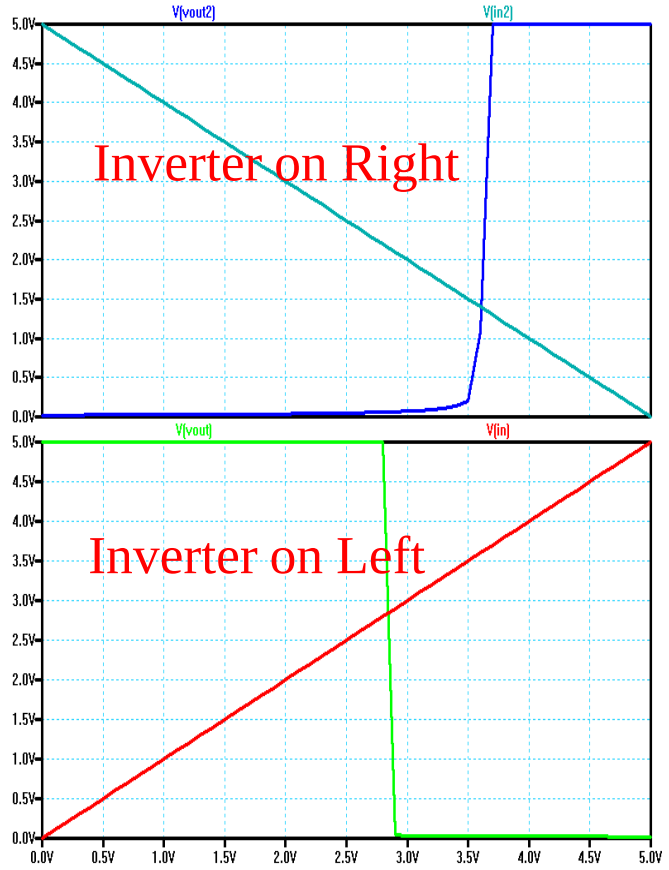
# *LC OSCILLATOR*



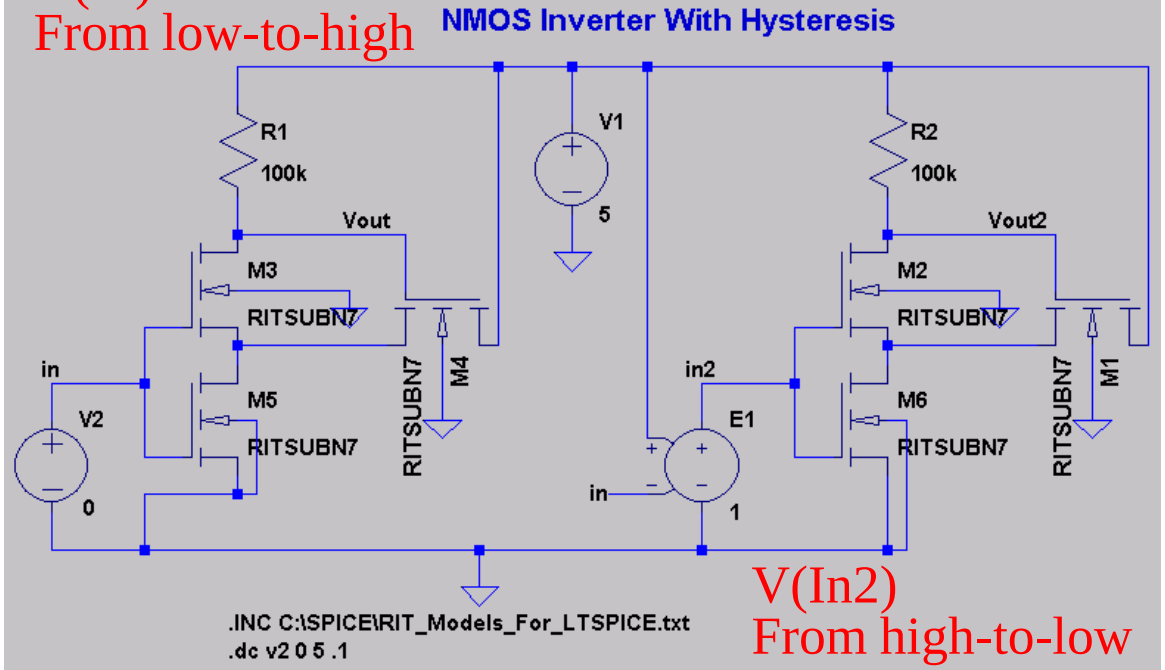




f = 1/(2 pi (sq root LC)) = 225 KHz

# NMOS INVERTER WITH HYSTERESIS




V(In)
From low-to-high

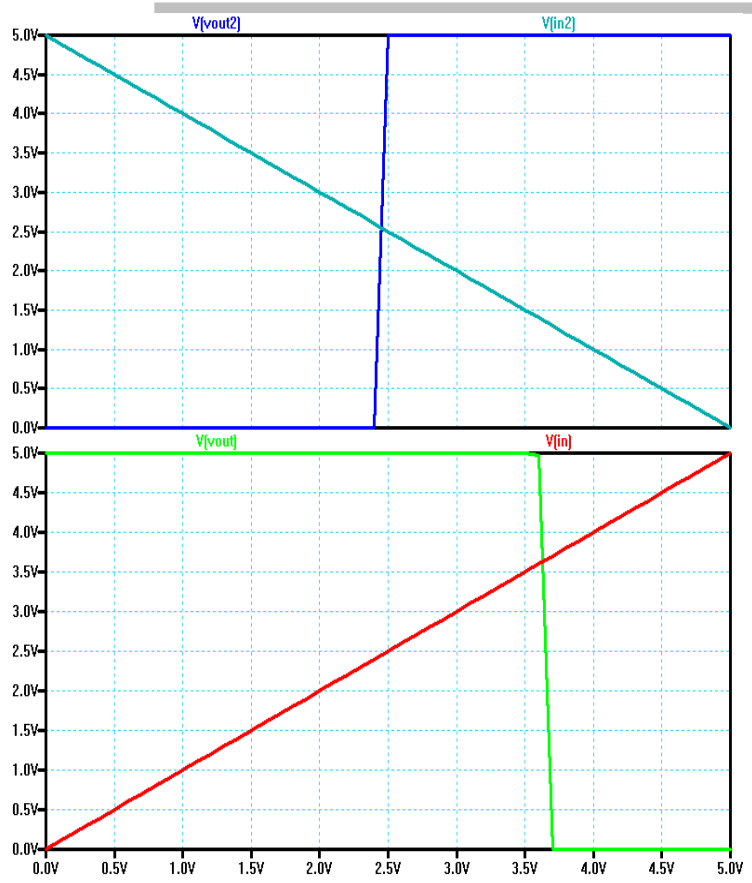


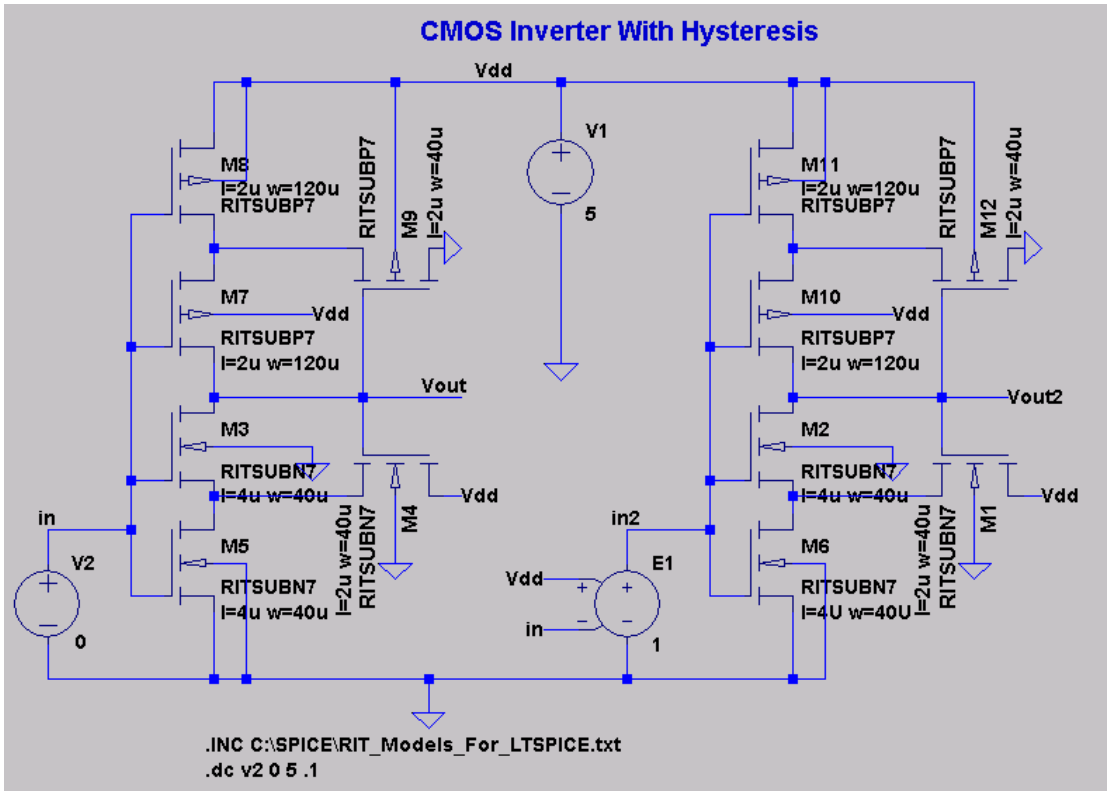

V(In2)
From high-to-low

M4 is used to change the threshold voltage of M3 by body effect through changing the voltage source-to-substrate of M3depending on if Vout is high or low.

Transition voltage depends on direction of sweep.

# CMOS INVERTER WITH HYSTERESIS



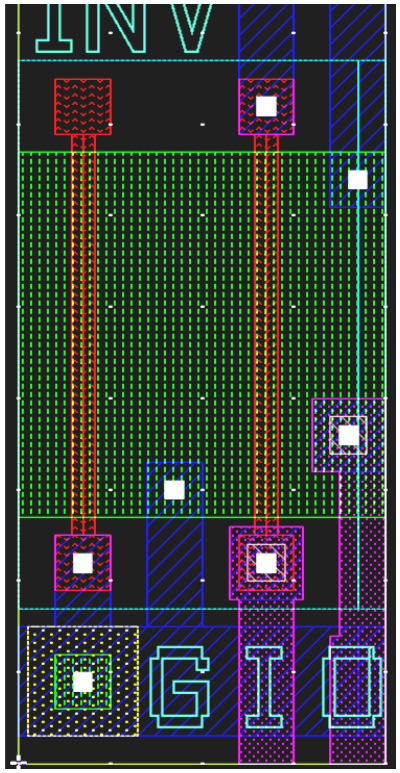




Replace the pull up resistor with PMOSFETs

# DIMENSIONS OF THE TRANSISTORS

Dimensions of transistors in Gate Array

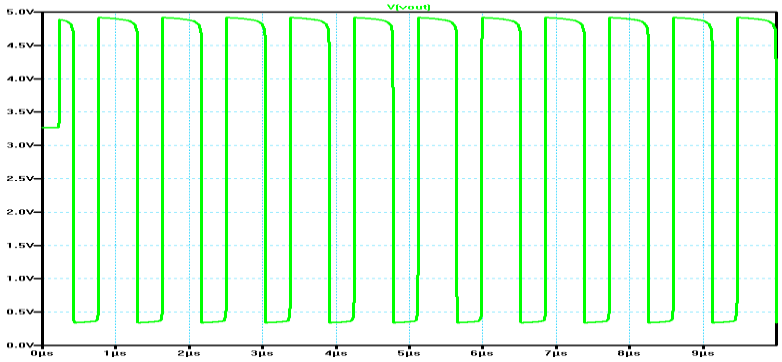
| | NMOS | PMOS |
|---|---|---|
| L | 2u | 2u |
| W | 40u | 40u |
| AD | 17ux40u=680p | 17ux40u=680p |
| AS | 17ux40u=680p | 17ux40u=680p |
| PD | 2x(17u+40u)=114u | 2x(17u+40u)=114u |
| PS | 2x(17u+40u)=114u | 2x(17u+40u)=114u |
| | | |
| | | |



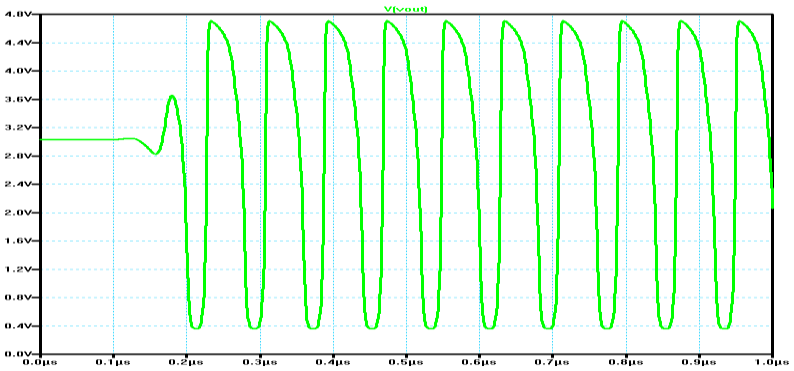

W = 40 µm
Ldrawn = 2.5µm
Lpoly = 2.0µm
Leff = 1.5 µm\
Pd=680p
Ad=114u

Right mouse click on each transistor and add these values to the properties/attributes.

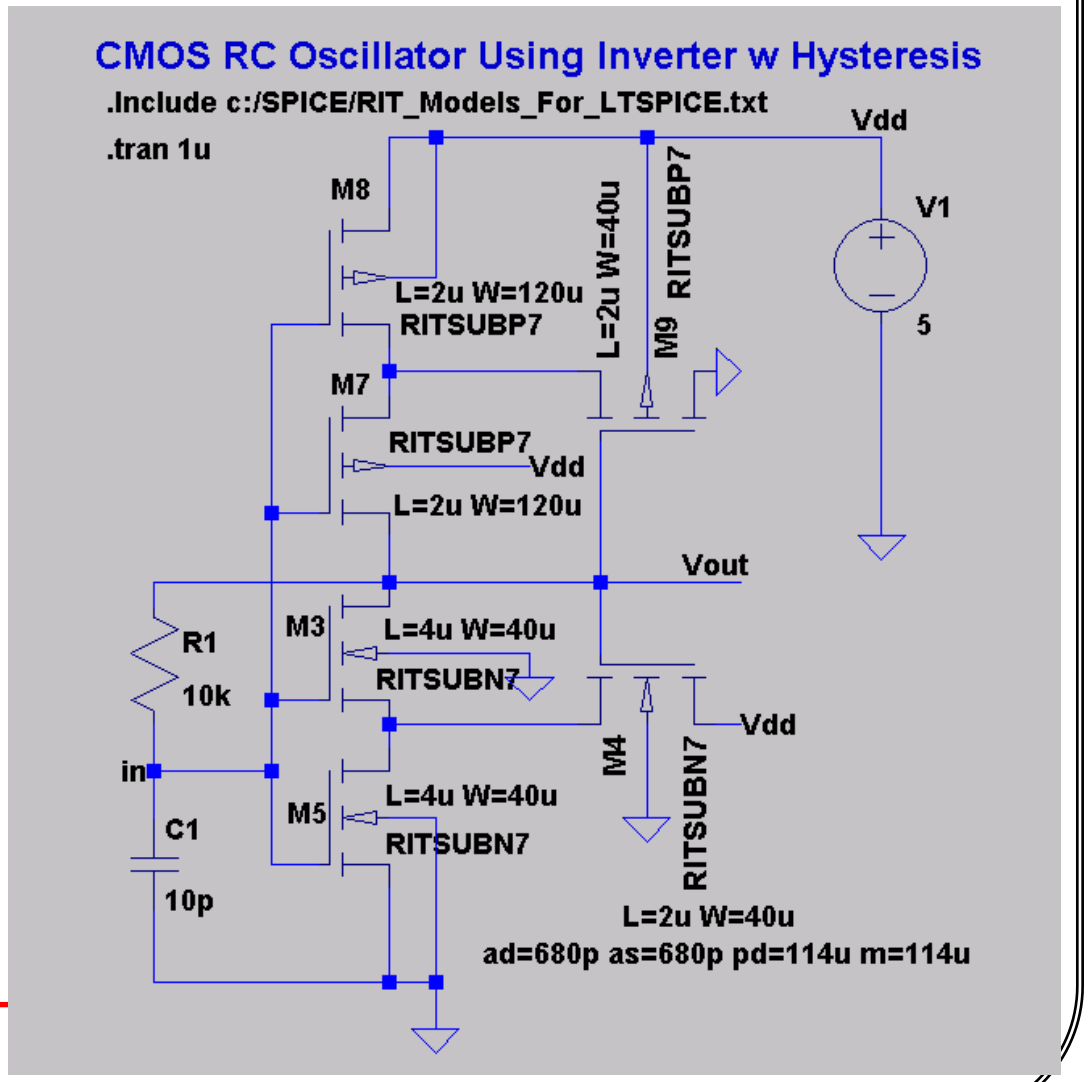
# CMOS RC OSCILLATOR USING INVERTER W HYSTERESIS



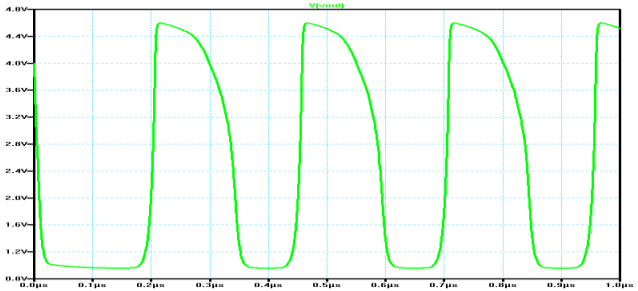
C1=100p gives f= 1 MHz



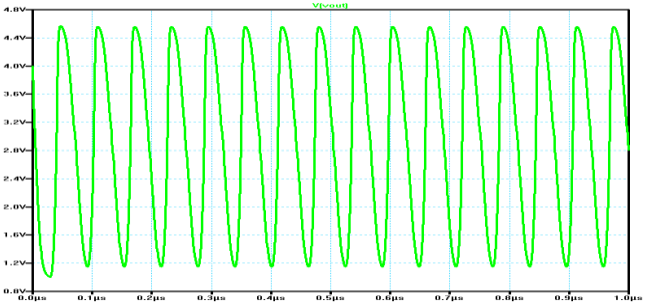
C1=10p gives f=10MHz



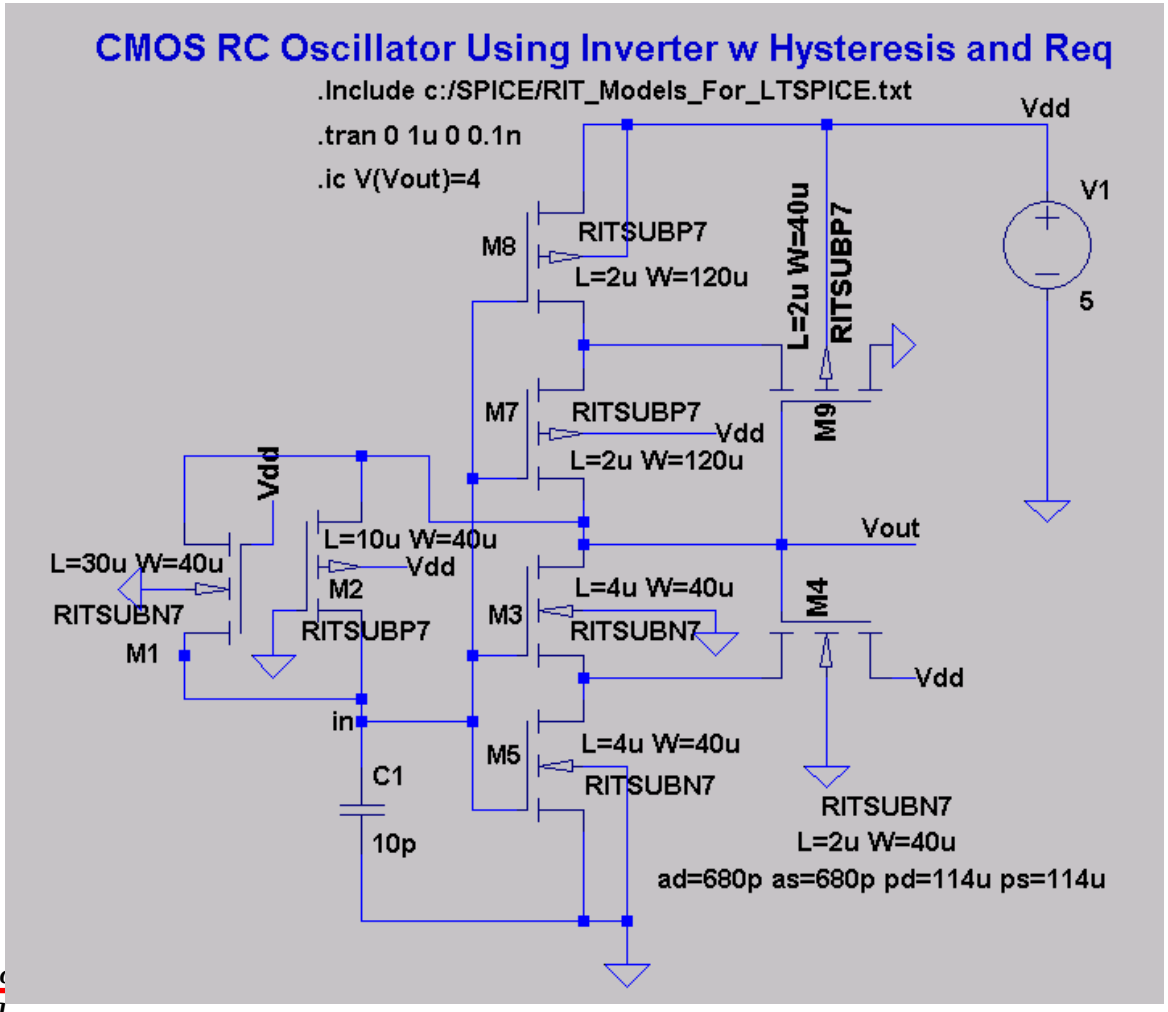
# CMOS OSCILLATOR REPLACE R WITH MOSFETS



C1 = 100pF gives f=4MHz



C1 = 10pF gives f=16MHz



# VOLTAGE CONTROLLED OSCILLATOR

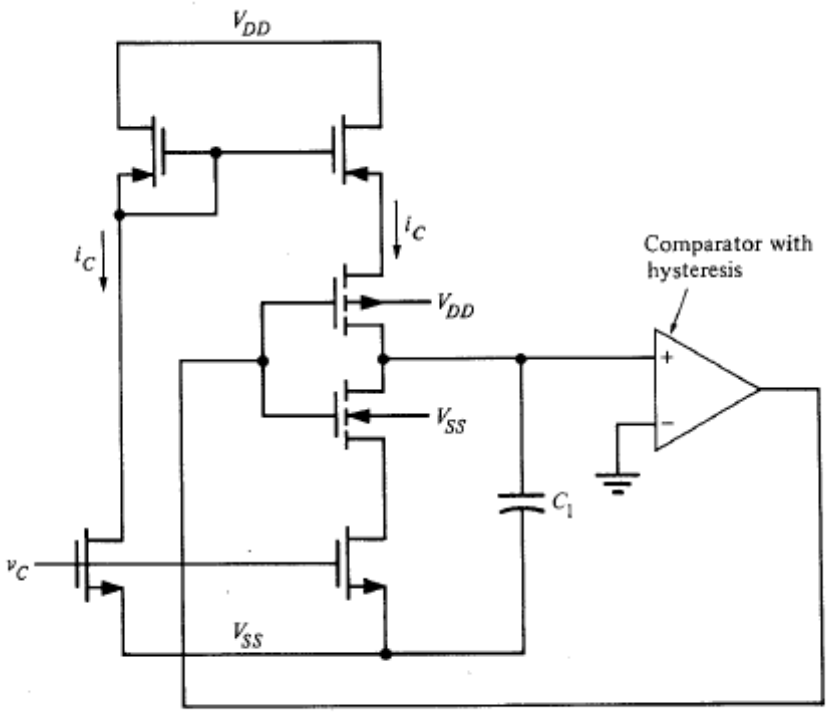
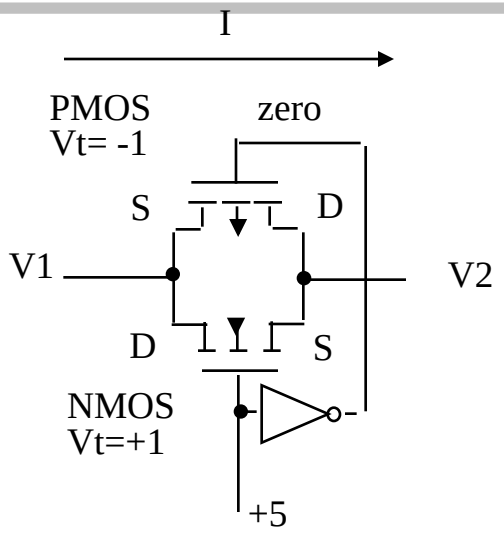


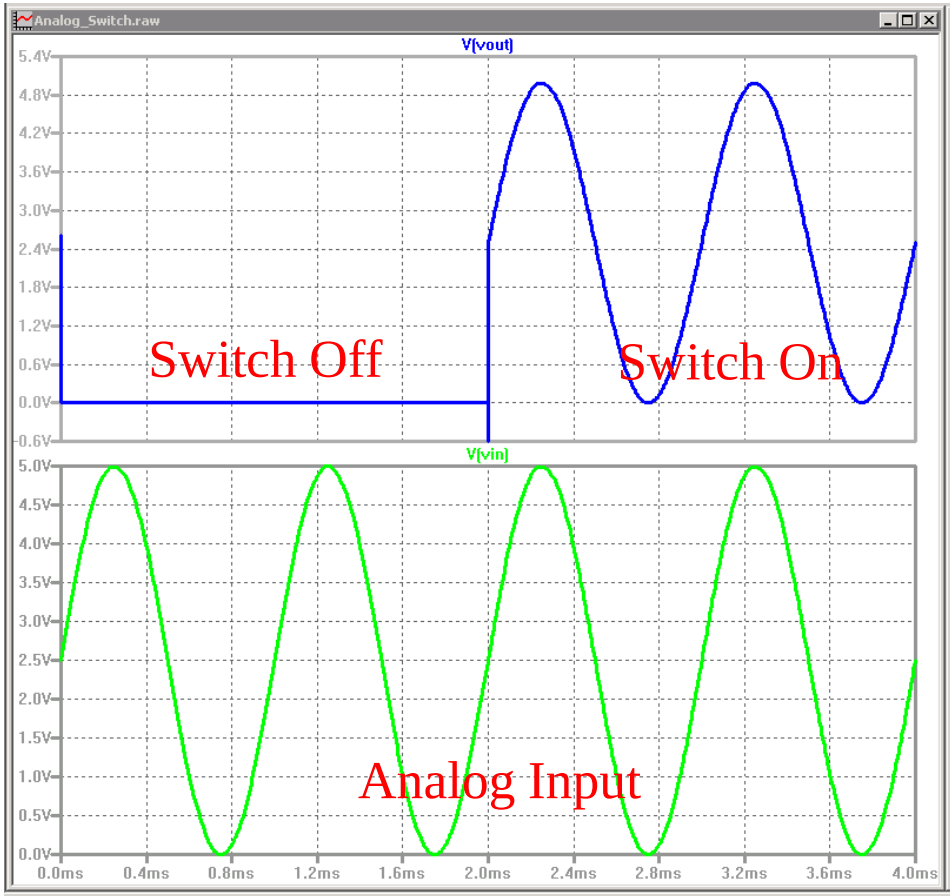

**Figure 11.4-15** A VCO compatible with CMOS technology.

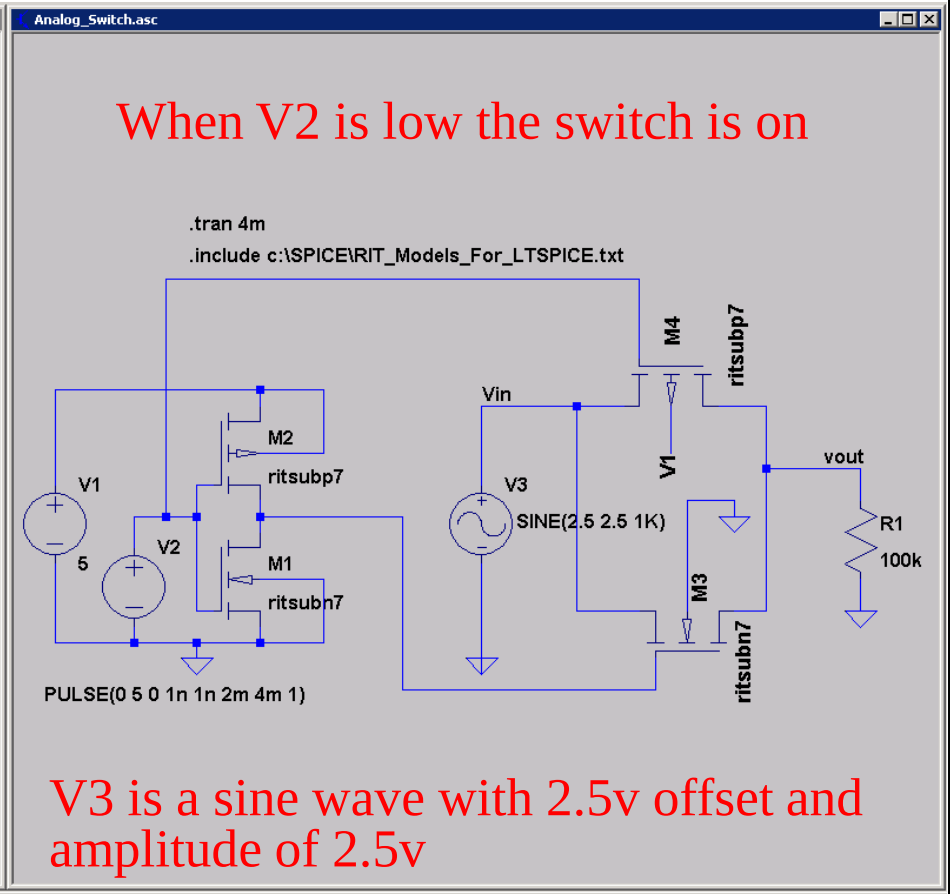
# ANALOG SWITCHES




For current flowing to the right (ie V1>V2) the PMOS transistor will be on if V1 is greater than the threshold voltage, the NMOS transistor will be on if V2 is <4 volts. If we are charging up a capacitor load at node 2 to 5 volts, initially current will flow through NMOS and PMOS but once V2 gets above 4 volts the NMOS will be off. If we are trying to charge up V2 to V1 = +1 volt the PMOS will never be on. A complementary situation occurs for current flow to the left. Single transistor switches can be used if we are sure the Vgs will be more than the threshold voltage for the specific circuit application. (or use larger voltages on the gates)

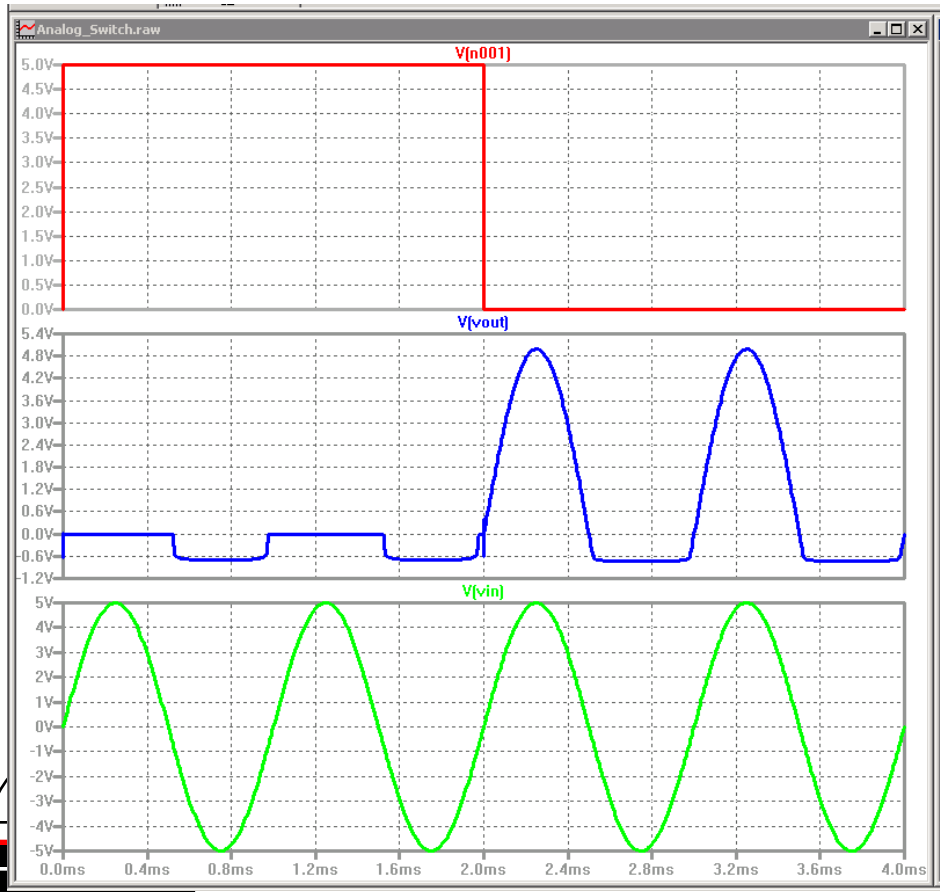
# ANALOG SWITCH

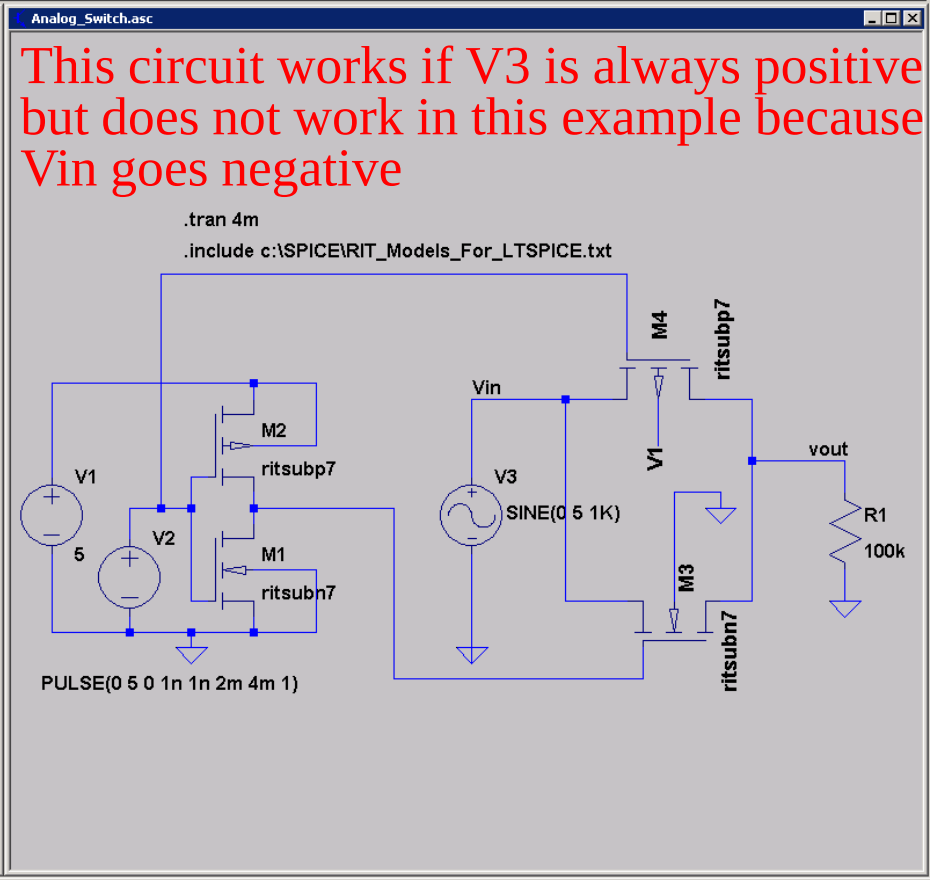


# ANALOG SWITCH FOR DUAL SUPPLY

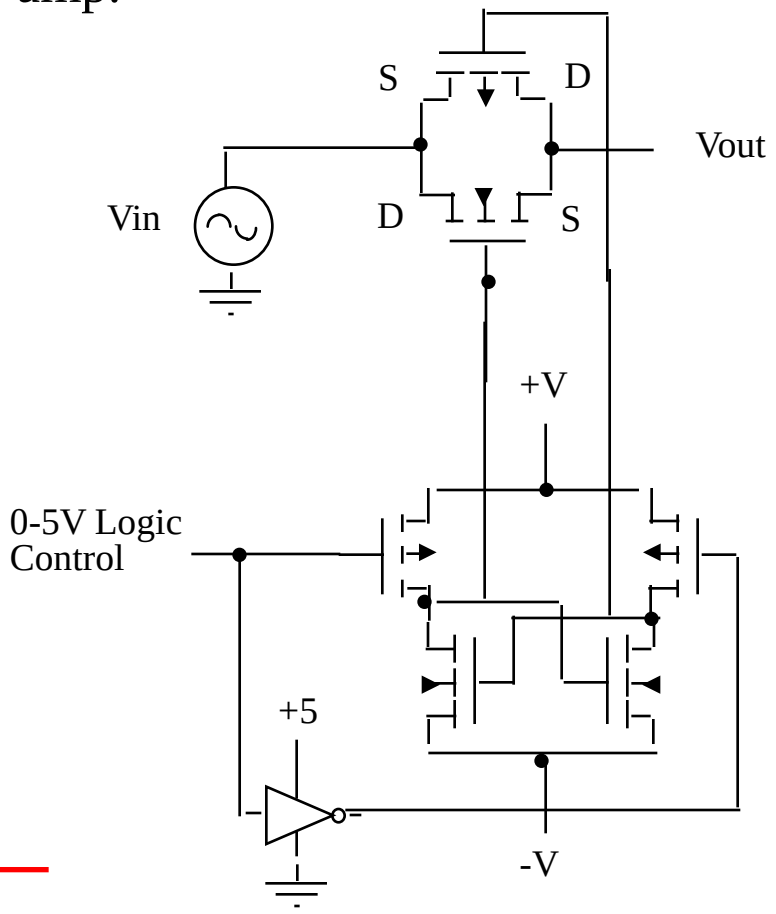
This example is for a mixed digital and analog circuit. For example a 3.3 volt digital logic and +/- 5 volt analog op amp. The signal going thru the switch is +/-5 volts.



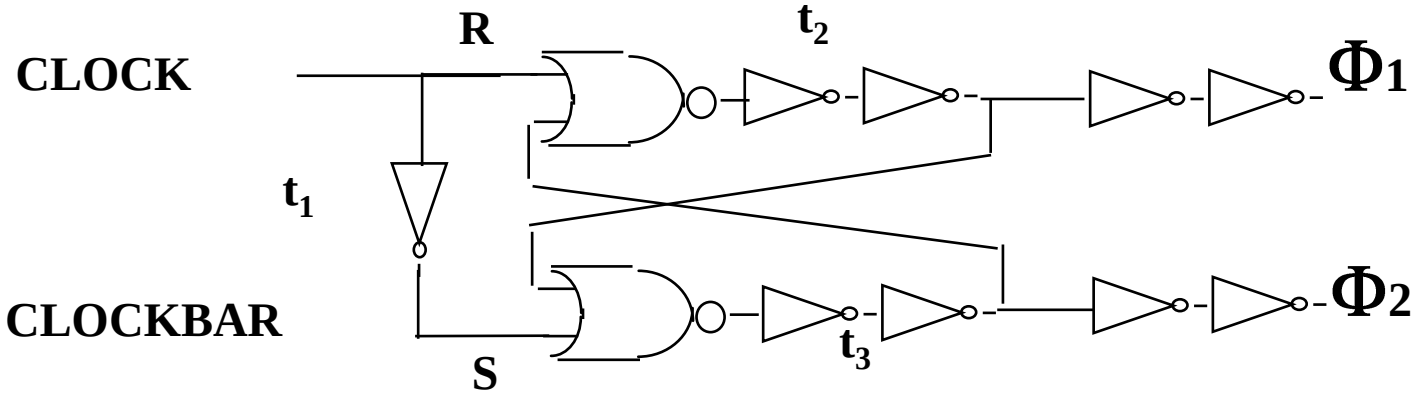



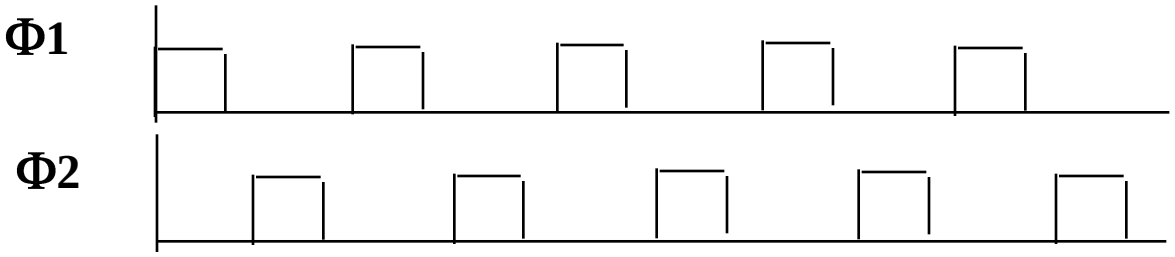
# ANALOG SWITCH FOR DUAL SUPPLY

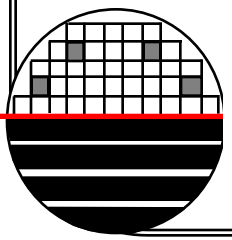
This example is for a mixed digital and analog circuit. For example a 3.3 volt digital logic and +/- 12 volt analog op amp.



# NON OVERLAPPING CLOCK PLUS BUFFERS



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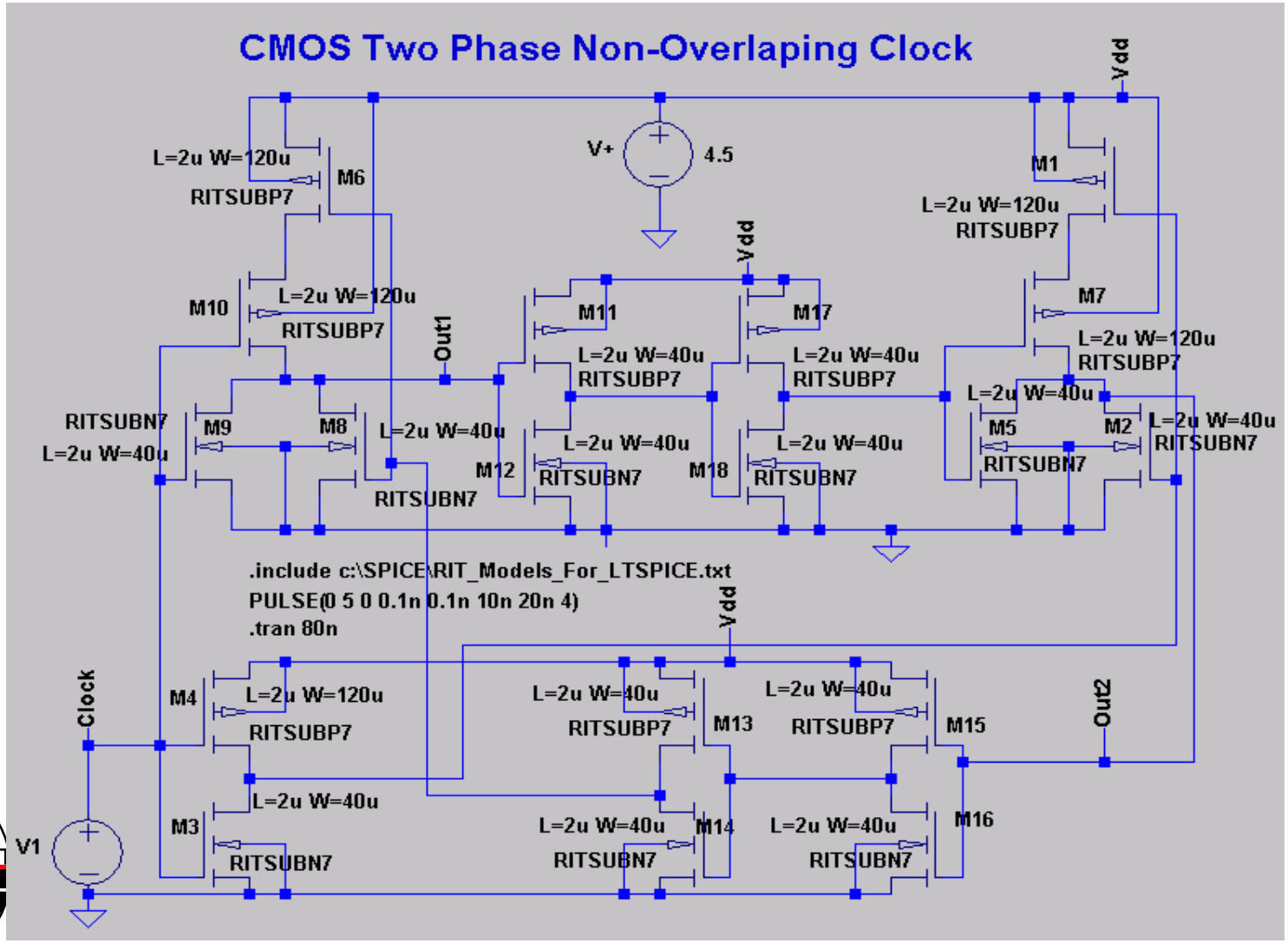
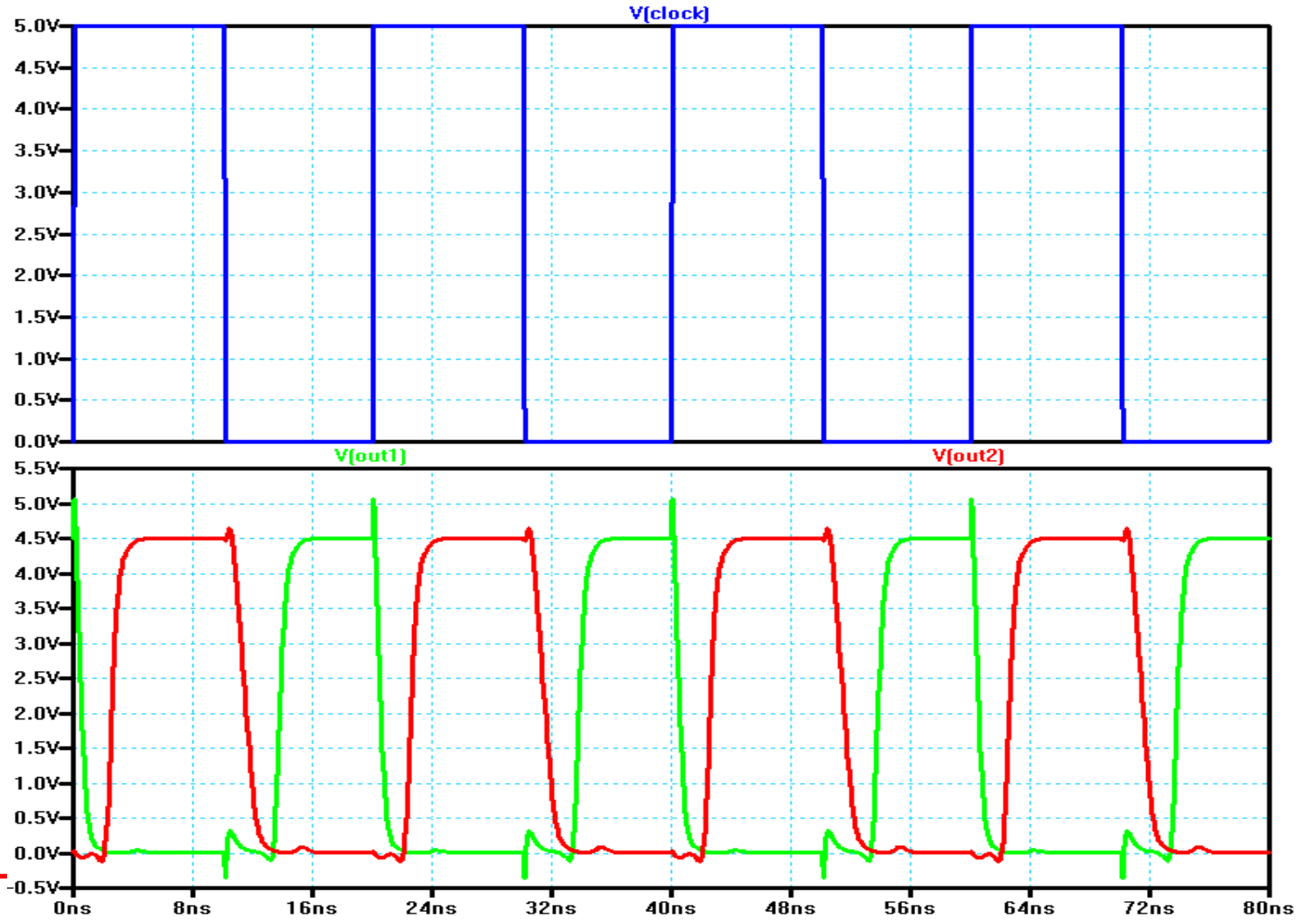
# CMOS TWO PHASE NON-OVERLAPPING CLOCK



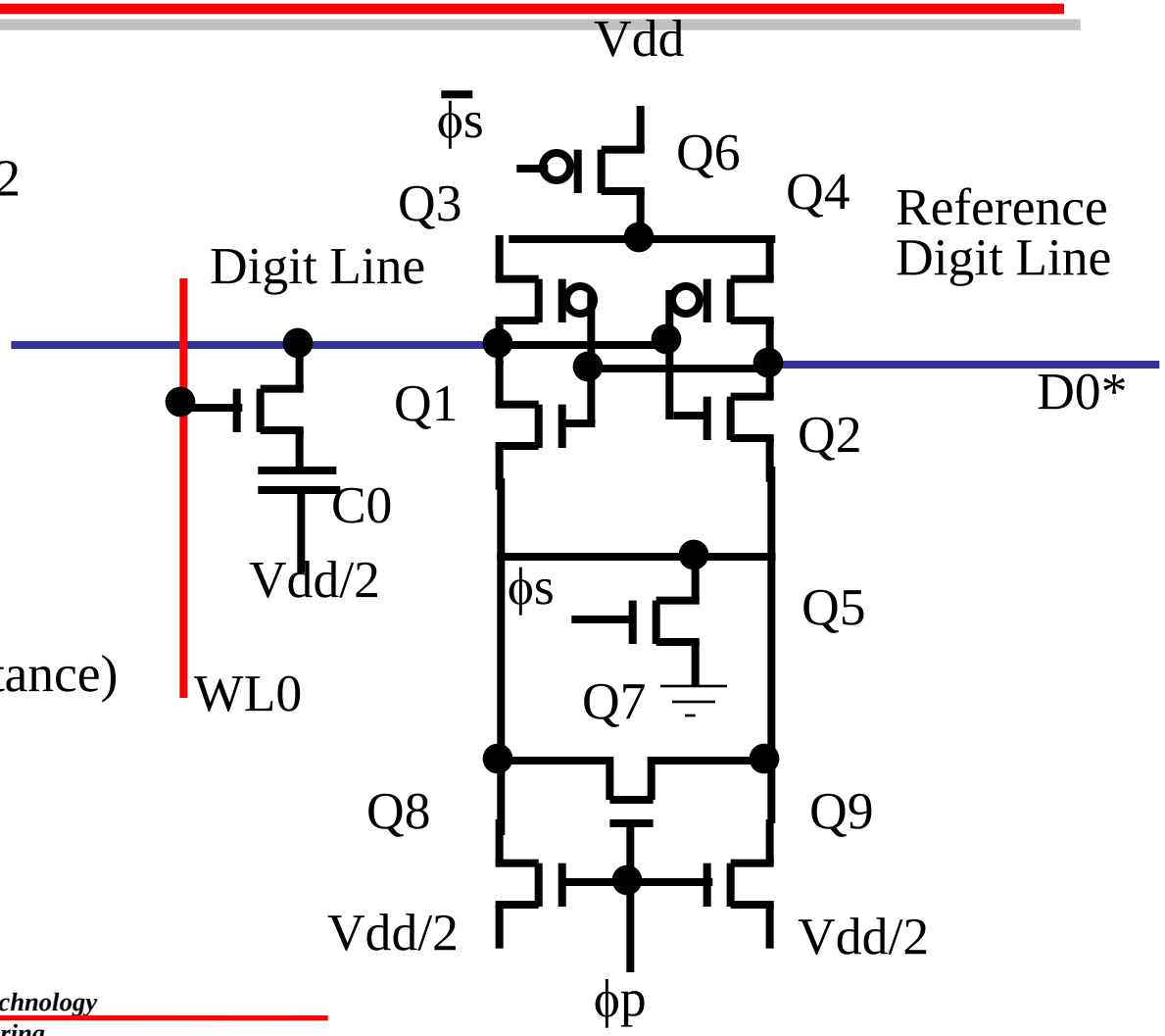
# CMOS TWO PHASE NON-OVERLAPPING CLOCK



# DRAM SENSE AMPLIFER DETAILS

Q7 is turned on with signal ϕp precharging the two digit lines to Vdd/2

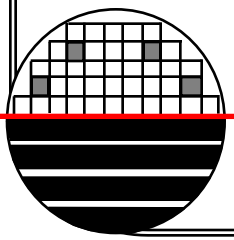
Note: the memory is organized into two arrays so that one can be used as the reference for the other. (with basically identical digit line capacitance)



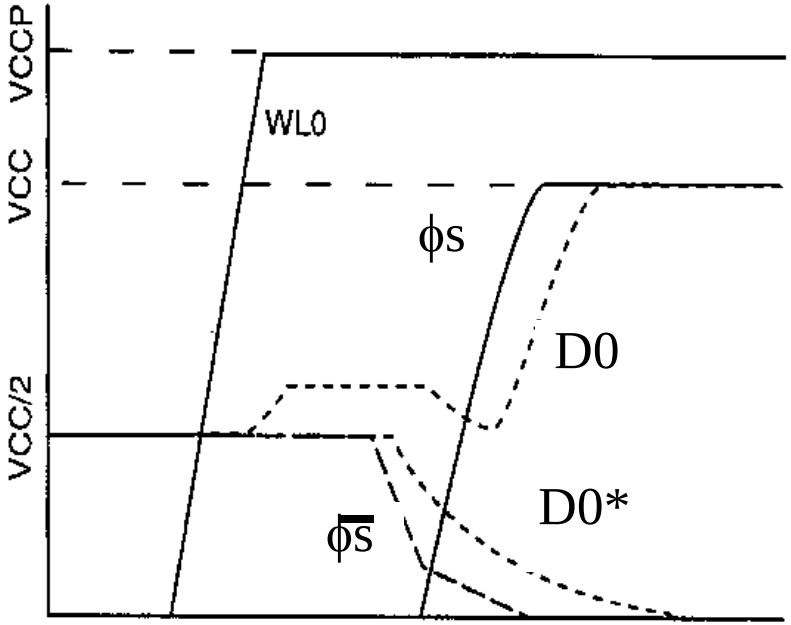
# SENSE AMPLIFIER DETAILS

Φs goes high and the data in the selected memory cell is sensed. The word line WL0 goes high and the charge on selected capacitor C0 is shared with the capacitance of the digit line D0. If a "1" was stored in C0 the voltage on D0 will initially be a little higher than Vdd/2. The voltage on the reference digit line will initially be Vdd/2. The crosscoupled inverters amplify these starting voltage and bring the digit line D0 to Vdd and D0* to zero volts. The capacitor C0 is recharged (refreshed) at the same time it is read.

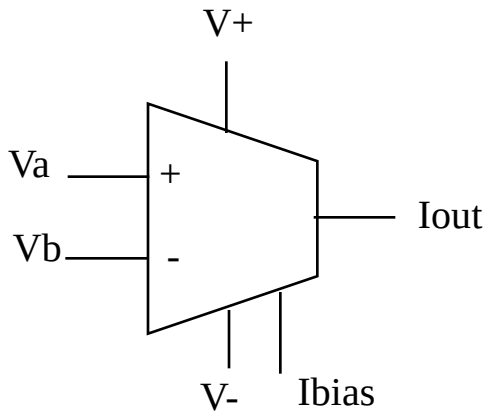
If a "0" was stored in C0 the voltage on D0 will initially be a little lower than Vdd/2. The crosscoupled inverters bring D0 to zero volts, refreshing C0 and providing a one for an output on D0*.

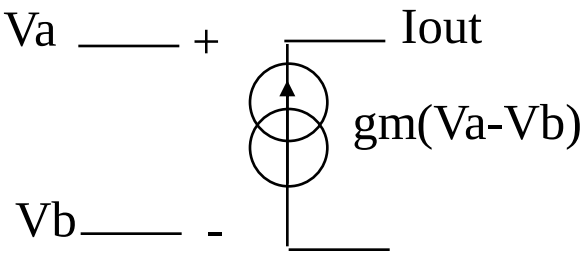


# SENSE AMPLIFER WAVEFORMS

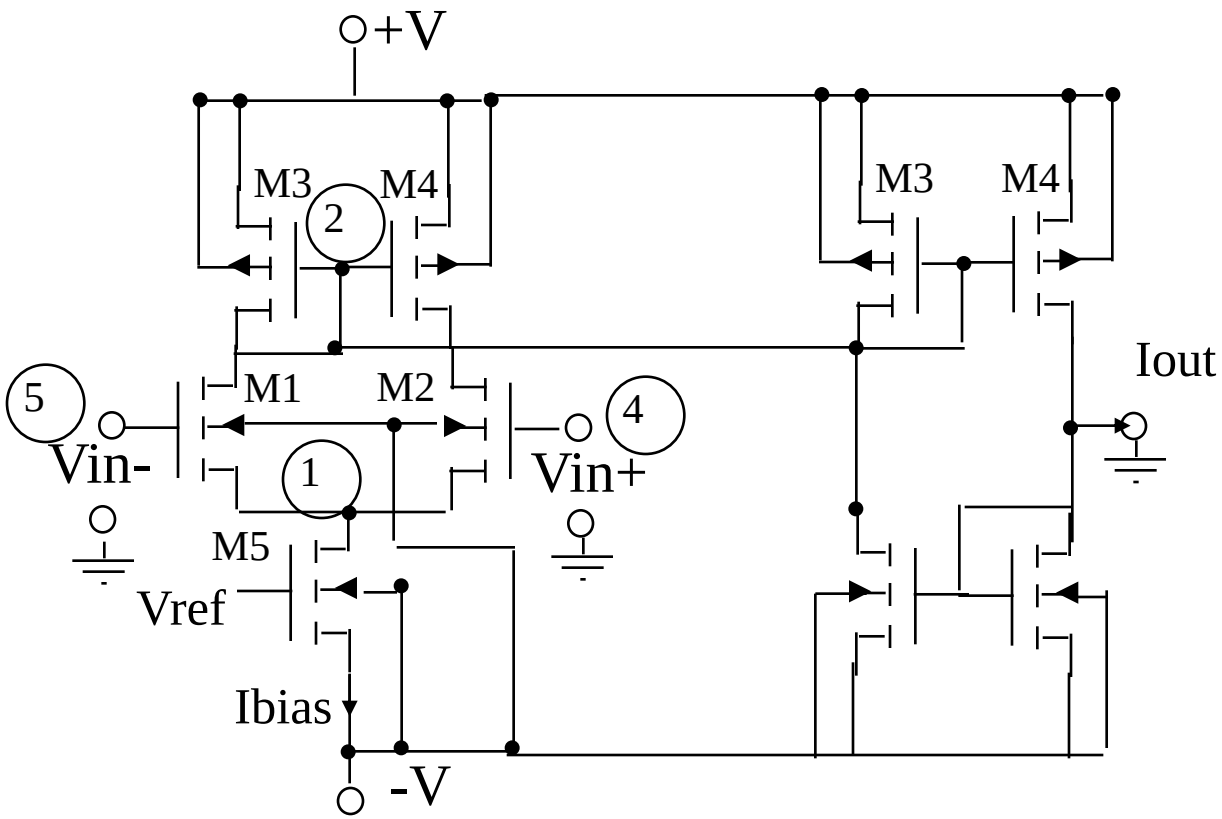


# OPERATIONAL TRANSCONDUCTANCE AMPLIFIER



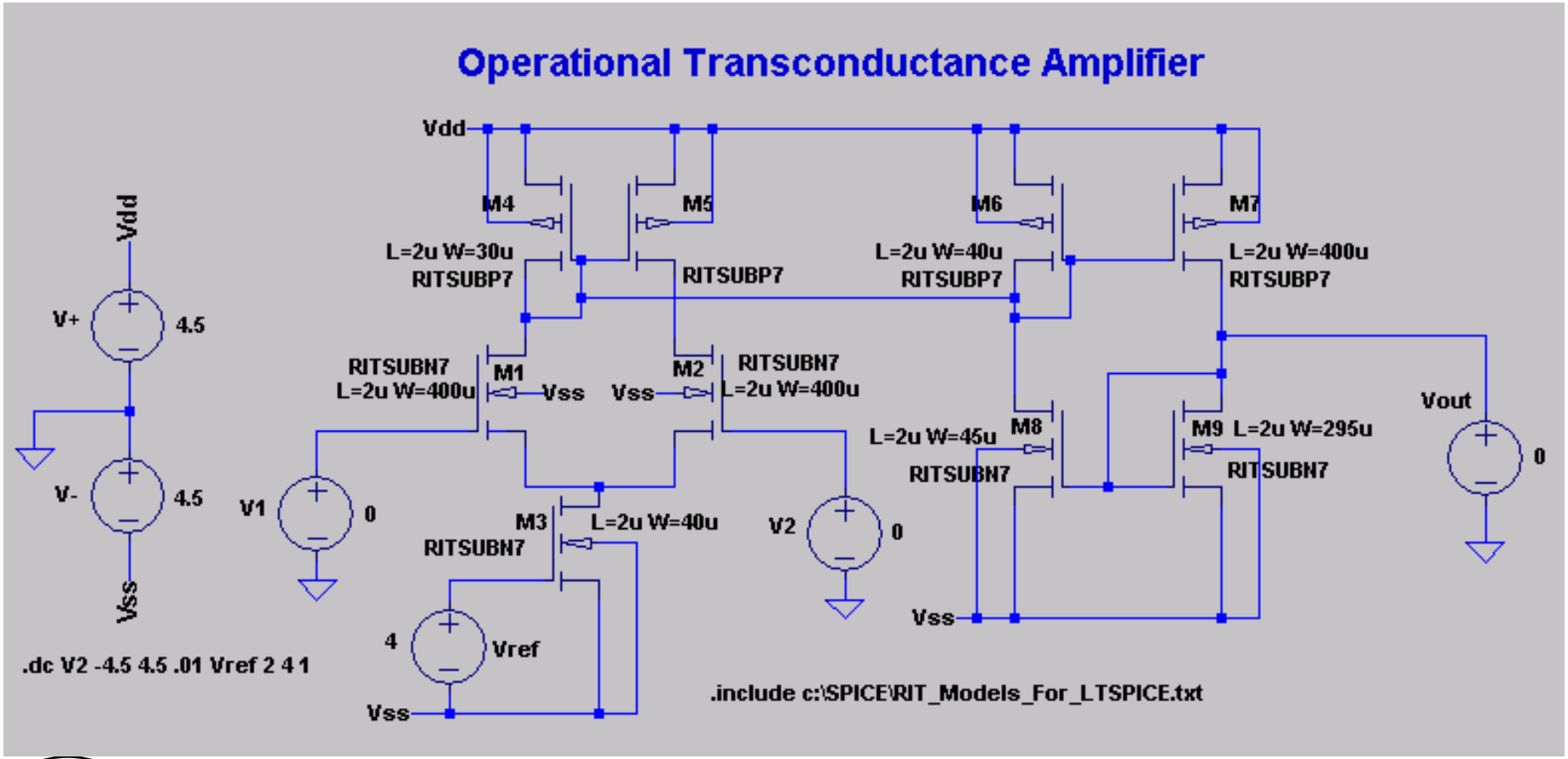




CMOS Realization

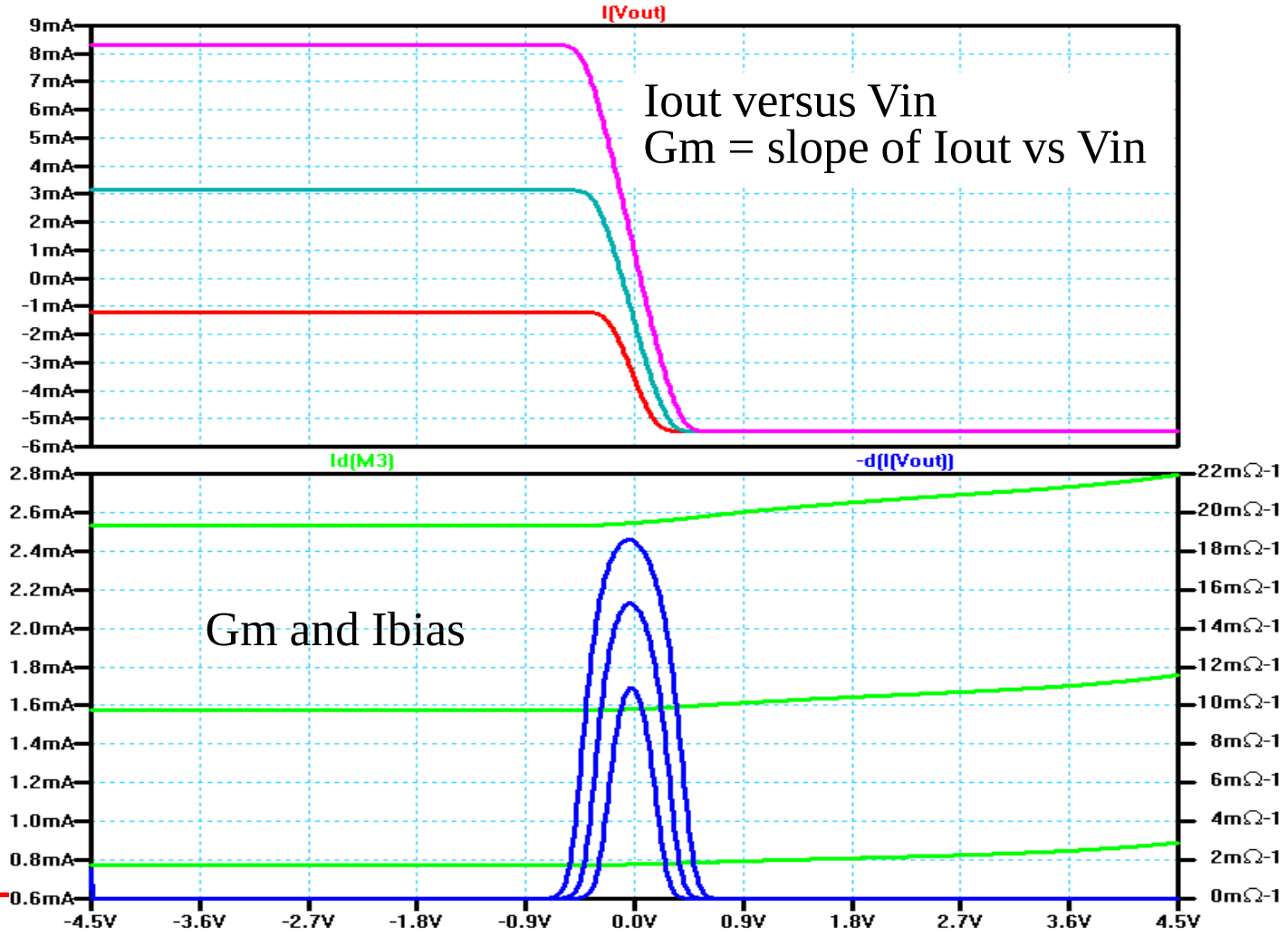



Note: gm is set by Ibias

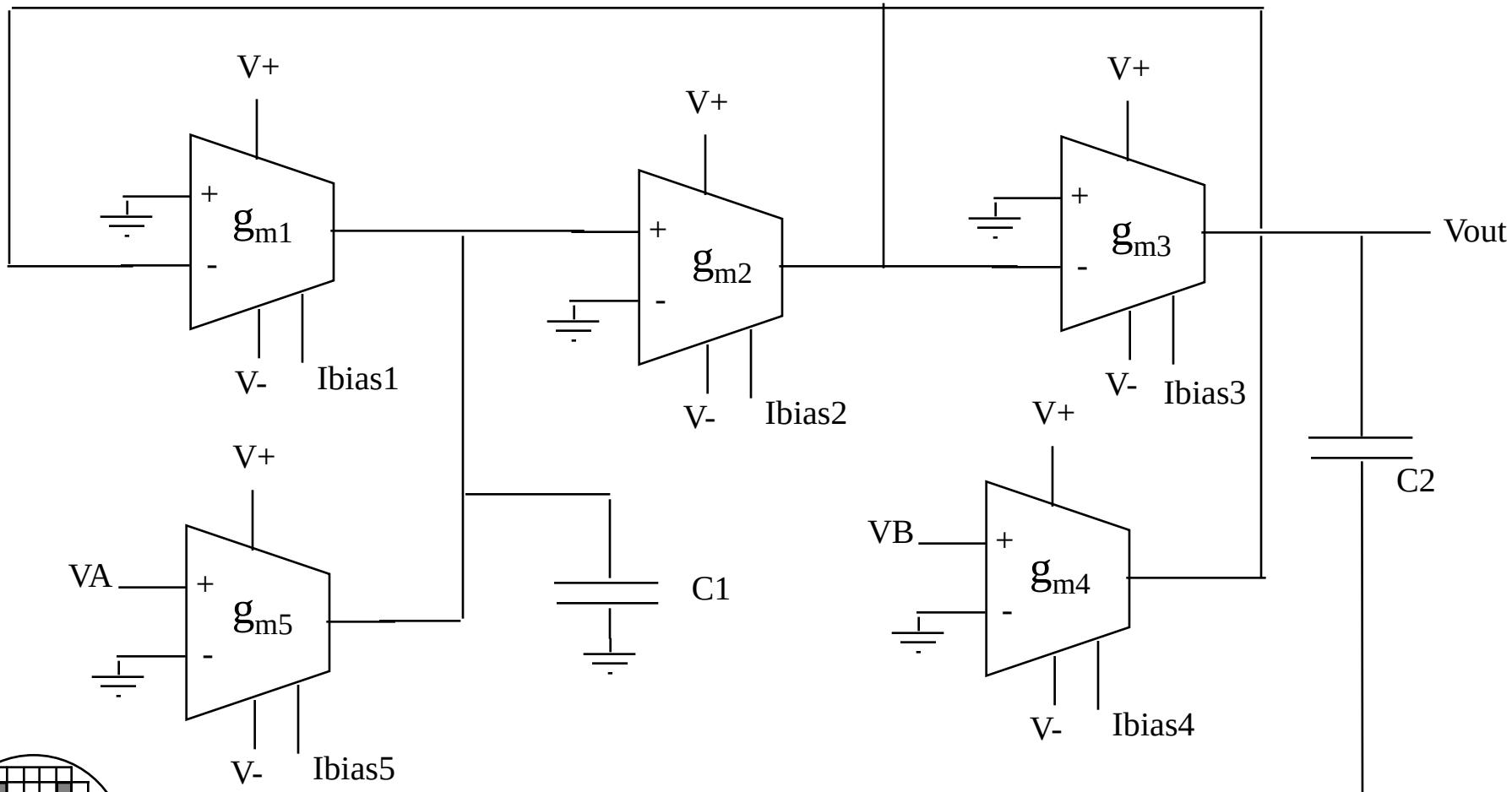
# SPICE OF OPERATIONAL TRANSCONDUCTANCE AMP



# TRANSCONDUCTANCE FOR Vref=2,3,4 volts



# BIQUAD FILTER



# BIQUAD FILTER

$$V_{out} = (s^2C_1C_2V_c + s\,C_1\,g_{m4}\,V_b + g_{m2}\,g_{m5}\,V_a)/(s^2C_1C_2 + sC_1g_{m3} + g_{m2}g_{m1})$$

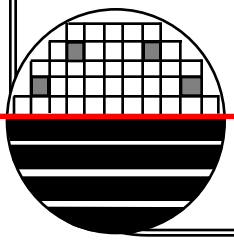
This filter can be used as a low-pass, high-pass, bandpass, bandrejection and all pass filter. Depending on the C and gm values a Butterworth, Chebyshev, Elliptic or any other configuration can be achieved

For example: let Vc=Vb=0 and Va=Vin, also let all $g_m$ be equal, then

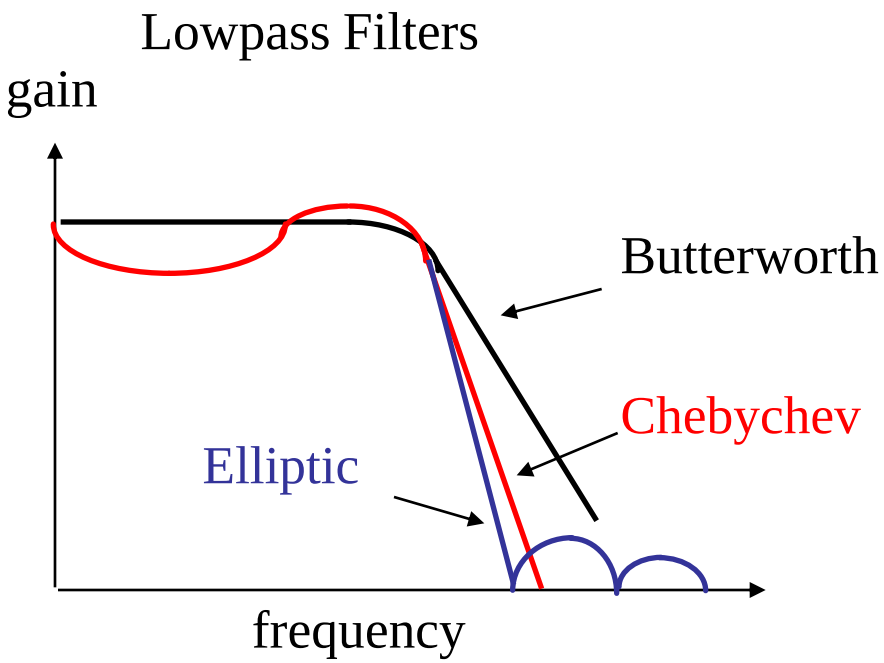
$$Vout = Vin / (s^2C_1C_2/ g_mg_m + sC_1/g_m + 1)$$

which is a second order low pass filter with corner frequency at

$$\omega_c = g_m / \sqrt{C_1C_2} \quad \text{and } Q = \sqrt{C_2/C_1}$$



# COMPARISON OF DIFFERENT FILTER DESIGNS

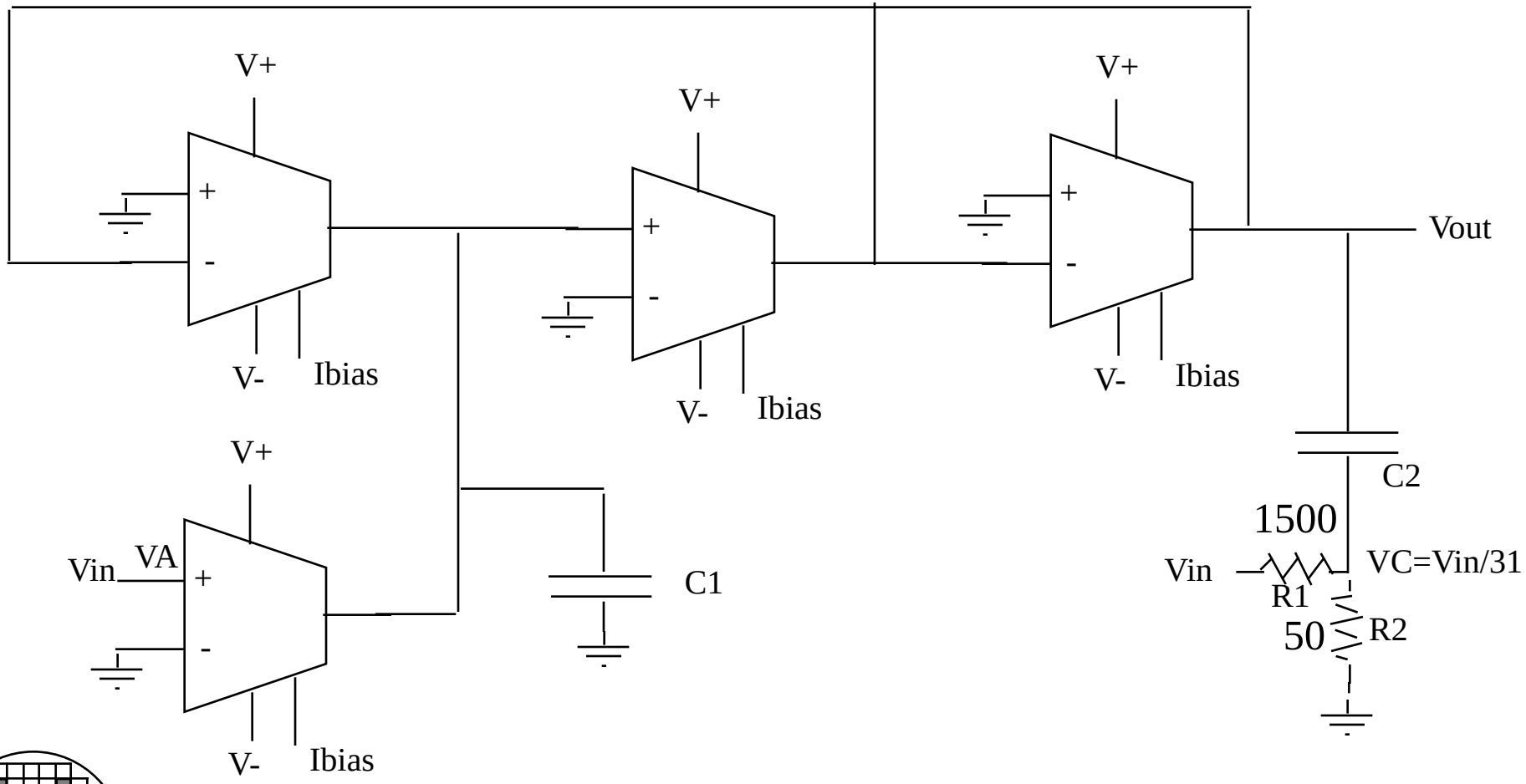



Butterworth is flat in the band pass region, has the least steep transition to band stop region

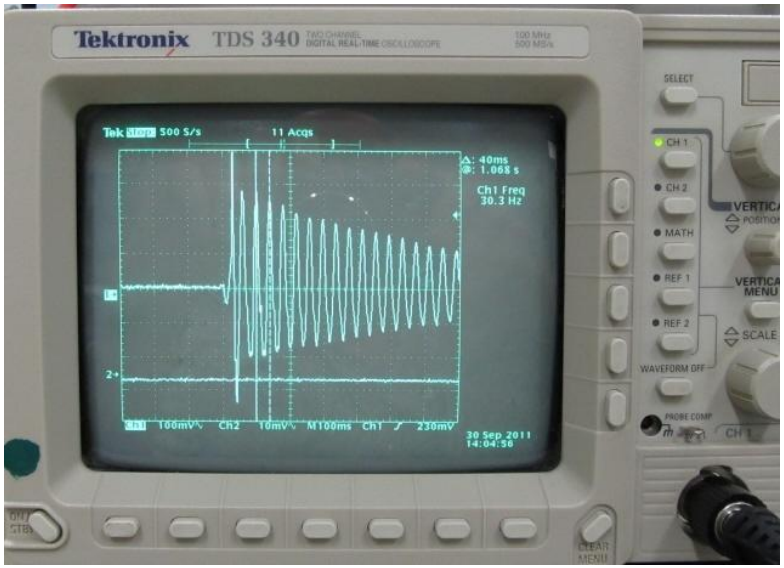
Chebychev is not flat in the band pass region, has a steeper transition to band stop region than Butterworth

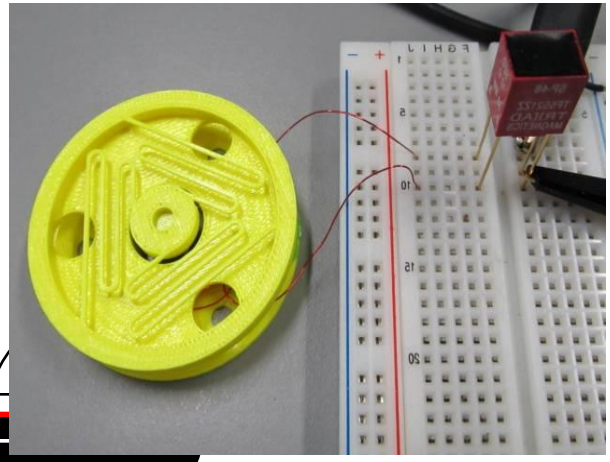
Elliptic is flat in the band pass region, has the steepest transition to band stop region but has some gain in the band stop region

# ELLIPTIC FILTER

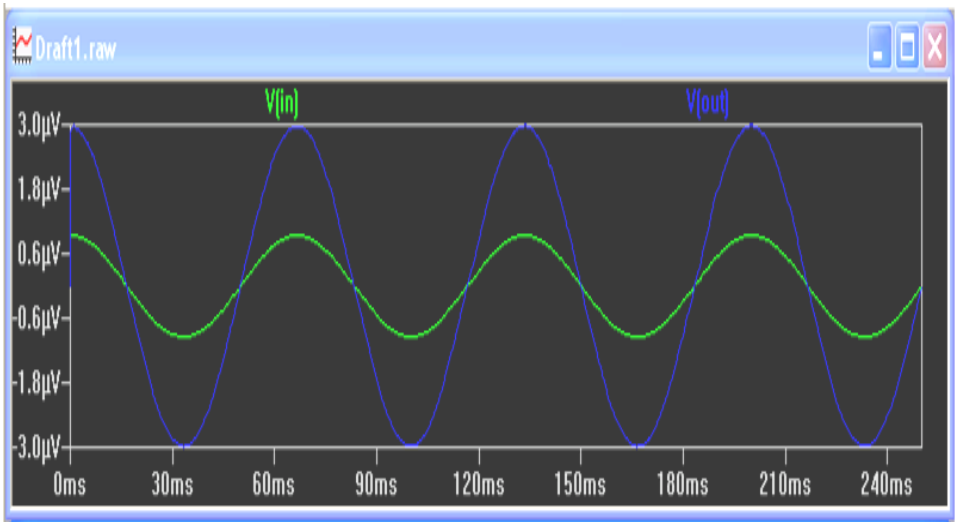


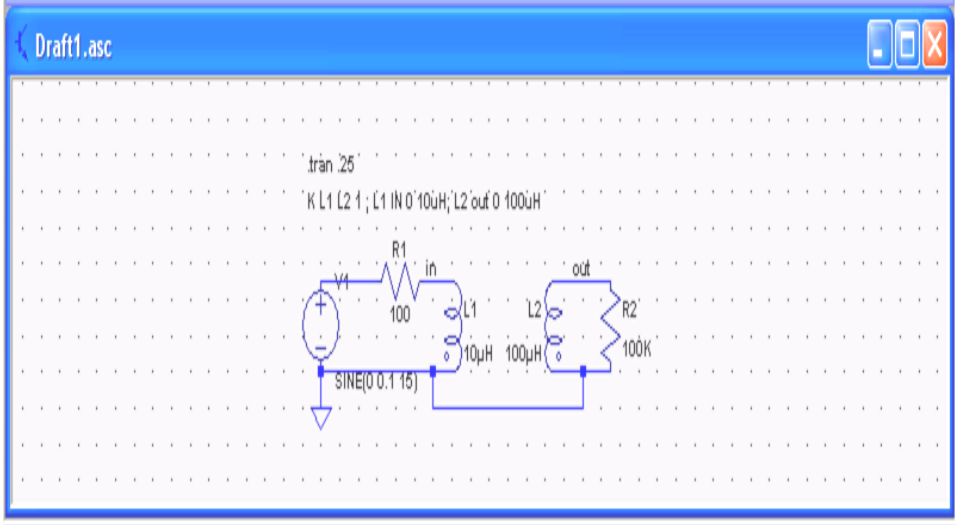
# VIBRATION ENERGY HARVESTER



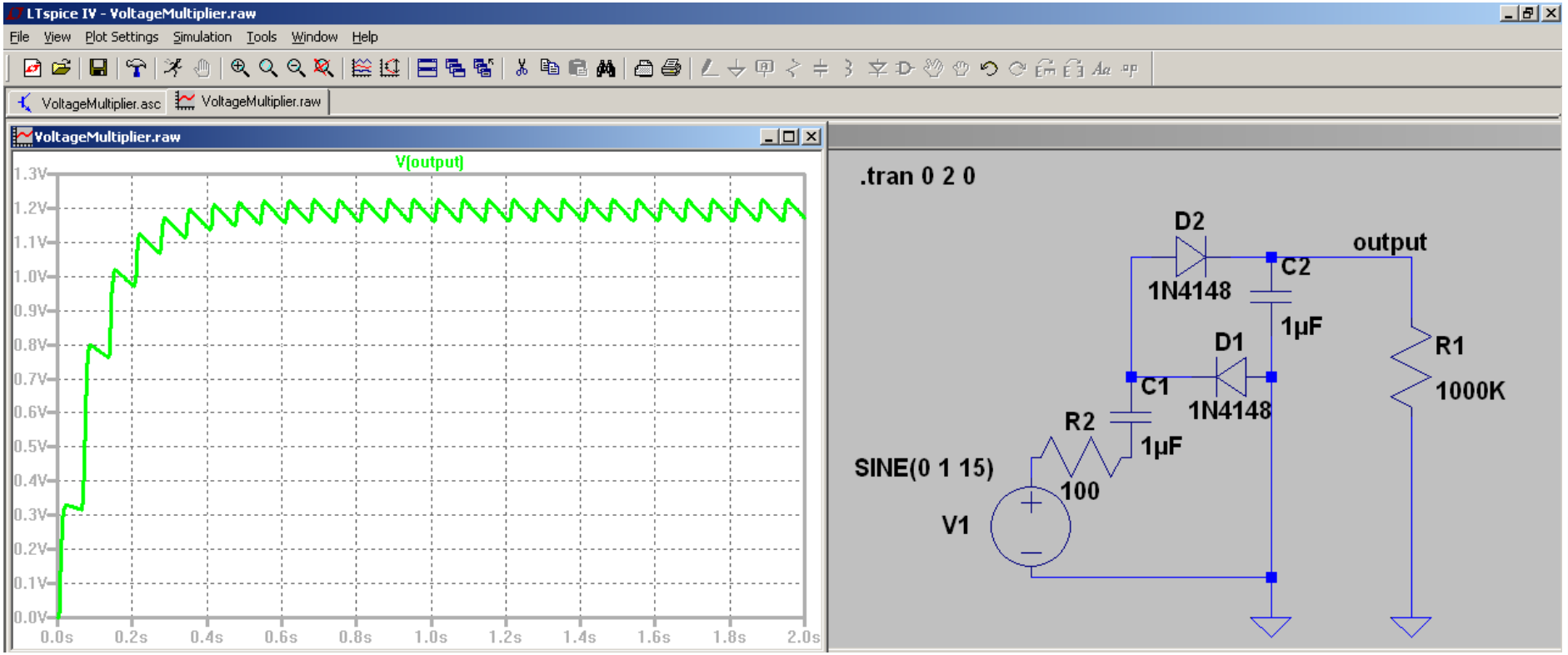



5V / 0.035F



# VOLTAGE MULTIPLIER



# IXOLAR SOLAR CELL – MEASURED CHARACTERISTICS

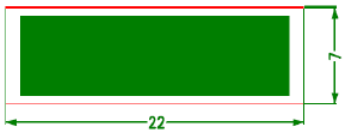
| MEASURED $I_{SC}$ | Cell 1 | Cell2 | Measured Light Intensity |
|---|---|---|---|
| Room Light at Desk Top | 0.0705mA | 0.0509mA | 300 Lux |
| Close to Light Fixture | 1.574mA | 1.560mA | XXX Lux |
| Highest Microscope Illuminator Setting | 51.2mA | 48.6mA | XXX Lux |
| Overhead Projector | 13.6mA | 15mA | XX Lux (~2.5mW/cm$^2$) |
| Direct Sunlight Through Window | 16.0mA | 16.0mA | 65,000 Lux |
| Dark Current | 58.1nA | 17.8nA | zero |
| Series Resistance | 1.6966Ω | 1.5363Ω | |
| Parallel Resistance | >1MEG | >1MEG | |

(~25w/m$^2$ = ~2.5mW/cm$^2$)

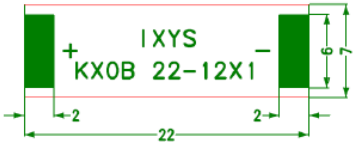
**Package front-side and back-side view.**

IXOLAR – KXOB22-12X1


**SolarBIT Pad Design.** (Dimensions in millimeters)

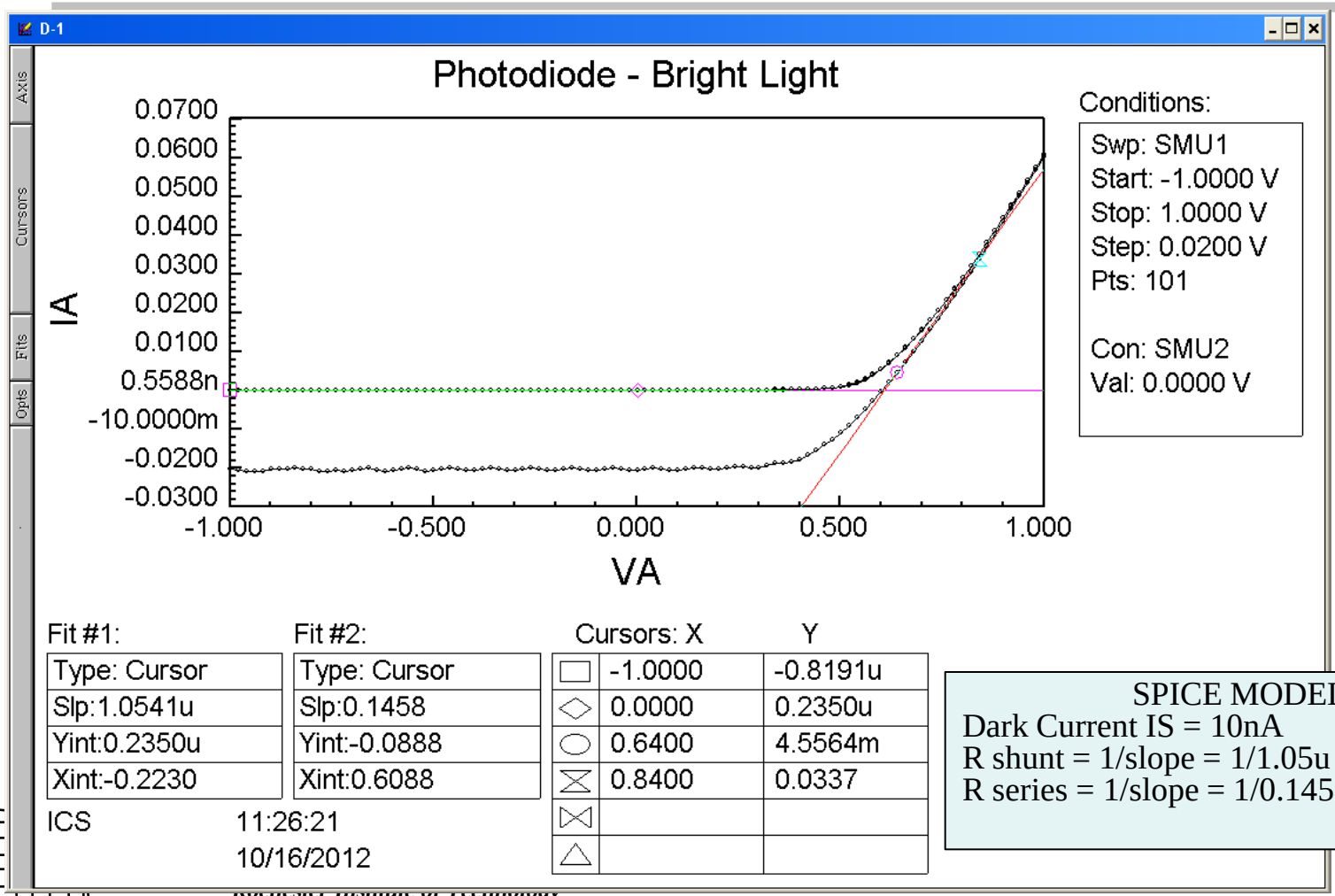



Front-side View details



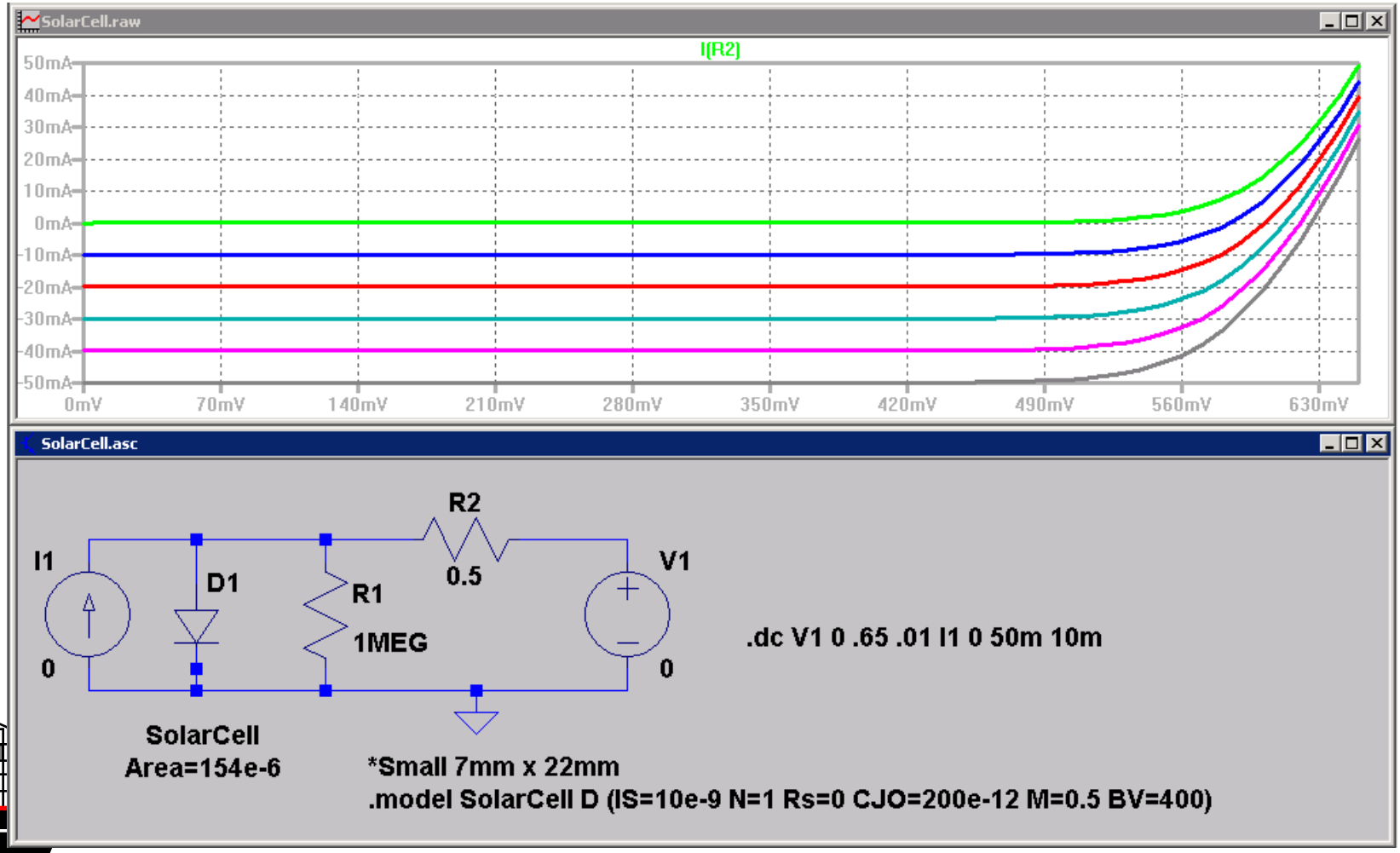

Back-side View details

# EXTRACT SPICE MODEL FROM I-V CHARACTERISTICS




SPICE MODEL
Dark Current IS = 10nA
R shunt = 1/slope = 1/1.05u = ~1 MEG ohm
R series = 1/slope = 1/0.1458 = 6.86 ohm

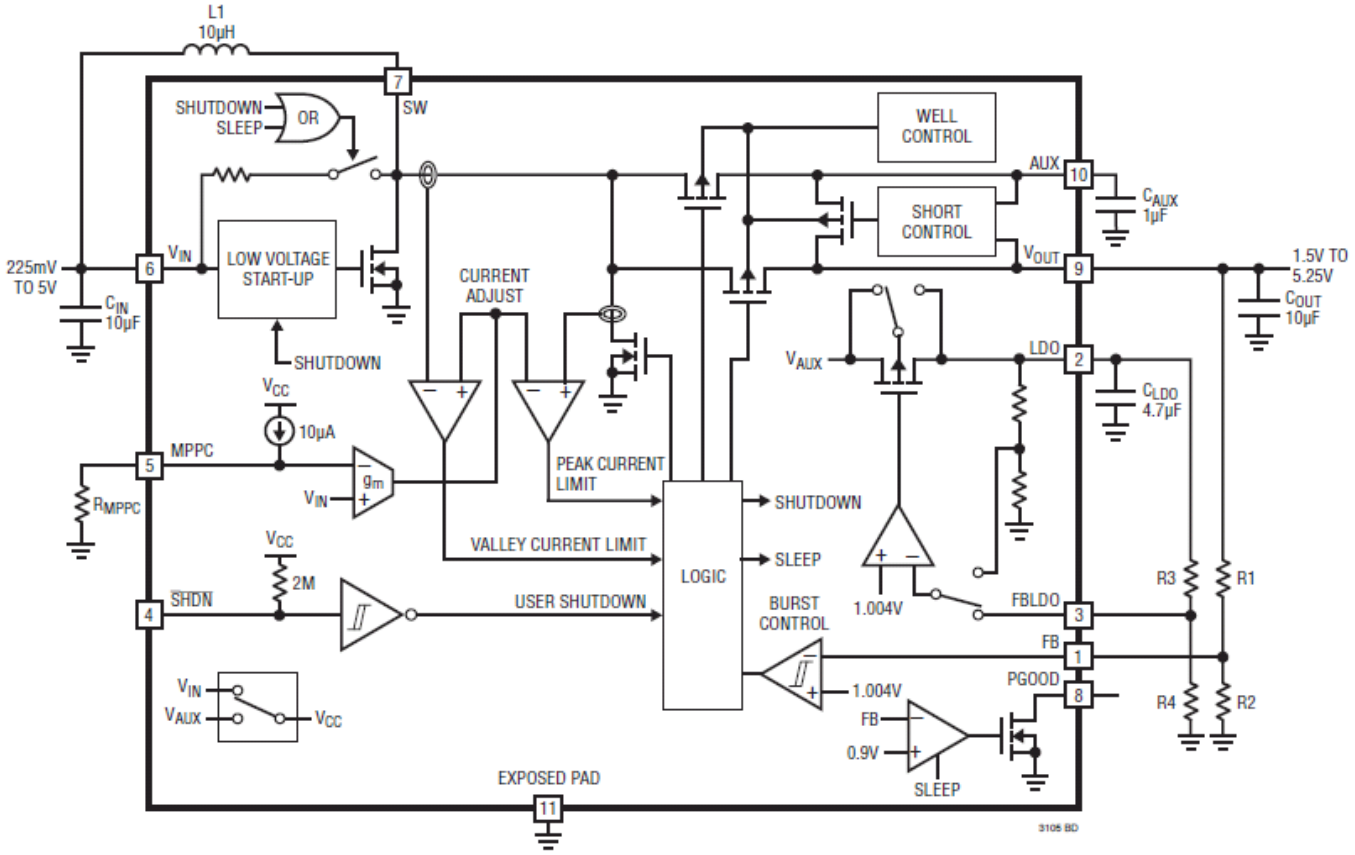
# LTSPICE SIMULATION OF 7MMX22MM SOLAR CELL



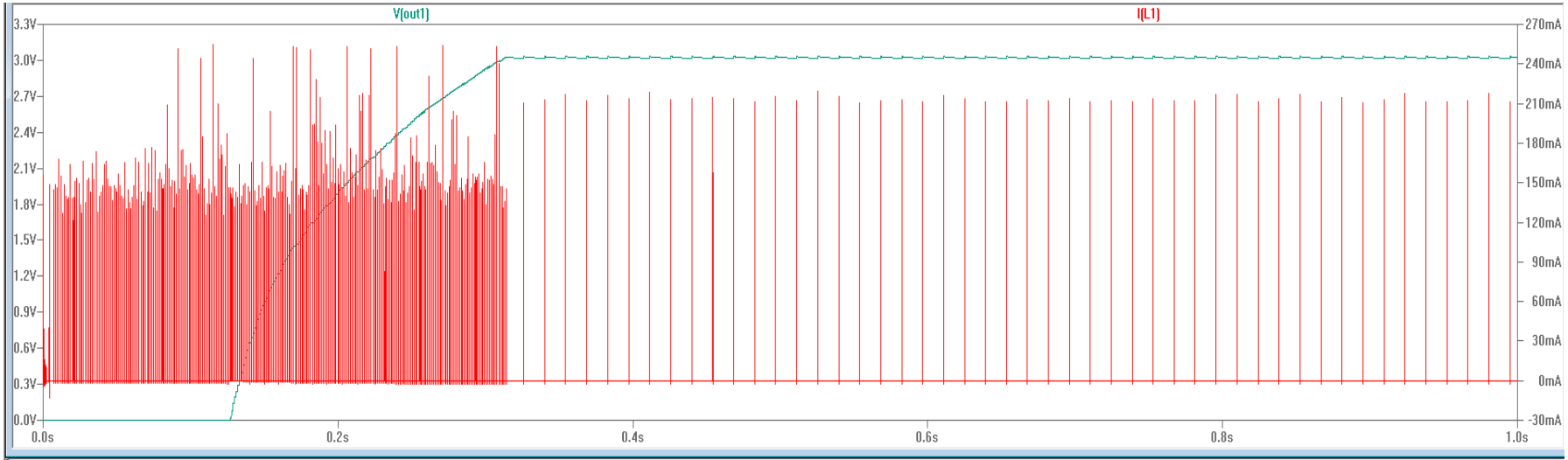
# BLOCK DIAGRAM FOR LTC3105



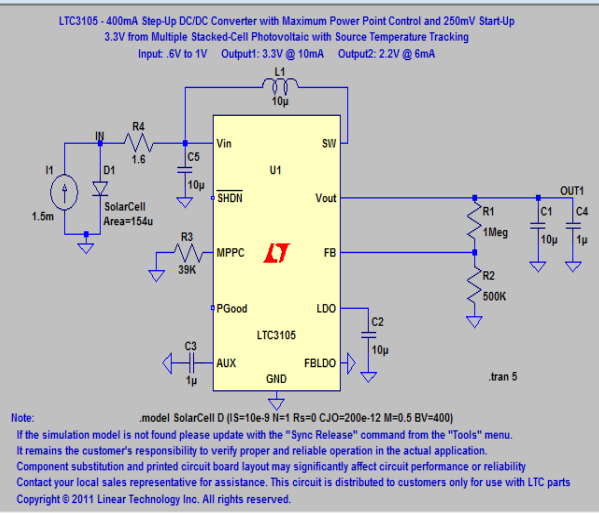
## BLOCK DIAGRAM (Pin Numbers for DFN Package Only)



# LTC3105 OUTPUT VOLTAGE AND INDUCTOR CURRENT



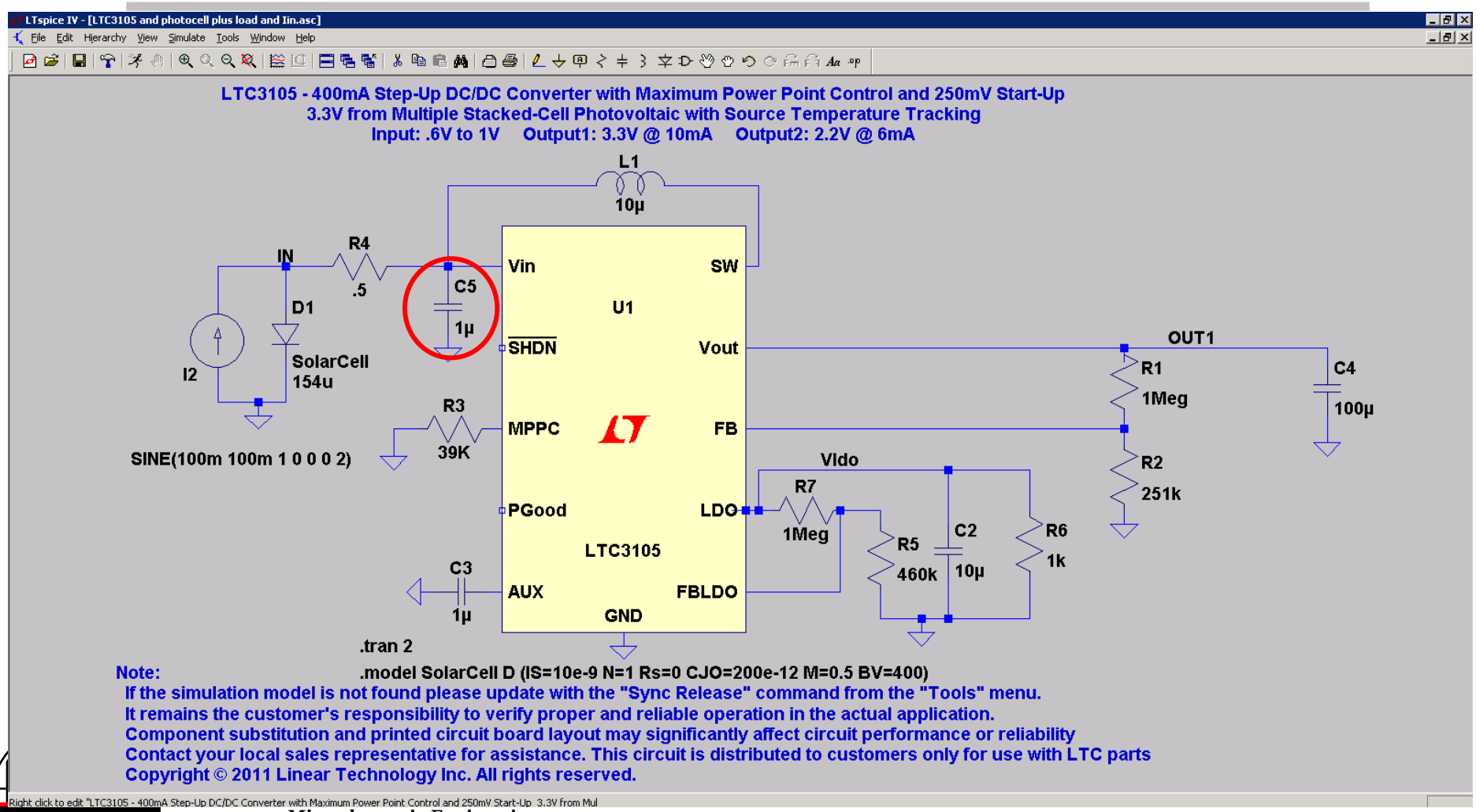

LTC3105 and photocell.asc




LTC3105
DC-to-DC
Converter

Simulation with minimum photocurrent that works
Photocurrent = 1.6 mA
Rs = 1.6 ohms
Rp = infinity

# SIMULATION TO OPTIMIZE TO LOW LIGHT LEVELS

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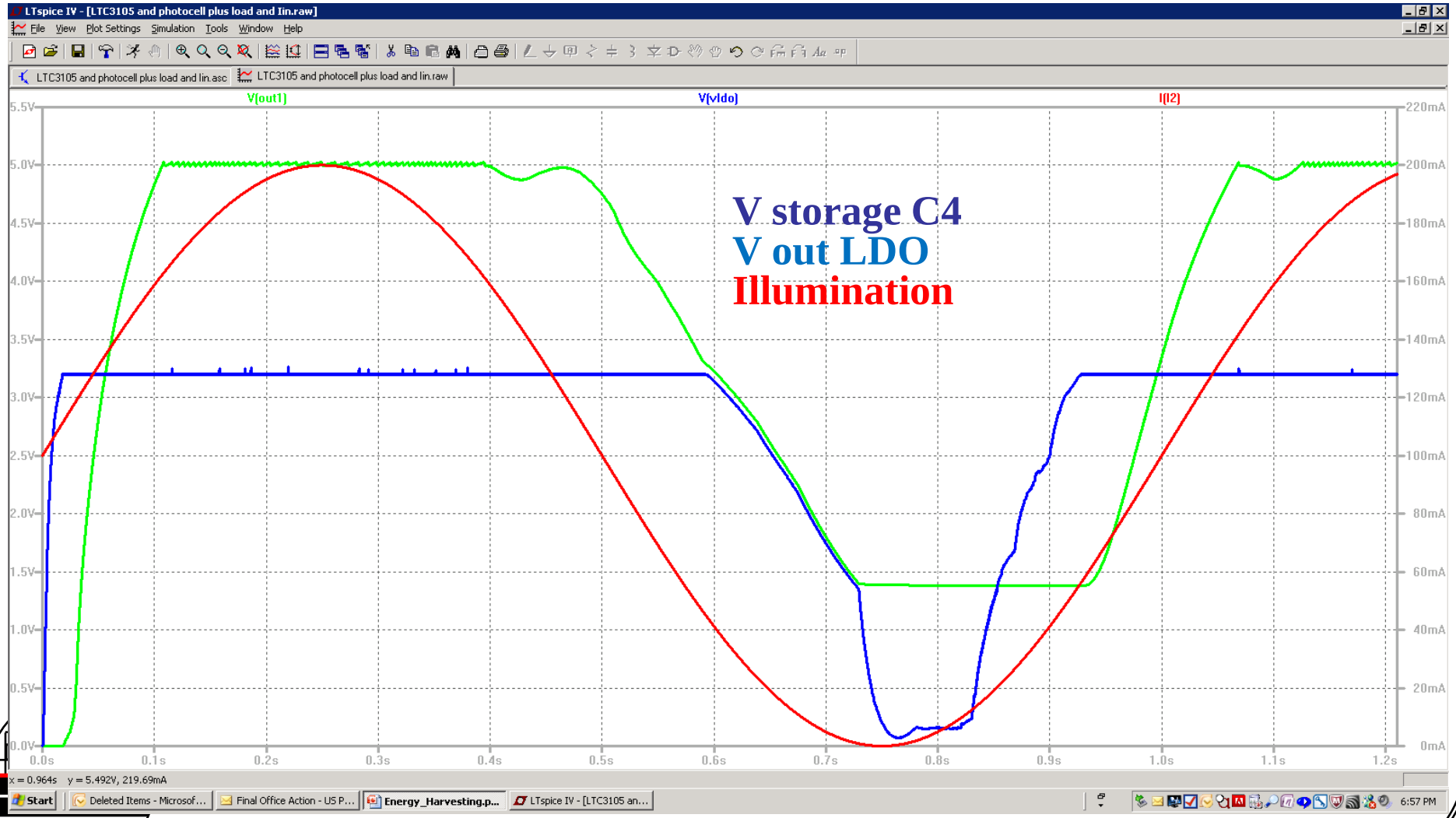
# *SIMULATION TO OPTIMIZE TO LOW LIGHT LEVELS*



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2. Operation and Modeling of the MOS Transistor, 2nd Edition, Yannis Tsividis, 1999, McGraw-Hill, ISBN-0-07-065523-5
3. UTMOST III Modeling Manual-Vol.1. Ch. 5. From Silvaco International.
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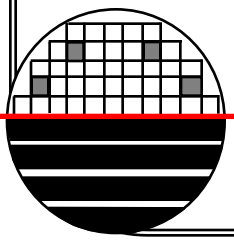
7. ICCAP Manual, Hewlet Packard
8. PSpice Users Guide.

# *HOMEWORK – MORE SPICE EXAMPLES*

Do SPICE for one of the following:

1. Use SPICE to investigate an elliptic filter.
2. Do a SPICE simulation for an Analog Switch that can pass positive and negative voltages. (+/-12 volts using 0- 5 volt logic)
3. Do a SPICE simulation for the two phase non-overlapping clock circuit.