ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

CMP and Lithography Considerations for Shallow Trench Isolation (STI)

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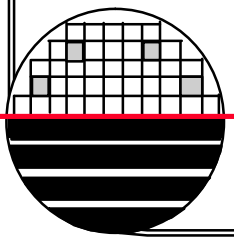
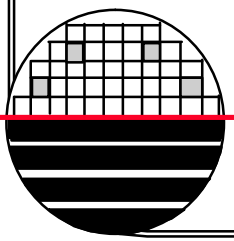


INTRODUCTION

We have made great progress in doing the CMP for our advanced CMOS process shallow trench isolation (STI). The progress has been made through:

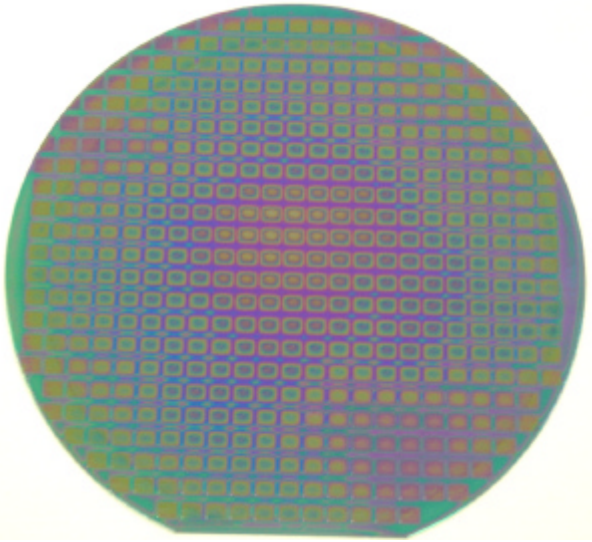
1. Getting the Westech CMP tool working correctly.
2. Getting a slurry especially made for STI that removes oxide and stops on nitride.
3. Adding tiles (dummy features) to the mask area outside of the active regions during computer aided transcription CATS prior to maskmaking.



WESTECH CMP TOOL USED AT RIT

NEW FACTORY STI RECIPE (FACTSTI)

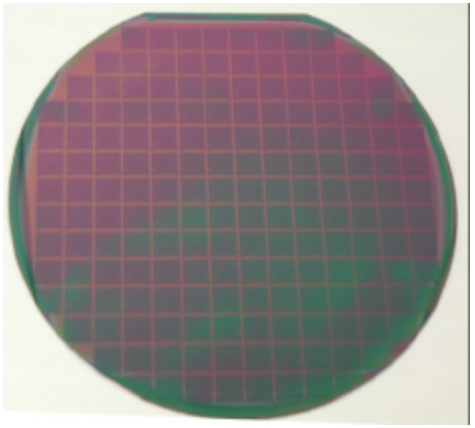
- Carrier speed: 30 RPM
- Platen speed: 100 RPM
- Without back pressure
- 8 PSI down force (36 PSI on the gauge)
- Slurry (Celexis CX94S CeO_2, ph=7)
- Slurry flow rate (60 mL/min)
- Pad conditioning: before every run
- Temperature: 80°C
- Polishing time: 2min 30 sec for 6500A oxide

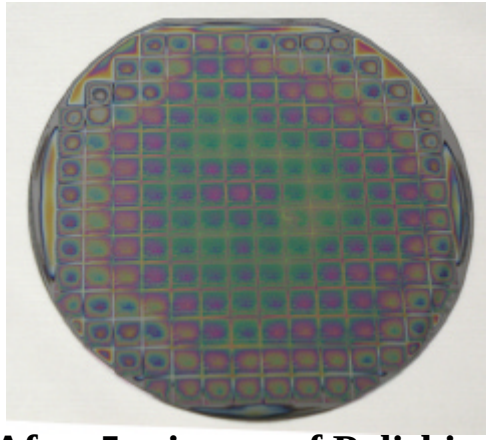


COMPARISON BETWEEN OLD CMP SLURRY AND PROCESS AND NEW SLURRY AND PROCESS

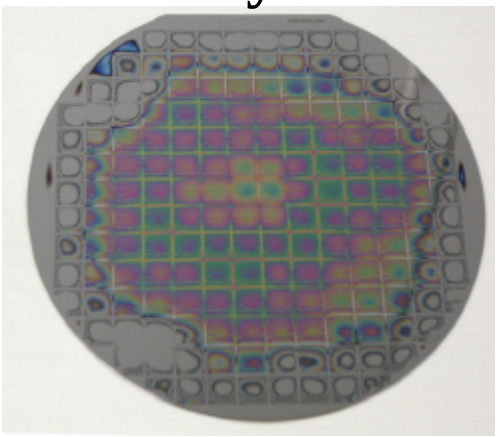
Old Process and Slurry

Wafer before CMP





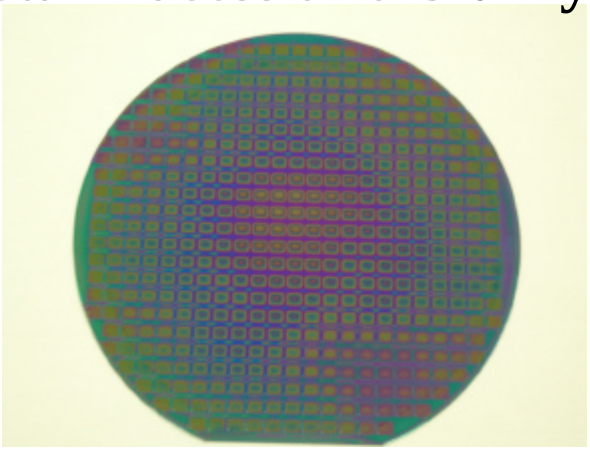
After 5 minutes of Polishing
Center not done

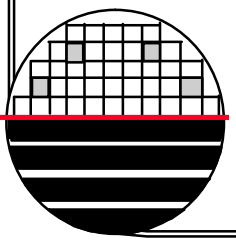


After 9.5 minutes of Polishing
Center done, Edges Bare

New Process and Slurry

After 2.25 minutes of Polishing
Clear almost every die
Even edge die





CMP SLURRY SUPPLIER

Eminess Technologies, Inc.
1620 West fountainhead Pkwy, Suite 510
Tempe, AZ 85282
Tel (408)505-3409, 888-899-1942,
fax (480)951-3842

Darlene Werkmeister
Dwerkmeister@eminess.com

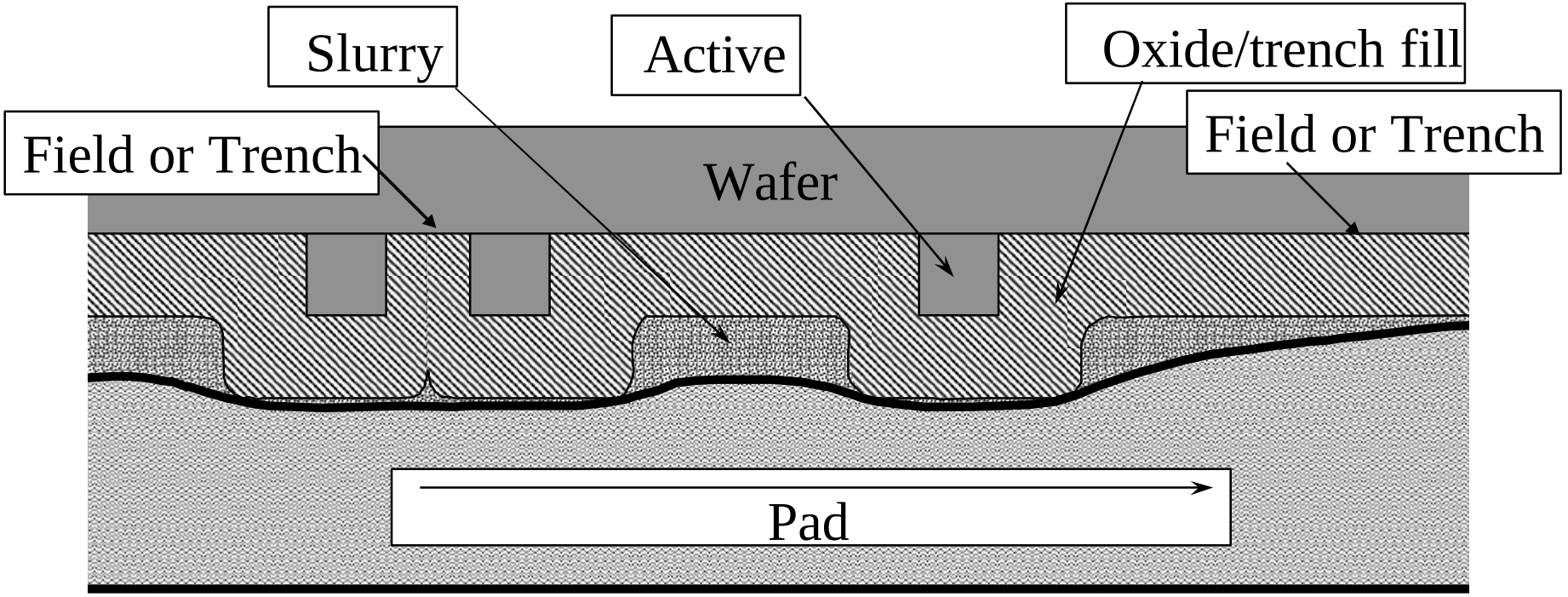
http://www.EMINESS.com
http://www.electronicmaterials.rohmhaas.com

1/05/06 Order:
N-2350-P Nalco 2350, 5 gal pail $166 each, Mfg by Rohm and Haas,
Silica, 70-100nm particle size, weight % 28, KOH, pH 11.4-12.4

R-10027556 Klebosol 1501-50 Colloidal Silica 5 gal pail $255 each,
Mfg AZ Electronic Materials, Clariant's Klebosol line of silica slurrys,50nm particles, KOH pH 10.9 50% solids

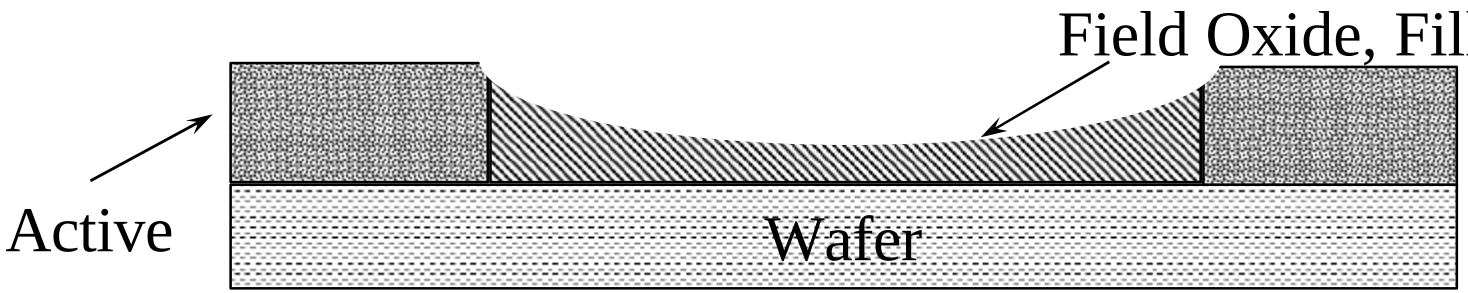
R-10087555 EXP CELEXIS CX94S Single Component Slurry, 20Liter pail $235 each, Mfg by Rohm and Haas Ceria 20nm particles, STI, pH ~7

PAD - SLURRY - SURFACE INTERACTION

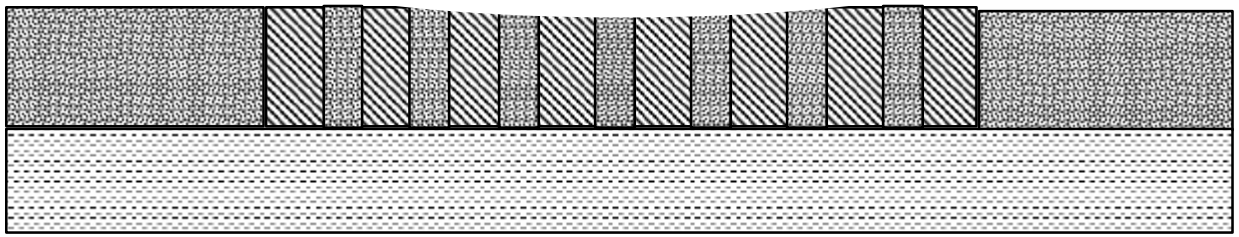


Pad saturated with slurry.
Polishing pressure greatest on small, elevated features (active).
Pad may contact larger low areas (large field regions) called dishing.

DISHING AND TILES



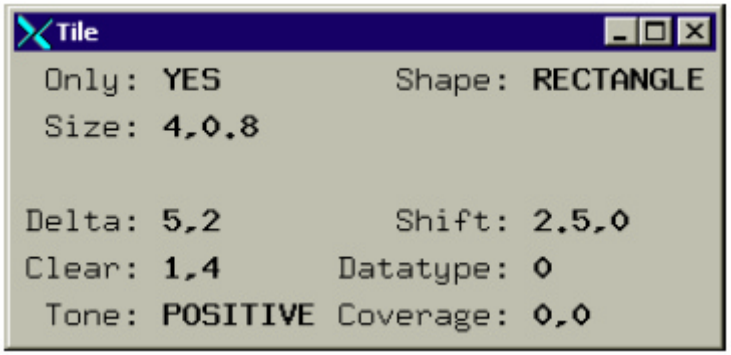
Dishing: large area becomes recessed
especially with over polishing



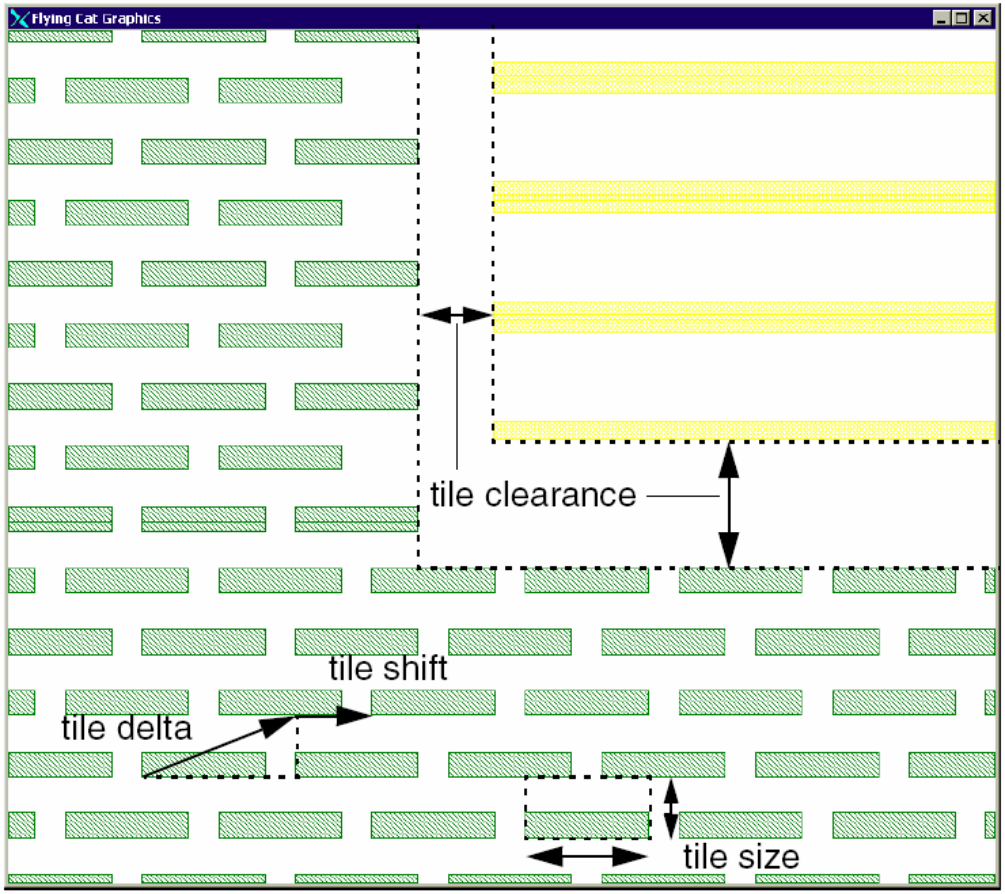
Multiple small dummy features (tiles) are used to reduce Dishing.

TILING FOR STI LAYER MASKMAKING

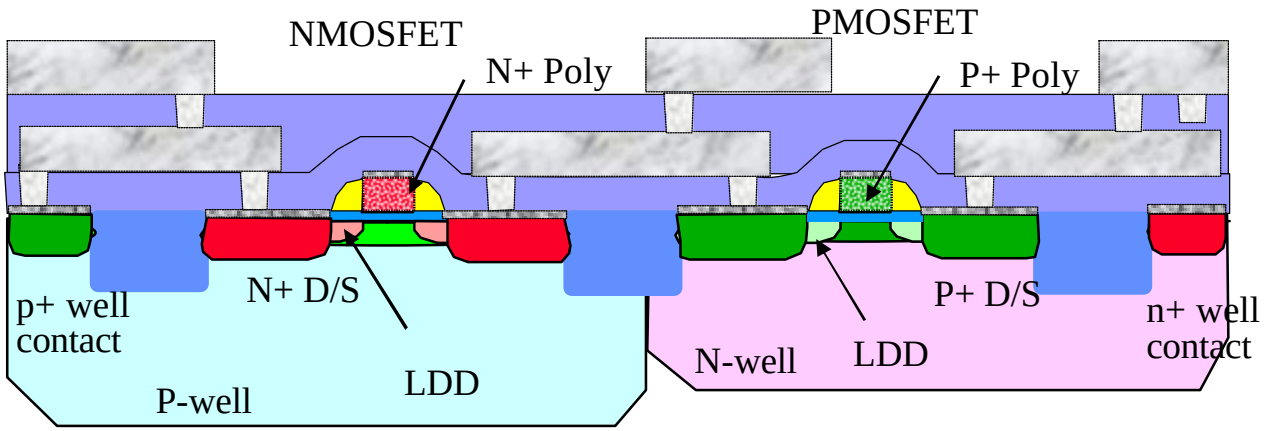
Synopsys, Inc.
CATS Software for transcription of CAD design files into readable e-beam and laser formats.



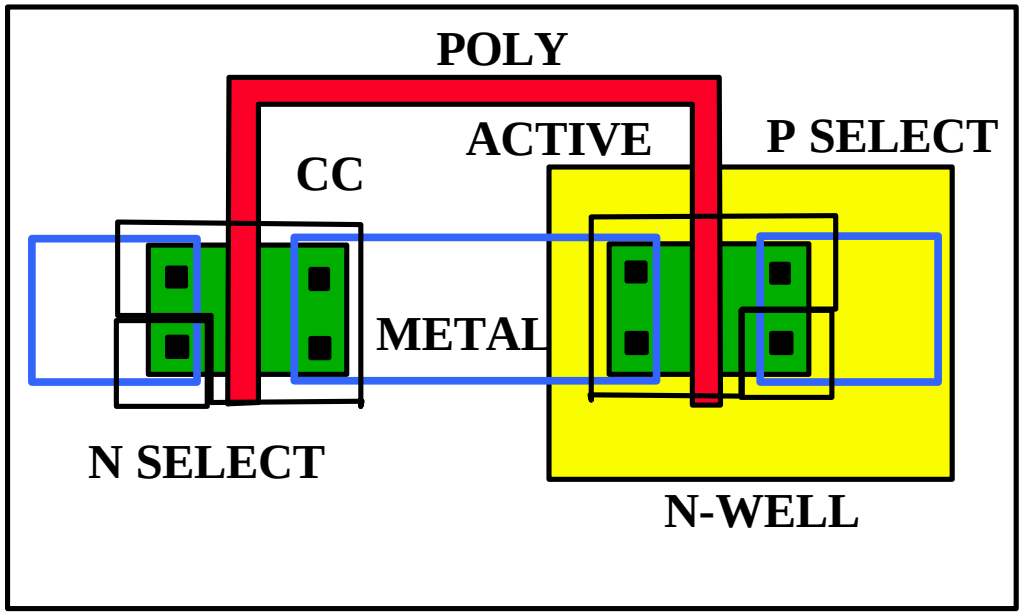
Tiles are defined by these parameters

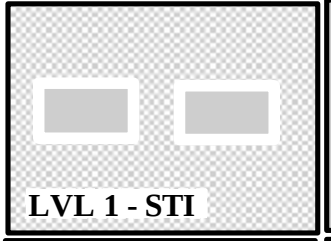


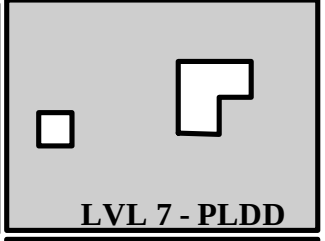
RIT ADVANCED CMOS

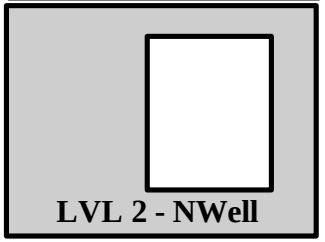


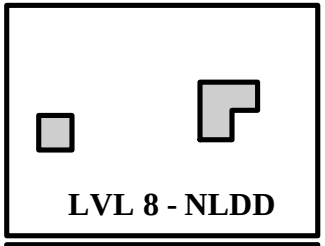
14 PHOTO LEVELS

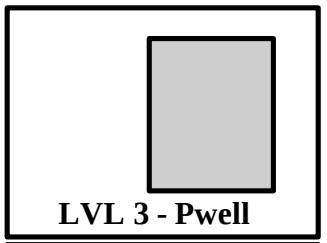


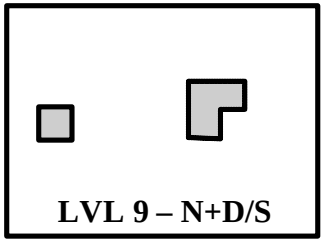


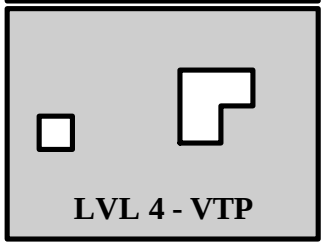


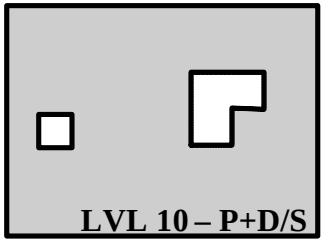


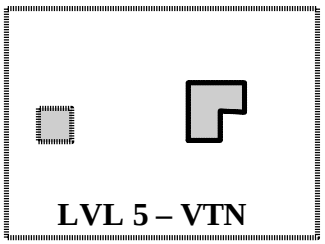


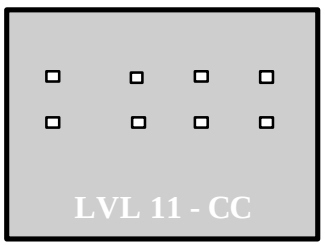


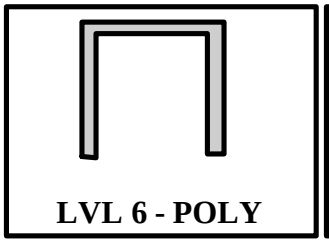


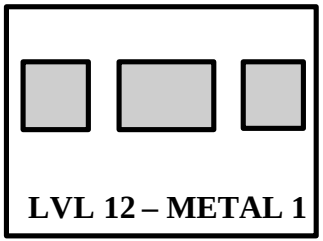






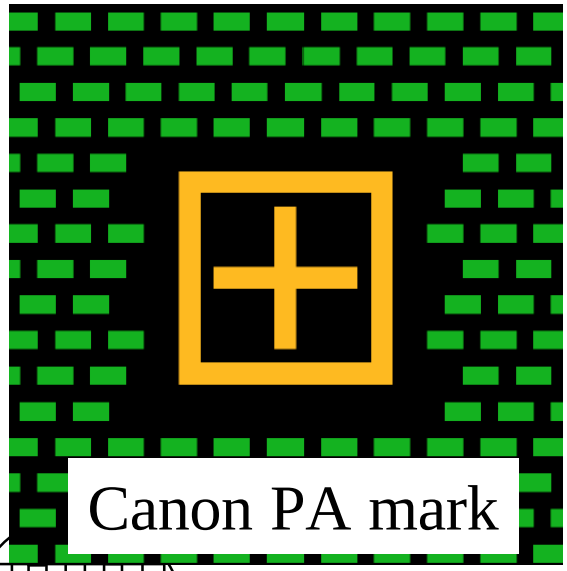




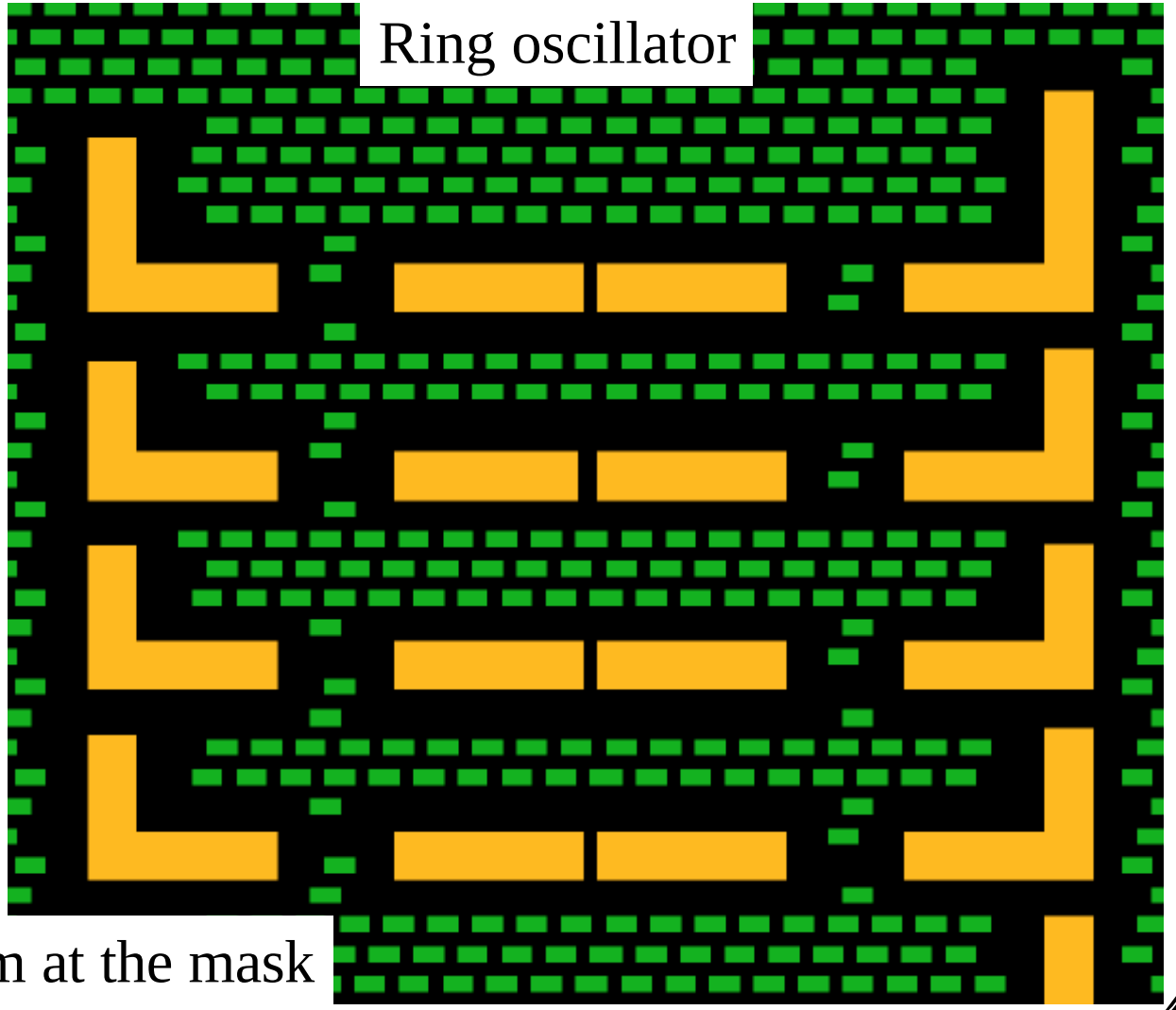


TILING FOR RIT'S ADV-CMOS PROCESS STI LEVEL

COMPACT NO
TILE ONLY NO
TILE SHAPE RECTANGLE
TILE SIZE 50,25
TILE DELTA 75,50
TILE CLEAR 50,50
TILE SHIFT 25,0



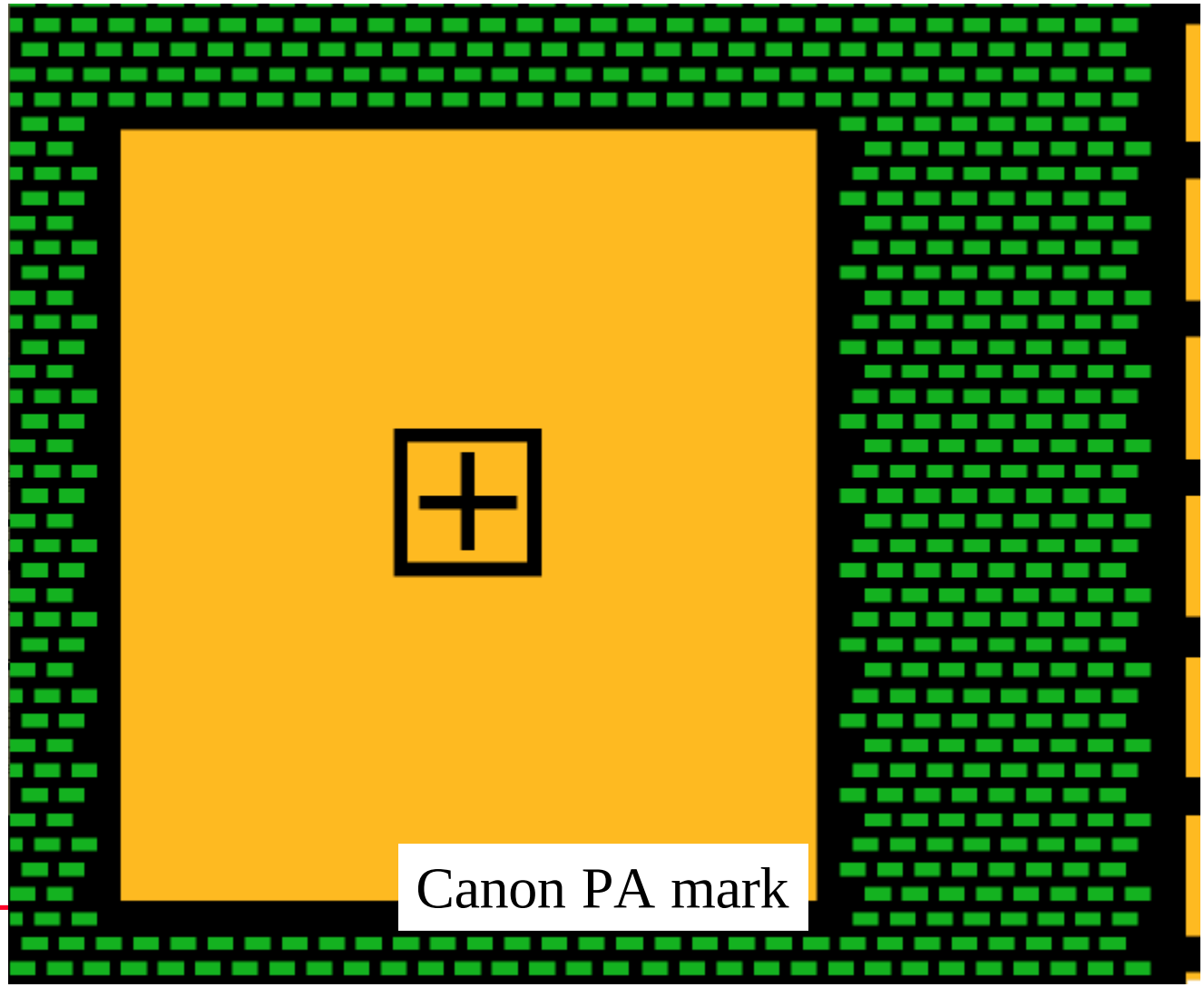
Canon PA mark



Ring oscillator

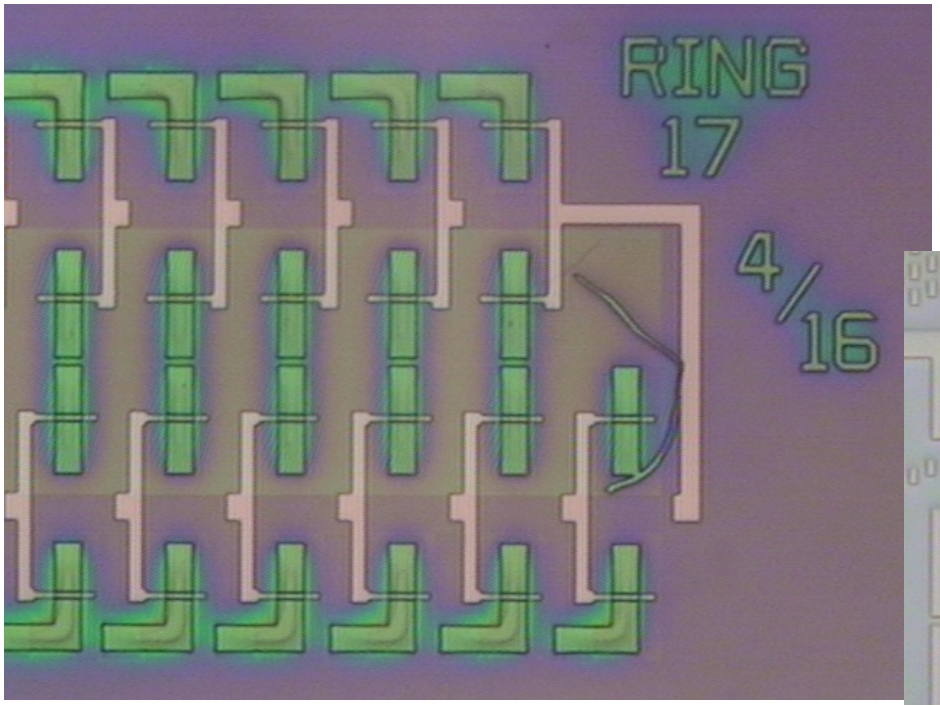
Sizes are in µm at the mask

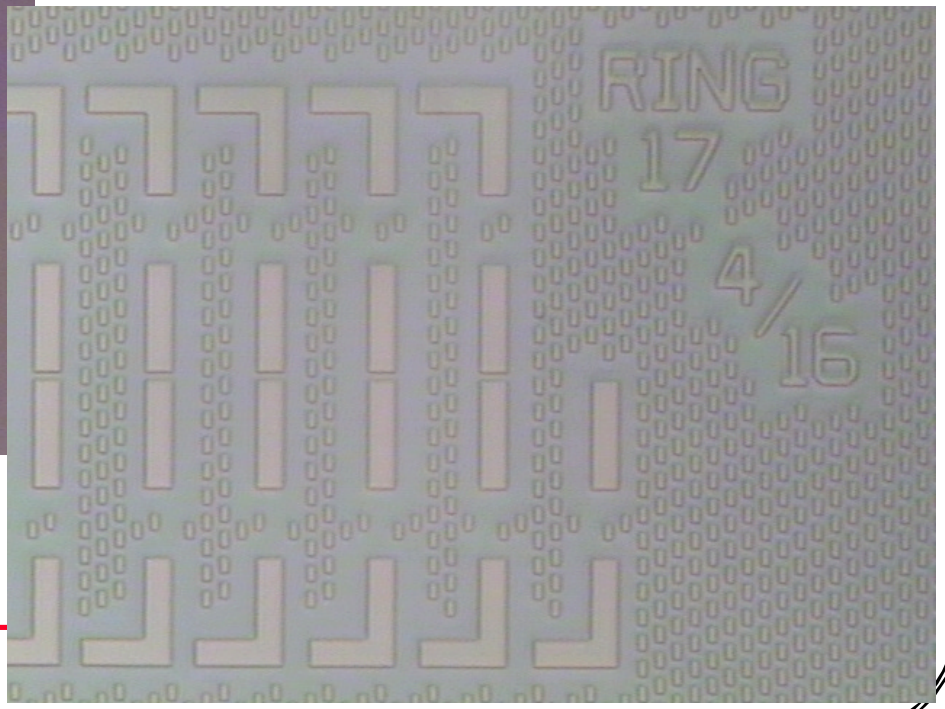
REMOVE TILING NEAR ALIGNMENT MARKS



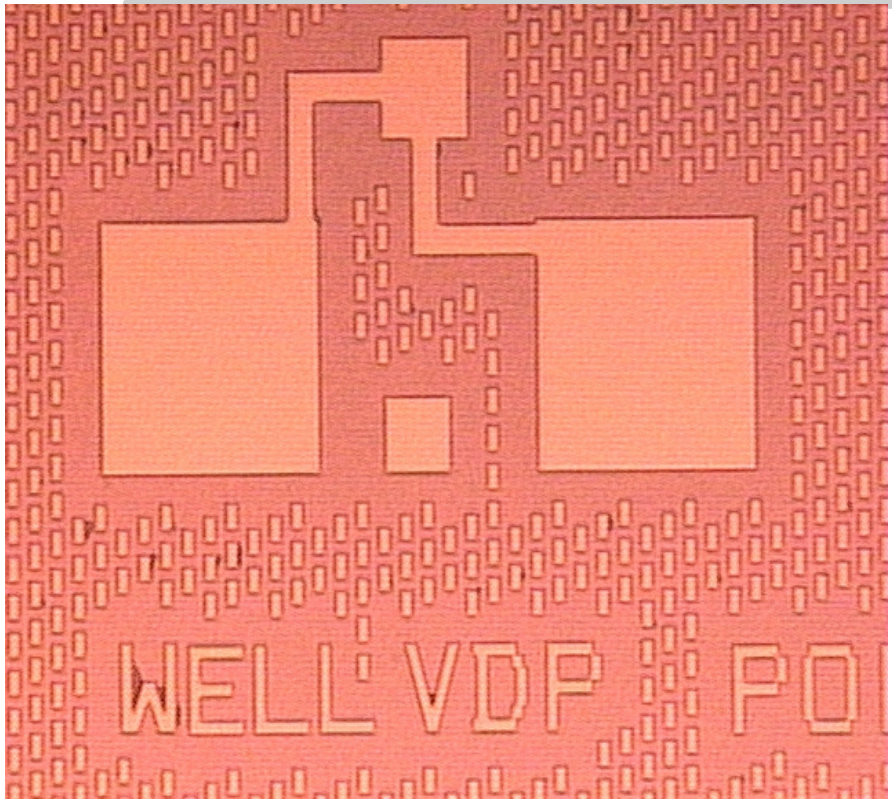
CMP RESULTS ON TILED DIE

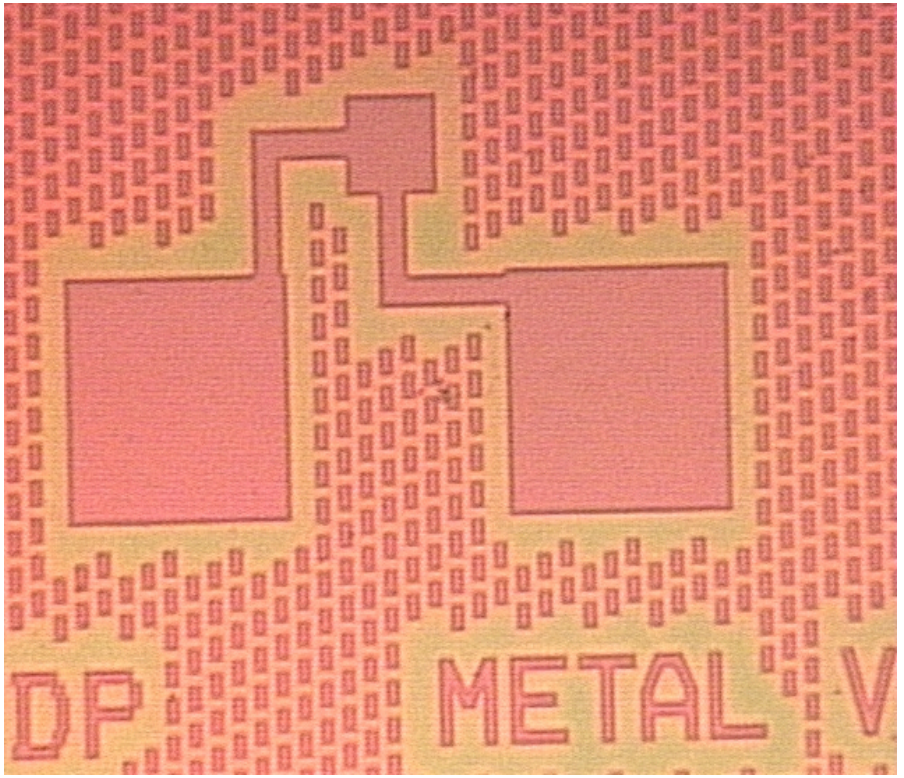
Comparison of pictures of dies with and without tiles for uniformity of oxide thickness in the trenches (field regions) after CMP.



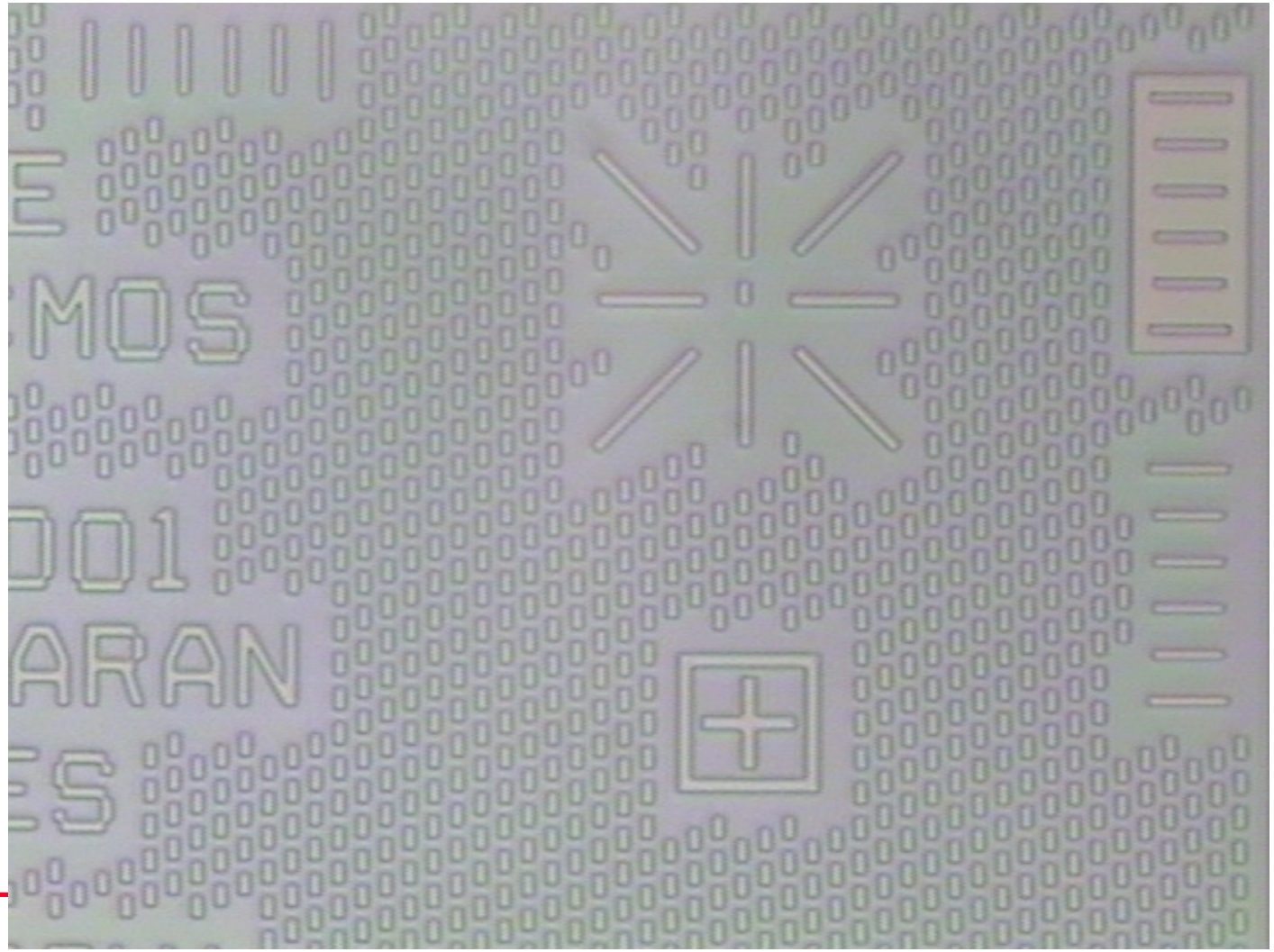


VDP Structure before and after CMP at 20x Zoom

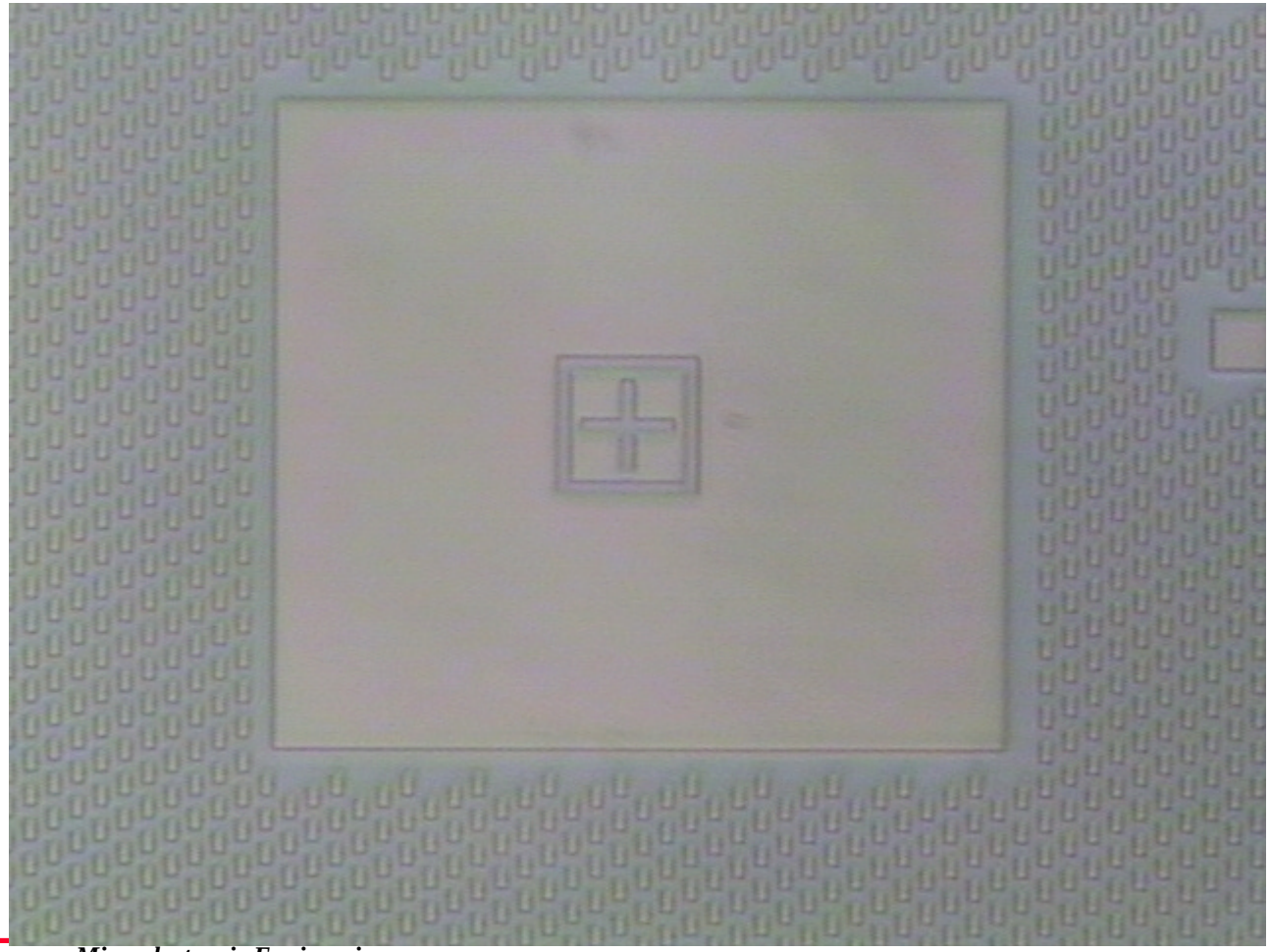




PA FINE ALIGNMENT MARKS WITH CLOSE TILING



PA MARK AND REMOTE TILING



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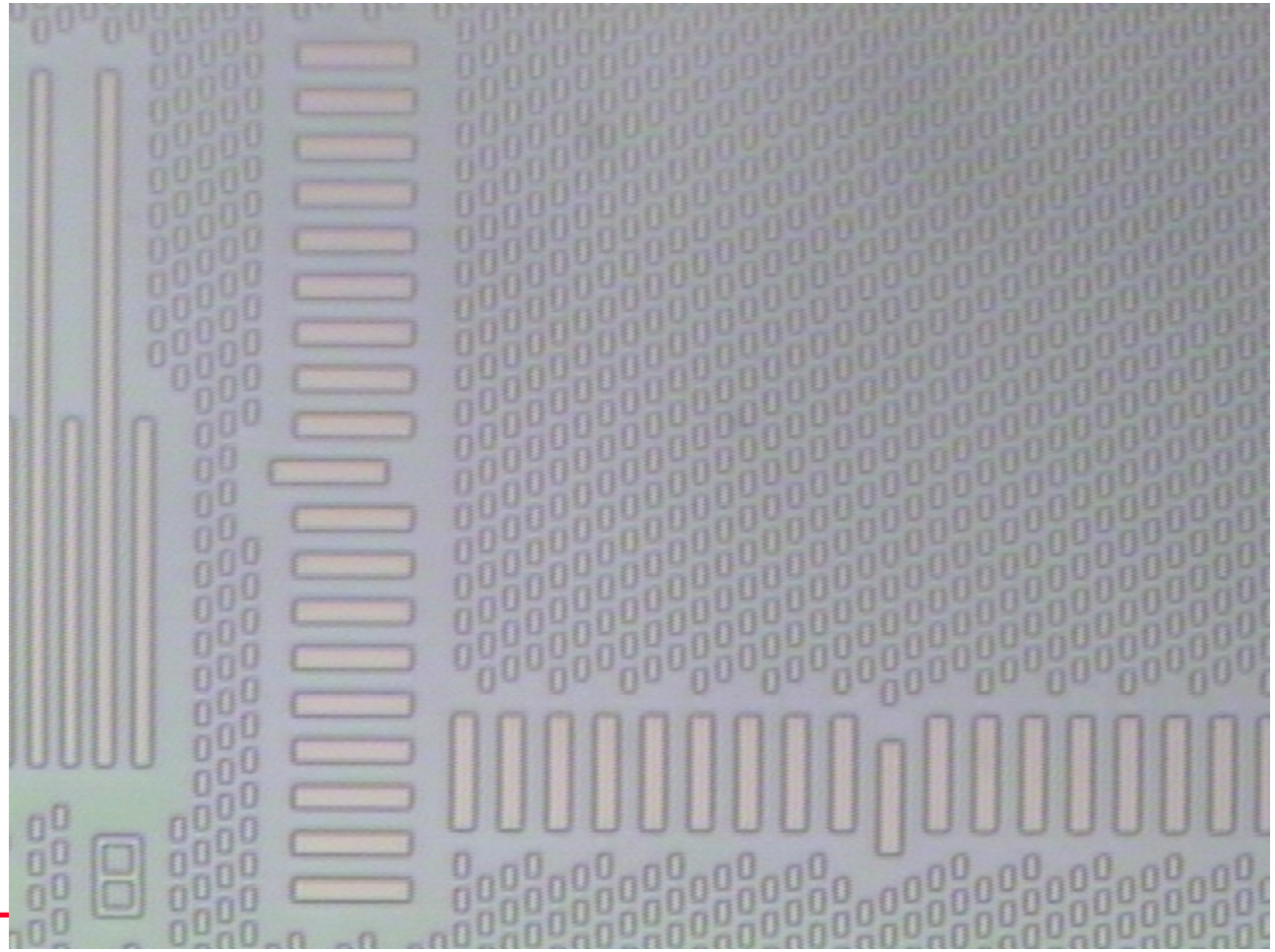
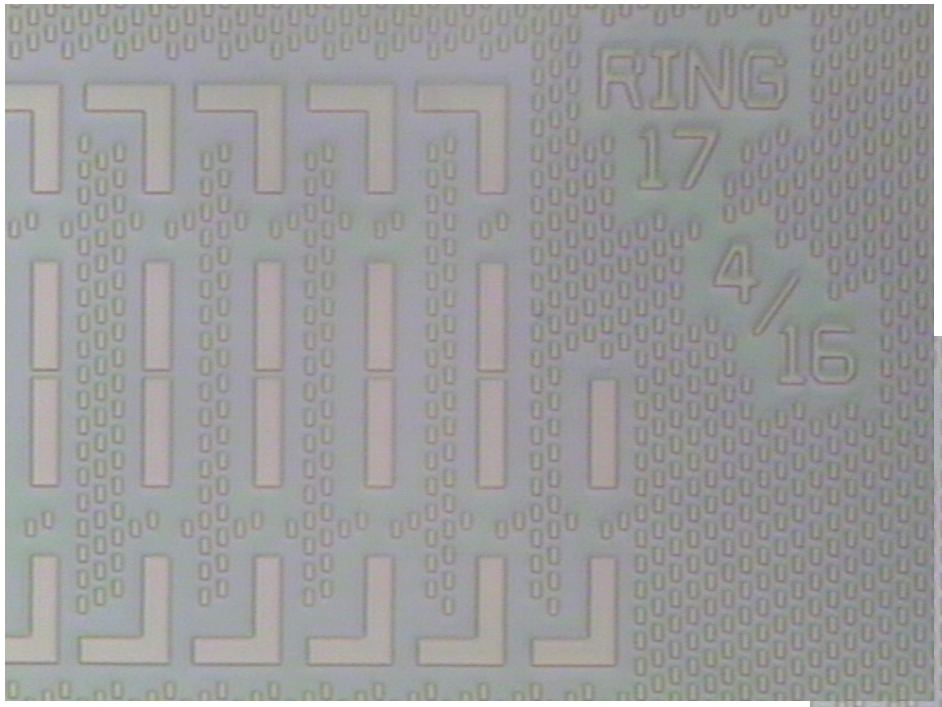
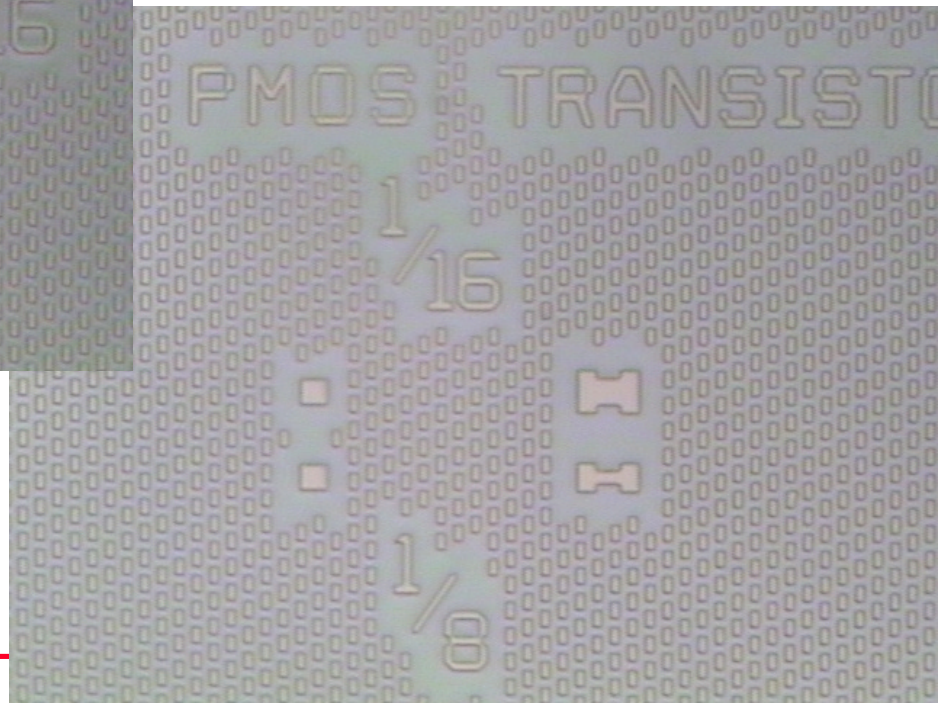
TILING NEAR RESOLUTION AND OVERLAY

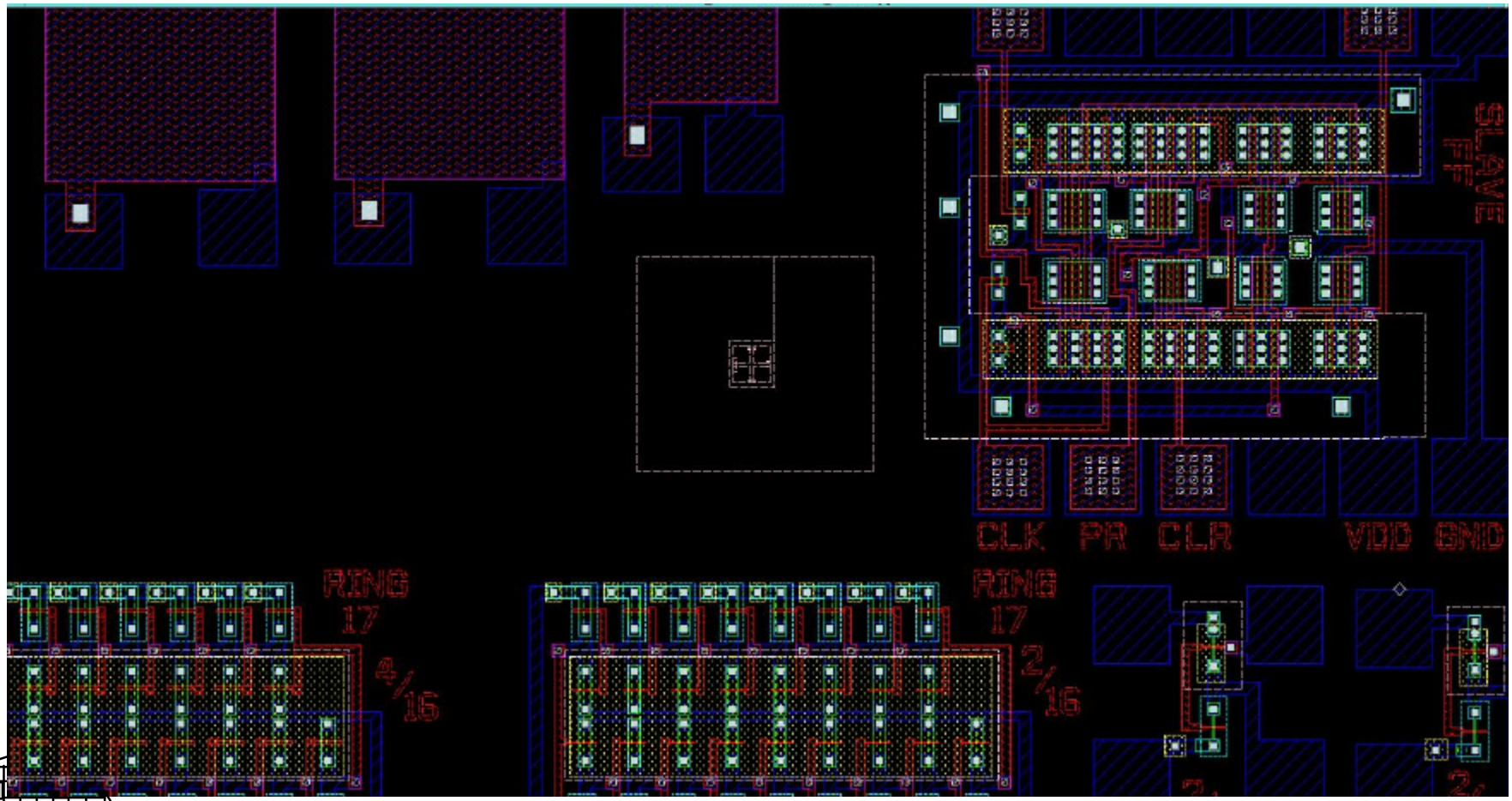


TILING NEAR DEVICE ACTIVE AREAS

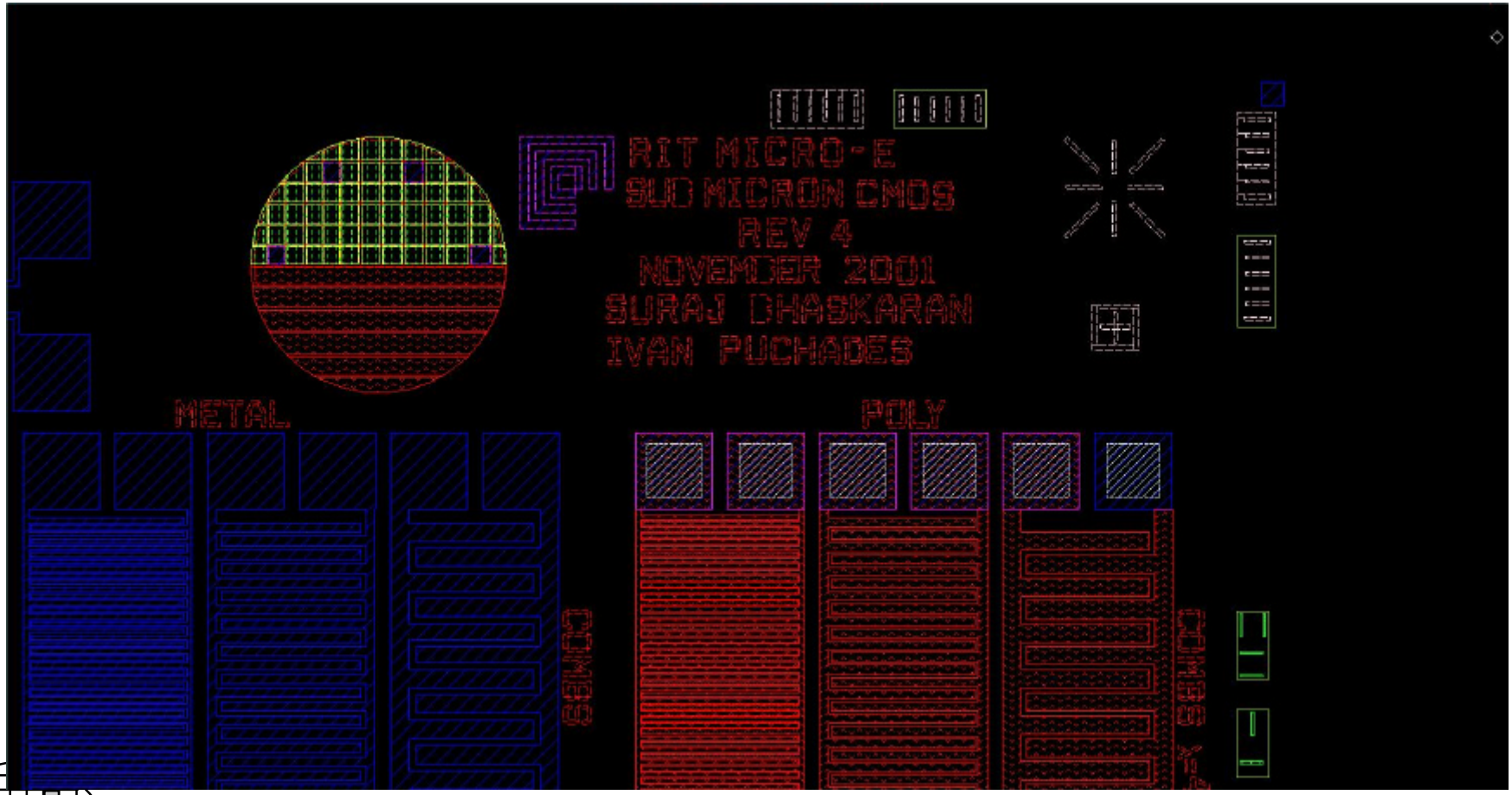




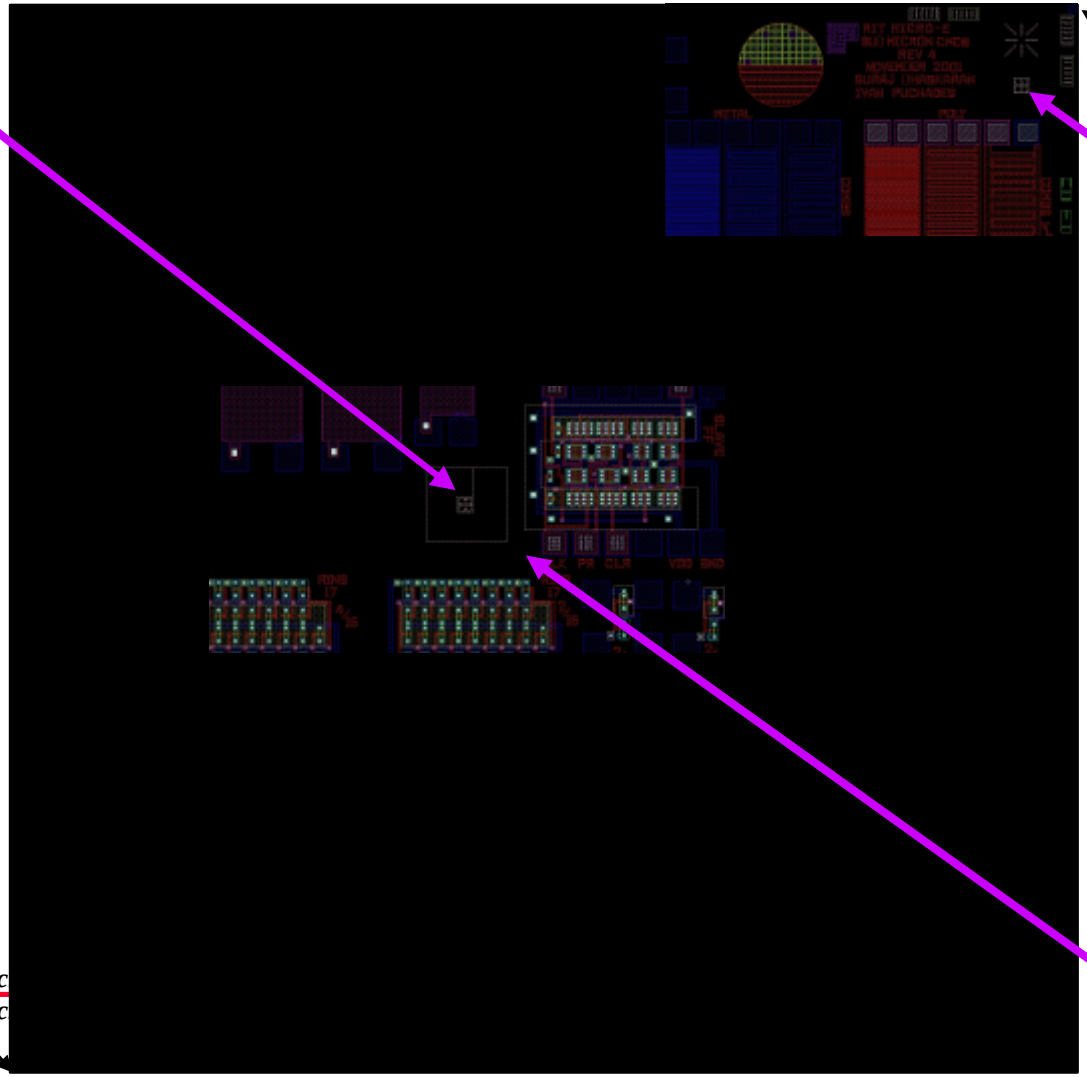
NEW ALIGNMENT PA MARK NEAR CENTER OF DIE



LOCATION OF ALIGNMENT KEYS – UPPER RIGHT



ALIGNMENT KEY LOCATIONS



New PA Mark
(-310,420)

(4840,3940)

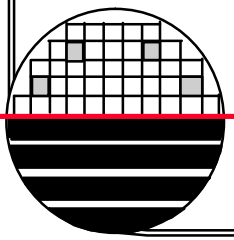
Old PA Mark
(0,0)

(0,0)

Die Center
(2420,1970)

ALIGNMENT KEY OFFSETS FOR CANON STEPPER

Lower Left Corner location: (0,0)
Upper Right Corner: (4840,3940)
Center of PA Mark Close Tiles: (4620,3620)
Center of PA Mark Remote Tiles: (2110,2390)
Center of B scope (Y) Fine Alignment Multi-marks: (4805,3840)
Center of C scope (X) Fine Alignment Multi-marks: (4230,3905)
Center of Die: (2420,1970)
Location of PA Mark Close Tile, relative to Die Center: (2200,1650)
Location of PA Mark Remote Tile, relative to Die Center: (-310,420)
B scope (Y) Fine Alignment Multi-marks, from die center: (2385,1870)
C scope (X) Fine Alignment Multi-marks, from die center: (1810,1935)



MORE ON ALIGNMENT KEY OFFSETS

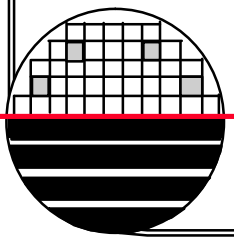
A stray box was found outside the bottom edge of the chip on one layer. This causes some of the y-measurements to be incorrect. We don't know the exact location of the stray box because it was deleted before we measured its location.

We determined the correct offsets empirically:

TVPA (-0.310, 0.466) 0.046 larger than theoretical
B scope (2.385, 1.916) 0.046 larger than theoretical
C scope (1.81, 1.981) 0.046 larger than theoretical

So the box lower edge must have been 0.092mm below the bottom of the chip

These numbers are used in the stepper job/process file on page 4 and 13.



CANON STEPPER - PROCESS FILE EDITOR

PROCESS EDITOR (File ID)### (page-1)

File name; FADVCMOS_NWELL

1. Comment;

2. Alignment Sequence: 1st Mask or AGA …. AGA

3. TTL Alignment Mode (none, I-line or HeNe/B^2) HeNe-TV

4. TV PA Measurement Mode; PA

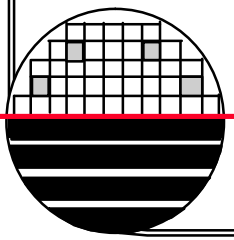
PROCESS EDITOR (Reticle ID)### (page-2)

1. Reticle ID Active

PROCESS EDITOR (Fine Reticle Alignment)### (page-3)

1. Fine Align Tol xy = 0.03 µm Theta = 0.03 µm

The Process file has 36 pages, only highlighted pages can be accessed, if AGA in item 2 page 2 is selected then page 4 is highlighted and gives row and column and x,y location of the prealignment marks. If alignment mode HeNe is selected page 13 gives the x&y coordinates of the fine alignment marks, if I-line was selected then pg 10&11give fine alignment mark locations



CANON STEPPER - PROCESS FILE EDITOR (cont.)

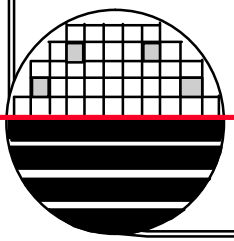
PROCESS EDITOR (TV Prealignment-1)### (page-4)

1. L) Shot ; clm = 3 row = 12
   PA Mark Position; Xlp = -0.310 mm Ylp= 0.466 mm
2. R) Shot ; clm = 20 row = 12
   PA Mark Position; Xlp= -0.310 mm Ylp= 0.466 mm

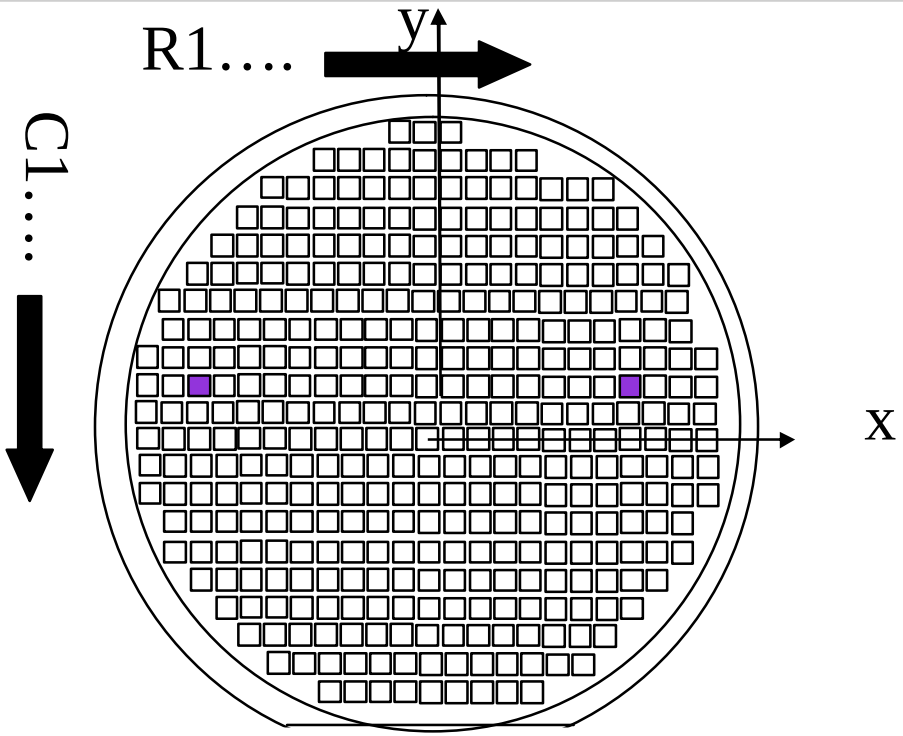
note: this is where the user inputs the **pre alignment (TVPA)** mark locations. X and Y locations are relative to the center of the die

PROCESS EDITOR (HeNe TV Alignment - 2)### (page-13)

note: this is where the user inputs the **fine alignment** mark locations for HeNe or Broadband (B^2) alignment method. X and Y locations are relative to the center of the die. Page 4 and 13 make it possible to overlay two levels



CANON – LAYOUT



Location, row and column, and distance from center of die to center of TVPA mark.

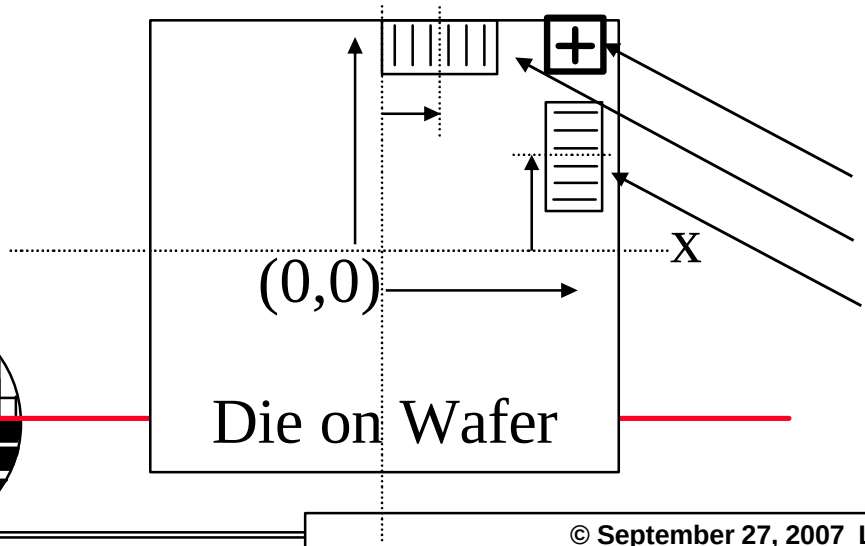
CANON STEPPER - PROCESS FILE EDITOR (cont.)

PROCESS EDITOR (HeNe TV Alignment - 2)### (page-13)

1. AA Mark Position; B X = 2.385 mm Y = 1.875 mm
   C X = 1.810 mm Y = 1.935 mm
   Brot X = 0.00 Y = 0.00
2. AA Mark Pattern: 20P-4F
   XY Mark: Multi
3. Mark Condition (Window or Island) Island
4. Wafer Surface Condition 0

20P means 20um pitch
4F means 4um feature

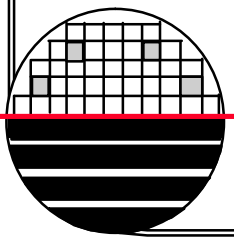
0 or 1 means default ~4um
2 means 4um marks are ~3.2um
3 means 4um marks are ~1.6um
4 means 4um marks are ~4.8um
5 means 4um marks are ~6.4um



Pre Alignment Mark
C mark is for x alignment
B mark is for y alignment

DEFINITIONS

Island/Window describes the slope of the edge of the multi-marks. If the marks are mesa shaped it is called an island. If the marks are below the surface (as in etched holes) they are windows. Note: marks can change during processing. For example marks made in the active layer might be islands and turn to windows after LOCOS. Marks made in the shallow trench isolation are neither because of the CMP process. Fortunately alignment looks for the edge of the marks and it does not seem to make much difference if marks are called island or window, either work. Mark edges look dark in bright field illumination.



TILE EXCLUSION LAYER

Add a new layer to the design which will result in areas with no tiles. Just boxes over resolution and overlay targets, lettering and any other regions where you don't want tiles. Then during mask making combine this layer with the active layer after tiling. The result will be no tiles there. If there are structures in these regions, like letters, resolution and overlay structures, they are inserted by boolean combination after tiling.

1. Positive of Active layer is tiled
2. Inverse of Exclusion layer is ANDED with tiled layer
3. Results of 2 is ORED with Positive of Active (ORED with letters, resolution, alignment, etc.)
4. Results of 3 is mirrored, 5X, etc.