ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

VLSI Computer Aided Design (CAD)

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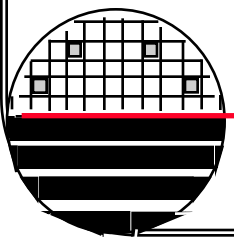
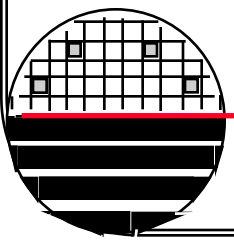


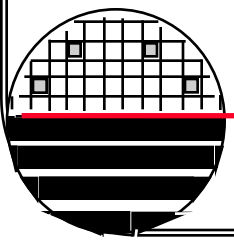
ADOBE PRESENTER

This PowerPoint module has been published using Adobe Presenter. Please click on the Notes tab in the left panel to read the instructors comments for each slide. Manually advance the slide by clicking on the play arrow or pressing the page down key.



OUTLINE

The Design Process
Introduction
Schematic Level Design
Simulation
Technology Selection
Design Rules
Physical Design
References
Homework

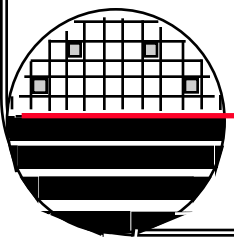


STAGES IN THE DESIGN PROCESS

Problem Specification -> Behavioral Design or Truth Table
Logic Design –> Gate Level Schematic
Circuit Design –> Transistor Level Schematic
Simulation –> Output File

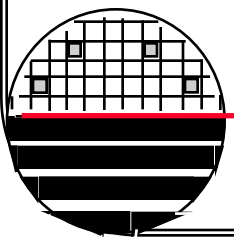
Technology Selection -> Design Rules, Layout Layers
Physical Design -> Layout

Maskmaking – Fabrication – Testing - Packaging



INTRODUCTION

This document is intended to lead the student through a simple digital circuit design with emphasis on the physical design (layout).



EXCLUSIVE OR (XOR) DESIGN EXAMPLE

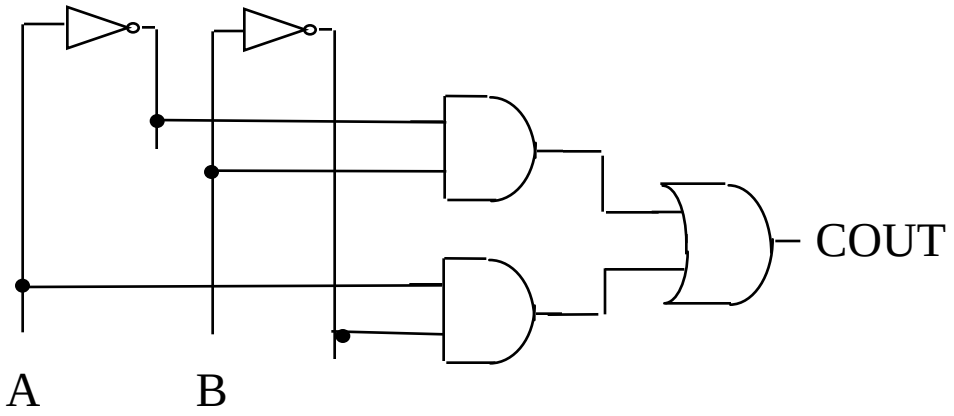
Functional Description – This digital logic circuit returns a true (high) value when one of two inputs is high and returns a false (zero) otherwise.

Exclusive OR
XOR

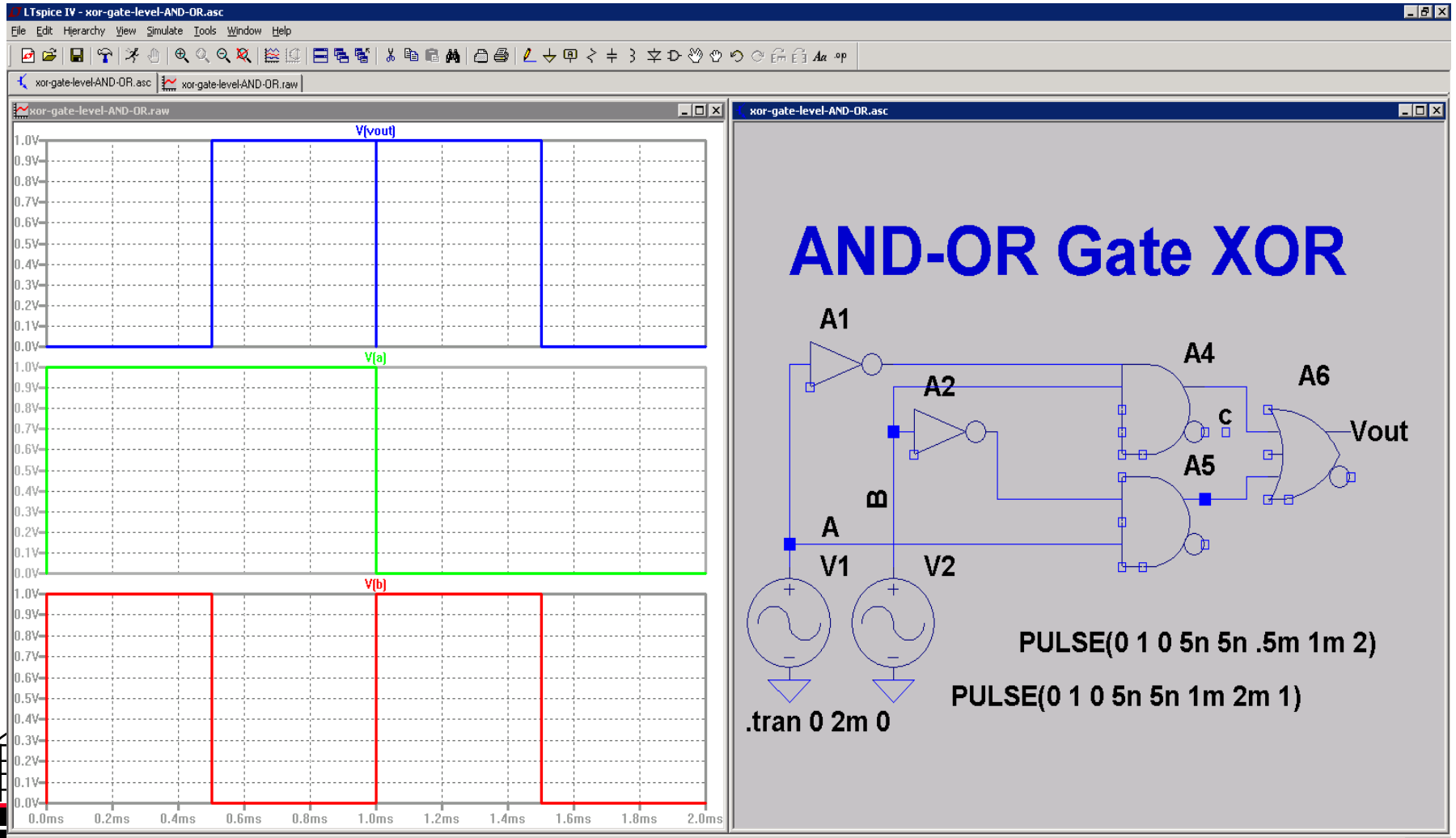
Truth Table

VA	VB	VOUT
0	0	0
0	1	1
1	0	1
1	1	0

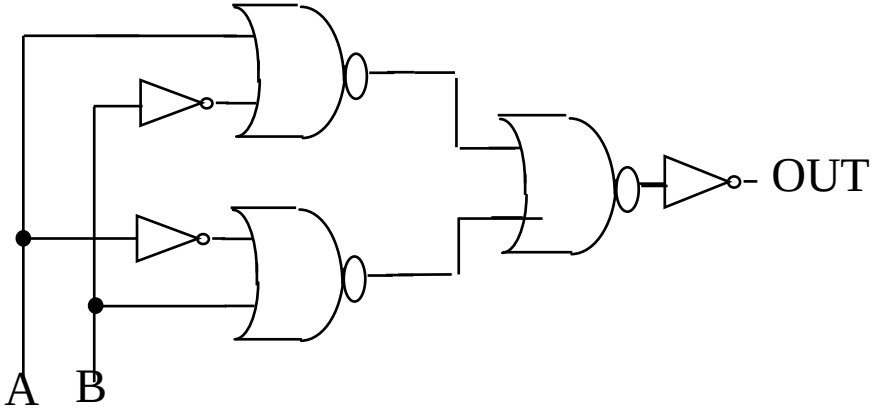
Gate Level Design



GATE LEVEL SIMULATION OF XOR – AND/OR



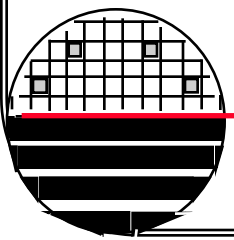
NOR CIRCUIT REALIZATION FOR XOR



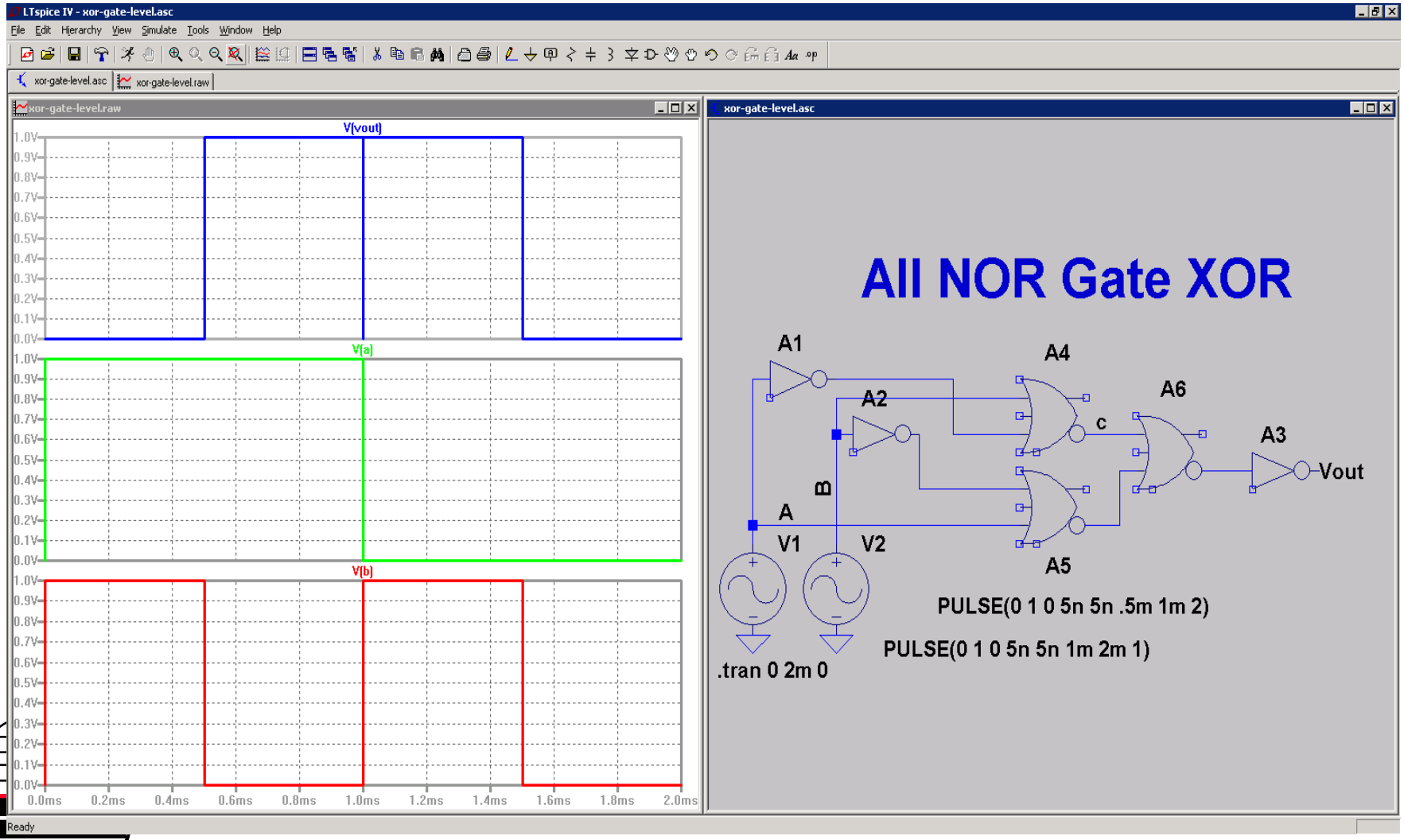
Exclusive OR

XOR

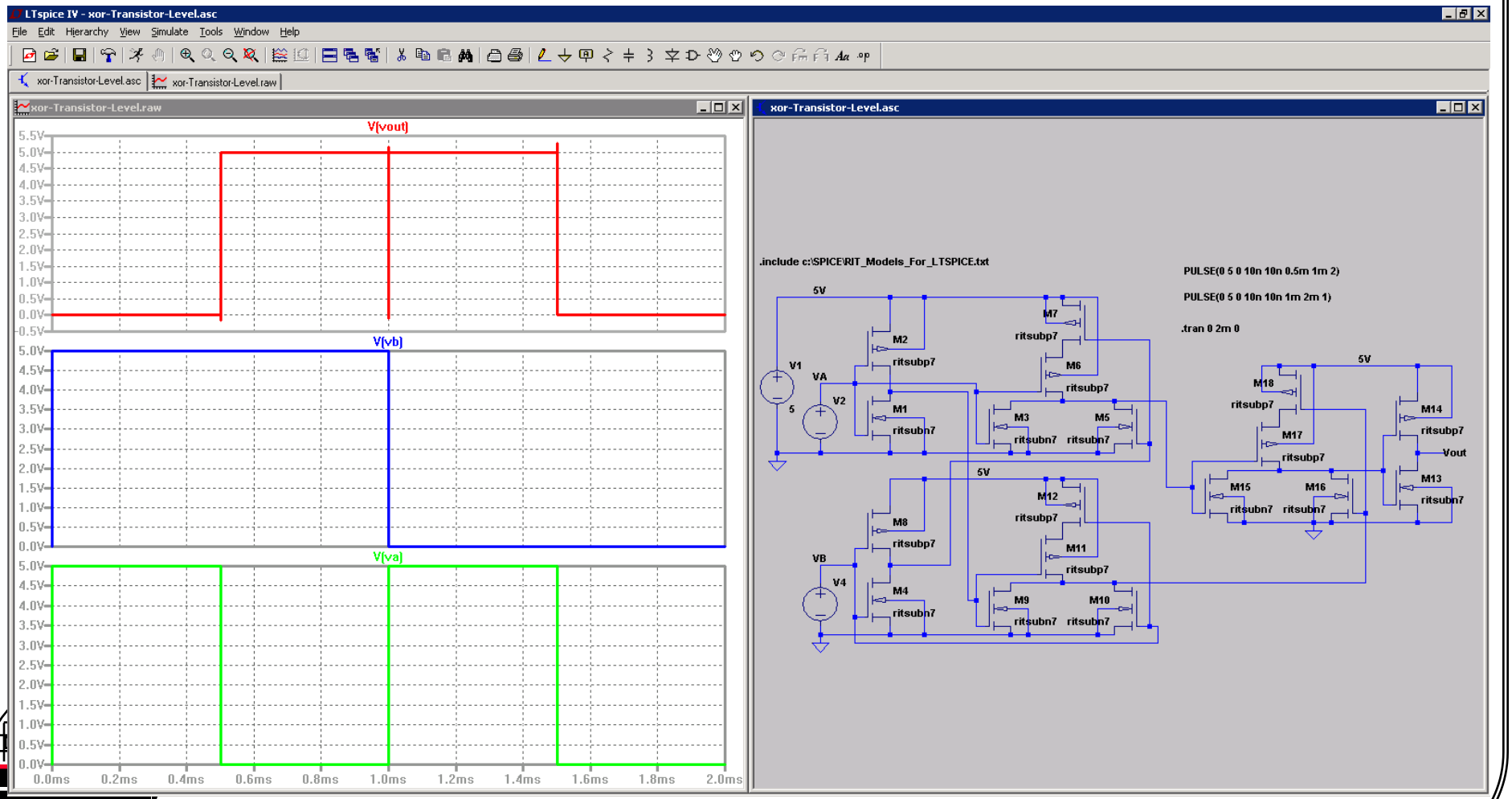
VA	VB	VOUT
0	0	0
0	1	1
1	0	1
1	1	0



GATE LEVEL SIMULATION OF XOR – ALL/NOR



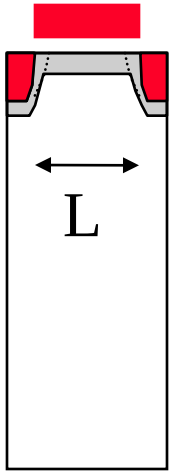
TRANSISTOR LEVEL SIMULATION OF XOR – ALL/NOR



RIT SUBμ CMOS – TECHNOLOGY SELECTION

RIT Subμ CMOS

150 mm wafers
Nsub = 1E15 cm-3
Nn-well = 3E16 cm-3
Xj = 2.5 μm
Np-well = 1E16 cm-3
Xj = 3.0 μm
LOCOS
Field Ox = 6000 Å
Xox = 150 Å
Lmin= 1.0 μm
LDD/Side Wall Spacers
2 Layers Aluminum



Long Channel Behavior

3.3 Volt Technology
VT's = +/- 0.75 Volt
Robust Process (always works)
Fully Characterized (SPICE)

MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

MASK LAYER NAME	MENTOR NAME	GDS #	COMMENT
N WELL	N_well.i	42	
ACTIVE	Active.i	43	
POLY	Poly.i	46	
N PLUS	N_plus_select.i	45	
P PLUS	P_plus_select.i	44	
CONTACT	Contact.i	25	Active_contact.i 48 poly_contact.i 47
METAL1	Metal1.i	49	
VIA	Via.i	50	
METAL2	Metal2.i	51	
VIA2	Via2.i	61	Under Bump Metal
METAL3	Metal3.i	62	Solder Bump

These are the main design layers up through metal two

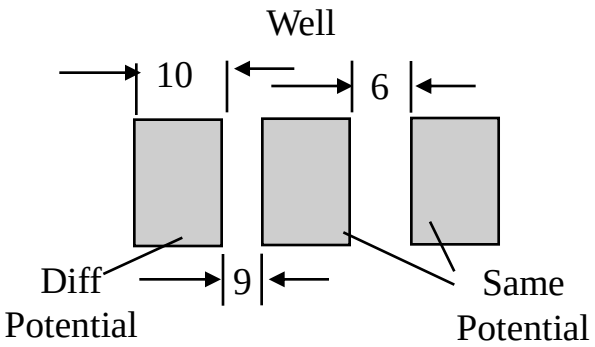
MORE LAYERS USED IN MASK MAKING

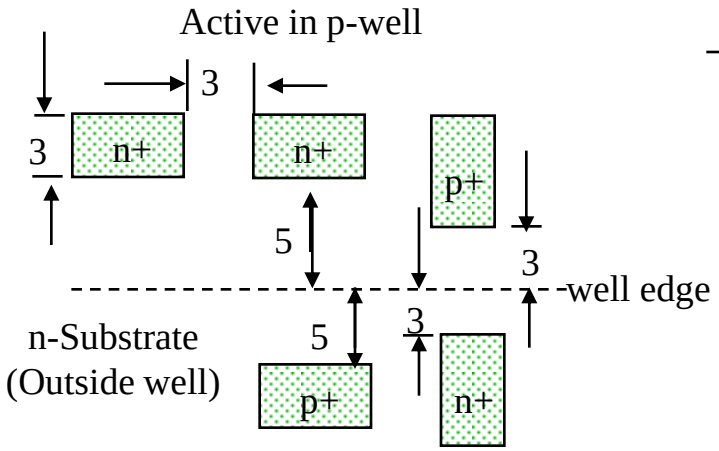
LAYER	NAME	GDS	COMMENT
	cell_outline.i	70	Not used
	alignment	81	Placed on first level mask
	nw_res	82	Placed on nwell level mask
	active_lettering	83	Placed on active mask
	channel_stop	84	Overlay/Resolution for Stop Mask
	pmos_vt	85	Overlay/Resolution for Vt Mask
	LDD	86	Overlay/Resolution for LDD Masks
	p plus	87	Overlay/Resolution for P+ Mask
	n plus	88	Overlay/Resolution for N+ Mask
	tile_exclusion	89	Areas for no STI tiling

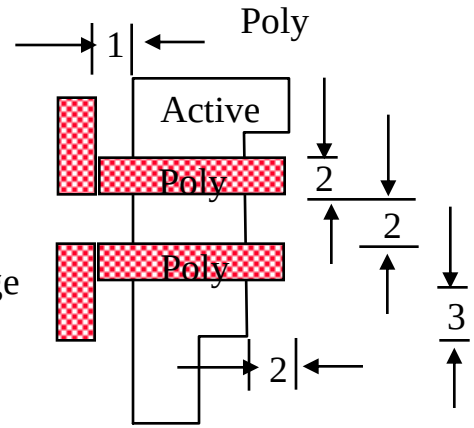
These are the additional layers used in layout and mask making

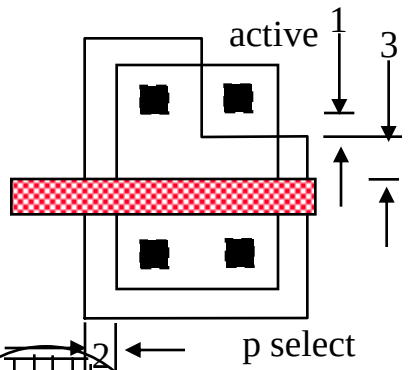
MOSIS LAMBDA BASED DESIGN RULES

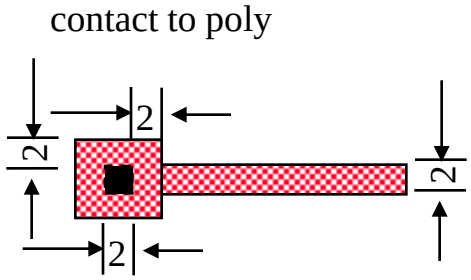
http://www.mosis.com/design/rules/

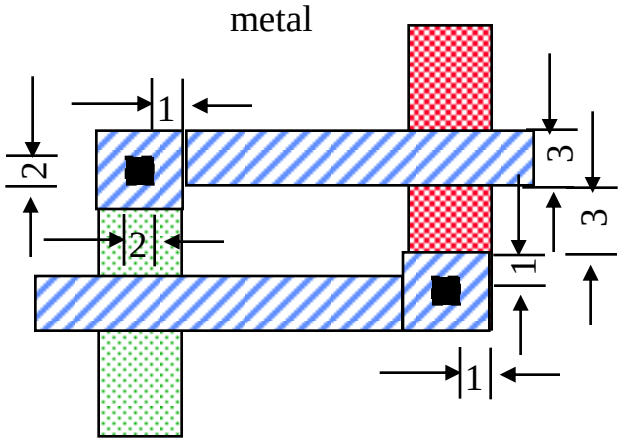




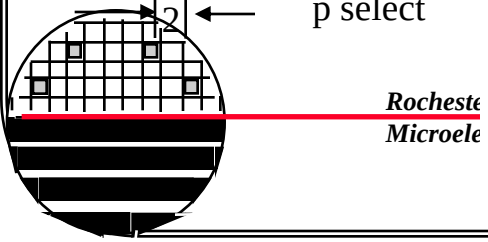






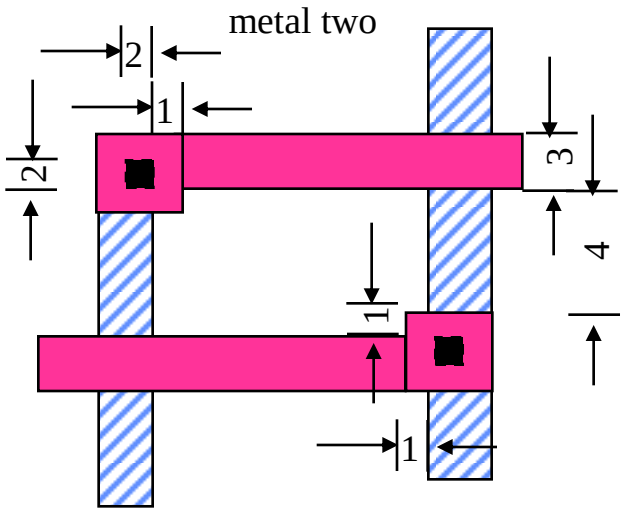


If λ = 1 µm then contact is
2 µm x 2 µm



MOSIS LAMBDA BASED DESIGN RULES

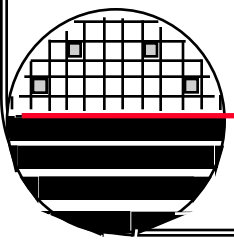
http://www.mosis.com/design/rules/



MOSIS Educational Program

Instructional Processes Include:
AMI $\lambda = 0.8$ µm SCMOS Rules
AMI $\lambda = 0.35$ µm SCMOS Rules

Research Processes:
go down to poly length of 65nm



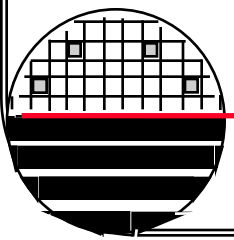
GETTING STARTED WITH LAYOUT EDITOR IC

Usually the workstation screen will be blank, move the mouse to view a login window.

Login: **username**
Password: ********

The screen background will change and your desktop will appear. On the top of the screen click on **Applications** then **System Tools** then **Terminal**. A window will appear that has a Unix prompt inside. Type the command **ls** at the prompt to see a list of directories and files, the account should be empty.

Type **ic <ENTER>,** it will take a few seconds, then maximize the IC Station window by clicking the left mouse button on the large square in the upper right corner of the IC Station window.



SHARED FOLDERS

We have set up a shared folder for this course that has primitive cells which you can open and copy from for your designs.

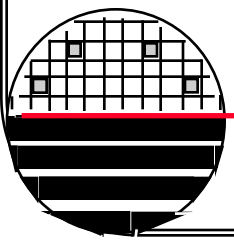
/shared/mcee550/

Students and faculty for this course have their own personal accounts where they can keep their designs.

/home/username/filename/

All users have access to some public folders that have files for processes, design rules, etc.

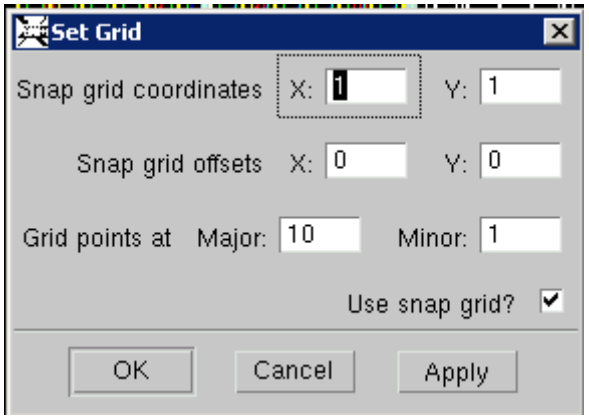
/tools/ritpub/process/fuller

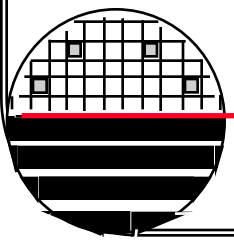


STARTING A STANDARD CELL DESIGN

On the right hand panel of the IC Station window click on **Create** to open the create Cell window. Fill in a cell name that includes your initials (so I can identify your cells from other students cells). For process browse to or type **/tools/ritpub/process/fuller** . This will select the correct level names, level numbers and colors for the TSMC 0.35 2P3M process as discussed above. The workspace should change to a black screen with dots. If you move the cursor around you can find different xy cursor locations as displayed at the top-center.

On top banner select **Other>Window>Set Grid**



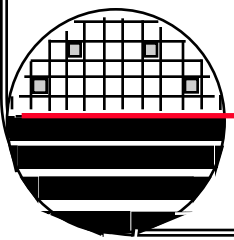


STARTING A STANDARD CELL DESIGN

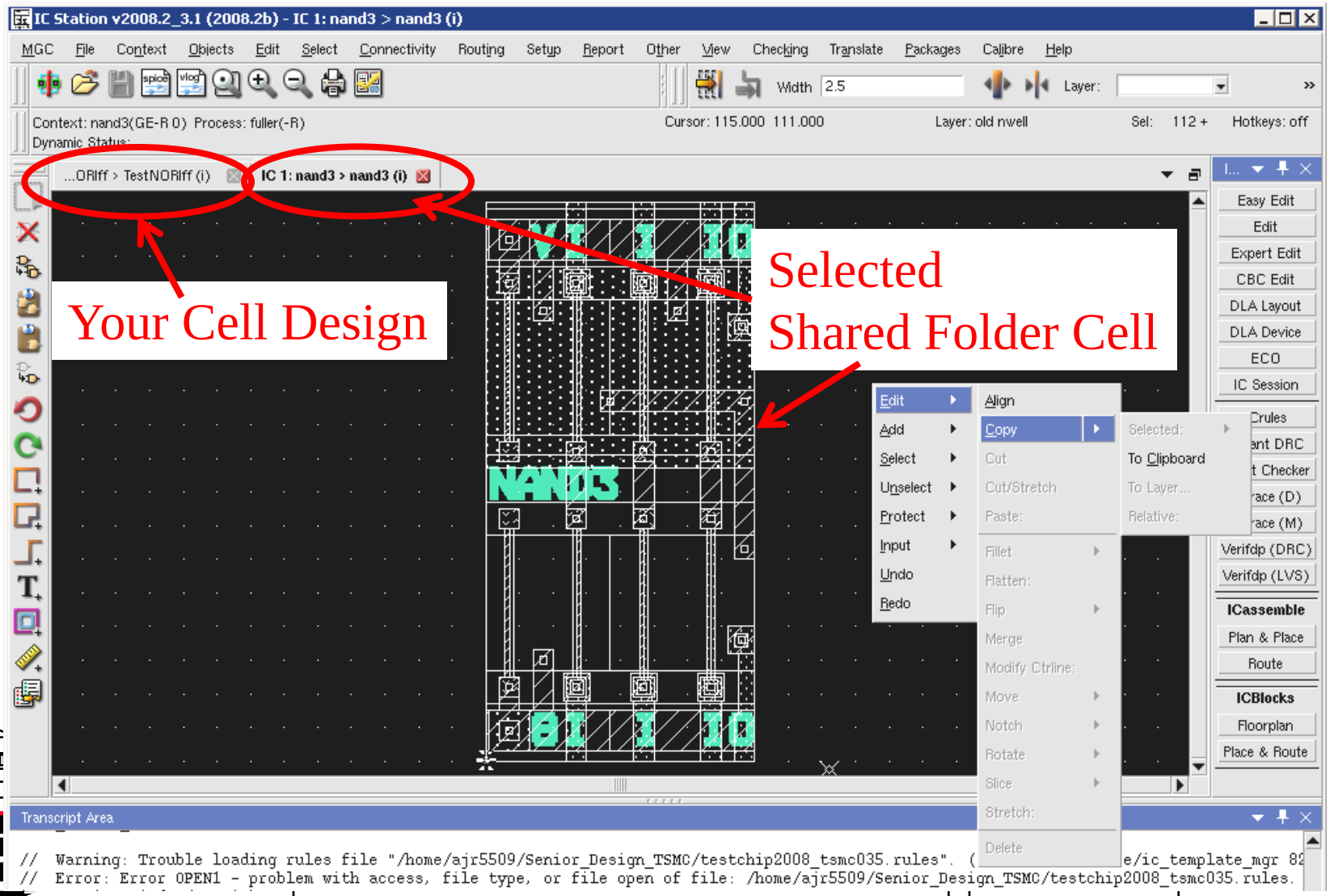
Open a cell from the shared folder by clicking on the open cell icon in the top-left banner. Navigate to **/shared/mcee550/** and select the cell you want in your design. Press **Shift+F8** to scale the window to fit the cell. Drag a box around the cell to select it and right click to **Edit>Copy>ToClipboard**

Then return to your cell and right click and **Edit>Paste**. Place the lower left corner where you want the cell. **Shift+F8** will scale the window to fit the cell. **F2** will unselect cell.

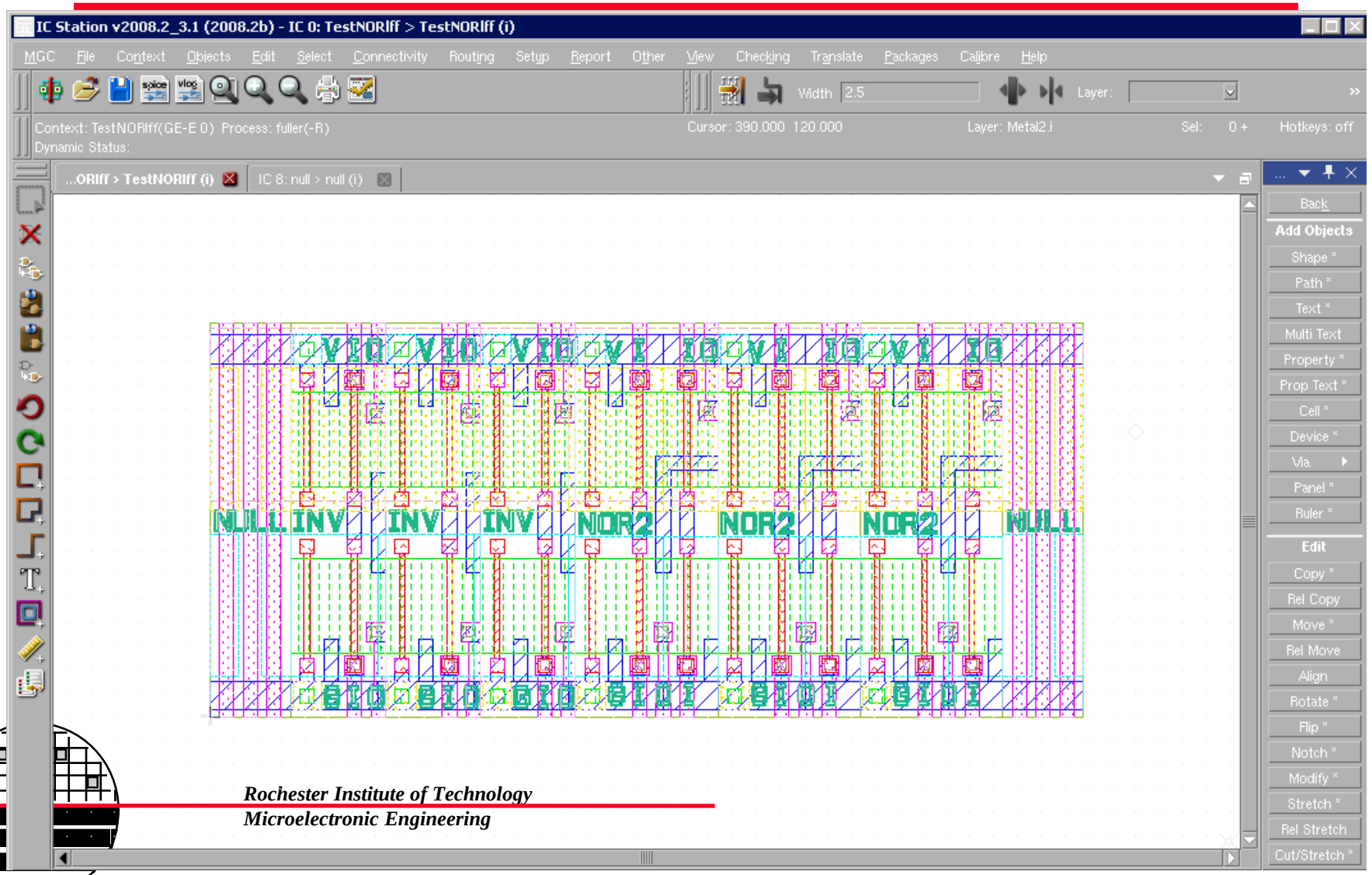
If you use the add cell approach to build your design you can place a cell from **/shared/mcee500** folder in your design. To see the details inside the cell type anywhere in the workspace **Peek** then **OK**.



COPYING CELL FROM SHARED FOLDER



PASTING PRIMITIVE CELLS INTO YOUR CELL DESIGN



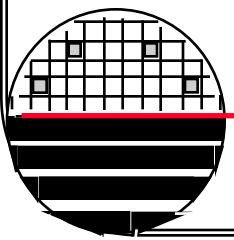
INTERCONNECTING PRIMITIVE CELLS

The primitive cells are interconnected using Metal-1 and Metal-2 in the routing channels above and below the primitive cells. First place horizontal metal lines in the routing channels by creating a shape with the following command (type anywhere in the drawing window)

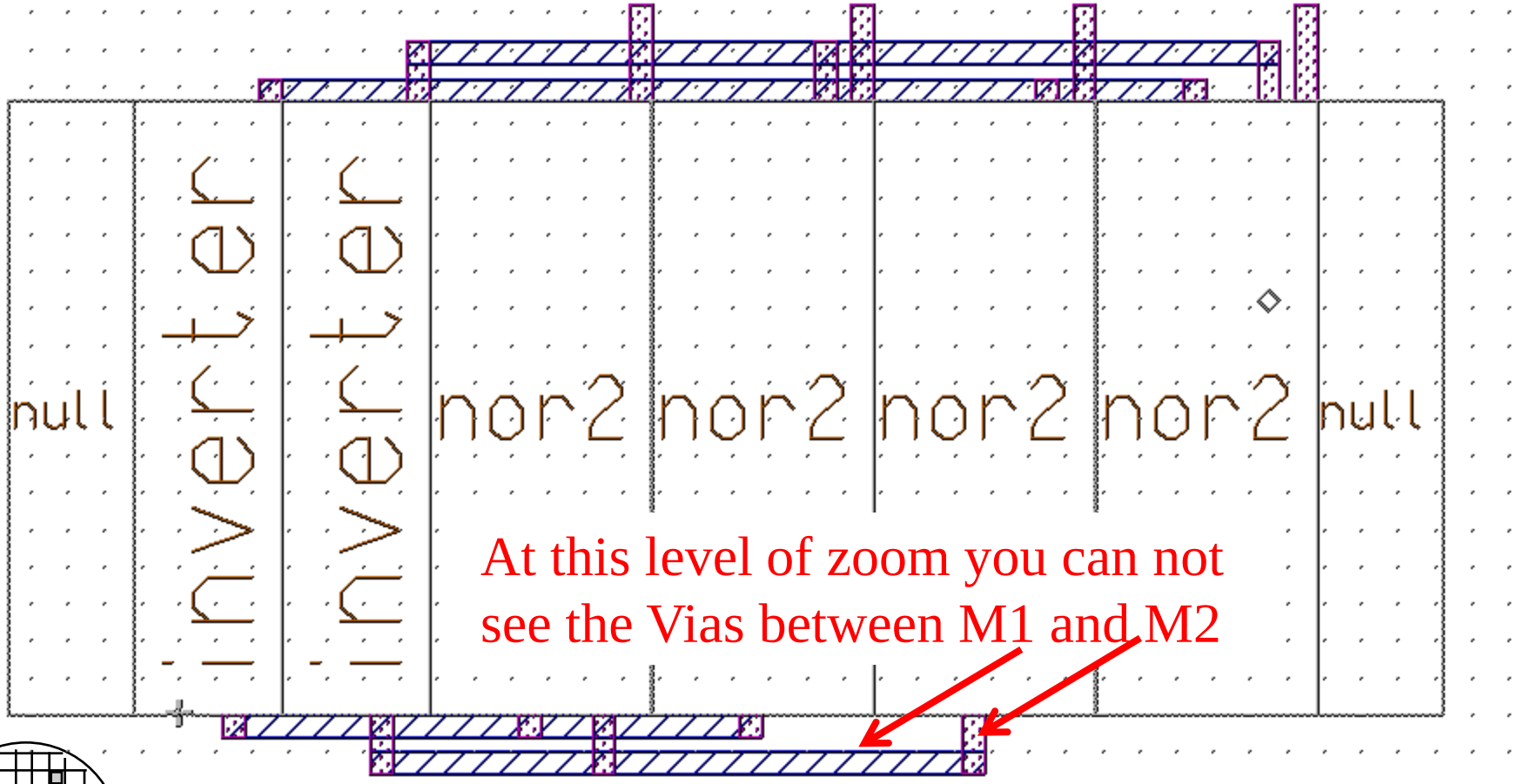
$add_shape([[0,166],[368,172]],49)

This will draw a box with lower left corner at x=0, y=166 and upper right corner at x=368um, y=172um, with layer number 49 (metal-1). This should be a horizontal metal-1 interconnect line at the top of your cell if you placed the lower left corner of your cell at (0,0)

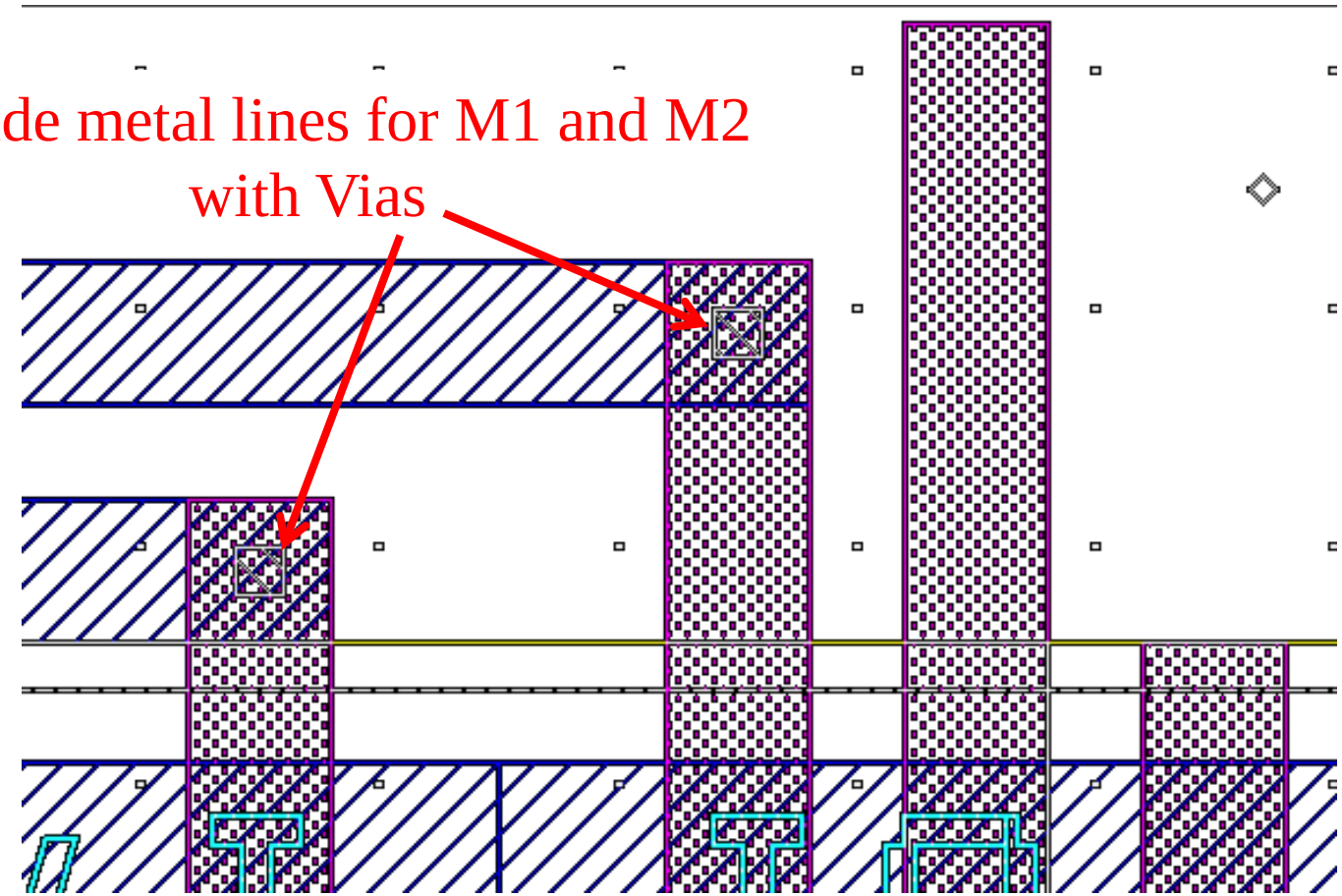
Both M1 and M2 will need some type of contact cut or Via. See next page for examples



M1 AND M2 INTERCONNECTS



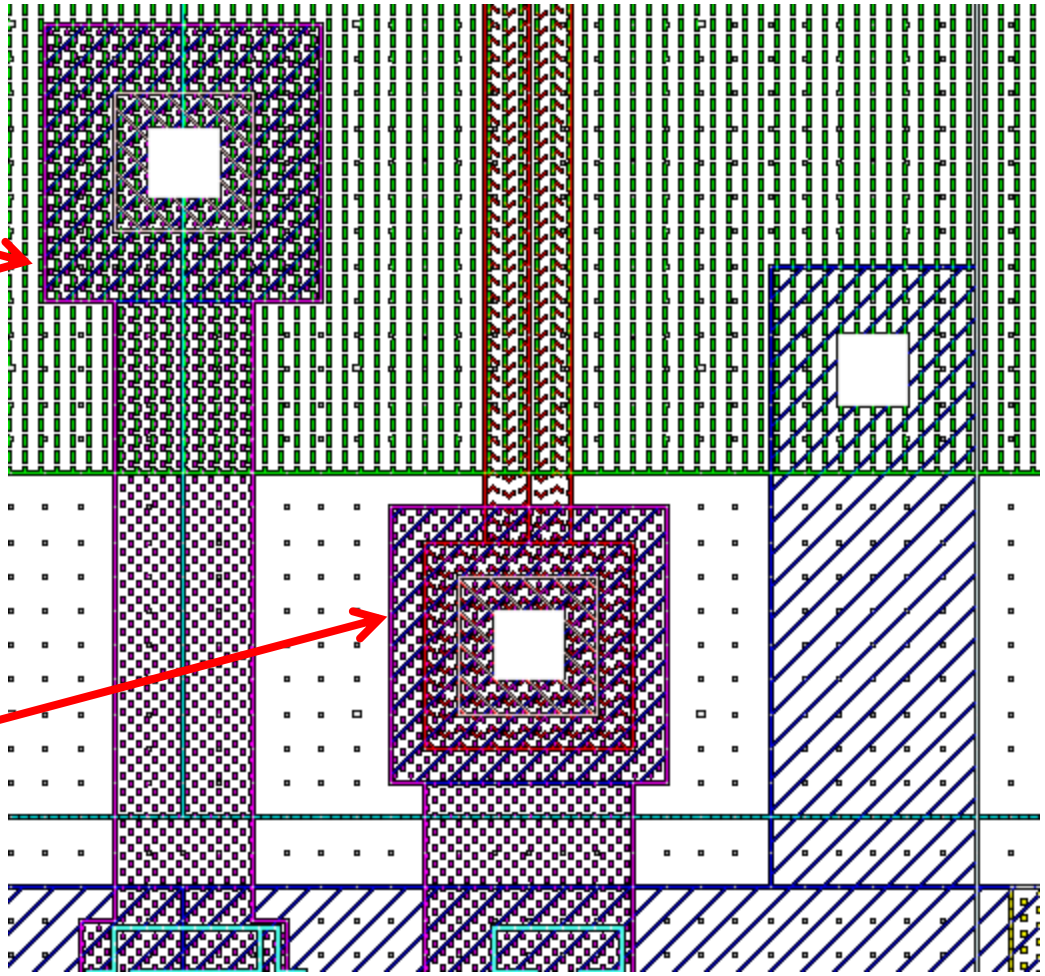
CONNECTIONS BETWEEN M1 AND M2



CONNECTIONS TO ACTIVE AND POLY

Metal-2 to Via to Metal-1 to CC to Active

Metal-2 to Via to Metal-1 to CC to Poly



USING THE VLSI LAB WORKSTATIONS AND MENTOR GRAPHICS CAD TOOLS

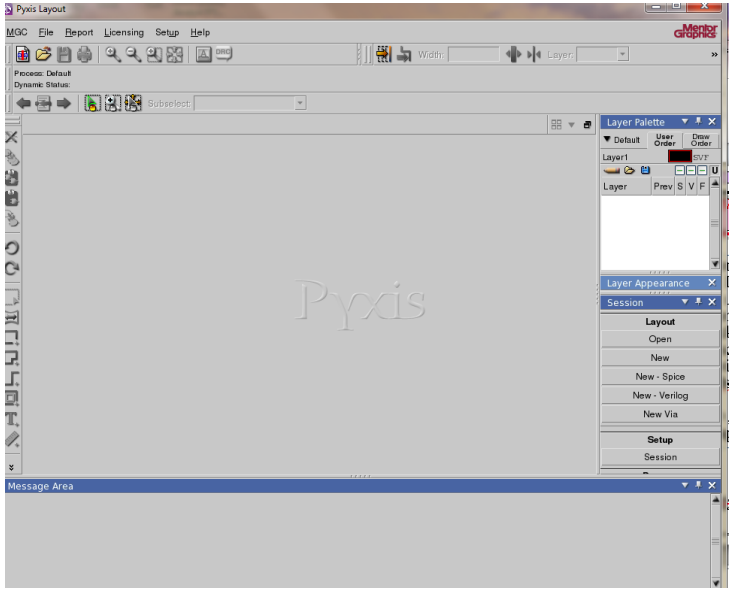
Usually the workstation screen will be blank, press any key to view a login window. Login or switch user and then login.

Login: username (RIT computer account)

Password: ********

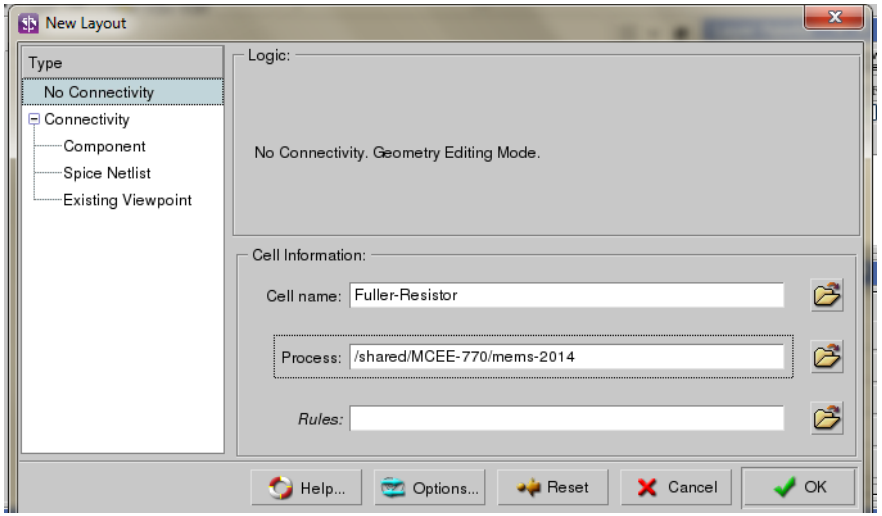
The screen background will change and your desktop will appear. On the top of the screen click on **Applications** then **System Tools** then **Terminal**. A window will appear that has a Unix prompt inside. Type the command **ls** at the prompt to see a list of your directories and files.

Type **ic** <RET>, it will take a few seconds, then the Pyxis Layout user interface will appear. Maximize the Pyxis Layout window.



USING THE HP WORKSTATIONS AND MENTOR GRAPHICS CAD TOOLS - PROCESS AND GRID

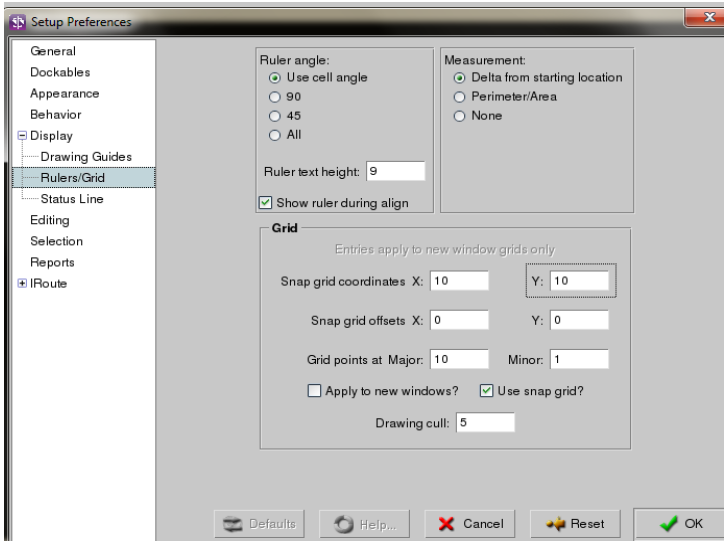
In the session menu palette on the right hand side of the screen, under Layout, select **New**, using the left mouse button. For cell name type **name-device**. Set the process by typing **/tools/ritpub/process/mems-2014** in the process field. Leave the Rules field blank. Click **OK**



At the top left of the window check that the process is **mems-2014** not Default. If not correct go to top banner click on **Context>Process>Set Process**

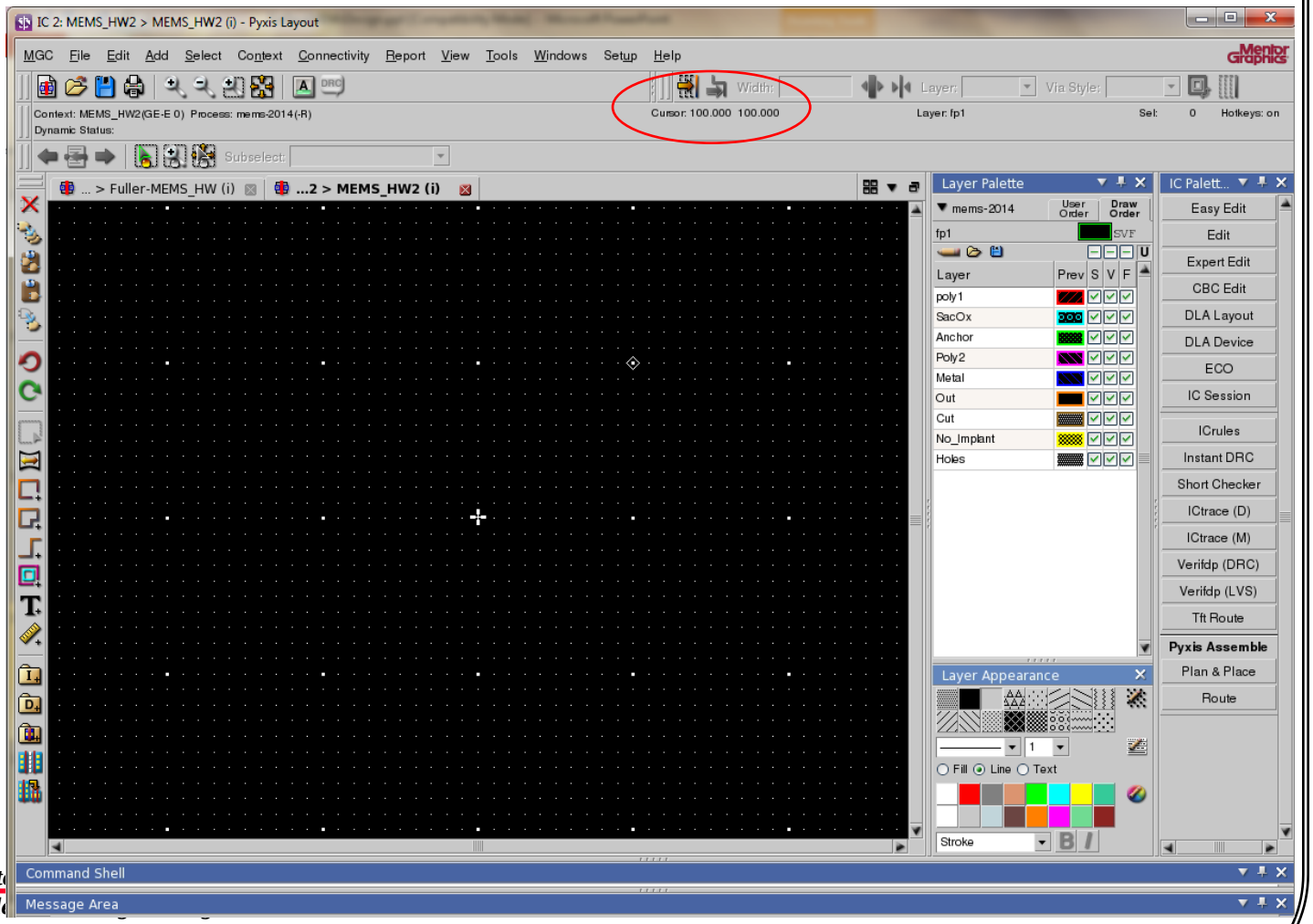
The Layer Palette should show the layers you expect to used for your device layout.

On top banner select **Setup>Preferences>Display>Rulers/Grid** Set Snap to **10** and **10** as shown. (or other values as necessary)



USING THE HP WORKSTATIONS AND MENTOR GRAPHICS CAD TOOLS – WORKSPACE, LOCATION

The plus mark + is (0,0) the small dots are the 10 um grid the large dots are the 100um grid. The mouse curser is shown by the diamond and is at (100um,100um) as indicated by the cursor position at the top of the workspace.

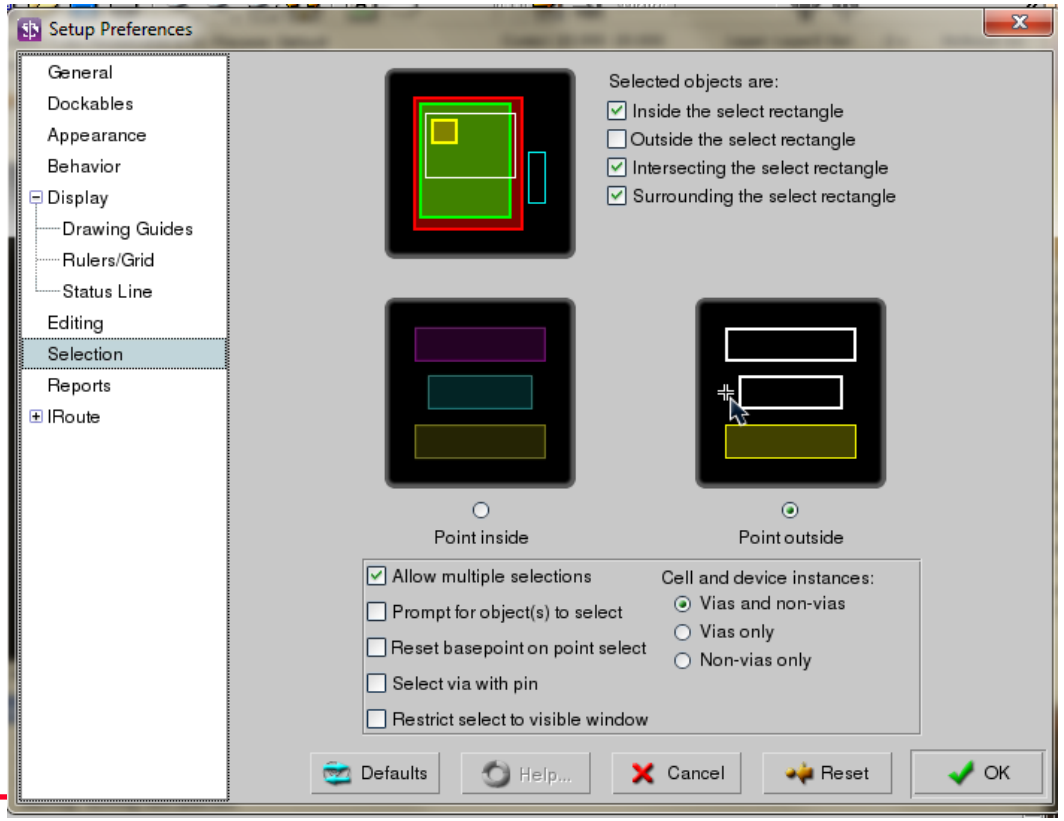


USING THE HP WORKSTATIONS AND MENTOR GRAPHICS CAD TOOLS – SELECTING OBJECTS

Select easy edit, Select Shape. Draw boxes by click and drag of mouse. Unselect by pressing **F2** function key. The highlighted layer in the layer palette is selected prior to drawing. Unselect by pressing **F2**. Exit drawing by pressing **ESC**.

Selecting multiple objects is defined in **Setup>Selection**

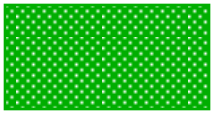
Unclick **Surrounding the select rectangle** to not select the cell outline



DRAWING BOXES AND OTHER SHAPES

Select easy edit, right click and select Show Scroll Bars, scroll through the various edit commands.

DRAW BOXES by click and drag of mouse. Unselect by pressing F2 function key. The following command will draw a 3000 µm by 3000 µm box with layer 4 color/shading. Put the curser in the workspace and start typing. A text line window will pop up. If the command has a typo just start typing again and use the up arrow to recall previous text.



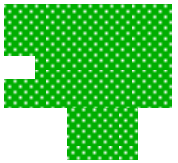
$add_shape([[0,0],[3000,3000]],4)

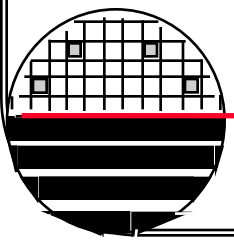
Location of lower left corner

Location of upper right corner

Box Color

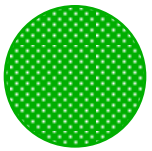
The Notch command is useful to change the size of a selected box or alter rectangular shapes into more complex shapes.



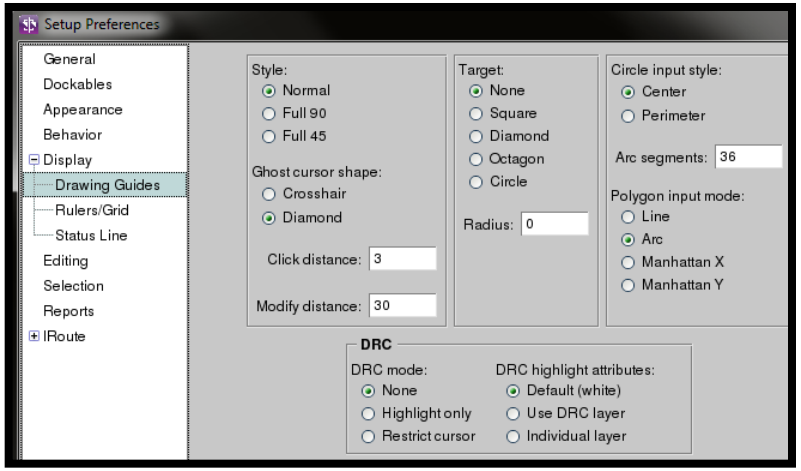


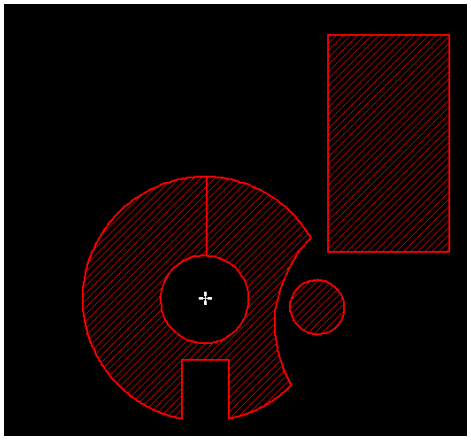
DRAWING CIRCLES

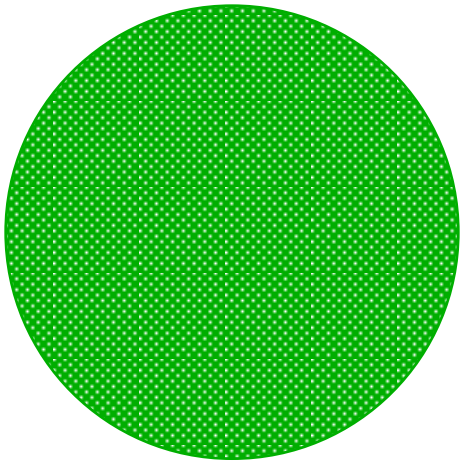
DRAW CIRCLES by typing **$set_location_mode(@arc)** return. The following command will draw a 100µm radius circle centered at (0,0) using 300 straight line segments.
$add_shape($get_circle([0,0],[100,0],300),3)
To reset to rectangles type $set_location_mode(@line) return.



MOVE, COPY, DELETE, NOTCH, etc: Selected objects will appear to have a bright outline. Selected objects can be moved (**Move**), copied (**Copy**), deleted (**Del**), notched (**Notc**). When done **unselect** objects, press F2.







Change an Object to another layer: Selected object(s) click on **Edit** on the top banner, select **Change Attributes**, change **layer name** to the name you want. When done press **F2** to unselect

USING THE HP WORKSTATIONS AND MENTOR GRAPHICS CAD TOOLS - OTHER

ZOOM IN OUT: pressing the + or - sign on right key pad will zoom in or out. Also pressing **shift + F8** will zoom so that all objects are in the view area. Select **View** then **Area** and click and drag a rectangle will zoom so that the objects in the rectangle are in the view area.

MOVING VIEW CENTER: pressing the middle mouse button will center the view around the pointer.\

ADDING TEXT: Add > Polygon Text click on layout where you want it located. Select the text box and **Edit > Change > Attributes**, change pgtext, change scale to 3.0

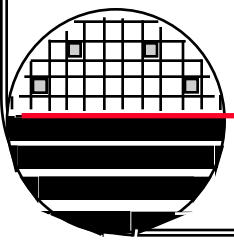
SCREEN PRINT: Click on **MGC** and select **Capture Screen.** Enter file name and location such as **Lynn.png** and **Desktop.** After saving you can use a flash drive and transfer the file to another computer.

LOG OUT: upper right of screen click on name and select **LOG OUT**

BASIC UNIX COMMANDS

Command	Description
ls	list the files and directories in the current directory
cd	change directory
cd ..	go up one directory
mv	move a file (rename a file)
rm	remove a file (delete a file)
pwd	display path of current directory
mkdir	create a new directory
rmdir	remove a directory
yppasswd	change your password

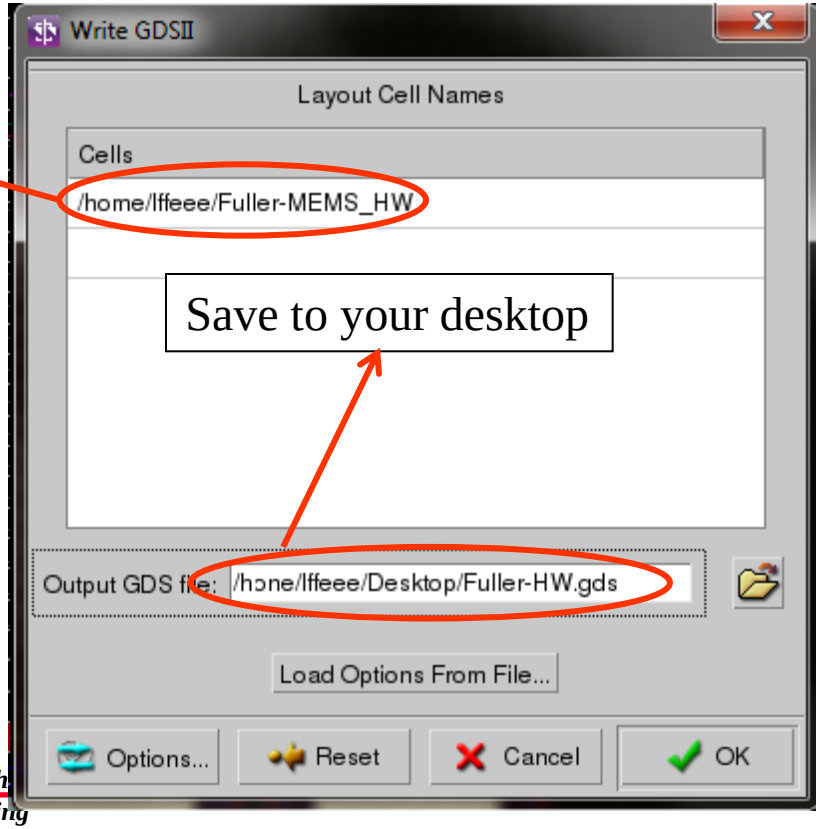
It is important to remember that since this is a UNIX operating system, the commands are case sensitive.



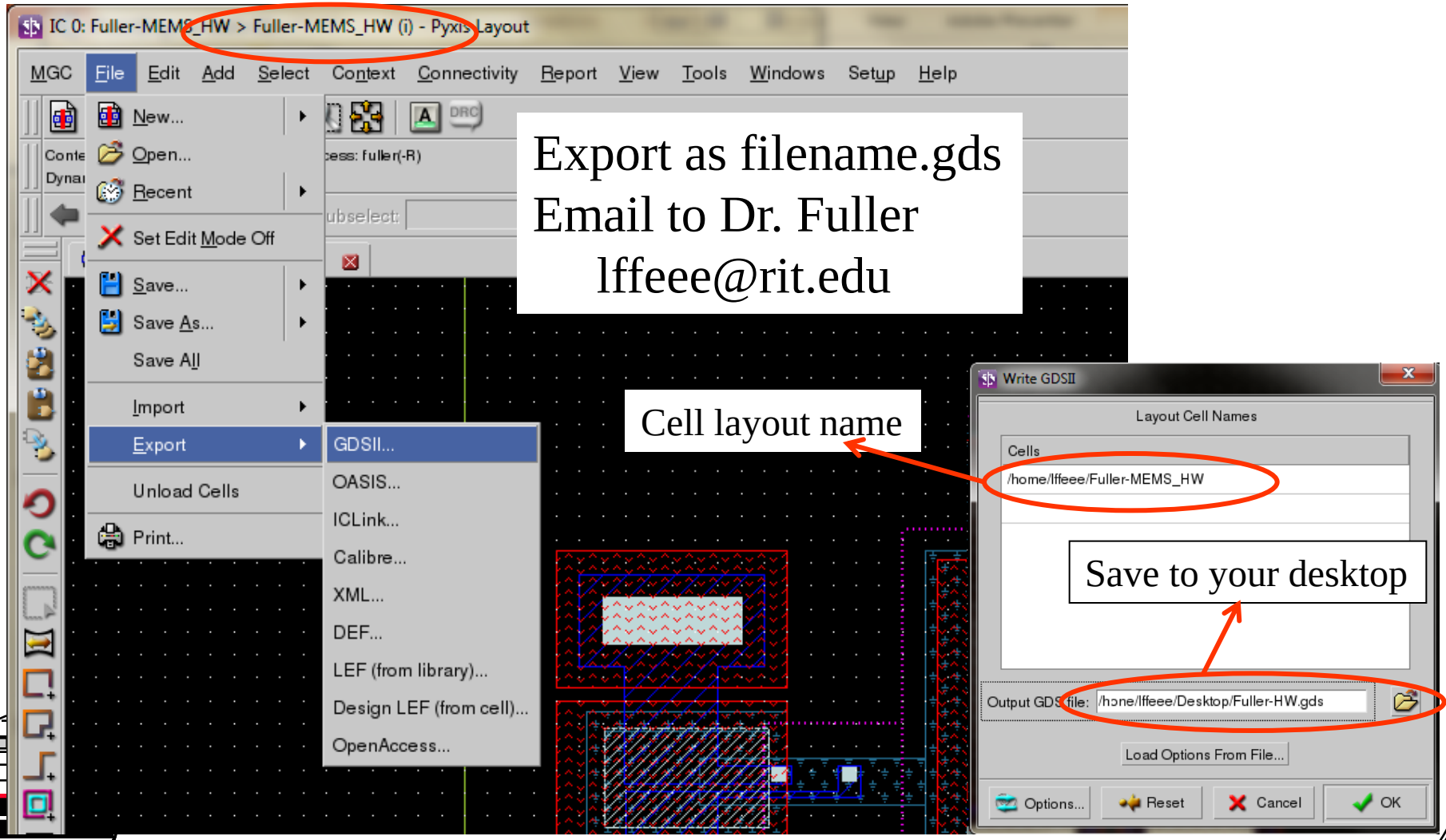
GDS FILE GENERATION

Once the cell design is completed export the GDS file for maskmaking. Select **Translate** on the top banner and then **Write GDSII** Output file needs full path name and .gds extension.

Cell layout name



EXPORT CELL DESIGN AS GDS II FILE



MASK ORDER FORM

Rochester Institute of Technology
Semiconductor & Microsystems Fabrication Laboratory

Maskmaking
Order Request

Name
Company
Department
Street Address
City, State and Zip Code
Phone Number
SMFL Project Code
Email Address

Order Date
Order Due Date

Dr Fuller
RIT

Design File Name (.gds)	**mems-2014-final.gds**
Number of Mask Levels to be Written	**7**
Cell Layout Size	**16.5mm x 16.5mm**
Name of Cell in Design File to be used	**mems-2014-final**

Mask Type Needed

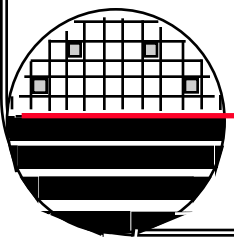
☐ Contact Aligner	Defaults	Scale:	1X
• Max field size – 105mm x 105mm		Mask Size:	5" x 5" x 0.09" Soda Lime
		Orientation:	Mirror 90
		Fracture Resolution:	0.5um
☐ GCA Stepper	Defaults	Scale:	5X
• Max field size – 20mm x 20mm		Mask Size:	5" x 5" x 0.09" Soda Lime
		Orientation:	Mirror 135
		Fracture Resolution:	0.5um
X ASML Stepper	Defaults	Scale:	5X
Max field size – 22mm x 22mm		Mask Size:	6" x 6" x 0.12" Quartz
		Orientation:	Mirror 90
		Fracture Resolution:	0.5um

Single Field Array Plate	☐ Yes
	☐ Array with ___ columns (x) and ___ rows (y)
Array element size	X: ___ um Y: ___ um

Notes:
If multiple design files are to be incorporated into your array – please specify the array layout separately
Your designs will be butted together to from the array unless otherwise specified

Multiple Field Array Plate	☐ Yes
Numbers of Levels on Plate	

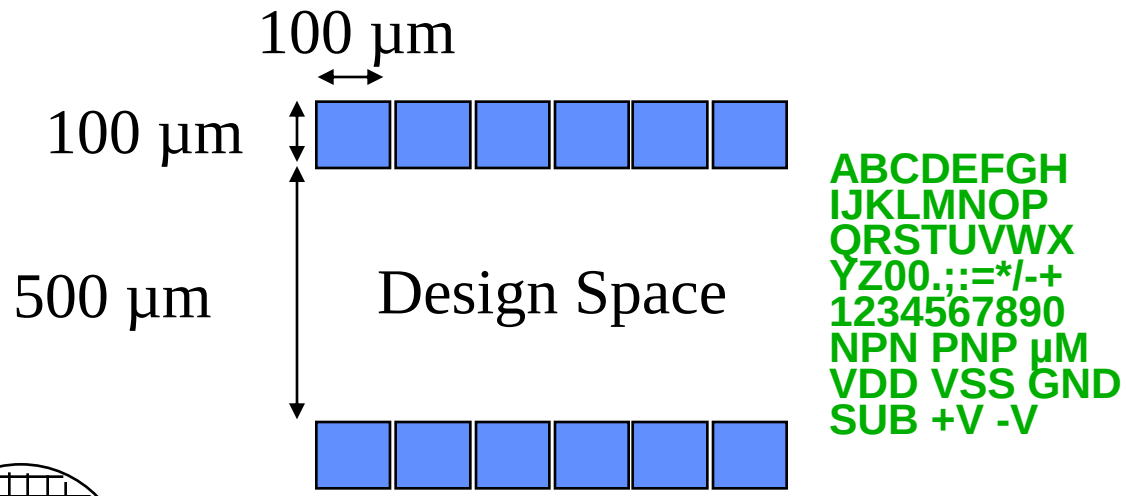
Please specify which levels are to be grouped together on which plate on the Details Sheet



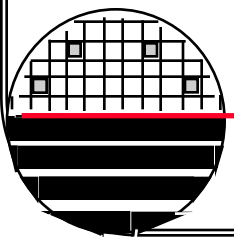
Rochester Institute of Te
Microelectronic Enginee

ADDING PAD CELL AND LETTERS

From the banner at the top of the page choose **Objects>add>cell**. A tan pop-up window will appear at the bottom of the page. Type in the following cell name, all lower case, **/tools/ritpub/padframes/ritpmos/ritpmos_12_pads** and click the left mouse button on the location button. Then position the cursor at the origin 0,0 and click the left mouse button. Click the left mouse button on the cancel button on the tan pop-up box. Press SHIFT and F8 to View All. You should see a white box with ritpmos_12_pads written inside it. Type flatten and select, OK. Press F2 to unselect all.



MEBES - Manufacturing Electron Beam Exposure System



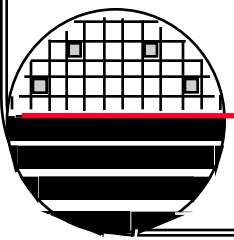
Maskmaking Tool

FILE FORMATS

Mentor- ICGraph files (filename.iccel), all layers, polygons with up to 200 vertices

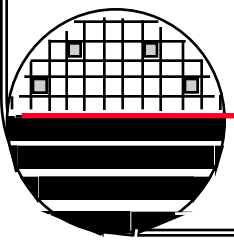
GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only



REFERENCES

1. Principles of CMOS VLSI Design, 2nd Ed., Neil H.E.Weste, Kmran Eshraghian, Addison Wesley, 1993.
2. Physical Design Automation of VLSI Systems, Bryan Preas, Michael Lorenzeti, Benjamin/Cummings, 1988.
3. VLSI Engineering, Thomas Dillinger, Prentice Hall, 1988.

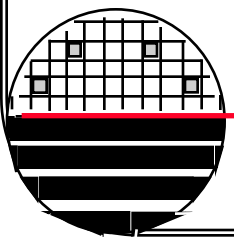


HOMEWORK VLSI-CAD

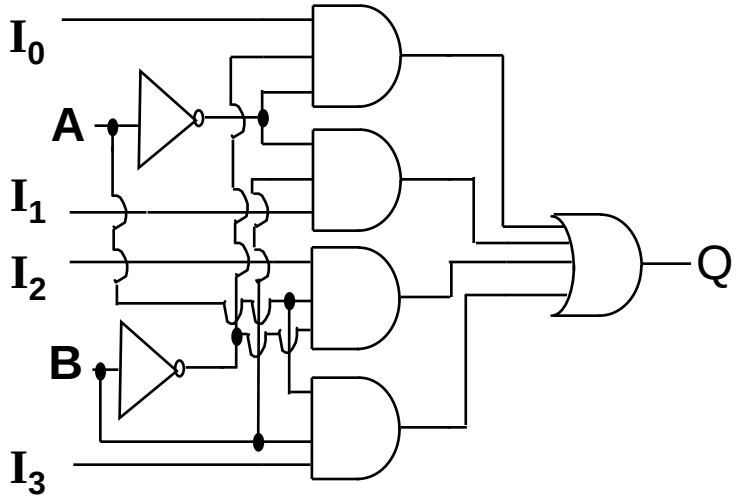
This assignment can be done using the tools in the VLSI lab. Ideally the switch level simulation and SPICE simulations are also done with the tools in the VLSI Lab.

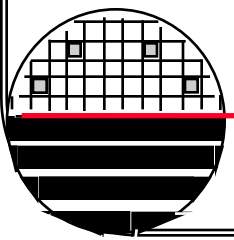
Design a 4 to 1 multiplexer. Two inputs (Input A and Input B) select which one of four other digital inputs (I1 I2 I3 I4) is output (Vout)

Document the following items, Truth Table, Gate Level Schematic, Gate Level Simulation, Transistor Level Schematic, Transistor Level Simulation, Layout using Gate Array, Including connections to 12-pad Pad Frame.

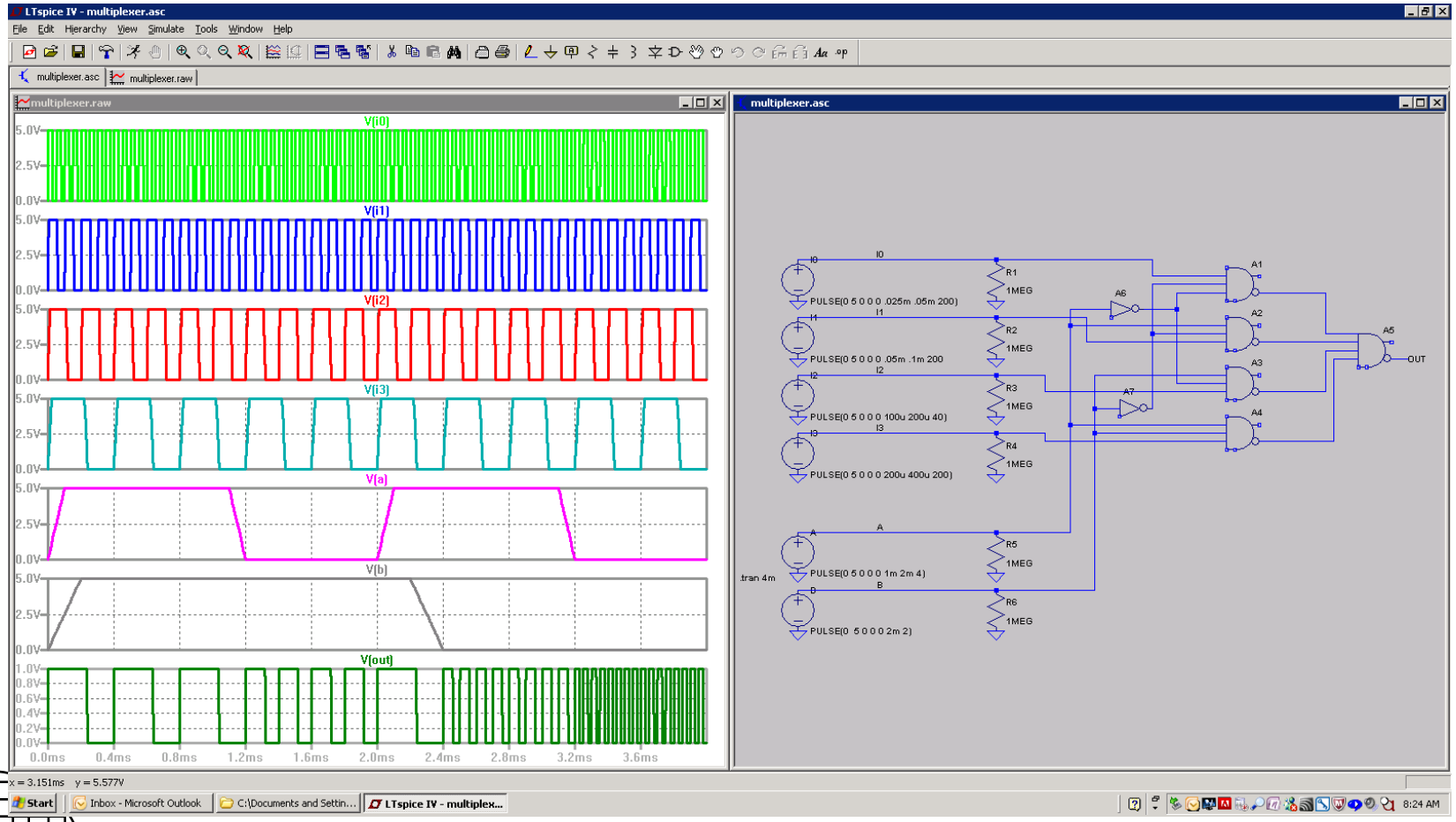


4 TO 1 MULTIPLEXER

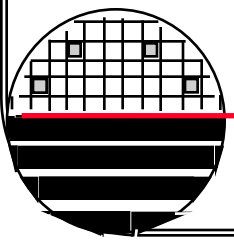




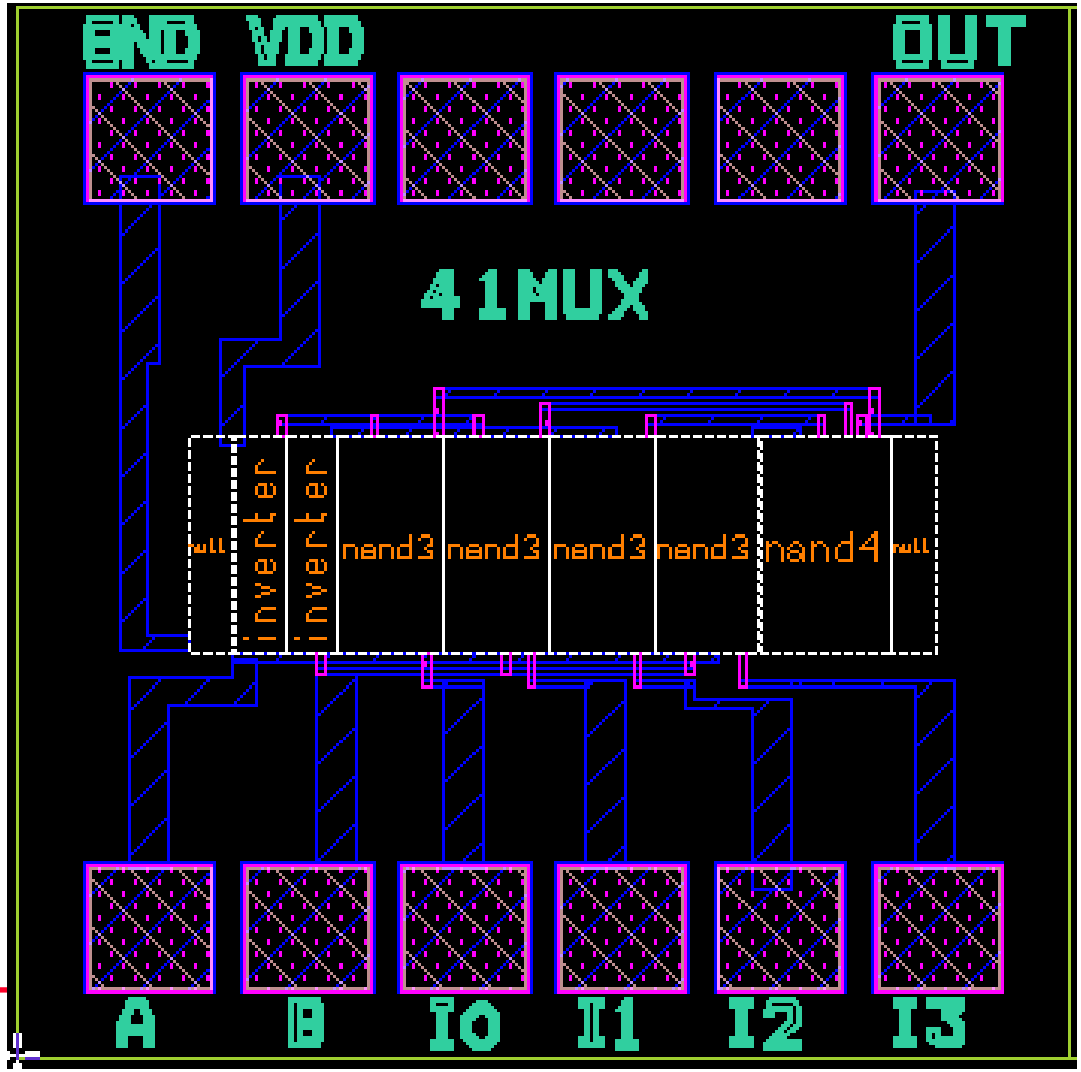
4 TO 1 MUX - GATE LEVEL SIMULATION



4 TO 1 MUX – TRANSISTOR LEVEL SIMULATION



4 TO 1 MUX – LAYOUT



4 TO 1 MUX – PEEKED AND ZOOM