*ROCHESTER INSTITUTE OF TECHNOLOGY*
*MICROELECTRONIC ENGINEERING*

# Introduction to Cycle Time Management Part 1

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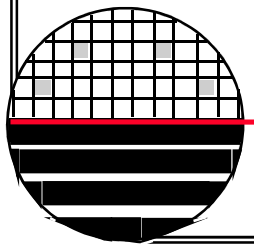
Acknowledgements: Motorola's Cycle Time Reduction Team, Jack Scholl, Michael Mandracchia, Jerry Walton, Jerry Chruma, Virgil Howarth, Gene Mullinnix, Michael Wolfe, Tom Filesi, et.al.





# *OUTLINE*

**Introduction: Why Cycle Time Reduction is Desirable**

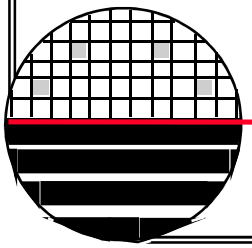
**Assessment**

**Develop a Cycle Time Reduction Plan**

**Macro Planning**

**Low Inventory Management**

- **Establish a Short cycle Time Culture**
- **Micro Planning**
- **Fine Tuning**



# *INTRODUCTION*

**What are the advantages of reduced cycle time?**

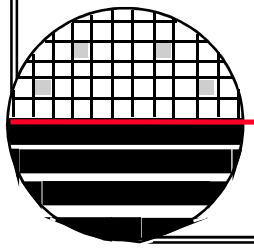
**1. More responsive to changing customer demands. Especially important in ASIC (Application Specific Integrated Circuit) manufacturing.**

**2. Quicker time to market with new products.**

**3. Save money by reducing WIP (Work in progress)**

**4. Increase yield**

**5. Quicker feedback for process development and process capability improvement programs. (Cpk will improve faster)**



# *INTRODUCTION*

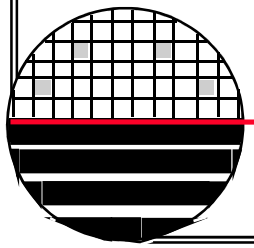
**What are the advantages of reduced cycle time? (Cont.)**

**6. Additional savings through incremental improvements:**

**6.1 Improved employee productivity, which means savings if less employees are needed or increased factory output if consistent with factory goals.**

**6.2 Improved equipment utilization by being smarter about maintenance, set ups, production tests, balance, etc.**

**6.3 Reduced non productive tests and process control measurements.**



# *INTRODUCTION*

**What are some of the basic ways to improve cycle time?**

**1. Reduce WIP**

**1.1 Decrease input until WIP drops to desired value.**

**1.2 Increased line speed (the number of moves or turns per day) until WIP drops to desired value**

**1.2.1 adding labor**

**1.2.2 adding overtime**

**1.2.3 reducing wasted time**

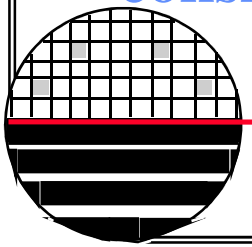
**2. Reduce the number of process steps**

**3. Reduce the lot size.**

**4. Reduce non value added operations. Like working on control wafers, measurements, unnecessary meetings, etc.**

**5. Fine tuning.**

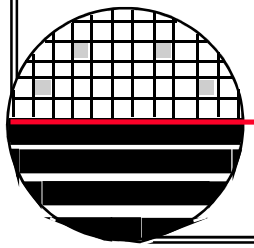
**All of the above needs to be done in such a way as to be consistent with output goals, factory tool capacity and direct labor goals for the factory.**



# *DEFINITIONS*

**CYCLE TIME - the time it takes to process wafers from start to finish. Various cycle times can be calculated depending on the exact definition. Usually cycle time is the number of calendar days to process a lot from start to ship. Other variations include single wafer cycle times, cycle time based on work days rather than calendar, etc.**

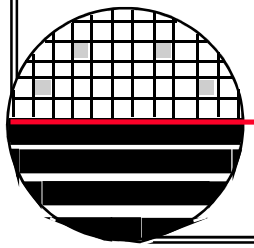
**BASELINE CYCLE TIME (work days), (BSWCT and BWLCT) - this is the cycle time at the start of a cycle time improvement program. At that point in time a CIM system data base query is done to find the cycle time for each process flow (PMOS, NMOS, CMOS, EEPROM, etc.) This is used as the reference point for measuring cycle time improvement.**



# *DEFINITIONS*

**THEORETICAL SINGLE WAFER CYCLE TIME (TSWCT) - the minimum cycle time calculated for a single wafer lot with no other wafers in the factory, no equipment down time, no queues, etc. (includes equipment set up time)**

**THEORETICAL WAFER LOT CYCLE TIME (TWLCT) - the minimum cycle time calculated for a single lot (typically 24 wafers but could be less) with no other wafers in the factory, no equipment down time, no queues, etc. Operations that one wafer at a time will result in additional processing time for the 2nd to Nth wafer in the lot. (includes equipment set up time)**

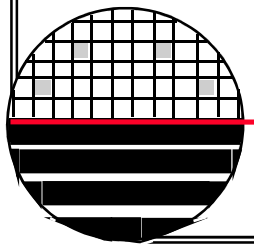


# *DEFINITIONS*

**ENTITLED CYCLE TIME (entitlement) - this is the goal for cycle time performance. It is somewhat arbitrary and is set low enough to be a challenge. For example the goal might be 2.5 X the TSWCT, which is considered world class today. In terms of wafer lot cycle time, one can calculate the ratio of TSWCT/TWLCT and that number times the single wafer goal is the equivalent wafer lot goal.**

**Example: if the TSWCT/TWLCT = 60% then**
**60% of 2.5 X = 1.5 X**

**Thus 2.5 X TSWCT is equivalent to 1.5 X TWLCT**

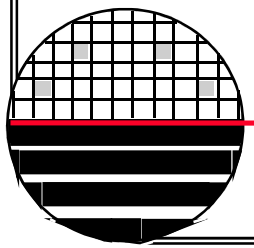


# *DEFINITIONS*

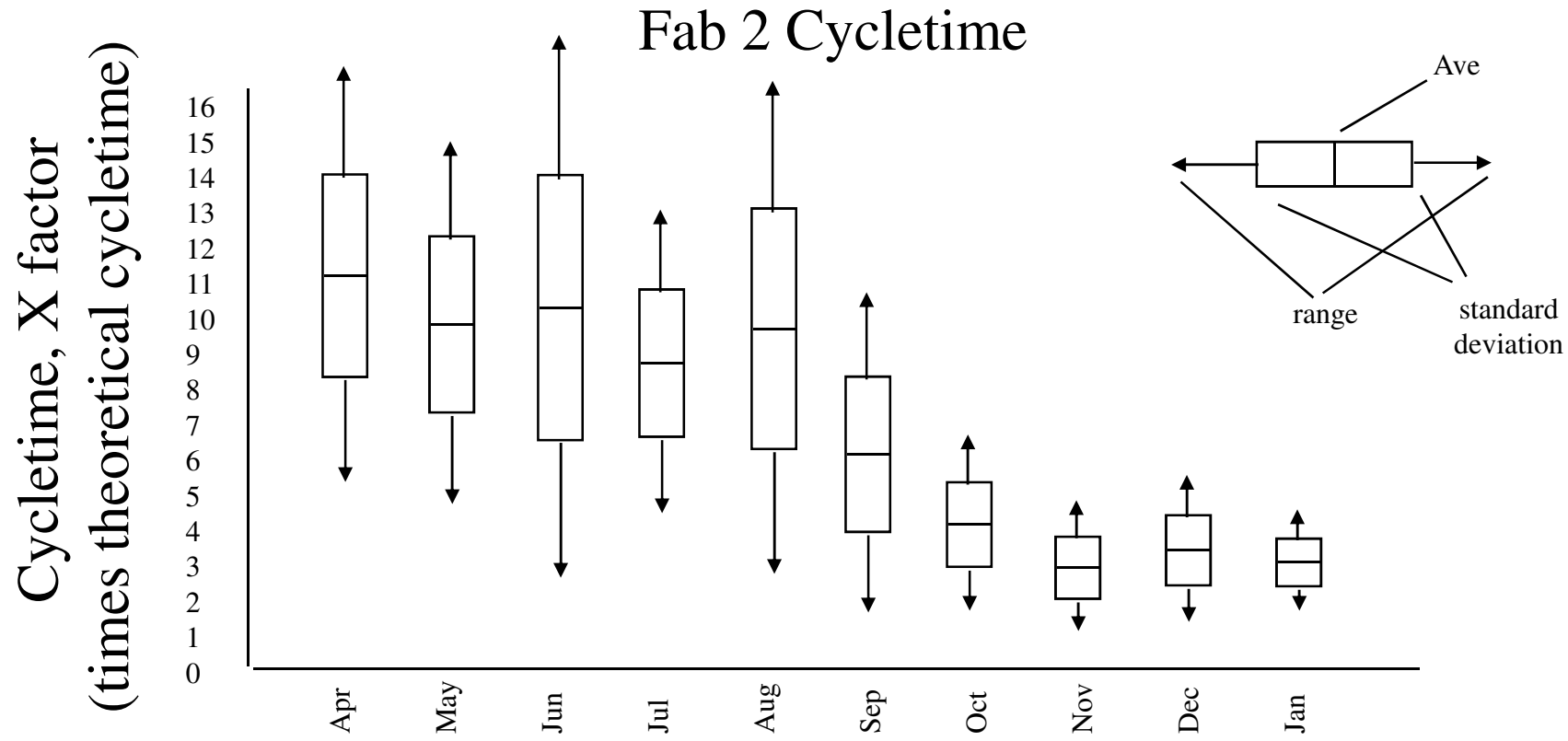
**CYCLE TIME FOR A PARTICULAR LOT - any specific lot will have its own cycle time and as progress is made during the manufacture of the lot it may appear to be ahead or behind the average wafer lot cycle time.**

**Example: The RIT factory does a p-well CMOS process that has TWLCT of 200 hours. The process is 67 steps long. Each operator can do about 5 moves in an 8 hour day and we have a total of 10 operators each working 4 hours per week. Thus: 10 operators x 1/2 day/week x 5 moves/day = 25 moves per week**

**a) 67 steps/lot divided by 25 moves per week = 2.68 weeks @ 1X**
**therefore at 3X it would take 8.0 weeks**
**b) 4 lots x 67 steps/lot divided by 25 moves per week = 10.7 weeks at 1X**
**therefore at 3X it would take 32.1 weeks**
**c) a wafer lot started 3 weeks ago is at step 20 what is its X factor?**
**It could be at step 75 so 75/20 = 3.75 X**



# CYCLE TIME IMPROVEMENT



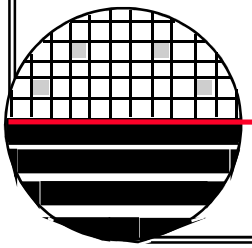
# *ASSESSMENT*

**The first action is to make a complete assessment of the existing cycle time performance.**

**1. THEORETICAL SINGLE WAFER AND WAFER LOT CYCLE TIMES**

**2. GOAL OR ENTITLED CYCLE TIME**

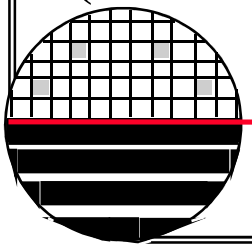
**3. BASELINE SINGLE WAFER AND WAFER LOT CYCLE TIMES**



## *ASSESSMENT*

# THEORETICAL SINGLE WAFER AND WAFER LOT CYCLE TIMES

**This is usually done by doing a factory data base query to find the minimum and average run times by operation. Then for each process the sum of the times for each operation in the process can give the cycle times. If the minimum times are used in the calculation the result is the theoretical wafer lot cycle time. The single wafer cycle times are calculated by subtracting the additional processing time for the 2nd to nth wafer (set up time is the same). The calculation using the minimum and the average values should be close. If they are not then same operation is taking different time depending on who is doing the operation. (at RIT this is often true, in industry this is less true)**



# SUB-CMOS 150 PROCESS

SUB-CMOS Versions 150

1. ID01 -scribe
2. DE01 – 4pt probe
3. CL01 – RCA Clean
4. OX05--- pad oxide, Tube 4
5. CV02- 1500 Å
6. PH03 –1- n well
7. ET29 – LAM490
8. IM01 – n-well P31
9. ET07 – Branson Asher
10. CL01 – RCA Clean
11. OX04 – well oxide, Tube 1
12. ET19 – Hot Phos
13. IM01 – p-well B11
14. OX06 – well drive, Tube 1
15. ET06 - BOE
16. CL01 – RCA Clean
17. OX05 – pad oxide, Tube 4
18. CV02 - 3500 Å
19. PH03 – 2 - Active
20. ET29 – LAM 490
21. ET07 – Branson Asher
22. PH03 – 3 - p-well stop
23. IM01- stop B11
24. ET07- Branson Asher
25. CL01 – RCA Clean
26. OX04 – field, Tube 1
27. ET19 – Hot Phos
28. ET06 – BOE
29. OX04 – Kooi, Tube 1
30. IM01 – Blanket Vt
31. PH03 – 4 - PMOS Vt Adjust
32. IM01 – Vt- B11
33. ET07 – Branson Asher
34. ET06 - BOE
35. CL01 – RCA Clean
36. OX06 – gate, Tube 4
37. CV01 – Poly 5000A
38. IM01 - dope poly
39. OX08 – Anneal, Tube 3
40. DE01 – 4pt probe
41. PH03 – 5 – poly
42. ET08 – LAM 490
43. ET07 – Branson Asher
44. PH03 – 6 - n-LDD
45. IM01 – LDD P31
46. ET07 – Branson Asher
47. PH03 – 7 - p-LDD
48. IM01 – LDD B11
49. ET07 – Branson Asher
50. CL01- RCA Clean
51. CV03 –TEOS, 5000A
52. ET10 – Drytek Quad
53. PH03 – 8 - N+D/S
54. IM01 – N+D/S P31
55. ET07 – Branson Asher
56. PH03 – 9 P+ D/S
57. IM01 – P+ D/S B11
58. ET07 – Branson Asher
59. CL01 Special - No HF Dip
60. OX08 – DS Anneal, Tube 2,3
61. CV03 – TEOS, 5000A
62. PH03 – 10 CC
63. ET06 – Drytek Quad / BOE
64. ET07 – Branson Asher
65. CL01 Special - Two HF Dips
66. ME01- CVC 601
67. PH03 -11- metal
68. ET15 – plasma Etch Al
69. ET07 – Solvent + Asher
70. SI01 – Sinter Tube 2
71. CV03 – TEOS- 5000Å
72. PH03 – VIA
73. ET06 – Drytek Quad / BOE
74. ET07- Strip Resist
75. ME01- PE 4400
76. PH03 - M2
77. ET15 -plasma Etch Al
78. ET07 – Solvent + Asher
79. SEM1 - pictures
80. TE01
81. TE02
82. TE03
83. TE04

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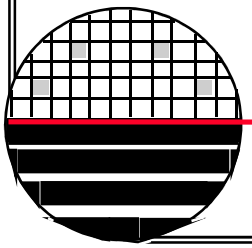
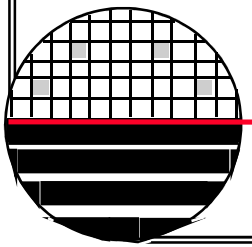


# ADV-CMOS 150 PROCESS

CMOS Versions 150, one level Metal

1. ID01 - scribe
2. DE01 - 4 pt probe
3. CL01 – RCA clean
4. OX05--- pad oxide 500 Å, Tube 4
5. CV02- 1500 Å $Si_3N_4$ Deposition
6. PH03 – level 1- STI
7. ET29 - etch shallow trench, 4000 Å
8. ET07 – ash
9. CL01 – RCA clean
10. OX05 – liner oxide, 500 Å, Tube 4
11. PH03 – level 2 - n-well
12. IM01 – 3E13, $P^{31}$, 170 KeV
13. ET07 – ash
14. PH03 – level 3 – p-well
15. IM01 – 8E13, $B^{11}$, 80 KeV
16. ET07 – ash
17. CL01 – RCA clean
18. CV03 – oxide trench fill, P-5000
19. CM01 – Trench CMP
20. CL02 – CMP Clean
21. CL01 – RCA clean
21.1 OX08 Anneal, Tube 1
22. ET19 – hot phos – $Si_3N_4$ removal
23. OX06 well drive, 6hr 1100C,Tube1
24. PH03 – level 4 – NMOS $V_T$ adjust
25. IM01 – 2.15E12, $P^{31}$, 60 KeV
26. ET07 – ash
27. PH03 – level 5 – PMOS $V_T$ adjust
28. IM01 – 1.75E12, $B^{11}$, 60 KeV
29. ET07 – ash
30. ET06 – etch 500 Å pad oxide
31. CL01 – pre-gate oxide RCA clean
32. ET06 – etch native oxide
33. OX06 – 100 Å gate oxide, Tube 4
34. CV01 – poly deposition, 4000 Å
35. PH03 – level 6 – poly gate
36. ET08 – poly gate plasma etch
37. ET07 – ash
38. CL01 – RCA clean
39. OX05 – poly re-ox, 500 Å, Tube 4
40. PH03 – level 7 - p-LDD
41. IM01 – 4E13, $B^{11}$, 50 KeV
42. ET07 – ash
43. PH03 – level 8 – n-LDD
44. IM01 – 4E13, $P^{31}$, 60 KeV
45. ET07 – ash
46. CL01 – RCA clean
47. CV02 – nitride spacer dep
48. ET39 – sidewall spacer etch
49. PH03 – level 9 - N+D/S
50. IM01 – 4E15, $P^{31}$, 60 KeV
51. ET07 – ash
52. PH03 – level 10 - P+ D/S
53. IM01 – 4E15, $B^{11}$, 50 KeV
54. ET07 – ash
55. CL01 – RCA clean
56. OX08 – DS Anneal, Tube2,3
57. ET06 – Silicide pad ox etch
58. ME03 – HF dip & Ti Sputter
59. RT01 – RTP 1 min, 650C
60. ET11 – Unreacted Ti Etch
61. RT02 – RTP 1 min,800C
62. CV03 – TEOS, P-5000
63. PH03 – level 11 - CC
64. ET06 – CC etch
65. ET07 – ash
66. CL01 – RCA clean
67. ME01 – Aluminum
68. PH03 – level 12-metal
69. ET15 – plasma Al Etch
70. ET07 – ash
71. SI01 – sinter
72. SEM1
73. TE01
74. TE02
75. TE03
76. TE04

L = 0.5 µm
$V_{DD}$ = 3.0 V
$V_{TN}$ = 0.75 V
$V_{TP}$ = - 0.75V



*Rochester Institute of Technology*
*Microelectronic Engineering*

(Revision 1-6-09)

# *ASSESSMENT*

**QUERY DEFINITION FOR AS/400**
**QUERY NAME:**ASSESSMENT **LIBRARY:**MESADB
**FILE:** LTLMD101 **FORMAT:**LTFMD101
**RESULT FIELDS:** SETUPTIME UDN04
**SELECT RECORDS:** MDLOT LIKE 'F%'
AND MDMVTP EQ '1'
AND MDTRTM GT 10
AND MDTRYR GT 95
OR MDLOT LIKE 'F%'
AND MDTRYR GT 95
AND MDFROP EQ 'IM01'
**ORDERING OF SELECTED FIELDS:**
**REPORT COLUMN FORMATTING AND SUMMARY FUNCTIONS**

| | | | |
|---|---|---|---|
| MDTRYR | | | 1=TOTAL |
| MDTRMO | | | 2=AVE |
| MDTRDY | | | 3=MIN |
| MDFROP | | 5 | 4=MAX |
| MDRTM | 2 3 4 | | 5=COUNT |
| SETUPTIME | 2 3 4 | | |

**REPORT COLUMN FORMATTING AND SUMMARY FUNCTIONS:**
**REPORT BREAKS:**

# ASSESSMENT

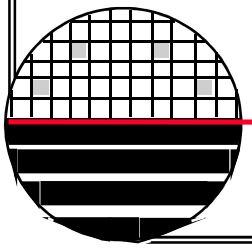
**QUERY OUTPUT**

| CL01 | | CV01 | | CV02 | |
|---|---|---|---|---|---|
| AVE | 64 | AVE | 203 | AVE | 171 |
| MIN | 20 | MIN | 120 | MIN | 20 |
| MAX | 200 | MAX | 301 | MAX | 480 |
| COUNT | 181 | COUNT | 26 | COUNT | 25 |

| CV03 | | DE01 | | DI01 | |
|---|---|---|---|---|---|
| AVE | 226 | AVE | 27 | AVE | 170 |
| MIN | 60 | MIN | 11 | MIN | 60 |
| MAX | 999 | MAX | 100 | MAX | 360 |
| COUNT | 25 | COUNT | 48 | COUNT | 22 |

| DI02 | | DI04 | | ET01 | |
|---|---|---|---|---|---|
| AVE | 39 | AVE | 110 | AVE | 170 |
| MIN | 10 | MIN | 15 | MIN | 60 |
| MAX | 180 | MAX | 230 | MAX | 360 |
| COUNT | 235 | COUNT | 27 | COUNT | 22 |

| ET02 | | ET07 | | ET08 | |
|---|---|---|---|---|---|
| AVE | 58 | AVE | 53 | AVE | 103 |
| MIN | 20 | MIN | 15 | MIN | 30 |
| MAX | 140 | MAX | 180 | MAX | 180 |
| COUNT | 264 | COUNT | 24 | COUNT | 24 |



# ASSESSMENT

## QUERY OUTPUT

| ET09 | | GR01 | | ID01 | |
|---|---|---|---|---|---|
| AVE | 101 | AVE | 25 | AVE | 23 |
| MIN | 20 | MIN | 20 | MIN | 13 |
| MAX | 240 | MAX | 30 | MAX | 45 |
| COUNT | 49 | COUNT | 18 | COUNT | 10 |

| IM01 | | ME01 | | OX01 | |
|---|---|---|---|---|---|
| AVE | 113 | AVE | 173 | AVE | 170 |
| MIN | 12 | MIN | 30 | MIN | 60 |
| MAX | 700 | MAX | 300 | MAX | 360 |
| COUNT | 261 | COUNT | 22 | COUNT | 22 |

| OX02 | | OX03 | | OX04 | |
|---|---|---|---|---|---|
| AVE | 39 | AVE | 196 | AVE | 211 |
| MIN | 10 | MIN | 30 | MIN | 55 |
| MAX | 180 | MAX | 360 | MAX | 720 |
| COUNT | 235 | COUNT | 18 | COUNT | 78 |

| OX05 | | OX06 | | OX07 | |
|---|---|---|---|---|---|
| AVE | 163 | AVE | 178 | AVE | 170 |
| MIN | 60 | MIN | 20 | MIN | 60 |
| MAX | 360 | MAX | 999 | MAX | 360 |
| COUNT | 20 | COUNT | 55 | COUNT | 22 |

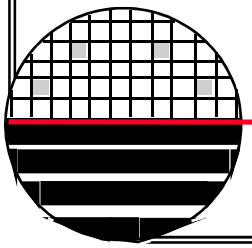
# ASSESSMENT

**QUERY OUTPUT**

| OX08 | | PH03 | | SI01 | |
|---|---|---|---|---|---|
| AVE | 113 | AVE | 116 | AVE | 170 |
| MIN | 45 | MIN | 15 | MIN | 60 |
| MAX | 180 | MAX | 360 | MAX | 360 |
| COUNT | 19 | COUNT | 221 | COUNT | 22 |

| TE01 | | TE02 | | TE03 | |
|---|---|---|---|---|---|
| AVE | 133 | AVE | 126 | AVE | 117 |
| MIN | 60 | MIN | 60 | MIN | 45 |
| MAX | 240 | MAX | 180 | MAX | 180 |
| COUNT | 17 | COUNT | 16 | COUNT | 16 |

| TE04 | | IM01 SETUP | | TOTAL | |
|---|---|---|---|---|---|
| AVE | 110 | AVE | 49 | AVE | 100 |
| MIN | 60 | MIN | 0 | MIN | 11 |
| MAX | 180 | MAX | 180 | MAX | 999 |
| COUNT | 6 | COUNT | 261 | COUNT | 1,567 |



# ASSESSMENT

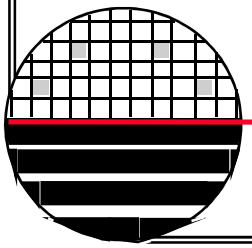
| Rochester Institute of Technology | | | | Assessment Tool | | Revision 3-12-2000 | |
|---|---|---|---|---|---|---|---|
| Microelectronic Engineering | | | | | | Name: assess.xls | |
| Microelectronics Manufacturing | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | FROM DATA BASE | | **CMOS-PW3 Process** | | | | |
| | | | | | ((C-B)/E+B)*D | C*D*E | |
| Operation | Ave Lot | minimum | Process | Lot | Theoretical | Theoretical | |
| | Setup time | lot run time | Operation | Multiplier | Single Wafer | Wafer Lot | |
| | | | Repeats | | Cycle Time | Cycle Time | |
| | minutes | minutes | | | minutes | minutes | |
| ID01 | 0 | 10 | 1 | 3 | 3.3 | 30.0 | |
| DE01 | 0 | 15 | 2 | 1 | 30.0 | 30.0 | |
| CL01 | 15 | 45 | 9 | 1 | 405.0 | 405.0 | |
| OX05 | 60 | 180 | 2 | 1 | 360.0 | 360.0 | |
| CV02 | 60 | 150 | 1 | 1 | 150.0 | 150.0 | |
| PHO3 | 30 | 120 | 9 | 3 | 540.0 | 3240.0 | |
| ETO9 | 30 | 60 | 2 | 3 | 80.0 | 360.0 | |
| ET06 | 0 | 10 | 4 | 3 | 13.3 | 120.0 | |
| IMO1 | 60 | 90 | 6 | 3 | 420.0 | 1620.0 | |
| ET07 | 0 | 45 | 9 | 1 | 405.0 | 405.0 | |
| OX04 | 60 | 180 | 2 | 1 | 360.0 | 360.0 | |
| GR01 | 0 | 30 | 0 | 1 | 0.0 | 0.0 | |
| ET03 | 0 | 10 | 1 | 1 | 10.0 | 10.0 | |
| 0X06 | 60 | 120 | 2 | 1 | 240.0 | 240.0 | |
| CV01 | 60 | 90 | 1 | 1 | 90.0 | 90.0 | |
| DI04 | 60 | 180 | 1 | 1 | 180.0 | 180.0 | |
| ET02 | 0 | 10 | 1 | 1 | 10.0 | 10.0 | |
| ET08 | 60 | 60 | 1 | 3 | 60.0 | 180.0 | |
| CV03 | 60 | 90 | 1 | 1 | 90.0 | 90.0 | |
| ME01 | 120 | 180 | 1 | 1 | 180.0 | 180.0 | |
| SI01 | 60 | 60 | 1 | 1 | 60.0 | 60.0 | |
| ET05 | 60 | 90 | 1 | 1 | 90.0 | 90.0 | |
| TE01 | 0 | 60 | 4 | 1 | 240.0 | 240.0 | |
| TOTALS= | | | 62 | | 4016.7 | 8450.0 | minutes |
| | | | | | 8.4 | 17.6 | days |

# *ASSESSMENT*

**GOAL or ENTITLED CYCLE TIME (entitlement) - this is the goal for cycle time performance. It is somewhat arbitrary and is set low enough to be a challenge. For example the goal might be 2.5 X the TSWCT, which is considered world class today. In terms of wafer lot cycle time, one can calculate the ratio of TSWCT/TWLCT and that number times the single wafer goal is the equivalent wafer lot goal.**

**Example: if the TSWCT/TWLCT = 60% then**
**60% of 2.5 X = 1.5 X**

**Thus 2.5 X TSWCT is equivalent to 1.5 X TWLCT**

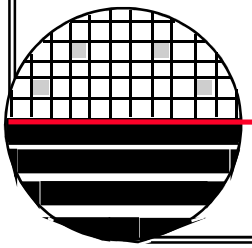


# *ASSESSMENT*

## BASELINE SINGLE WAFER AND WAFER LOT CYCLE TIMES

**A data base query is made to determine the date lots were started and the date they were completed. The difference is the Cycle Time in Calendar Days.**

**A data base query is made to determine the number of work days between the start of a lot and the completion of a lot. This is the Cycle Time in Work Days.**



# *ASSESSMENT*

**QUERY DEFINITION FOR AS/400**
**QUERY NAME:**CYCLETIME1 **LIBRARY:**MESADB
**FILE:** LTLMD101 **FORMAT:**LTFMD101
**RESULT FIELDS:** DATE
MDTRYR*10,000+MDTRMO*100+MDTRDY
DAYS (MDTRYR-90)*12*30+MDTRMO*30+MDTRDY

**SELECT RECORDS:**

| | | | |
|---|---|---|---|
| | MDLOT LIKE | | 'F%' |
| AND | MDFROP | EQ | 'ID01' |
| AND | MDMVTP | EQ | '1' |
| AND | DATE GT | 950101 | |
| OR | DATE GT | 950101 | |
| AND | MDLOT LIKE | 'F%' | |
| AND | MDTOOP | EQ | 'TE01' |
| AND | MDMVTP | EQ | '1' |

**ORDERING OF SELECTED FIELDS:**
**REPORT COLUMN FORMATTING AND SUMMARY FUNCTIONS**
**REPORT COLUMN FORMATTING AND SUMMARY FUNCTIONS:**
**REPORT BREAKS:**



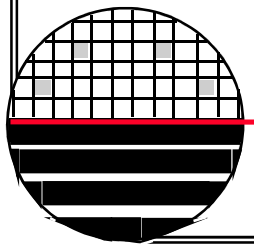
 

# *ASSESSMENT*

| DAY | DATE | LOT NUMBER | PRODUCT | STEP | FROM | TO |
|---|---|---|---|---|---|---|
| 2,956 | 98-02-16 | F970620 | RIT-FAC-CPW-0944 | 59 | | 60 |
| 2,727 | 97-04-14 | | | 1 | | 2 |
| 2,915 | 98-01-05 | F970414 | RIT-FAC-CPW-2000 | 58 | | 59 |
| 2,654 | 97-04-14 | | | 1 | | 2 |
| 2,918 | 98-01-08 | F970324 | RIT-FAC-CPW-0944 | 59 | | 60 |
| 2,634 | | | | 1 | | 2 |

**ETC.**

**SUBTRACT DAY FOR STEP 1 FROM DAYS FOR LAST STEP TO GET CYCLE TIME IN CALENDAR DAYS**



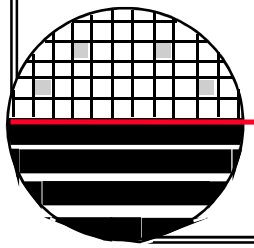
# *ASSESSMENT*

**QUERY DEFINITION FOR AS/400**

**QUERY NAME:**CYCLETIME2 **LIBRARY:**MESADB
**FILE:** LTLMD101 **FORMAT:**LTFMD101
**RESULT FIELDS:** DATE
MDTRYR*10,000+MDTRMO*100+MDTRDY
DAYS (MDTRYR-90)*12*30+MDTRMO*30+MDTRDY

**SELECT RECORDS:** DATE GT 950101
AND MDLOT LIKE 'F%'
AND MDMVTP EQ '1'
AND MDPRDI LIKE '%FAC%'

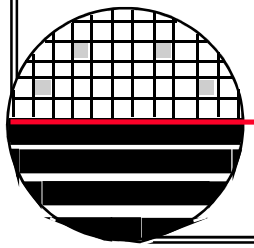
**ORDERING OF SELECTED FIELDS:**
**REPORT COLUMN FORMATTING AND SUMMARY FUNCTIONS:**
**REPORT BREAKS:**



# *ASSESSMENT*

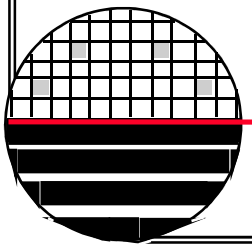
**This Query gives the date for any day that a factory move was made. This is combined with the start date and end date from the CYCLETIME1 query results to give the Cycle Time in work days.**

| | Date | | Date | | Date | | Date | | Date |
|---|---|---|---|---|---|---|---|---|---|
| | 97-04-24 | | 97-04-14 | | 97-04-28 | | 97-05-02 | | |
| COUNT | 10 | COUNT | 2 | COUNT | 5 | COUNT | 4 | COUNT | |
| | 97-04-04 | | 97-04-17 | | 97-04-30 | | 97-06-03 | | |
| COUNT | 3 | COUNT | 9 | COUNT | 3 | COUNT | 2 | COUNT | |
| | 97-04-06 | | 97-04-20 | | 97-05-04 | | 97-06-04 | | |
| COUNT | 1 | COUNT | 1 | COUNT | 1 | COUNT | 7 | COUNT | |
| | 97-04-07 | | 97-04-21 | | 97-05-05 | | 97-06-05 | | |
| COUNT | 5 | COUNT | 6 | COUNT | 7 | COUNT | 1 | COUNT | |
| | 97-04-09 | | 97-04-22 | | 97-05-07 | | 97-06-08 | | |
| COUNT | 5 | COUNT | 2 | COUNT | 2 | COUNT | 2 | COUNT | |
| | 97-04-10 | | 97-04-23 | | 97-05-27 | | 97-06-09 | | |
| COUNT | 8 | COUNT | 4 | COUNT | 2 | COUNT | 3 | COUNT | |

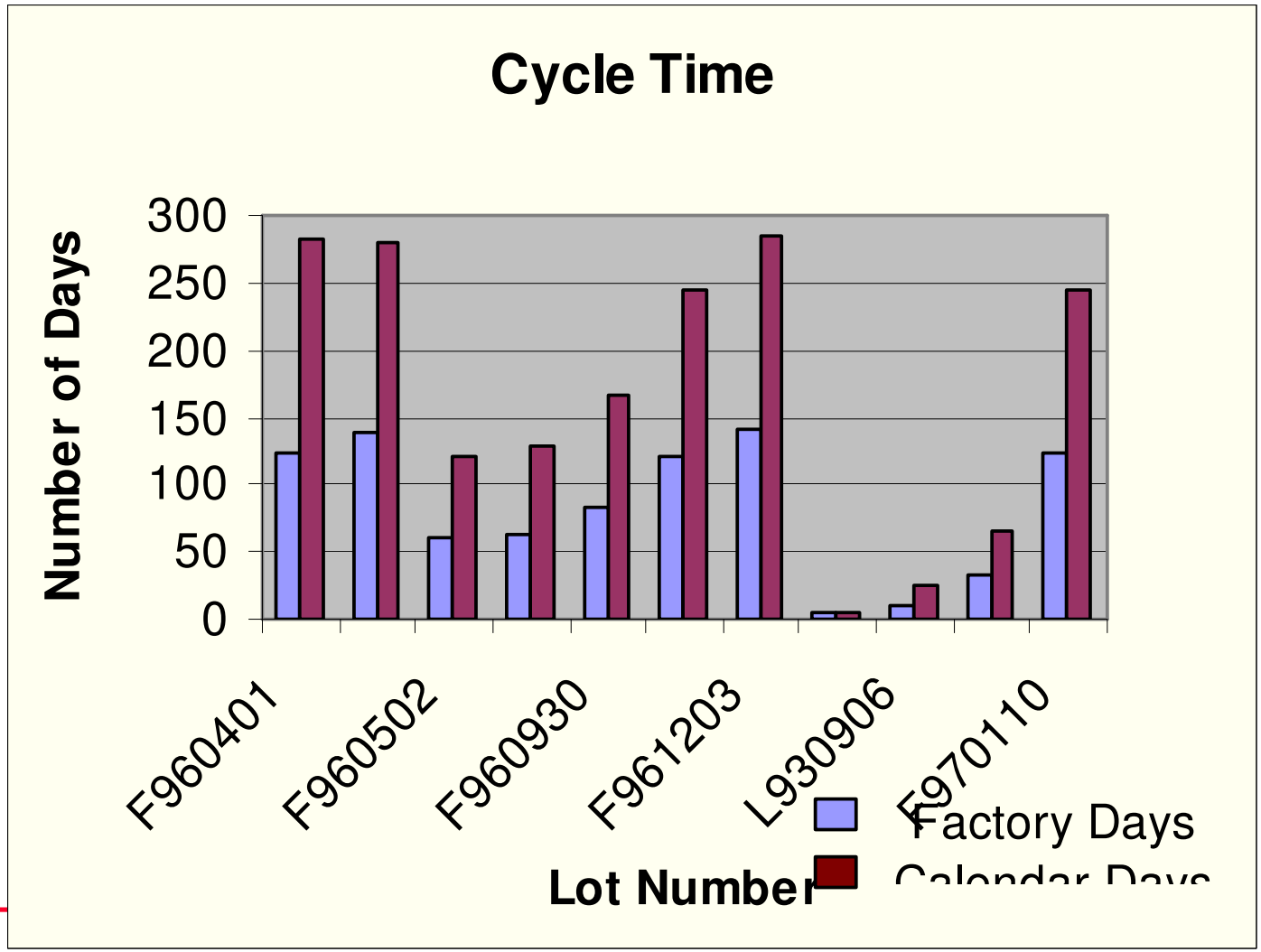


# ASSESSMENT

| ROCHESTER INSTITUTE OF TECHNOLOGY | | | | | | | 3/12/00 | |
|---|---|---|---|---|---|---|---|---|
| MICROELECTRONIC ENGINEERING | | | | | | | | |
| | | | | | | | | |
| CYCLE TIME | | | | | | | | |
| | | | WORK | CALENDAR | | | | |
| END | START | LOT # | DAYS | DAYS | PROCESS | TSWCT | X-FACTOR | |
| 1/6/97 | 4/3/96 | F960401 | 123 | 283 | CMOS-4 | 10 | 12 | |
| 2/11/97 | 5/2/96 | F96001 | 139 | 279 | CMOS-3 | 8 | 17 | |
| 9/4/96 | 5/2/96 | F960502 | 61 | 122 | CMOS-4 | 10 | 6 | |
| 1/17/97 | 9/9/96 | F960909 | 64 | 128 | CMOS-3 | 8 | 8 | |
| 3/17/97 | 9/30/96 | F960930 | 83 | 167 | CMOS-4 | 10 | 8 | |
| 7/2/97 | 10/28/96 | F961028 | 122 | 244 | CMOS-4 | 10 | 12 | |
| 9/17/97 | 12/3/96 | F961203 | 142 | 284 | CMOS-3 | 8 | 18 | |
| 7/16/93 | 7/13/93 | L930712 | 4 | 4 | PMOS | 2 | 2 | |
| 9/29/93 | 9/6/93 | L930906 | 9 | 24 | PMOS | 2 | 5 | |
| 2/17/97 | 12/12/96 | F961212 | 33 | 65 | NWELL | 4 | 8 | |
| 9/15/97 | 1/10/97 | F970110 | 123 | 245 | CMOS-3 | 8 | 15 | |
| | | | | | | | | |



# *ASSESSMENT*


Cycle Time
Number of Days
300
250
200
150
100
50
0
F960401
F960502
F960930
F961203
L930906
F970110
Factory Days
Calendar Days
Lot Number

# CYCLE TIME REDUCTION

$$\text{Cycle Time} = \frac{\text{WIP}}{\text{Line Speed}}$$

where WIP is work in process (wafers)

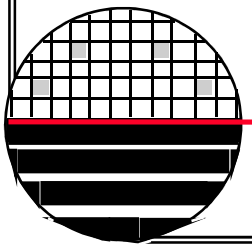
$$\text{Line speed} = \frac{\text{Outs} + \text{Starts}}{2}$$

To show the relationship between daily turns (t) and cycle time, let each start represent the introduction of wafers requiring some number of turns per start (T)

$$\text{Starts} = \frac{t}{T}$$

Also Outs are related to starts with process yield (Y)

$$\text{Outs} = \text{Starts}\ Y$$



# CYCLE TIME REDUCTION

Combining the equations above we see an expression for Cycle Time that includes WIP, Starts, turns, Turns/start, and Yield.

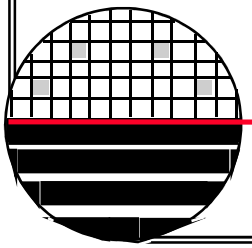
$$\text{Cycle Time} = \frac{2\,(\text{WIP})\,(T)}{t\,(1+Y)}$$

It becomes obvious from the above equations that to decrease cycle time one should

decrease WIP and/or Turns/Start (T)

and/or

increase Yield and/or turns (t)

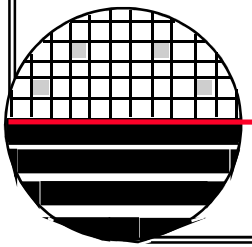


# CYCLE TIME REDUCTION

WIP reduction is normally achieved by setting the starts to a number somewhat lower than the sum of Outs plus scrap. Then over a period of months (6 to 12 months) the WIP is gradually reduced to a predetermined level.

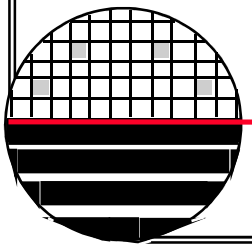
Line speed is increased by increasing the daily turns, t, simplifying the process to reduce the number of steps in the process (T) turns/start, and/or increasing the process yield (Y)

To increase the daily turns one could use overtime, add labor, and/or increase productivity. This activity must be combined with proper control of wafer input to control WIP otherwise increasing the daily turns may not result in a decrease in cycle time.



# CYCLE TIME REDUCTION

*"Caution!!! Most fabs will first choose to focus exclusively on increasing turns and not set starts at a level consistent with turns capability and a plan to reduce WIP. The reason is probably because the fab is being driven harder than its existing capability and still not meeting demand. Any mention of a reduction in starts is met with strong opposition. The belief is that a push for more turns is always possible. It is a fatal mistake to not regulate starts as part of the plan to reduce WIP. You simply can not "outrun" the starts. To increase turns, especially if overtime is used up is not easy and if it an be done at all it takes time. Hiring and training more people also takes time. A successful cycle time reduction plan must plan to increase turns and plan to regulate starts in such a way as to systematically reduce the WIP over a period of time". Jack Scholl, Motorola*



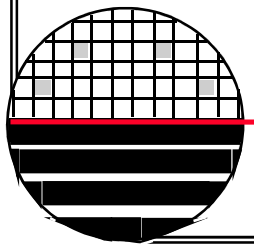
# CONSERVATIVE APPROACH TO REDUCING WIP

1. Determine the daily turns capability of the line.

2. Calculate the daily outs by using the weighted required turns/start, the process yield of the line and the daily turns.

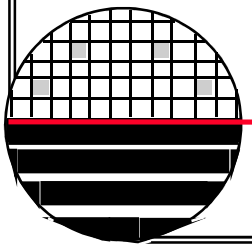
3. Determine the final desired WIP goal and when this is to be achieved. Divide the delta in WIP by the number of weeks to get an average delta inventory per week. (Typical numbers might be to drop 1000 wafers per month which works out to about 50 wafers per day.)

4. Set daily inputs at a level 50 wafers below the sum of daily Outs plus daily scrap.



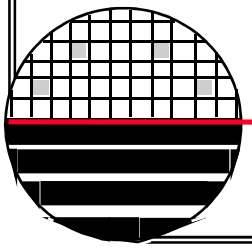
# CYCLE TIME REDUCTION

Over the following months, if the plan is a good one, the inventory should drop without any drop in the output of the line. Even though the starts have been lowered, the output is maintained as the dropping WIP continues to drive the outs. It is very important during this time to carefully monitor two critical parameters: daily turns and daily turns/WIP. An increase in the daily turns/WIP is an indication that the cycle time is improving, but it is important that this be achieved without reducing turns which would cause outs to be missed. As the WIP is reduced sooner or later the factory will begin to struggle to maintain the daily turns due to reduced buffer stock not being available when equipment or processes go down. When this happens it is time to re-evaluate the WIP reduction plan.



# CYCLE TIME REDUCTION

*Caution!!! Although a good WIP control program will definitely produce an improvement in cycle time, it is primarily aimed at targeting starts at a level consistent with the factory's demonstrated ability to turn product. Continuing to reduce WIP beyond the point where turns begin to drop may make a good looking cycle time graph, but it will also reduce output which can result in a dramatic negative impact to business." Jack Scholl, Motorola*

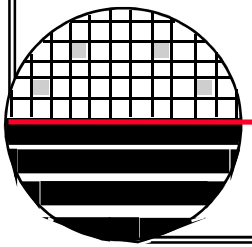


# CYCLE TIME REDUCTION

Example: Given a factory that typically does 30,000 turns/day and the number of wafers started per week is 5000. If the number of turns per start is 50 calculate the change in WIP after one week.

5000 wafers x 50 turns/wafer = 250,000 turns and the number of turns per week is 30,000 x 7 = 210,000 so WIP will increase by 40,000 turns or about 800 wafers. After 1 month that will be 3200 wafers and after four months WIP will increase by 12,800 wafers and increasing every month.

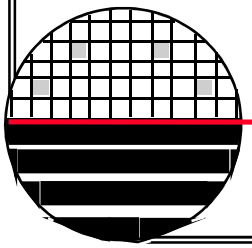
This factory is not balanced and it will be necessary to decrease input or increase turns. Turns is directly related to output and if the customer demand exists it is useful to look at increasing turns.



# *CYCLE TIME REDUCTION*

Increasing turns (Line Speed) can be done by adding labor or by improving the efficiency of the labor already employed. The people working in the factory spend some of their time in productive activities and some in non-productive activities. Some of the non-productive activities are required. The goal should be to minimize the required non-productive activities and maximize the productive activities of labor.

$$\text{Cycle Time} = \frac{\text{WIP}}{\text{Line Speed}}$$



# *CYCLE TIME REDUCTION*

## PRODUCTIVE HOURS (MAXIMIZE)

Processing Wafers

## NON-PRODUCTIVE HOURS (MINIMIZE)

## REQUIRED (MINIMIZE)

Department Meetings
Team Improvement Activities
Vacation/Sick Time
Essential Set-up and Monitors
Training
Clerical/Administrative Duties

## NOT REQUIRED (ELIMINATE)

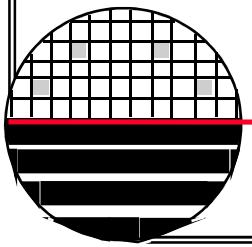
| No Equipment | No Material | No Operator |
|---|---|---|
| Process/Equipment Down | Out of Balance Line | Absenteeism |
| Excessive Equipment Set-up | Material on Hold | Excessive Paperwork |
| Excessive Qualifications | Minimum Load Sizes | Start-up/shut down |
| Equipment Modifications | | Idle time |

# CYCLE TIME REDUCTION

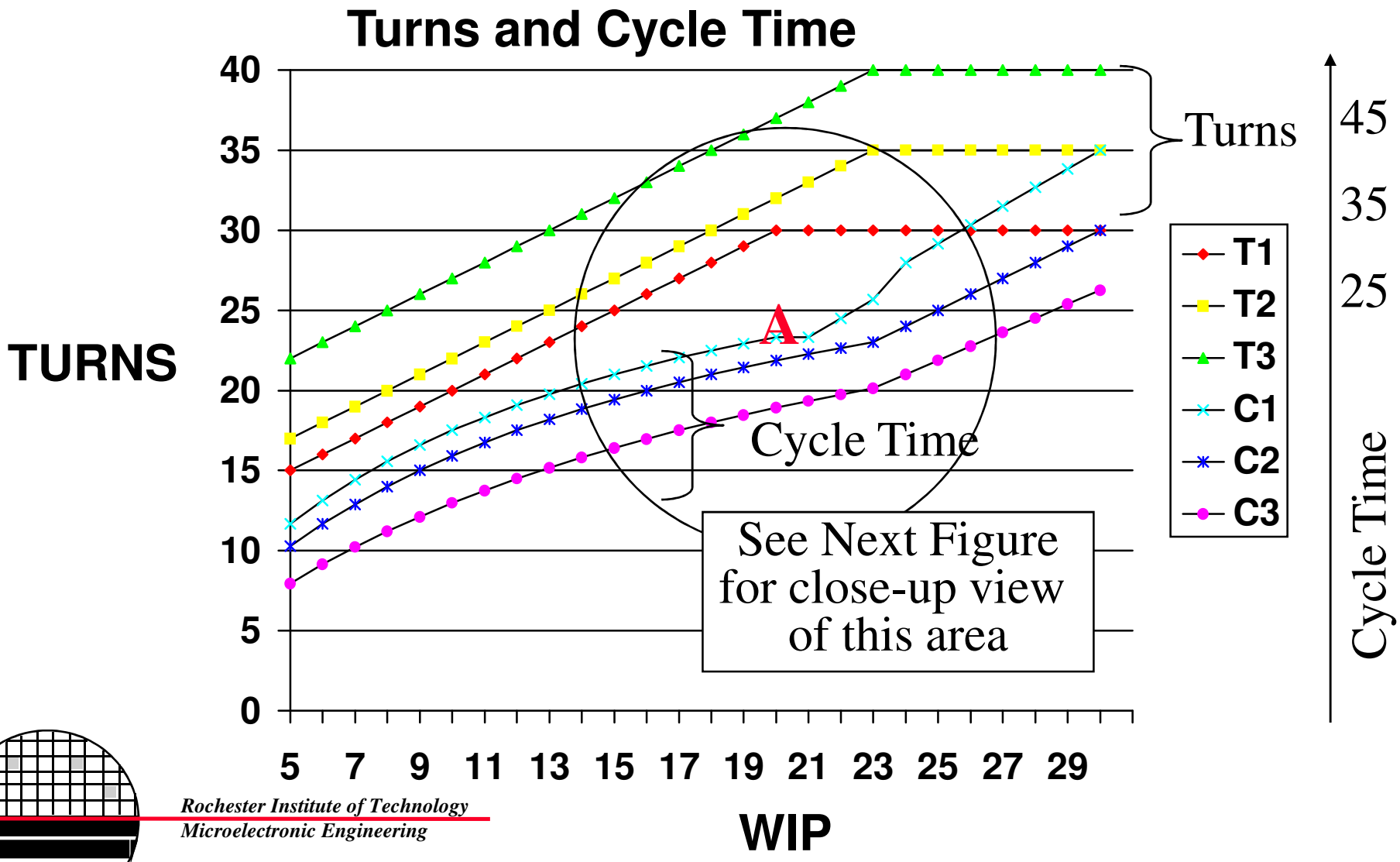
Example: The figure on the next page illustrates the relationship between turns, WIP and cycle time. The data represents a factory at three different times (Time-1, Time-2, and Time-3) in its cycle time improvement program where the turns per day is given by T1, T2, and T3 and the corresponding cycle time is C1, C2 and C3.

Initially at Time-1 the factory is capable of a maximum of 30K turns per day unless the WIP drops below 20K wafers then lower WIP would result in lower turns per day. This is point "A" the cycle time is 23 days.

At a later Time-2 the factory is generating up to 35K turns per day. The factory can either reduce cycle time or increase capacity.



# CYCLE TIME REDUCTION



# CYCLE TIME REDUCTION

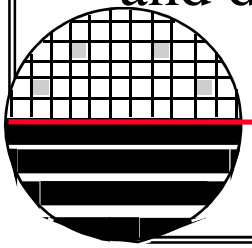
At Time-1:

At point A the WIP is 20K wafers, Cycle Time is 23 days, Turns are 30K

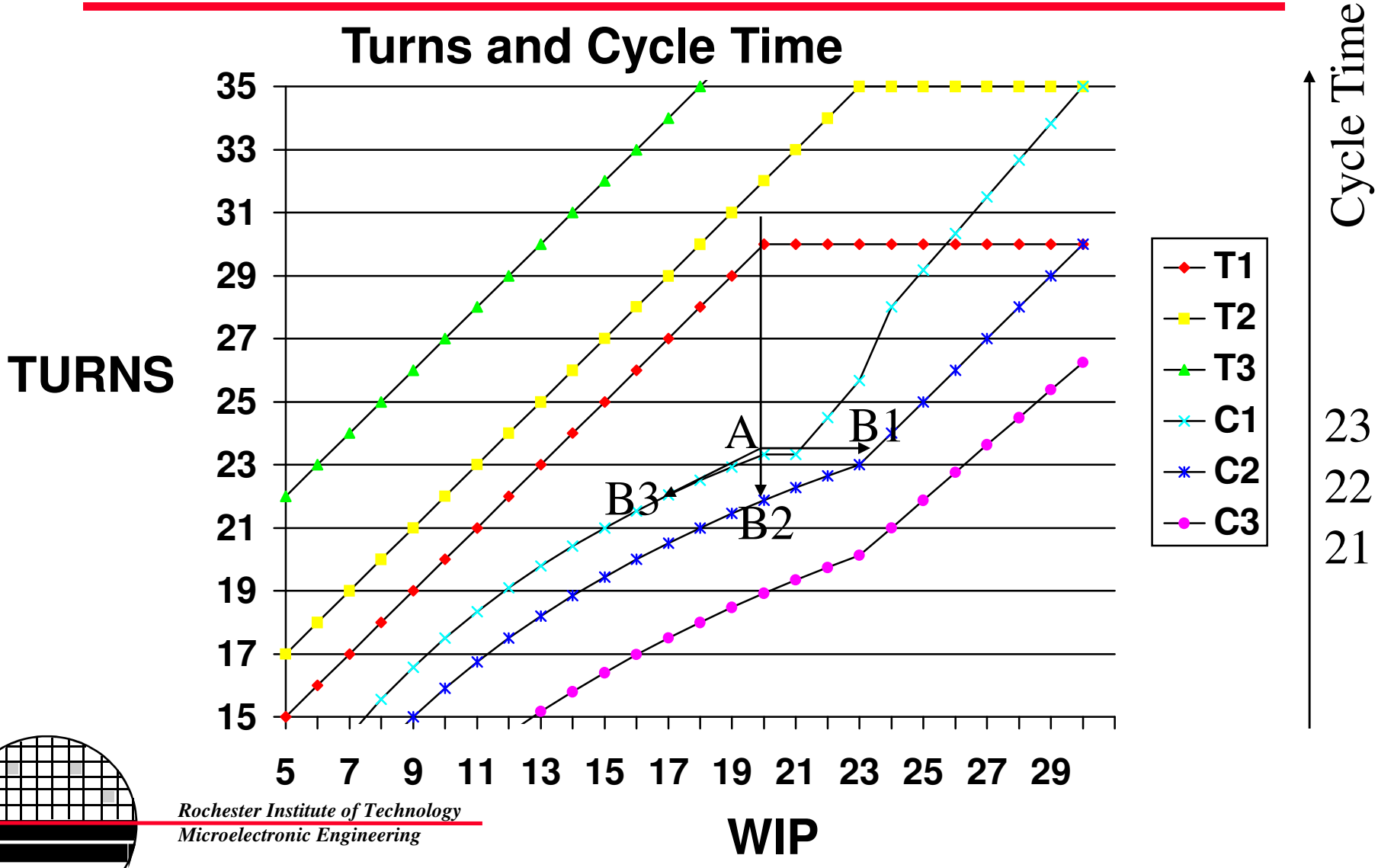
At Time-2:

At point B1 the WIP is 23K wafers, Cycle Time is 23 days, Turns are 35K
At point B2 the WIP is 20K wafers, Cycle Time is 22 days, Turns are 32K
At point B3 the WIP is 18K wafers, Cycle Time is 21 days, Turns are 30K

At Time-2 lets say that the factory has increased the turns capability to 35K turns per day. A decision could be made to use the possible increase in turns/day to increase factory output (B1) and not reduce Cycle Time, or to reduce Cycle Time a little compared to Time-1 while increasing the output a little to 32K turns/day (B2), or to keep the output the same at 30K turns/day and decrease cycle time to 21 days.

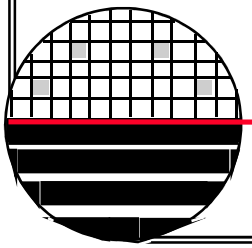


# CYCLE TIME REDUCTION



# *SPLIT THE WIP*

If the current cycle time is less than 3 times theoretical than an action plan to gradually decrease WIP over a period of six months to a year, with an objective of cutting the cycle time in half should be considered. For fabs with time greater than 3.5 times theoretical a technique called "split-the-WIP" should be considered.



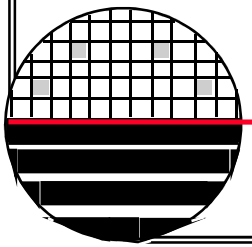
# *SPLIT THE WIP*

1. Analyze the WIP - looking for the high volume products. Normally 80% of the WIP is associated with only 20% of the products. We would like to select products that have more than several lot starts per week called high volume. Working with the high volume products identify about half of that WIP to be split. The low volume WIP will be given no special treatment.

2. Remove one half of all lots between the first step and first layer metal (almost last step). These lots are put on hold at the next safe point (generally just prior to the next photo step, that is no abnormally exposed silicon) and actually removed from the factory. At this time wafer starts on these products (the major products) are discontinued.

3. Starts are continued as normal on low volume products. No new starts are made on high volume products.

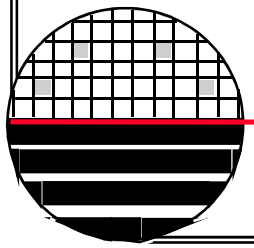
4. When the lots which were at the first step reach first metal photo, we will move all of the lots which were on hold back into the fab. At this point starts on all products are resumed as normal.



# *SPLIT THE WIP*

Example: Fab Prior to Split-the-WIP

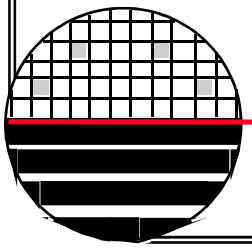
| | | |
|---|---|---|
| Total WIP | 25,000 | wafers |
| Wafers on Hold | 0 | wafers |
| Total Weekly Starts | 5,000 | wafers |
| Starts for High volume Products | 2,500 | wafers |
| Starts for Remainder | 2,500 | wafers |
| WIP of High Volume Products | 12,500 | wafers |
| WIP of Remainder | 12,500 | wafers |
| Daily Turns (moves) | 30,000 | wafers |
| Turns-to-WIP Ratio | 1.2 | |
| Wafer Ships to Probe @95% yield | 4,750 | wafers/week |



# *SPLIT THE WIP*

Example: Fab Immediately Following Start of WIP Split

| | | |
|---|---|---|
| Total WIP | 18,750 | wafers |
| Wafers on Hold | 6,250 | wafers |
| Total Weekly Starts | 2,500 | wafers |
| Starts for High volume Products | 0 | wafers |
| Starts for Remainder | 2,500 | wafers |
| WIP of High Volume Products | 6,250 | wafers |
| WIP of Remainder | 12,500 | wafers |
| Daily Turns (moves) | 30,000 | wafers |
| Turns-to-WIP Ratio | 1.6 | |
| Wafer Ships to Probe @95% yield | 4,750 | wafers/week |

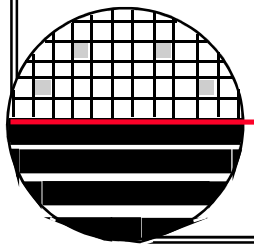


# SPLIT THE WIP

During the period of Split-the-WIP (about 2 to 2.5 weeks), no starts are made on the high volume products involved in Split-the-WIP. The fab is run normally during this period. However, we must keep tabs on the high volume products which are in the fab. When the lots which were at the first step reach metal photo, we will move all of the lots which were on hold back into the fab.

Example: Fab just prior to bringing in the wafers that were on hold

| | | |
|---|---|---|
| Total WIP | 12,500 | wafers |
| Wafers on Hold | 6,250 | wafers |
| Total Weekly Starts | 2,500 | wafers |
| Starts for High volume Products | 0 | wafers |
| Starts for Remainder | 2,500 | wafers |
| WIP of High Volume Products | 0 | wafers |
| WIP of Remainder | 12,500 | wafers |
| Daily Turns (moves) | 30,000 | wafers |
| Turns-to-WIP Ratio | 2.4 | |
| Wafer Ships to Probe @95% yield | 4,750 | wafers/week |

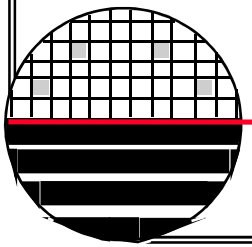


# *SPLIT THE WIP*

Example: Fab at Completion of Split-the-WIP

| | | |
|---|---|---|
| Total WIP | 18,750 | wafers |
| Wafers on Hold | 0 | wafers |
| Total Weekly Starts | 5,000 | wafers |
| Starts for High volume Products | 2,500 | wafers |
| Starts for Remainder | 2,500 | wafers |
| WIP of High Volume Products | 6,250 | wafers |
| WIP of Remainder | 12,500 | wafers |
| Daily Turns (moves) | 30,000 | wafers |
| Turns-to-WIP Ratio | 1.6 | |
| Wafer Ships to Probe @95% yield | 4,750 | wafers/week |

Note: the wafers shipped to probe was constant in all of the above examples.

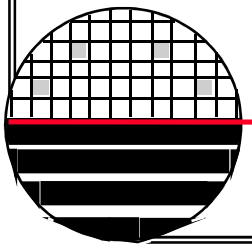


# *RAMP UP*

Ramp up refers to the process of increasing output from a semiconductor fab.

*"Often the process was to increase input and wait for one cycle time, then look for the increase in output. What would really happen would be an increase in WIP and an increase in cycle time with no increase in output" Tom Filesi, Motorola.*

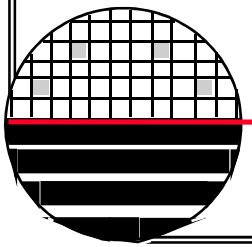
In order to increase output labor needs to be increased either through more people or overtime so that more turns will be generated each day.



# *RAMP UP*

Approach:

Determine the machine capacity per week
Determine the bottleneck machine operations
Determine the direct labor staff capacity
Determine the current fab productivity as measured by turns/day or turns per direct labor hour (including burden hours)
Calculate the desired increase in number of daily wafer starts (include wafers for expected yield loss)
Determine the increased number of turns per week using the known number of turns per start for the given products
At a rate of 15 turns per direct labor hour, calculate the overtime or additional trained operators needed.



# *RAMP UP*

Example:

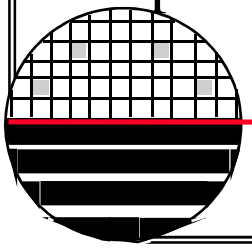
Given the average turns per start is 60, lets say we want an increase in 20 wafer outs per day.

Then 60 turns/wafer x 20 wafers/day x 5 days/week = 6000 turns/week

6000 turns/week divided by 15 turns/hour = 400 hours/week of overtime

or 10 additional people

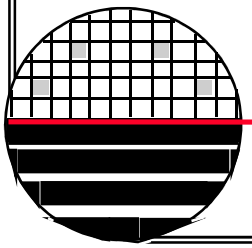
This is a simplistic approach that does not include machine capacity and other considerations.



# *MACRO PLANNING*

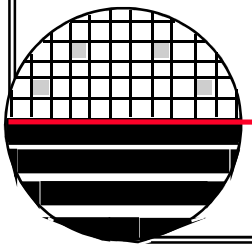
A simple approach to macro planning is described below. It is basically a spreadsheet model of a factory operation that emphasizes cycle time. The model takes into consideration a variety of details associated with the factory including:

process yield
number of operators
attendance
work schedule
scrap rate
bottlenecks
multiple processes
tool uptime
tool capacity
rework

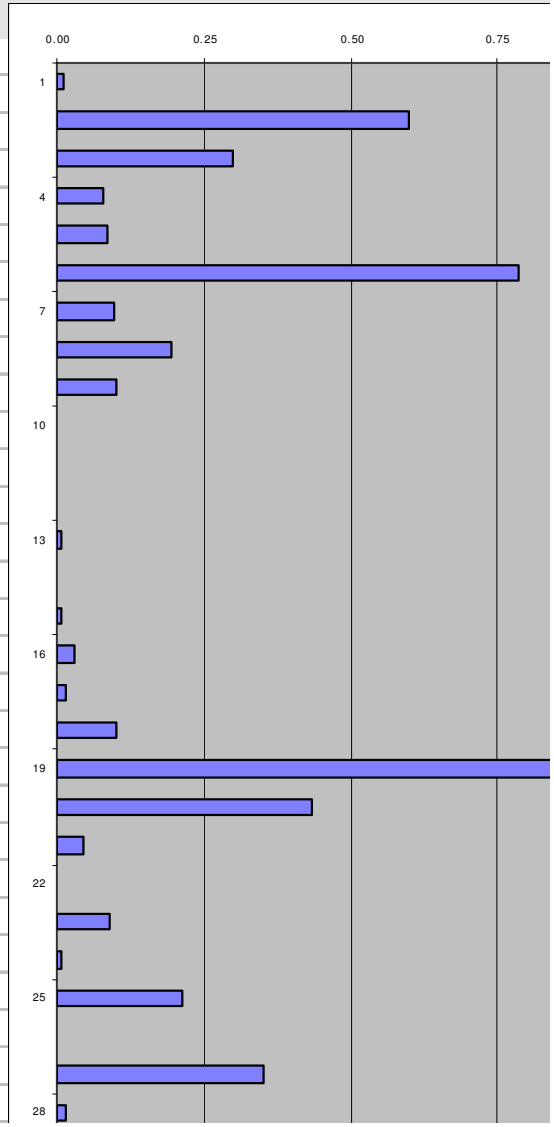


# *MACRO PLANNING*

**See Spreadsheet**
**CYCLE2MOD.XLS**
**See Tools Folder on your CD**

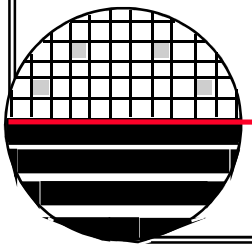


| OPER NAME | TOOL | RAW W/H | UP time % | REWORK % | PLAN W/H | PLAN W/WK | NEED W/WK | Bottleneck STATUS |
|---|---|---|---|---|---|---|---|---|
| ID01 | SCRIBE | 40 | 90 | 5 | 34 | 4104 | 53 | 0.01 |
| PHOTO | STEPPER | 10 | 80 | 5 | 8 | 912 | 547 | 0.60 |
| | TRACK | 20 | 80 | 5 | 15 | 1824 | 547 | 0.30 |
| CL01 | CLEAN | 60 | 99 | 0 | 59 | 7128 | 547 | 0.08 |
| IMP MED | | 20 | 80 | 5 | 15 | 1824 | 158 | 0.09 |
| IMP HIGH | | 1 | 90 | 1 | 1 | 107 | 84 | 0.79 |
| RIE | Poly | 4 | 90 | 0 | 4 | 432 | 42 | 0.10 |
| | Nitride | 4 | 90 | 0 | 4 | 432 | 84 | 0.19 |
| | CC | 4 | 90 | 5 | 3 | 410 | 42 | 0.10 |
| OXIDE | Gate | 100 | 90 | 5 | 86 | 10260 | 11 | 0.00 |
| | Drive | 100 | 90 | 5 | 86 | 10260 | 53 | 0.01 |
| | Anneal | 100 | 90 | 5 | 86 | 10260 | 53 | 0.01 |
| | Kooi | 100 | 80 | 5 | 76 | 9120 | 53 | 0.01 |
| | Pad | 100 | 90 | 5 | 86 | 10260 | 42 | 0.00 |
| | 5000 Wet | 50 | 90 | 5 | 43 | 5130 | 42 | 0.01 |
| DIFF | POLY | 20 | 90 | 5 | 17 | 2052 | 63 | 0.03 |
| | D/S | 20 | 90 | 5 | 17 | 2052 | 32 | 0.02 |
| CVD NITRI | Nitride | 1 | 90 | 5 | 1 | 103 | 11 | 0.10 |
| | Poly | 1 | 85 | 5 | 1 | 97 | 84 | 0.87 |
| | Oxide | 1 | 85 | 5 | 1 | 97 | 42 | 0.43 |
| METAL | | 10 | 85 | 5 | 8 | 969 | 42 | 0.04 |
| ETCH | Oxide | 100 | 90 | 5 | 86 | 10260 | 53 | 0.01 |
| | Metal | 25 | 95 | 5 | 23 | 2708 | 242 | 0.09 |
| STRIP | | 75 | 95 | 5 | 68 | 8123 | 53 | 0.01 |
| GROOVE | | 25 | 90 | 5 | 21 | 2565 | 547 | 0.21 |
| 4PT PROBE | | 100 | 95 | 5 | 90 | 10830 | 32 | 0.00 |
| TEST | | 3 | 100 | 0 | 3 | 360 | 126 | 0.35 |
| SHIP | | 100 | 100 | 0 | 100 | 12000 | 158 | 0.01 |



# *REFERENCES*

1. Motorola's Cycle Time Reduction Handbook, Jack Scholl, et.al.



# *HOMEWORK - CYCLE TIME*

1. **Discuss five reasons why reducing cycle time is good.**
2. **What can be done to reduce cycle time?**
3. **Derive the equation for cycle time shown below**

$$\text{Cycle Time} = \frac{2\,(\text{WIP})\,(\text{T})}{\text{t}\,(1+\text{Y})}$$

4. **Give an example of split-the-wip (not the same as in the notes).**
5. **Using a spread sheet model similar to that shown in CYCLE2MOD.XLS investigate setting up a factory for 5000 wafers per week.**