ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Hand Calculations for RIT's Advanced CMOS Process

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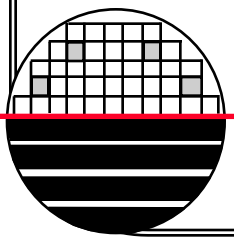
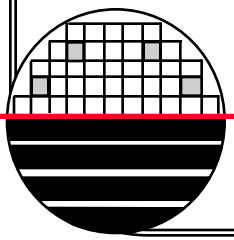


OUTLINE

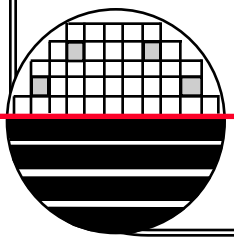
Introduction
Calculations



INTRODUCTION

RIT is supporting two different CMOS process technologies. The older p-well CMOS and SMFL-CMOS have been phased out. The SUB-CMOS process is used for standard 3 Volt Digital and Analog integrated circuits. This is the technology of choice for teaching circuit design and fabricating CMOS circuits at RIT. The ADV-CMOS process is intended to introduce our students to process technology that is close to industry state-of-the-art. This process is used to build test structures and develop new technologies at RIT.

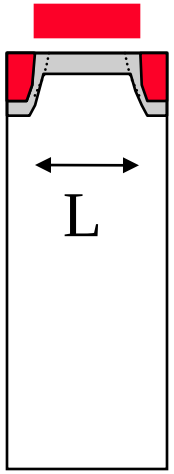
RIT p-well CMOS	$\lambda = 4\ \mu m$	Lmin = 8 µm
RIT SMFL-CMOS	$\lambda = 1\ \mu m$	Lmin = 2 µm
RIT Subµ-CMOS	$\lambda = 0.5\ \mu m$	Lmin = 1.0 µm
RIT Advanced-CMOS	$\lambda = 0.25\ \mu m$	Lmin = 0.5 µm



RIT ADVANCED CMOS VER 150

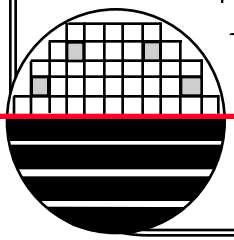
RIT Advanced CMOS

150 mm Wafers
Nsub = 1E15 cm-3 or 10 ohm-cm, n or p
Nn-well = 1E17 cm-3
Xj = 2.5 µm
Np-well = 1E17 cm-3
Xj = 2.5 µm
Shallow Trench Isolation
Field Ox = 4000 Å
Dual Doped Gate n+ and p+
Xox = 100 Å
Lmin= 0.5 µm
LDD/Nitride Side Wall Spacers
TiSi2 Silicide
Tungsten Plugs, CMP, 2 Layers Aluminum

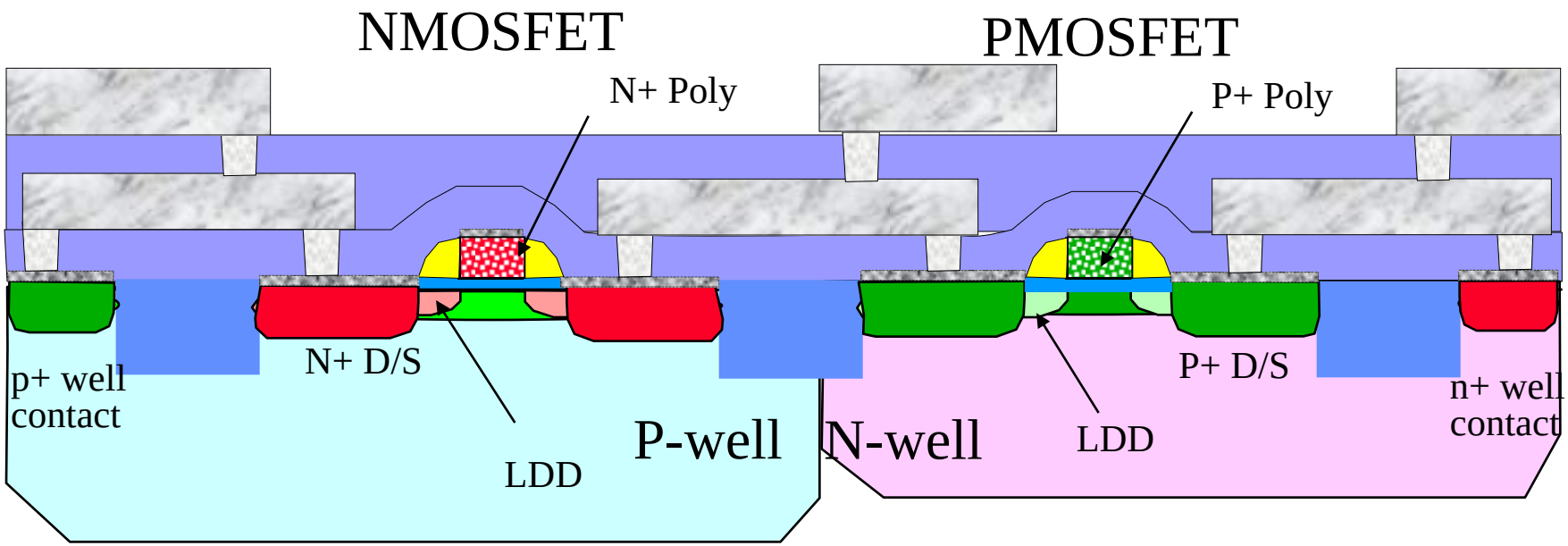


Long Channel Behavior

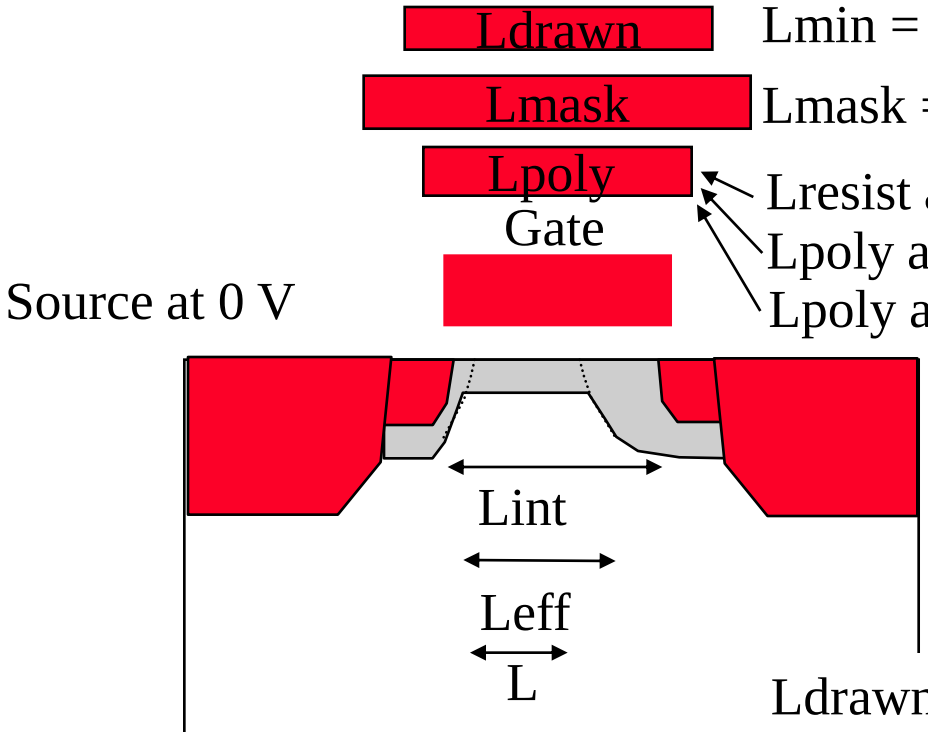
Supply = 3 Volt
Vth = +/- 0.75 Volts



RIT ADVANCED CMOS



LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L



Lambda = design rule parameter, λ, ie 0.25µm

Lmin = min drawn poly length, 2λ 0.50µm

Lmask = ? Depends on +/-bias 1.00µm x 5

Lresist after photo (resist trimming??) 0.50µm

Lpoly after poly etch 0.40µm

Lpoly after poly reoxidation 0.35µm

0.30µm

0.20µm

0.11µm

Ldrawn = what was drawn

Internal Channel Length, Lint =distance between junctions, including under diffusion

Effective Channel Length, Leff = distance between space charge layers,Vd = Vs= 0

Channel Length, L, = distance between space charge layers, when Vd= what it is

Extracted Channel Length Parameters = anything that makes the fit good (not real)

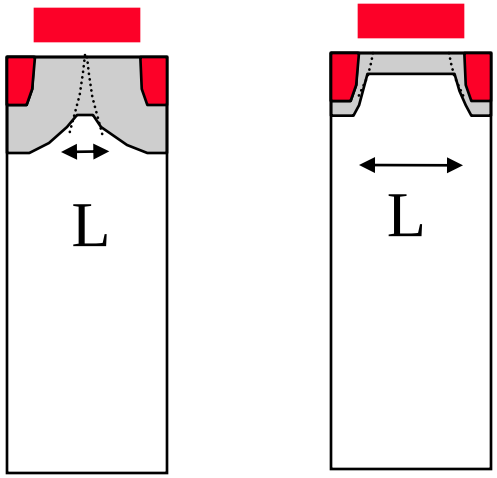
CALCULATION OF SC LAYER SIZE, ELECTRIC FIELD

Width of Space Charge Layer:

$$W = (W_1 + W_2) = [(2\varepsilon/\theta)(\Psi_o + V_R)(1/N_A + 1/N_D)]^{1/2}$$

Maximum Electric Field:

$$E_o = -[(2q/\varepsilon)(\Psi_o + V_R)(N_A N_D/(N_A + N_D))]^{1/2}$$



Let $N_A = N_D = 1E17$

Well Doping	Bias (volts)	SC Layer (µm)	Efield (V/cm)
1E17	0	0.07	-1.09E5
1E17	3	0.14	-2.42E5

Breakdown Electric Field = 3E5 V/cm

$\varepsilon = \varepsilon_o \varepsilon_r = 8.85E\text{-}12\ (11.7)$ F/m
8.85E-14 (11.7) F/cm

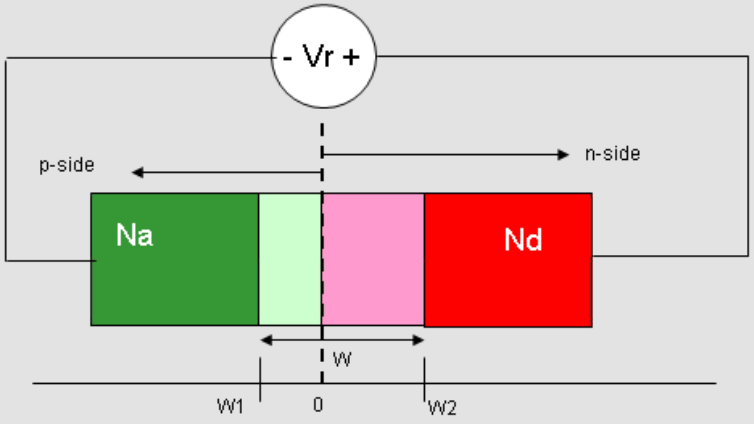
USING EXCEL SPREADSHEET FOR CALCULATIONS

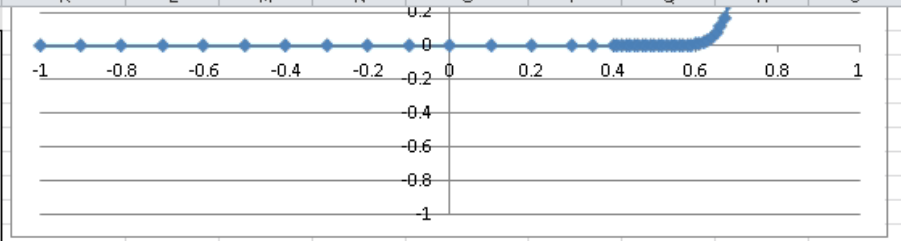
pn_ electrostatics_currnet_temp.xls

CONSTANTS			VARIABLES	
K	1.38E-23	J/K		
q	1.60E-19	Coul	Temp= 300	°K
Ego	1.12	eV		
so	8.85E-14	F/cm	Nd = 1.00E+17	cm-3
sr	11.7		Na = 1.00E+17	cm-3
ni	1.45E+10	cm-3		
Breakdown E=	3.00E+05	V/cm	Vr = 0	Volts Reverse Bias Voltage

CALCULATIONS:

Eg = Ego - (aT^2/(T+B)	1.075	eV
ni^2 = A T^3 e^(-Eg/KT/q)	9.84E+20	cm-6
KT/q =	0.0259	Volts
Vbi = (KT/q) ln (NaNd/ni2)	0.78	Volts
W = [(2s/q)(Vbi+Vr)(1/Na +1/Nd)]^0.5	0.14	µm
W1 =W[Nd/(Na+Nd)]	0.07	µm
W2 =W[Na/(Na+Nd)]	0.07	µm
Eo = -[(2q/eoer)(Vbi+Va)(NaNd/(Na+Nd)]^0.5	-1.09E+05	V/cm
Cj' = eoer/W	7.31E-08	F/cm2





$Id = Is\,(e^{qV/KT} - 1)$

$Is = CT^2 \exp^{(-qEg/KT)}$

Is = 9.73E-13

V	Id
-1	-9.72785E-13
-0.9	-9.72785E-13
-0.8	-9.72785E-13
-0.7	-9.72785E-13
-0.6	-9.72785E-13
-0.5	-9.72785E-13
-0.4	-9.72784E-13
-0.3	-9.72776E-13
-0.2	-9.72355E-13
-0.1	-9.52349E-13
0	0
0.1	4.53343E-11
0.2	2.20336E-09
0.3	1.04931E-07
0.35	7.23973E-07
0.4	4.99503E-06
0.41	7.35024E-06
0.42	1.08159E-05
0.43	1.59158E-05
0.44	2.34202E-05
0.45	3.4463E-05
0.46	5.07127E-05
0.47	7.46242E-05
0.48	0.00010981
0.49	0.000161587
0.5	0.000237776

HAND CALCULATIONS FOR ADV-CMOS WELL

The well implant dose is estimated from the selected values of well doping and junction depth of 2.5µm.

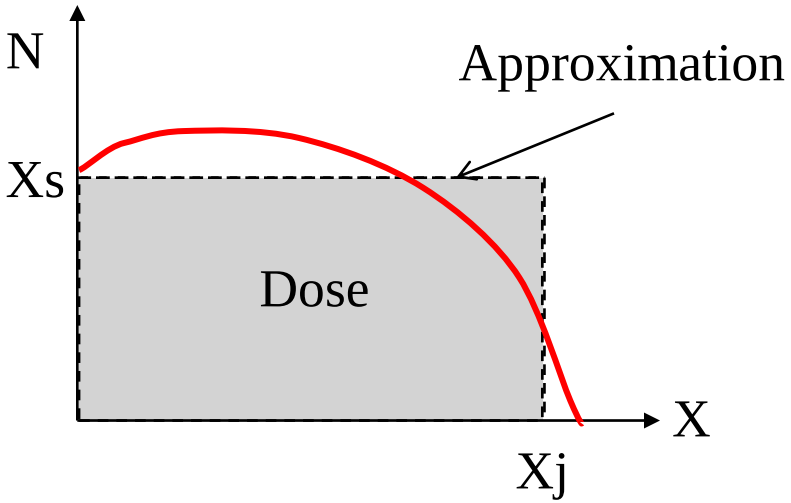
The dose is the total number of impurity atoms per cm2 in the well.

$$\text{Dose} = \int N_{well}\, dx = N_{well}\, X_j$$ if we assume the well is uniformly doped as Ns from the surface x=0 to the junction x=Xj

$$= N_s \times X_j$$

$$= (1E17\ cm^{-3})\ (2.5E\text{-}4\ cm)$$

Dose = 2.5 E 13 cm^{-2}



HAND CALCULATIONS FOR ADV-CMOS WELL

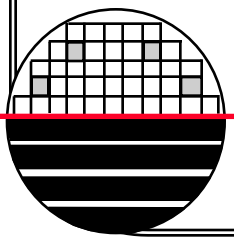
Well calculations for junction depth, well sheet resistance, well surface concentration and average well doping

Given: Dose=2.5E13, Drive-in Time=6 Hrs Drive in Temp = 1100 C
Starting wafer 1E15 cm-3 from 10 ohm-cm

$$N(x,t) = \frac{Q'_A(tp)}{\sqrt{\pi Dt}} \text{Exp}\ (- x^2/4Dt)$$

Surface concentration

Nave = Dose/xj



WELL DRIVE CALCULATIONS

Implant.xls

GIVEN		VALUE	UNITS
Starting Wafer Resistivity	Rho =	10	ohm-cm
Starting Wafer Type	n-type = 1	0	1 or 0
	p-type = 1	1	1 or 0
Pre Deposition Ion Implant Dose		2.50E+13	ions/cm2
Drive-in Temperature		1100	°C
Drive-in Time		360	min

CALCULATE	VALUE	UNITS
Diffusion Constant at Temperature of Drive-in	1.33E-13	cm/sec

CALCULATION OF DIFFUSION CONSTANTS

	D0 (cm2/s)	EA (eV)
Boron	0.76	3.46
Phosphorous	3.85	3.66

CALCULATIONS	VALUE	UNITS
Substrate Doping = 1 / (q μmax Rho)	1.33E+15	cm-3

RESULTS	VALUE	UNITS
Pre deposition Dose	2.50E+13	atoms/cm2
xj after drive-in = ((4 Dd td/QA) ln (Nsub (πDdtd)^0.5))^0.5	2.47	μm
average doping Nave = Dose/xj	1.01E+17	atoms/cm3
mobility (μ) at Doping equal to Nave	718	cm2/V-s
Sheet Resistance = 1/(q (μ(Nave))Dose)	348.2	ohms
Surface Concentration = Dose/ (pDt)^0.5	2.63E+17	cm-3

WELL CALCULATIONS

Given	Ns = 1E17cm-3	Xj=2.5 µm			Dose= 2.5E13 cm^{-2}	Well Drive =6hr,1100C
Calculated	Ns	Xj	Nave cm-3	Rhos Ω		
N-well	2.63E17	2.47	1.01E17	348		
P-well	2.54E17	2.80	8.93E16	768		
Photoresist	13000Å		Boron Emax	105KeV	Phos Emax	210KeV
Oxide	4000Å		Boron Emin	80KeV	Phos Emin	120KeV

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

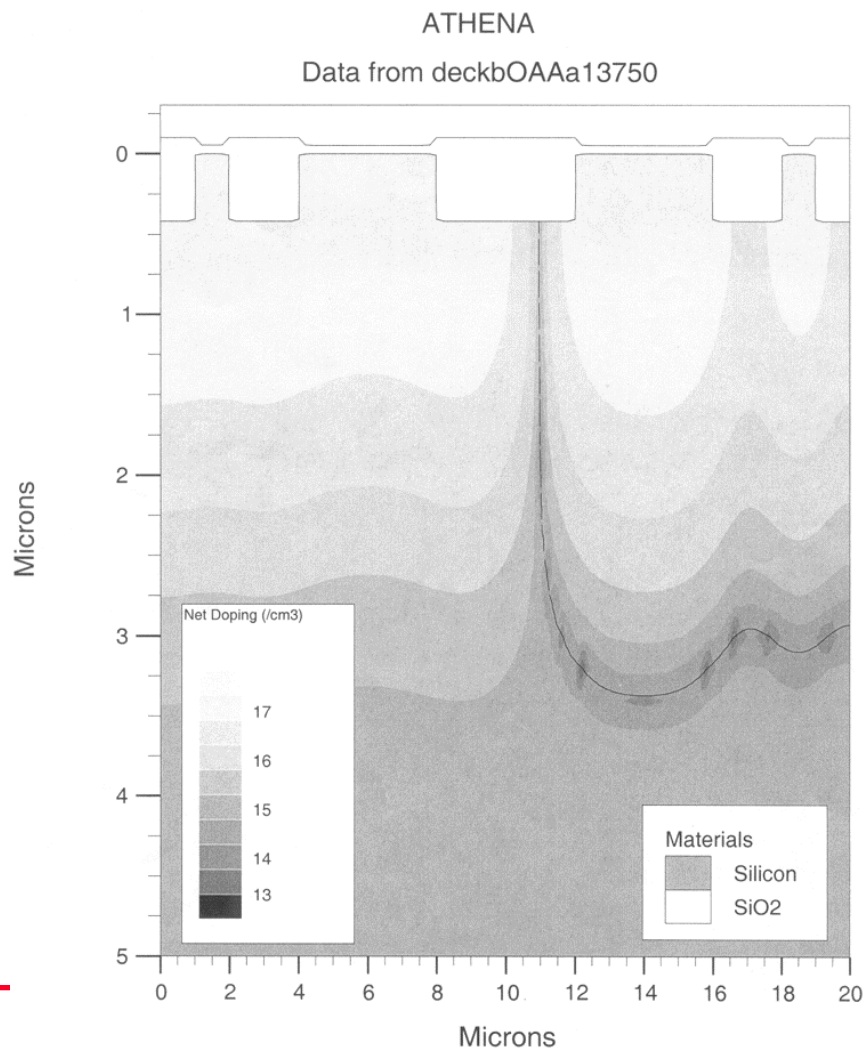
DOPANT SPECIES		MASK TYPE		ENERGY	
B11	1	Resist	1	105	KeV
BF2	0	Poly	0		
P31	0	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 12753.72 Angstroms

SILVACO ATHENA WELL SIMULATION

P-well
Dose=7.0E13
Energy=120KeV
Drive 6 hr, 1100 C
Find:
Nsurface=1E17
Nsti=1E17
Xj=3.0 um

N-well
Dose=3E13
Energy=170KeV
Drive 6 hr, 1100 C
Find
Nsurface=1E17
Nsti=2E16
Xj=3.0um



HAND CALCULATIONS FOR ADV-CMOS OXIDE

Oxide Growth Calculations

Step 4 - Pad oxide 1/3 nitride thickness so oxide target is 500 Å
55 min at 1000 C dry O2 gives 500 Å, Recipe 250

Step 10 – Pad Oxide Trench Liner, **500Å, Recipe 250**

Step 23 - Well Drive is in Nitrogen: **no oxide growth, Recipe 11**

Step 30 - Gate Oxide 100Å, **40 min at 900 C dry O2, Recipe 213**
Fowler/Nordheim Tunneling Consideration: **3 volt power supply and max field of 4E6 V/cm gives Xox min of 75 A, pick 100 A for gate oxide target thickness**

Step 36 - Poly Reox, **500 Å, Recipe 250**

Step 52 - DS Anneal will be in N2: **no oxide growth, 900C for 30 min., Recipe ???**

Step 67 – Sinter, **Recipe 101 no oxide growth**

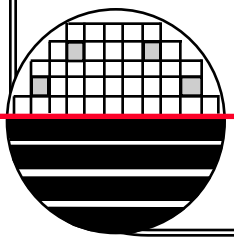
HAND CALCULATIONS FOR ADV-CMOS POLY

Poly Thickness and Sheet Resistance Calculations

Poly thickness needs to mask D/S implants (see next page)
Target should be 4000 Å, USL 4500 Å, LSL 3500 Å

Rhos=1/(qμDose) and Dose is 4E15 for both, μ=20 and 10

Poly Doping by Ion Implant, N+, Rhos=78 ohms
Poly Doping by Ion Implant, P+, Rhos=156 ohms



DRAIN/SOURCE IMPLANT ENERGY CALCULATIONS

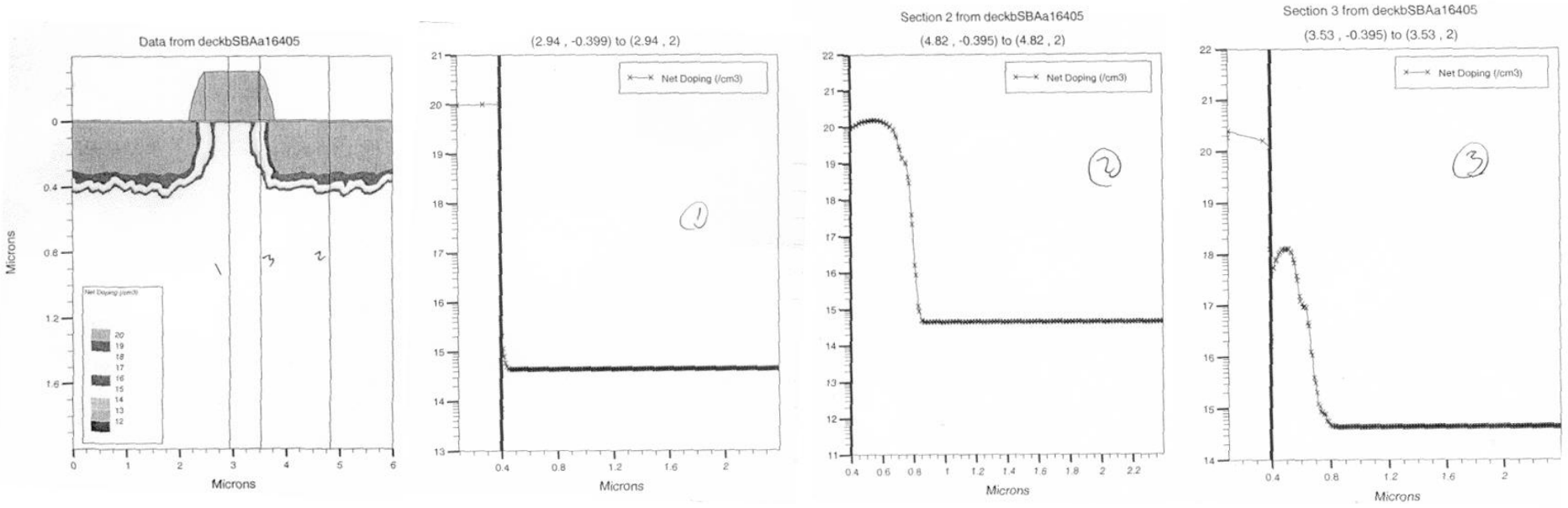
		B11	P31		
	Min Thickness	E max	E max	E used	E used
Resist	13000 Å	105	210		
Poly	3500 Å	50	80	50	50
Oxide	4000 Å	75	115		
Nitride	3000 Å	95	145		

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		MASK TYPE		ENERGY	
B11	0	Resist	0	80	KeV
BF2	0	Poly	1		
P31	1	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 3417.1483 Angstroms

SILVACO ATHENA SIMULATIONS OF D/S IMPLANT



These simulations show that 3000 A of poly and nitride spacer is enough to block P31 implants from reaching the channel (region 1), the n+ D/S implant profile is shown in region 2, the LDD n- D/S implant profile is shown in region 3, both after 900 C, 30 min anneal. Note doping ~1E20 in D/S and ~1E18 in LDD/LDS and xj ~ 0.6 µm

HAND CALCULATIONS FOR ADV-CMOS D/S

D/S Sheet Resistance and Junction Depth Calculations

(Rhos=1/(quDose)), Xj depends on implant energy so Xj~0.2

N-LDD implant dose 4E13 and 50KeV, μ=100, Rhos=1250 ohms

N+ D/S implant dose 4E15 and 50 KeV, μ=100, Rhos=12.5 ohms

P-LDD implant dose 4E13 and 50 KeV, μ=75, Rhos=1667 ohms

P+ D/S implant dose 4E15 and 50 KeV, μ=75, Rhos=16.7 ohms

Silicide Consideration: will reduce sheet resistance to as low as 5 ohms

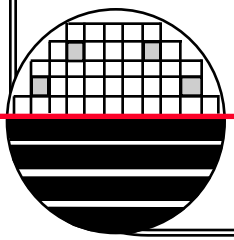
Drain Source Space Charge Layer Calculations

N-D/S using Nd=1E18, Na=1E17 gives W=0.10um at 0V and W=0.21um at 3V

N+D/S using Nd=1E20, Na=1E17 gives W=0.11um at 0V and W=0.23um at 3V

P-D/S using Na=1E18, Nd=1E17 gives W=0.10um at 0V and W=0.21um at 3V

P+D/s using Na=1E20, Nd=1E17 gives W=0.11um at 0V and W=0.23um at 3V

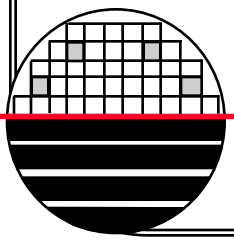


HAND CALCULATIONS FOR ADV-CMOS VT

Threshold Voltage Calculations, target +0.75 and –0.75 volts

N-MOSFET VT, Nss=1E11, Xox=100 A, Na=1E17, VT=0.25, Wdmax=.103um
Dose=1.07E12 x 2 = 2.15E12 Boron
P-MOSFET VT, Nss=1E11, Xox=100 A, Nd=1E17, VT=-0.34, Wdmax=.103um
Dose=8.76E11 x 2 = 1.75E12 Phosphorous

N-Field VT, Nss=1E11, Xox=4000 A, Na=1E17, VT=17 volts
P-Field VT, Nss=1E11, Xox=4000 A, Nd=1E17, VT=-20 volts
No channel stop needed



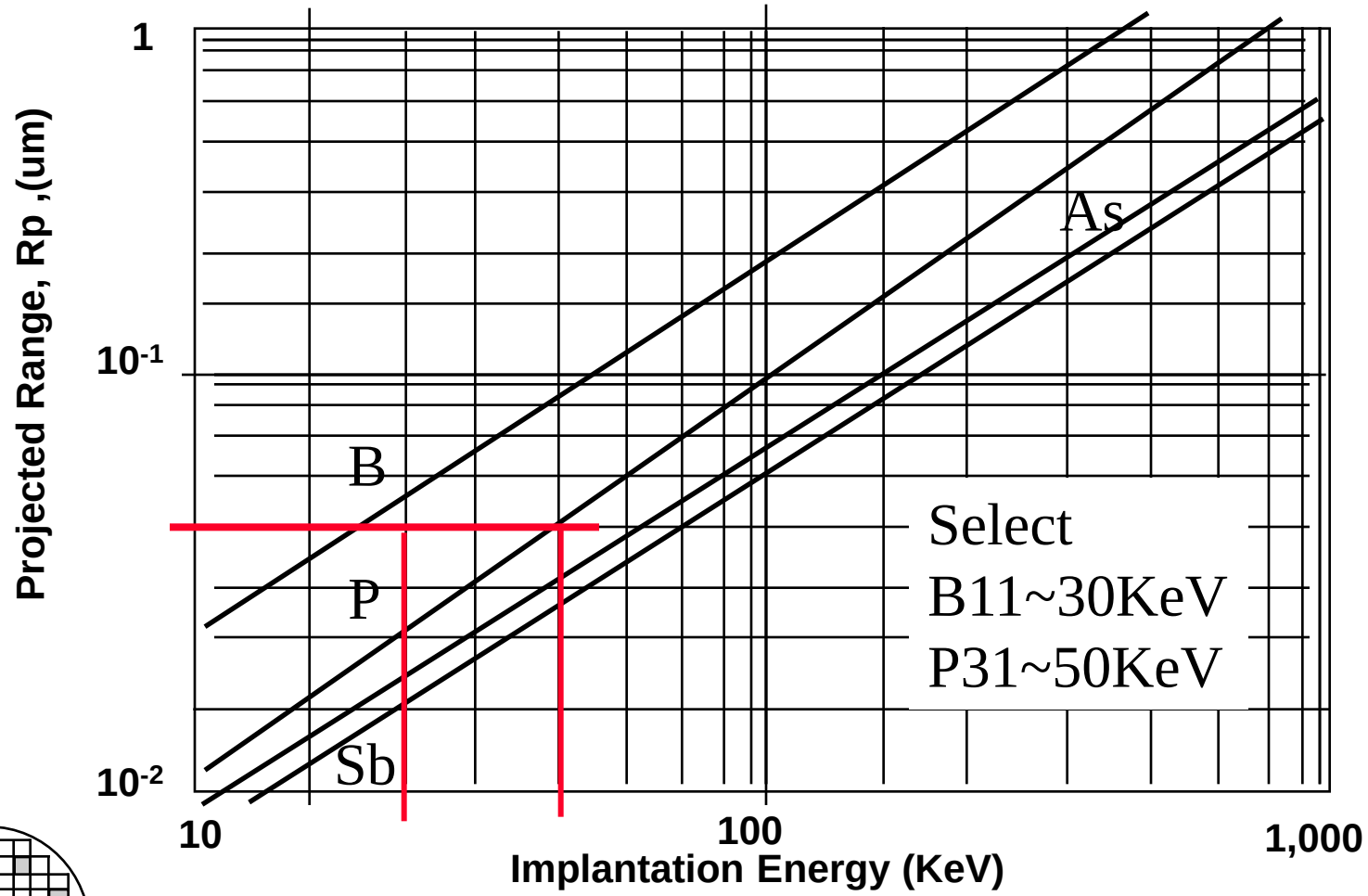
VT CALCULATIONS

CONSTANTS			VARIABLES			CHOICES		
							1=yes, 0=No	
T=	300	K	Na =	1.00E+17	cm-3	Aluminum gate	0	} Select one type of gate
KT/q =	0.026	volts	Nd =	1.00E+17	cm-3	n+ Poly gate	1	
ni =	1.45E+10	cm-3	Nss =	1.00E+11	cm-2	p+ Poly gate	0	
Eo =	8.85E-14	F/cm	Xox =	100	Ang	N substrate	0	} Select one type of substra
Er si =	11.7					P substrate	1	
Er SiO2 =	3.9							
E affinity =	4.15	volts				Desired VT	0.75	
q =	1.60E-19	coul				or		
Eg =	1.124	volts				Delta VT	20	
						Given Dose (Boron)	1.30E+12	

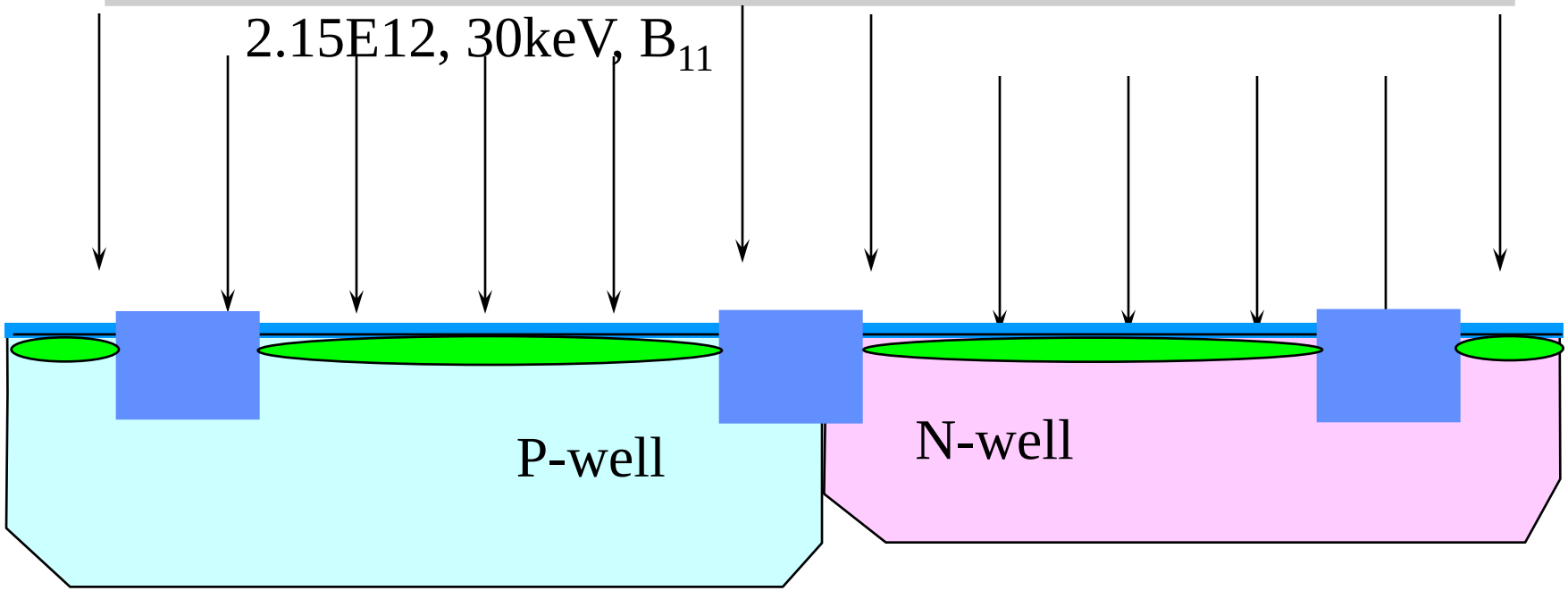
CALCULATIONS:

		RESULTS				
METAL WORK FUNCTION	=	4.122988528	volts			
SEMICONDUCTOR POTENTIAL	= +/-	0.409409834	volts			
OXIDE CAPACITANCE / CM2	=	3.4515E-07	F/cm2	Wdmax =	0.103	µm
METAL SEMI WORK FUNCTION DIFF	=	-0.998421306	volts			
FLAT BAND VOLTAGE	=	-1.044777963	volts			
THRESHOLD VOLTAGE	=	0.25126959	volts			
DELTA VT = VTdesired - VT	=	0.49873041	volts			
IMPLANT DOSE	=	1.07586E+12	ions/cm2	x 2 =	2.15171E+12	
		where + is Boron, - is Phosphorous				
IMPLANT DOSE FOR GIVEN Delta VT	=	4.31438E+13	ions/cm2	x 2 =	8.62875E+13	
Vt WITH GIVEN DOSE	=	0.552587857	volts	assume 1/2 dose in Si		

ION IMPLANT RANGE

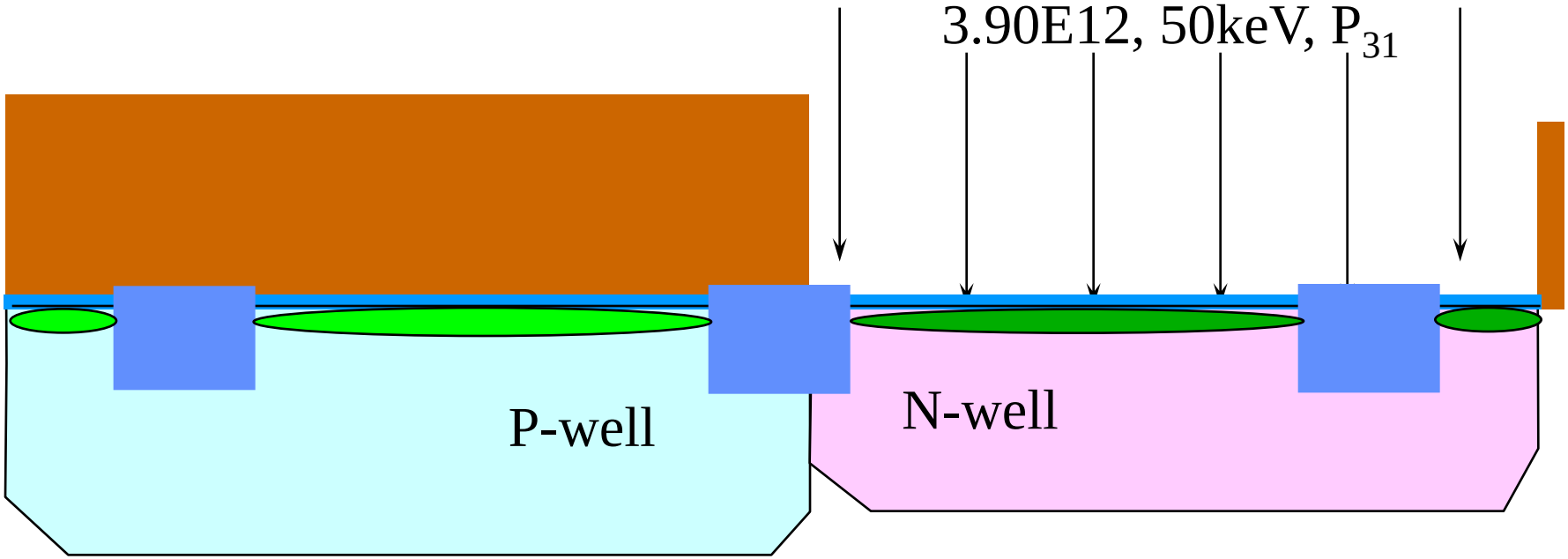


BLANKET PMOS & NMOS VT ADJUST IMPLANT

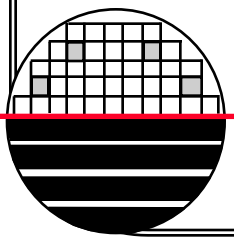


Substrate 10 ohm-cm

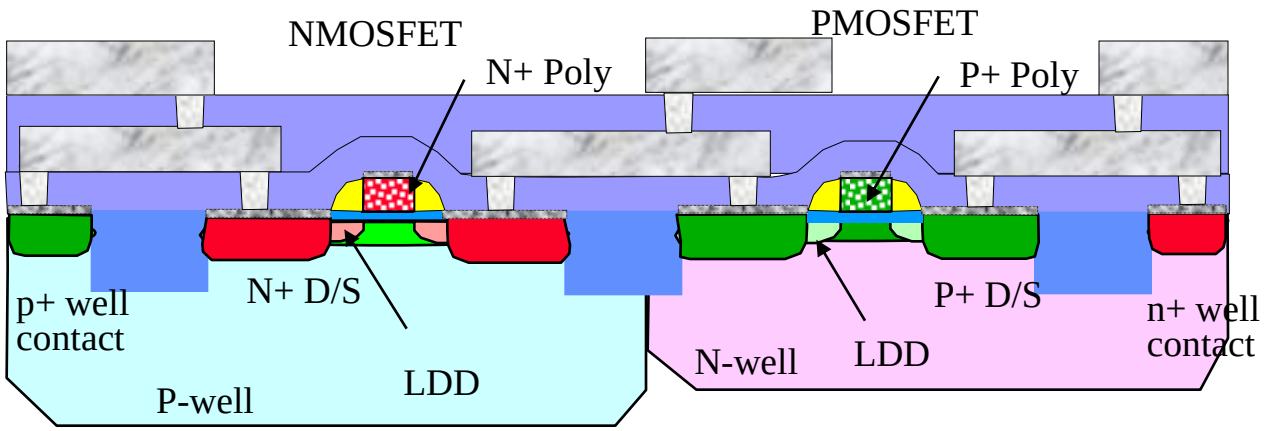
PMOS VT IMPLANT

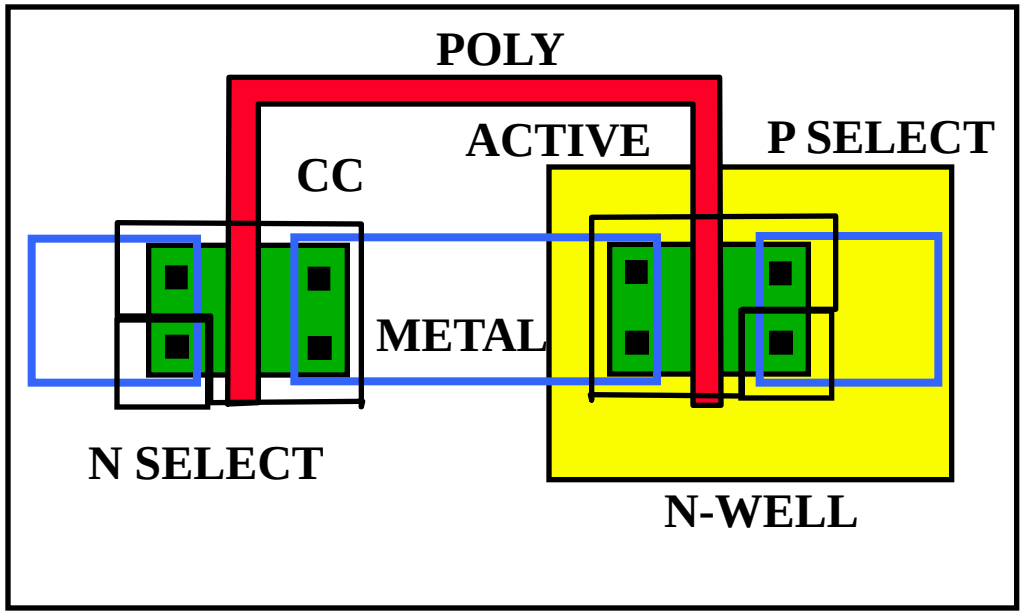


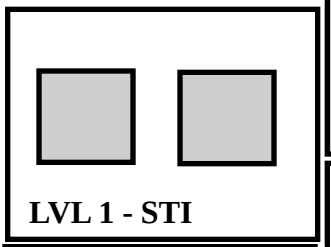
Substrate 10 ohm-cm

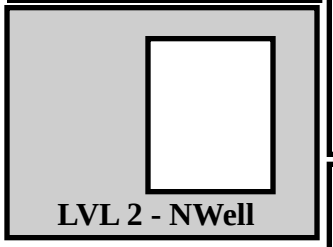


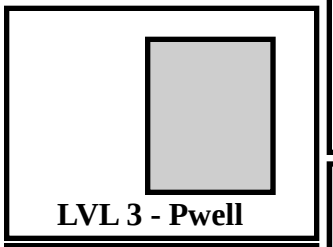
RIT ADVANCED CMOS PROCESS

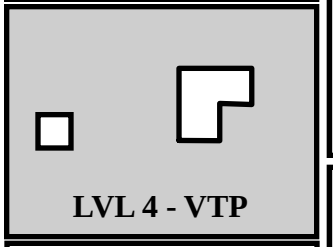


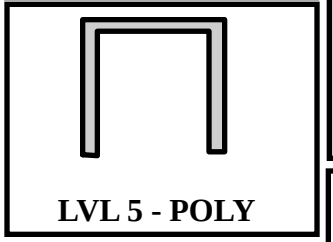




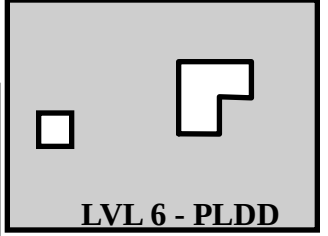


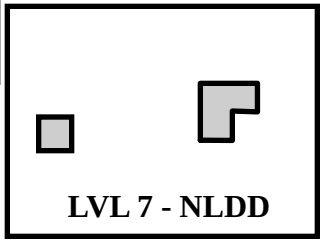


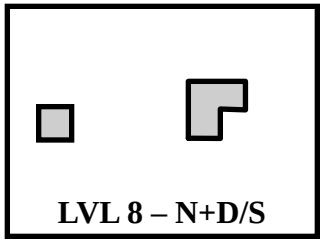


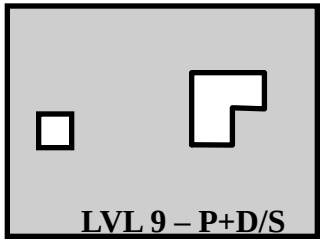


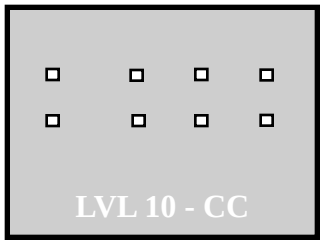
11 PHOTO LEVELS

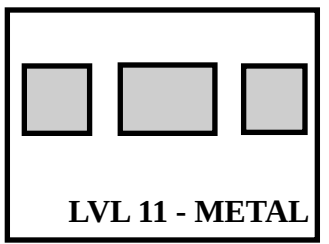












ADV-CMOS 150 PROCESS

CMOS Versions 150, one level Metal

1. ID01
2. DE01
3. CL01
4. OX05--- pad Ox 500A, 1000C, 45min
5. CV02- 1500 Å, ~30min
6. PH03 –1- STI
7. ET29 etch shallow trench, 4000A
8. ET07-ash
9. CL01
10. OX05 – pad oxide, 500 A
11. CV03 – CVD oxide trench fill

11.1 OX07 - Anneal

12. CM01 – Trench CMP
13. CL02 - CMP_Clean
14. CL01-rca clean
15. ET19 hot phos
16. PH03-2-n-well, 1.3um thick resist
17. IM01 3E13, P31, 180 KeV
18. ET07-ash
19. PH03 – 3 – p-well
20. IM01 – 3E13, B11, 150KeV
21. ET07 -ash
22. CL01
23. OX06 well drive, 6hr 1100C
24. IM01 blanket implant
25. PH03 – 4 - VT adjust
26. IM01 adjust
27. ET07
28. CL01
29. ET06 oxide etch
30. OX06 gate oxide
31. CV01 poly dep
32. PH03 - 5 - poly
33. ET08 poly etch
34. ET07

35 CL01

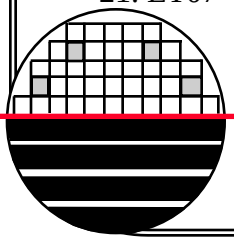
36 OX05 pad oxide

37. PH03 –6- p LDD
38. IM01 p LDD
39. ET07
40. PH03 –7- n LDD
41. IM01 n LDD
42. ET07
43. CL01
44. CV02 nitride spacer dep
45. ET39 spacer etch
46. PH03 – 8 - N+D/S
47. IM01 – N+D/S
48. ET07
49. PH03 – 9- P+ D/S
50. IM01 – P+ D/S
51. ET07
52. CL01
53. OX08 – DS Anneal
54. ME03 HF dip & Co/Ti
55. RT01
56. ET11 Ti Etch
57. RT02
58. CV03 – LTO
59. PH03 – 10 CC
60. ET10
61. ET07
62. CL01

62.1 CV04 W Plugs

63 ME01 Aluminum

64. PH03 -11- metal
65. ET15 plasma Al Etch
66. ET07
67. SI01
68. SEM1
69. TE01
70. TE02
71. TE03
72. TE04



ETCH RATES

STI etch rates 1000A/min Nitride, 500A/min Oxide, 5000A/min Si, 1000A/min PR

Hot Phos Nitride Etch Rate 80A/min, 45 min to etch 1500A nitride

Poly Etch Lam 490, Gap 1.5, 325 mTorr, 140 w, 150 sccm SF6, 15sccm O2, rate=6000Å/min

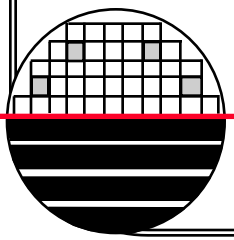
Sidewall spacer etch, Power=250 Watts, Pressure=40 mTorr, SF6=30 sccm, CHF3=30 sccm, Nitride Etch Rate=1250 A/min, Nitride Etch %NU ~ 4%, Oxide Etch Rate~ 950 A/min Oxide Etch %NU~ 10% , Selectivity Nitride:Oxide 1.3:1

H2SO4/H2O2 (1:2) Ti etch for silicide, at 100°C (set plate temperature to 150°C), Rate ~500Å/min

Aluminum Etch Rate LAM4600 ~10,000Å/min.

DEPOSITION RATES

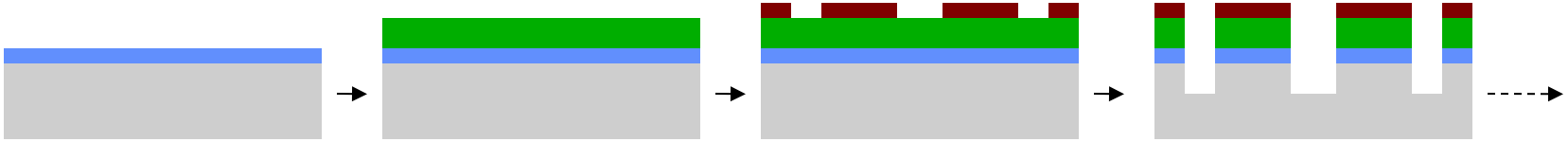
LPCVD Nitride dep rate at 810°C = 50 A/min.
1500 Å for STI Stop, time = 30 min
4000 Å for Side Wall Spacer = 80 min
PECVD TEOS Oxide dep rate 91A/sec
10,000 Å trench fill
4000 Å for contact cuts
LPCVD Poly dep rate at 610°C = 75 Å/min
4000 Å gate deposition time = 53 min.
Aluminum Sputter dep rate at 2000 w = 300Å/min.
7500 Å metal one dep time = 25 min
Ti Sputter dep rate, 4" target, 350w, 5mTorr = 100Å/min
700 A Ti dep time = 7 min
Ti Sputter dep rate, 8" target, 750w, 5mTorr=176Å/min.
700 A Ti dep time = 4 min



ADV-CMOS PHOTO

Level Name	Coat Recipe	Coat Xpr µm	Dose mj/cm2	Develop Recipe	Dev Time	Post Bake Time at 140°C
STI	Coat.rcp	1.0	160	develop.rcp	50s	1 min.
N-well	Coatmtl.rcp	1.3	185	Devmtl.rcp	75s	2 min.
P-well	Coatmtl.rcp	1.3	185	Devmtl.rcp	75s	2 min.
Vtn	Coat.rcp	1.0	185	DevFac.rcp	180s	1 min.
Vtp	Coat.rcp	1.0	185	DevFac.rcp	180s	1 min.
Poly	Coat.rcp	1.0	160	develop.rcp	50s	1 min.
Ldd P	Coat.rcp	1.0	160	develop.rcp	50s	1 min.
Ldd N	Coat.rcp	1.0	160	develop.rcp	50s	1 min.
N+ D/S	Coat.rcp	1.0	160	develop.rcp	50s	1 min.
P+ D/S	Coat.rcp	1.0	160	develop.rcp	50s	1 min.
CC	Coat.rcp	1.0	260	DevFac.rcp	180s	1 min.
Metal 1	Coatmtl.rcp	1.3	160	Devmtl.rcp	75s	2 min.

ORIGINAL ADV-CMOS PROCESS FLOW

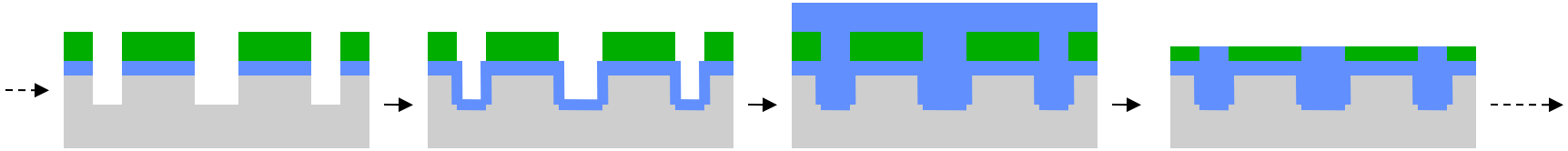


500Å Pad Ox.
-Bruce Tube 4

1500Å CVD Nitride
-LPCVD

STI Litho- level 1

4000Å Plasma etch
-Lam 490

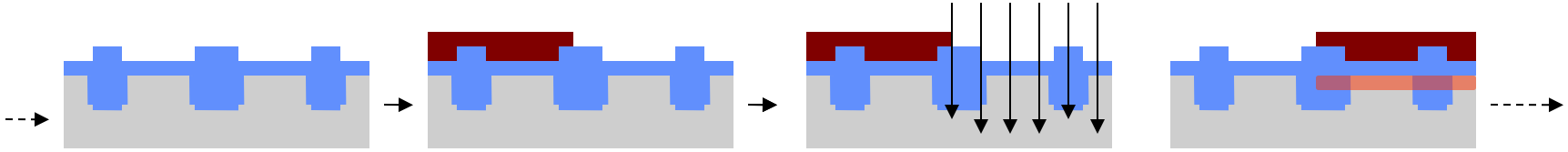


PR Ash
RCA Clean

500Å Pad Oxide
-Bruce Tube 1

CVD Trench fill- P-5000
Anneal –Bruce Tube 1

Trench CMP
CMP Clean

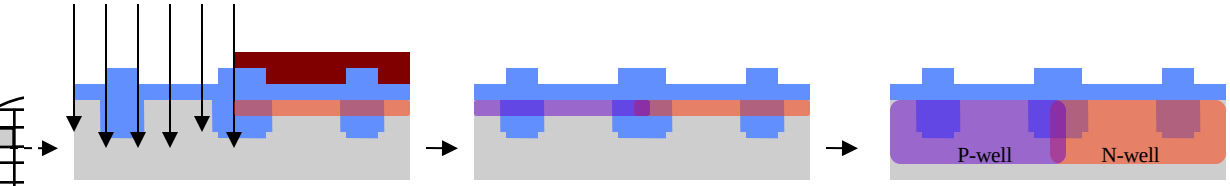


RCA Clean
Hot Phos. Nitirde strip

N-well Litho
-Level 2

N-well implant
-P31, 3E13 cm^{-2} E=180KeV

Ash
P-well Litho - level 3

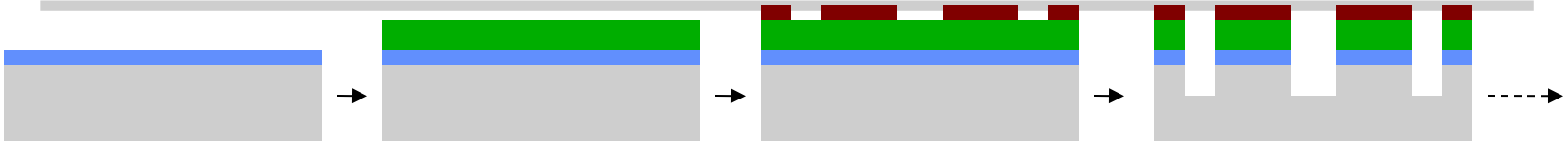


P-well implant
-B11, 3E13 cm^{-2} E=150KeV

Ash, RCA clean
Drive in- 6hr 1100C-Tube 1

X_j approx. 3 μm

PROPOSED ADV-CMOS PROCESS FLOW

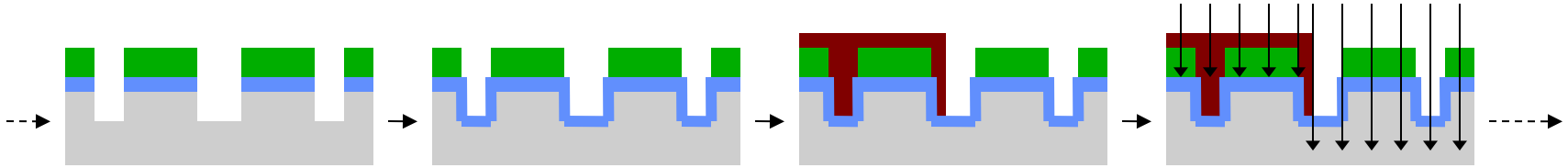


500Å Pad Ox.
-Bruce Tube 4

1500Å CVD Nitride
-LPCVD

STI Litho- level 1

4000Å Plasma etch
-Lam 490

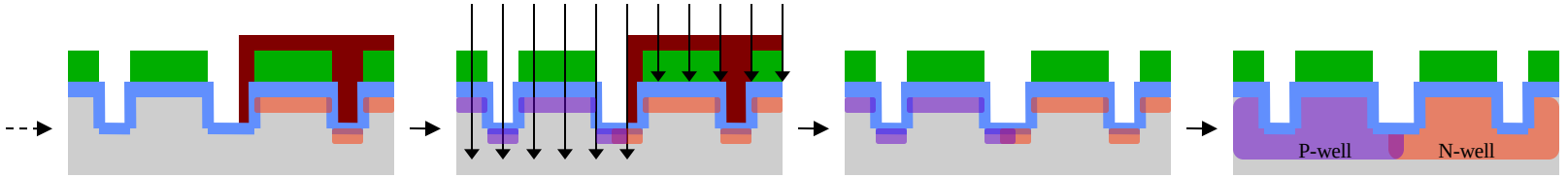


PR Ash
RCA Clean

500Å Pad Oxide
-Bruce Tube 1

N-well Litho
-Level 2

N-well implant
-P31, 8e13 cm^{-2} E=80 KeV

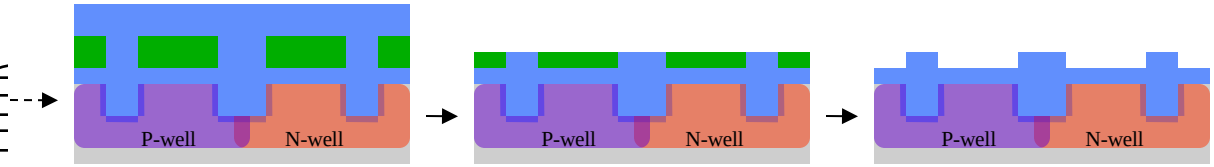


P-well Litho
-Level 3

P-well implant
-B11, 3e13 cm^{-2} E=170 KeV

PR Ash
RCA Clean

Drive in- 6hr 1100˚C-Tube 1
X_j approx. 3 µm



CVD Trench fill- P-5000
Anneal –Bruce Tube 1

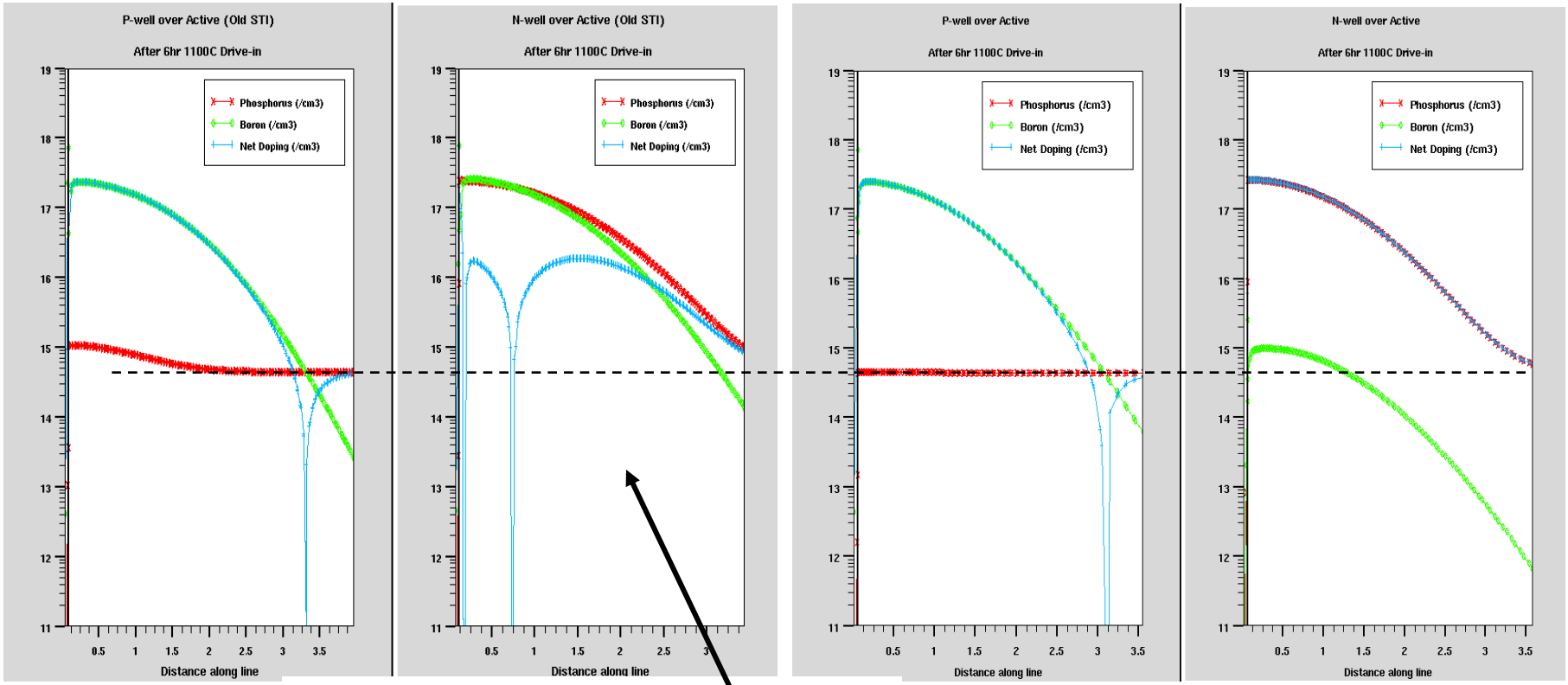
Trench CMP
CMP Clean

RCA Clean
Hot Phos. Nitirde strip

SIMULATION: ORIGINAL PROCESS WELL PROFILES

Current Process

Proposed Process



Problems with Boron Penetration of Masking Resist

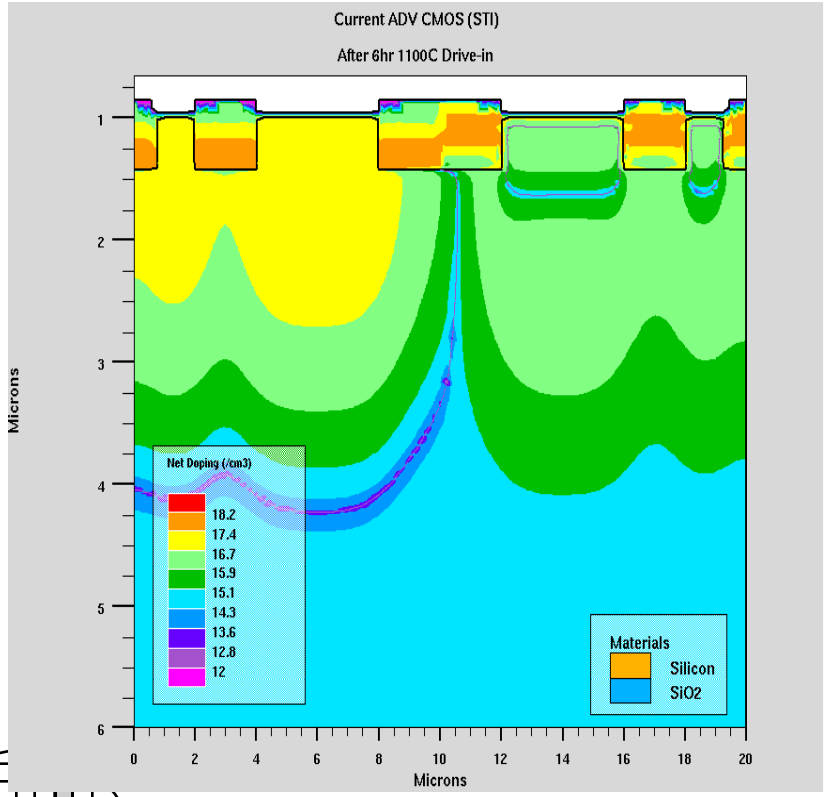
WELL PARAMETERS

	Design Parameters	Old Process Simulation	New Process Simulation	
N well				
Dose	3E13	3E13	3E13	
Energy		180	170	Lower
Surface Conc.	~1E17	2.4E17	1.0E17	Better
N well Xj	~3.0	4.0#	3.5	Better
P well				
Dose	3E13	3E13	7E13	
Energy		150	120	Lower
Surface Conc.	~1E17	3.6E16	1.0E17	Better
P well Xj	~3.0	3.3	3.1	Better

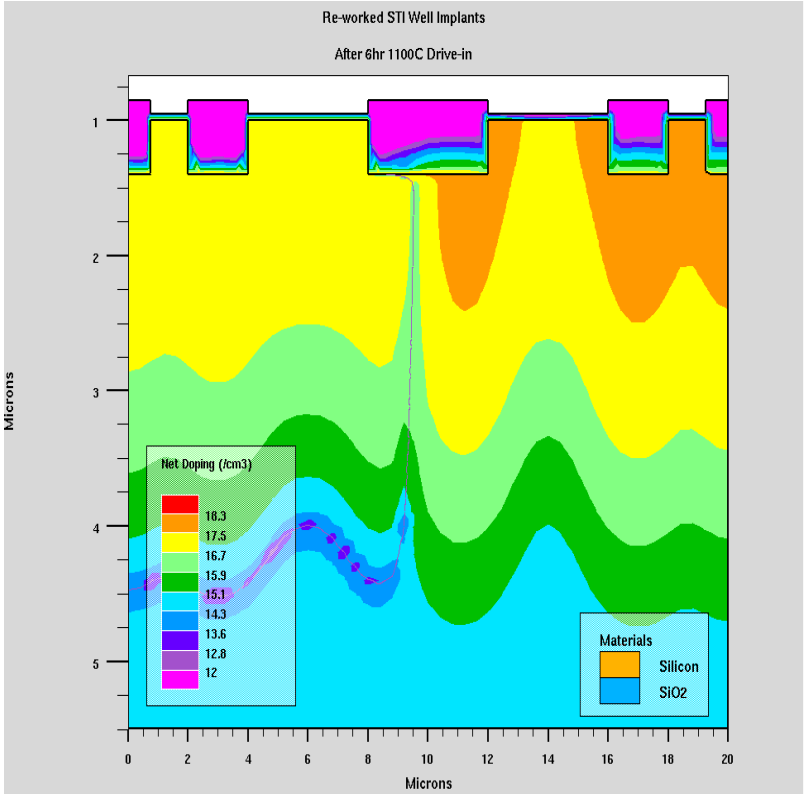
If Boron penetration into N-well can be eliminated with thicker photoresist

SIMULATION: PROCESS CROSS-SECTION

Current Process



Proposed Process

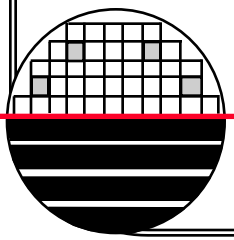


TARGET, USL AND LSL

	Unit	LSL	Target	USL
Pad Oxide	Å	400	500	600
Nitride 1	Å	1000	1500	2000
Nitride 2	Å	3500	4000	4500
Gate Oxide	Å	80	100	120
Poly	Å	3500	4000	4500
STI Depth	Å	3500	4000	4500
Poly ReOx	Å	400	500	600
Trench Liner Ox	Å	400	500	600
TEOS Ox 1	Å	3500	4000	4500
Metal One	Å	7000	7500	8000
TEOS Ox 2	Å	3500	4000	4500
Metal Two	Å	7000	7500	8000

SUMMARY

The numbers found from these hand calculations should be close to the actual values. SUPREM simulations will give more accurate results, but the hand calculations are useful for comparison and trouble shooting the simulation. Actual factory values have a target, USL and LSL due to processing variations.



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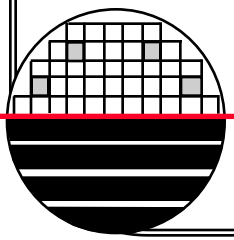
1. Silicon Processing for the VLSI Era, Volume 1 – Process Technology, 2nd, S. Wolf and R.N. Tauber, Lattice Press.
2. The Science and Engineering of Microelectronic Fabrication, Stephen A. Campbell, Oxford University Press, 1996.



HOMEWORK – HANDCALC FOR ADV-CMOS

1. Why is 1E16 cm-3 well doping too low for this process?

2. Why is 5 volts supply too high for this process?

3. Adding another photo level will allow for separate VT adjust implants (no blanket implant). What will the VT adjust implant dose be for each transistor?