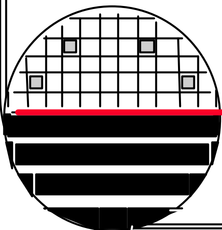
Dynamic Random Access Memory
DRAM

Bill Polinsky
Micron Technology, Boise, Idaho
Dr. Lynn Fuller
Motorola Professor
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041
LFFEEE@rit.edu

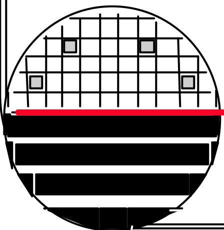


8-28-2001 lec_dram.ppt

© Dr. Lynn Fuller, Motorola Professor

OUTLINE

- Introduction
- Memory Organization
- DRAM Basics
- Capacitor Classification
- Tantalum PentaOxide Capacitor
- $(Ba,Sr)TiO_3$ (BST) Capacitor
- Single Layer Nitride Capacitor
- Salicide Bridged Trench Capacitor
- SOI DRAM
- Future of DRAM
- References



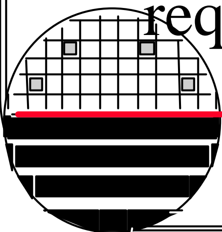
INTRODUCTION

Read-Only Memories (ROMs) - These are used to store information that will not change during the life of the system. They are permanently programmed during manufacture.

Nonvolatile read-write Memories (EPROM, EEPROM) - These devices retain the information stored in them when the power is turned off. They can be erased but usually much slower than they can be written. The number of erase/write cycles may be limited.

Dynamic Random Access Memories (DRAMs) - Information is stored as charge on a capacitor. The stored charge will eventually leak away so DRAMs must be periodically refreshed. Typically DRAMs are refreshed every 5-50 milli seconds. One transistor one capacitor per cell.

Static Random Access Memories (SRAM) - These devices store information in two cross-coupled inverters. Such a memory does not need to be refreshed. CMOS SRAM is low power. The SRAM cell requires six transistors making it fewer bits per chip than DRAM.



MEMORY ORGANIZATION

A_0
.
A_J

Row
Address
Bits

Row decoder

2^0

2^J

Word Line

Storage Cell

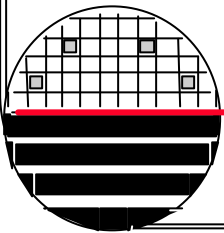
Bit Line

sense amplifiers/drivers

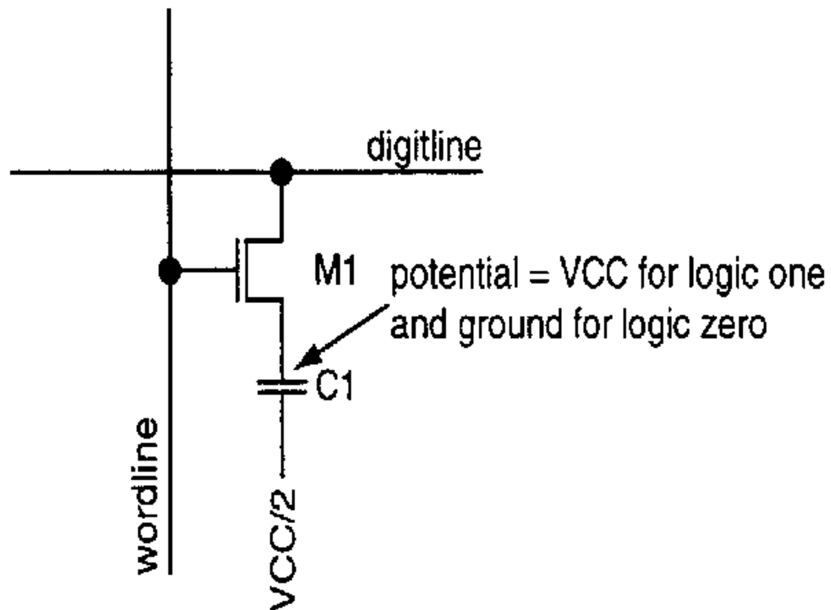
Column
Address bits

Column decoder

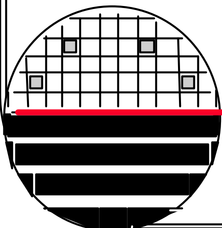
Input/output



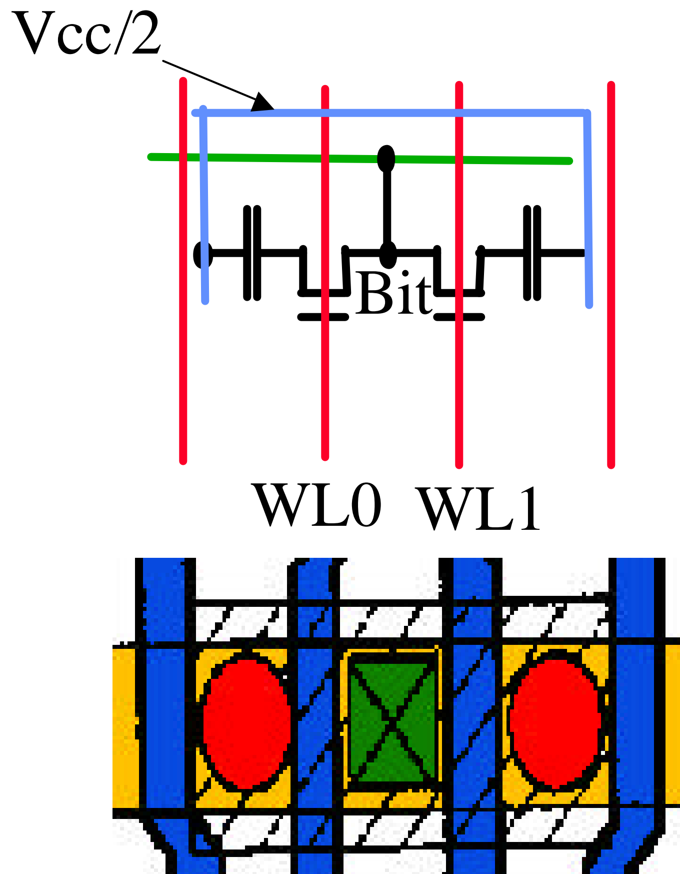
DRAM BASICS

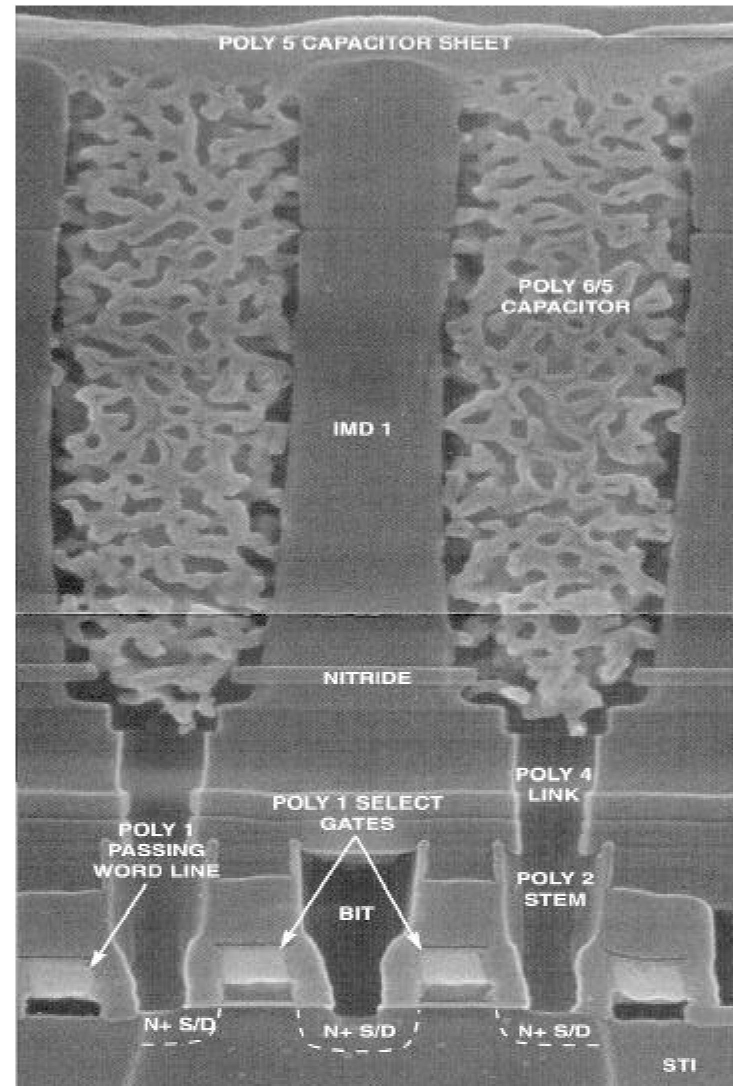


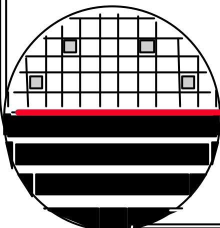
- A DRAM memory cell is formed with one transistor and one capacitor. Referred to as a 1T1C cell.
- Storing a logic ONE requires a voltage of +Vcc/2 across C1.
- Storing a logic ZERO requires a voltage of -Vcc/2 across C1.
- Various leakage paths cause the capacitor to slowly deplete charge.
- The capacitor needs to be refreshed periodically, which makes the DRAM dynamic rather than static.
- Typical refresh rates are every 5-50 msec



TWO DRAM STORAGE CELLS

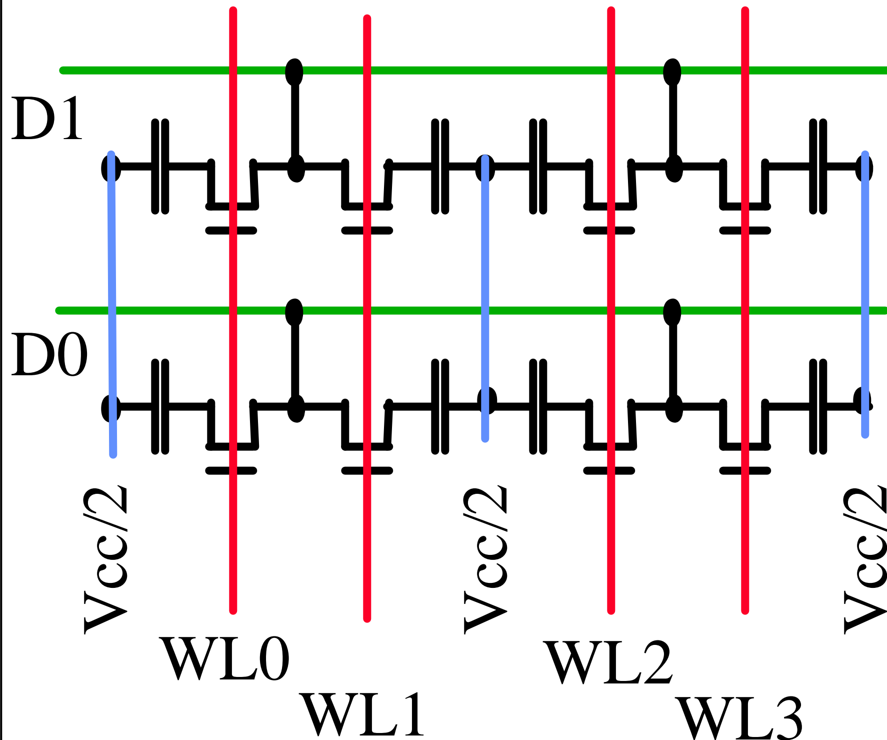






© Dr. Lynn Fuller, Motorola Professor

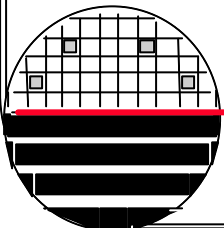
OPEN DIGITLINE MEMORY ARRAY



The memory bit transistor gate is connected to a word line (column)

A memory array is a quantity of 1T1C cells along a given digit line (row). None of the cells connected to a given digit line share a common word line.

Only one word line at a time is activated.



READ OUT AMPLIFIER

D1

D0

Vcc/2

C1

Vcc/2

Vcc/2

WL0

WL1

WL2

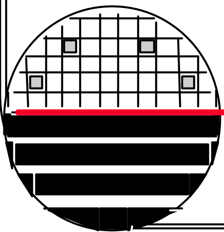
WL3

D1 Out

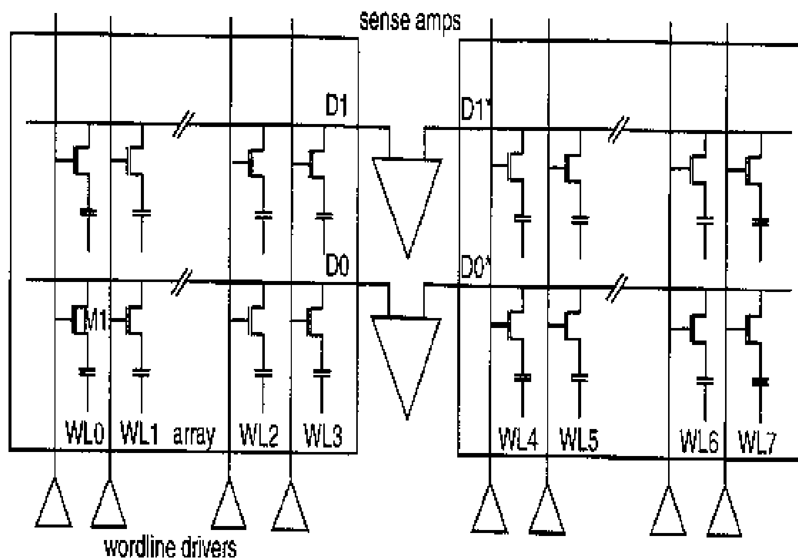
D0 Out

Vref

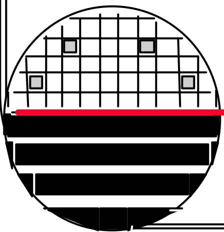
If a 1 was stored in C1 then when WL0 goes high D0 will go higher. If it is higher than Vref D0 Out will be high. The problem is that the voltage on D0 only increases a small amount because the capacitance of the digit line is large compared to C1



SIMPLE ARRAY



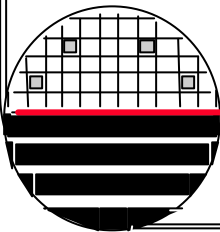
- Accessing the DRAM cell results in charge sharing between the capacitor and the digitline.
- This causes the digitline voltage to either increase or decrease for a ONE or ZERO on the capacitor.
- This causes a differential in voltage between two digitlines, D0 and D0*.
- The voltage difference can be "sensed" and the correct logic level can be determined.



SENSE AMPLIFER DETAILS

Q7 is turned on with signal ϕp precharging the two digit lines to Vdd/2

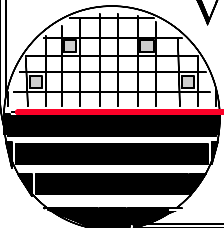
Note: the memory is organized into two arrays so that one can be used as the reference for the other. (with basically identical digit line capacitance)



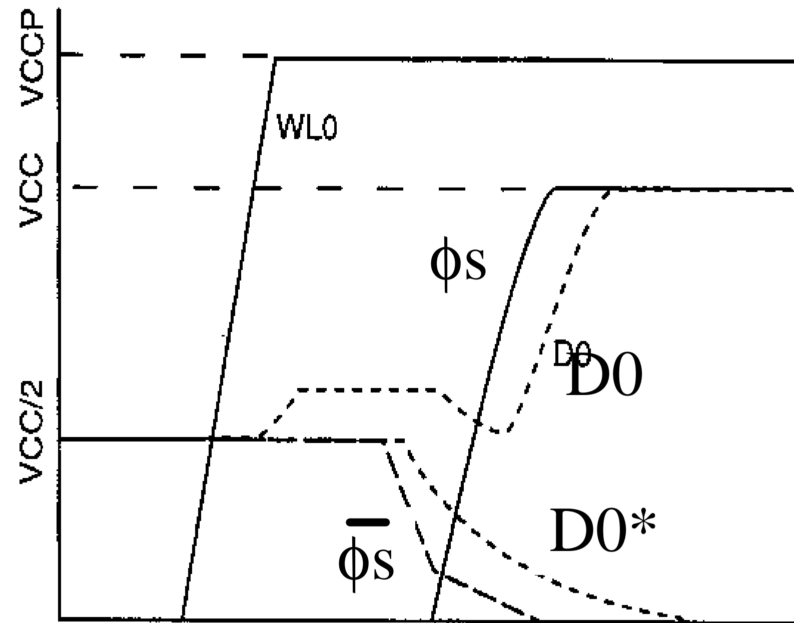
SENSE AMPLIFIER DETAILS

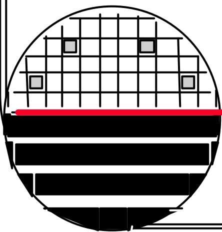
Φs goes high and the data in the selected memory cell is sensed. The word line WL0 goes high and the charge on selected capacitor C0 is shared with the capacitance of the digit line D0. If a "1" was stored in C0 the voltage on D0 will initially be a little higher than Vdd/2. The voltage on the reference digit line will initially be Vdd/2. The crosscoupled inverters amplify these starting voltage and bring the digit line D0 to Vdd and D0* to zero volts. The capacitor C0 is recharged (refreshed) at the same time it is read.

If a "0" was stored in C0 the voltage on D0 will initially be a little lower than Vdd/2. The crosscoupled inverters bring D0 to zero volts, refreshing C0 and providing a one for an output on D0*.



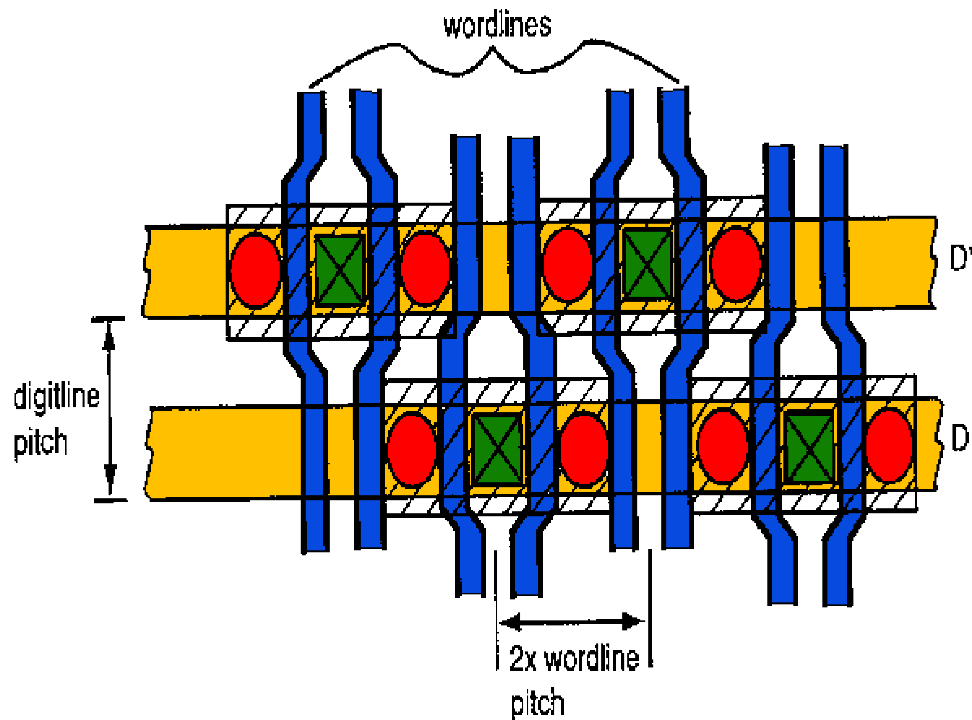
SENSE AMPLIFER WAVEFORMS



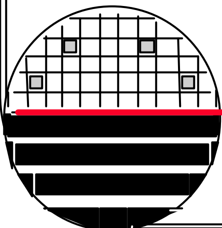


Rochester Institute of Technology
Microelectronic Engineering

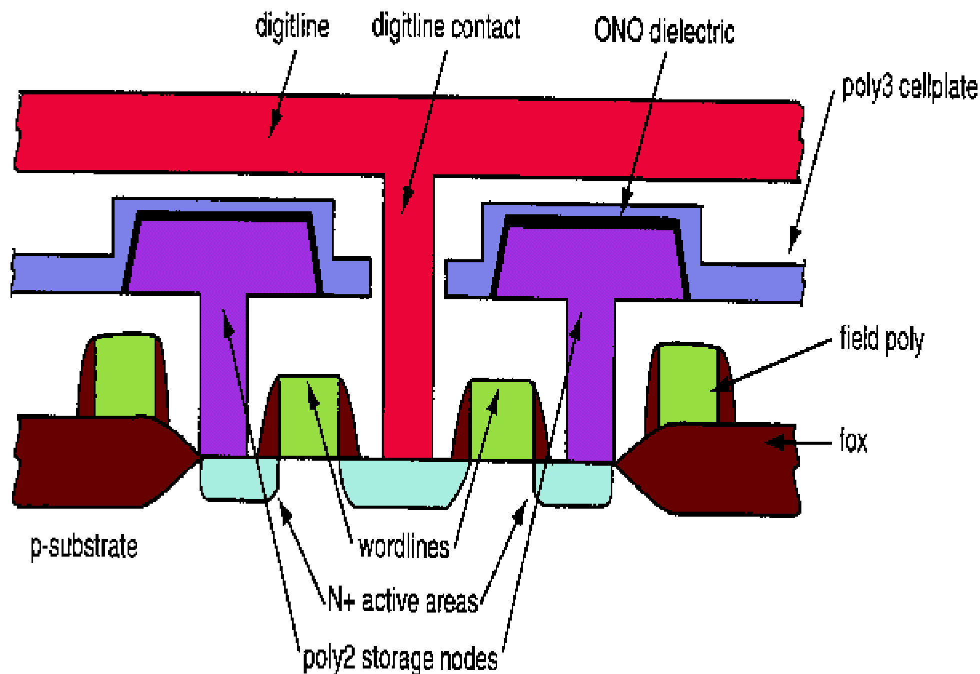
LAYOUT OF BASIC CELL



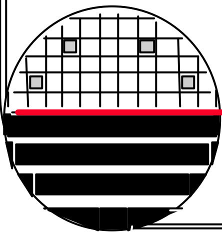
Eight Cells - Each red oval shape is a capacitor. The blue poly wordlines form transistors between the green rectangular connection to the digitline.



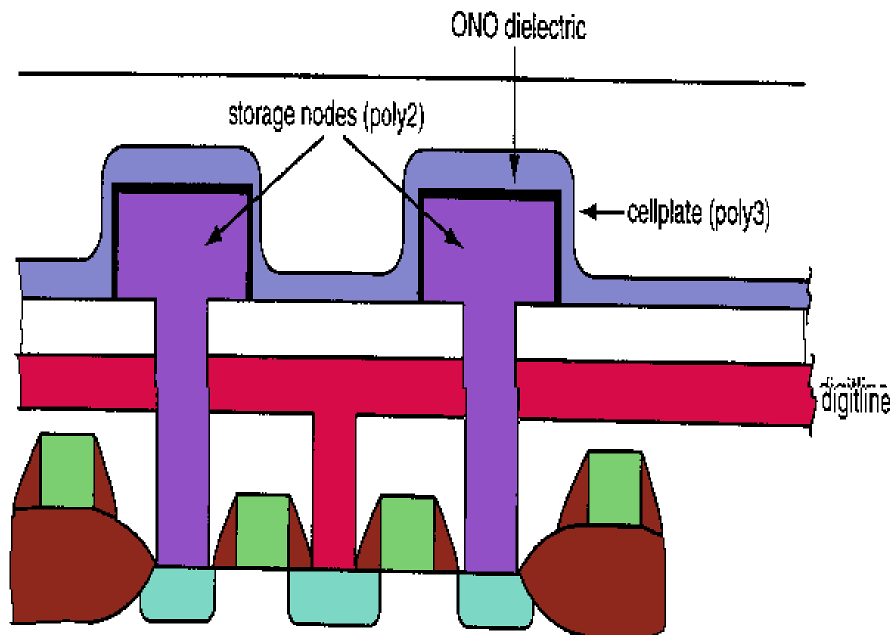
BURIED CAPACITOR CELL



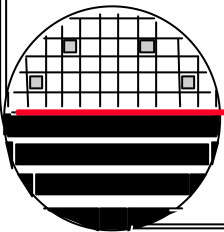
- Digitline (bitline) is made of Aluminum with a Tungsten plug.
- Capacitor top and bottom plate is made from poly-silicon.
- The top plate (poly 3) forms the cell plate and is shared by all capacitors.
- The capacitor shape can be a rectangle or concentric cylinders.
- The ONO dielectric is optimized to achieve low leakage and maximum capacitance.
- The ONO must be able to handle fields caused by the maximum DRAM operating voltage. For this reason the cell plate is biased at +Vcc/2.



BURIED DIGITLINE CELL



- This type of cell is called a COB (Capacitor over Bitline) or buried digitline configuration.
- The digitline is very close to the surface of silicon, making the digitline pitch small and the contact is easier to produce.
- However, the capacitor contact is very hard to produce because the contact has to be cut in between the digitlines, which are at near minimum pitch to begin with.



© Dr. Lynn Fuller, Motorola Professor

BURIED DIGITLINE CELL

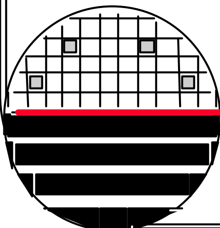
POLY 5 COMMON CAPACITOR PLATE

POLY 4 INDIVIDUAL CAPACITOR PLATE

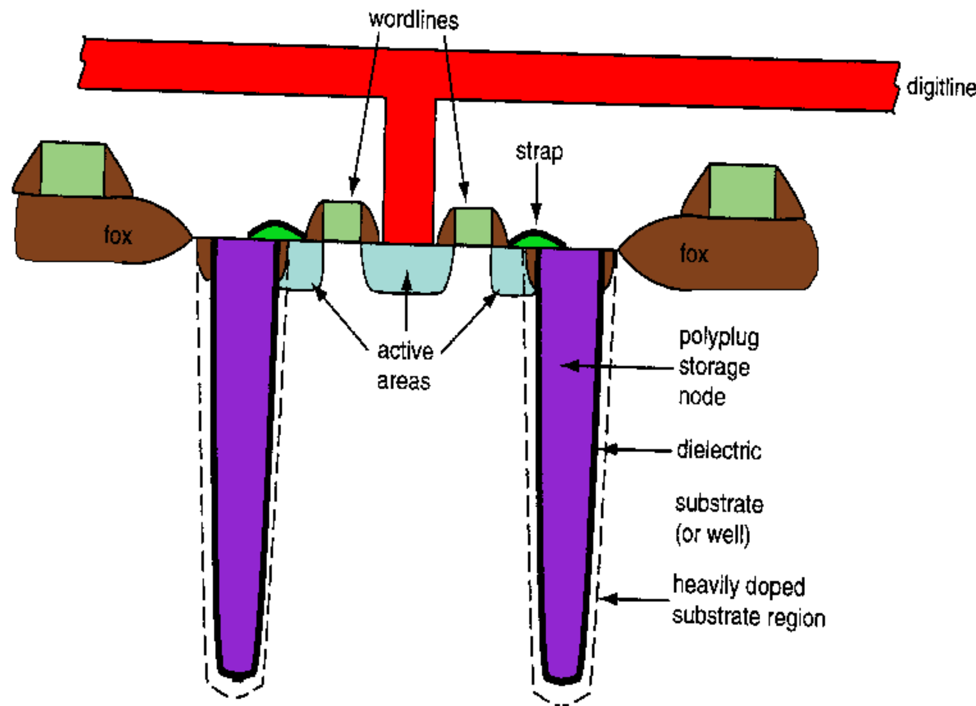
POLY 4 STEM INTERCONNECT

POLYCIDE 3 BIT LINE

POLY 2 INTERCONNECT



TRENCH CAPACITOR CELL



•Trench capacitors are formed by etching deep holes into the silicon substrate.

•The trench is coated with a dielectric material, eg. ONO or Nitride.

•The storage node if formed by depositing doped poly-silicon into the trench.

•Contact from the transistor to the capacitor is done with a conductive strap.

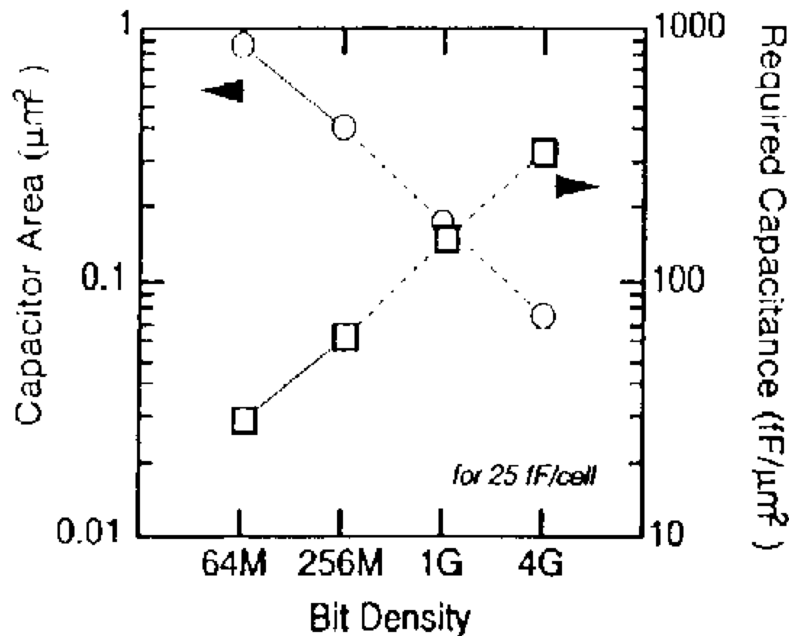
•The substrate serves as a common node for all of the capacitors, which prevents the use of a +Vcc/2 bias.

•For Gbit and beyond DRAMs the trench will be too difficult to etch, the aspect ratio will be too great for acceptable capacitance.

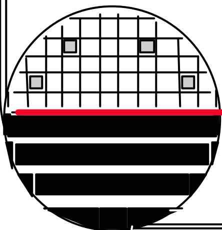
•Advantage of the trench capacitor is that the DRAM structure will have less topology than other cell structures.

CAPACITOR AREA AND REQUIRED CAPACITANCE

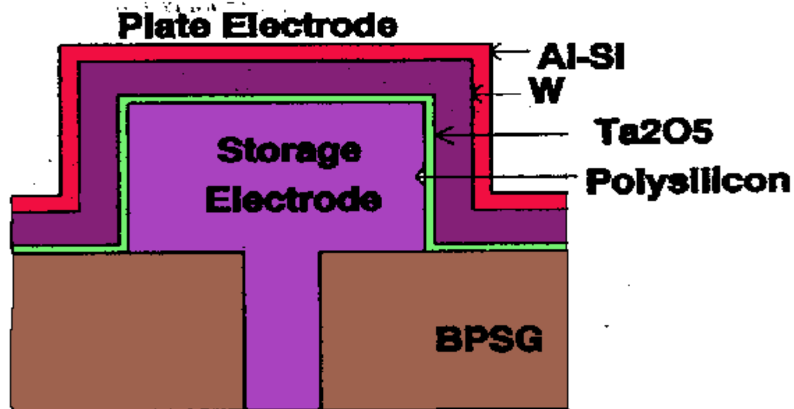
Shows the trend of capacitor area and required capacitance.



- Thermally robust Ta2O5 (Tantalum PentaOxide) has been attractive for DRAM capacitors.
- Ta2O5 has a dielectric constant in the range of 16-40.
- Ta2O5 has good conformal step coverage when deposited using CVD.
- (Ba,Sr)TiO3 Is Another Alternative Capacitor.

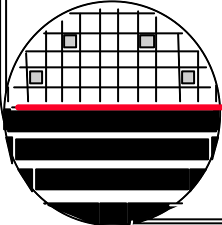


TANTALUM PENTAOXIDE CAPACITOR



Capacitance of more than 90fF/cell and leakage current less than 2x10^-15 A/cell is obtained by applying a WNx/poly-si top electrode with a rugged poly-si surface (projection area = 0.4um) with an effective oxide thickness of 3.5 nm.

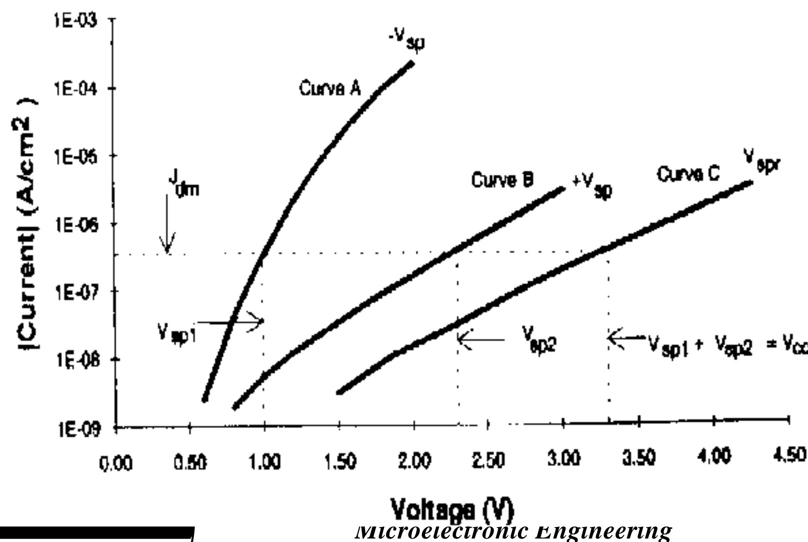
As deposited Ta2O5 is known to be very leaky. The leakage current is reduced by annealing the film in UV-O3 at 300 C and dry O2 at 800 C. Annealing in O2 forms a thin layer of SiO2 over the poly and provides a barrier to carrier flow. The ozone provides atomic oxygen to fill vacancies in the film.



BIAS OPTIMIZATION FOR TANTALUM PENTAOXIDE

At Vcc of 3.3 volts the maximum leakage current can be reduced by two orders of magnitude when Vp is changed from 1.65 volts (conventional Vp=Vcc/2) to a Vp of 1.0 volts.

By using a bias Vp = 1.0 volts, Vspr is the maximum Vcc that can be applied for a given current magnitude.

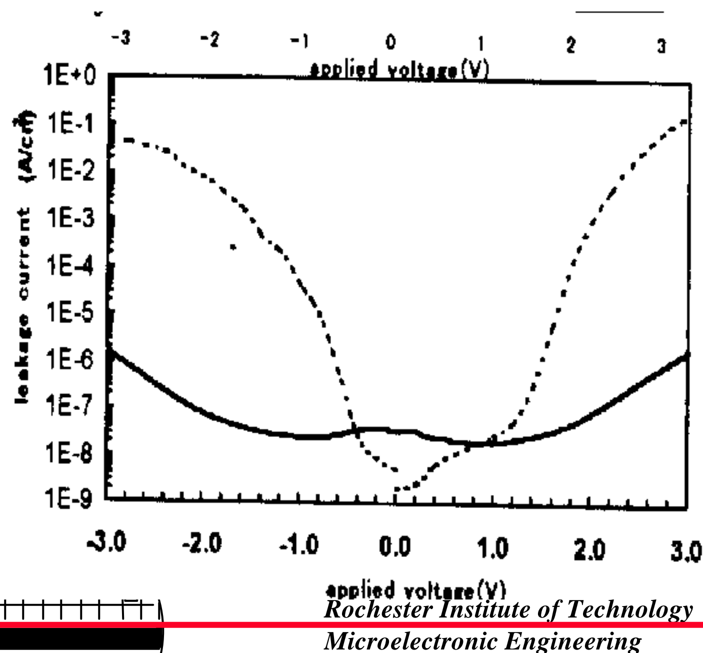


Using a bias optimization scheme can greatly improve the quality of the capacitor by reducing leakage current at a given supply voltage, VCC.

EPITAXIAL (Ba,Sr)TiO3 CAPACITOR

As well as a high dielectric constant, low leakage current in very thin capacitors with a epitaxial (Ba,Sr)TiO3 dielectric.

To achieve this superior performance the film is because of the heteroepitaxial technique used to deposit the film.



Their superior performance is attributed to the appropriate lattice deformation caused by the lattice constant mismatch between BSTO and SRO and the cleanliness of their hetroepitaxial interfaces.

HETEROEPITAXY

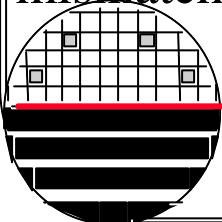
Their superior performance is attributed to the appropriate lattice deformation caused by the lattice constant mismatch between BSTO and SRO and the cleanliness of their hetroepitaxial interfaces.

Heteroepitaxial growth is classified as the growth on dissimilar materials. Which means that the material being grown has a lattice mismatch from the underlying material.

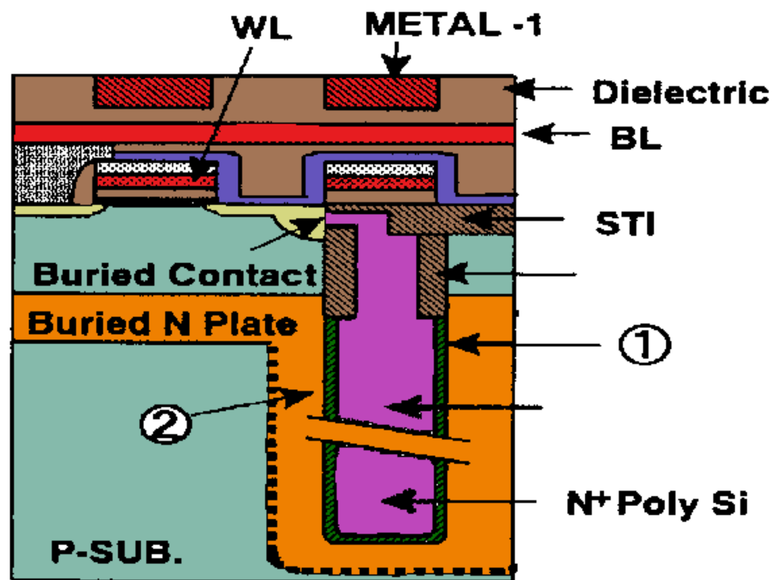
The heteroepitaxial growth in this case of (Ba,Sr)TiO3 thin film is classified as incommensurate growth.

Incommensurate growth is the production of thick layers that are not lattice matched to the substrate. The misfit between the two crystals must be accommodated by defects at or near the interface.

In this case, the mismatch is a plus to the capacitor, as a result of comparision between epitaxial and polycrystalline capacitors with identical dielectric thicknesses, the mismatched induced lattice deformation is highly effective to increase the dielectric constant of the film.

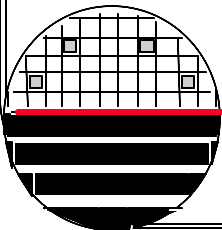


SINGLE LAYER NITRIDE CAPACITOR

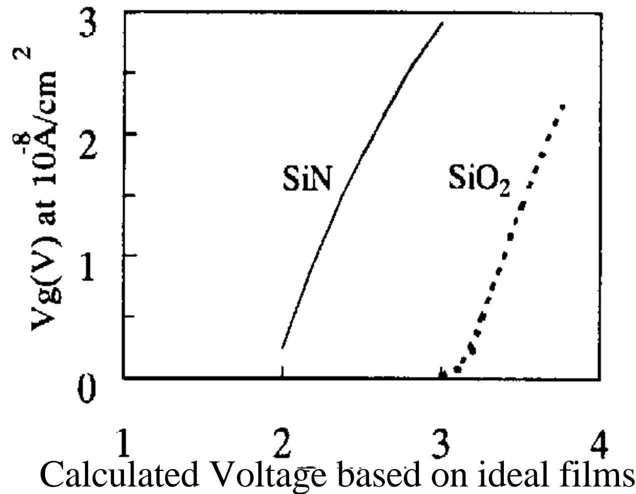


Key Technology for increasing capacitance for the Gbit era trench capacitors is a thinner dielectric film with low leakage current.

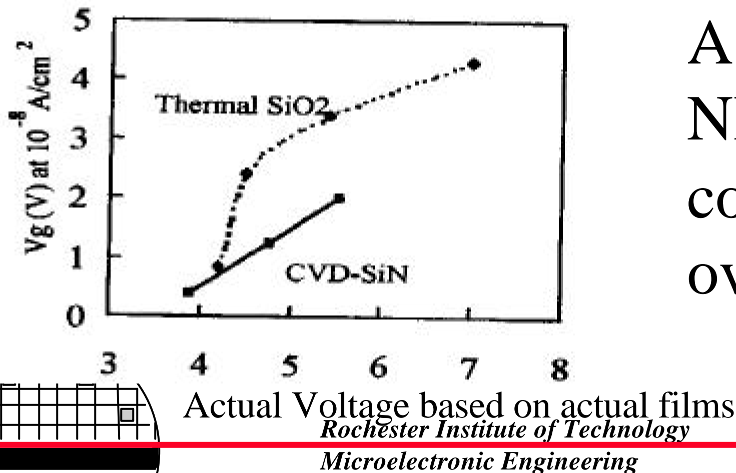
SiN is promising for material that has low leakage current and the potential to be thinned further and it has a high dielectric constant.



SINGLE LAYER NITRIDE CAPACITOR



Calculated Voltage based on ideal films



Actual Voltage based on actual films

SiN Film has a greater potential for thickness reduction because of its higher dielectric constant. Nitride ε~7 Whereas SiO2 ε~4-5.

However, the actual leakage current in SiN film is larger than in Si02 films because of bonds introduced in deposition.

A novel SiN-CVD technology using SiCl4-NH3 system was developed instead of conventional SiH2Cl2-NH3 system to overcome this subject.

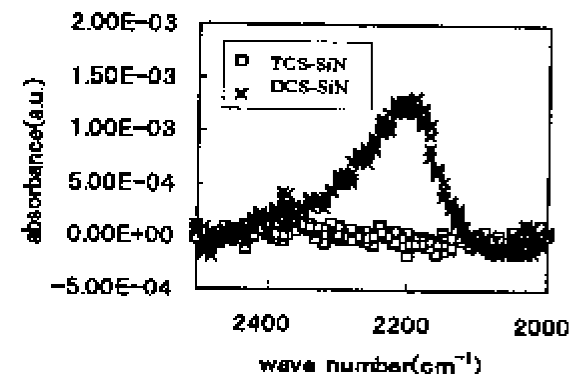
SINGLE NITRIDE LAYER CAPACITOR BY NOVEL CVD

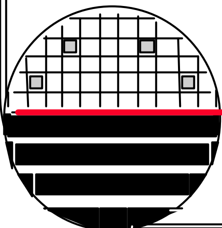
In order to improve the SiN film quality, the Si-H bond density has been reduced using this method; SiCl4-NH3 (TCS-SiN) as reactants.

SiCl4 has no Si-H molecular bond in itself.

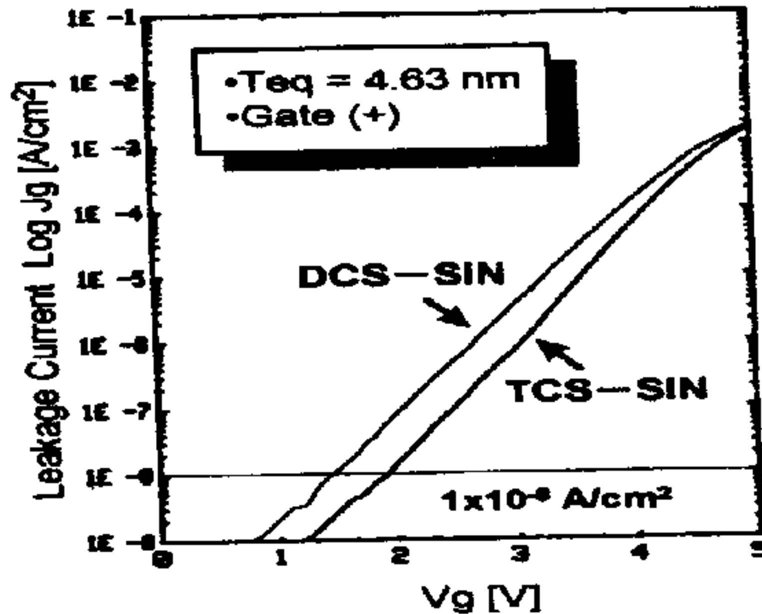
SiCl4 can react with NH3 at room temperature and form Si(NH2)4 or Si(NH)2 molecule, which has no Si-H bond.

A FT-IR measurement was done to find out how many Si-H bonds are present in the film. As shown in the figure, the Si-H bond that usually exists in conventional Nitride deposition cannot be detected.



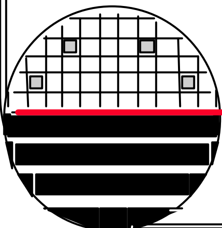


SINGLE NITRIDE LAYER CAPACITOR BY NOVEL CVD



This new Si-N (TCS) shows superior electrical characteristics over the conventional DCS Nitride deposition. At the required leakage current, the TCS capacitor can handle ~2 volts compared to the conventional ~1.3 volts with a dielectric thickness of 4.63 nm.

The equivalent oxide thickness is can be reduced below 4 nm which is a promising capacitor dielectric for the Gigabit era and beyond.



SALICIDE BRIDGED TRENCH CAPACITOR

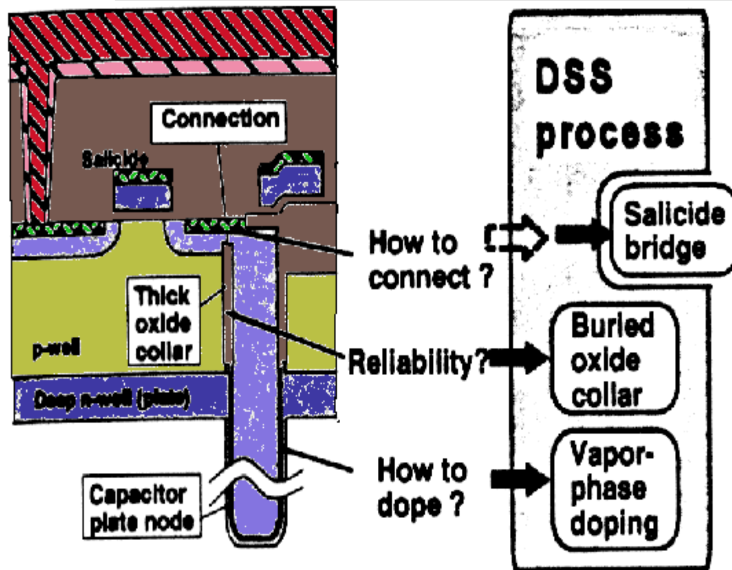
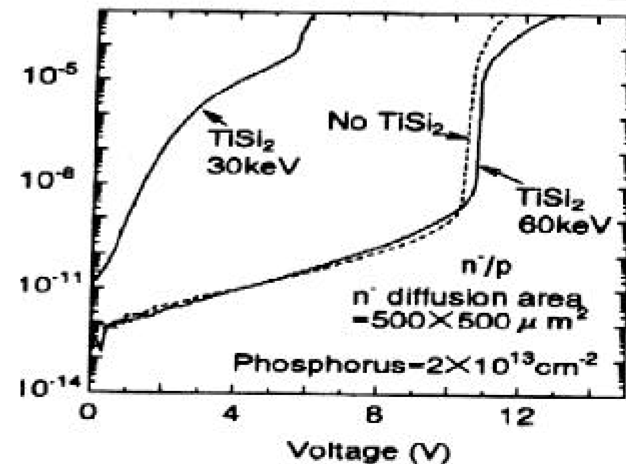


Fig. 1. Schematic cross-sectional view of a trench capacitor DRAM and key issues. The DSS technology is the solution to these issues.

The connection from capacitor to the transistor can be made with a salicide bridge on top of the conventional Drain connection.

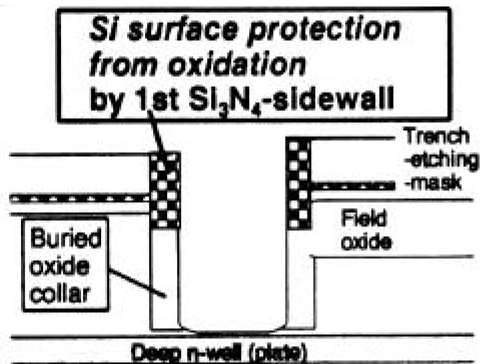
The salicide bridge provides a low series resistance path for current to flow through.

The salicide bridge does not increase the leakage current in the trench capacitor which is always a concern. When introducing new materials.

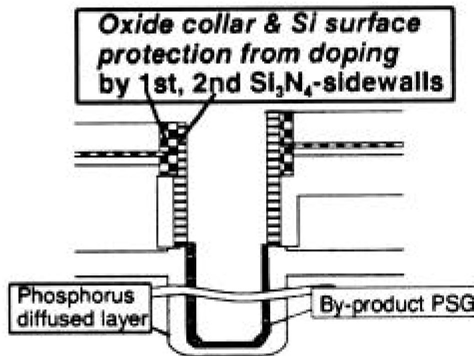


© Dr. Lynn Fuller, Motorola Professor

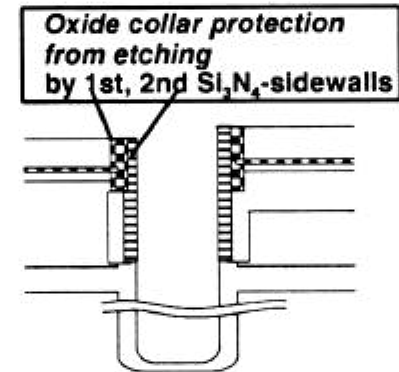
SALICIDE BRIDGED TRENCH CAPACITOR



(A) Buried oxide collar formation.



(B) Vapor-phase doping for capacitor-plate-node formation.



(C) By-product PSG removal with HF.

(D) 1st, 2nd Si_3N_4-sidewalls *removal* with HPO_3.

(E) Conventional trench formation and cell transistor formation.

Silicidation

The DSS process makes it possible to fabricate a self-aligned buried oxide collar and a salicide bridge over a thick oxide collar.

PATTERN BONDED SOI DRAM

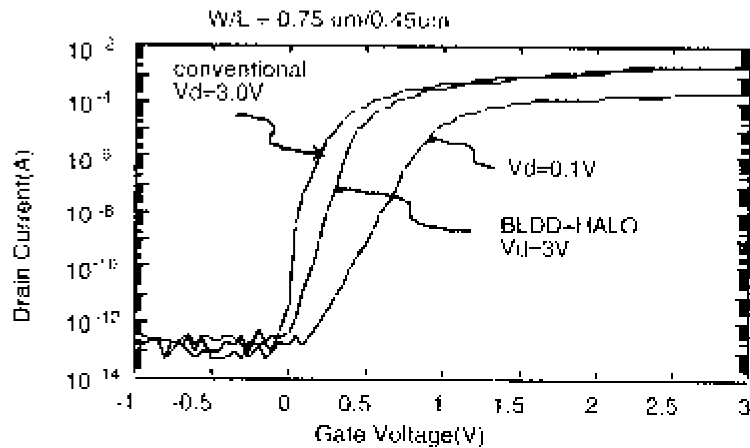


Fig. 10 DIBL characteristics of NMOS peripheral transistors

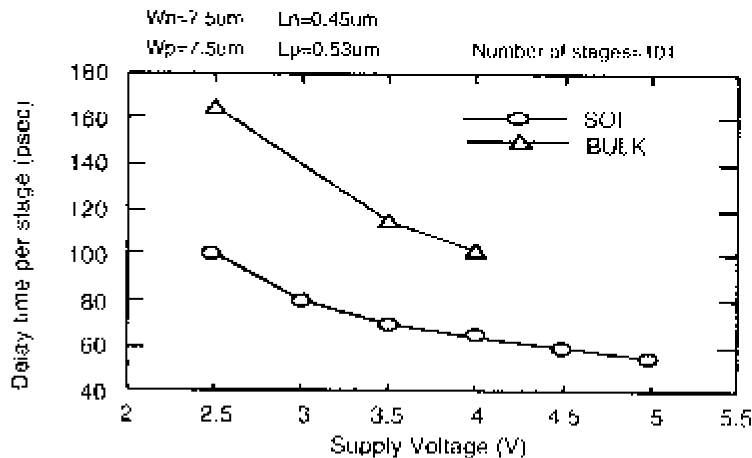


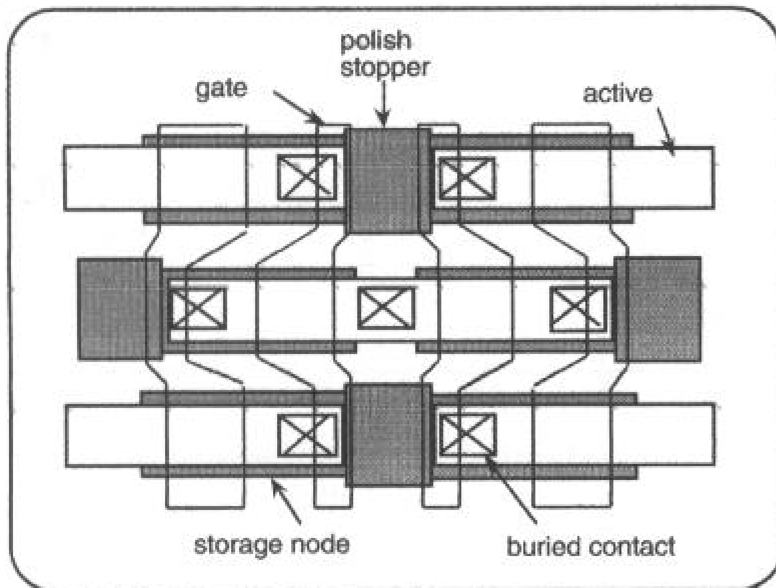
Fig. 11 The delay time per stage of ring oscillators

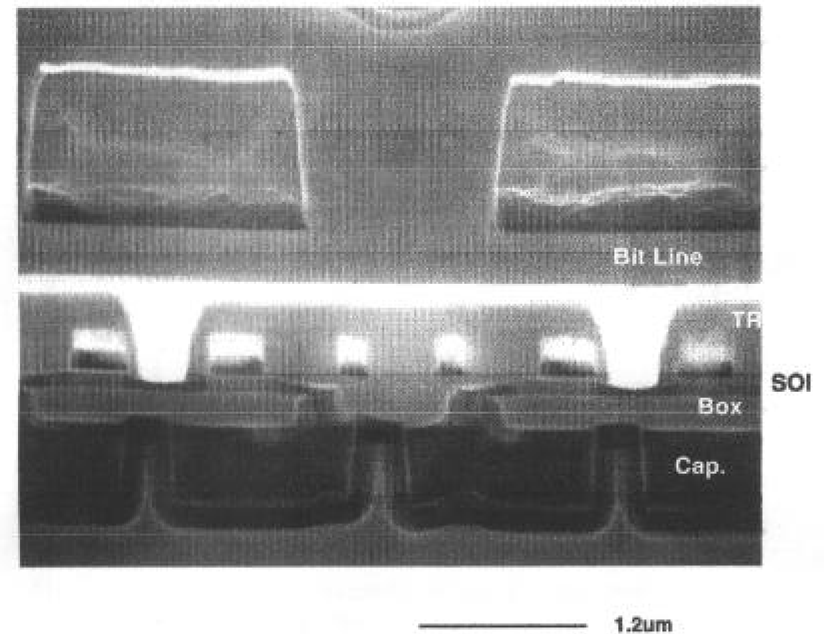
Previous reports of SOI DRAM described the limitation of scaling down due to short channel effects of the PMOS, and the LOCOS isolation scheme.

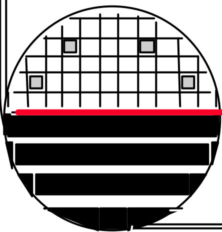
The process described here pattern bonded SOI (PBSOI) reduces negative effects, and reduces gate delay and leakage is just as good as conventional Bulk type DRAMs.

The PBSOI will enable higher speed DRAMs for future DRAM generations.

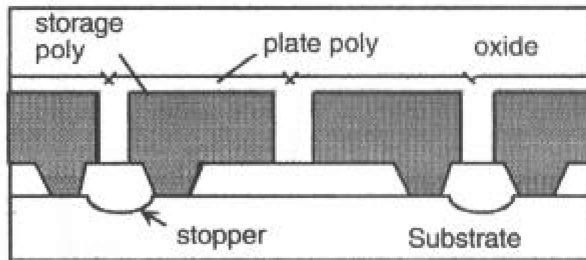
PATTERN BONDED SOI DRAM



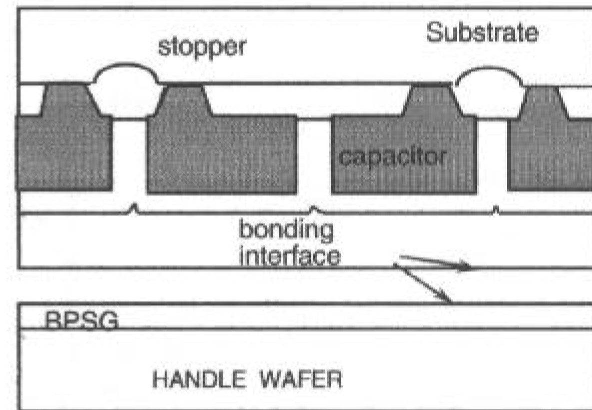




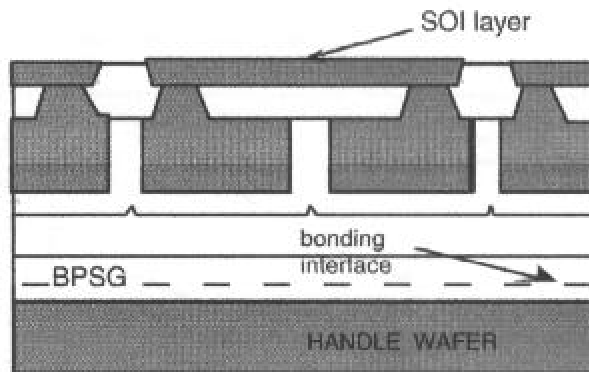
PATTERN BONDED SOI



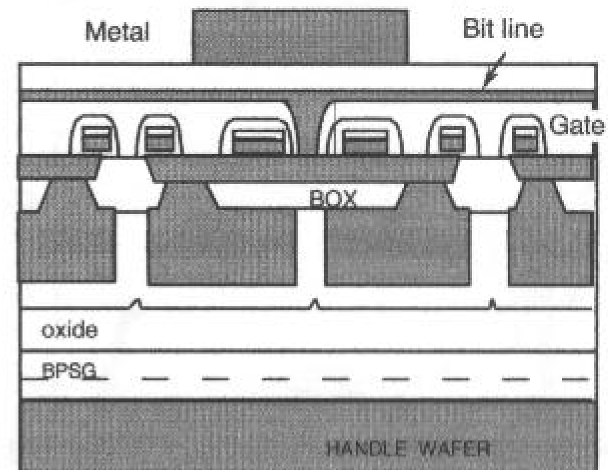
A. LOCOS stopper / capacitor Formation
/ Planarization for Wafer Bonding



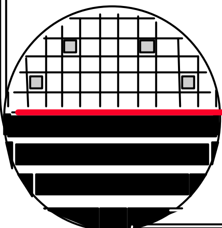
B. Wafer Bonding and Anneal



C. Grinding and Selective Silicon CMP
/ Shallow Trench Isolation



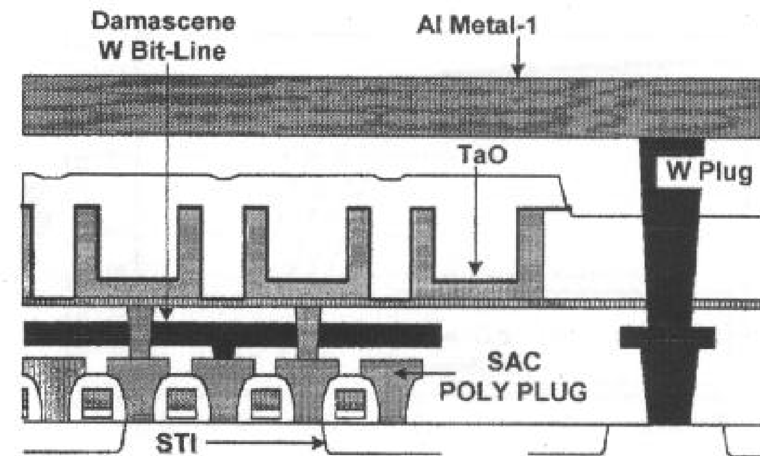
D. Gate Formation / Bit Line Damascene / Metallization

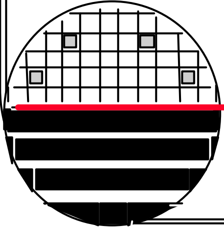


FUTURE OF DRAM

With increasing density of DRAM a trench type capacitor will not suffice do to increasing aspect ratio of trenches needed to have enough capacitance. The etch will just become impossible.

This will force the industry to use Capacitor over bitline (COB) schemes. With COB the capacitor size can increase by increasing size in the vertical direction, which itself poses many etch and planarization challenges. In the near future the dielectric will be Ta2O5 thin films due to its high dielectric constant and good film quality for small film thickness.

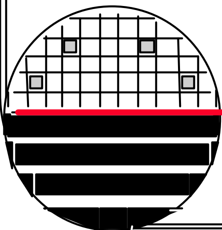




FUTURE OF DRAM

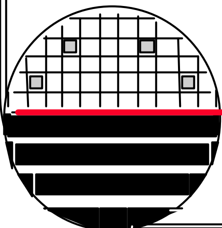
DRAM will move towards SOI formation to minimize floating body effects and minimize latchup.

DRAM will become less of a commodity with the introduction and manufacturability of embedded DRAM, that is DRAM on the same substrate as logic and microprocessors.



REFERENCES

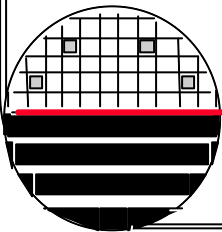
1. "State-of-the-art and future trends in DRAMS", Microelectronics Journal 27 (1996), C.G. Hwang, S.I. Lee and M.Y. Lee
2. "DRAM Plate Electrode Bias Optimization for Reducing Leakage Current in UV-O3 and O2 Annealed CVD Deposited Ta2O5 Dielectric Films", Transactions on Electron Devices, Vol. 42, No. 10, Sudhir K. Madan.
3. "Single Layer Nitride Capacitor Dielectric Film and High Concentration Doping Technology for 1Gb/4Gb Trench-Type DRAMs", IEDM 97-265, Shigehiko Saida, Tsutomu Sato, Ichiro Mizushima, Yoshio Ozawa and Yoshitaka Tsunashima.
4. "Epitaxial (Ba,Sr)TiO3 Capacitors with Extremely High Dielectric Constant for DRAM Applications", IEDM 97-257, N. Fukushima, K. Abe, M. Izuha, T. Schimizu and T. Kawakubo.
5. The Science and Engineering of Microelectronic Fabrication, Stephen Cambell p.355.



REFERENCES (CONTINUED)

.

6. “A Salicide-Bridged Trench Capacitor with a Double-Sacrificial-Si2N4 Sidewall (DSS) for High-Performance Logic-Embedded DRAMs:, IEDM 97-37, M.Togo, S.Iwao, H.Nobusawas,M.Hamada,K.Yoshida,N.Yasuzato and T.Tanigawa.
7. “A New Planer Stacked Technology (PST) for Scaled and Embedded DRAMS”, IEDM 1996, S.P. Sim, W.Lee,Y.Ohu,H.Choe, J.Kim, H. Ban, I.Kim, Y. Chang, Y. Lee, H.Kang, U.Chung, C. Choi and C.Hwang.
8. “Advanced Integration Technology for a Highly Scalable SOI DRAM with SOC”, IEDM 96, Il-Kwon Kim, Woo-Tag Kang, Joon-Hee Lee, Sunil Yu, Sang Lee, Kyehee Yeom.



HOMEWORK - MEMORY DEVICES